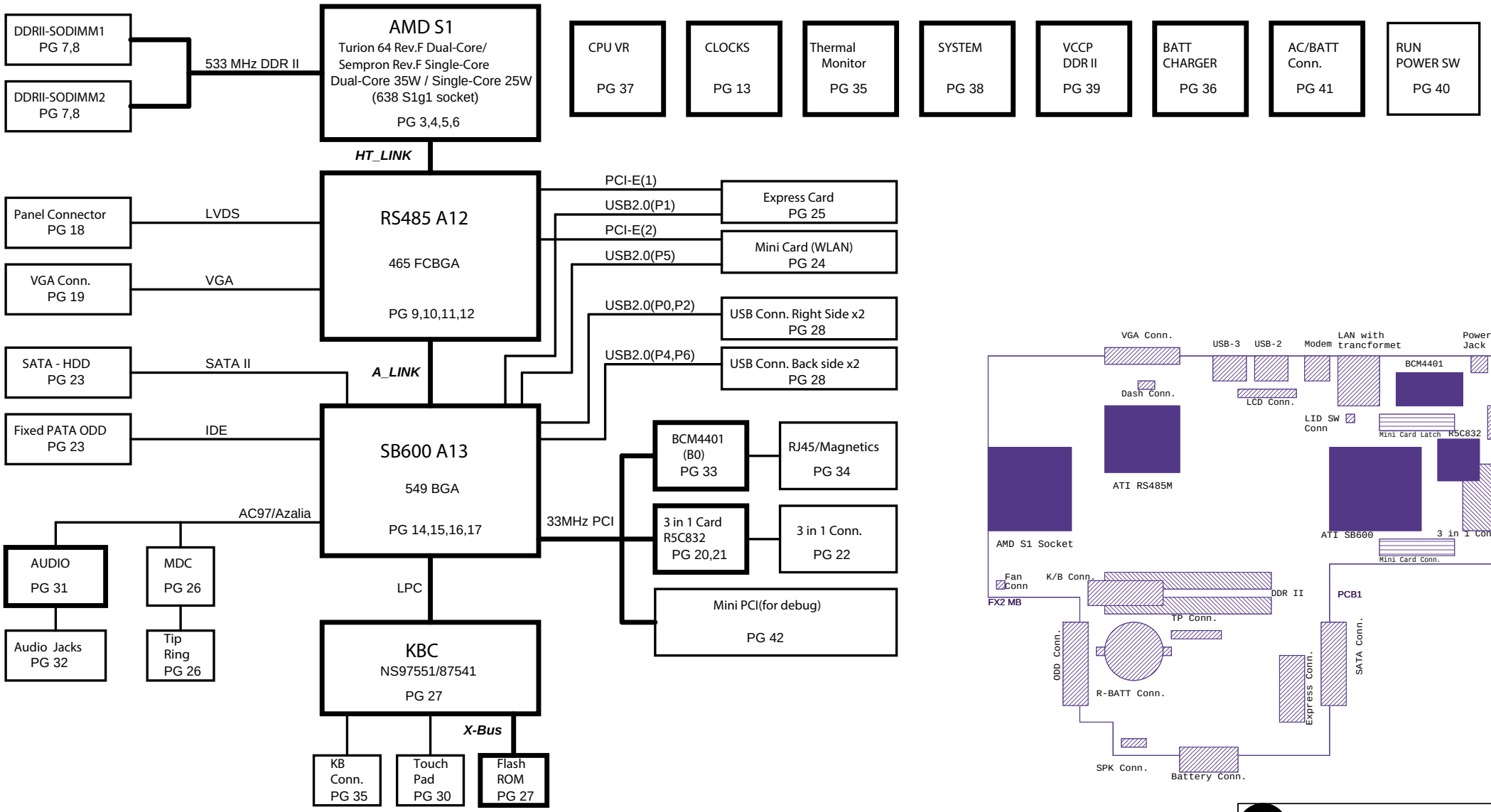
DELL Inspiron 1501 / PP23LA / DA0FX2MBAD7

REV: D



QUANTA COMPUTER

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QUANTA COMPUTER

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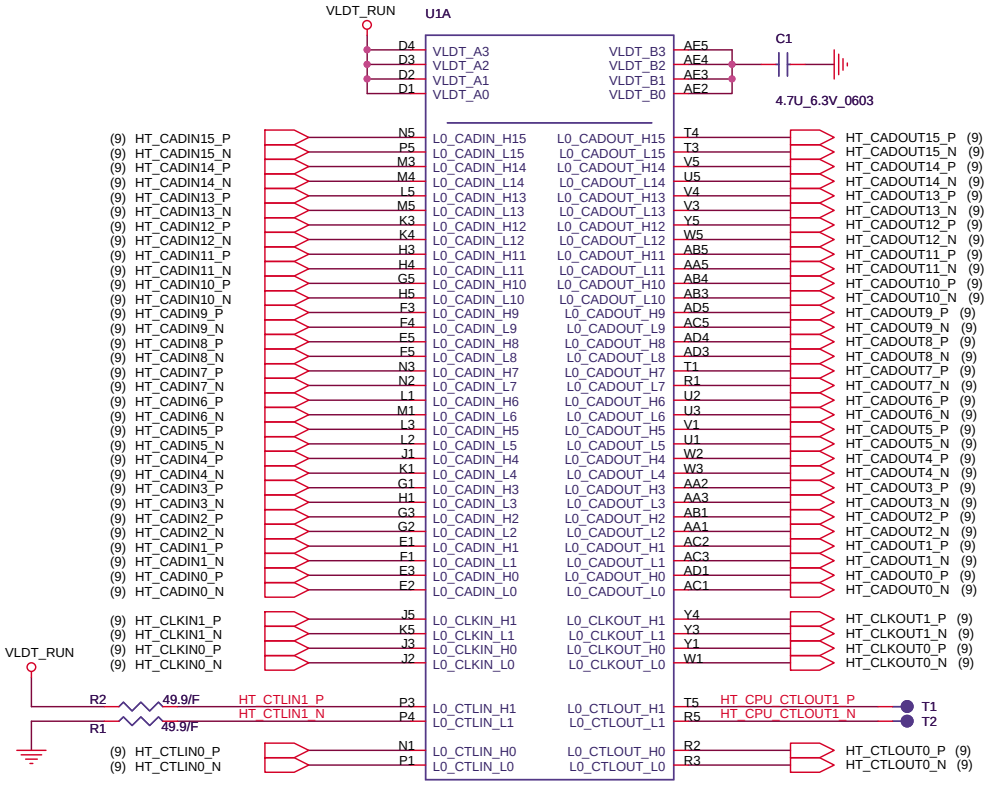
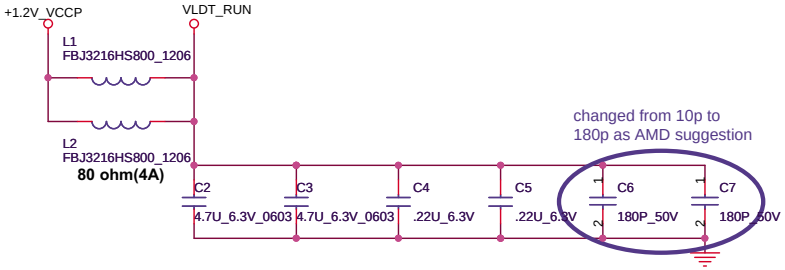
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Athlon 64 S1
Processor Socket



LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

QUANTA COMPUTER

Title	ATHLON64 HT I/F	
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Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

PLACE THEM CLOSE TO CPU WITHIN 1"

for +0.9V_DDR_VTT feedback

+1.8V_SUS

R3 2K/F

R4 2K/F

CPU_M_VREF

C8 .1U_10V

C9 1000p_50V

(39) VTT_SENSE

VTT_SENSE

C677 470P_50V

R6 39.2/F

R5 39.2/F

R566 0

+0.9V_DDR_VTT

U1B

MEMVREF, VTT_SENSE, MEMZN, MEMZP

VTT1 VTT2 VTT3 VTT4 VTT5 VTT6 VTT7 VTT8 VTT9

PMA0_CS_L3 PMA0_CS_L2 PMA0_CS_L1 PMA0_CS_L0

MA0_CLK_H2 MA0_CLK_L2 MA0_CLK_H1 MA0_CLK_L1

M_CLKOUT1 (7) M_CLKOUT1# (7) M_CLKOUT0 (7) M_CLKOUT0# (7)

PMB0_CS_L3 PMB0_CS_L2 PMB0_CS_L1 PMB0_CS_L0

MB0_CLK_H2 MB0_CLK_L2 MB0_CLK_H1 MB0_CLK_L1

M_CLKOUT4 (7) M_CLKOUT4# (7) M_CLKOUT3 (7) M_CLKOUT3# (7)

MB_CKE1 MB_CKE0 MA_CKE1 MA_CKE0

MB0_ODT1 MB0_ODT0 MA0_ODT1 MA0_ODT0

M_ODT3 (7,8) M_ODT2 (7,8) M_ODT1 (7,8) M_ODT0 (7,8)

MA_ADD15 MA_ADD14 MA_ADD13 MA_ADD12 MA_ADD11 MA_ADD10 MA_ADD9 MA_ADD8 MA_ADD7 MA_ADD6 MA_ADD5 MA_ADD4 MA_ADD3 MA_ADD2 MA_ADD1 MA_ADD0

MB_ADD15 MB_ADD14 MB_ADD13 MB_ADD12 MB_ADD11 MB_ADD10 MB_ADD9 MB_ADD8 MB_ADD7 MB_ADD6 MB_ADD5 MB_ADD4 MB_ADD3 MB_ADD2 MB_ADD1 MB_ADD0

M_B_A[0..15] (7,8)

MA_BANK2 MA_BANK1 MA_BANK0

MB_BANK2 MB_BANK1 MB_BANK0

M_B_BS#2 (7,8) M_B_BS#1 (7,8) M_B_BS#0 (7,8)

PMA_RAS_L PMA_CAS_L PMA_WE_L

MB_RAS_L MB_CAS_L MB_WE_L

M_B_RAS# (7,8) M_B_CAS# (7,8) M_B_WE# (7,8)

DDR II: CMD/CTRL/CLK

Athlon 64 S1
Processor Socket

U1C

(7) M_B_DQ[0..63]

MB_DATA63 MB_DATA62 MB_DATA61 MB_DATA60 MB_DATA59 MB_DATA58 MB_DATA57 MB_DATA56 MB_DATA55 MB_DATA54 MB_DATA53 MB_DATA52 MB_DATA51 MB_DATA50 MB_DATA49 MB_DATA48 MB_DATA47 MB_DATA46 MB_DATA45 MB_DATA44 MB_DATA43 MB_DATA42 MB_DATA41 MB_DATA40 MB_DATA39 MB_DATA38 MB_DATA37 MB_DATA36 MB_DATA35 MB_DATA34 MB_DATA33 MB_DATA32 MB_DATA31 MB_DATA30 MB_DATA29 MB_DATA28 MB_DATA27 MB_DATA26 MB_DATA25 MB_DATA24 MB_DATA23 MB_DATA22 MB_DATA21 MB_DATA20 MB_DATA19 MB_DATA18 MB_DATA17 MB_DATA16 MB_DATA15 MB_DATA14 MB_DATA13 MB_DATA12 MB_DATA11 MB_DATA10 MB_DATA9 MB_DATA8 MB_DATA7 MB_DATA6 MB_DATA5 MB_DATA4 MB_DATA3 MB_DATA2 MB_DATA1 MB_DATA0

MA_DATA63 MA_DATA62 MA_DATA61 MA_DATA60 MA_DATA59 MA_DATA58 MA_DATA57 MA_DATA56 MA_DATA55 MA_DATA54 MA_DATA53 MA_DATA52 MA_DATA51 MA_DATA50 MA_DATA49 MA_DATA48 MA_DATA47 MA_DATA46 MA_DATA45 MA_DATA44 MA_DATA43 MA_DATA42 MA_DATA41 MA_DATA40 MA_DATA39 MA_DATA38 MA_DATA37 MA_DATA36 MA_DATA35 MA_DATA34 MA_DATA33 MA_DATA32 MA_DATA31 MA_DATA30 MA_DATA29 MA_DATA28 MA_DATA27 MA_DATA26 MA_DATA25 MA_DATA24 MA_DATA23 MA_DATA22 MA_DATA21 MA_DATA20 MA_DATA19 MA_DATA18 MA_DATA17 MA_DATA16 MA_DATA15 MA_DATA14 MA_DATA13 MA_DATA12 MA_DATA11 MA_DATA10 MA_DATA9 MA_DATA8 MA_DATA7 MA_DATA6 MA_DATA5 MA_DATA4 MA_DATA3 MA_DATA2 MA_DATA1 MA_DATA0

M_A_DQ[0..63] (7)

(7) M_B_DM[0..7]

MB_DM7 MB_DM6 MB_DM5 MB_DM4 MB_DM3 MB_DM2 MB_DM1 MB_DM0

MA_DM7 MA_DM6 MA_DM5 MA_DM4 MA_DM3 MA_DM2 MA_DM1 MA_DM0

M_A_DM[0..7] (7)

MB_DQS_H7 MB_DQS_L7 MB_DQS_H6 MB_DQS_L6 MB_DQS_H5 MB_DQS_L5 MB_DQS_H4 MB_DQS_L4 MB_DQS_H3 MB_DQS_L3 MB_DQS_H2 MB_DQS_L2 MB_DQS_H1 MB_DQS_L1 MB_DQS_H0 MB_DQS_L0

MA_DQS_H7 MA_DQS_L7 MA_DQS_H6 MA_DQS_L6 MA_DQS_H5 MA_DQS_L5 MA_DQS_H4 MA_DQS_L4 MA_DQS_H3 MA_DQS_L3 MA_DQS_H2 MA_DQS_L2 MA_DQS_H1 MA_DQS_L1 MA_DQS_H0 MA_DQS_L0

(7) M_B_DQS[0..7]

(7) M_B_DQS#[0..7]

(7) M_A_DQS[0..7]

(7) M_A_DQS#[0..7]

DDR: DATA

Athlon 64 S1
Processor Socket

To SODIMM socket B (Far)

To SODIMM socket A (near)

+0.9V_DDR_VTT

C10 4.7U_6.3V_0603 C11 4.7U_6.3V_0603 C12 4.7U_6.3V_0603 C13 4.7U_6.3V_0603 C14 .22U_6.3V C15 .22U_6.3V C16 .22U_6.3V C17 .22U_6.3V

+0.9V_DDR_VTT

C18 1000p_50V C19 1000p_50V C20 1000p_50V C21 1000p_50V C22 180P_50V C23 180P_50V C24 180P_50V C25 180P_50V

QUANTA COMPUTER

Title: ATHLON64 DDRII MEMORY

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ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

+2.5V_RUN
BLM18PG330SN1D_0603
L3
CPU_VDDA_RUN
C26 4.7U_6.3V_0603
C27 .22U_6.3V
C28 3900p_25V
C29 100U_6.3V_3528

(13) CPUCLK — C30 3900p_25V — CPU_CLKIN_SC_P / CPU_CLKIN_SC_N
R14 169/F_0603
(13) CPUCLK# — C31 3900p_25V

R14 close U1 within 600 mil , C30 & C31 close U1 within 1250 mil

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

+1.8V_SUS
R7 *300_NC
R9 *300_NC
R10 300
(14) CPU_SIC — R523 *0_NC
(14) CPU_SID — R524 *0_NC
CPU_SIC_R
CPU_SID_R

for CPU rev.F , if for rev.G , populate R7,R9,R523,R524 and depopulate R10

place them to CPU within 1"

VLDT_RUN
R13 44.2/F
R12 44.2/F
CPU_HTREF1
CPU_HTREF0

(37) COREFB+V
(37) COREFB-
To Power
T8
T4
(39) VDDIO_FB_H
C678 470P_50V
R567 0
CPU_CLKIN_SC_P
CPU_CLKIN_SC_N

for +1.8V_SUS feedback

+1.8V_SUS
R551 300
R8 300

U1D

CPU_VDDA_RUN — F8 VDDA2, F9 VDDA1
T6 CPU_HT_RESET# — B7 PRESET_L
T5 CPU_ALL_PWROK — A7 PWROK
T7 CPU_LDTSTOP# — F10 PLDTSTOP_L
CPU_SIC_R — AF4 SIC
CPU_SID_R — AF5 SID
HT_REF1, HT_REF0
VDD_FB_H — F6, VDD_FB_L — E6
VDDIO_FB_H — W9, VDDIO_FB_L — Y9
CLKIN_H — A9, CLKIN_L — A8
CPU_DBRDY — G10 DBRDY
CPU_TMS — AA9 TMS
CPU_TCK — AC9 TCK
CPU_TRST# — AD9 TRST_L
CPU_TDI — AF9 TDI
TDO — AF9 CPU_TDO
DBREQ_L — E10 CPU_DBREQ#

THERMTRIP_L — AF6 H_THERMTRIP#
PROCHOT_L — AC7 H_PROCHOT#
H_THERMTRIP# (35)

VID5 A5 (37)
VID4 C6 (37)
VID3 A6 (37)
VID2 A4 (37)
VID1 C5 (37)
VID0 B5 (37)

CPU_PRESENT_L — AC6 CPU_PRESENT#
PSI_L — A3 PSI# (37)
T11

PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

TEST29_H — C9 CPU_TEST29_H_FBCLKOUT_P — R16 80.6/F
TEST29_L — C8 CPU_TEST29_L_FBCLKOUT_N
ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

CPU_TEST25_H_BYPASSCLK_H — F9 TEST25_H
CPU_TEST25_L_BYPASSCLK_L — E8 TEST25_L
CPU_TEST19_PLLTEST0 — G9 TEST19
CPU_TEST18_PLLTEST1 — H10 TEST18
AA7 TEST13
C2 TEST9
T13 CPU_TEST17_BP3 — D7 TEST17
T12 CPU_TEST16_BP2 — E7 TEST16
TEST15
TEST14
TEST12
T15 CPU_TEST07_ANALOG_T — C3 TEST7
T16 CPU_TEST6_DIECRACKMON — AA6 TEST6
CPU_TEST5_THERMDC — W7 TEST5
CPU_TEST4_THERMDA — W8 TEST4
T19 CPU_TEST3_GATE0 — Y6 TEST3
T21 CPU_TEST2_DRAIN0 — AB6 TEST2

(35) CPU_TEST5_THERMDC
(35) CPU_TEST4_THERMDA
add port to Page 35 U36 Thermal IC

TEST24 AE7 — CPU_TEST23_TSTUPD — T14
TEST23 AD8
TEST22 AB8 — CPU_TEST21_SCANEN
TEST21 AC8
TEST20 AE8
TEST28_H — J7 — CPU_TEST28_H_PLLCHRZ_P — T18
TEST28_L — H8 — CPU_TEST28_L_PLLCHRZ_N — T17
TEST27 AA8
TEST26 AB5 — CPU_TEST26_BURNIN# — T20
TEST10 K8 — CPU_TEST10_ANALOGOUT — T22
TEST8 C4 — CPU_TEST08_DIG_T — T22

T24 CPU_RSVD_MA0_CLK3_P — P20 RSVD0
T23 CPU_RSVD_MA0_CLK3_N — P19 RSVD1
T26 CPU_RSVD_MA0_CLK0_P — N20 RSVD2
T28 CPU_RSVD_MA0_CLK0_N — N19 RSVD3

RSVD8 H16 — CPU_MA_RESET# — T25
RSVD9 B18 — CPU_MB_RESET# — T27
RSVD10 B3 — CPU_RSVD_VIDSTRB1 — T30
RSVD11 C1 — CPU_RSVD_VIDSTRB0 — T29
RSVD12 H6 — CPU_RSVD_VDDNB_FB_P — T31
RSVD13 G6 — CPU_RSVD_VDDNB_FB_N — T32
RSVD14 D5 — CPU_RSVD_CORE_TYPE — T33

MISC

RSVD15 R24
RSVD16 W18
RSVD17 R23
RSVD18 AA8
RSVD19 R18
RSVD20 H19

T34 CPU_RSVD_MB0_CLK3_P — R26 RSVD4
T36 CPU_RSVD_MB0_CLK3_N — R25 RSVD5
T35 CPU_RSVD_MB0_CLK0_P — P22 RSVD6
T37 CPU_RSVD_MB0_CLK0_N — R22 RSVD7

AMD NPT S1 SOCKET
Processor Socket

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

(14,15) CPU_PWRGD — R19 0 — CPU_ALL_PWROK
R525 10K
(11,14) LDT_STOP# — R20 0 — CPU_LDTSTOP#
R526 10K
(14) LDT_RST# — R527 0 — CPU_HT_RESET#
R528 10K

change for SB600 from SB460

R527 can be used for EMI verifing, place close to CPU

+1.8V_RUN
+1.8V_SUS
R24 *10K_NC
R27 300
H_PROCHOT#
Q2 *MMBT3904_NC
CPU_EC_PROCHOT# (27)
CPU_PROCHOT# (15)
*MMBT3904_NC Q49

0428 : depopulate R24 & Q2 , because AMD Errata 141 "PROCHOT_L should not be used as an output from the processor"

SB this pin is 3.3V,need it level-shift.

delete ED5 H_THERMTRIP# circuit

+1.8V_SUS
CPU_TEST26_BURNIN# R22 300
CPU_PRESENT# R25 1K/F
CPU_TEST25_H_BYPASSCLK_H R26 510/F
CPU_TEST21_SCANEN R32 300
CPU_TEST25_L_BYPASSCLK_L R44 510/F
CPU_TEST19_PLLTEST0 R45 300
CPU_TEST18_PLLTEST1 R46 300

If no use which Net need pull-up or down

add HDT connector for debug convenience

HDT CONNECTOR

JHDT1
CPU_DBREQ# 7
CPU_DBRDY 9
CPU_TCK 11
CPU_TMS 13
CPU_TDI 15
CPU_TRST# 17
CPU_TDO 19
+1.8V_SUS 23
GND 1,3,5,2,4,6,8,10,12,14,16,18,20,22,24,25
Resereved 5
Resereved 6
DBREQ_L 8
DBRDY 10
TCK 12
TMS 14
TDI 16
TRST_L 18
TDO 20
VDDIO 21
RESET_L 24
CPU_RESET#
*HDT conn_NC

+3.3V_SUS
+1.8V_SUS
R580 *10K_NC
R581 *10K_NC
Q55 *MMBT3904_NC
CPU_HT_RESET#

delete ED5 thermal sensor

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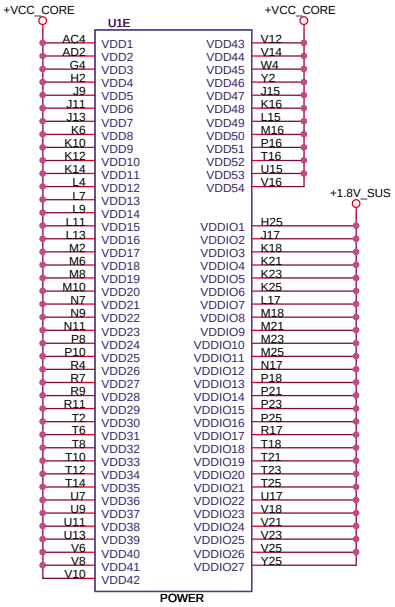
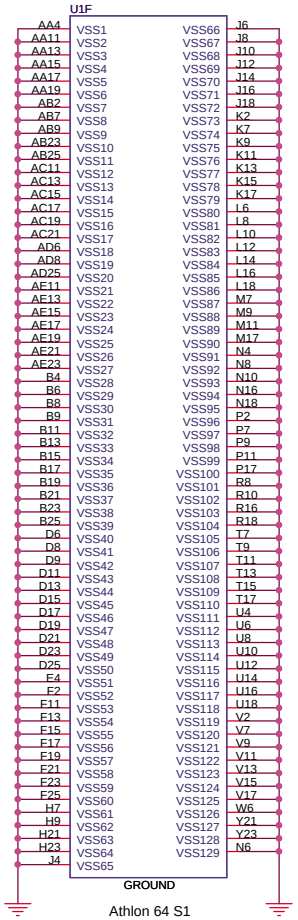
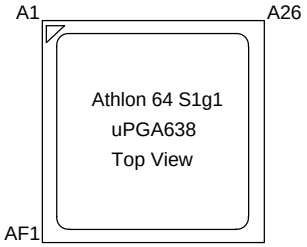
QUANTA COMPUTER

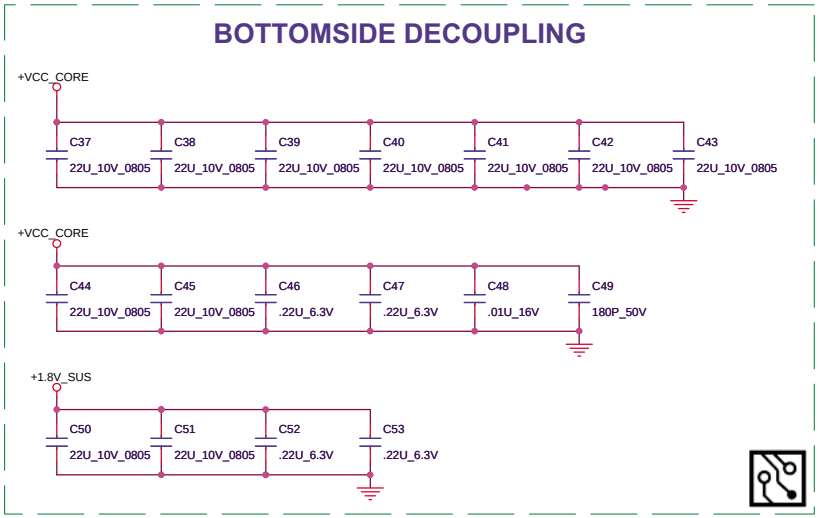


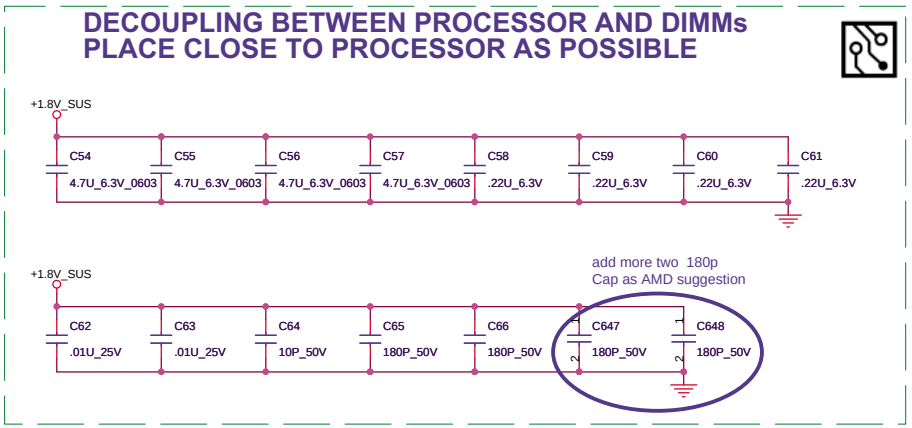
Athlon 64 S1
Processor Socket



Athlon 64 S1
Processor Socket







PROCESSOR POWER AND GROUND

QUANTA COMPUTER

Title	ATHLON64 PWR & GND	
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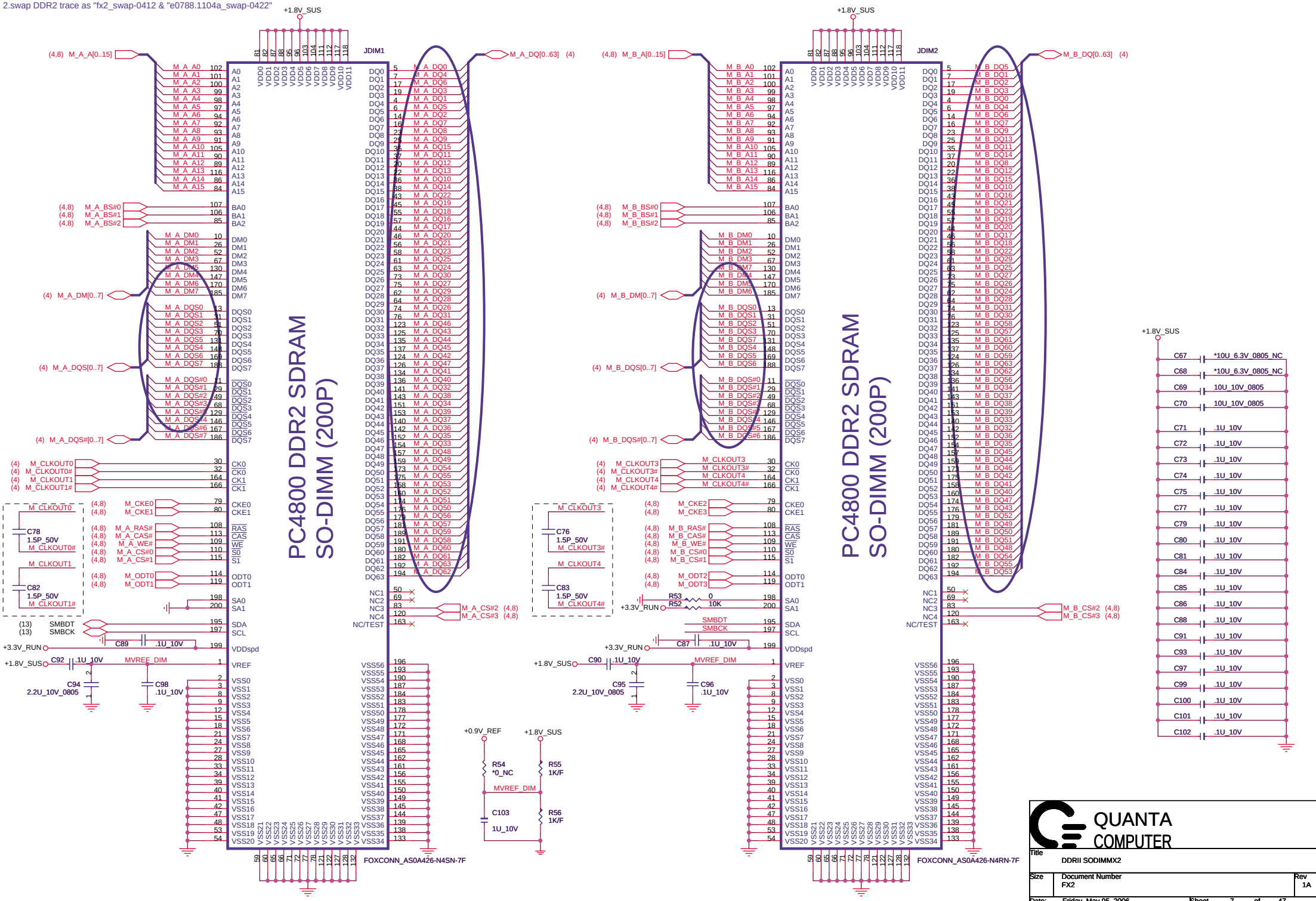
1.Change DDR2 socket(P/N, Description, footprint, part reference, value)
2.swap DDR2 trace as "fx2_swap-0412 & "e0788.1104a_swap-0422"



QUANTA COMPUTER

Title	DDRII SODIMMX2	
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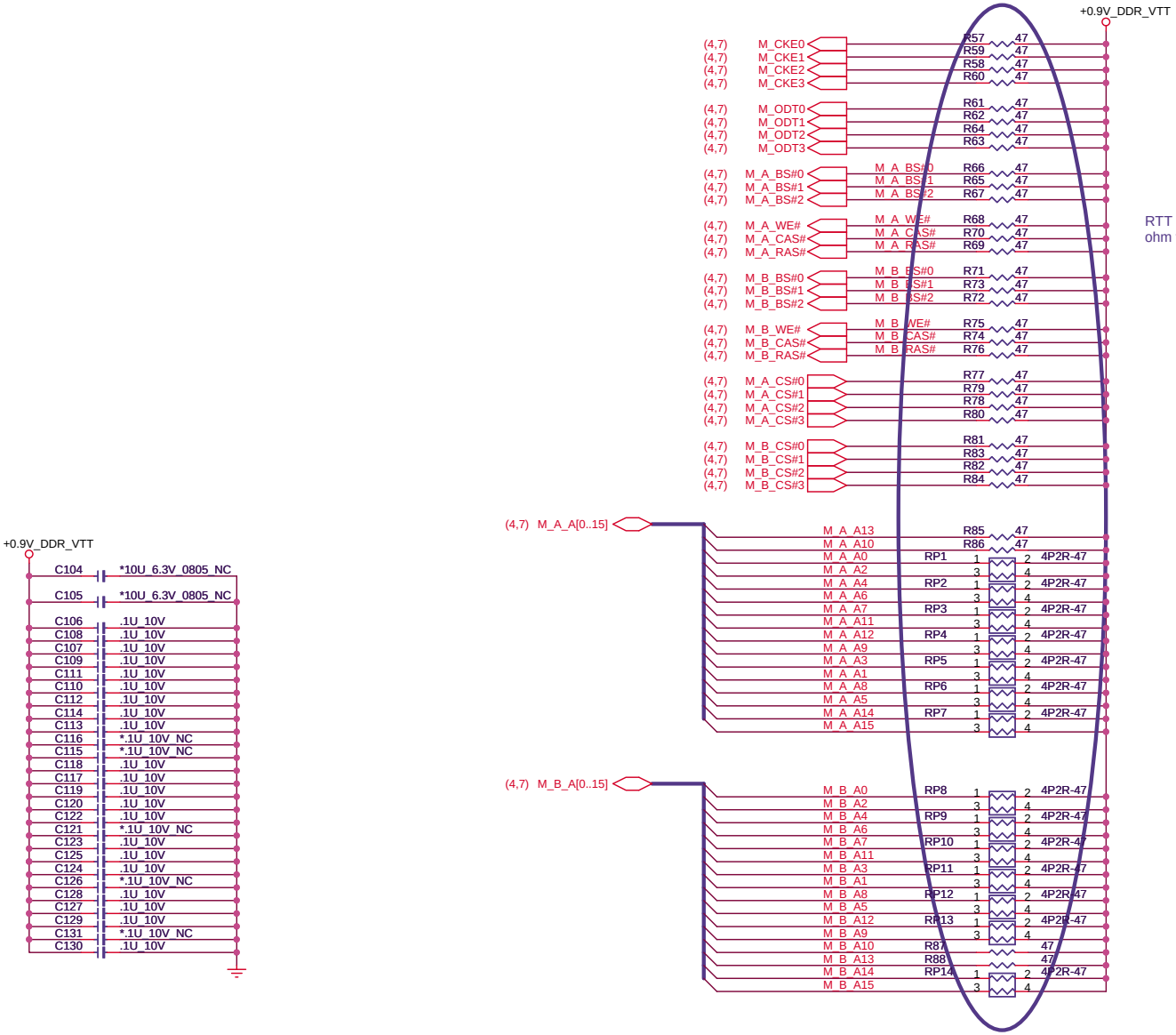

RTT termination changed from 56 ohm to 47 ohm as AMD suggestion

QUANTA COMPUTER

Title	DDRII TERMINATION	
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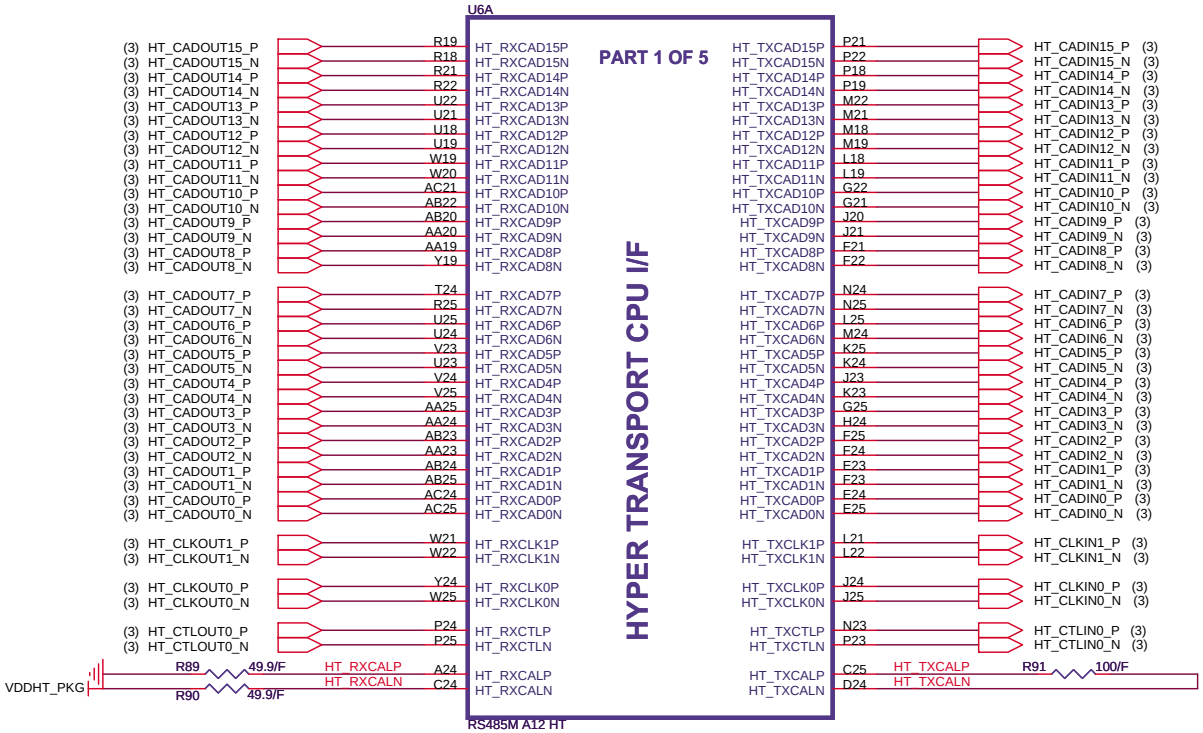

QUANTA COMPUTER

Title	RS485-HT LINK0 I/F	
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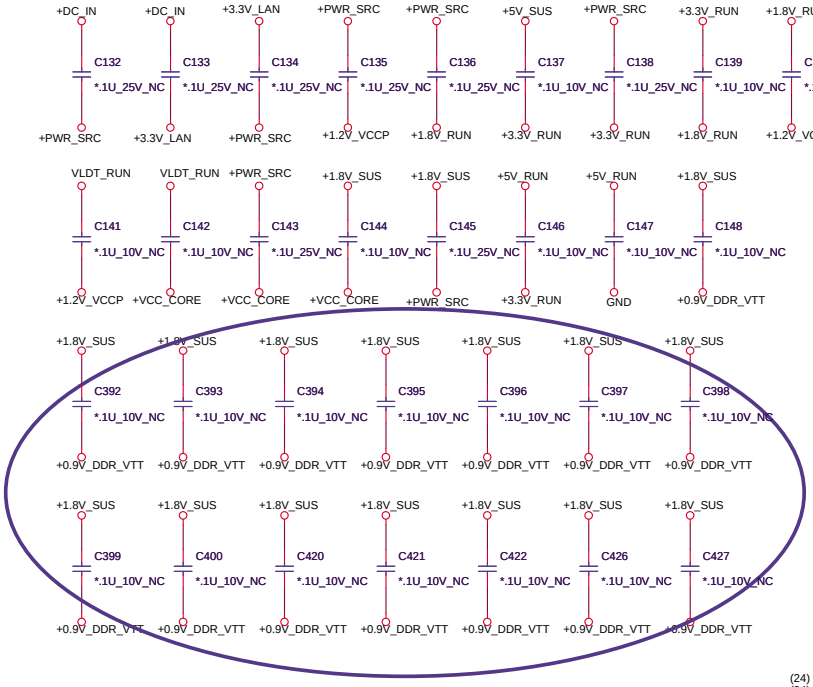
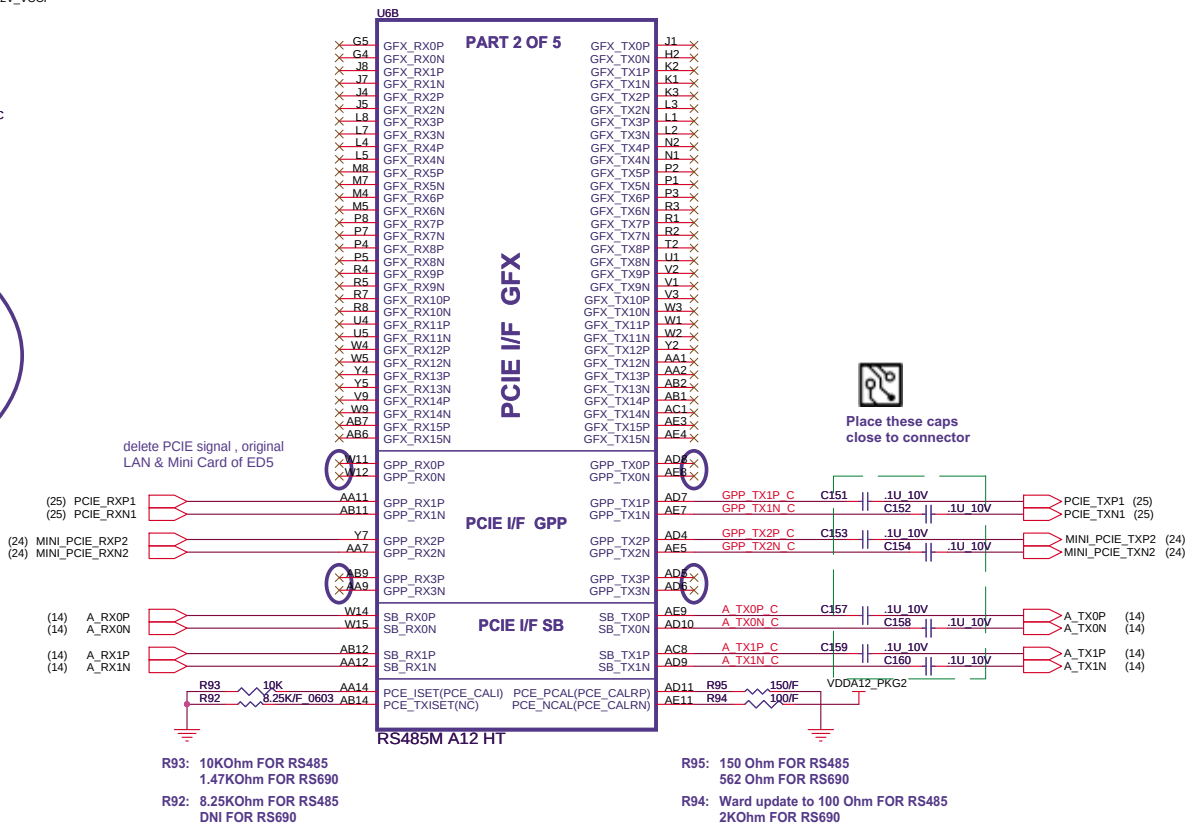


reserve more 14 Cap. between +0.9V_DDR_VTT & +1.8V_SUS



R93: 10KOhm FOR RS485
1.47KOhm FOR RS690

R92: 8.25KOhm FOR RS485
DNI FOR RS690

R95: 150 Ohm FOR RS485
562 Ohm FOR RS690

R94: Ward update to 100 Ohm FOR RS485
2KOhm FOR RS690

QUANTA COMPUTER

Title	RS485-PCIE LINK I/F	
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+1.8V_RUN L4 — BK1608HS600 — HTPVDD — C161 10U_10V — C162 4.7U_6.3V

+1.8V_RUN L5 — BK1608HS600 — AVDDQ — C163 10U_10V — C164 2.2U_10V

+3.3V_RUN L6 — BK1608HS600 — AVDD_NB — C165 4.7U_6.3V — C166 .1U_10V

+1.8V_RUN — R96 0_0603 — AVDD1 — C167 2.2U_10V

+1.8V_RUN L7 — BK1608HS600 — PLLVDD — C168 10U_10V — C169 4.7U_6.3V

added as FM1 application for ED5

+3.3V_RUN — RP15 4P2R-2.2K — Q7 2N7002W-7-F — DDCDAT — DAT_DDC2 (19)

+3.3V_RUN — Q8 2N7002W-7-F — DDCCLK — CLK_DDC2 (19)

+1.8V_RUN +3.3V_RUN — R110 10K — R111 10K — LDT_STOP# NB — (5,14) LDT_STOP# — Q9 MMBT3904

LOAD_ROM#: LOAD ROM STRAP ENABLE

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

deleted caused by Svideo defeature

close to NB

(19) VGA_RED — R104 150/F
(19) VGA_GRN — R105 150/F
(19) VGA_BLU — R106 150/F

external trace become to internal trace

U6C

AVDD_NB — B22 AVDD1, C22 AVDD2
AVDD1 — G17 AVSSN1, H17 AVSSN2, A20 AVDDDI, B20 AVSSDI
AVDDQ — A21 AVDDQ, A22 AVSSQ
C171 .1U_10V

C_R — C21
Y_G — C20
COMP_B — D19
139, 140, 141

RED — E19
GREEN — F19
BLUE — G19
DACVSYNC — C6
DACHSYNC — A5
(19) VSYNC
(19) HSYNC
RSET — B21
R107 715/F

DACSCL — B6
DACSDA — A6
DDCCLK R108 0
DDCDAT R101 0

PLLVDD — A10 PLLVDD(PLLVDD18), B10 PLLVSS
HTPVDD — B24 HTPVDD, B25 HTPVSS

(14,23,24,25,33) ALINK_RST#
(27) NB_PWRGD
R109 0 NB_RST# — C10 SYSRESET#
R102 0 LDT_STOP#_NB — C11 POWERGOOD, C5 LDTSTOP#
(14) ALLOW_LDTSTOP — B5 ALLOW_LDTSTOP

(13) HTREFCLK — R112 10K — C23 HTTSTCLK, B23 HTREFCLK
TV_SWITCH — R124 10K — C2 TVCLKIN

(13) NB_OSC — B11 OSCIN
T50 PLLVDD12 — A11 OSCOUT(PLLVDD12)

(13) NBSRC_CLKP — F2 GFX_CLKP
(13) NBSRC_CLKN — F1 GFX_CLKN
(13) SBLINK_CLKP — G1 SB_CLKP
(13) SBLINK_CLKN — G2 SB_CLKN

R116 *3K_NC by default — LOAD_ROM#
R115 *2.7K_NC DFT_GPIO0 — D6 DFT_GPIO0
R118 *2.7K_NC DFT_GPIO2 — C8 DFT_GPIO1
R120 *2.7K_NC DFT_GPIO3 — C7 DFT_GPIO2
R119 *2.7K_NC DFT_GPIO4 — B8 DFT_GPIO3
R121 *2.7K_NC DFT_GPIO5 — A8 DFT_GPIO4, DFT_GPIO5

(14) BMREQ# — D1 RB751 — B2 BMREQb
(18) PHL_CLK — A2 I2C_CLK
(18) PHL_DATA — B4 I2C_DATA
(16) SB_NB_THRMDA — R583 *0_NC — AA15 THERMALDIODE_P
(16) SB_NB_THRMDC — R584 *0_NC — AB15 THERMALDIODE_N

0428 : reserve for NB thermal Diode

T65 — C14 TMDS_HPD
T68 — B3 DDC_DATA
C3 TESTMODE
+3.3V_RUN — R123 2K/F — A3 STRP_DATA

R126 4.7K/F

PART 3 OF 5

CRT/TVOUT: AVDD1, AVDD2, AVSSN1, AVSSN2, AVDDDI, AVSSDI, AVDDQ, AVSSQ, C_R, Y_G, COMP_B, RED, GREEN, BLUE, DACVSYNC, DACHSYNC, RSET, DACSCL, DACSDA

PLL PWR: PLLVDD(PLLVDD18), PLLVSS, HTPVDD, HTPVSS

CLOCKs: SYSRESET#, POWERGOOD, LDTSTOP#, ALLOW_LDTSTOP, HTTSTCLK, HTREFCLK, TVCLKIN, OSCIN, OSCOUT(PLLVDD12), GFX_CLKP, GFX_CLKN, SB_CLKP, SB_CLKN

MIS.: DFT_GPIO0, DFT_GPIO1, DFT_GPIO2, DFT_GPIO3, DFT_GPIO4, DFT_GPIO5, BMREQb, I2C_CLK, I2C_DATA, THERMALDIODE_P, THERMALDIODE_N, TMDS_HPD, DDC_DATA, TESTMODE, STRP_DATA

LVDS: TXOUT_L0P, TXOUT_L0N, TXOUT_L1P, TXOUT_L1N, TXOUT_L2P, TXOUT_L2N, TXOUT_L3P, TXOUT_L3N, TXOUT_U0P, TXOUT_U0N, TXOUT_U1P, TXOUT_U1N, TXOUT_U2P, TXOUT_U2N, TXOUT_U3P, TXOUT_U3N, TXCLK_LP, TXCLK_LN, TXCLK_UP, TXCLK_UN, LPVDD, LPVSS, LVDDR18D_1, LVDDR18D_2, LVDDR18A_1, LVDDR18A_2, LVSSR1, LVSSR3, LVSSR5, LVSSR6, LVSSR7, LVSSR8, LVSSR12, LVSSR13, LVDS_DIGON, LVDS_BLON, LVDS_BLEN

DVO: DVO_D0(GPP_TX4P), DVO_D1(GPP_TX4N), DVO_D2(NC), DVO_D3(GPP_RX4P), DVO_D4(GPP_RX4N), DVO_D5(NC), DVO_D6(NC), DVO_D7(GPP_TX5N), DVO_D8(GPP_TX5P), DVO_D9(GPP_RX5N), DVO_D10(GPP_RX5P), DVO_D11(NC), DVO_VSYNC(NC), DVO_DE(NC), DVO_HSYNC(NC), DVO_IDCKP(NC), DVO_IDCKN(NC)

RS485M A12 HT

TXOUT_L0P B14 — TXLOUT0+ (18)
TXOUT_L0N B15 — TXLOUT0- (18)
TXOUT_L1P B13 — TXLOUT1+ (18)
TXOUT_L1N A13 — TXLOUT1- (18)
TXOUT_L2P H14 — TXLOUT2+ (18)
TXOUT_L2N G14 — TXLOUT2- (18)
TXOUT_L3P D17 — T47
TXOUT_L3N E17 — T48

ED5 is single ch , change to dual ch as FM1

TXOUT_U0P A15 — TXUOUT0+ (18)
TXOUT_U0N B16 — TXUOUT0- (18)
TXOUT_U1P C17 — TXUOUT1+ (18)
TXOUT_U1N C18 — TXUOUT1- (18)
TXOUT_U2P B17 — TXUOUT2+ (18)
TXOUT_U2N A17 — TXUOUT2- (18)
TXOUT_U3P A18 — T49
TXOUT_U3N B18 — T46

TXCLK_LP E15 — TXLCLKOUT+ (18)
TXCLK_LN D15 — TXLCLKOUT- (18)
TXCLK_UP H15 — TXUCLKOUT+ (18)
TXCLK_UN G15 — TXUCLKOUT- (18)

LPVDD D14
LPVSS E14
C172 .1U_10V — C170 4.7U_6.3V

LVDDR18D_1 A12
LVDDR18D_2 B12
LVDDR18A_1 C12
LVDDR18A_2 C13

RS485: LVDDR18A=1.8V

CHECK TO 2200HM

+1.8V_RUN — L8 BK1608HS600 — L9 BK1608HS600 — L10 BK1608HS600

LVSSR1 A16
LVSSR3 A14
LVSSR5 D12
LVSSR6 C19
LVSSR7 C15
LVSSR8 C16
C173 .1U_10V — C174 4.7U_6.3V — C175 .1U_10V — C176 4.7U_6.3V

LVSSR12 F14
LVSSR13 F15

LVDS_DIGON E12 — LCD_PON — R114 0 — LCD_POWER_ON (18)
LVDS_BLON G12 — LVDS_BLON
LVDS_BLEN F12 — LVDS_BLEN — T146

DVO_D0(GPP_TX4P) AD14 — T51
DVO_D1(GPP_TX4N) AD15 — T52
DVO_D2(NC) AE15 — T54
DVO_D3(GPP_RX4P) AD16 — T53
DVO_D4(GPP_RX4N) AE16 — T55
DVO_D5(NC) AC17 — T57
DVO_D6(NC) AD18 — T56
DVO_D7(GPP_TX5N) AE19 — T58
DVO_D8(GPP_TX5P) AD19 — T59
DVO_D9(GPP_RX5N) AE20 — T60
DVO_D10(GPP_RX5P) AD20 — T64
DVO_D11(NC) AE21 — T63

DVO_VSYNC(NC) AD13 — T67
DVO_DE(NC) AC13 — T66
DVO_HSYNC(NC) AE13 — T69
DVO_IDCKP(NC) AE17 — T71
DVO_IDCKN(NC) AD17 — T70

R125 2K/F — LCD_PON
R127 2K/F — LVDS_BLON
R128 2K/F — LVDS_BLEN

	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVDD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P

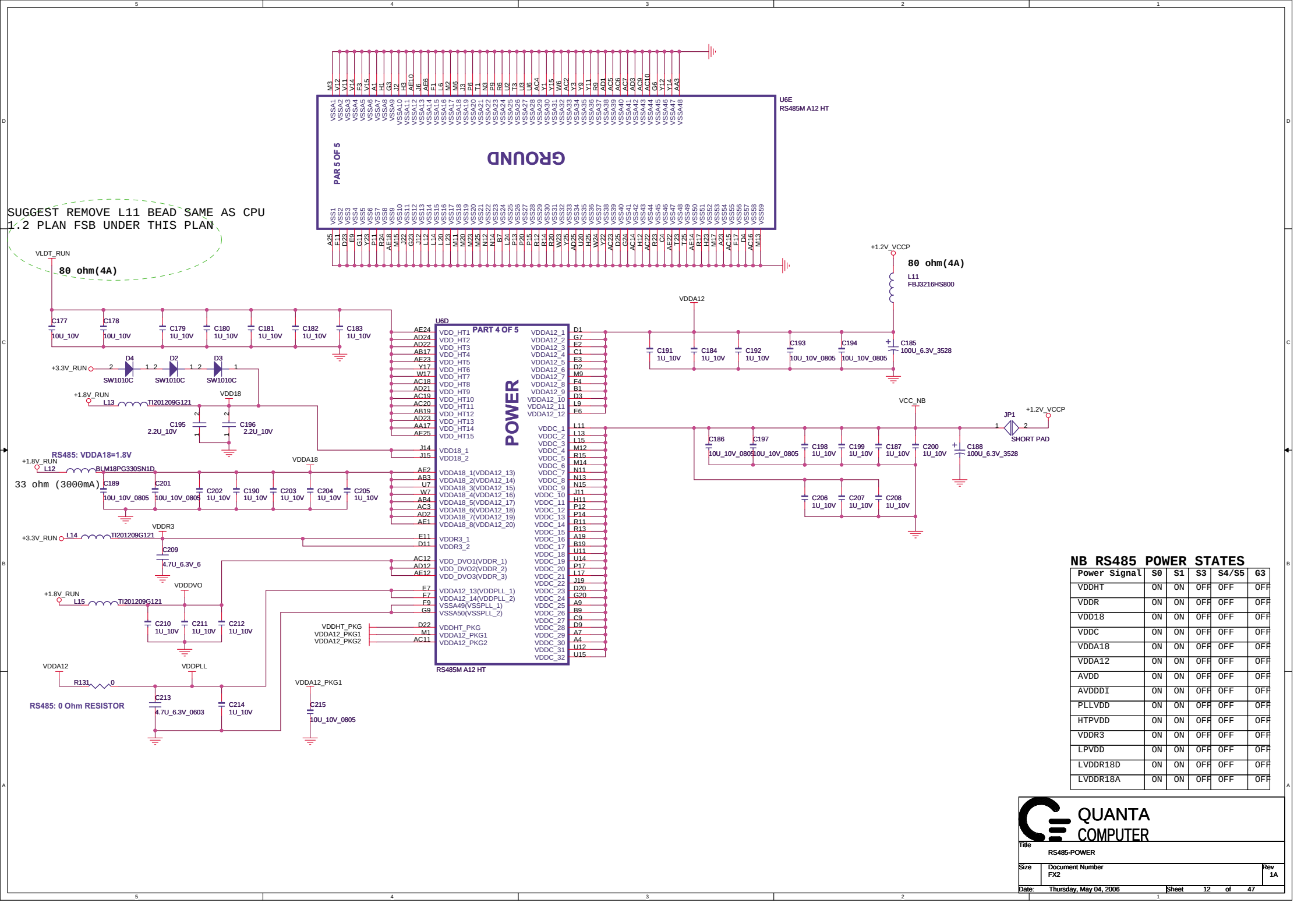
reserve 0 ohm to connect "LVDS_BLON" to LCD conn directly

R129 0_NC — +3.3V_RUN — +3.3V_RUN
LVDS_BLON — U40 NC7SZ08P5X_NL
(27) FPBACK_EN — NB_PWRGD — U7 NC7SZ08P5X_NL
R591 100K
R130 0 — BLON (18)

0504 : change "FPBACK_EN" from connected with "LVDS_BLEN" directly to connected with "LVDS_BLON" by a AND gate

QUANTA COMPUTER

Title	RS485-LVDS	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 11 of 47	

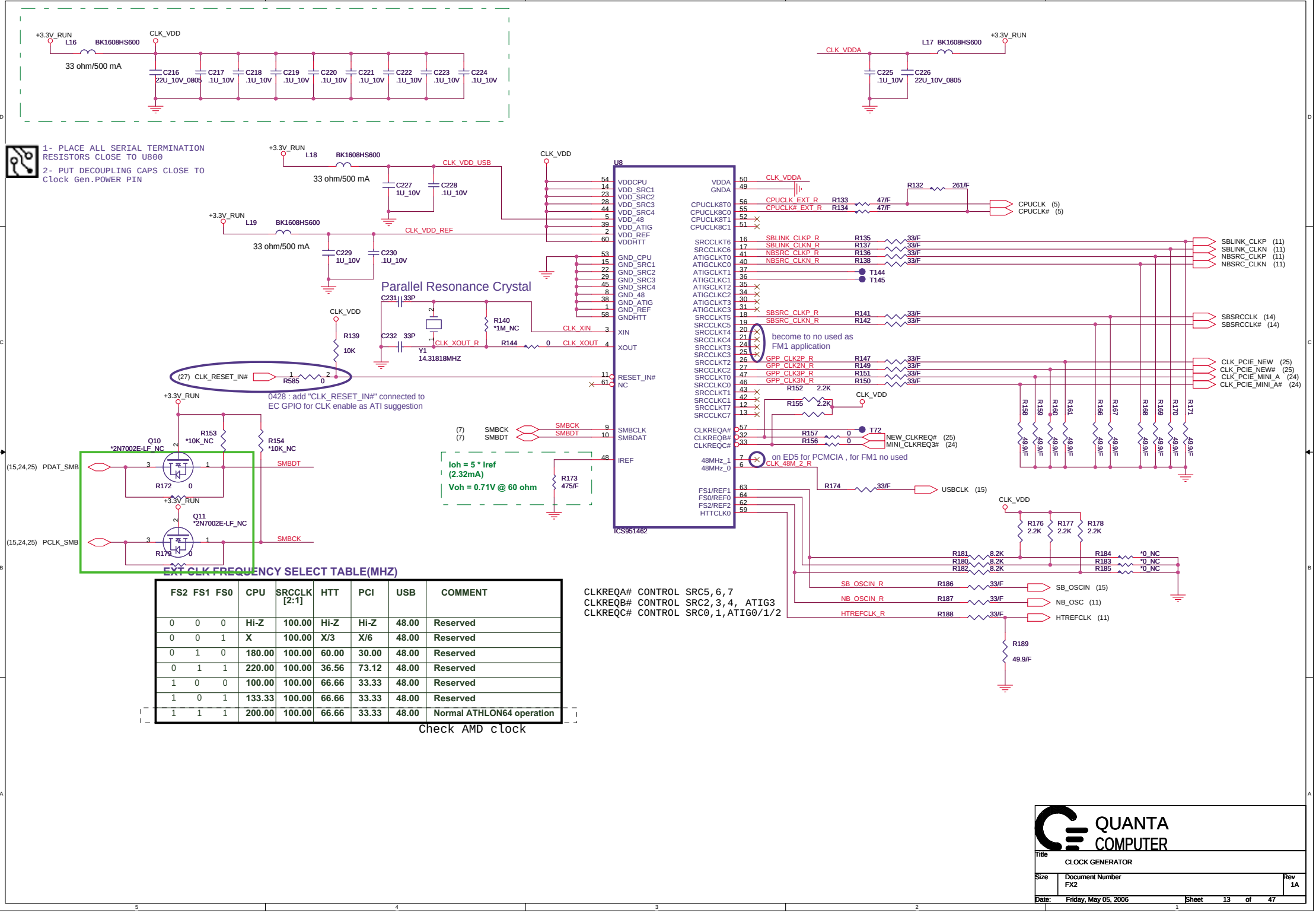


NB RS485 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

QUANTA COMPUTER

Title	RS485-POWER	
Size	Document Number FX2	Rev 1A
Date: Thursday, May 04, 2006	Sheet 12 of 47	



EXT CLK FREQUENCY SELECT TABLE(MHZ)

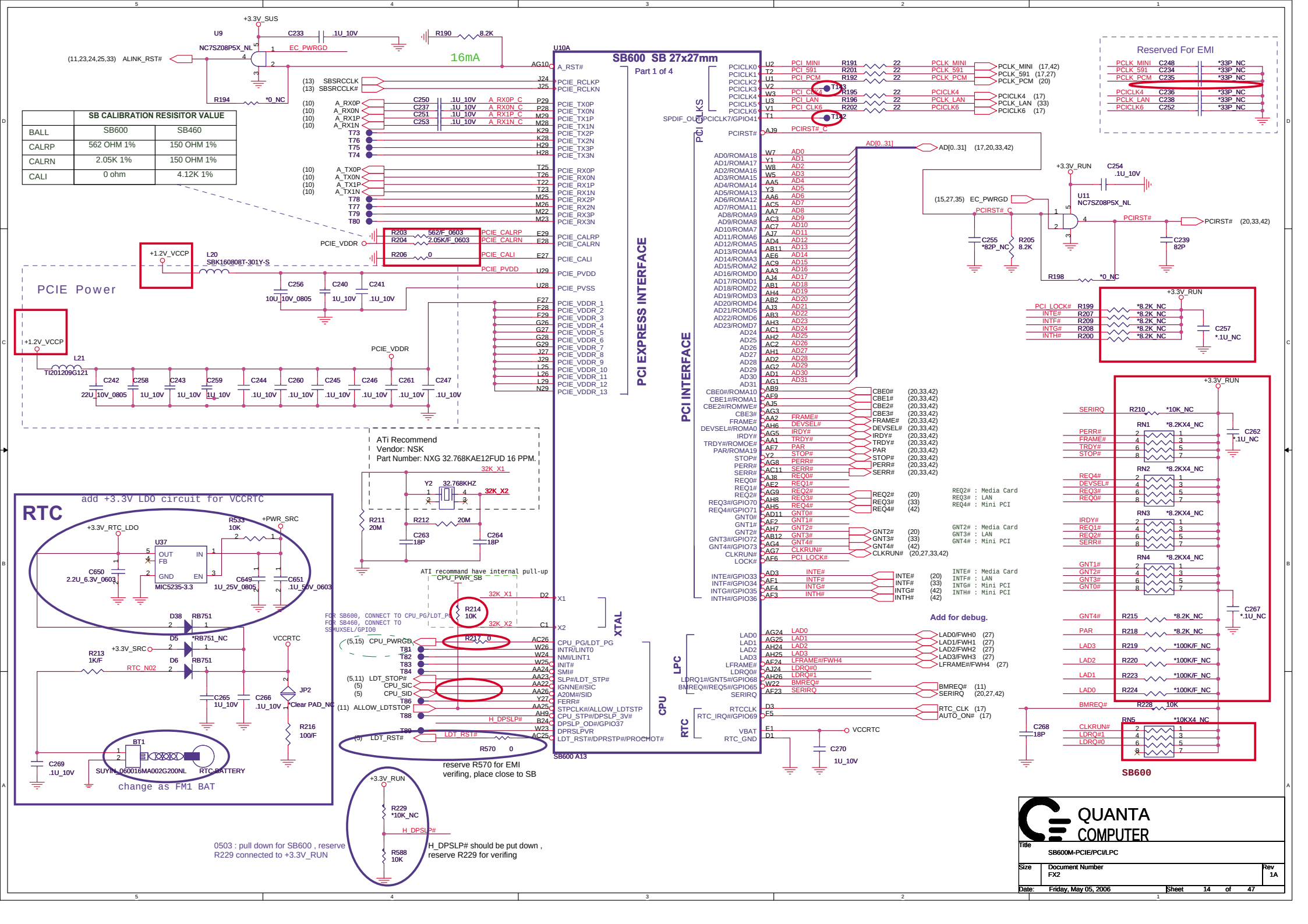
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Check AMD clock

CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4, ATIG3
CLKREQC# CONTROL SRC0,1,ATIG0/1/2

QUANTA COMPUTER

Title	CLOCK GENERATOR	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 13 of 47	


SB600 SB 27x27mm
Part 1 of 4
SB600 A13
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
CPU
LPC
RTC
PCIE Power
SB CALIBRATION RESISITOR VALUE
BALL | SB600 | SB460
CALRP | 562 OHM 1% | 150 OHM 1%
CALRN | 2.05K 1% | 150 OHM 1%
CALI | 0 ohm | 4.12K 1%
16mA
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.
RTC
add +3.3V LDO circuit for VCCRTC
change as FM1 BAT
ATI recommand have internal pull-up
reserve R570 for EMI
verifing, place close to SB
0503 : pull down for SB600 , reserve
R229 connected to +3.3V_RUN
H_DPSLP# should be put down ,
reserve R229 for verifing
Add for debug.
Reserved For EMI
SB600
QUANTA COMPUTER
Title: SB600M-PCIE/PCI/LPC
Size: Document Number: FX2
Rev: 1A
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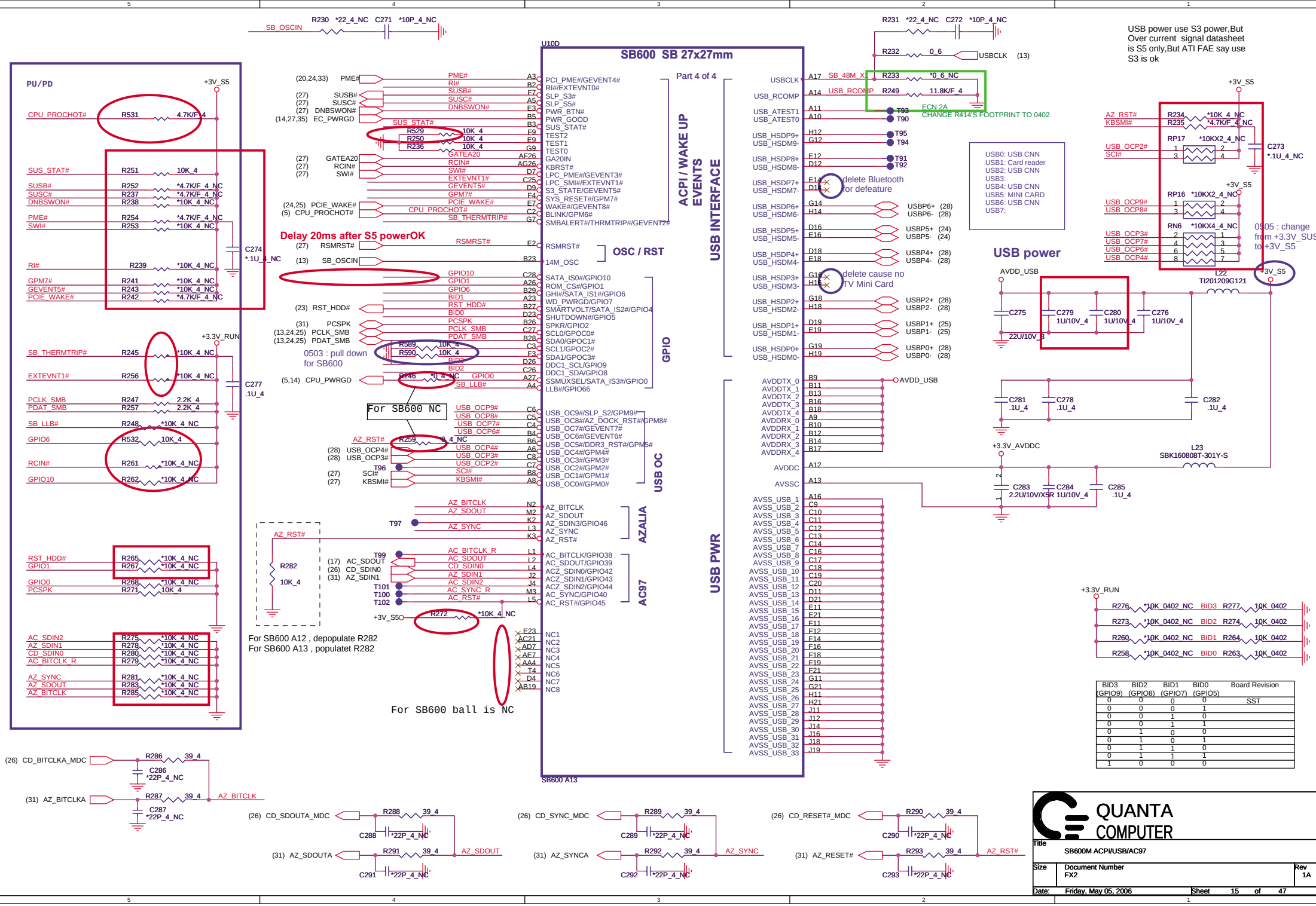
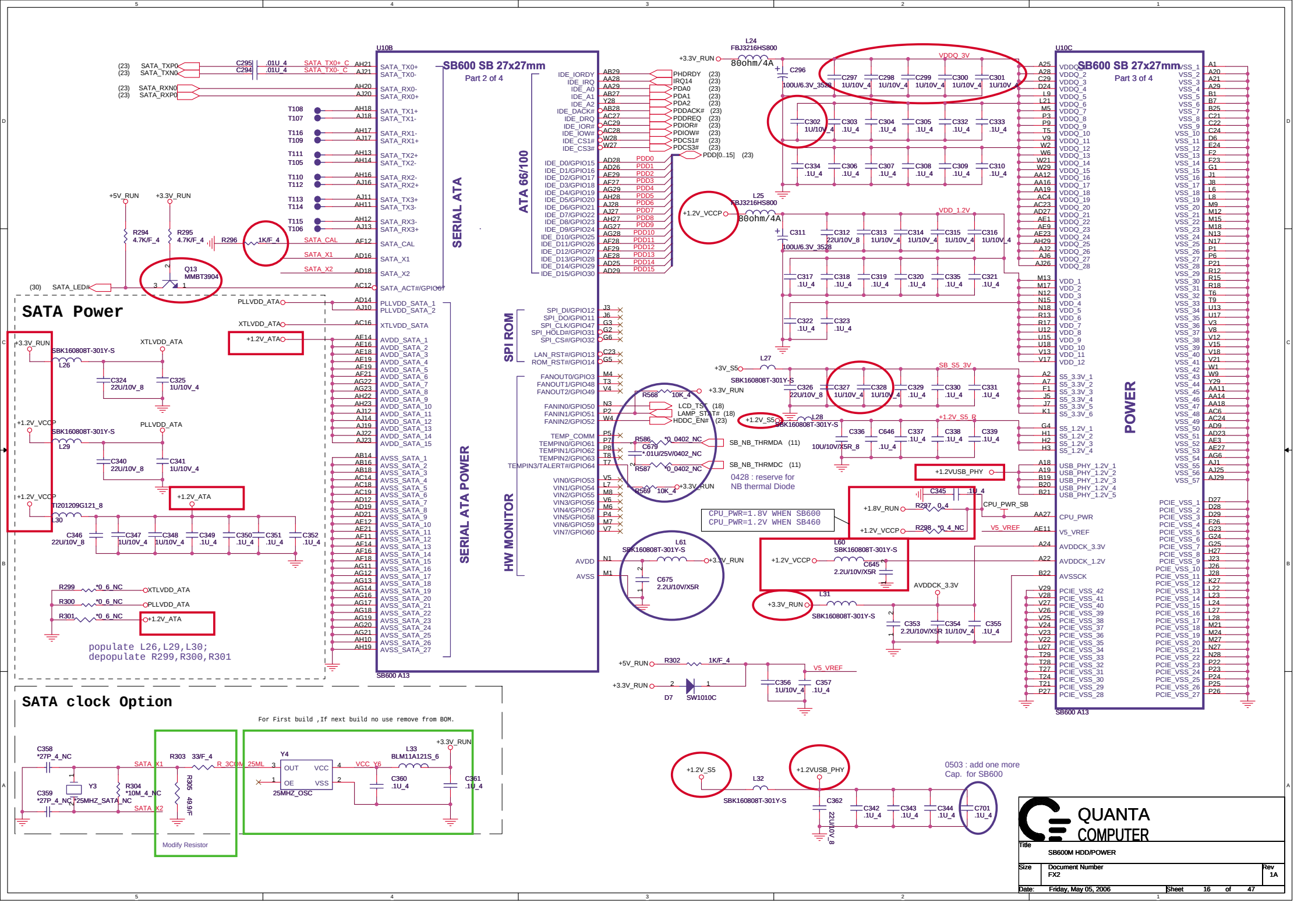
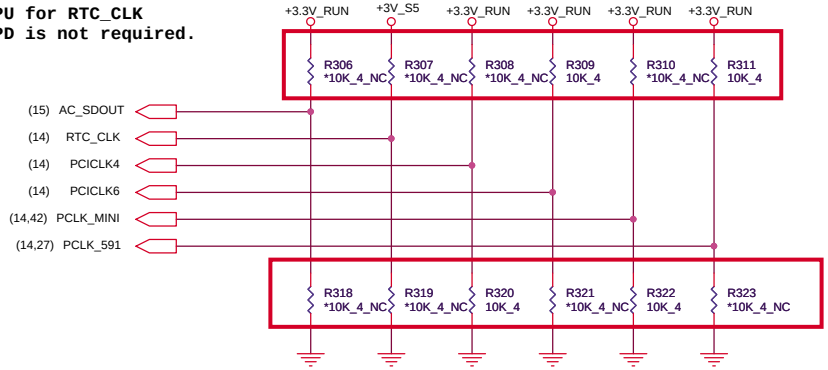
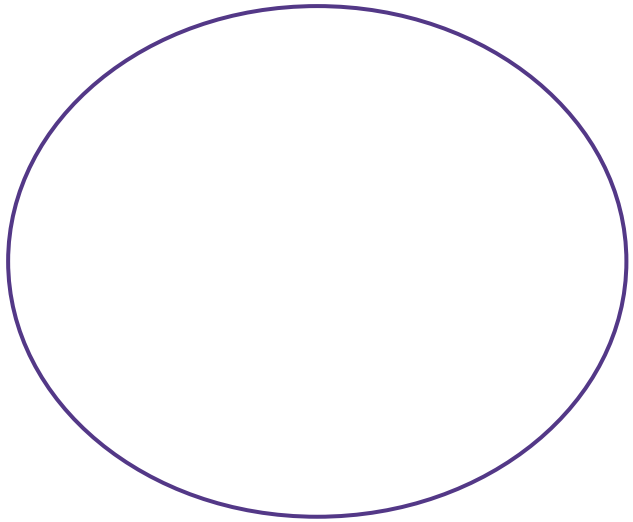

SB600 SB 27x27mm
U10D
Part 4 of 4
SB600 A13
PU/PD
ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
Delay 20ms after S5 powerOK
0503 : pull down for SB600
For SB600 NC
For SB600 A12 , depopulate R282
For SB600 A13 , populatet R282
For SB600 ball is NC
delete Bluetooth for defeature
delete cause no TV Mini Card
USB power
USB power use S3 power,But Over current signal datasheet is S5 only,But ATI FAE say use S3 is ok
ECN 2A
CHANGE R414'S FOOTPRINT TO 0402
USB0: USB CNN
USB1: Card reader
USB2: USB CNN
USB3:
USB4: USB CNN
USB5: MINI CARD
USB6: USB CNN
USB7:
0505 : change from +3.3V_SUS to +3V_S5
L22 TI201209G121
L23 SBK160808T-301Y-S
QUANTA COMPUTER
Title SB600M ACPI/USB/AC97
Size Document Number FX2 Rev 1A
Date: Friday, May 05, 2006 Sheet 15 of 47


SB600 SB 27x27mm
Part 2 of 4
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
SB600 A13
SB600 SB 27x27mm
Part 3 of 4
POWER
SB600 A13
SATA Power
populate L26,L29,L30;
depopulate R299,R300,R301
SATA clock Option
For First build ,If next build no use remove from BOM.
Modify Resistor
CPU_PWR=1.8V WHEN SB600
CPU_PWR=1.2V WHEN SB460
0428 : reserve for
NB thermal Diode
0503 : add one more
Cap. for SB600
QUANTA
COMPUTER
SB600M HDD/POWER
Document Number
FX2
Rev
1A
Friday, May 05, 2006
Sheet 16 of 47

SB600 has 15K internal PD for AC_SDOUT
15K internal PU for RTC_CLK
,External PU/PD is not required.

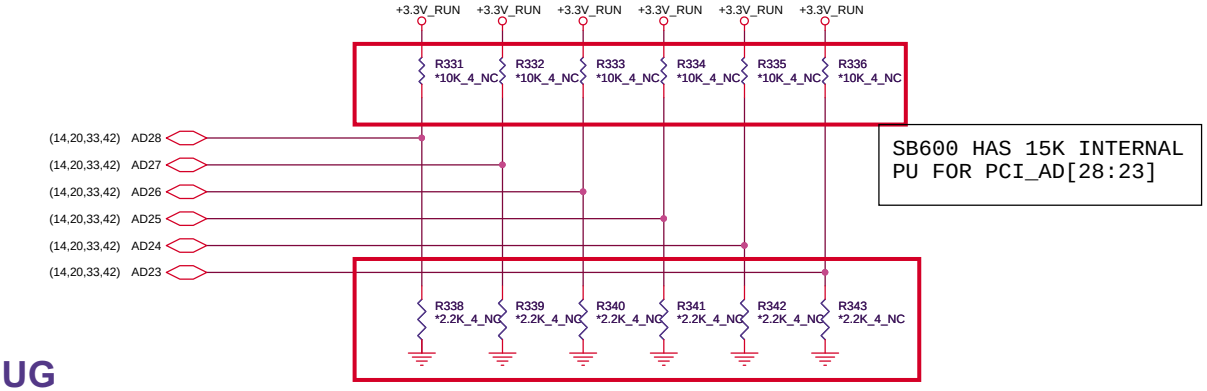


delete SB460 setting



REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI PCLK_591 PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48 DEFAULT	CPU IF=K8 DEFAULT	H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	



SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Use Long Reset DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	boot fail time disabled DEFAULT
PULL LOW	USE SHORT RESET	Use Short Reset	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	boot fail time enabled
	SB460 Only	SB600 Only					SB600 Only

QUANTA COMPUTER

Title	SB600M STRAPS	
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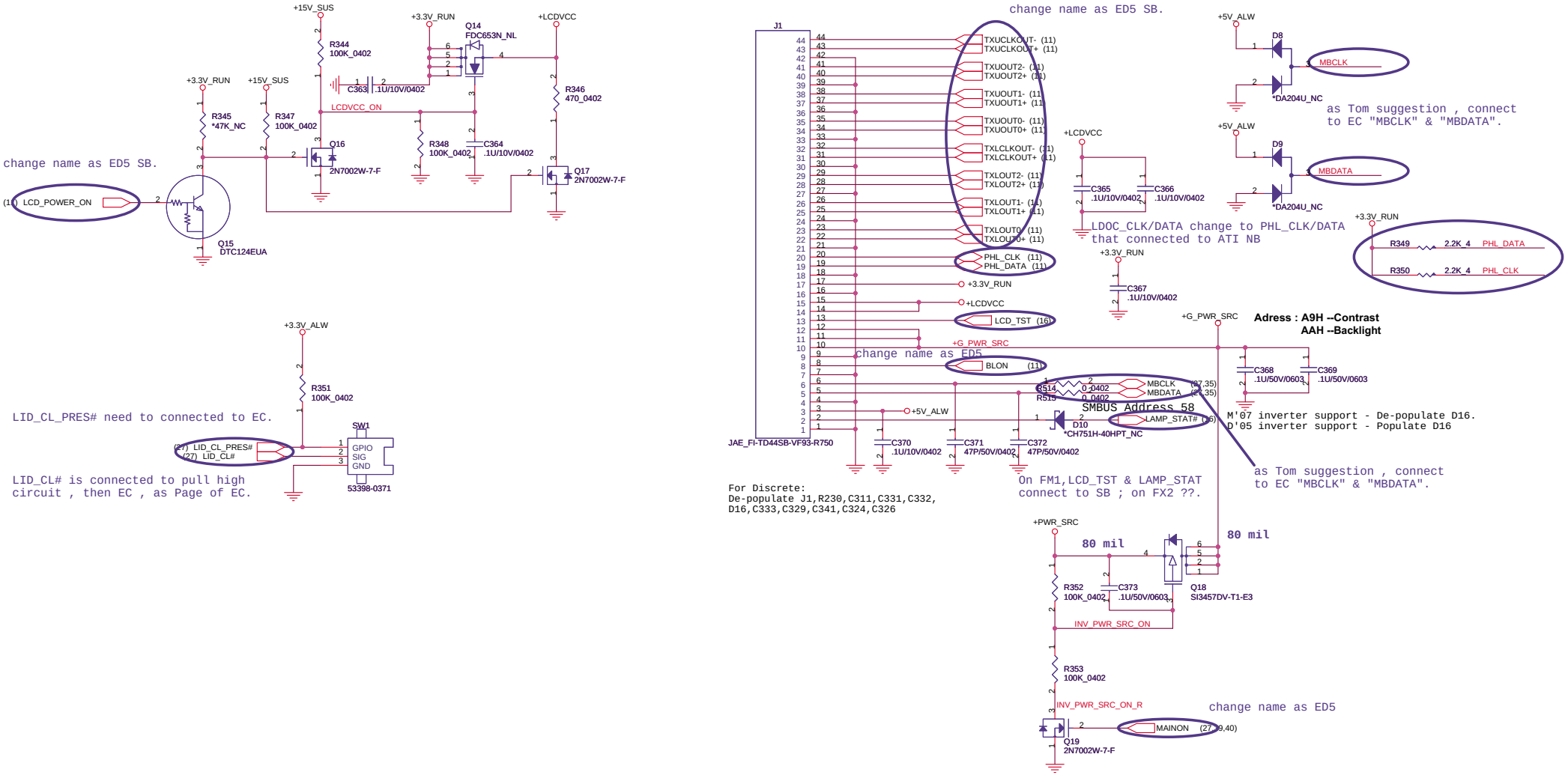

QUANTA COMPUTER

Title	LCD CONN	
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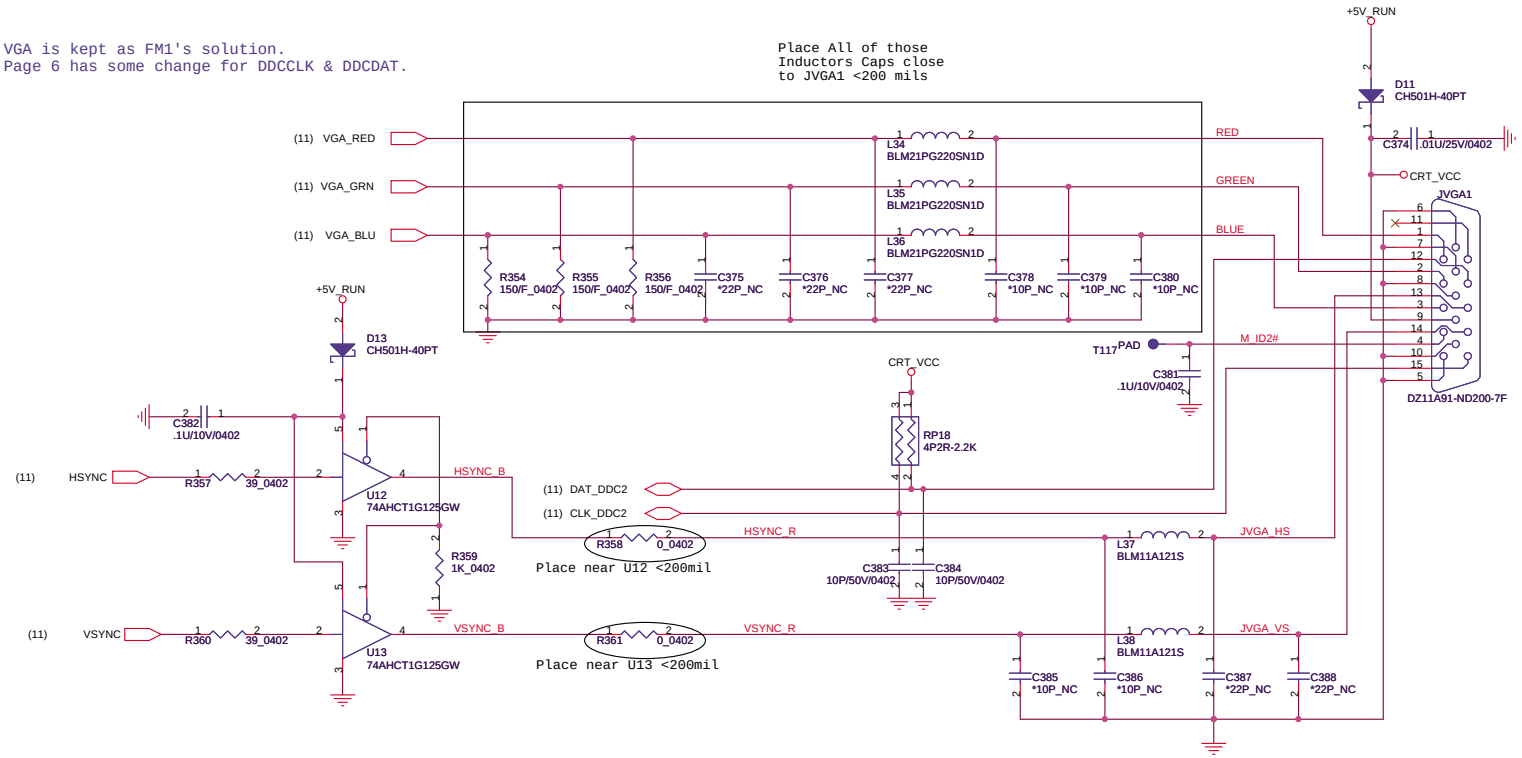
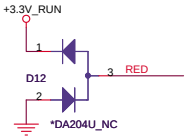
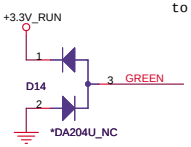
VGA is kept as FM1's solution.
Page 6 has some change for DDCCLK & DDCDAT.

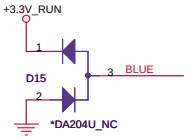
Place All of those
Inductors Caps close
to JVGA1 <200 mils



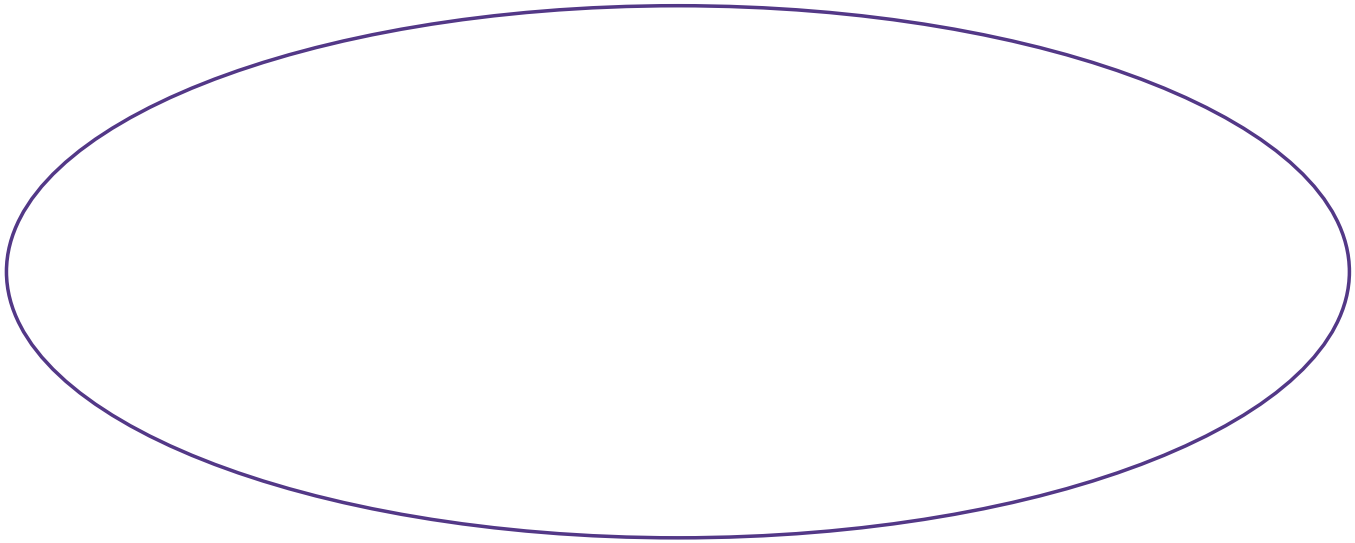


Place D4,D5,D6 close
to JVGA1 <200 mils





delete Svideo for defeature



QUANTA COMPUTER		
Title: CRT		
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change name for ED5
copy ED5 to FX2
Waiting to check

+3.3V_R5C832
C401 10U/10V/0805
C402 .01U/25V/0402
C403 .01U/25V/0402
C404 .01U/25V/0402
C405 .01U/25V/0402
C406 .01U/25V/0402
C407 10U/10V/0805
C408 .01U/25V/0402
C409 .1U/10V/0402
C410 .01U/25V/0402
Place the power caps close to the relation pins.
C413 .01U/25V/0402
C414 .01U/25V/0402
C415 .47U/10V/0603
C416 .47U/10V/0603
U15B
VCC_PCI1 10
VCC_PCI2 20
VCC_PCI3 27
VCC_PCI4 32
VCC_PCI5 41
VCC_PCI6 128
VCC_RIN 61
VCC_ROUT1 16
VCC_ROUT2 34
VCC_ROUT3 64
VCC_ROUT4 114
VCC_ROUT5 120
VCC_3V 67
VCC_MD 86
Place the power caps close to the relation pins.
C411 .01U/25V/0402
C412 10U/10V/0805
+3.3V_RUN
+3.3V_R5C832
R371 0_0805
(14,17,33,42) AD[0..31]
PCI Bus
PowerOnReset for VccCore
Route GBRST# to GPIOG3 (pin 91) of the SIO companion chip ECE5011, and name the signal CBUS_GRST#. If CBUS_GRST# is controlled by the sysem, then C850 does not need to apply.
If R374 is populated, both C417 and R372 can be depop.
R372 100K_0402
(27) CBUS_GRST#
R374 *0_NC
C417 1U/10V/0603
GBRST# should be asserted only when system power supply is on.
AD31 125
AD30 126
AD29 127
AD28 1
AD27 2
AD26 3
AD25 5
AD24 6
AD23 9
AD22 11
AD21 12
AD20 14
AD19 15
AD18 17
AD17 18
AD16 19
AD15 36
AD14 37
AD13 38
AD12 39
AD11 40
AD10 42
AD9 43
AD8 44
AD7 46
AD6 47
AD5 48
AD4 49
AD3 50
AD2 51
AD1 52
AD0 53
PAR 33
C/BE3# 7
C/BE2# 21
C/BE1# 35
C/BE0# 45
IDSEL 8
REQ# 124
GNT# 123
FRAME# 23
IRDY# 24
TRDY# 25
DEVSEL# 26
STOP# 29
PERR# 30
SERR# 31
GBRST# 71
PCIRST# 119
PCICLK 121
PME# 70
CLKRUN# 117
PCI / OTHER
R5C832T_V00
GND1 4
GND2 13
GND3 22
GND4 28
GND5 54
GND6 62
GND7 63
GND8 68
GND9 118
GND10 122
AGND1 99
AGND2 102
AGND3 103
AGND4 107
AGND5 111
R373 10K_0402
Route to GPIOG6 (pin 94) on the SIO companion chip ECE5011, with the signal named CB_HWSPND#
HWSPND# 69
R375 *0_NC
CB_HWSPND# (27)
MSEN 58
XDEN 55
R517 10K_0402
pull down to disable MS & XD
UDIO5 57
UDIO3 65
UDIO4 59
UDIO2 56
UDIO1 60
UDIO0/SRIRQ# 72
R376 10K_0402
R377 100K_0402
Memory Stick disable
XD Card disable
Serial ROM disable
SD Card Enable
MMC Card Enable
SERIRQ (14,27,42)
Waiting to check LINK SB460 SERIRQ PIN PCLK_PCM
PCI Bus
R559 10K_0402
INTA# 115
INTB# 116
INTE# (14)
1394 Interrupt
Media card Interrupt
TEST 66
T118 PAD
R380 100K_0402
Waiting to check LINK SB460 PCI CLKS PIN PCLK_PCM
PCI Bus
(14,33,42) PAR
(14,33,42) CBE3#
(14,33,42) CBE2#
(14,33,42) CBE1#
(14,33,42) CBE0#
AD17
R378 100_0402
(14) REQ2#
(14) GNT2#
(14,33,42) FRAME#
(14,33,42) IRDY#
(14,33,42) TRDY#
(14,33,42) DEVSEL#
(14,33,42) STOP#
(14,33,42) PERR#
(14,33,42) SERR#
as ED5 application
+3.3V_RUN
Q43
*DTC144EUA_NC
(14,33,42) PCIRST#
(14) PCLK_PCM
(15,24,33) PME#
R379 *0_NC
(14,27,33,42) CLKRUN#
CoreLogic CLOCKRUN#
The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive thesignal low, in order to disable CLKRUN#.
PCLK_PCM
R381 *10_NC
C418 *10P_NC
Refer to DELL M07 schematic X06

QUANTA COMPUTER
Title: 5C832/PCI
Size: Document Number: FX2
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deleted 1394 for defeature

3.AVCC_PHY3V, connection with +3.3V_R5C832 power
4.AVCC_PHY3V, Inductor Required between +3.3V_R5C832 and AVCC_PHY

80 mils

+3.3V_R5C832

+3.3V_RUN_PHY

C423 10U/10V/0805

C424 .1U/10V/0402

C419 .01U/25V/0402

C425 1000P/50V/0402

L43 BLM18PG181SN1D

modify

U15A

Place these caps as close to the U15 as possible.

AVCC_PHY1 98
AVCC_PHY2 106
AVCC_PHY3 110
AVCC_PHY4 112

TPBIAS0 113

94 XI
95 XO
96 FIL0
101 REXT
100 VREF

TPBN0 104
TPBP0 105

5.TPBN1 & TPBP1, Short to GND
if the 1394 Port Is Not Used

TPAN0 108
TPAP0 109

IEEE1394/SD

MDIO17 87
MDIO16 92
MDIO15 89
MDIO14 91
MDIO13 90 SD/XD/MS_DATA3 — SD/XD/MS_DATA3 (22)
MDIO12 93 SD/XD/MS_DATA2 — SD/XD/MS_DATA2 (22)
MDIO11 81 SD/XD/MS_DATA1 — SD/XD/MS_DATA1 (22)
MDIO10 82 SD/XD/MS_DATA0 — SD/XD/MS_DATA0 (22)

MDIO05 75
MDIO08 88 SD/XD/MS_CMD — SD/XD/MS_CMD (22)
MDIO19 83
MDIO18 85
MDIO02 78

changed for SD/MMC/SDIO only

MDIO03 77 SD_WP#(XDR/B#) — SD_WP#(XDR/B#) (22)
MDIO00 80 SD_CD# — SD_CD# (22)
MDIO01 79
MDIO09 84 SD/XD/MS_CLK (22)
MDIO04 76 MC_PWR_CTRL_0 (22)
MDIO06 74 T119 PAD
MDIO07 73

97 RSV

R5C832T_V00

QUANTA COMPUTER

Title	CARD READER	
Size	Document Number FX2	Rev 1A
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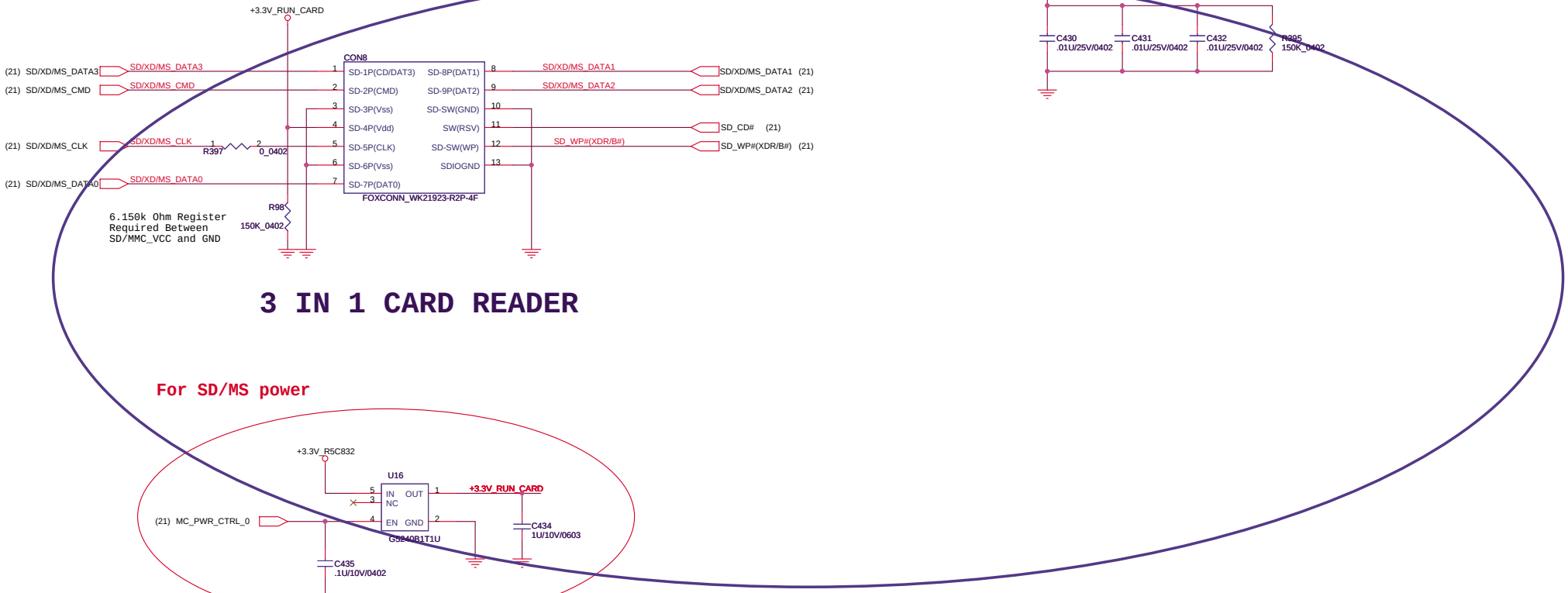
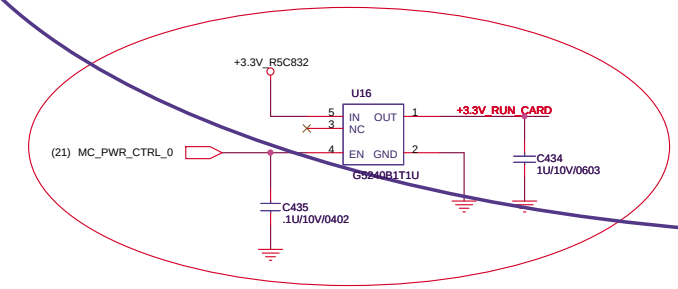
DO NOT INSERT SD/MMC SIMULTANEOUSLY.

changed for SD/MMC/SDIO only



3 IN 1 CARD READER

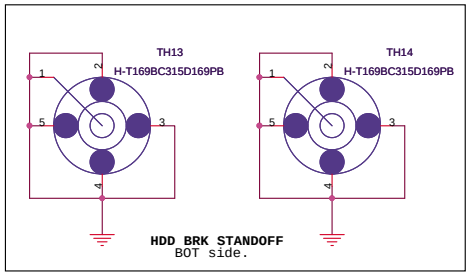
For SD/MS power



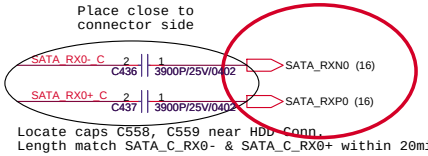
QUANTA COMPUTER

Title	CARD READER CONN	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 22 of 47	

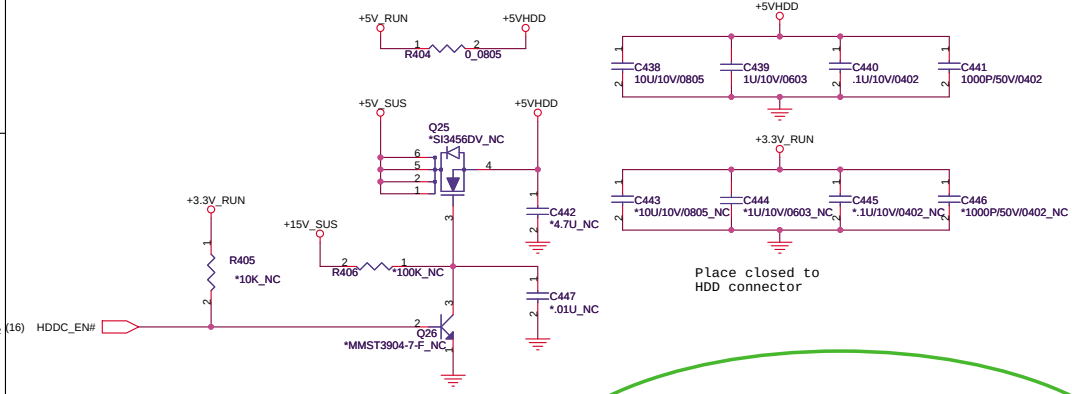
SATA HDD



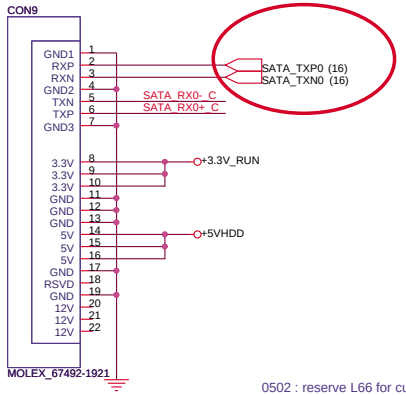
Place close to
connector side



Locate caps C558, C559 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 20mils.



Place closed to
HDD connector



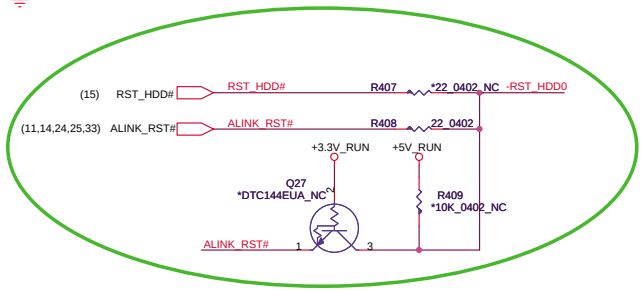
SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.

change name for ED5

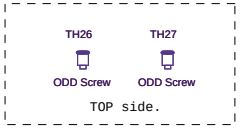
copy ED5 to FX2

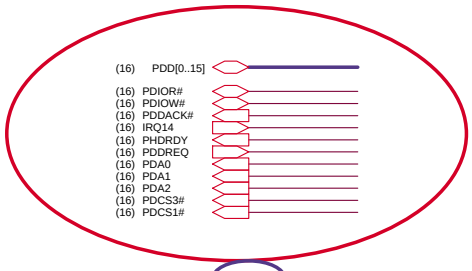
Waiting to check



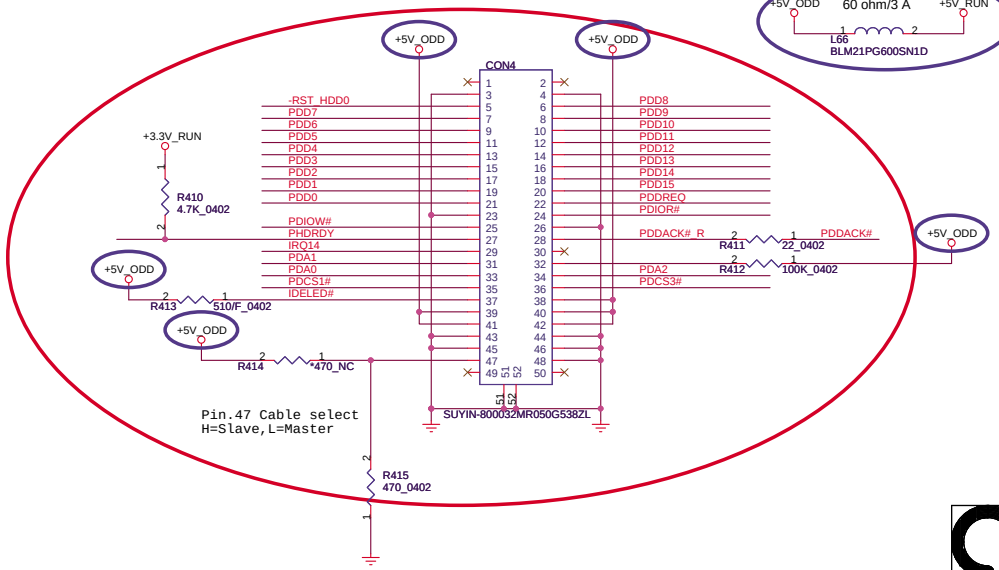
PATA ODD

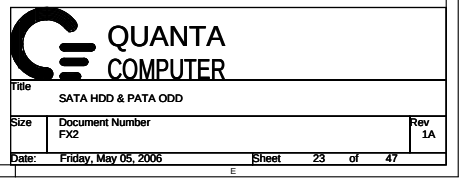
0502 : reserve L66 for current measurement , can be removed and short directly after RTS ; and change +5V_RUN to +5V_ODD for ODD side power



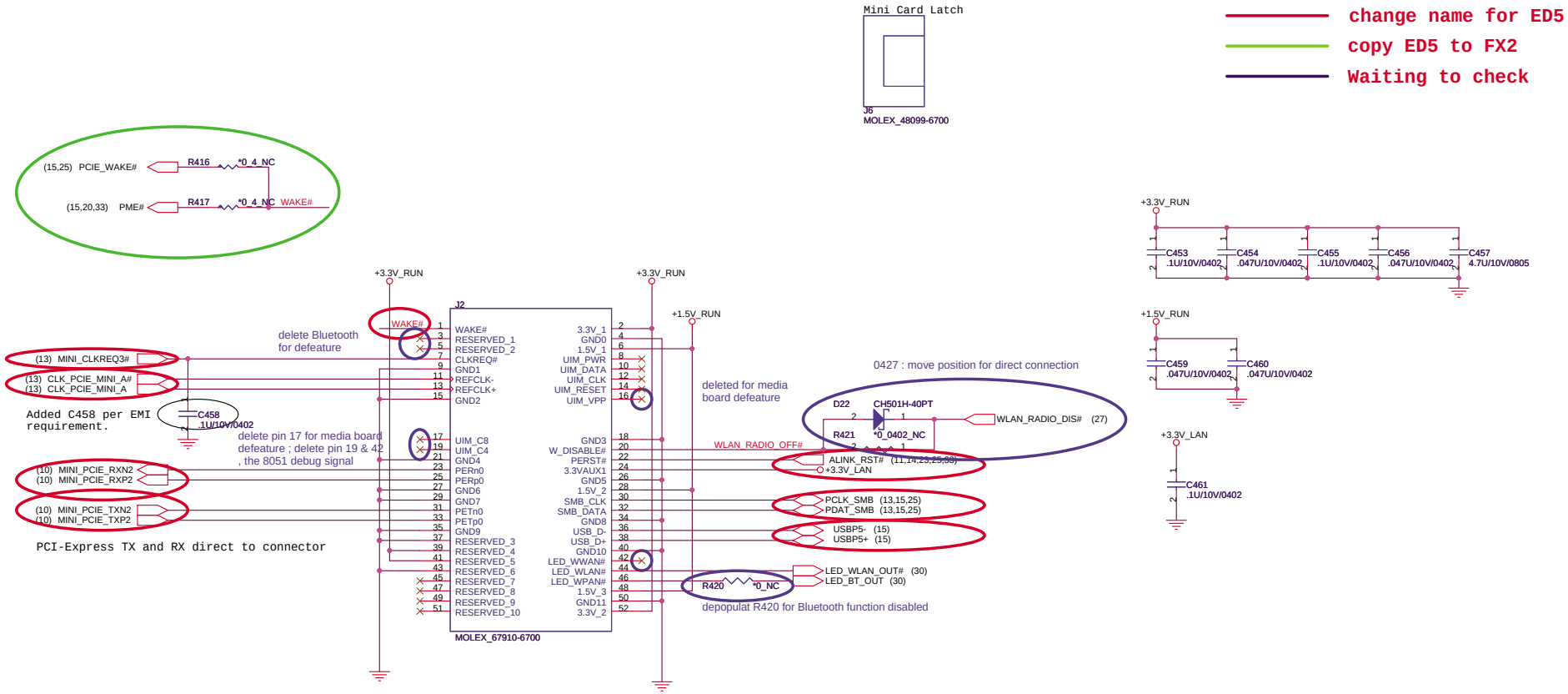


Place closed to
MOD connector





MINI CARD



QUANTA COMPUTER

Title	MINI Card	
Size	Document Number FX2	Rev 1A
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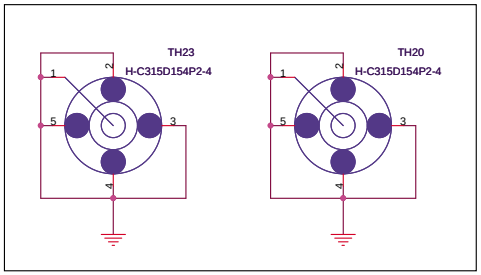
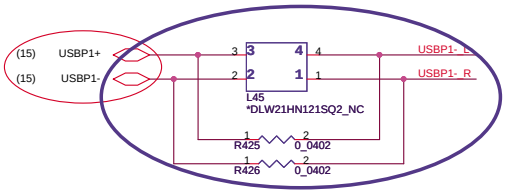
Express Card

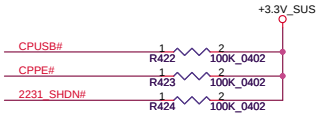


change name for ED5
copy ED5 to FX2
Waiting to check

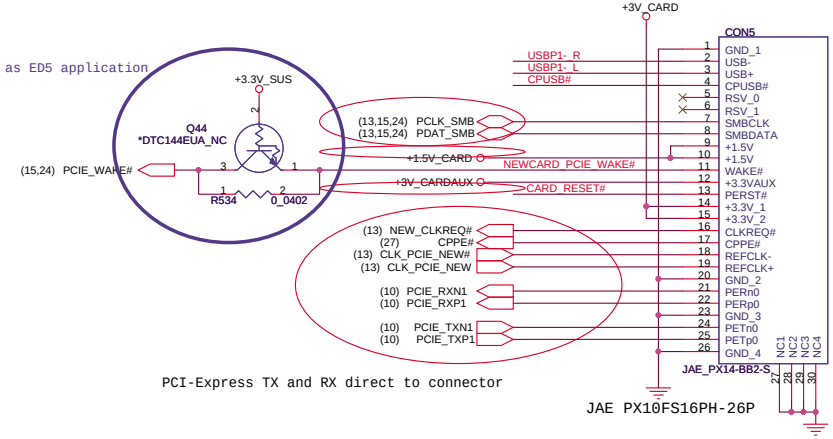
NEW CARD GUIDE POST
TOP side.

swap traces as "fx2_swap-0412"





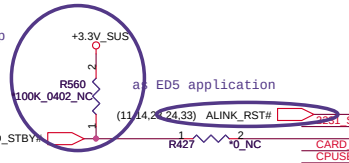
as ED5 application



PCI-Express TX and RX direct to connector

JAE PX10FS16PH-26P

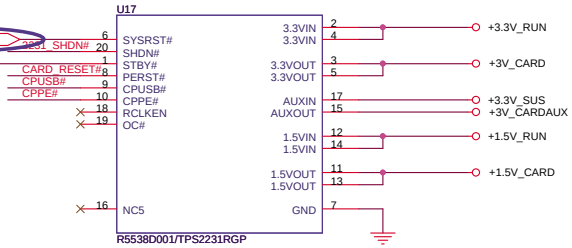
reserve for pull up



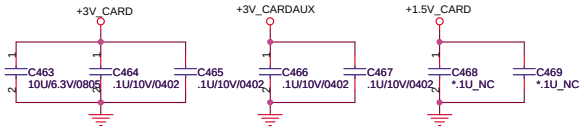
as ED5 application

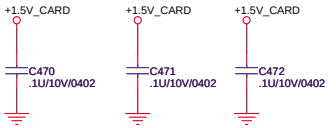
(11,14,24,33) ALINK_RST#

+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

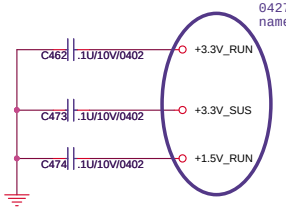


+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA





0427 : change from only net name to symbol "power point"



QUANTA COMPUTER

Title	Express Card	
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MDC INTERFACE

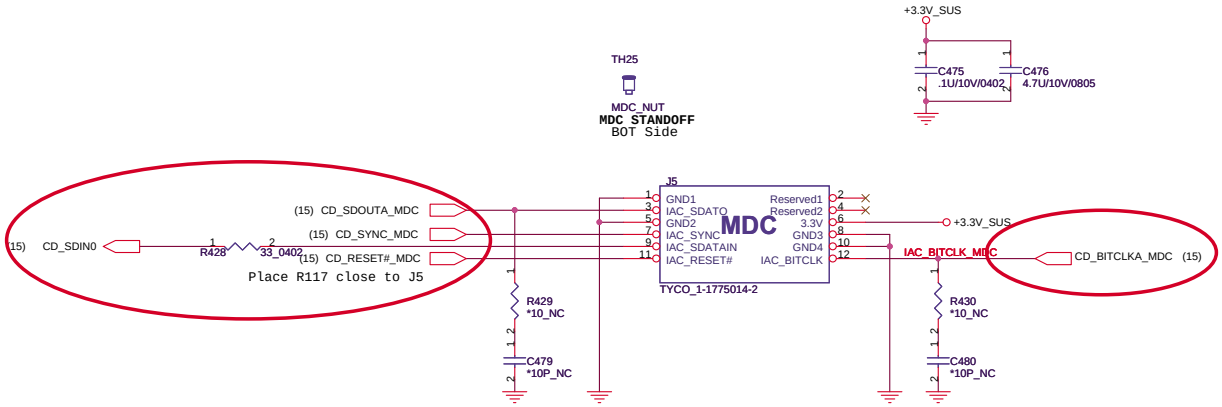
MDC Layout Notes

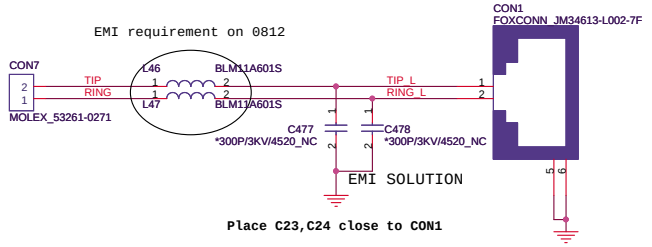
1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG
(stranded or twisted pair wire)

change name for ED5

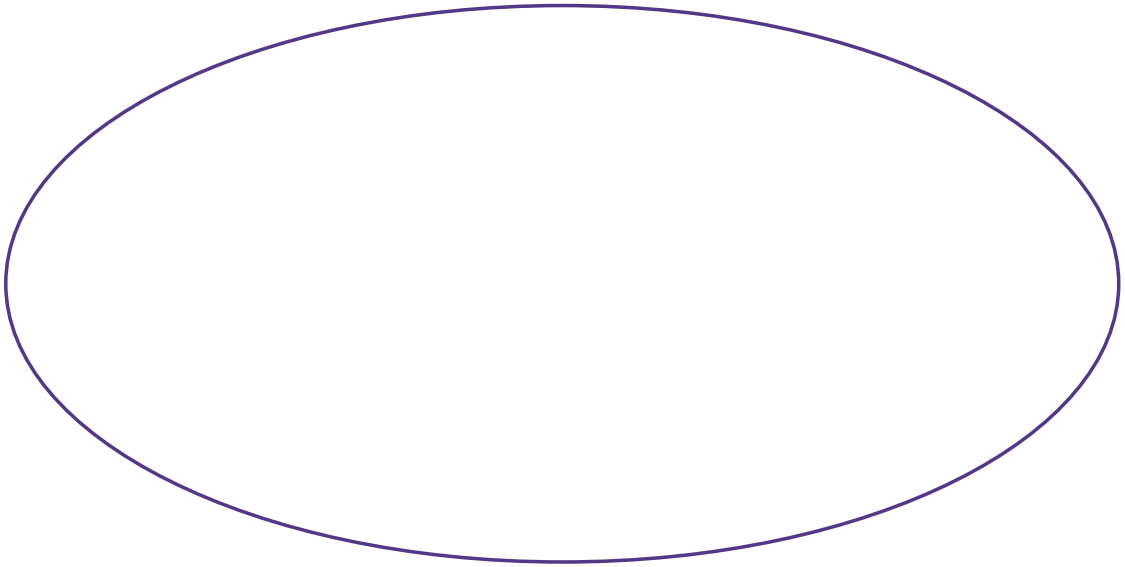
copy ED5 to FX2

Waiting to check





delete Bluetooth
for defeature



QUANTA COMPUTER

Title	MDC CONN	
Size	Document Number FX2	Rev 1A
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EC pin updated as "FX2 KBC GPIO define v14"

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

add R468 for +3.3_SRC & R516 connected to +3.3V_ALW as power concern about the leakage; create +3.3V_97551.

+3.3V_SRC to +3.3V_97551

delete pull up circuit of BT_PWERON#

SHBM=1: Enable shared memory with host BIOS

0502 : added as Loki's suggestion

delete pull up circuit of RF_SW#, TV_SENSE#_D, MONITOR_PLUG#

as FM1

Instant on power switch input only

modify for thermal protect

0427 : change from BREATH_LED to BREATH_LED#

PBAT_SMBCLK/DAT : Charger, Battery
MBCLK/DATA : LCD, Password, CPU internal thermal diode

+3.3V_SRC to +3.3V_97551

delete PLCC32 connector

delete HWPG_1.8V

FOR 97551 ONLY

U18 PC97551/87541

U21 ST Micro M29W008AB/AMD-29LV081B/SST39VF080

U19 M24C08-WMN6TP

Q29 *PDTC143TT_NC

Y6 32.768KHZ

EC & FALSH ROM

DIRECTLY 50 mS

HWPG_591 ===> NB_PWRGD ===> EC_PWRGD

NORTH BRIDGE SOUTH BRIDGE

QUANTA COMPUTER

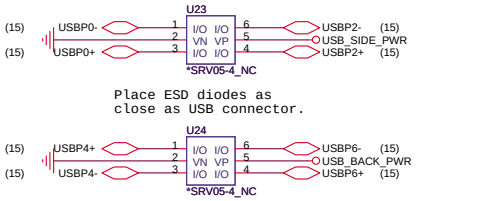
Title	PC97551 & FLASH		
Size	Document Number FX2		Rev 1A
Date: Friday, May 05, 2006		Sheet 27 of 47	

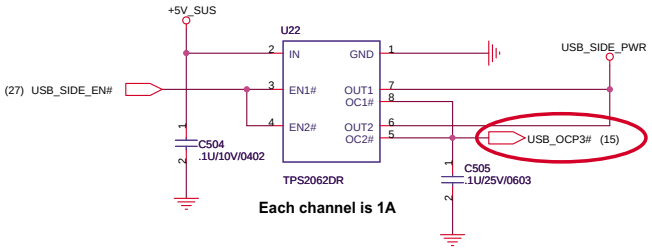
change name for ED5

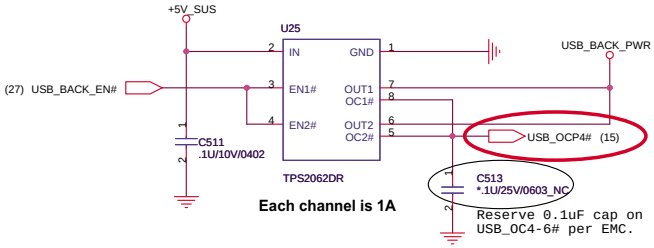
copy ED5 to FX2

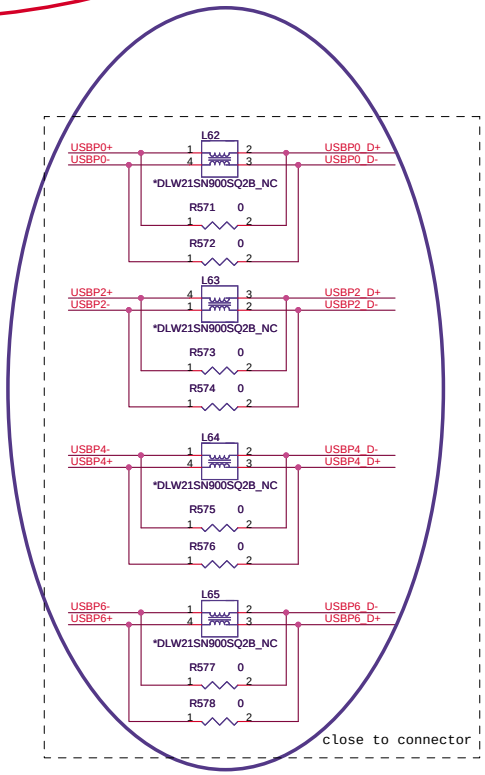
Waiting to check

8Mbit (1M Byte), SPI

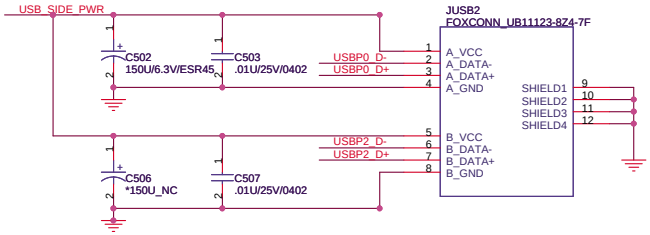


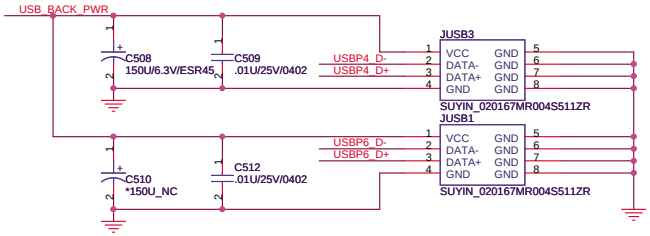






add for EMI suggestion ,
0502 : swap P0/P2 traces as "fx2-swap-0502"





QUANTA COMPUTER

Title	USB	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 28 of 47	

TH3 H-C197D63P2
TH12 H-C197D63P2
TH1 HOLE-C315D126P2-4
TH2 H-C197D63P2
TH4 H-C197D63P2
TH18 H-C197D63P2
TH21 H-C197D63P2

TH16 H-C110D110N
TH22 H-C110D110N

PAD1 e-354x315R
PAD2 e-394x315L
PAD3 e-315x354D

0427 : add 3 pads for EMI need

TH7 H-C197D63P2
TH8 H-C197D63P2
TH10 H-C217D98P2-8
TH11 H-C217D98P2-8
TH24 H-C197D63P2
TH5 H-C197D63P2
TH17 H-C197D63P2

change footprint from
"H-C315D98P2-4" to "H-C217D98P2-8".

PV4 PAD138X98_H:4
PV10 PAD138X98_H:4
PV9 PAD138X98_H:4
PV8 PAD138X98_H:4
PV2 PAD138X98_H:4
PV7 PAD138X98_H:4
PV5 PAD138X98_H:3.5
PV3 PAD138X98_H:4
PV1 PAD138X98_H:3.5
PV6 PAD138X98_H:4
PV11 PAD138X98_H:4

0505 : delete PV12 , caused interference with
power component , EMI confirm no concern

+3.3V_RUN C514 *.1U_NC +1.5V_RUN
+3.3V_RUN C515 *.1U_NC +1.5V_RUN
+3.3V_SUS C516 *.1U_NC +5V_SUS
+3.3V_RUN C517 *.1U_NC +5V_SUS
+3.3V_RUN C518 *.1U_NC +5V_SUS

+PWR_SRC C519 *.1U_NC +5V_SUS
+PWR_SRC C520 *.1U_NC +5V_SUS
+PWR_SRC C521 *.1U_NC +5V_SUS
+PWR_SRC C522 *.1U_NC +5V_SUS
+PWR_SRC C523 *.1U_NC +3.3V_RUN
+PWR_SRC C524 *.1U_NC
+PWR_SRC C525 *.1U_NC
DC_IN+ C526 *.1U_NC
+1.5V_RUN C527 *.1U_NC
+1.5V_RUN C528 *.1U_NC
+1.5V_RUN C529 *.1U_NC
+1.5V_RUN C530 *.1U_NC
+1.5V_RUN C531 *.1U_NC
+1.5V_RUN C532 *.1U_NC
+1.5V_RUN C533 *.1U_NC
+3.3V_SUS C534 *.1U_NC

+PWR_SRC C535 .1U/25V/0603
+PWR_SRC C536 .1U/25V/0603
+PWR_SRC C537 .1U/25V/0603
+PWR_SRC C538 .1U/25V/0603
+PWR_SRC C539 .1U/25V/0603
+PWR_SRC C540 .1U/25V/0603

0502 : reserve 20 pcs of 4700pF stiching Cap. from +1.8V_SUS to GND for EMI concern

+1.8V_SUS C681 *4700P/25V/0402_NC
+1.8V_SUS C682 *4700P/25V/0402_NC
+1.8V_SUS C683 *4700P/25V/0402_NC
+1.8V_SUS C684 *4700P/25V/0402_NC
+1.8V_SUS C685 *4700P/25V/0402_NC
+1.8V_SUS C686 *4700P/25V/0402_NC
+1.8V_SUS C687 *4700P/25V/0402_NC
+1.8V_SUS C688 *4700P/25V/0402_NC

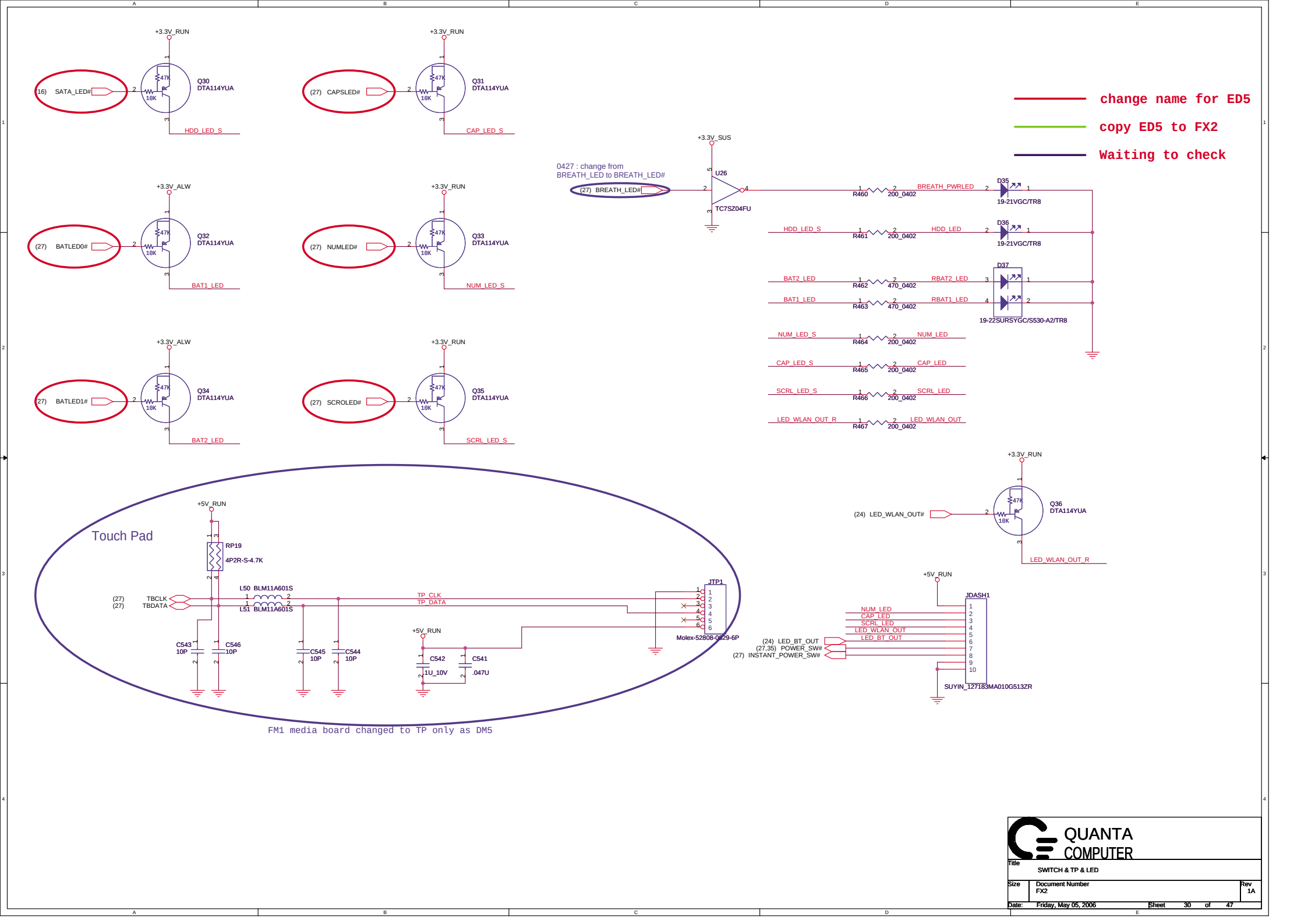
place close to CPU

+1.8V_SUS C689 *4700P/25V/0402_NC
+1.8V_SUS C690 *4700P/25V/0402_NC
+1.8V_SUS C691 *4700P/25V/0402_NC
+1.8V_SUS C692 *4700P/25V/0402_NC
+1.8V_SUS C693 *4700P/25V/0402_NC
+1.8V_SUS C694 *4700P/25V/0402_NC
+1.8V_SUS C695 *4700P/25V/0402_NC
+1.8V_SUS C696 *4700P/25V/0402_NC
+1.8V_SUS C697 *4700P/25V/0402_NC
+1.8V_SUS C698 *4700P/25V/0402_NC
+1.8V_SUS C699 *4700P/25V/0402_NC
+1.8V_SUS C700 *4700P/25V/0402_NC

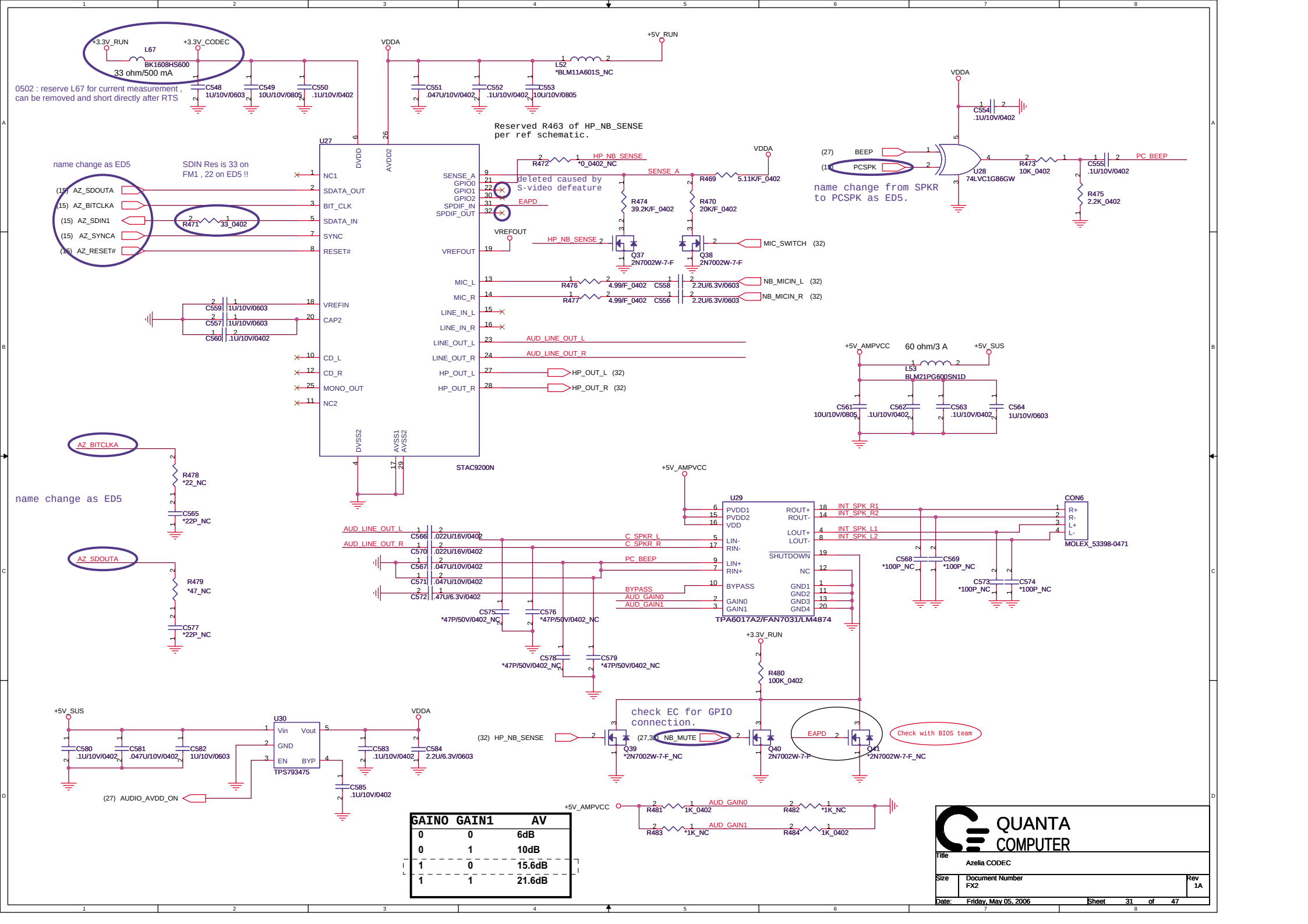
place close to DDR II connector

QUANTA COMPUTER

Title	EMI & Screw hole	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 29 of 47	



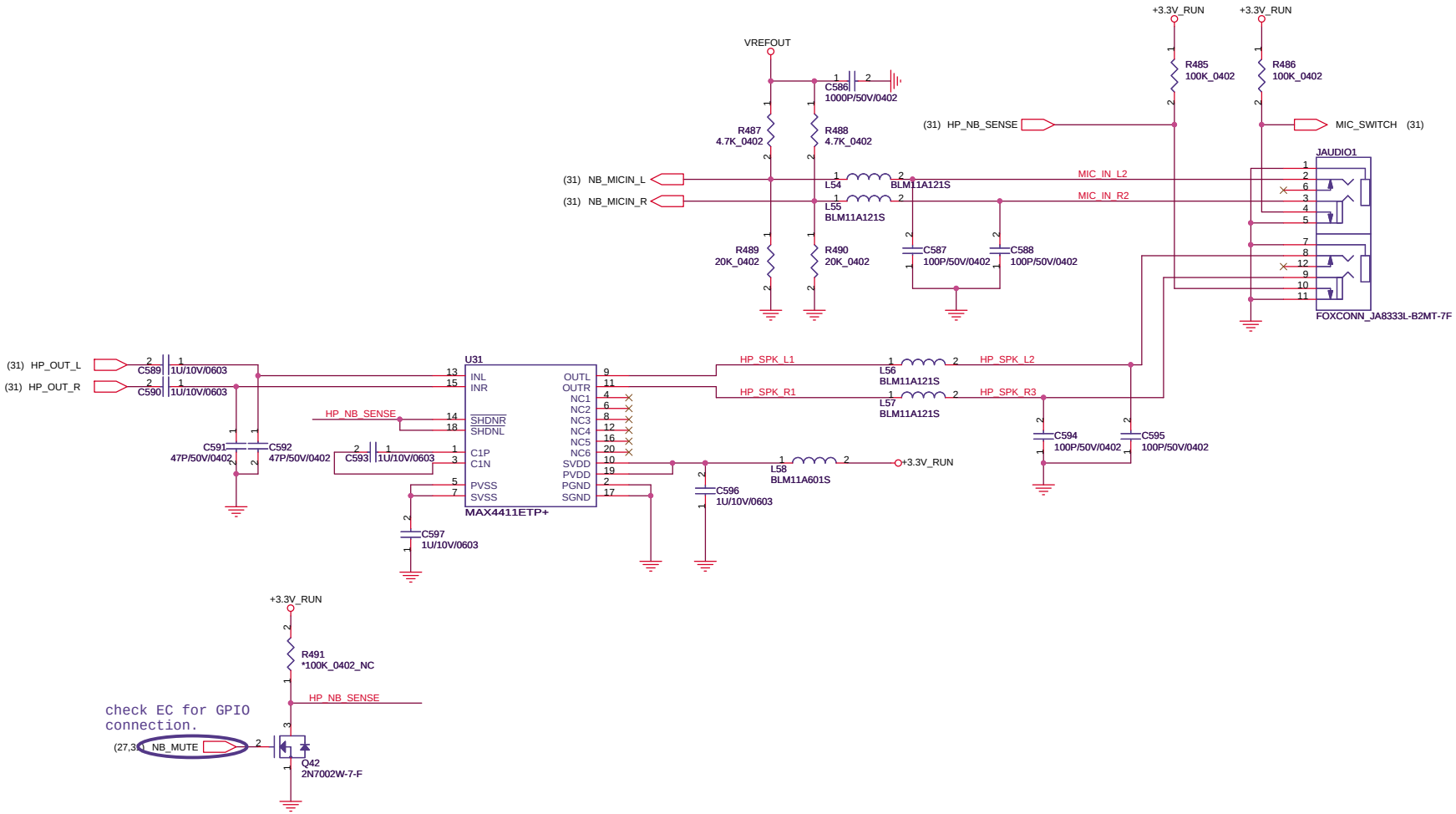
QUANTA COMPUTER		
Title	SWITCH & TP & LED	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 30 of 47	



GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

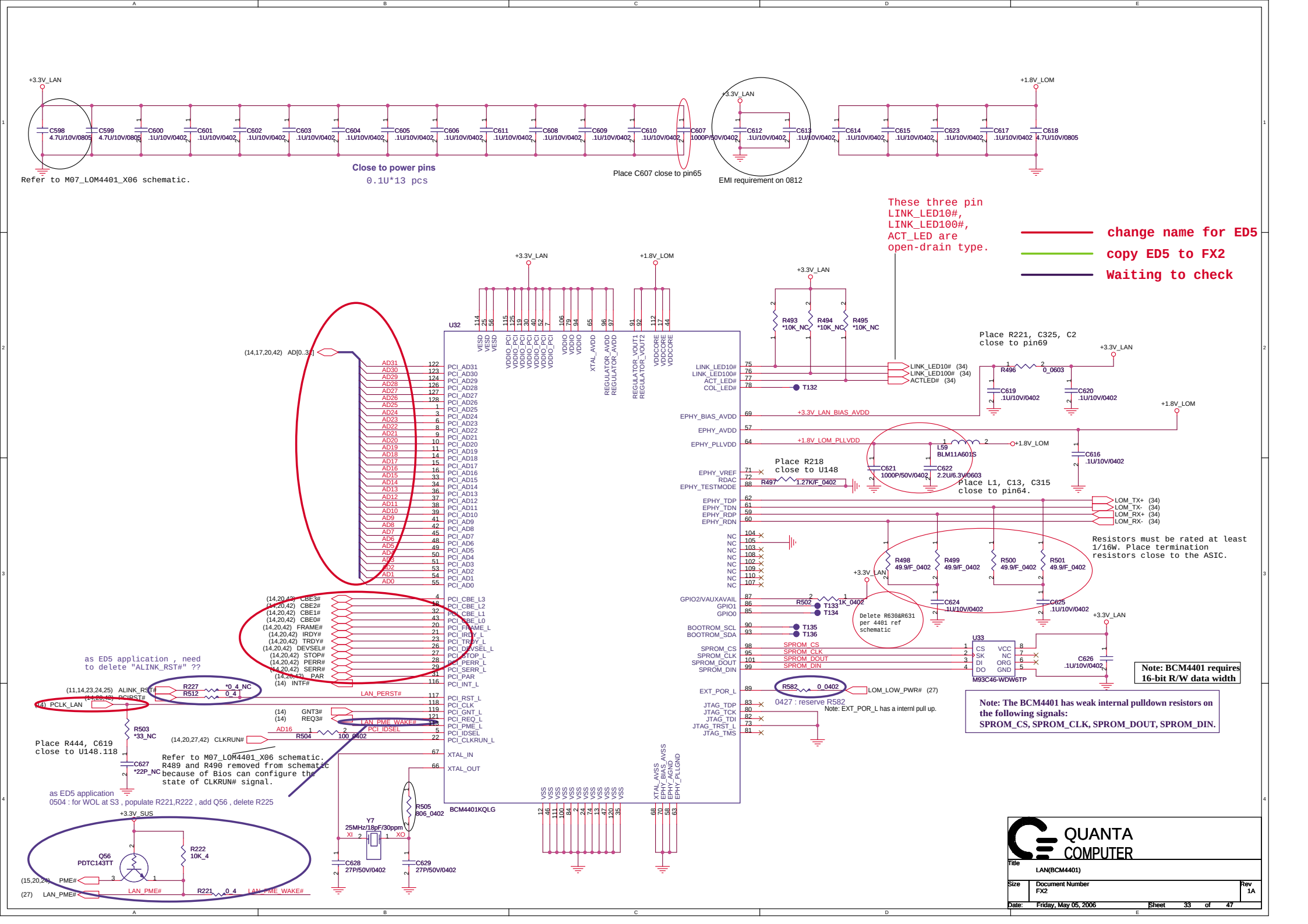
QUANTA COMPUTER

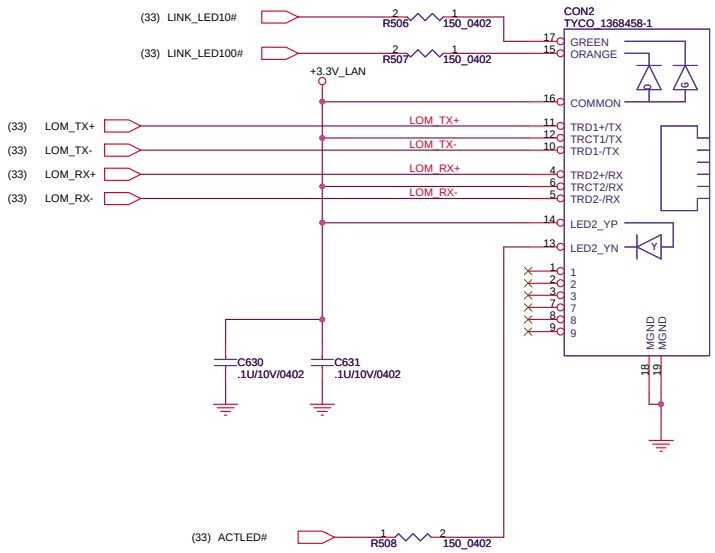
Title	Azelia CODEC	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 31 of 47	



QUANTA COMPUTER

Title	AUDIO CONN	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 32 of 47	


+3.3V_LAN
+1.8V_LOM
C598 4.7U/10V/0805
C599 4.7U/10V/0805
C600 .1U/10V/0402
C601 .1U/10V/0402
C602 .1U/10V/0402
C603 .1U/10V/0402
C604 .1U/10V/0402
C605 .1U/10V/0402
C606 .1U/10V/0402
C611 .1U/10V/0402
C608 .1U/10V/0402
C609 .1U/10V/0402
C610 .1U/10V/0402
C607 1000P/50V/0402
C612 .1U/10V/0402
C613 .1U/10V/0402
C614 .1U/10V/0402
C615 .1U/10V/0402
C623 .1U/10V/0402
C617 .1U/10V/0402
C618 4.7U/10V/0805
Refer to M07_LOM4401_X06 schematic.
Close to power pins
0.1U*13 pcs
Place C607 close to pin65
EMI requirement on 0812
These three pin LINK_LED10#, LINK_LED100#, ACT_LED are open-drain type.
change name for ED5
copy ED5 to FX2
Waiting to check
U32
BCM4401KQLG
R493 *10K_NC
R494 *10K_NC
R495 *10K_NC
T132
Place R221, C325, C2 close to pin69
R496 0_0603
C619 .1U/10V/0402
C620 .1U/10V/0402
L59 BLM11A601S
C621 1000P/50V/0402
C622 2.2U/6.3V/0603
C616 .1U/10V/0402
Place R218 close to U148
R497 1.27K/F_0402
Place L1, C13, C315 close to pin64.
R498 49.9/F_0402
R499 49.9/F_0402
R500 49.9/F_0402
R501 49.9/F_0402
C624 .1U/10V/0402
C625 .1U/10V/0402
Resistors must be rated at least 1/16W. Place termination resistors close to the ASIC.
R502 1K_0402
T133
T134
Delete R630&R631 per 4401 ref schematic
T135
T136
U33
M93C46-WDW6TP
C626 .1U/10V/0402
Note: BCM4401 requires 16-bit R/W data width
R582 0_0402
0427 : reserve R582
Note: EXT_POR_L has a internl pull up.
Note: The BCM4401 has weak internal pulldown resistors on the following signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.
as ED5 application , need to delete "ALINK_RST#" ??
R227 *0_4_NC
R512 0_4
R503 *33_NC
C627 *22P_NC
Place R444, C619 close to U148.118
Refer to M07_LOM4401_X06 schematic. R489 and R490 removed from schematic because of Bios can configure the state of CLKRUN# signal.
R504 100_0402
as ED5 application
0504 : for WOL at S3 , populate R221,R222 , add Q56 , delete R225
+3.3V_SUS
Q56 PDTC143TT
R222 10K_4
R221 0_4
LAN_PME#
LAN_PME_WAKE#
Y7 25MHz/18pF/30ppm
R505 806_0402
C628 27P/50V/0402
C629 27P/50V/0402
QUANTA COMPUTER
Title: LAN(BCM4401)
Size: Document Number: FX2
Rev: 1A
Date: Friday, May 05, 2006
Sheet 33 of 47

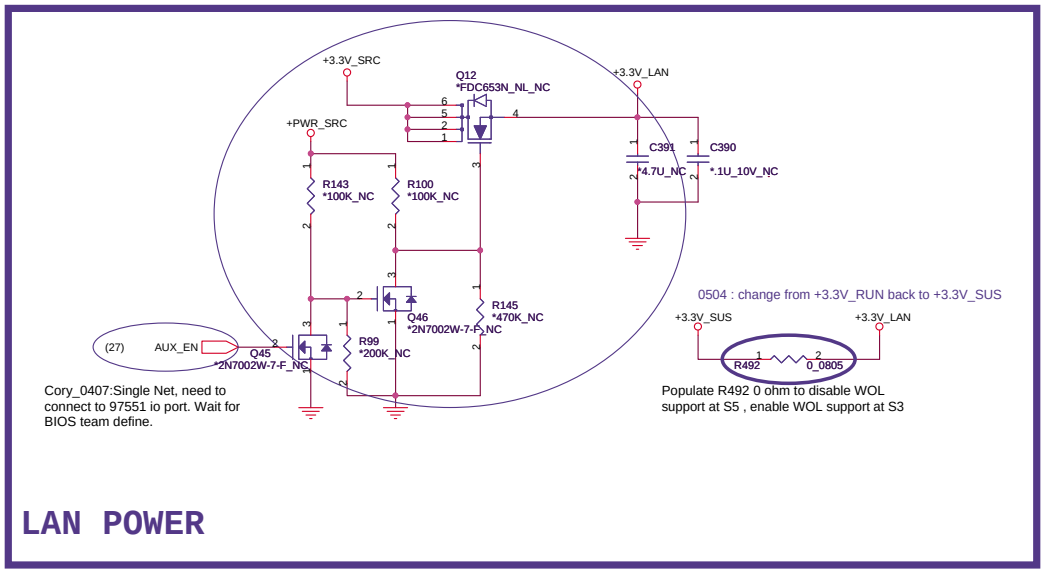


change name for ED5

copy ED5 to FX2

Waiting to check

copy DM5 to FX2



LAN POWER

QUANTA COMPUTER

Title	LAN JACK	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 34 of 47	

add Thermal IC as FM1

H_THERMDA&h_THERMDC
trace routing = W:10/S:10

(5) CPU_TEST4_THERMDA
(5) CPU_TEST5_THERMDC

Place C653 close to U36

C653 2200P/50V/0402

U36 EMC4000

+3.3V_SUS
R536 7.5K/F_0402
(18,27) MBDATA
(18,27) MBCLK
SMDATA
SMBCLK
LDO_SHDN#_ADDR
DP2
DN2
+3V_SUS
VSUS_PWRGD
+RTC_PWR3V
+3V_PWROK#
POWER_SW#
THERMTRIP1#
THERMTRIP2#
THERMTRIP3#
VSET
HW_LOCK#
VSS
FAN_DAC
FAN_OUT
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5

+3.3V_SUS
R537 49.9/F_0402
+3VSUS_THRM
C655 .1U/10V/0402
VCCRTC
C658 .1U/10V/0402
SUSPWROK
R539 1K_0402
EC_PWRGD#
R540 1K_0402
(27,30) POWER_SW#
THERMTRIP1#

+3.3V_SUS
R554 10K_0402
C663 .1U/10V/0402
R542 147K/F_0402
R543 41.2K_0402
C664 2200P/50V/0402
R544 1K_0402
VSET
HW_LOCK#
FAN1_VOUT

+3.3V_SUS
R552 10K_0402
ATF_INT# (27)
ATF_INT#
VCP1
VCP2
delete single net "VCP1" & "VCP2"
LDO_POK
R553 10K_0402
+3.3V_RUN

Place Q50 at bottom of CPU
REM_DIODE1_N & REM_DIODE1_P trace routing = W:10/S:10
Place C656 close to the pins as possible.
DN1
DP1
REM_DIODE1_N
REM_DIODE1_P
C656 2200P/50V/0402
Q50 MMST3904-7-F
C657 *2200P_NC
Place C657 close to the Q50

THERMTRIP_SIO
R541 10K_0402
+3.3V_ALW
THERMTRIP_SIO (27)
ACAvail_Clr
ACAV_IN (27,36)
SYS_SHDN#
R555 *10K_0402_NC
THERM_SYS_PWR# (27,38)
VCCRTC
VDD_5V
+5V_RUN
LDO_OUT
LDO_OUT
+2.5V_RUN
LDO_IN
LDO_IN
+3.3V_RUN_IN
R545 0_1210
+3.3V_RUN

REM_DIODE3_N & REM_DIODE3_P trace routing = W:10/S:10
DP3
DN3
REM_DIODE3_P
REM_DIODE3_N
LDO_SET
C668 2200P/50V/0402
Q51 MMST3904-7-F
C669 *2200P_NC
Place C669 close to Q51
Place Q51 Near the SO-DIMM.
Place C668 close to U36

+3.3V_RUN
R535 10K_0402
FAN1_TACH (27)
R538 0_0402
FAN1
J3
FAN1_VOUT
FAN1_TACH_FB
VCC
SIG
GND
MOLEX_53398-0371
D39 *CH751H-40HPT_NC
C654 22U/10V/1206

+5V_RUN
C659 10U/10V/0805
C660 .1U/10V/0402
+2.5V_RUN
C661 10U/10V/0805
C662 .1U/10V/0402
Place C659~C662, C665~C667, close to U36

+3.3V_RUN_IN
C665 1U/10V/0603
C666 .1U/10V/0402
C667 *10U_NC

Notes:
Vset=(Tp-70)/21
3.3*(R543/R542+R543)=(Tp-70)/21
Where Tp=70 to 101 degree C
Set trip point=85 degree C
Vset = (85-75)/16= 0.625 V
Guardian II temp-tolerance= +/-3 degree C

+3.3V_SUS
R546 100K_0402
EC_PWRGD#
(14,15,27) EC_PWRGD
Q52 2N7002W-7-F

VLDT_RUN
R549 2.2K_0402
+3.3V_SUS
R547 8.2K_0402
THERMTRIP1#
Q53 MMST3904-7-F
C670 .1U/10V/0402
(5) H_THERMTRIP#
C670 needs to be placed near Guardian IC.

+2.5V_RUN
R548 *31.5K_NC
LDO_SET
R550 1K_0603
Voltage margining circuit for LDO output.
For Vmargin, stuff R548 and R550=30K.
R550=1K for production

as FM1 keyboard matrix & "e0788.1104a_swap-0422"

JKB1
(27) MY9 MY9 1
(27) MY10 MY10 2
(27) MY8 MY8 3
(27) MY13 MY13 4
(27) MY12 MY12 5
(27) MY14 MY14 6
(27) MY15 MY15 7
(27) MY11 MY11 8
(27) MY0 MY0 9
(27) MY2 MY2 10
(27) MY1 MY1 11
(27) MY3 MY3 12
(27) MY7 MY7 13
(27) MY5 MY5 14
(27) MY6 MY6 15
(27) MY4 MY4 16
(27) MY16 MY16 17
(27) MX7 MX7 18
(27) MX4 MX4 19
(27) MX6 MX6 20
(27) MX2 MX2 21
(27) MX5 MX5 22
(27) MX3 MX3 23
(27) MX1 MX1 24
(27) MX0 MX0 25
HRS_FH28D-50(25)SB-1SH(86)

+3.3V_SUS
RP20 10KX8 MX0 MX1 MX3 MX5 MX7 MX4 MX6 MX2
RP21 10KX8 MY16 MY4 MY6 MY5 MY2 MY1 MY3 MY7
RP22 10KX8 MY0 MY11 MY15 MY14 MY10 MY8 MY13 MY12

CA1 *220PX4_NC MX0 MX1 MX3 MX5 MX7 MX4 MX6 MX2
CA2 *220PX4_NC
CA3 *220PX4_NC MY16 MY4 MY6 MY5 MY2 MY1 MY3 MY7
CA4 *220PX4_NC
CA5 *220PX4_NC MY0 MY11 MY15 MY14 MY10 MY8 MY13 MY12
CA6 *220PX4_NC

+3.3V_SUS
R513 10K_0402
MY9
C638 *220P/50V/0402_NC

wait to discuss !!
(27,38,39,40) SUSON
+1.8V_SUS
+3.3V_ALW
+3.3V_SUS
+3.3V_SUS
R557 10K_0402
R556 100K_0402
U38 TC7SZ04FU
C671 *.047U_NC
U39 TC7SZ08FU
SUSPWROK
Q54 3904
C672 1U/50V/0603

0427 : change Q54 from 2N7002W-7-F to 3904 ; C672 from .1U/10V/0402 to .1U/50V/0603 as voltage level & timing concern

KBC

QUANTA COMPUTER

Title	KB & THERMAL & FAN	
Size	Document Number FX2	Rev 1A
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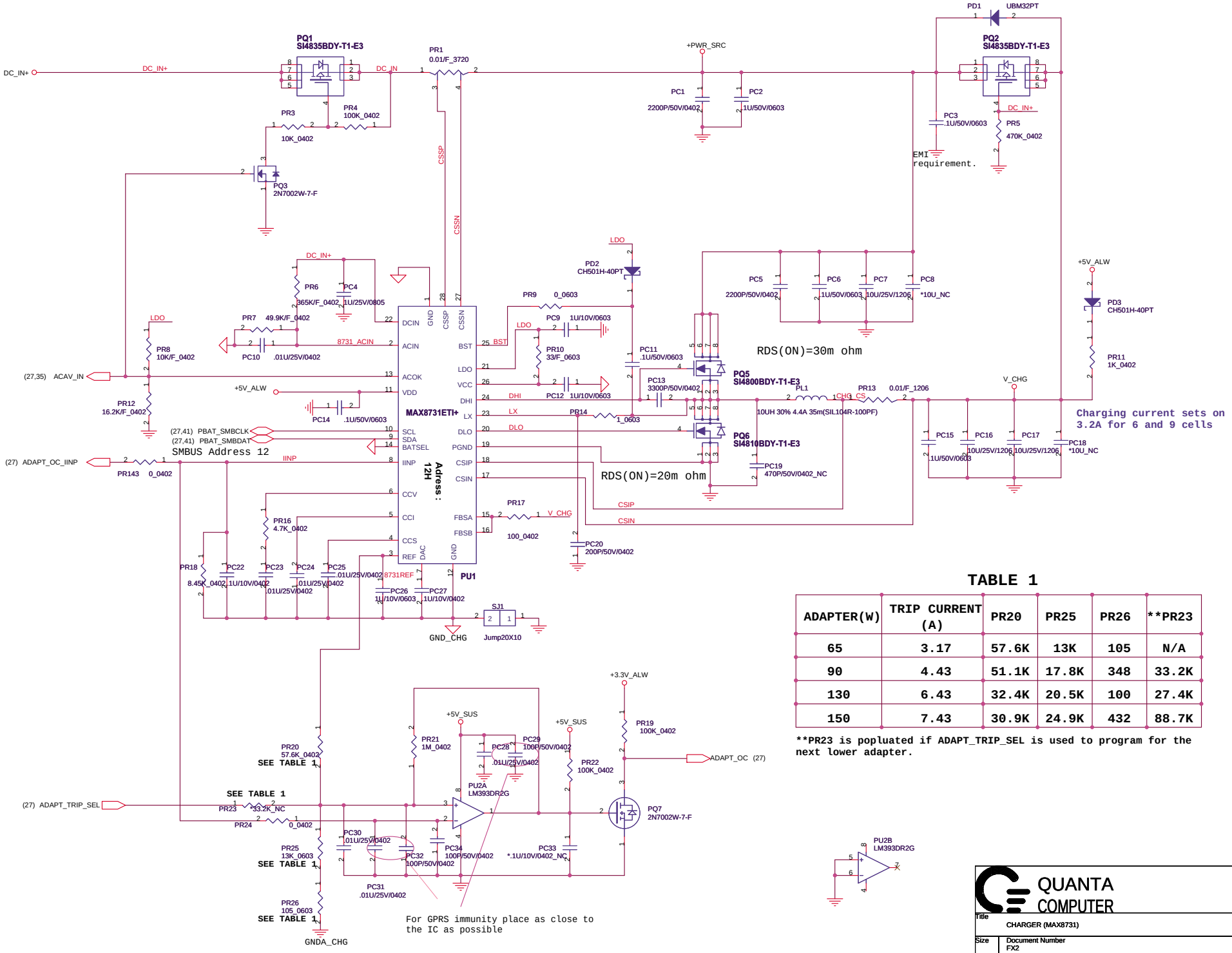


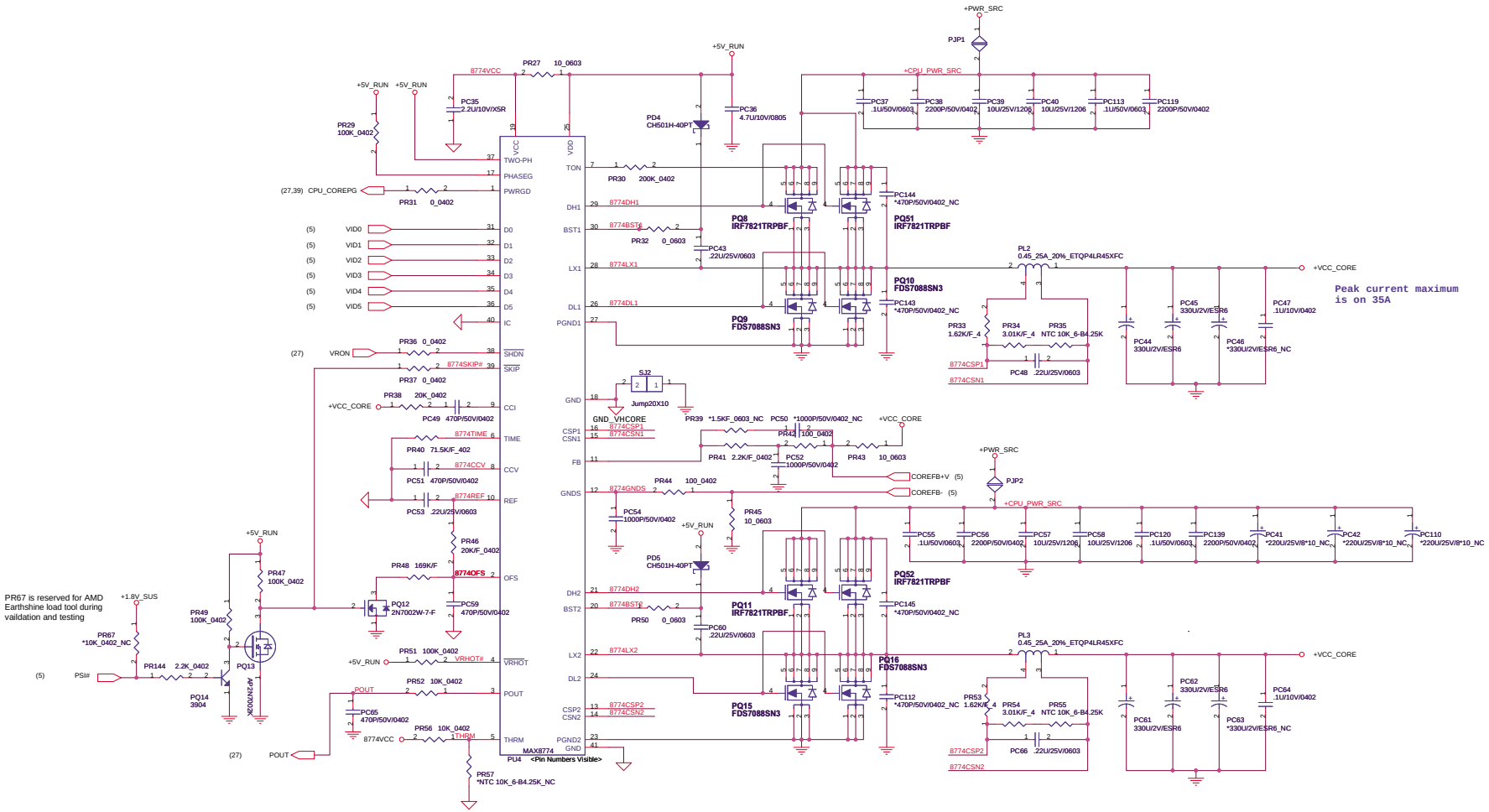
TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	PR20	PR25	PR26	**PR23
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K

**PR23 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

QUANTA COMPUTER

Title	CHARGER (MAX8731)	
Size	Document Number FX2	Rev 1A
Date: 2005/4/21	Sheet 36 of 47	



D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V
0	0	0	0	0	1	1.5250V
0	0	0	0	1	0	1.5000V
0	0	0	0	1	1	1.4750V
0	0	0	1	0	0	1.4500V
0	0	0	1	0	1	1.4250V
0	0	0	1	1	0	1.4000V
0	0	0	1	1	1	1.3750V
0	0	1	0	0	0	1.3500V
0	0	1	0	0	1	1.3250V
0	0	1	0	1	0	1.3000V
0	0	1	0	1	1	1.2750V
0	0	1	1	0	0	1.2500V
0	0	1	1	0	1	1.2250V
0	0	1	1	1	0	1.2000V
0	0	1	1	1	1	1.1750V
0	1	0	0	0	0	1.1500V
0	1	0	0	0	1	1.1250V
0	1	0	0	1	0	1.1000V
0	1	0	0	1	1	1.0750V
0	1	0	1	0	0	1.0500V
0	1	0	1	0	1	1.0250V
0	1	0	1	1	0	1.0000V
0	1	0	1	1	1	0.9750V
0	1	1	0	0	0	0.9500V
0	1	1	0	0	1	0.9250V
0	1	1	0	1	0	0.9000V
0	1	1	0	1	1	0.8750V
0	1	1	1	0	0	0.8500V
0	1	1	1	0	1	0.8250V
0	1	1	1	1	0	0.8000V
0	1	1	1	1	1	0.7750V

D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	0.7625V
1	0	0	0	0	1	0.7500V
1	0	0	0	1	0	0.7375V
1	0	0	0	1	1	0.7250V
1	0	0	1	0	0	0.7125V
1	0	0	1	0	1	0.7000V
1	0	0	1	1	0	0.6875V
1	0	0	1	1	1	0.6750V
1	0	1	0	0	0	0.6625V
1	0	1	0	0	1	0.6500V
1	0	1	0	1	0	0.6375V
1	0	1	0	1	1	0.6250V
1	0	1	1	0	0	0.6125V
1	0	1	1	0	1	0.6000V
1	0	1	1	1	0	0.5875V
1	0	1	1	1	1	0.5750V
1	1	0	0	0	0	0.5625V
1	1	0	0	0	1	0.5500V
1	1	0	0	1	0	0.5375V
1	1	0	0	1	1	0.5250V
1	1	0	1	0	0	0.5125V
1	1	0	1	0	1	0.5000V
1	1	0	1	1	0	0.4875V
1	1	0	1	1	1	0.4750V
1	1	1	0	0	0	0.4625V
1	1	1	0	0	1	0.4500V
1	1	1	0	1	0	0.4375V
1	1	1	0	1	1	0.4250V
1	1	1	1	0	0	0.4125V
1	1	1	1	0	1	0.4000V
1	1	1	1	1	0	0.3875V
1	1	1	1	1	1	0.3750V

QUANTA COMPUTER

Title	VHCORE (MAX8774)	
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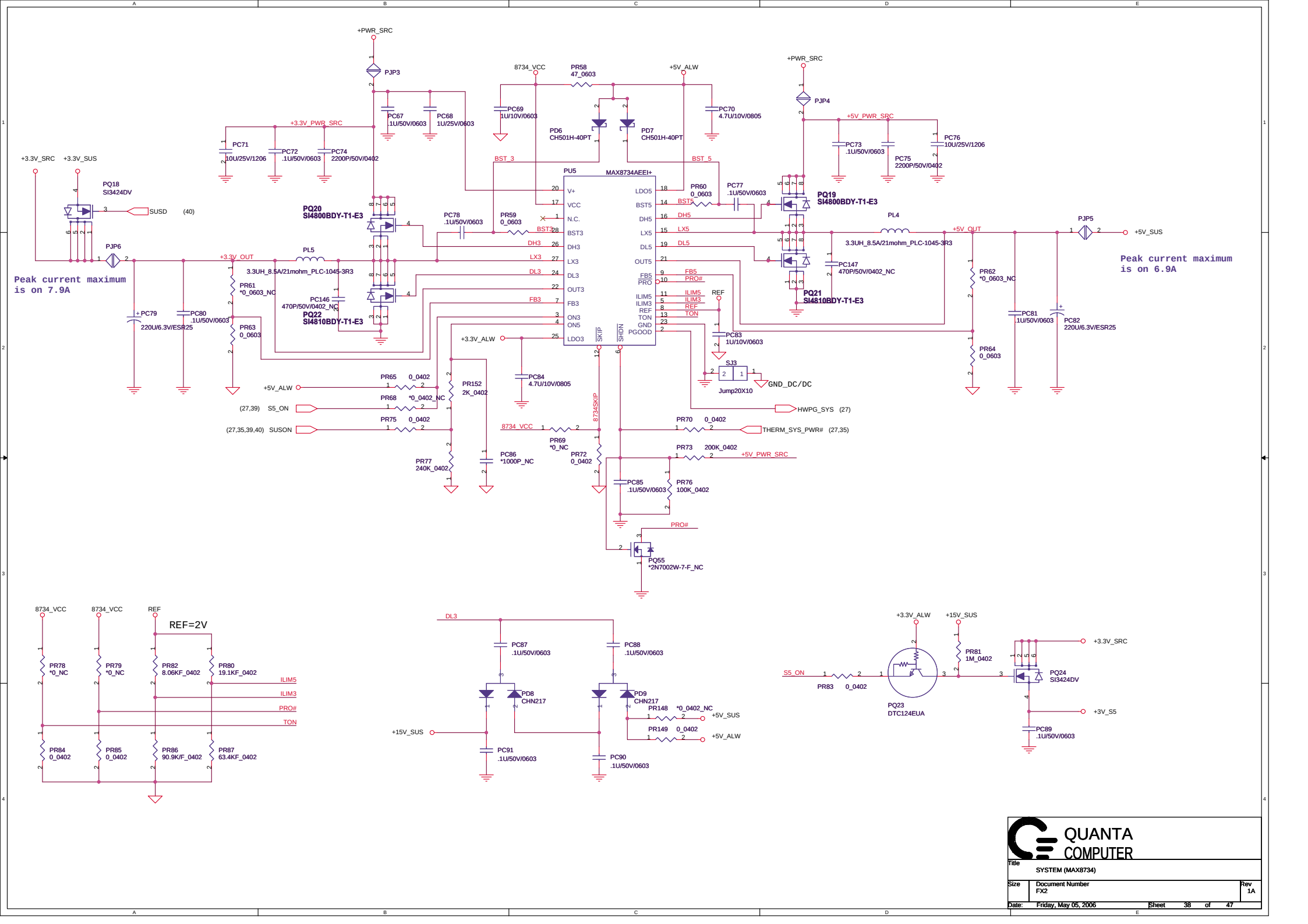
+PWR_SRC
PJP3
PJP4
PJP5
PJP6
8734_VCC
+5V_ALW
+3.3V_PWR_SRC
+5V_PWR_SRC
+3.3V_SRC
+3.3V_SUS
+5V_SUS
+3.3V_OUT
+5V_OUT
PU5
MAX8734AEEI+
V+
VCC
N.C.
BST3
DH3
LX3
DL3
OUT3
FB3
ON3
ON5
LDO3
LDO5
BST5
DH5
LX5
DL5
OUT5
FB5
PRO
ILIM5
ILIM3
REF
TON
GND
PGOOD
SKIP
SHDN
PQ18
SI3424DV
PQ19
SI4800BDY-T1-E3
PQ20
SI4800BDY-T1-E3
PQ21
SI4810BDY-T1-E3
PQ22
SI4810BDY-T1-E3
PQ23
DTC124EUA
PQ24
SI3424DV
PQ55
*2N7002W-7-F_NC
PL4
PL5
3.3UH_8.5A/21mohm_PLC-1045-3R3
PD6
CH501H-40PT
PD7
CH501H-40PT
PD8
CHN217
PD9
CHN217
SJ3
Jump20X10
GND_DC/DC
SUSD
(40)
Peak current maximum
is on 7.9A
Peak current maximum
is on 6.9A
(27,39) S5_ON
(27,35,39,40) SUSON
HWPG_SYS (27)
THERM_SYS_PWR# (27,35)
8734SKIP
REF=2V
ILIM5
ILIM3
PRO#
TON
DL3
+15V_SUS
+3.3V_ALW
+3V_S5
PC67 .1U/50V/0603
PC68 1U/25V/0603
PC69 1U/10V/0603
PC70 4.7U/10V/0805
PC71 10U/25V/1206
PC72 .1U/50V/0603
PC73 .1U/50V/0603
PC74 2200P/50V/0402
PC75 2200P/50V/0402
PC76 10U/25V/1206
PC77 .1U/50V/0603
PC78 .1U/50V/0603
PC79 220U/6.3V/ESR25
PC80 .1U/50V/0603
PC81 .1U/50V/0603
PC82 220U/6.3V/ESR25
PC83 1U/10V/0603
PC84 4.7U/10V/0805
PC85 .1U/50V/0603
PC86 *1000P_NC
PC87 .1U/50V/0603
PC88 .1U/50V/0603
PC89 .1U/50V/0603
PC90 .1U/50V/0603
PC91 .1U/50V/0603
PC146 470P/50V/0402_NC
PC147 470P/50V/0402_NC
PR58 47_0603
PR59 0_0603
PR60 0_0603
PR61 *0_0603_NC
PR62 *0_0603_NC
PR63 0_0603
PR64 0_0603
PR65 0_0402
PR68 *0_0402_NC
PR69 *0_NC
PR70 0_0402
PR72 0_0402
PR73 200K_0402
PR75 0_0402
PR76 100K_0402
PR77 240K_0402
PR78 *0_NC
PR79 *0_NC
PR80 19.1KF_0402
PR81 1M_0402
PR82 8.06KF_0402
PR83 0_0402
PR84 0_0402
PR85 0_0402
PR86 90.9K/F_0402
PR87 63.4KF_0402
PR148 *0_0402_NC
PR149 0_0402
PR152 2K_0402
BST_3
BST_5
BST3
BST5
DH3
DH5
LX3
LX5
DL3
DL5
FB3
FB5
PRO#
ILIM5
ILIM3
REF
TON
SKIP
SHDN
8734SKIP
S5_ON
SUSON
HWPG_SYS
THERM_SYS_PWR#
QUANTA
COMPUTER
Title
SYSTEM (MAX8734)
Size
Document Number
FX2
Rev
1A
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Friday, May 05, 2006
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38
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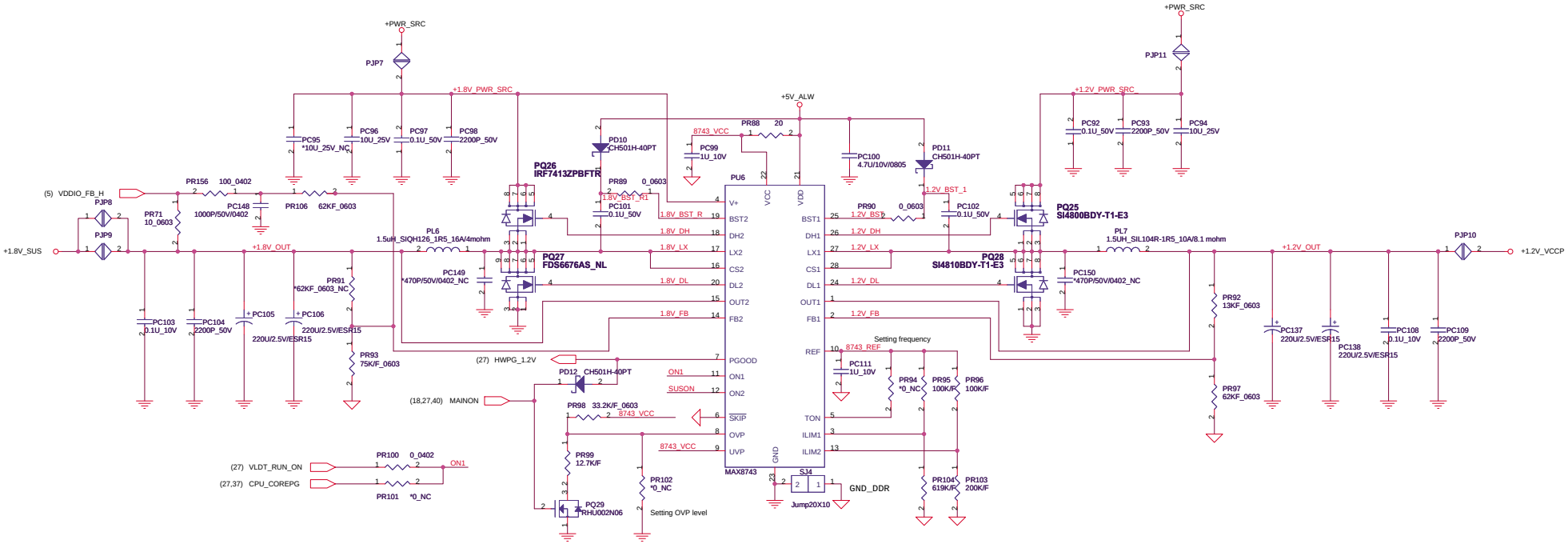
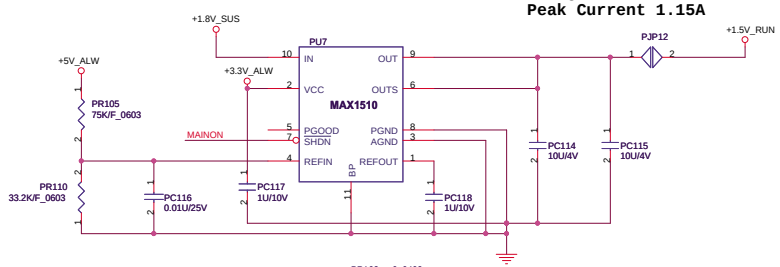
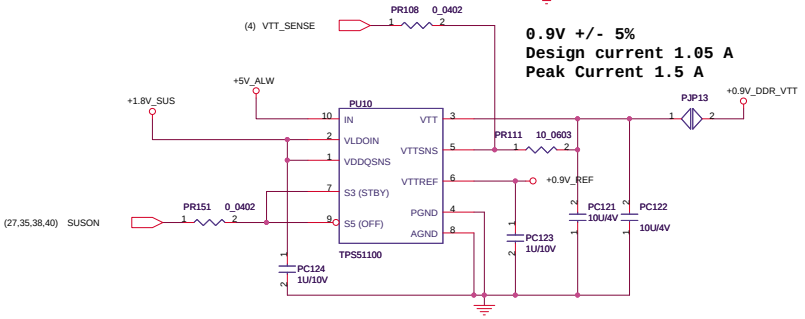
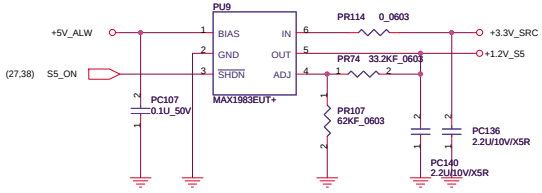


1.5 Volt +/- 5%
Design current 0.7A
Peak Current 1.15A



0.9V +/- 5%
Design current 1.05 A
Peak Current 1.5 A





QUANTA COMPUTER		
Title	VCCP	
Size	Document Number FX2	Rev 1A
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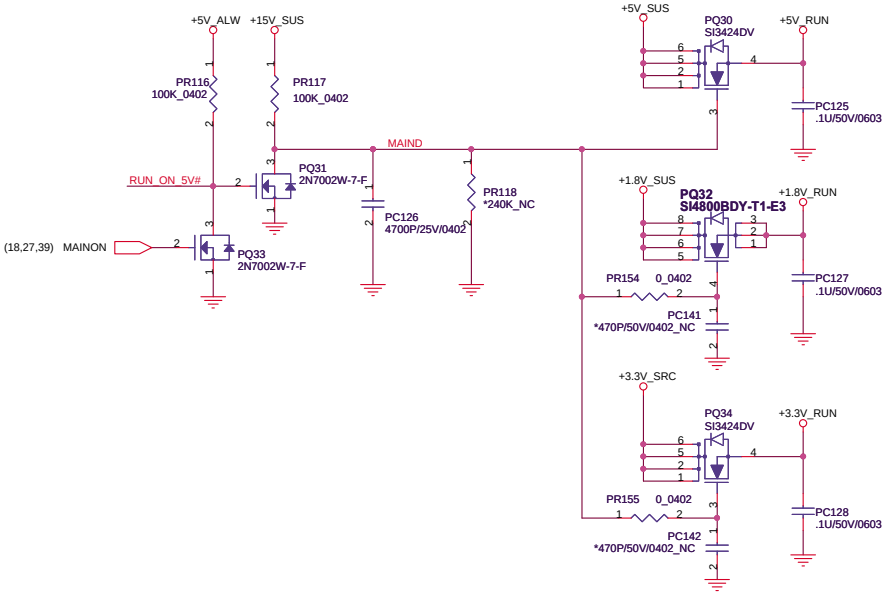
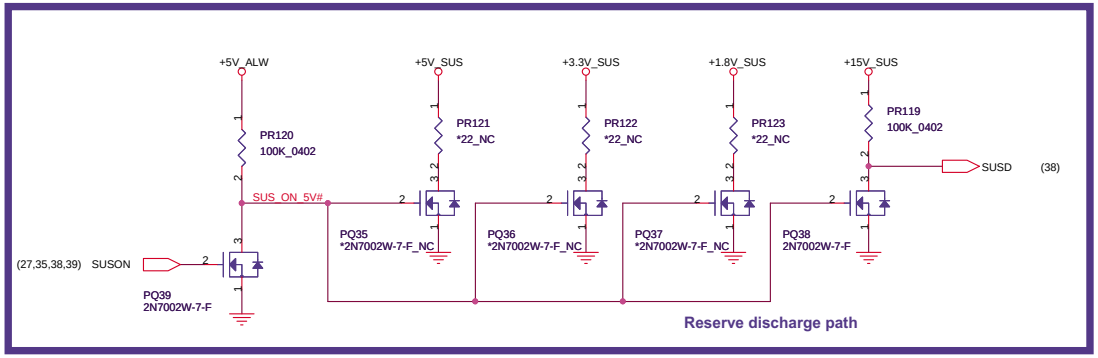
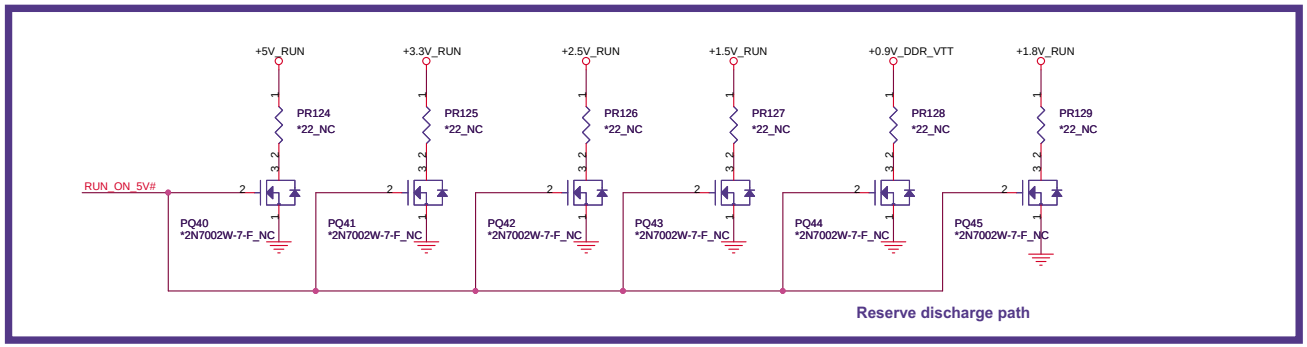
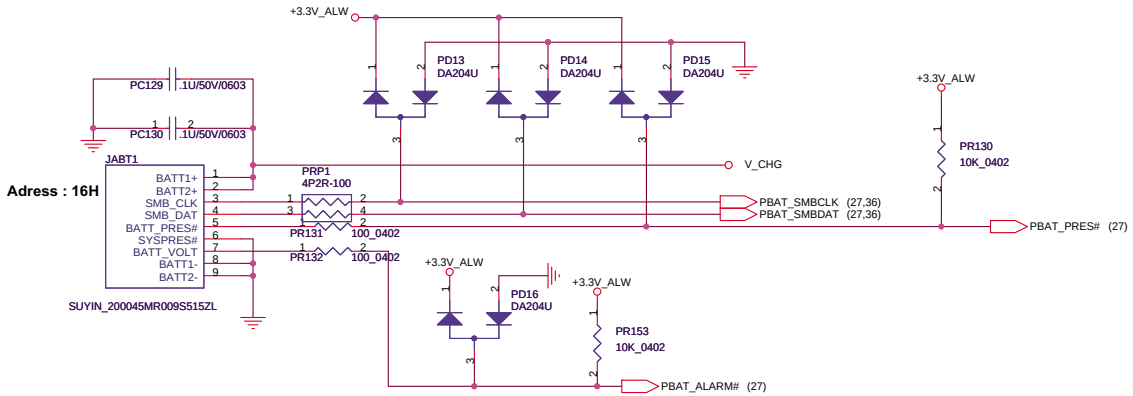


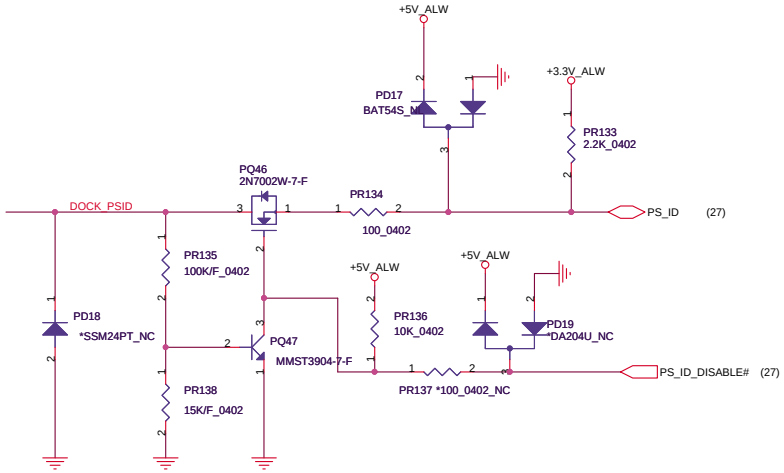


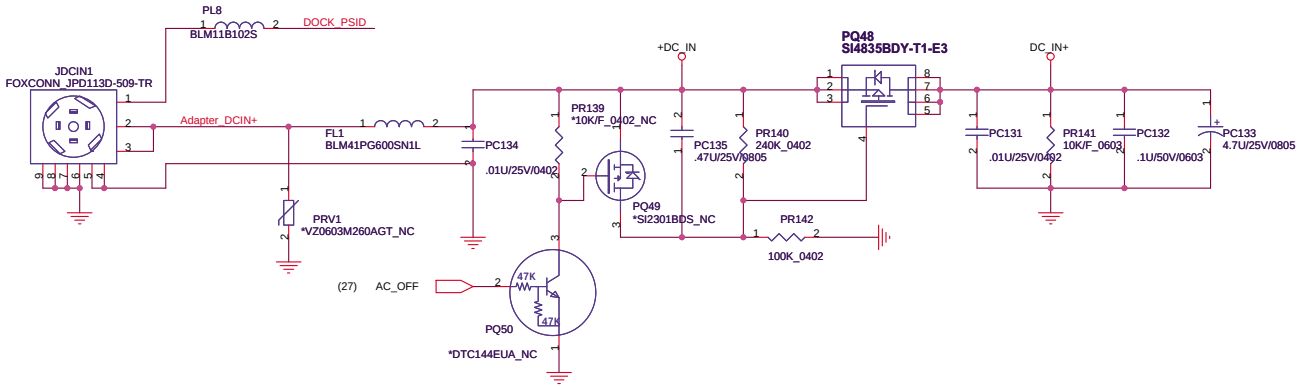


QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 40 of 47	







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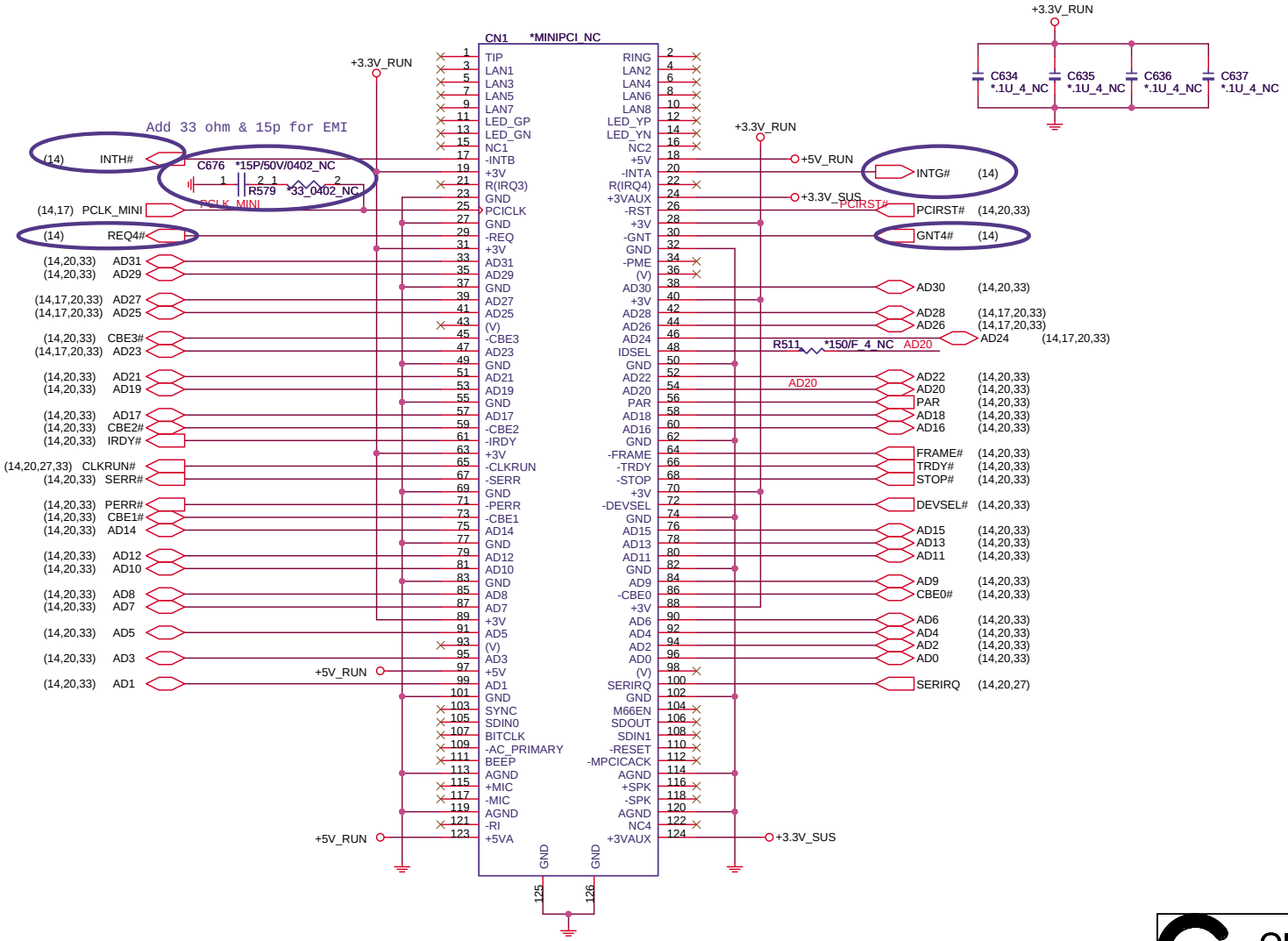
ID Select : AD20
Interrupt Pin : INTG# , INTH#
Request Indicate : REQ4#
Grant Indicate : GNT4#

DEBUG PURPOSE ONLY



MPC

QUANTA COMPUTER		
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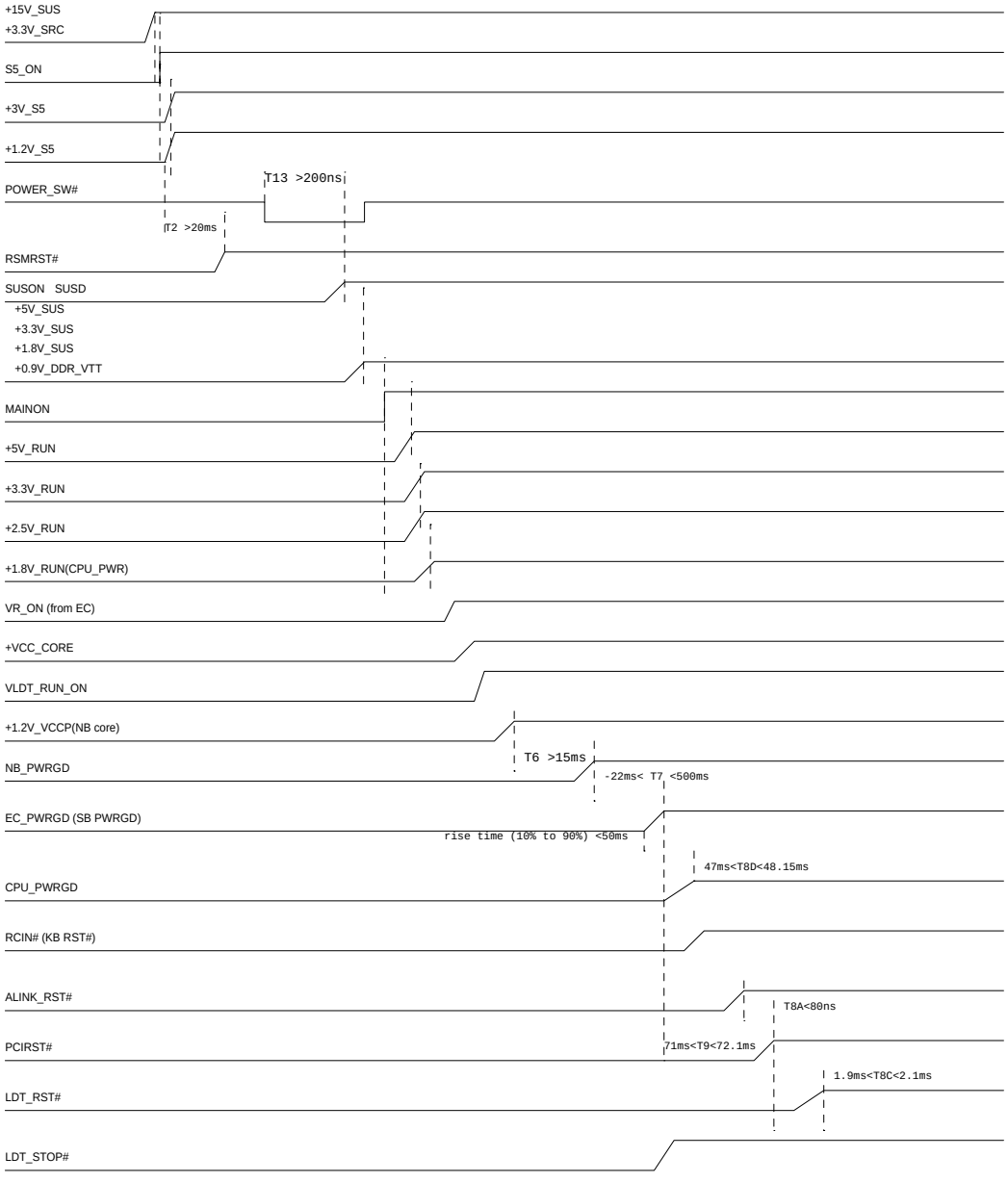
Power On Sequence



T6: NB core voltage to NB_PWRGD
T7: NB_PWRGD to SB_PWRGD
T8D: SB_PWRGD to CPU_PWRGD

T8A: ALINK_RST# to PCIRST#
T9: SB_PWRGD to PCIRST#
T8C: PCIRST# to LDT_RST#

QUANTA COMPUTER

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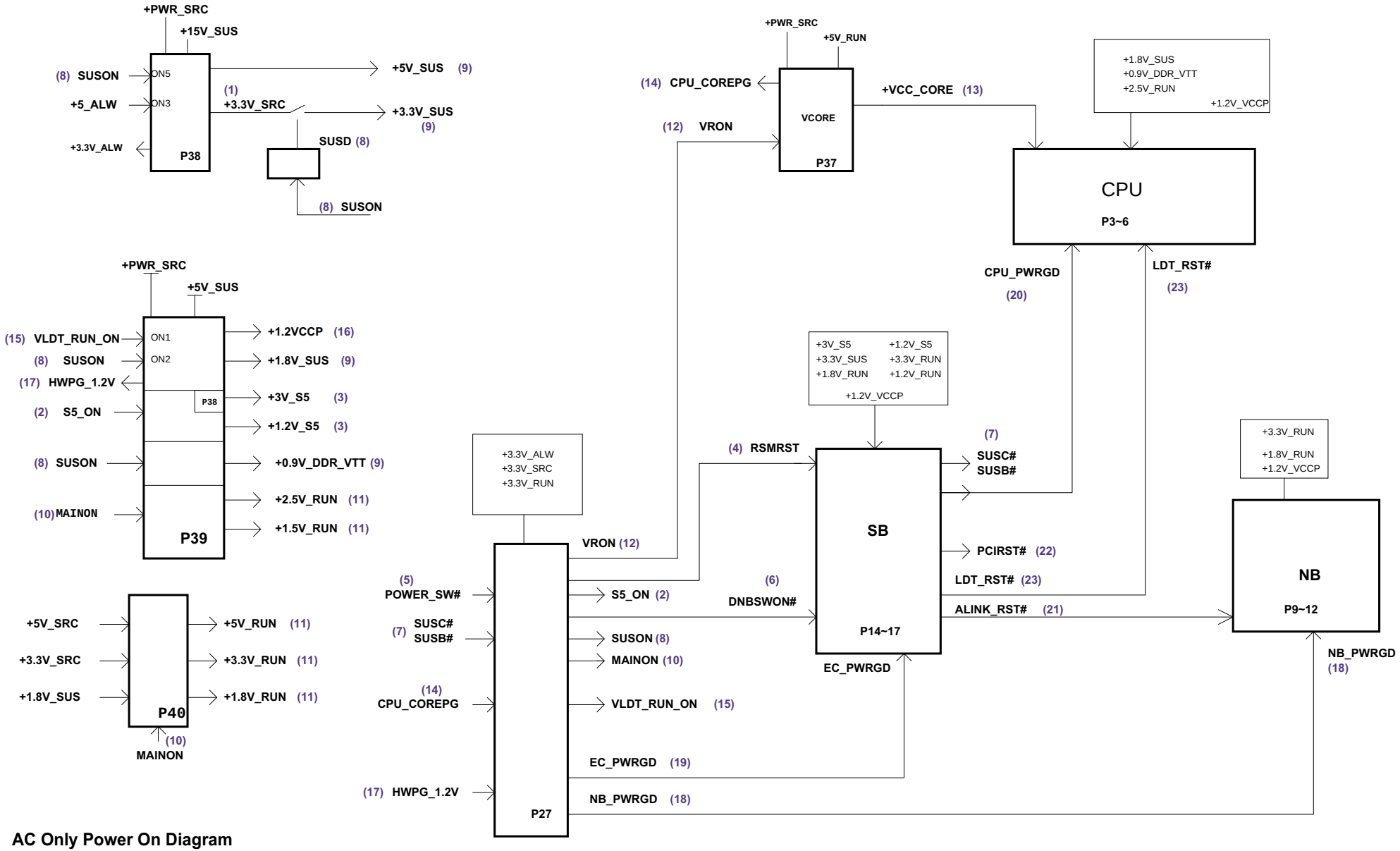

AC Only Power On Diagram

(1) +3.3V_SRC
(2) S5_ON
(3) +3V_S5, +1.2V_S5
(4) RSMRST
(5) POWER_SW#
(6) DNBSWON#
(7) SUSC#, SUSB#
(8) SUSON, SUSD
(9) +5V_SUS
+0.9V_DDR_VTT, +3.3V_SUS, +1.8V_SUS
(10) MAINON
(11) +5V_RUN, +3.3V_RUN
+2.5V_RUN, +1.8V_RUN, +1.5V_RUN
(12) VRON
(13) +VCC_CORE
(14) CPU_COREPG
(15) VLDT_RUN_ON
(16) +1.2_VCCP
(17) HWPG_1.2V
(18) NB_PWRGD
(19) EC_PWRGD
(20) CPU_PWRGD
(21) ALINK_RST#
(22) PCI_RST#
(23) LDT_RST#

QUANTA COMPUTER

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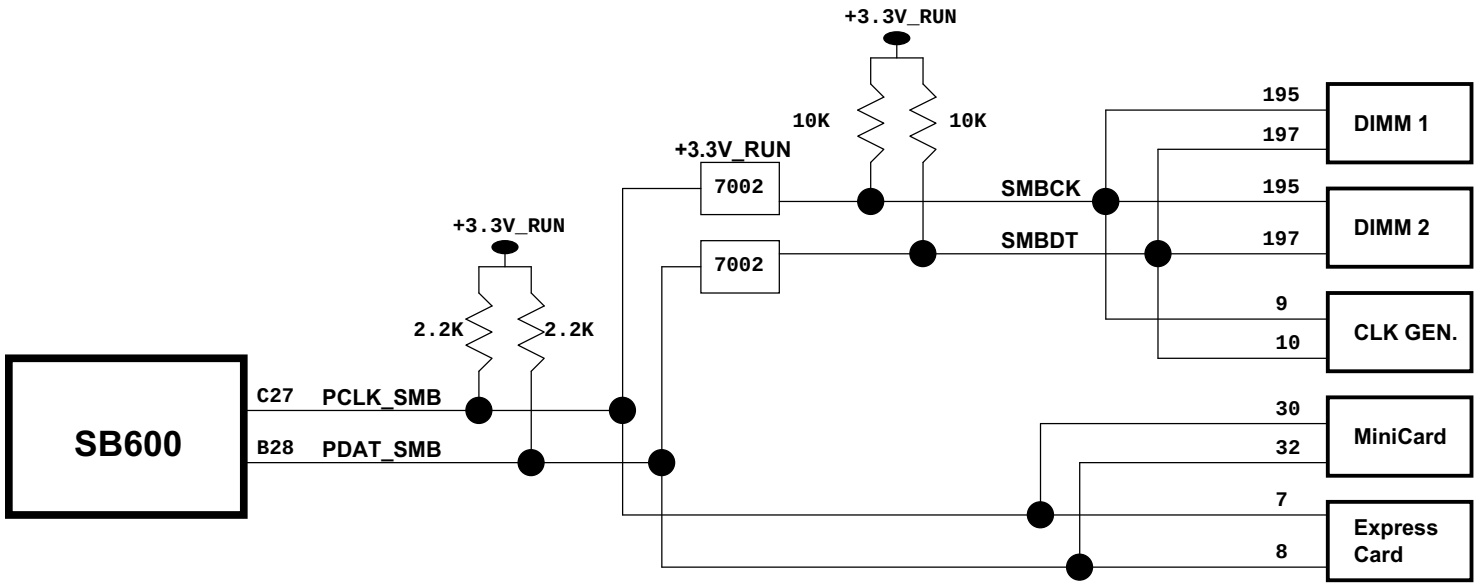

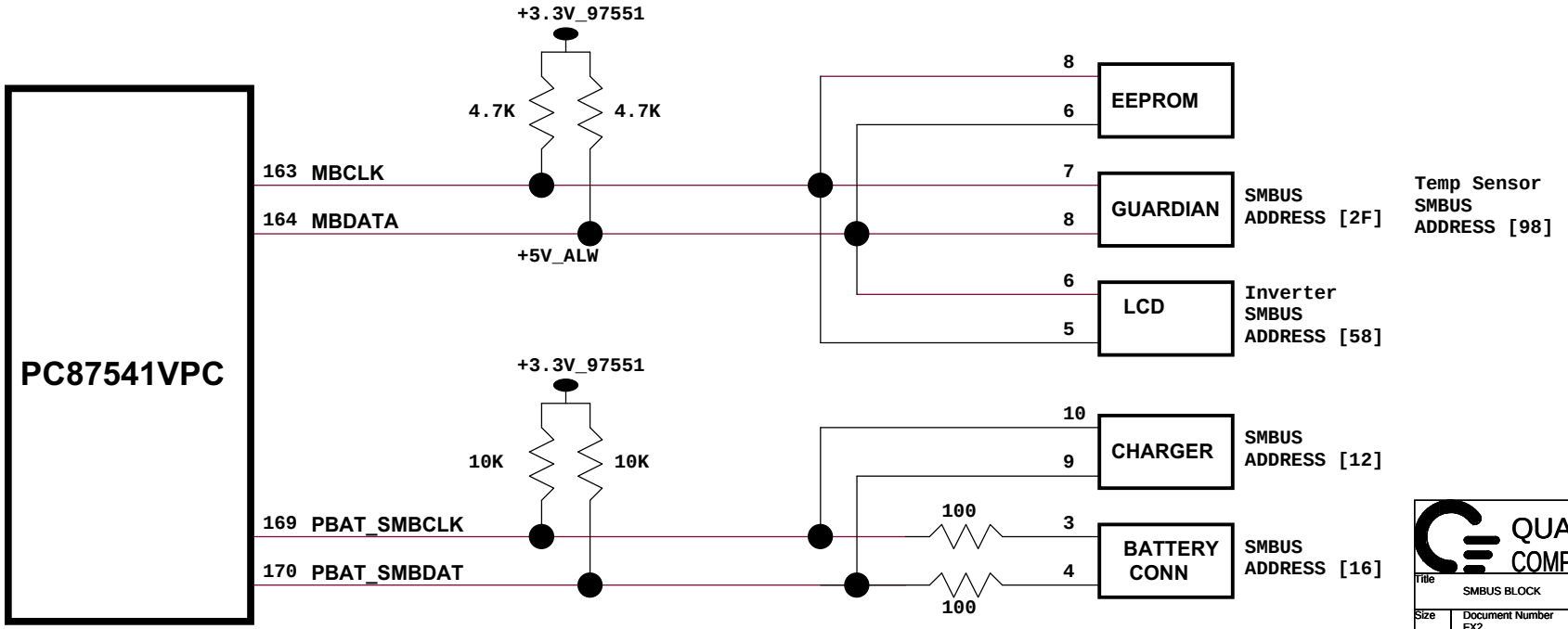

QUANTA COMPUTER

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