See 'TEXT' in 0MEMO or 1MEMO property in component

Dummy when 'USE EZ4'
Dummy when 'NO EZ4'
Dummy when use '10/100'
Dummy when use 'GIGA'
Dummy when use 'UMA'
Dummy when use 'DIS'
Dummy when use 'SATA'
Dummy when use 'IDE'
Dummy when use ''M26'
Dummy when use ''M24'

Bolsena Block Diagram

91.4C501.001 (04243)

CLK GEN
IDT CV137 3

LEDs 17
RTC BAT. 18
BUTTONs 35

AMD CPU
35W/25W
4,5,6,7

DDR 333/400

200-PIN DDR SODIMM
DDR x2
8,9,10

HyperTransport
6.4GB/S 16b/8b

SVIDEO/COMP
TVOUT 16

LVDS
LCD 17

ATI
RS480M
AGTL+ CPU I/F + UMA
11,12,13,14

PCI Express x16

ATI
M26/M24
50,51,52

RGB CRT
CRT 16

CH7301C 15

TMDS
DVI-D
(EZ4 only) 15

VRAM x4
(M26/M24 diff.) 53,54

PCI-Express
x2

Power Block Diag -> Page 40

PWR SW
TSP2220A
28

PCMCIA
SLOT
Support
TypeII 28

PCMCIA I/F

MS/xD
SM/MMC/SD
5 in 1 28

1394 4pin
Conn 28

TI
PCI 7411
1* Slot Cardbus
1* 1394
CardReader
26,27

Mini-PCI
802.11a/b/g
31

PCI Bus / 33MHz

ATI
SB400
PCI
ACPI 2.0
6xUSB 2.0
6-CH
AC97 2.2
LPC I/F
ATA 133
18,19,20,21,22

BlueTooth
miniUSB 24

USB x 4
24

CODEC
ALC655
32

AC97

Line In
MIC In 33

MODEM
MDC Card
24

RJ11
CONN 30

OP AMP
G1421
33

Line Out 33

Int. SPKR 33

RJ45
30

TXFM
30

1000Mb

TXFM
30

10/100Mb

PCI LAN
Realtek
RTL8110SBL
1000/100/10
RTL8100C
100/10
29

LPC Bus / 33MHz

NS SIO
PC87392
37

Thermal
& Fan
G792 23

KBC
KB3910
34

XBUS

Touch
Pad 35

Int.
KB 35

ISA ROM
36

FIR
37

SATA
25

PIDE

HDD
25

SIDE

DVD/
CD-RW
25

Port Replicator 4 (124 PIN)

AC IN	RJ45-11	SEARIAL PORT	CRT	PRINTER	PS2	MIC	LINE IN	LINE OUT	TV OUT	DVI	PCIeX2	SMBUS

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	Bolsena	-1

Date: Tuesday, April 12, 2005 Sheet 1 of 58

PCI Routing

	IDSEL	IRQ	REQ/GNT
MiniPCI	21	F	0
LAN	23	H	2
7411	22	E (CardBus)	1
7411	22	G (1394)	1
7411	22	E (FlashMedia)	1

Ref.	function	schematic	BOM
U81	cpu socket	62.10055.091 (DON'T CHANGE) (3mm high)	
U80	north bridge	71.RS48M.00U	71.RS48M.B0U (ver A22)
U43	south bridge	71.SB400.B0U	71.SB400.D0U (ver A32)
U32	clock gen.	71.00137.A0W	71.00137.B0W

U70	VGA M24	71.0M26P.00U	71.00M24.C0U
U64	VRAM FOR M24	72.55732.B0U	72.52832.E05
U65	VRAM FOR M24	72.55732.B0U	72.52832.E05
U69	VRAM FOR M24	72.55732.B0U	72.52832.E05
U71	VRAM FOR M24	72.55732.B0U	72.52832.E05

U70	VGA M26	71.0M26P.00U (DON'T CHANGE)	
U64	VRAM FOR M26	72.55732.B0U (DON'T CHANGE)	
U65	VRAM FOR M26	72.55732.B0U (DON'T CHANGE)	
U69	VRAM FOR M26	72.55732.B0U (DON'T CHANGE)	
U71	VRAM FOR M26	72.55732.B0U (DON'T CHANGE)	

U66	BIOS SOCKET	72.39040.G03	62.10002.032 (NO NEED WHEN PD)
U66	BIOS IC	72.39040.G03	72.39040.H03 (DIP STAGE IN LAB, SMT IN PD)

LOUT1	AUDIO	22.10257.001	22.10147.031 (NO SPDIF)

U75	GIGA LAN	71.08110.00G	71.08110.A0G
U75	10/100 LAN	71.08110.00G	71.08100.C0G

HDD1		20.80175.044	20.80592.044
SATA1		20.F0614.022	20.F0665.022
EZ4		20.80579.120	20.80591.120 (AFTER SB)

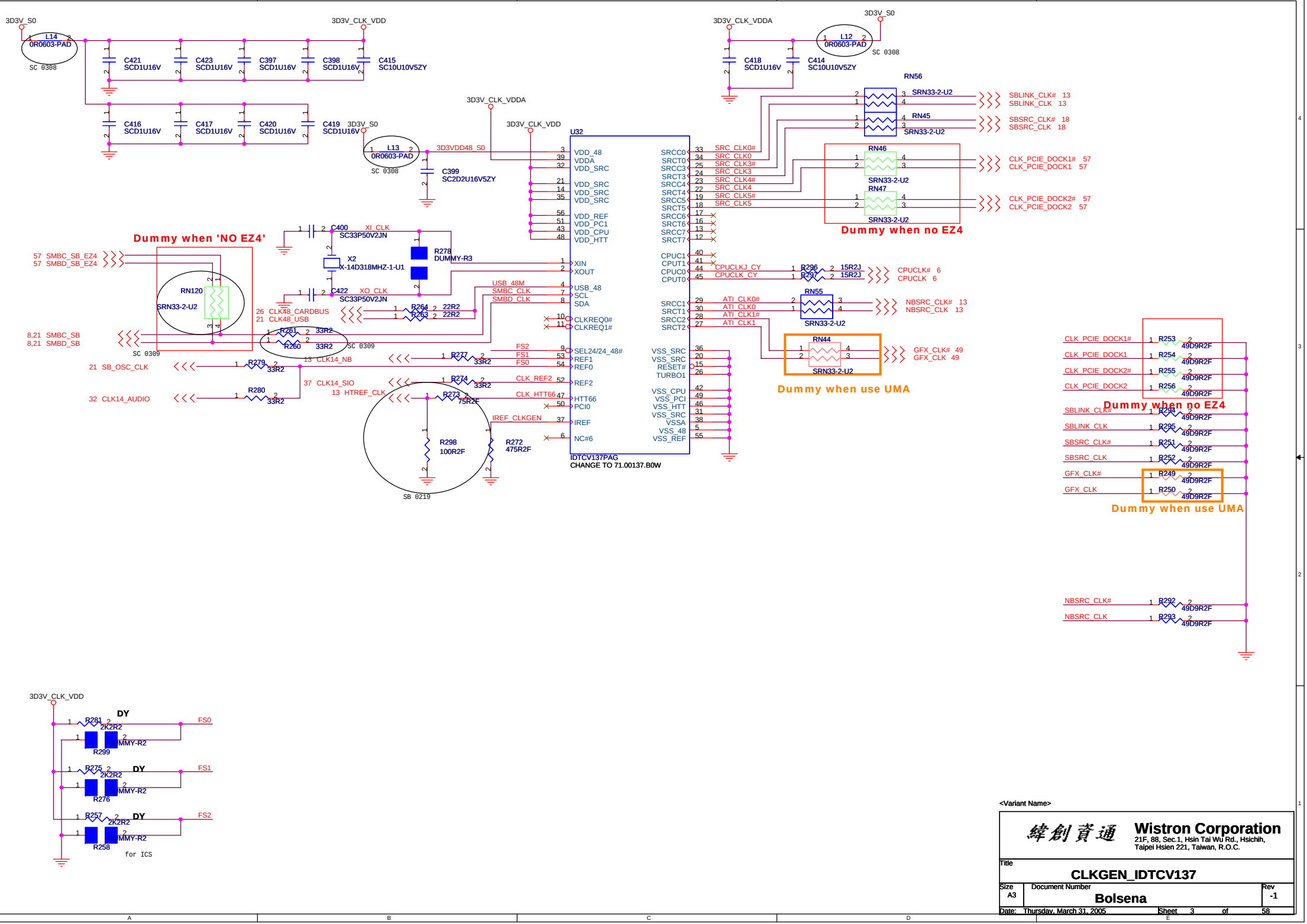
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHANGE HISTORY

Size: A3 | Document Number: Boisena | Rev: -1

Date: Thursday, March 31, 2005 | Sheet 2 of 58



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

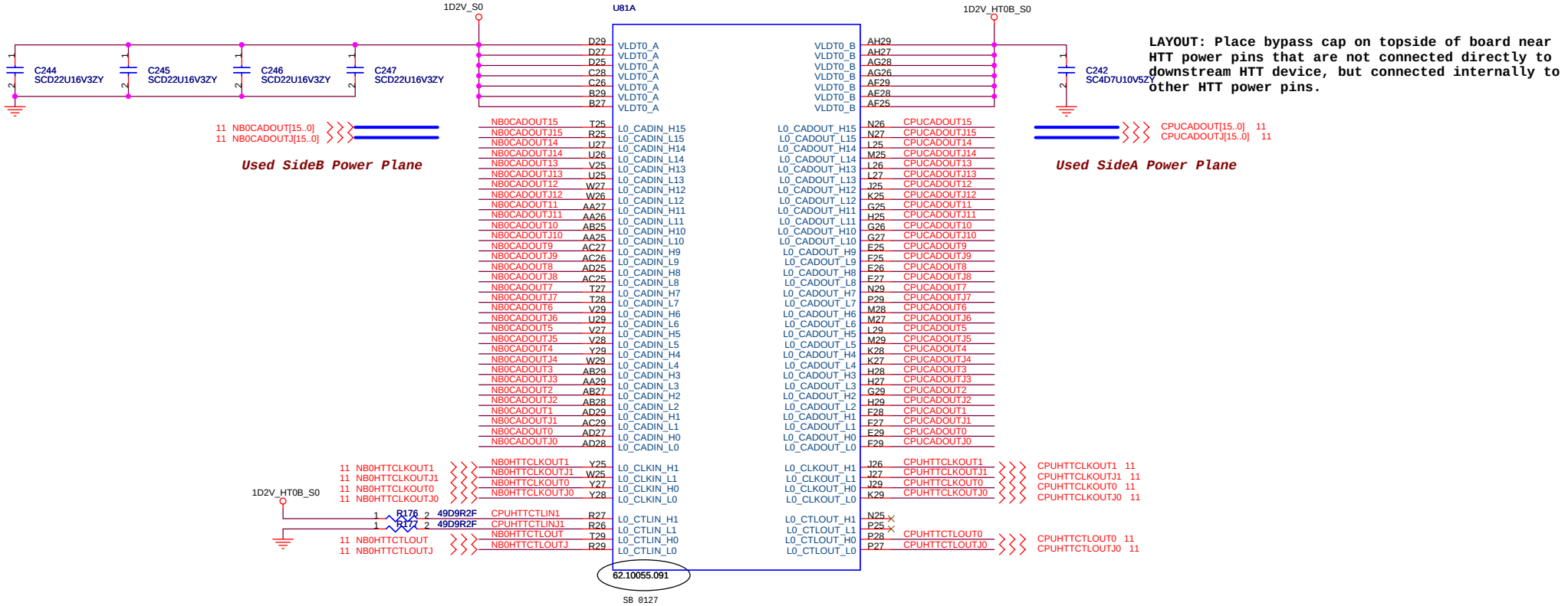
Title: CLKGEN_IDTCV137

Size	Document Number	Rev
A3	Bolsena	-1

Date: Thursday, March 31, 2005 Sheet 3 of 58

HTT for CPU sideA Transmit power and NB sideA Receive power

HTT for CPU sideB Receive power and NB sideA Transmit power



LAYOUT: Place bypass cap on topside of board near HTT power pins that are not connected directly to downstream HTT device, but connected internally to other HTT power pins.

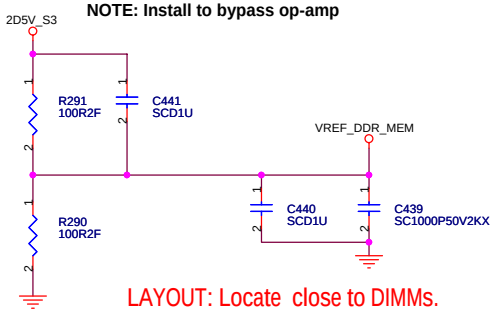
ME : 60.10055.091
(3MM HEIGHT)

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**CPU(1/4)_HyperTransport I/F**
Size: A3	Document Number: **Bolsena**
Rev: -1	
Date: Thursday, March 31, 2005	Sheet 4 of 58

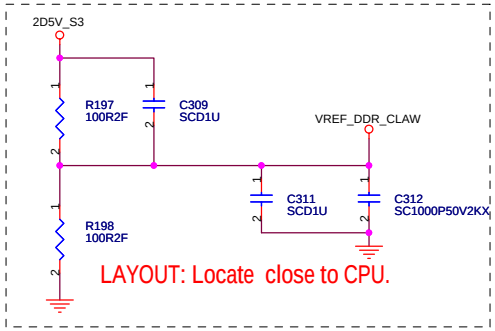
VREF_DDR_MEM

NOTE: Test with passive probes only.
NOTE: Install to bypass op-amp

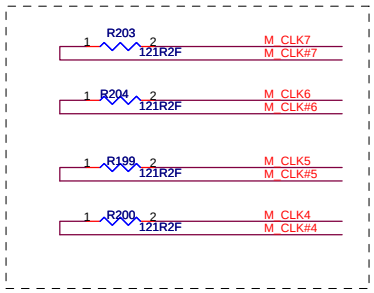


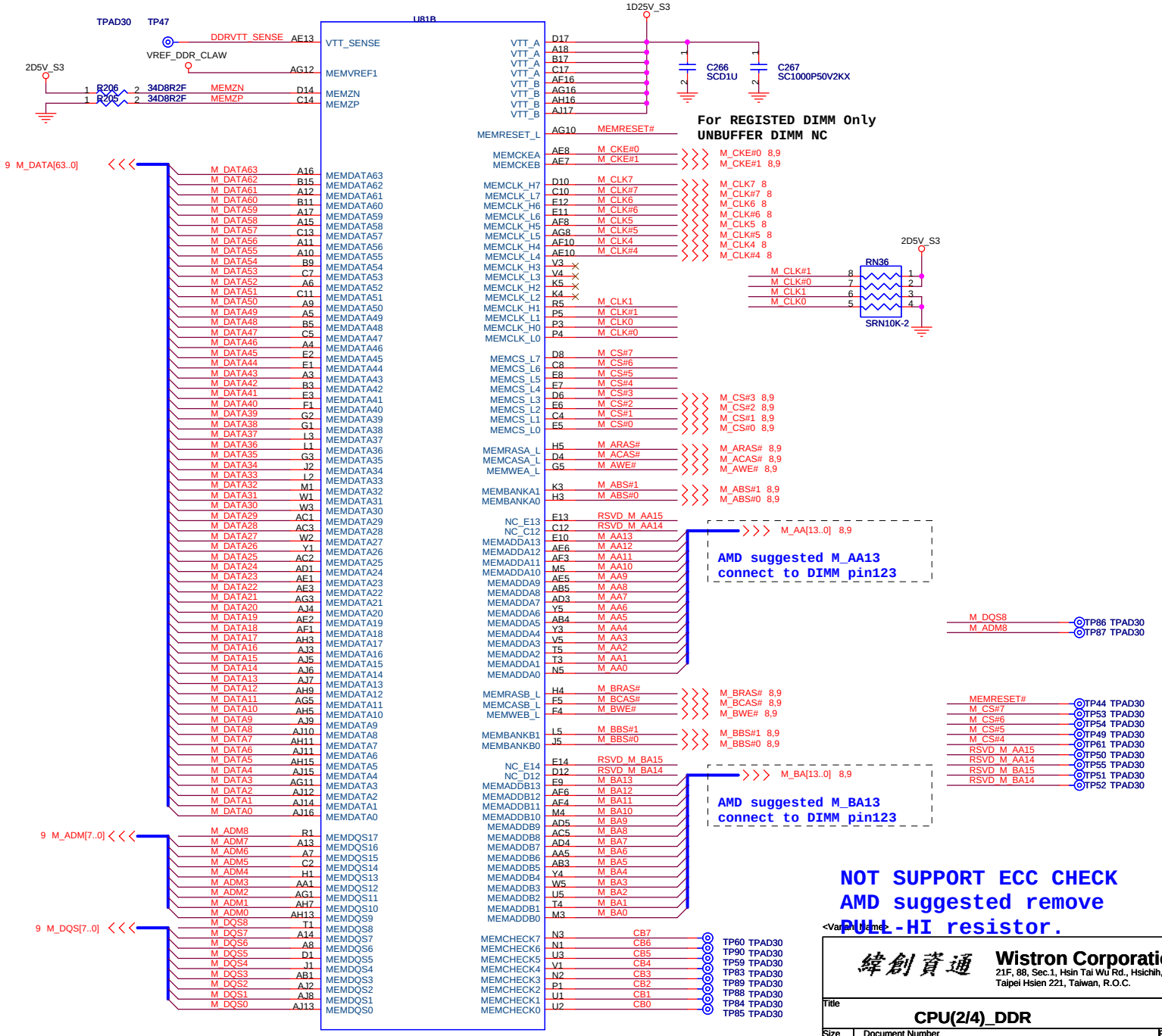
NOTE: Remove to bypass op-amp

VREF_DDR_CLAW



Place it near CPU





NOT SUPPORT ECC CHECK
AMD suggested remove
PULL-HI resistor.

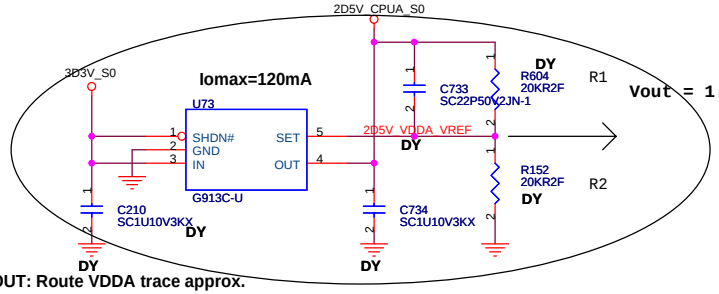
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(2/4)_DDR

Size	Document Number	Rev
A3	Bolsena	-1

Date: Thursday, March 31, 2005 Sheet 5 of 58

2D5V_VDDA_S0



AMD SUGGEST TO USE 100 ~ 300UH

LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.

LAYOUT: Route VDDA trace approx. 50 mils wide (use 2x25 mil traces to exit ball field) and 500 mils long.

AMD SUGGEST TO USE 2D5V_CPUA_S0

KEMET,NT:5.7, B2 size
ST100U4VBM-1 (80.10716.321)
Iripple=1.1A,ESR=70mohm

SANYO, NT$:6.1
Iripple=1.1A,ESR=70mohm
3.5/2.8/2.0
77.21071.031

AMD suggest voltege from 2D5V_S0 to 2D5V_S3 differentially impedance 100

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

Connect to VDDIO for AMD suggest.

THERMTRIP#Level shift to SB400

CHANGE FROM 1KR3 TO 680R2 FOR AMD CHECK LIST

Validation Test Points

LAYOUT: Place close to the CPU.

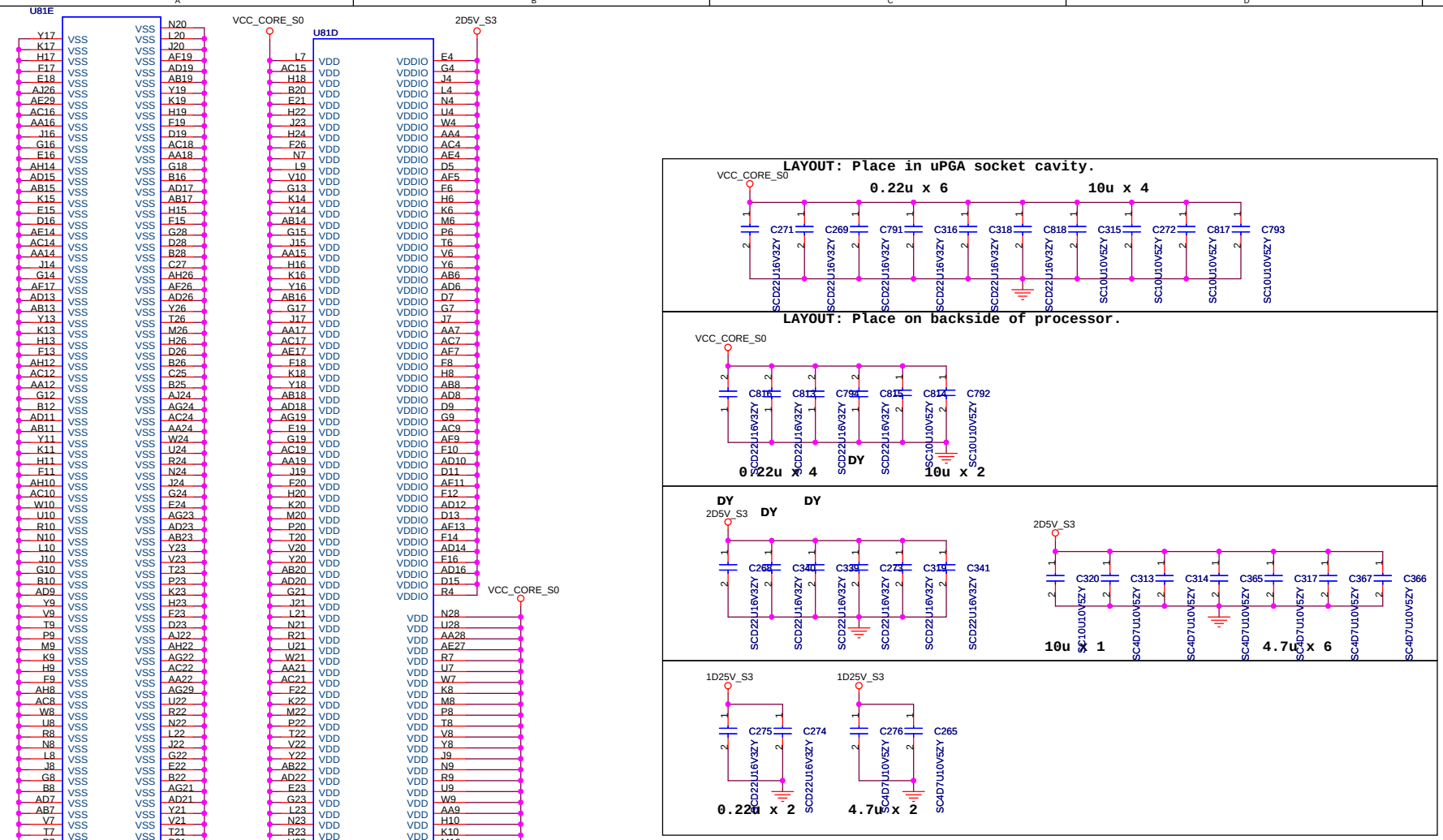
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: CPU(3/4)_Control & Debug

Size: A3 | Document Number: Bolsena | Rev: -1

Date: Thursday, March 31, 2005 | Sheet 6 of 58



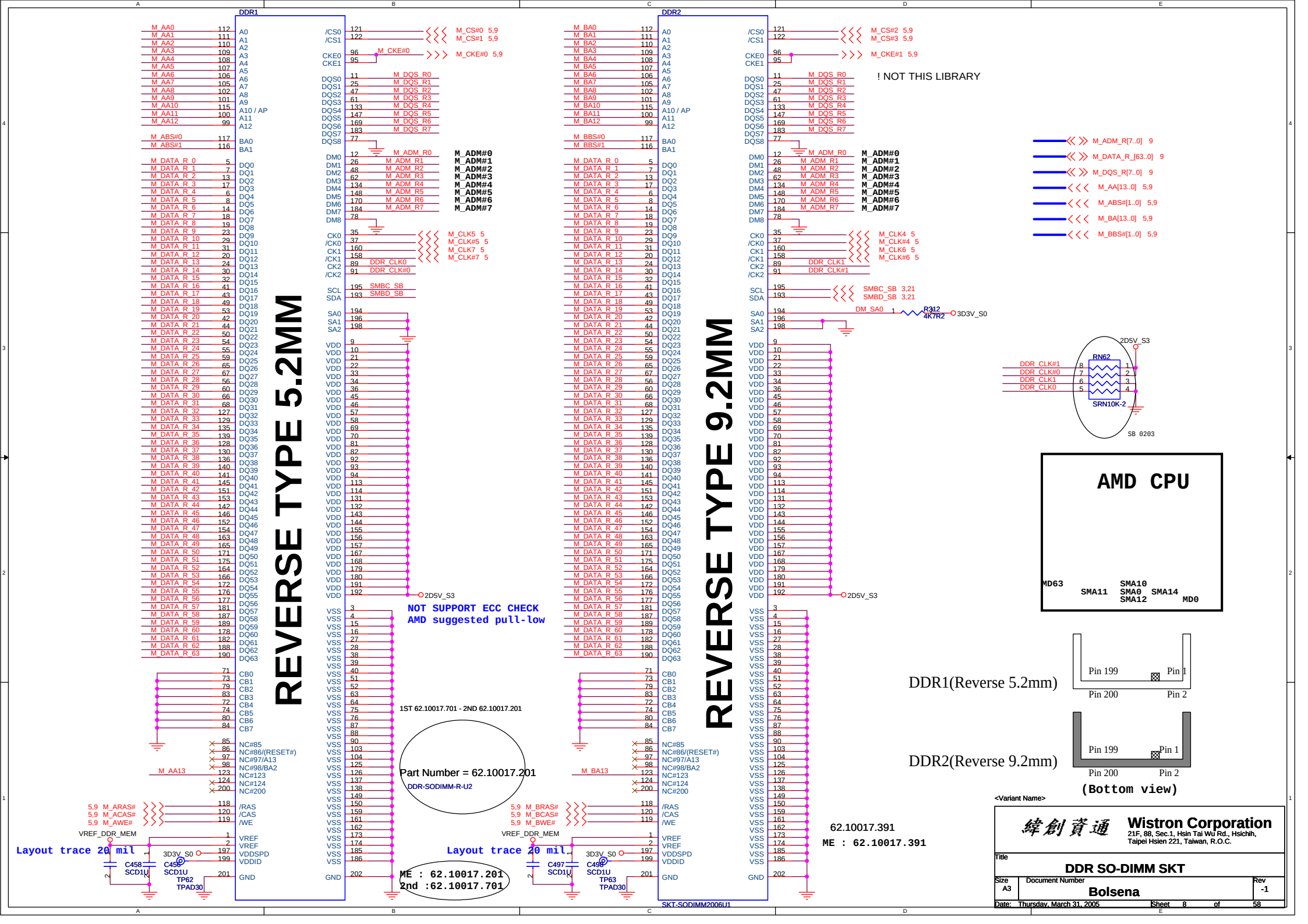
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(4/4)_Power**

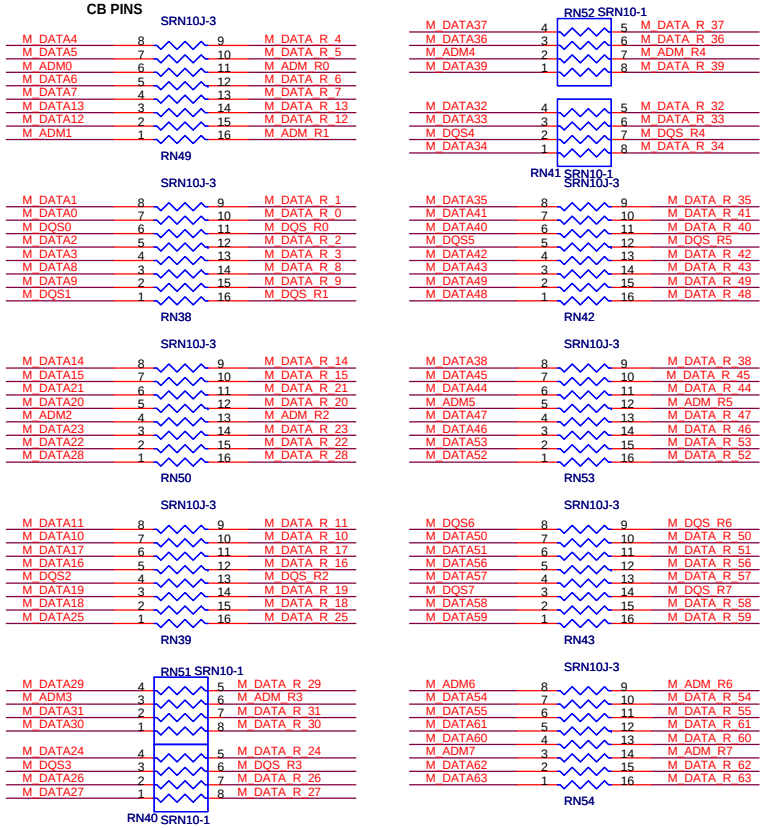
Size	Document Number	Rev
A3	**Bolsena**	-1

Date: Thursday, March 31, 2005 Sheet 7 of 58


DDR1
REVERSE TYPE 5.2MM
DDR2
REVERSE TYPE 9.2MM
! NOT THIS LIBRARY
NOT SUPPORT ECC CHECK
AMD suggested pull-low
1ST 62.10017.701 - 2ND 62.10017.201
Part Number = 62.10017.201
DDR-SODIMM-R-U2
ME : 62.10017.201
2nd :62.10017.701
62.10017.391
ME : 62.10017.391
Layout trace 20 mil
Layout trace 20 mil
SKT-SODIMM2006U1
AMD CPU
MD63
SMA11
SMA10
SMA0
SMA14
SMA12
MD0
DDR1(Reverse 5.2mm)
DDR2(Reverse 9.2mm)
Pin 199
Pin 1
Pin 200
Pin 2
(Bottom view)
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR SO-DIMM SKT
Size
A3
Document Number
Bolsena
Rev
-1
Date: Thursday, March 31, 2005
Sheet 8 of 58

SERIES DAMPING

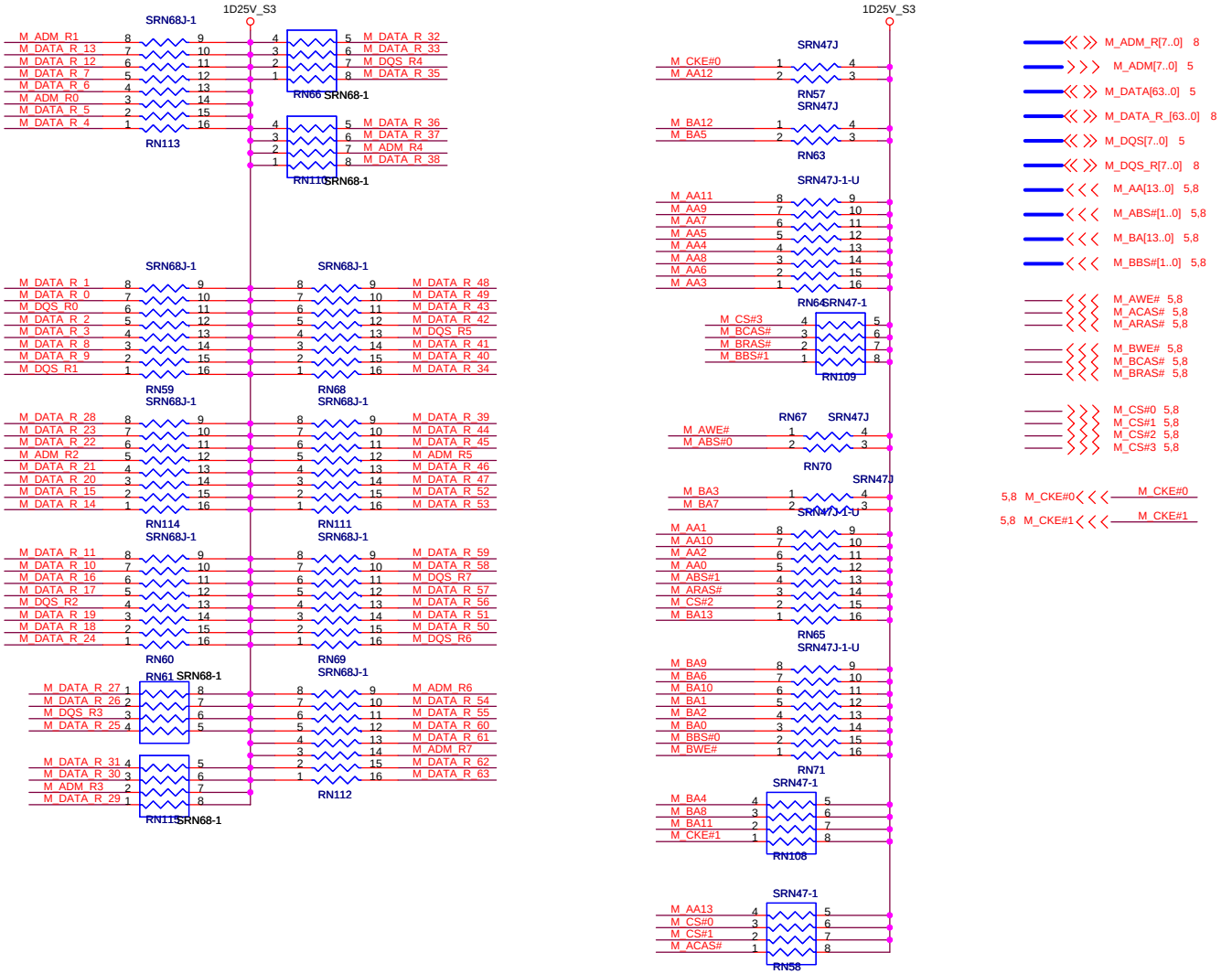
PLACE RNs CLOSE TO FIRST DIMM, < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS,
CB PINS



05/10
Remove the damping resistor for AMD suggest.

PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM2)
NO EQUAL LENGTH LIMITATION



<Variant Name>

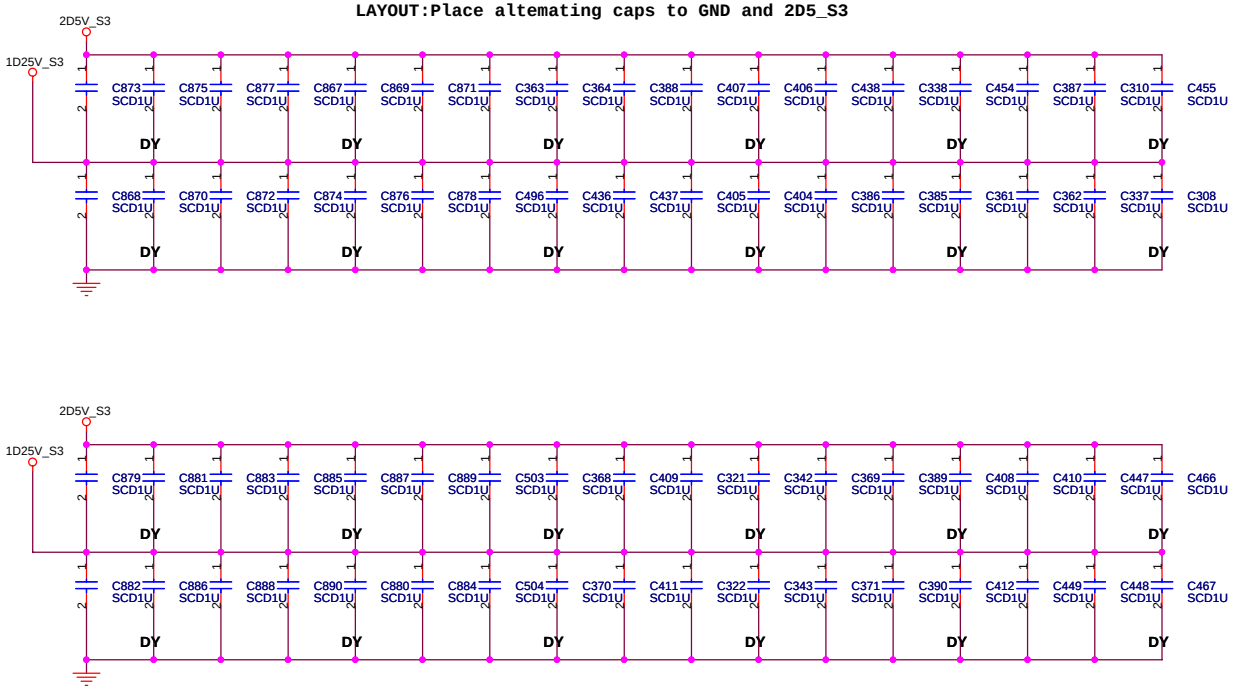
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

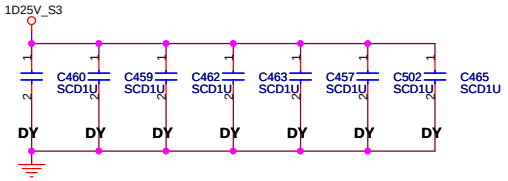
Title: **DDR DAMPING & TERMINATION**

Size	Document Number	Rev
A3	Bolsena	-1

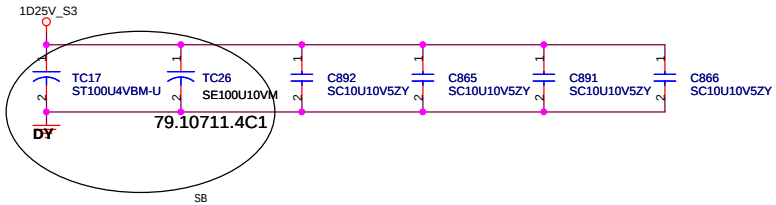
Date: Thursday, March 31, 2005 Sheet 9 of 58

LAYOUT:Place altemating caps to GND and 2D5_S3

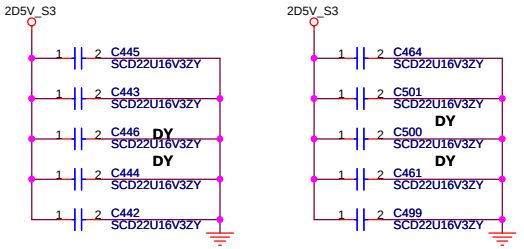




LAYOUT:Place at end of the DIMMs



LAYOUT:Place close to Power Pin of DDR socket.



0.22u x 10

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

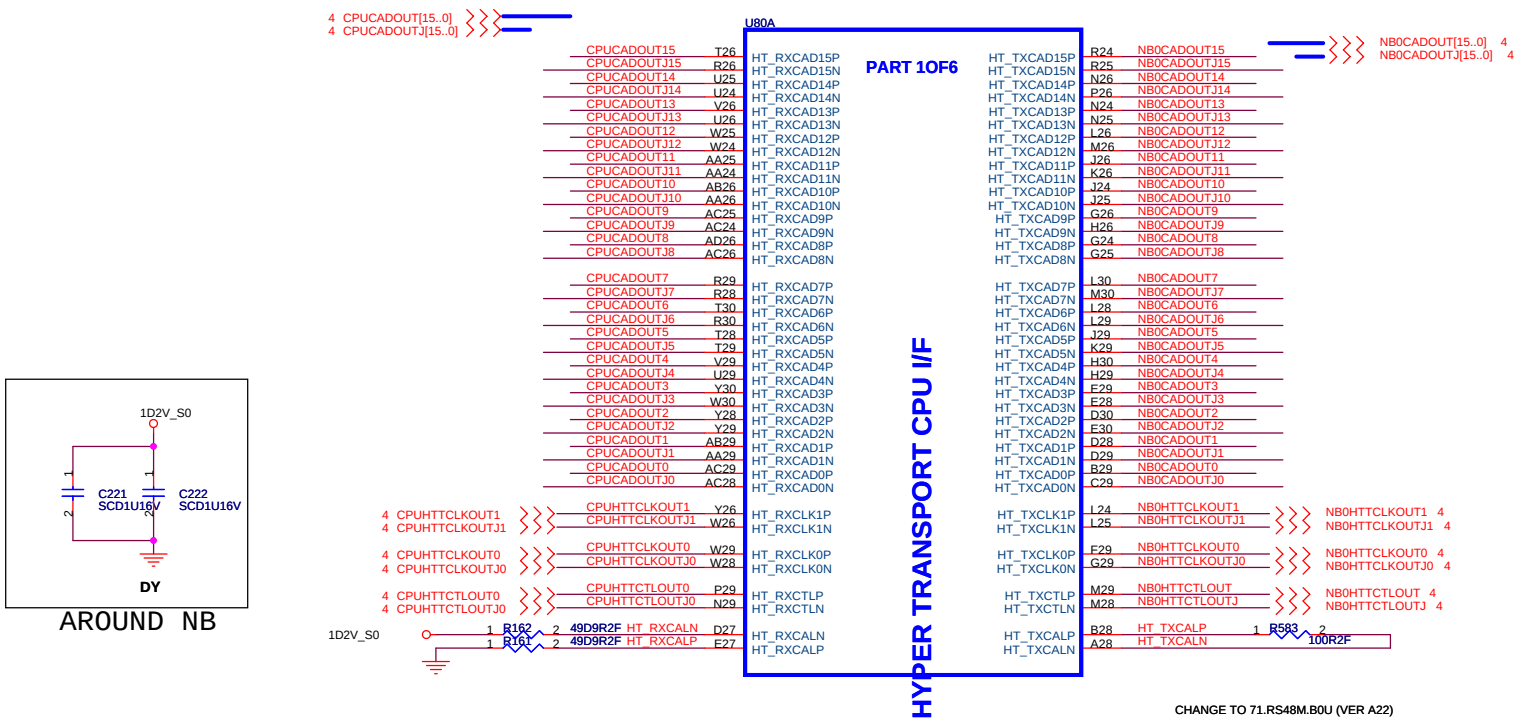
Title: DDR DECOUPLING

Size	Document Number	Rev
A3	Bolsena	-1

Date: Thursday, March 31, 2005 Sheet 10 of 58

CLAW HAMMER TO NB

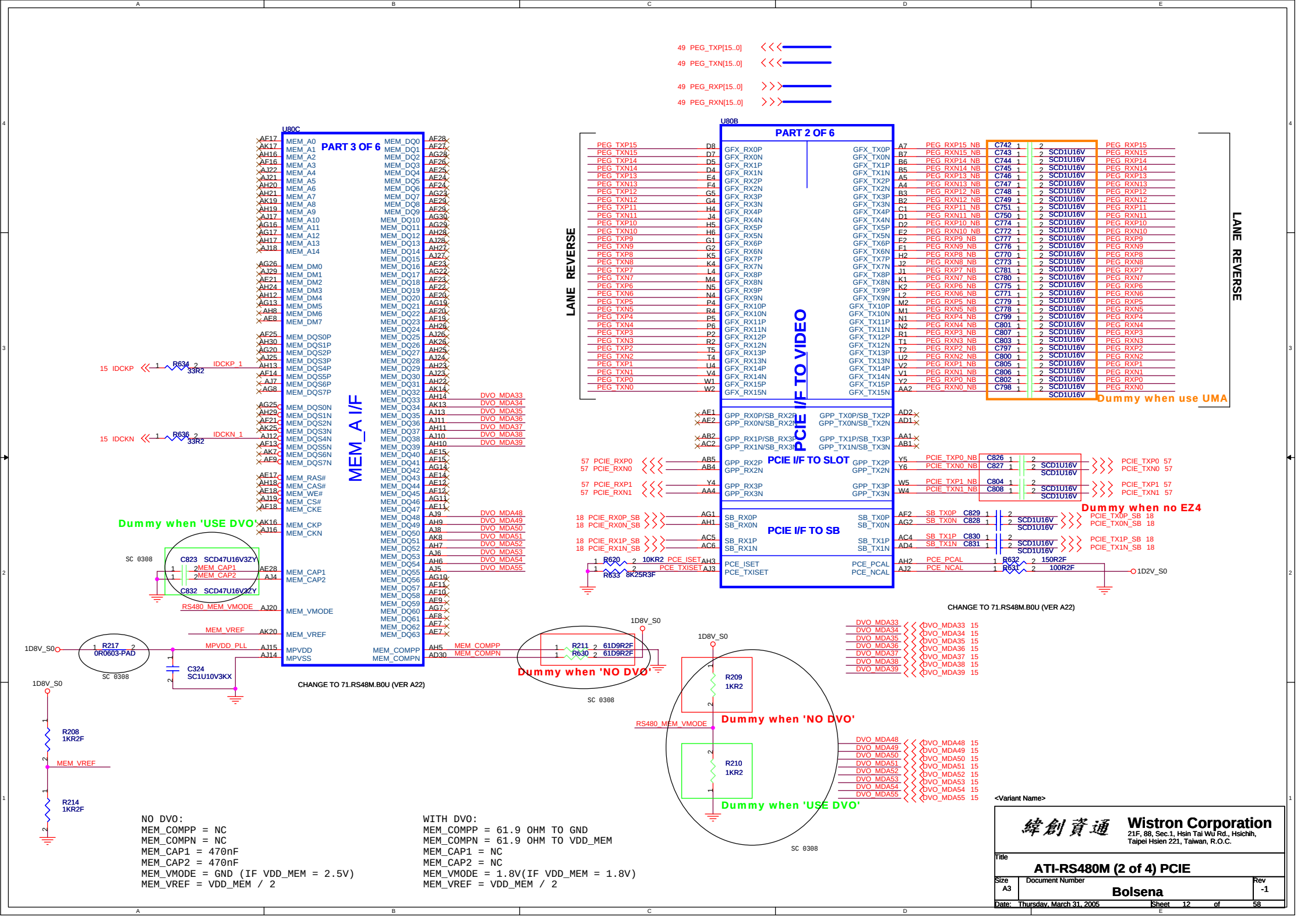
NB TO CLAW HAMMER

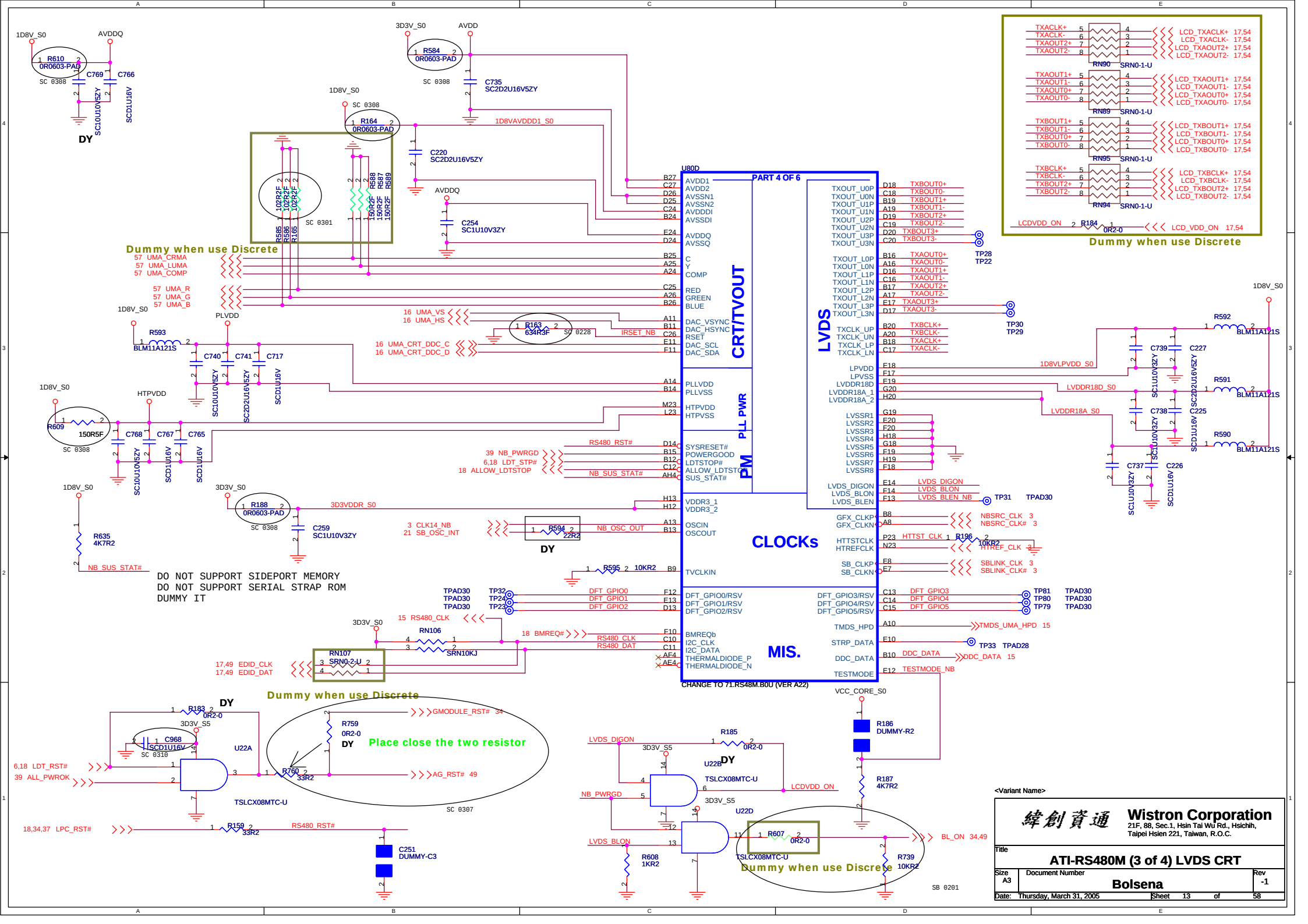


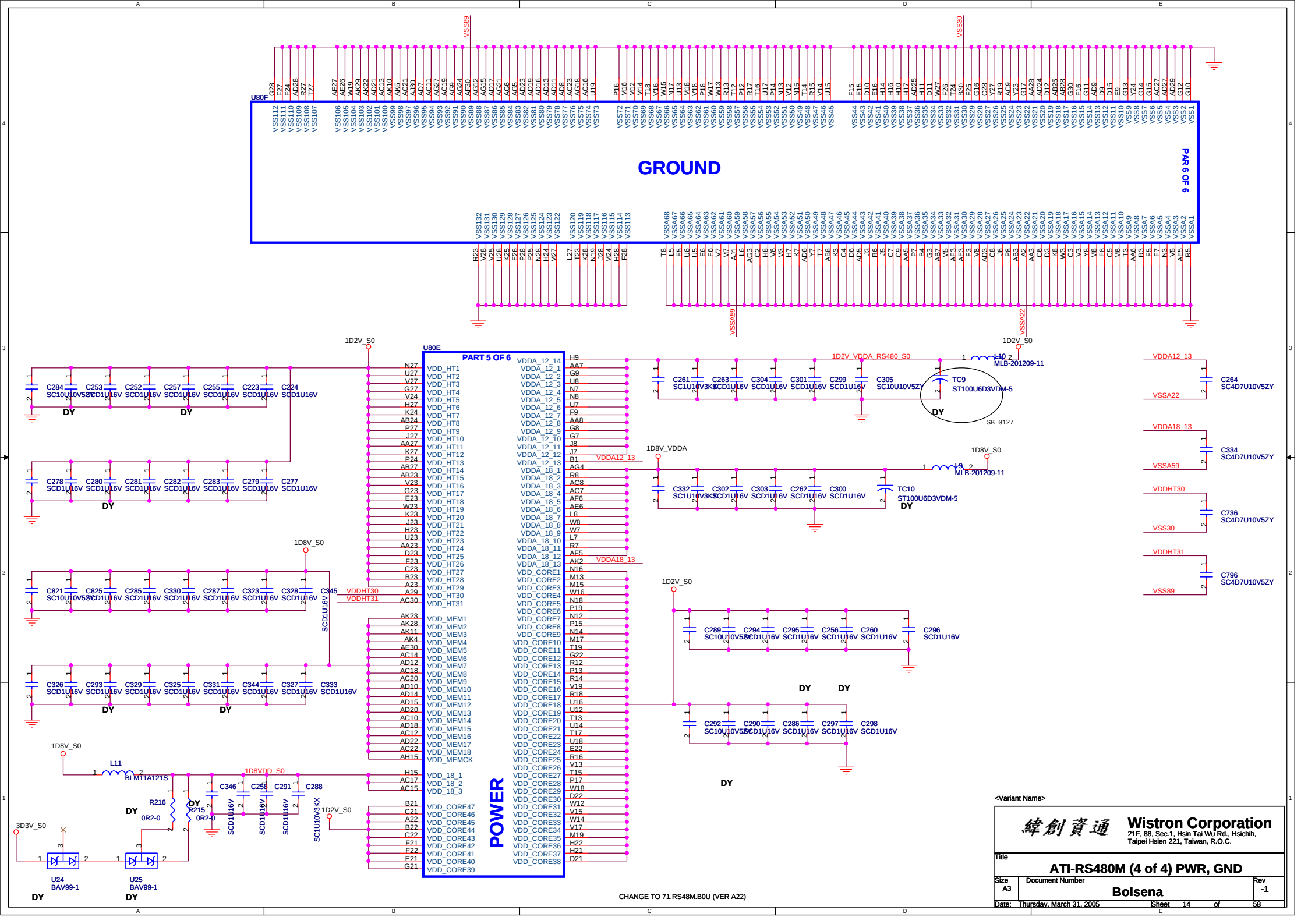
AROUND NB

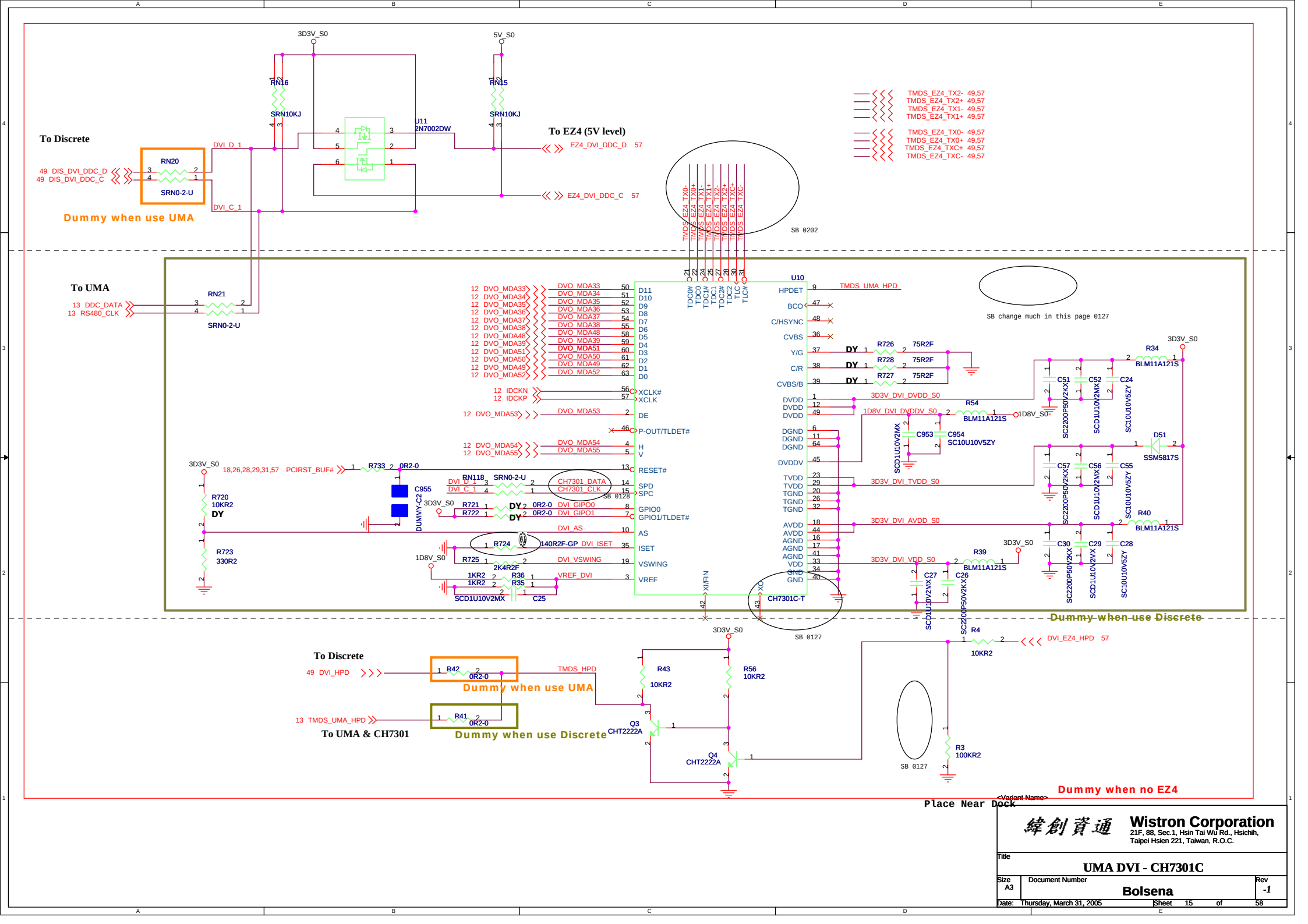
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**ATI-RS480M (1 of 4) HT**
Size: A3	Document Number: **Bolsena**
Rev: -1	
Date: Thursday, March 31, 2005	Sheet 11 of 58


49 PEG_TXP[15..0]
49 PEG_TXN[15..0]
49 PEG_RXP[15..0]
49 PEG_RXN[15..0]
U80C
PART 3 OF 6
MEM_A I/F
CHANGE TO 71.RS48M.B0U (VER A22)
U80B
PART 2 OF 6
PCIE I/F TO VIDEO
PCIE I/F TO SLOT
PCIE I/F TO SB
LANE REVERSE
Dummy when use UMA
Dummy when no EZ4
CHANGE TO 71.RS48M.B0U (VER A22)
Dummy when 'USE DVO'
Dummy when 'NO DVO'
Dummy when 'NO DVO'
Dummy when 'USE DVO'
NO DVO:
MEM_COMPP = NC
MEM_COMPN = NC
MEM_CAP1 = 470nF
MEM_CAP2 = 470nF
MEM_VMODE = GND (IF VDD_MEM = 2.5V)
MEM_VREF = VDD_MEM / 2
WITH DVO:
MEM_COMPP = 61.9 OHM TO GND
MEM_COMPN = 61.9 OHM TO VDD_MEM
MEM_CAP1 = NC
MEM_CAP2 = NC
MEM_VMODE = 1.8V(IF VDD_MEM = 1.8V)
MEM_VREF = VDD_MEM / 2
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI-RS480M (2 of 4) PCIE
Size A3
Document Number
Bolsena
Rev -1
Date: Thursday, March 31, 2005
Sheet 12 of 58

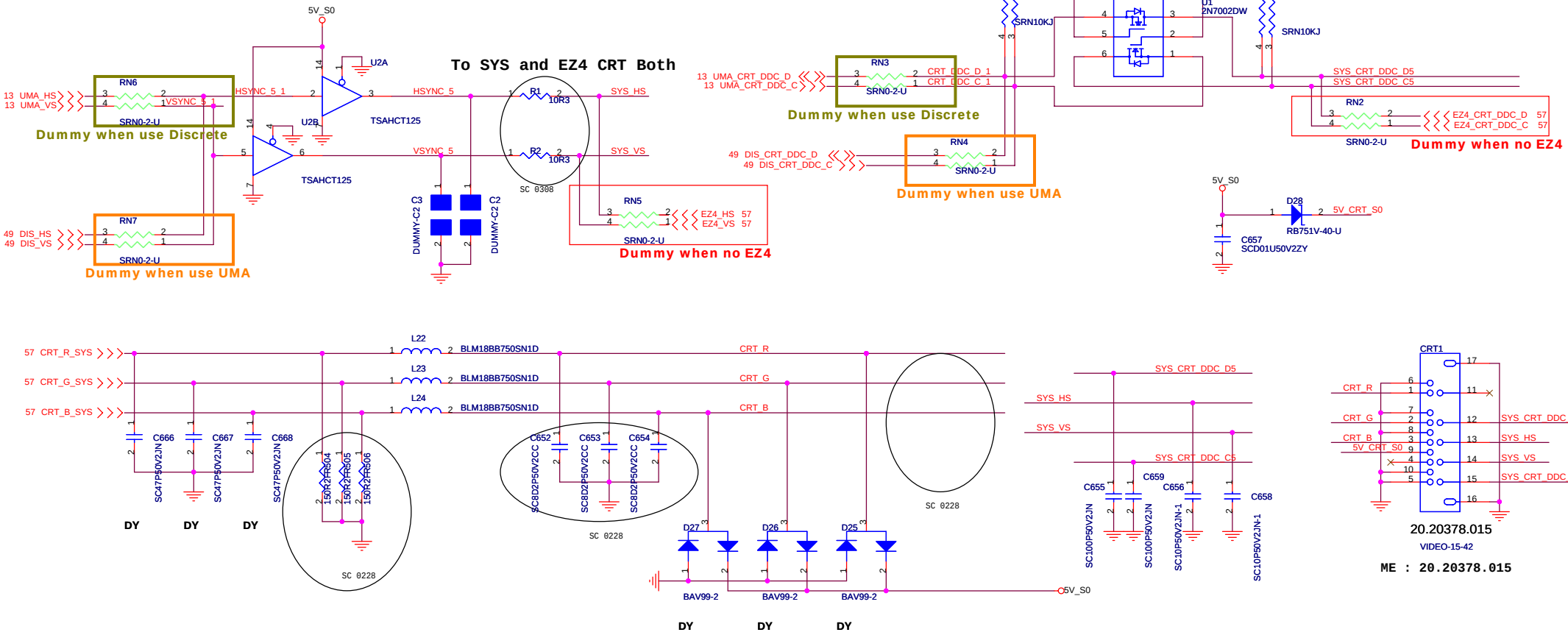

U80D
PART 4 OF 6
CRT/TVOUT
LVDS
PLL PWR
PM
CLOCKs
MIS.
AVDD1
AVDD2
AVSSN1
AVSSN2
AVDDDI
AVSSDI
AVDDQ
AVSSQ
C
Y
COMP
RED
GREEN
BLUE
DAC_VSYNC
DAC_HSYNC
RSET
DAC_SCL
DAC_SDA
PLLVDD
PLLVSS
HTPVDD
HTPVSS
SYSRESET#
POWERGOOD
LDTSTOP#
ALLOW_LDTSTOP
SUS_STAT#
VDDR3_1
VDDR3_2
OSCIN
OSCOUT
TVCLKIN
DFT_GPIO0/RSV
DFT_GPIO1/RSV
DFT_GPIO2/RSV
BMREQb
I2C_CLK
I2C_DATA
THERMALDIODE_P
THERMALDIODE_N
TXOUT_U0P
TXOUT_U0N
TXOUT_U1P
TXOUT_U1N
TXOUT_U2P
TXOUT_U2N
TXOUT_U3P
TXOUT_U3N
TXOUT_L0P
TXOUT_L0N
TXOUT_L1P
TXOUT_L1N
TXOUT_L2P
TXOUT_L2N
TXOUT_L3P
TXOUT_L3N
TXCLK_UP
TXCLK_UN
TXCLK_LP
TXCLK_LN
LPVDD
LPVSS
LVDDR18D
LVDDR18A_1
LVDDR18A_2
LVSSR1
LVSSR2
LVSSR3
LVSSR4
LVSSR5
LVSSR6
LVSSR7
LVSSR8
LVDS_DIGON
LVDS_BLON
LVDS_BLEN
GFX_CLKP
GFX_CLKN
HTTSTCLK
HTREFCLK
SB_CLKP
SB_CLKN
DFT_GPIO3/RSV
DFT_GPIO4/RSV
DFT_GPIO5/RSV
TMDS_HPD
STRP_DATA
DDC_DATA
TESTMODE
CHANGE TO 71.RS48M.B0U (VER A22)
DO NOT SUPPORT SIDEPORT MEMORY
DO NOT SUPPORT SERIAL STRAP ROM
DUMMY IT
Dummy when use Discrete
DY
Place close the two resistor
TSLCX08MTC-U
U22A
U22B
U22D
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
<Variant Name>
Title
ATI-RS480M (3 of 4) LVDS CRT
Size A3
Document Number
Bolsena
Rev -1
Date: Thursday, March 31, 2005
Sheet 13 of 58

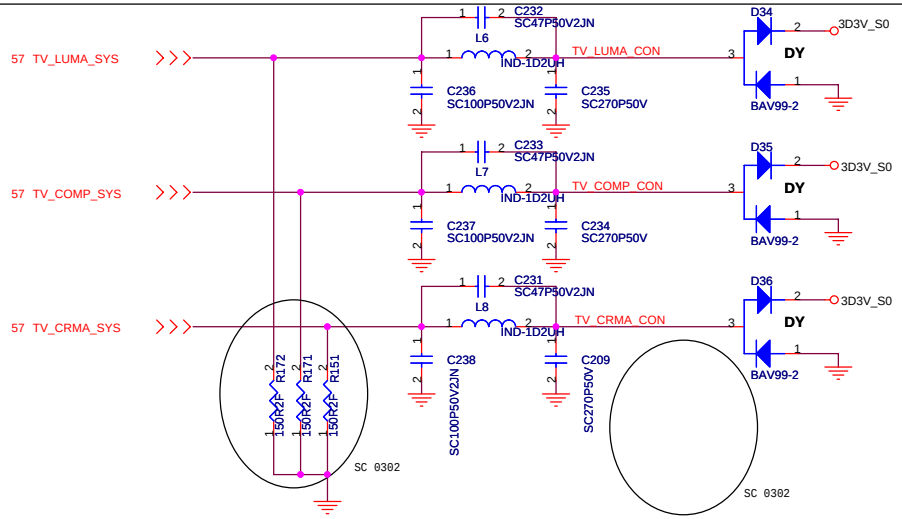

GROUND
PAR 6 OF 6
U80F
U80E
PART 5 OF 6
POWER
1D2V_S0
1D8V_S0
1D8V_VDDA
1D2V_VDDA_RS480_S0
1D8VDD_S0
3D3V_S0
VDDHT30
VDDHT31
VDDA12_13
VDDA18_13
DY
SCD1U16V
SC10U10V5ZY
SC4D7U10V5ZY
BLM11A121S
MLB-201209-11
ST100U6D3VDM-5
BAV99-1
0R2-0
SB 0127
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATI-RS480M (4 of 4) PWR, GND
Bolsena
Size A3
Rev -1
Date: Thursday, March 31, 2005
Sheet 14 of 58
CHANGE TO 71.RS48M.B0U (VER A22)

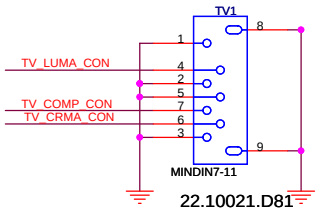

3D3V_S0
5V_S0
RN16
SRN10KJ
RN15
SRN10KJ
U11
2N7002DW
To Discrete
RN20
SRN0-2-U
DVI_D_1
DVI_C_1
49 DIS_DVI_DDC_D
49 DIS_DVI_DDC_C
Dummy when use UMA
To EZ4 (5V level)
EZ4_DVI_DDC_D 57
EZ4_DVI_DDC_C 57
TMDS_EZ4_TX2- 49,57
TMDS_EZ4_TX2+ 49,57
TMDS_EZ4_TX1- 49,57
TMDS_EZ4_TX1+ 49,57
TMDS_EZ4_TX0- 49,57
TMDS_EZ4_TX0+ 49,57
TMDS_EZ4_TXC+ 49,57
TMDS_EZ4_TXC- 49,57
SB 0202
To UMA
RN21
SRN0-2-U
13 DDC_DATA
13 RS480_CLK
U10
CH7301C-T
TMDS_UMA_HPD
SB change much in this page 0127
Dummy when use Discrete
SB 0127
To Discrete
49 DVI_HPD
R42
0R2-0
TMDS_HPD
Dummy when use UMA
13 TMDS_UMA_HPD
R41
0R2-0
To UMA & CH7301
Dummy when use Discrete
R43
10KR2
R56
10KR2
Q3
CHT2222A
Q4
CHT2222A
R4
10KR2
DVI_EZ4_HPD 57
R3
100KR2
SB 0127
Dummy when no EZ4
Place Near Dock
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
UMA DVI - CH7301C
Size
A3
Document Number
Bolsena
Rev
-1
Date: Thursday, March 31, 2005
Sheet 15 of 58

CRT CONN

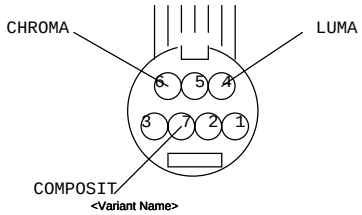
200mA Rating/Spec 500mA





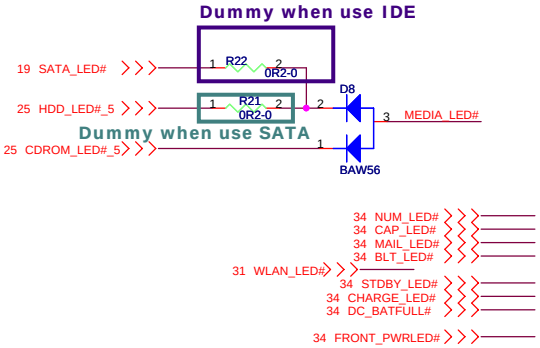


TV CONN

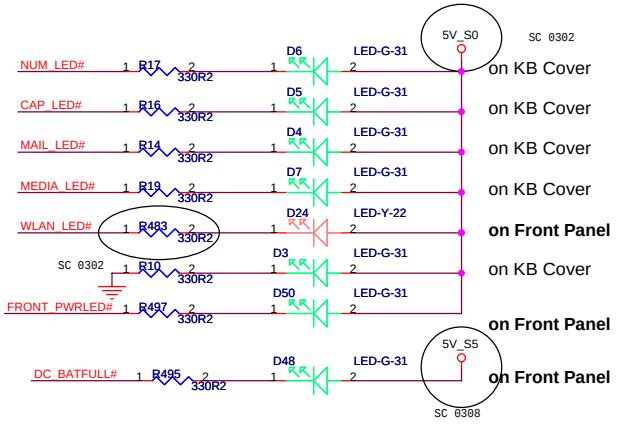


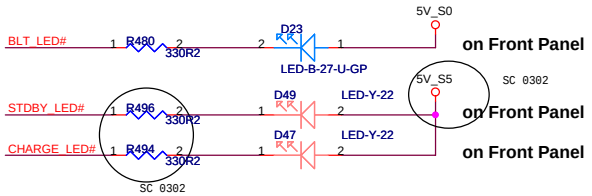
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CRT / TV	
Size A3	Document Number: Bolsena	Rev -1
Date: Thursday, March 31, 2005	Sheet 16 of 58	

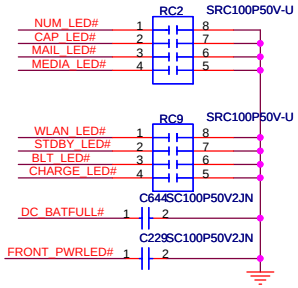
LEDs



?modify R
?half light







on KB cover

LED	V	V				V	V	V
Button	V	V	V	V	V			
	POWER1	E-MAIL	INTERNET	e-BTN	PROGRAM	CAPS	NUM	HDD

Front panel

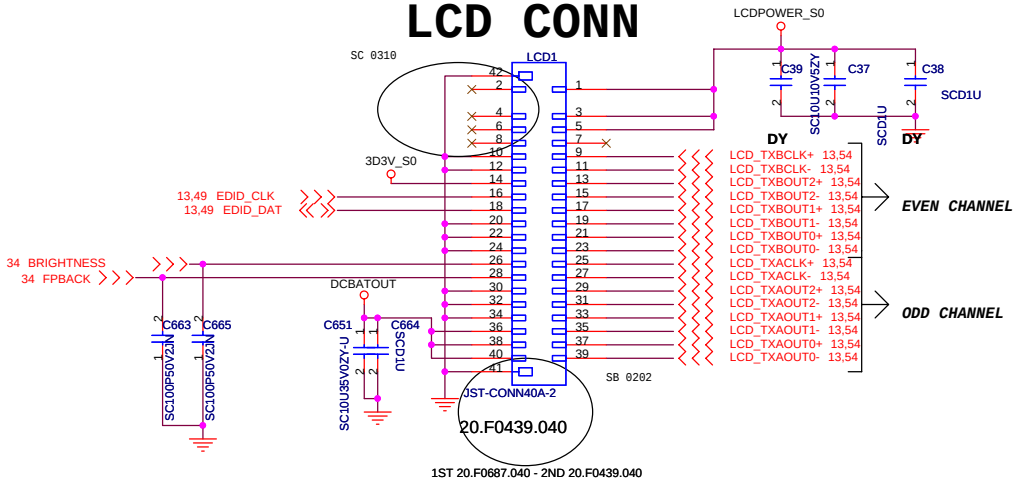
LED	V	V	V	V
Button	V	V		
	BlutTooth	Wireless	Charger	Power2

Charger:
Green : DC only or Battery full with DC
Orange : Charging
Orange Blink : Battery low

Power2:
Green : S0
Orange : S3
Orange Blinking : Enter S4

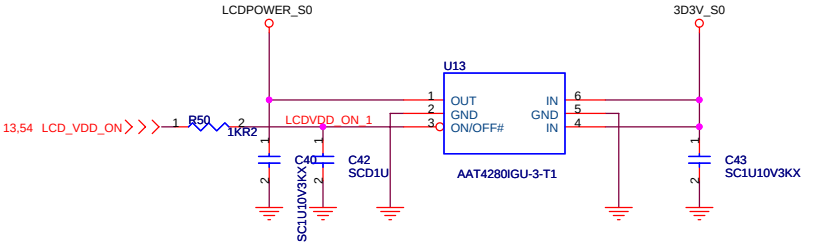
(Please See M.E. drawing LED position)

LCD CONN



LCD POWER

Layout 40 mil



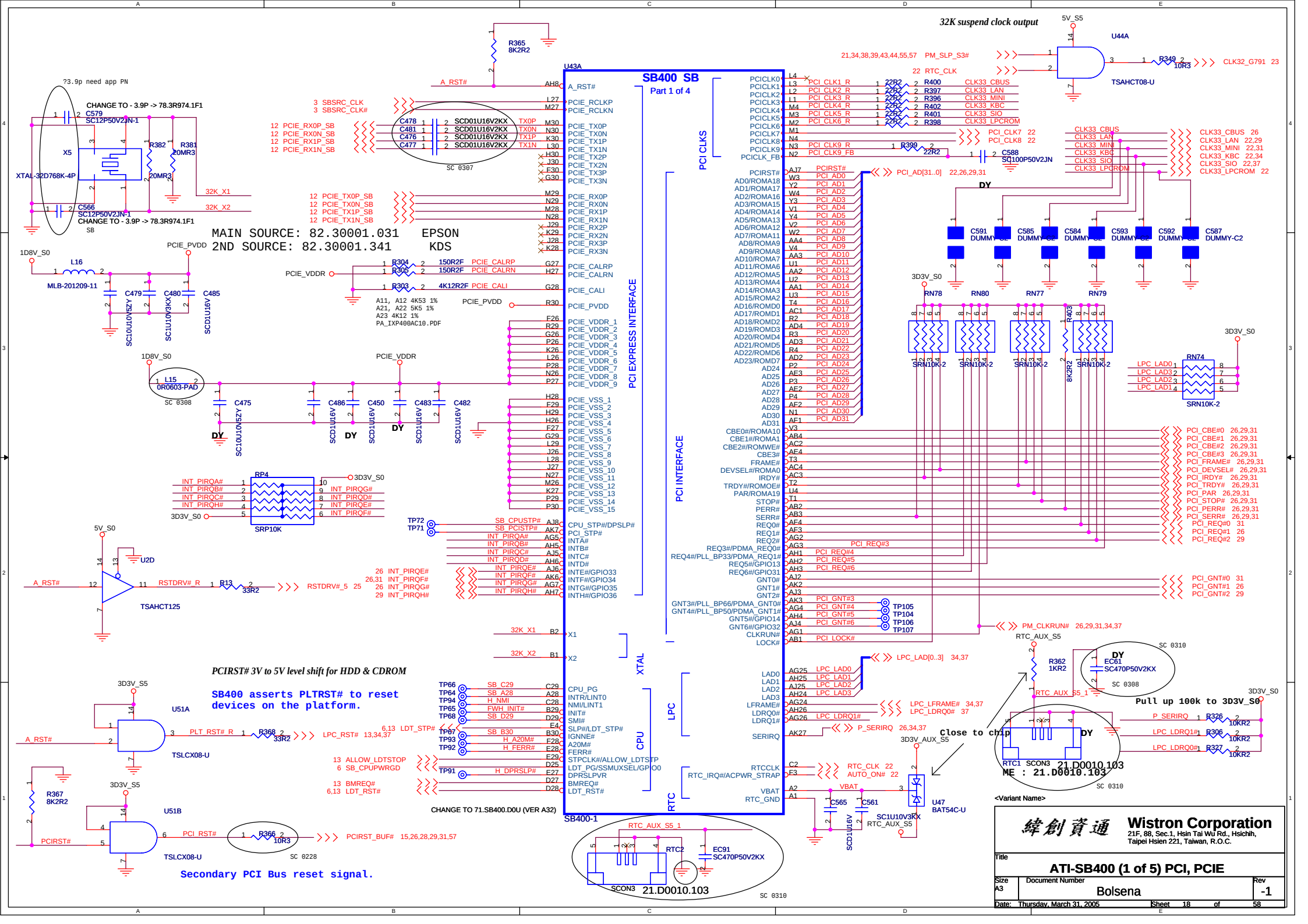
<Variant Name>

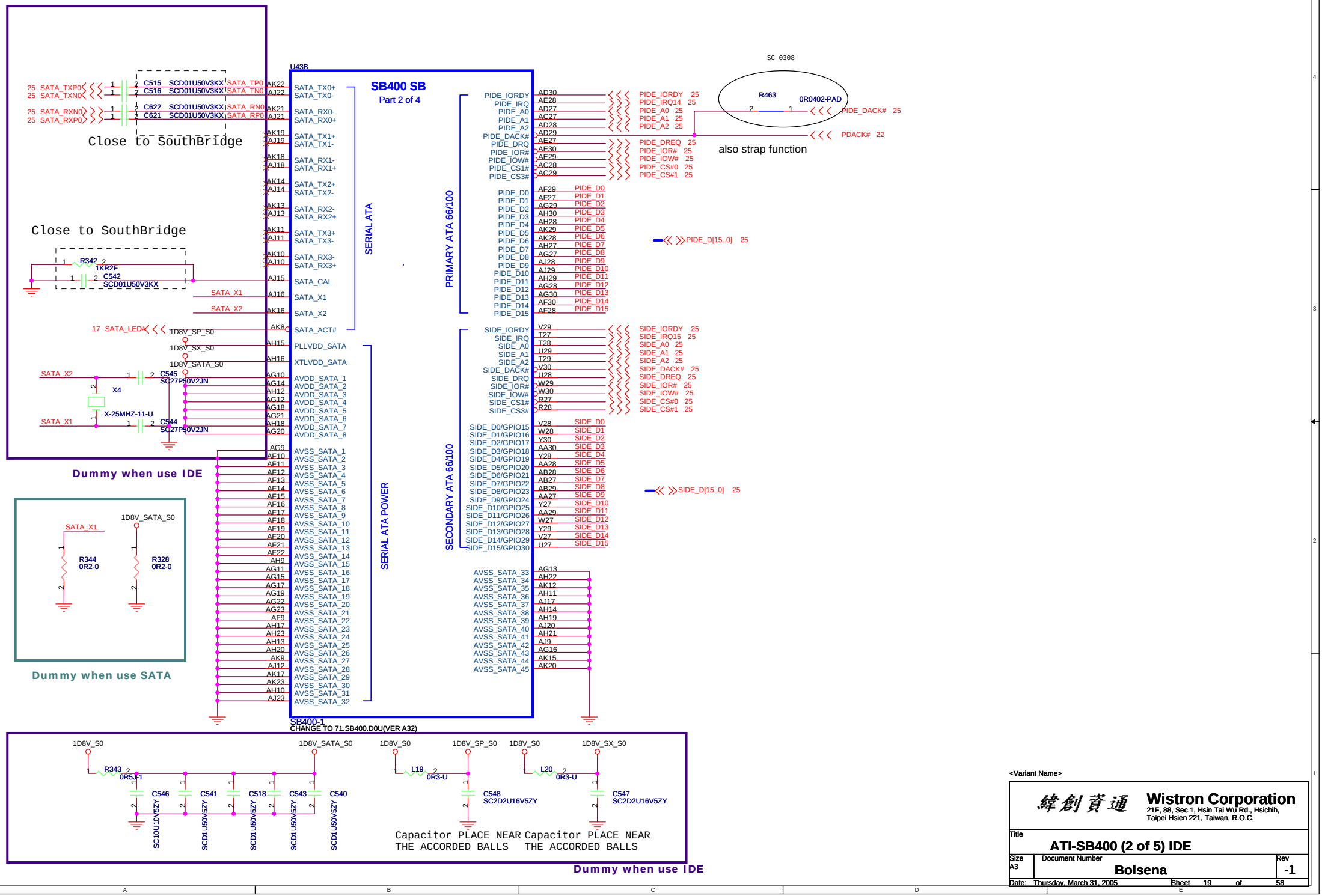
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD / LEDs**

Size	Document Number	Rev
A3	**Bolsena**	-1

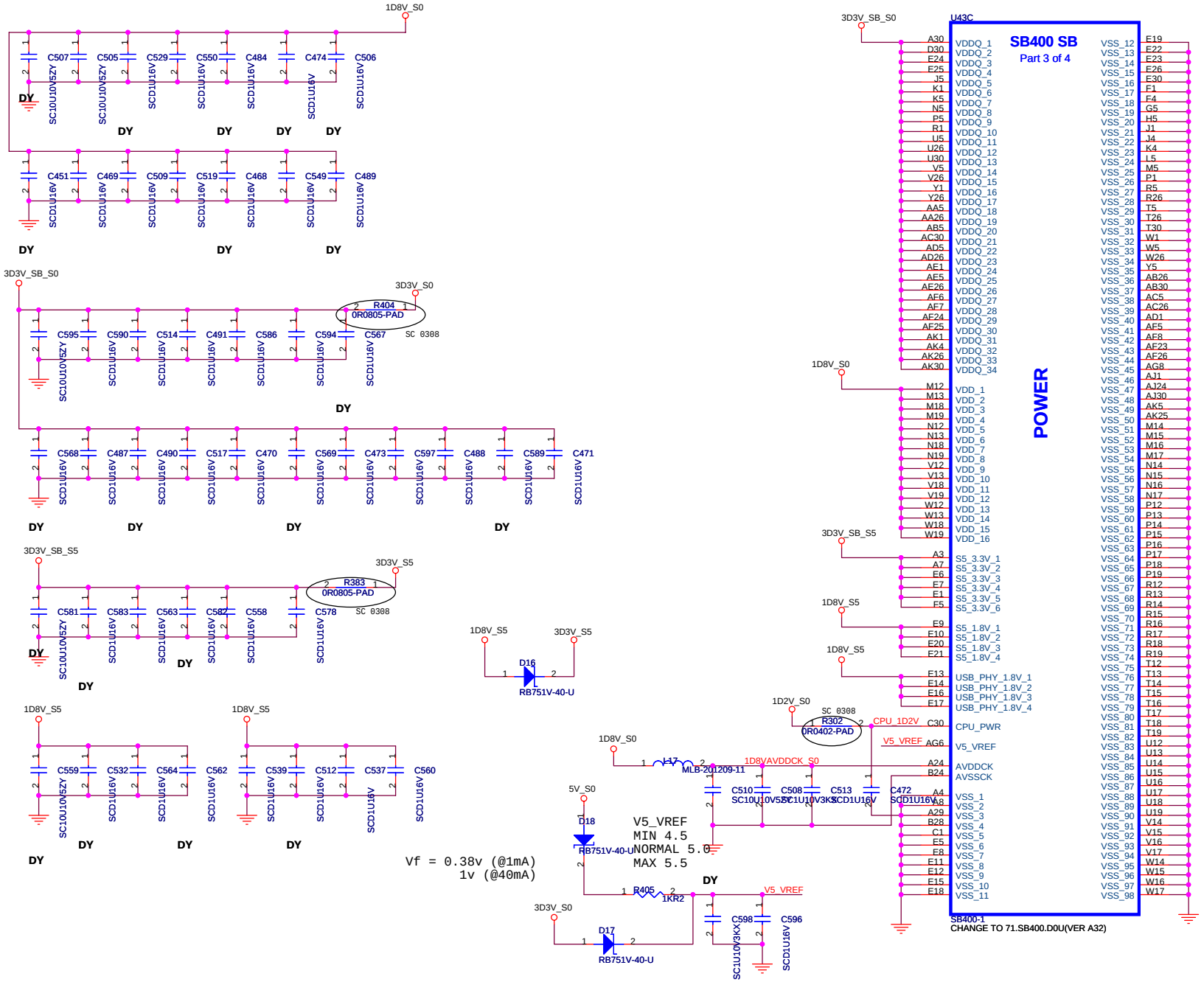
Date: Thursday, March 31, 2005 Sheet 17 of 58


32K suspend clock output
SB400 SB
Part 1 of 4
U43A
SB400-1
MAIN SOURCE: 82.30001.031 EPSON
2ND SOURCE: 82.30001.341 KDS
CHANGE TO - 3.9P -> 78.3R974.1F1
PCIRST# 3V to 5V level shift for HDD & CDROM
SB400 asserts PLTRST# to reset devices on the platform.
Secondary PCI Bus reset signal.
CHANGE TO 71.SB400.D0U (VER A32)
Close to chip
Pull up 100k to 3D3V_S0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATI-SB400 (1 of 5) PCI, PCIE
Bolsena
Rev -1
Thursday, March 31, 2005
Sheet 18 of 58



<variant_name>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ATI-SB400 (2 of 5) IDE
Size A3	Document Number: Bolsena
Rev	-1
Date: Thursday, March 31, 2005	Sheet 19 of 58



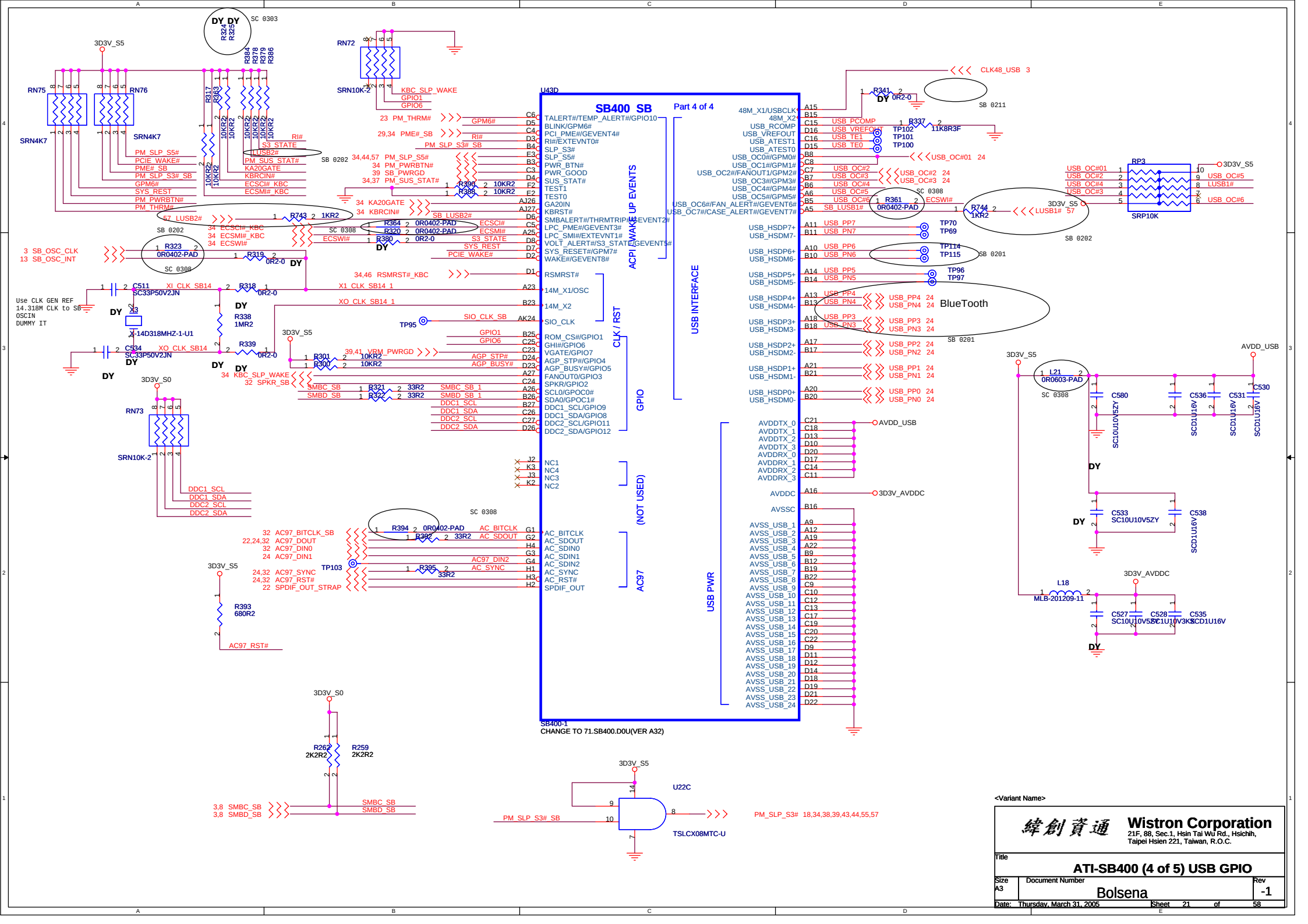
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

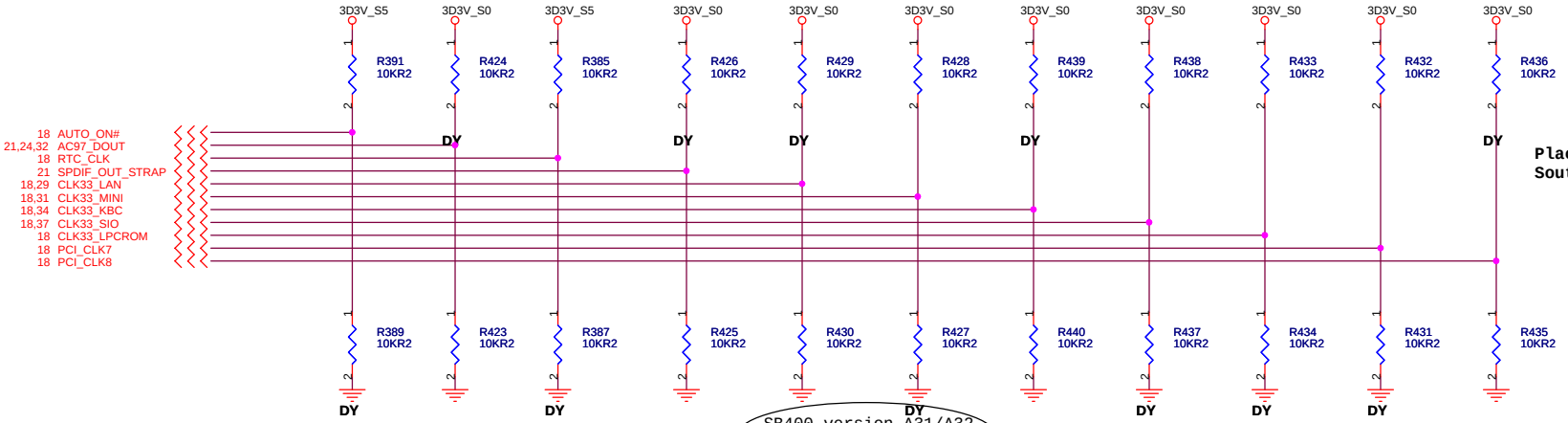
<Variant Name>

Title: ATI-SB400 (3 of 5) POWER

Size	Document Number	Rev
A3	Bolsena	-1

Date: Thursday, March 31, 2005 Sheet 20 of 58


SB400 SB
Part 4 of 4
U43D
ACPI/WAKE UP EVENTS
CLK / RST
GPIO
USB INTERFACE
(NOT USED)
AC97
USB PWR
SB400-1
CHANGE TO 71.SB400.D0U(VER A32)
BlueTooth
Use CLK GEN REF
14.318M CLK to SB
OSCIN
DUMMY IT
U22C
TSLCX08MTC-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
<Variant Name>
Title
ATI-SB400 (4 of 5) USB GPIO
Size A3
Document Number
Bolsena
Rev -1
Date: Thursday, March 31, 2005
Sheet 21 of 58

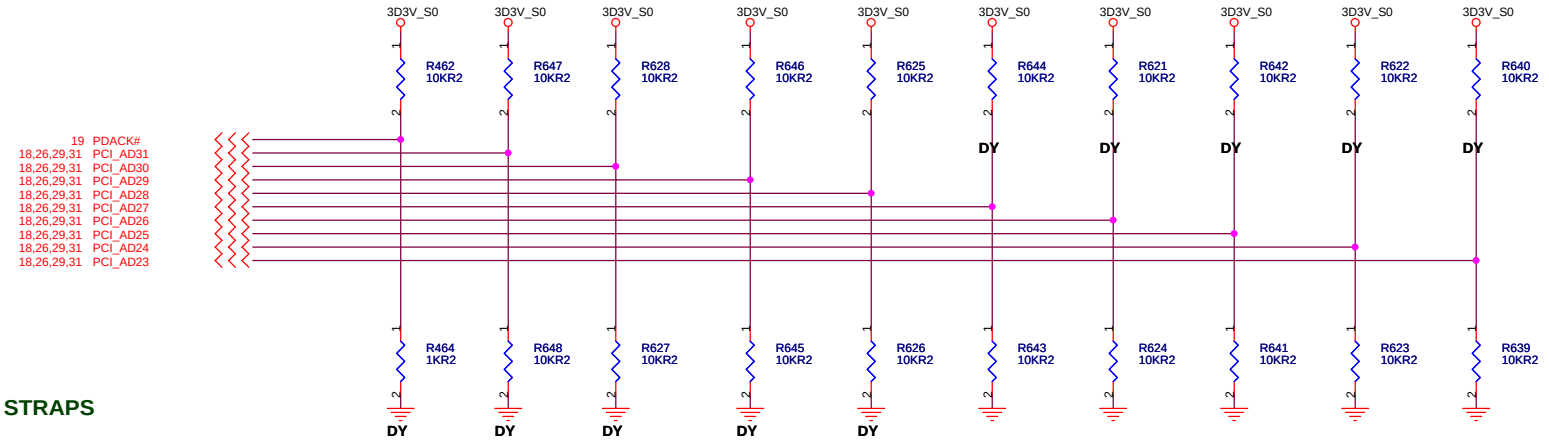


Place these R close to SouthBridge if possible

SB400 version A31/A32 not the same!

REQUIRED SYSTEM STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7 PCI_CLK8
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHZ-Clock Input Buffer DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	USB INT PLL48 DEFAULT	14MHZ OSC MODE DEFAULT	CPU I/F=K8 DEFAULT	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTENNAL RTC (NOT SUPPORTED W/IT8712)	SIO 48MHz DEFAULT	48MHZ -Crytsal Pad	USB PHY PWRDOWN ENABLE	USB EXT. 48MHZ	14MHZ XTAL MODE	CPU I/F=P4	L,H=LPC ROM II L,L=Firmware Hub ROM



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

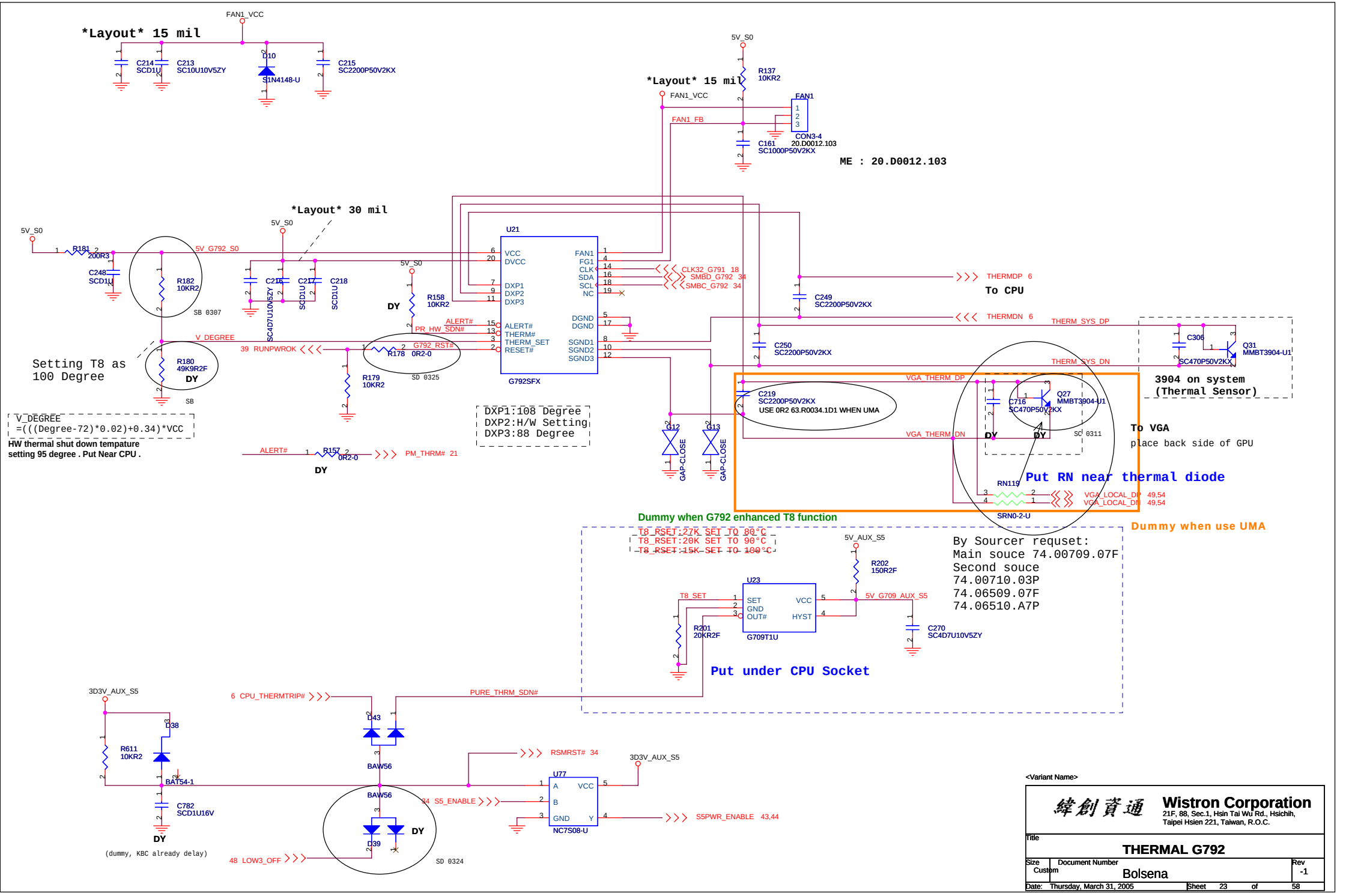
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB400 STRAPPING(5 of 5)

Size: A3 | Document Number: Bolsena | Rev: -1

Date: Thursday, March 31, 2005 | Sheet 22 of 58



<Variant Name>

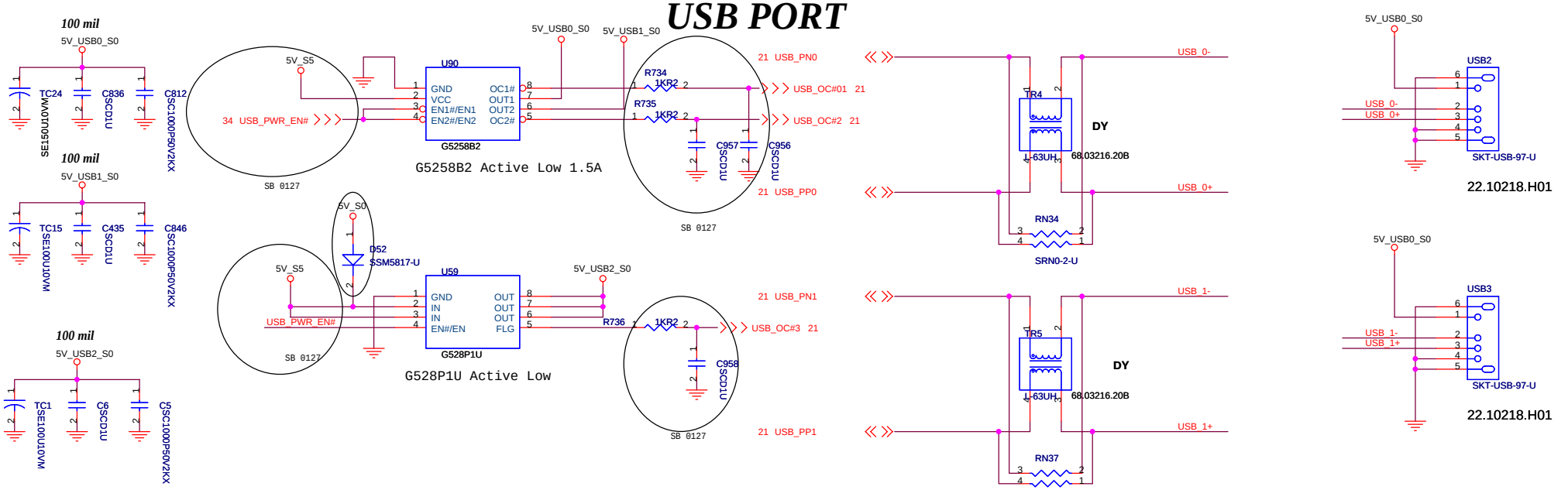
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **THERMAL G792**

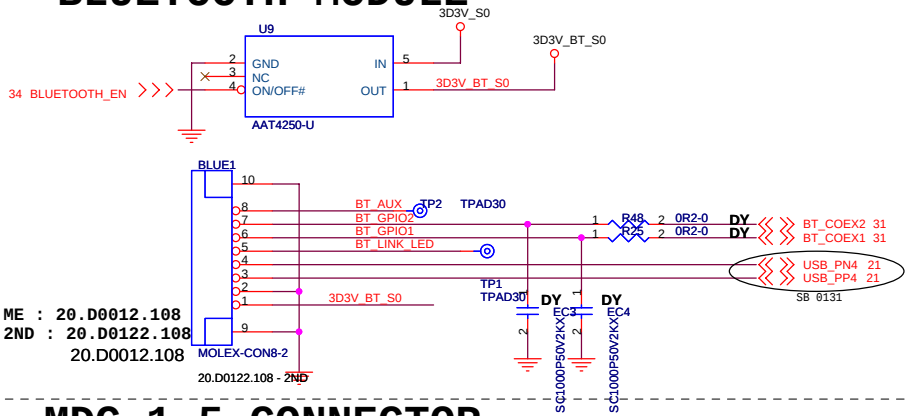
Size	Document Number	Rev
Custom	Bolsena	-1

Date: Thursday, March 31, 2005 Sheet 23 of 58

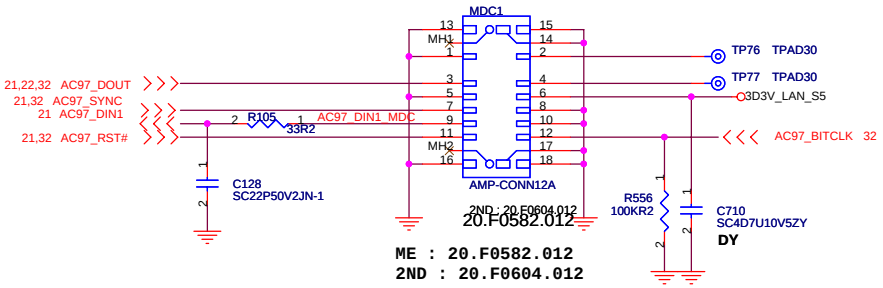
USB PORT

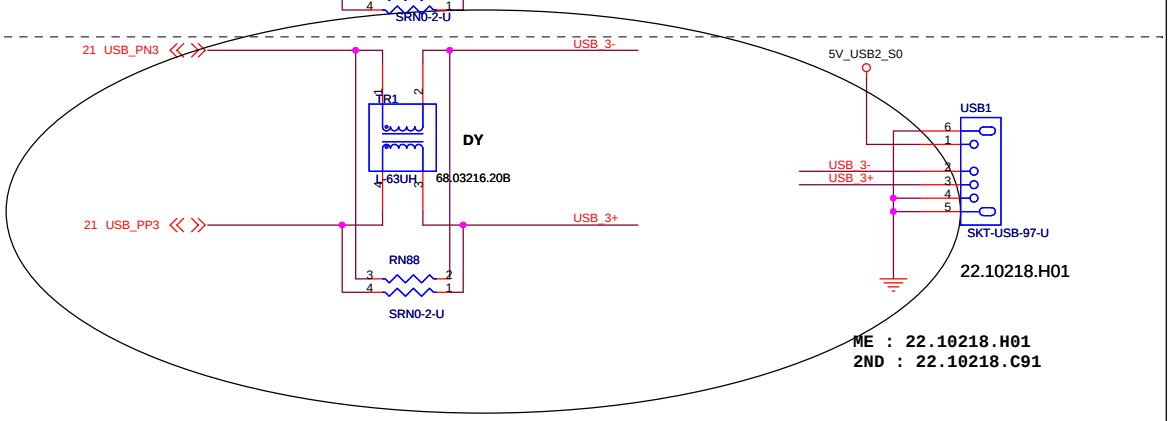


BLUETOOTH MODULE



MDC 1.5 CONNECTOR





<Variant Name>

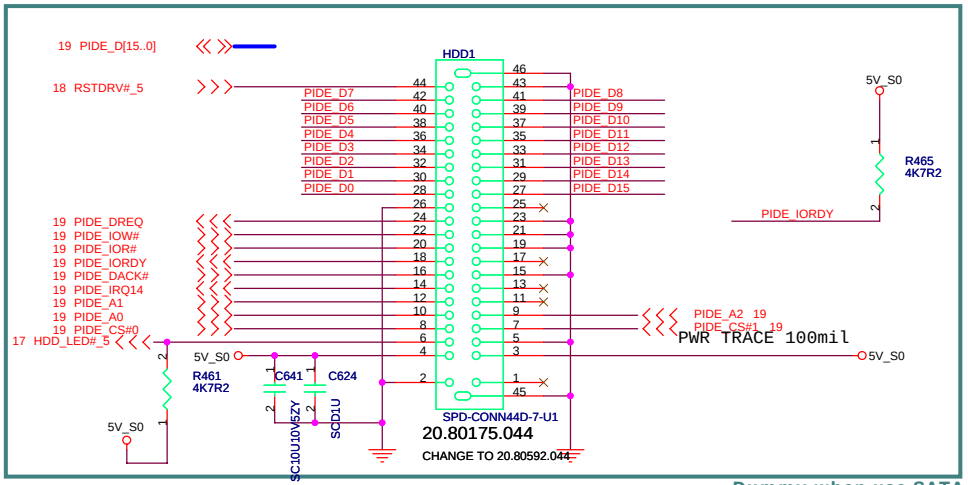
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB / MDC / BLUETOOTH

Size: A3 | Document Number: Bolsena | Rev: -1

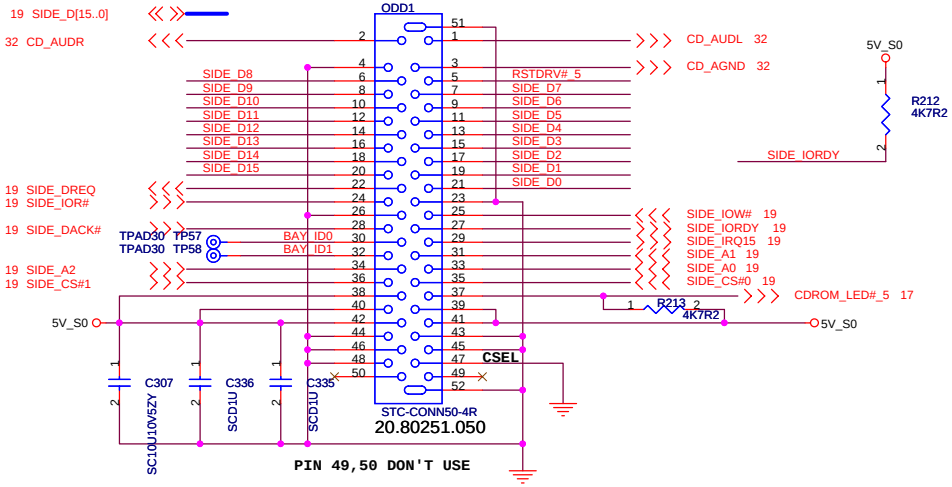
Date: Thursday, March 31, 2005 | Sheet 24 of 58

HDD



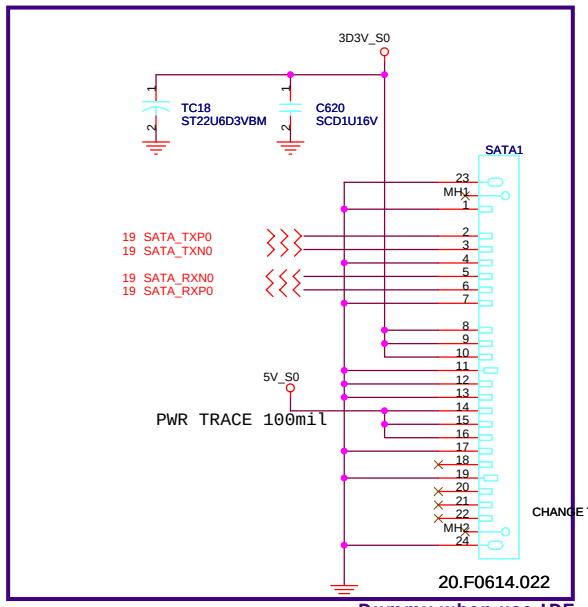
ME : 20.80592.044
(DIFFERENT FROM ORCAD P/N)

CDROM



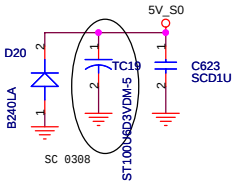
ME : 20.80251.050

SATA Connector



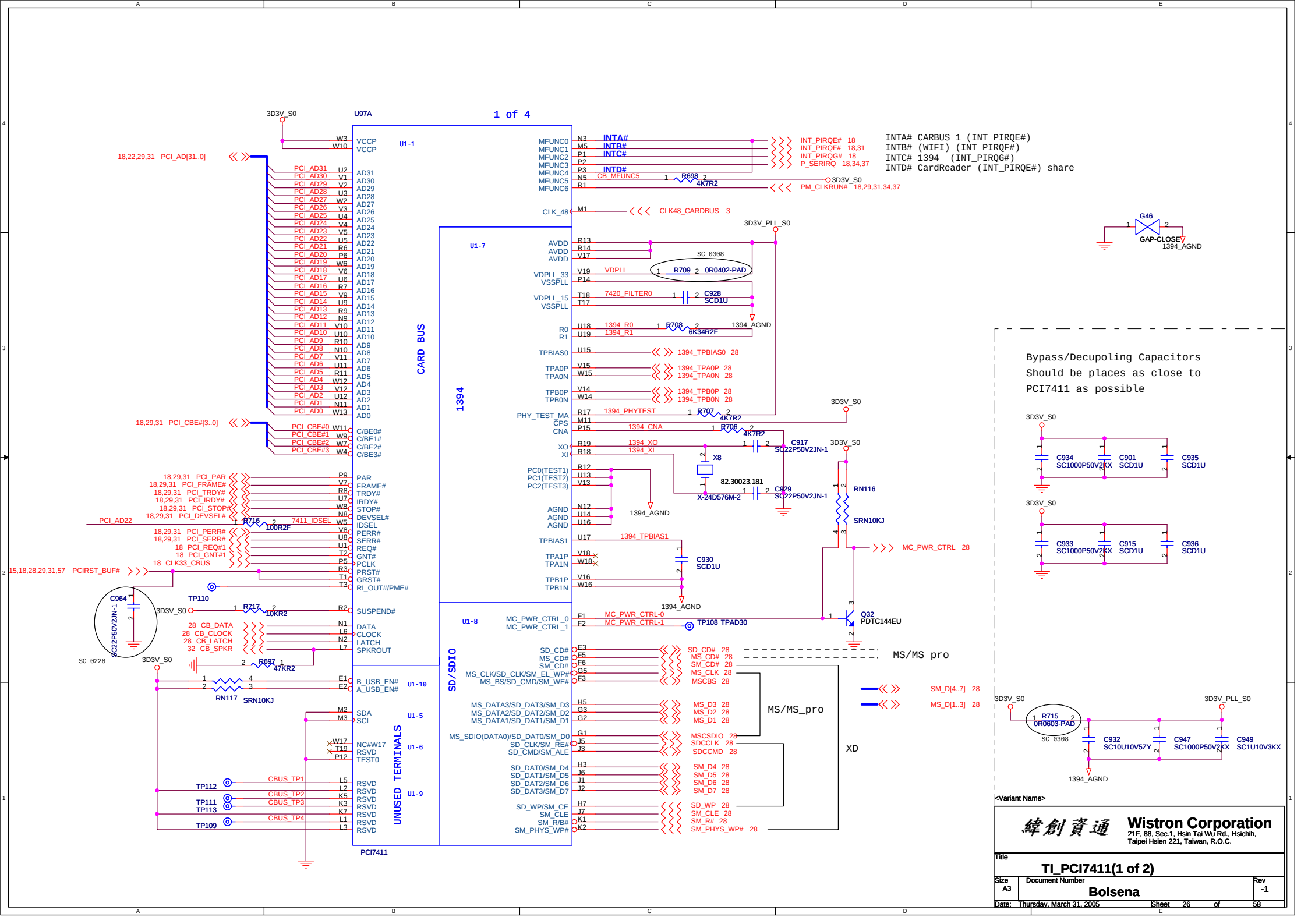
ME : 20.F0665.022
(DIFFERENT FROM ORCAD P/N)

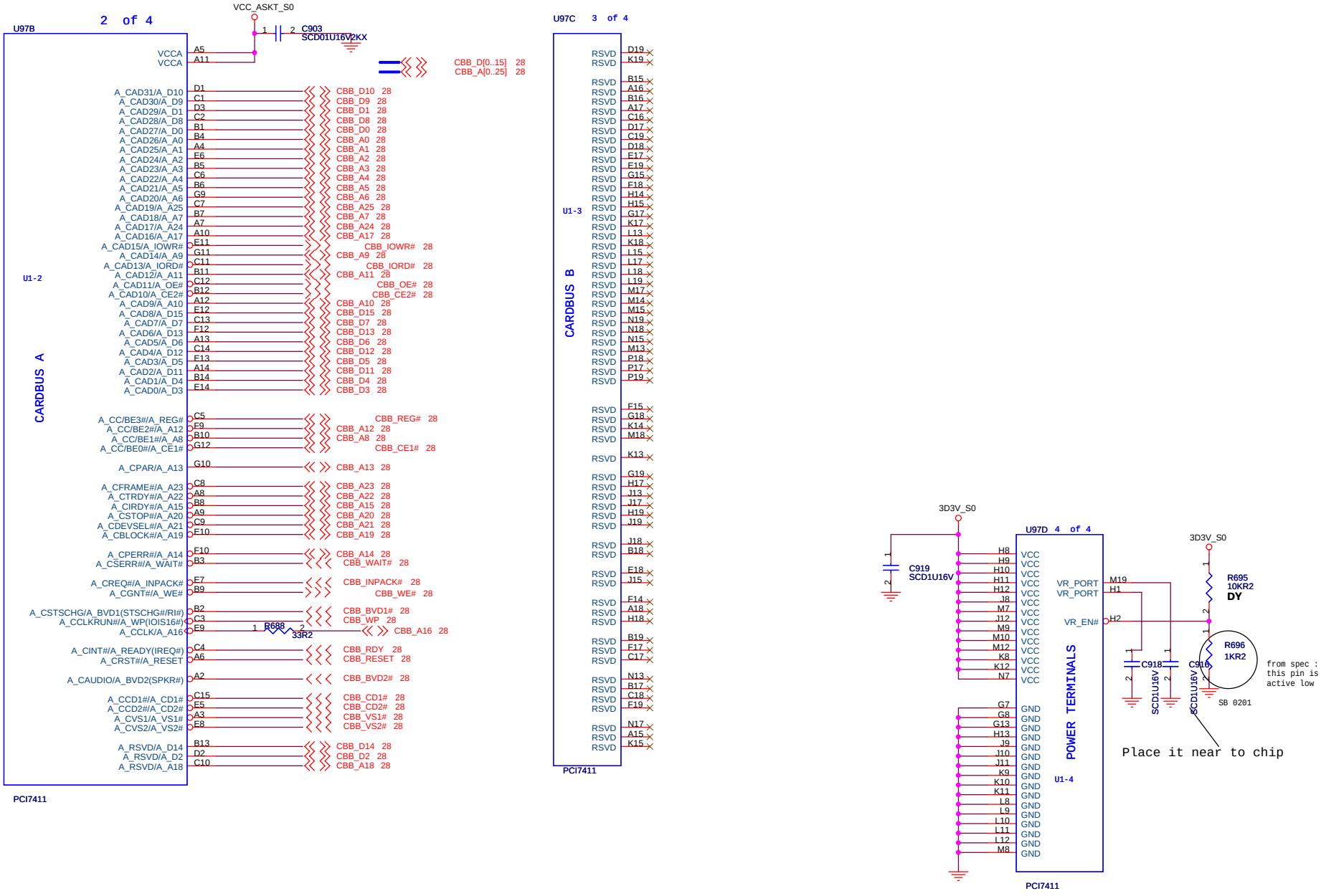
For HDD & SATA both



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**HDD / CDROM / SATA**
Size A3	Document Number **Bolsena** Rev -1
Date: Thursday, March 31, 2005	Sheet 25 of 58


1 of 4
U97A
CARD BUS
1394
SD/SDIO
UNUSED TERMINALS
PCI7411
U1-1
U1-7
U1-8
U1-10
U1-5
U1-6
U1-9
INTA# CARBUS 1 (INT_PIRQE#)
INTB# (WIFI) (INT_PIRQF#)
INTC# 1394 (INT_PIRQG#)
INTD# CardReader (INT_PIRQE#) share
Bypass/Decupoling Capacitors
Should be places as close to
PCI7411 as possible
MS/MS_pro
MS/MS_pro
XD
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TI_PCI7411(1 of 2)
Size A3
Document Number
Bolsena
Rev -1
Date: Thursday, March 31, 2005
Sheet 26 of 58



<Variant Name>

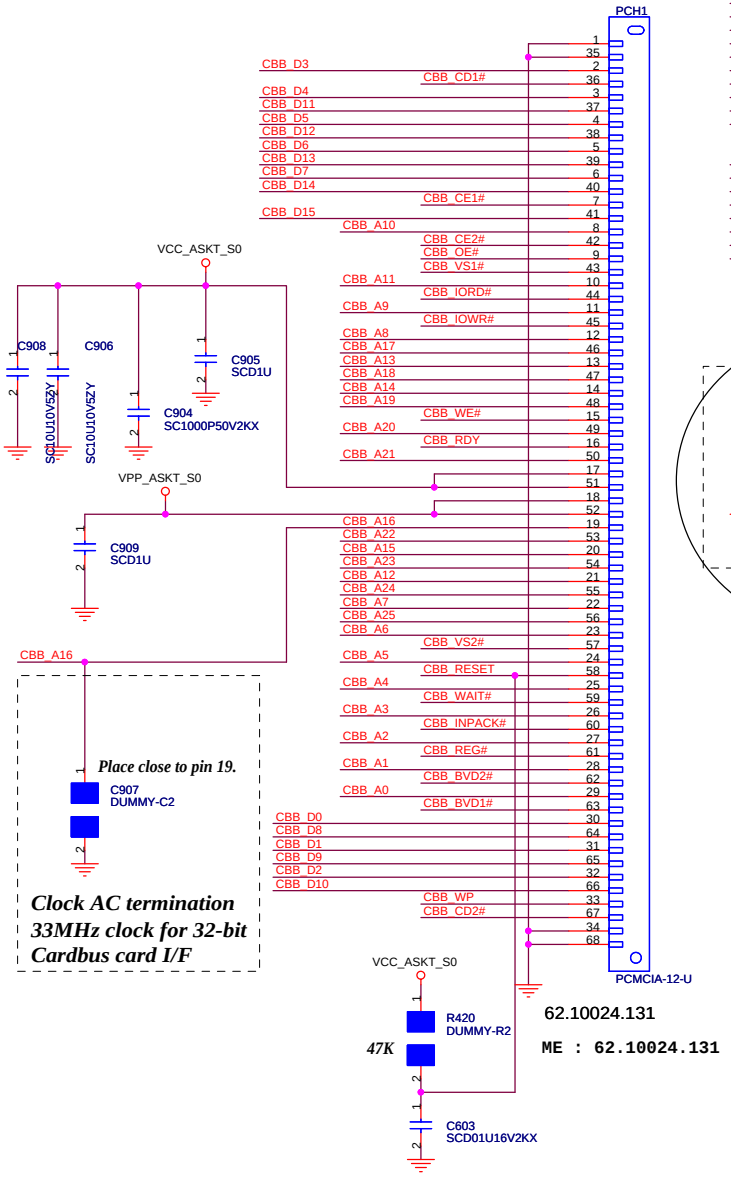
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TI_PCI7411(2 of 2)**

Size	Document Number	Rev
A3	Bolsena	-1

Date: Thursday, March 31, 2005 Sheet 27 of 58

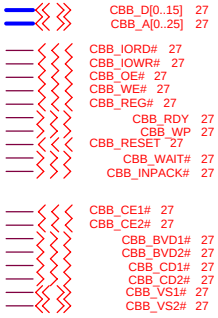
PCMCIA Socket

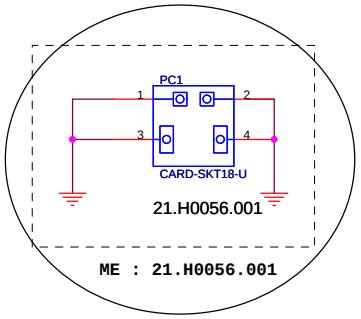


62.10024.131

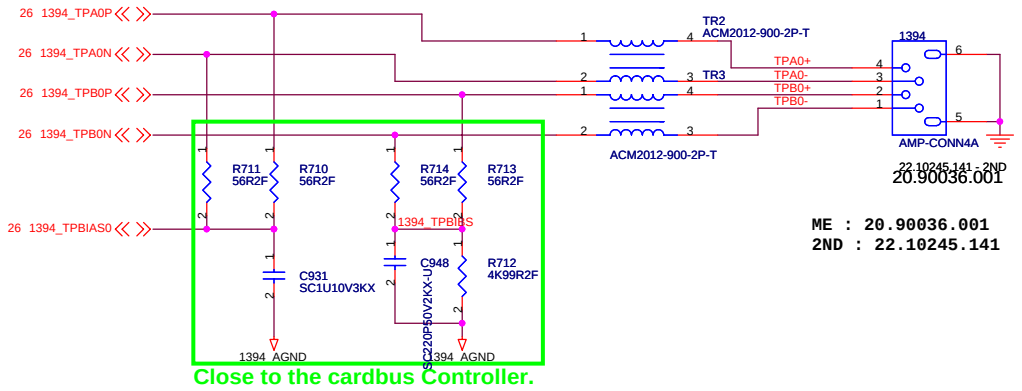
ME : 62.10024.131

Cardbus I/F

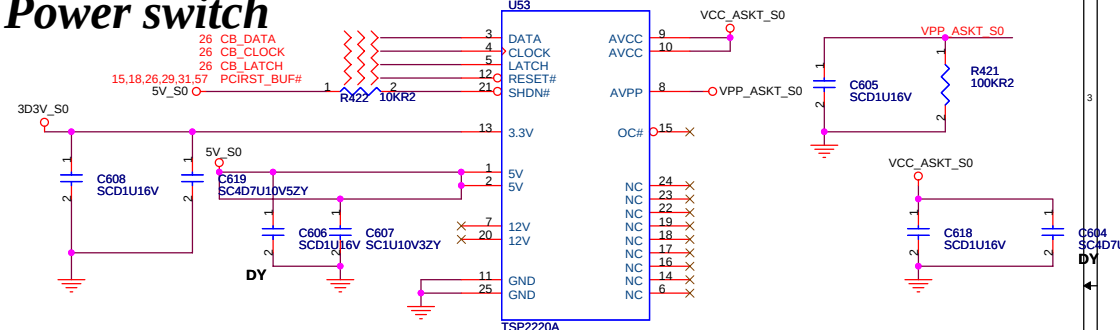


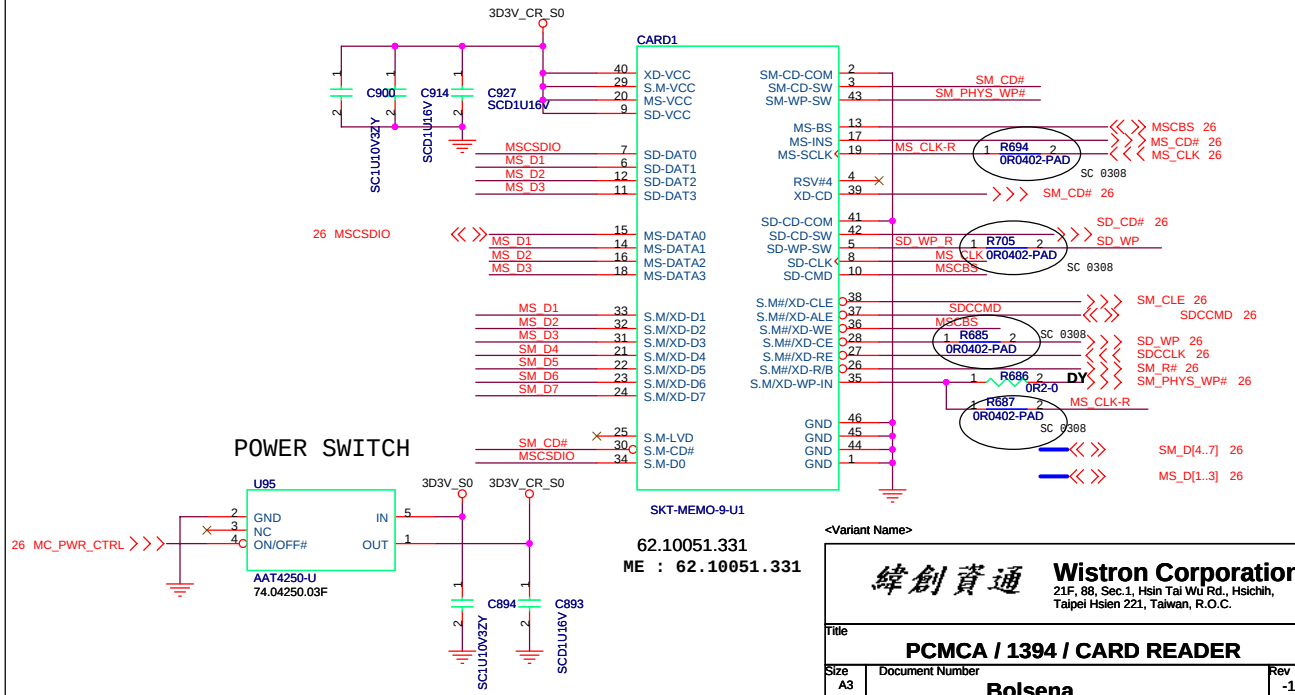


1394 Connector



Power switch





POWER SWITCH

62.10051.331

ME : 62.10051.331

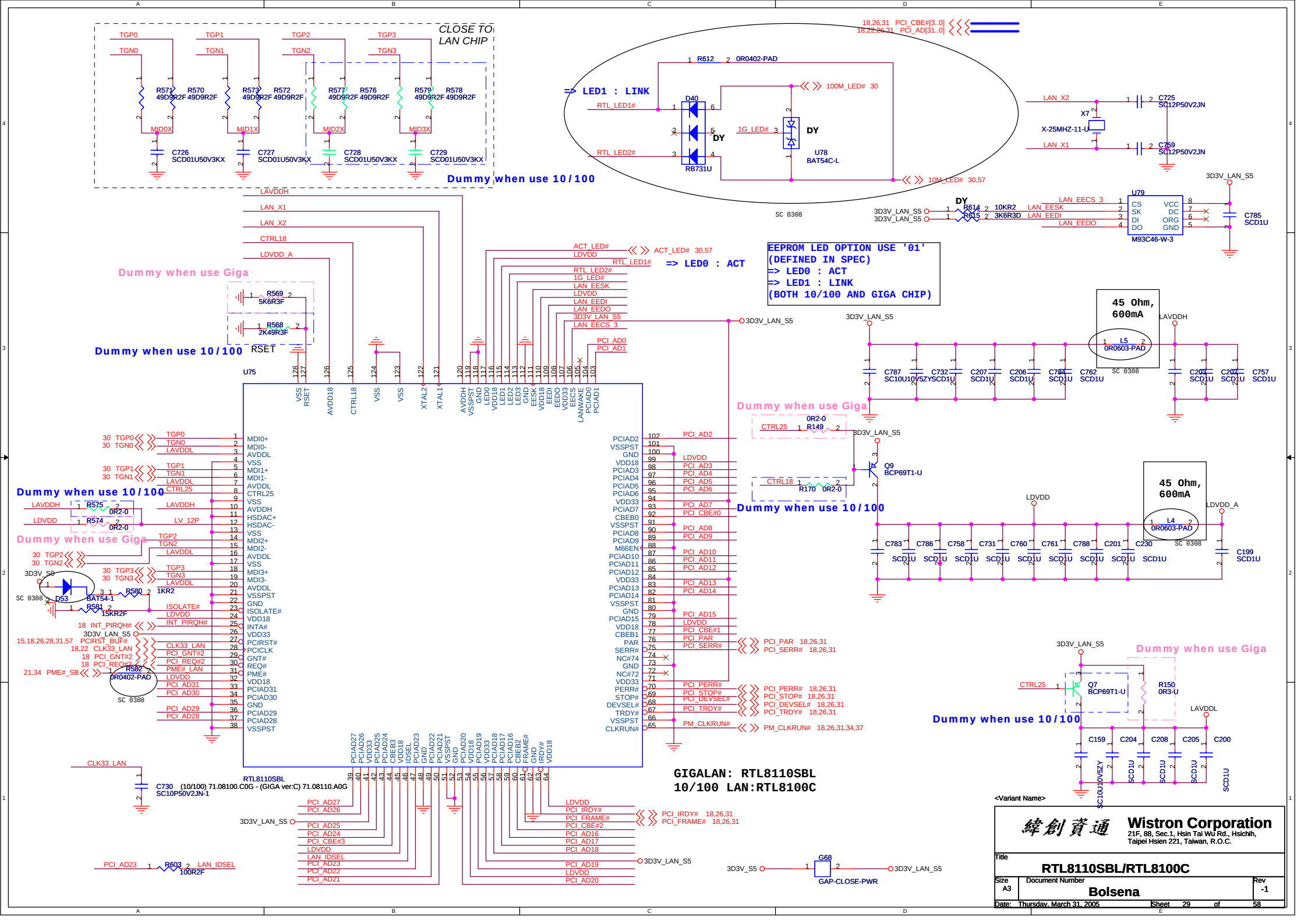
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCMCA / 1394 / CARD READER**

Size	Document Number	Rev
A3	Bolsena	-1

Date: Thursday, March 31, 2005 Sheet 28 of 58


CLOSE TO LAN CHIP
TGP0 TGN0 TGP1 TGN1 TGP2 TGN2 TGP3 TGN3
R571 49D9R2F R570 49D9R2F R573 49D9R2F R572 49D9R2F R577 49D9R2F R576 49D9R2F R579 49D9R2F R578 49D9R2F
MID0X MID1X MID2X MID3X
C726 SCD01U50V3KX C727 SCD01U50V3KX C728 SCD01U50V3KX C729 SCD01U50V3KX
Dummy when use 10/100
18,26,31 PCI_CBE#[3..0]
18,22,26,31 PCI_AD[31..0]
=> LED1 : LINK
R612 0R0402-PAD
100M_LED# 30
RTL_LED1#
D40
1G_LED#
DY
U78 BAT54C-L
RTL_LED2#
RB731U
10M_LED# 30,57
SC 0308
LAN_X2 X7 X-25MHZ-11-U LAN_X1
C725 SC12P50V2JN
C759 SC12P50V2JN
3D3V_LAN_S5
R614 10KR2
R615 3K6R3D
LAN_EECS_3 LAN_EESK LAN_EEDI LAN_EEDO
U79 CS SK DI DO VCC DC ORG GND
M93C46-W-3
C785 SCD1U
LAVDDH LAN_X1 LAN_X2 CTRL18 LDVDD_A
Dummy when use Giga
R569 5K6R3F
R568 2K49R3F
Dummy when use 10/100
RSET
ACT_LED# 30,57
LDVDD
RTL_LED1#
=> LED0 : ACT
RTL_LED2#
1G_LED#
LAN_EESK
LDVDD
LAN_EEDI
LAN_EEDO
3D3V_LAN_S5
LAN_EECS_3
PCI_AD0
PCI_AD1
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)
U75
VSS RSET AVDD18 CTRL18 VSS VSS XTAL2 XTAL1 AVDDH VSSPST GND LED0 VDD18 LED1 LED2 LED3 GND EESK VDD18 EEDI EEDO VDD33 EECS LANWAKE PCIAD0 PCIAD1
45 Ohm, 600mA
L5 0R0603-PAD
C787 SC10U10V5Z C732 SCD1U C207 SCD1U C206 SCD1U C784 SCD1U C762 SCD1U C203 SCD1U C202 SCD1U C757 SCD1U
MDI0+ MDI0- AVDDL VSS MDI1+ MDI1- AVDDL CTRL25 VSS AVDDH HSDAC+ HSDAC- VSS MDI2+ MDI2- AVDDL VSS MDI3+ MDI3- AVDDL VSSPST GND ISOLATE# VDD18 INTA# VDD33 PCIRST# PCICLK GNT# REQ# PME# VDD18 PCIAD31 PCIAD30 GND PCIAD29 PCIAD28 VSSPST
30 TGP0 30 TGN0 TGP1 30 TGP1 30 TGN1 CTRL25 LV_12P TGP2 30 TGP2 30 TGN2 TGP3 30 TGP3 30 TGN3 1KR2 ISOLATE# INT_PIRQH#
R575 0R2-0 R574 0R2-0
Dummy when use 10/100
Dummy when use Giga
3D3V_S0 D53 BAT54-1 R580 15KR2F R581
18 INT_PIRQH#
15,18,26,28,31,57 PCIRST_BUF#
18,22 CLK33_LAN
18 PCI_GNT#2
18 PCI_REQ#2
21,34 PME#_SB
R582 0R0402-PAD
SC 0308
PCIAD2 VSSPST GND VDD18 PCIAD3 PCIAD4 PCIAD5 PCIAD6 VDD33 PCIAD7 CBEB0 VSSPST PCIAD8 PCIAD9 M66EN PCIAD10 PCIAD11 PCIAD12 VDD33 PCIAD13 PCIAD14 VSSPST GND PCIAD15 VDD18 CBEB1 PAR SERR# NC#74 GND NC#72 VDD33 PERR# STOP# DEVSEL# TRDY# VSSPST CLKRUN#
PCI_AD2 LDVDD PCI_AD3 PCI_AD4 PCI_AD5 PCI_AD6 PCI_AD7 PCI_CBE#0 PCI_AD8 PCI_AD9 PCI_AD10 PCI_AD11 PCI_AD12 PCI_AD13 PCI_AD14 PCI_AD15 LDVDD PCI_CBE#1 PCI_PAR PCI_SERR# PCI_PERR# PCI_STOP# PCI_DEVSEL# PCI_TRDY# PM_CLKRUN#
PCI_PAR 18,26,31
PCI_SERR# 18,26,31
PCI_PERR# 18,26,31
PCI_STOP# 18,26,31
PCI_DEVSEL# 18,26,31
PCI_TRDY# 18,26,31
PM_CLKRUN# 18,26,31,34,37
Dummy when use Giga
0R2-0 CTRL25 R149
3D3V_LAN_S5
Q9 BCP69T1-U
CTRL18 R170 0R2-0
Dummy when use 10/100
45 Ohm, 600mA
L4 0R0603-PAD
LDVDD
LDVDD_A
C783 C786 C758 C731 C760 C761 C788 C201 C230 C199 SCD1U
Dummy when use Giga
3D3V_LAN_S5
CTRL25 Q7 BCP69T1-U R150 0R3-U
Dummy when use 10/100
LAVDDL
C159 C204 C208 C205 C200 SC10U10V5Z SCD1U
PCIAD27 PCIAD26 VDD33 PCIAD25 PCIAD24 CBEB3 VDD18 IDSEL PCIAD23 GND PCIAD22 PCIAD21 VSSPST GND PCIAD20 VDD18 PCIAD19 VDD33 PCIAD18 PCIAD17 PCIAD16 CBEB2 FRAME# GND IRDY# VDD18
RTL8110SBL
C730 (10/100) 71.08100.C0G - (GIGA ver:C) 71.08110.A0G SC10P50V2JN-1
CLK33_LAN
PCI_AD27 PCI_AD26 PCI_AD25 PCI_AD24 PCI_CBE#3 LDVDD LAN_IDSEL PCI_AD23 PCI_AD22 PCI_AD21
PCI_AD23 R603 100R2F LAN_IDSEL
LDVDD PCI_IRDY# PCI_FRAME# PCI_CBE#2 PCI_AD16 PCI_AD17 PCI_AD18 PCI_AD19 LDVDD PCI_AD20
PCI_IRDY# 18,26,31
PCI_FRAME# 18,26,31
3D3V_S5 G68 GAP-CLOSE-PWR
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
RTL8110SBL/RTL8100C
Size A3
Document Number
Bolsena
Rev -1
Date: Thursday, March 31, 2005
Sheet 29 of 58

Link: Green - 10Mbps/802.11b Activity: Yellow
Orange - 100Mbps/802.11a
Yellow - 1Gbps

LINK:GREEN ON
ACT:YELLOW BLINKING

22.10177.721
22.10177.711
LED COLOR
A1:GREEN
A3:ORANGE
B2:YELLOW

22.10177.711 - 2ND

ME : 22.10177.721
2nd : (canceled)

SC 0310

21.D0010.102

ME : 21.D0010.102

10/100M Lan Transformer

Dummy when use Giga

CHANGE NETSWAP?

LANKOM 68.0H80P.301

GIGA Lan Transformer

LANKOM 68.02402.30A
netSWAP 68.62401.301 (GIGA ,Thick)

SC 0310

NETSWAP GIGA THICK PN IS 68.62401.301, DON'T USE NETSWAP THIN

Dummy when use 10/100

Dummy when use Giga

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

Function	SEL
An to nB1	L
An to nB2	H

LAN switch

SYSTEM

DOCK

PI3L301DA

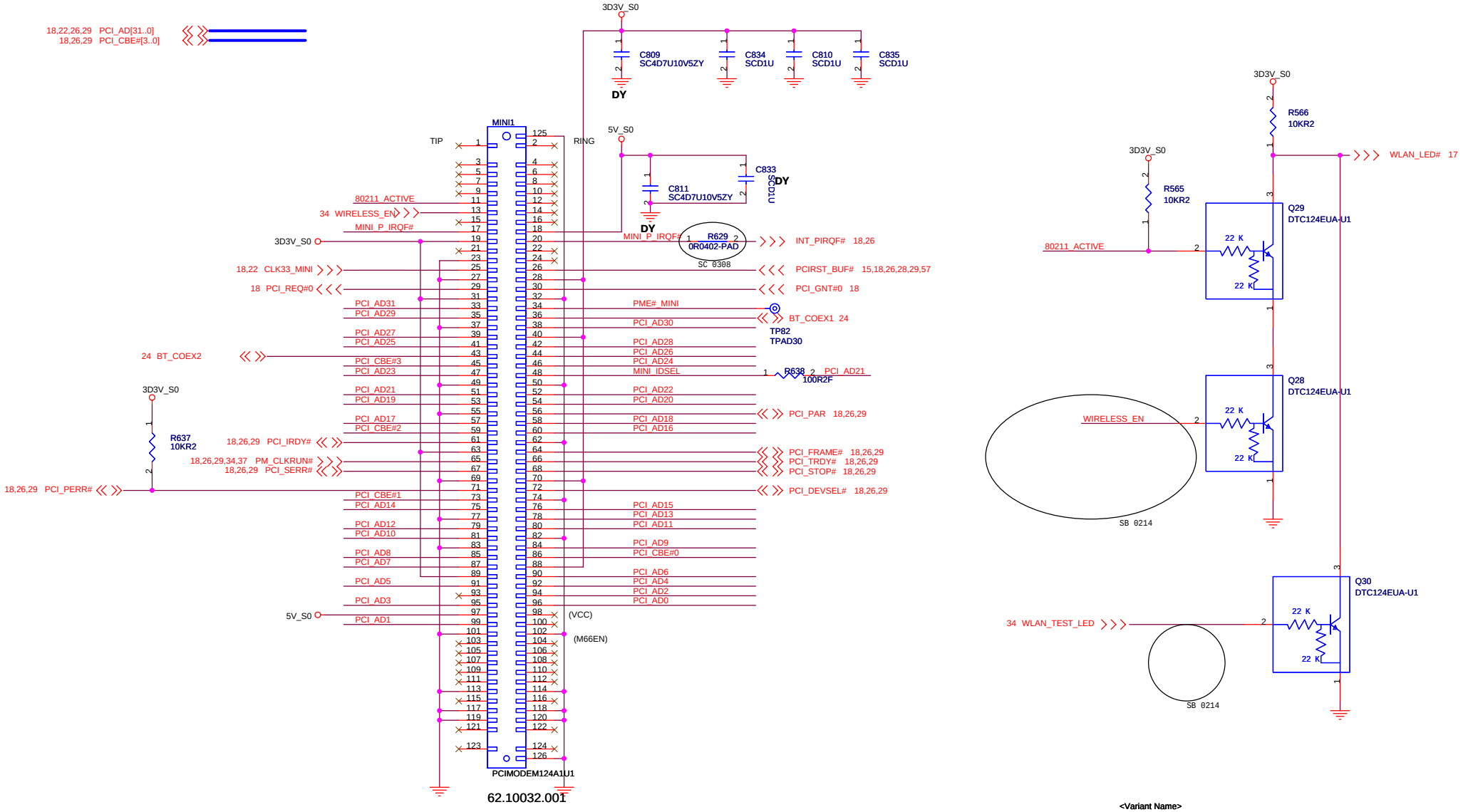
Dummy when no EZ4

Dummy when use EZ4

Title	LAN CONN
Size	A3
Document Number	Bolsena
Rev	-1
Date:	Thursday, March 31, 2005
Sheet	30 of 58

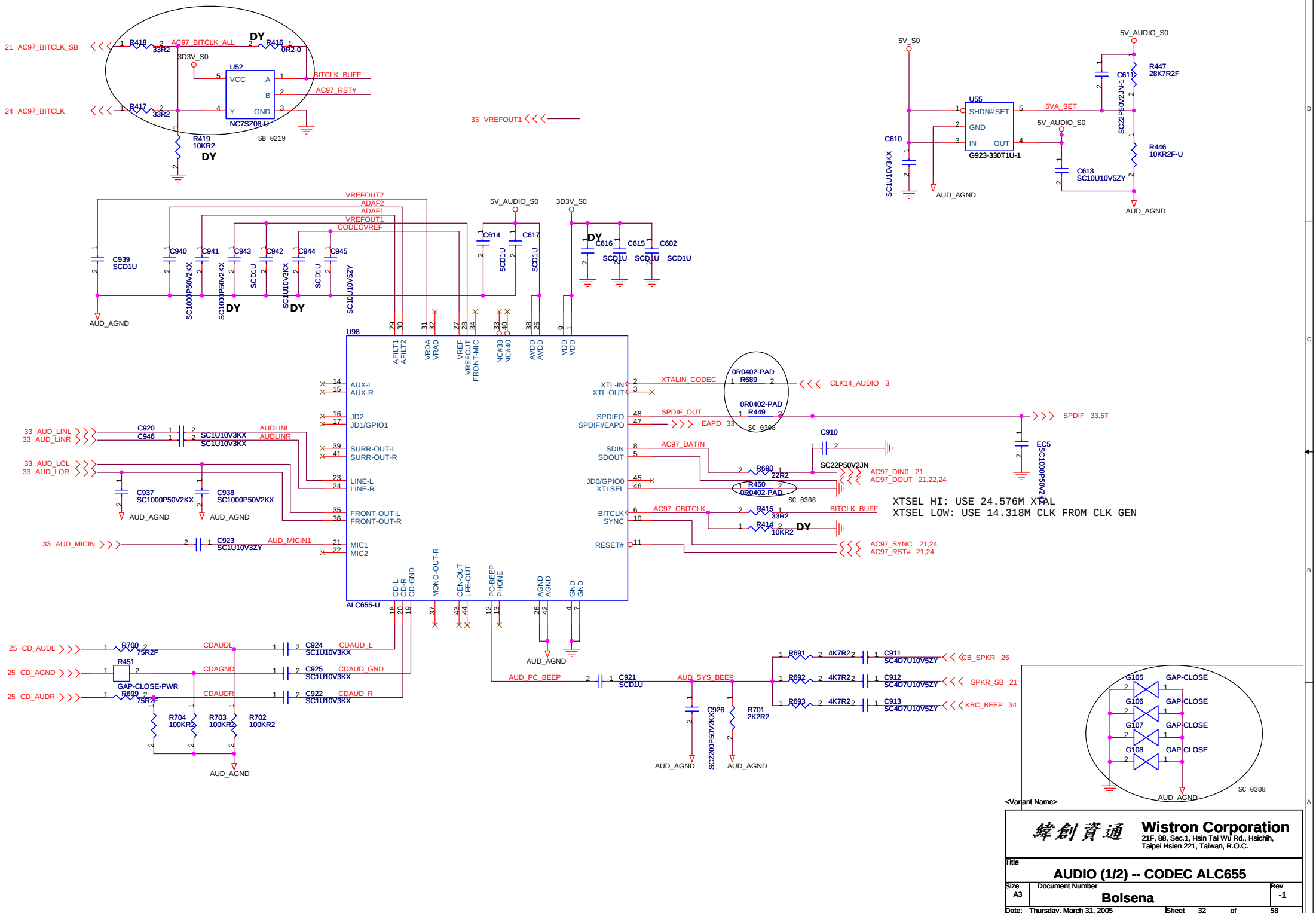
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

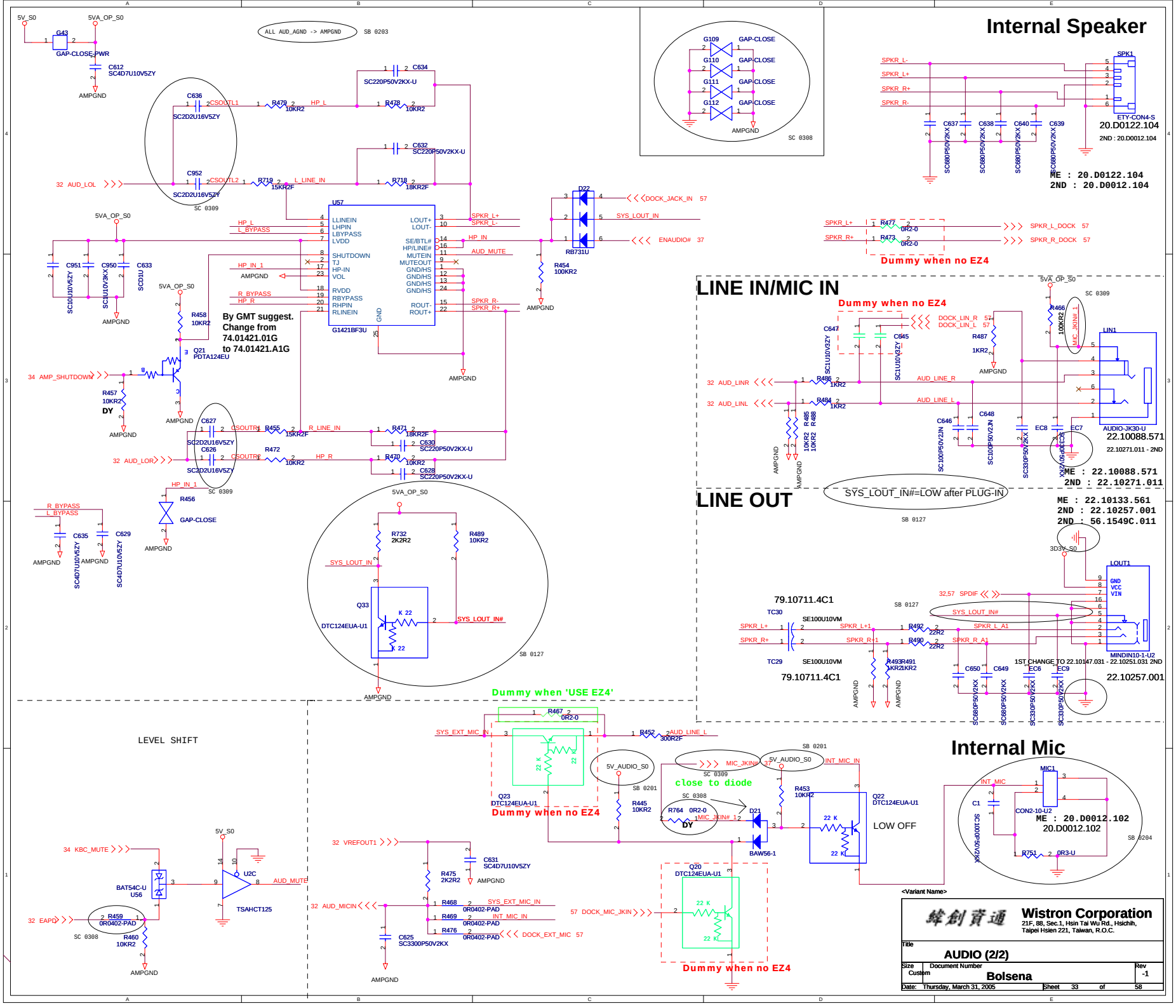
MINI-PCI

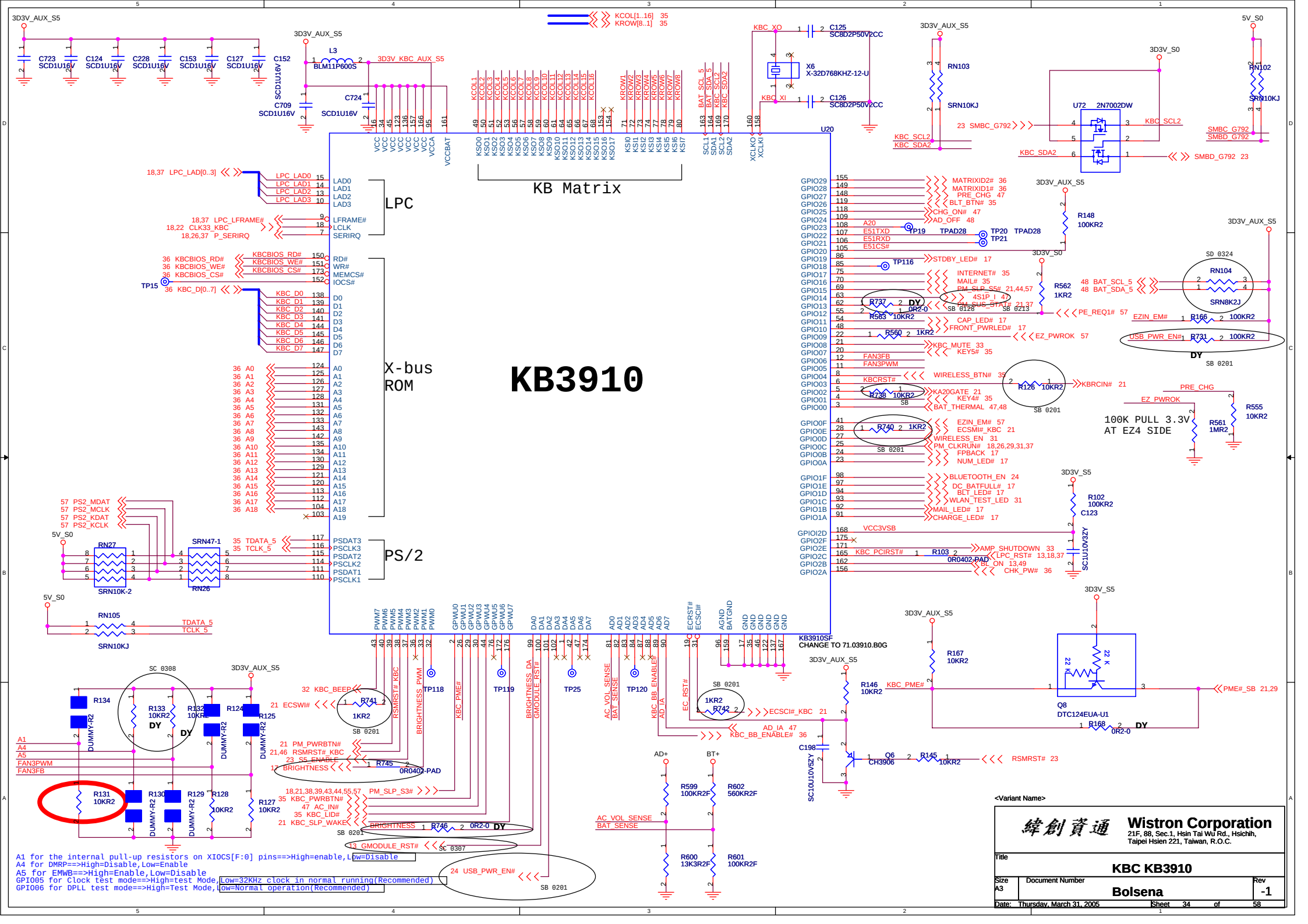


<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**MINI-PCI**	
Size A3	Document Number **Bolsena**	Rev -1
Date: Thursday, March 31, 2005	Sheet 31 of 58	


21 AC97_BITCLK_SB
R418 33R2
AC97_BITCLK_ALL
R416 0R2-0
3D3V_S0
U52
VCC
A
B
Y
GND
NC7SZ08-U
BITCLK_BUFF
AC97_RST#
24 AC97_BITCLK
R417 33R2
R419 10KR2
DY
SB 0219
33 VREFOUT1
5V_S0
U55
SHDN# SET
GND
IN
OUT
G923-330T1U-1
5VA_SET
5V_AUDIO_S0
C610 SC1U10V3KX
C611 SC22P50V2JN-1
R447 28K7R2F
R446 10KR2F-U
C613 SC10U10V5ZY
AUD_AGND
VREFOUT2
ADAF2
ADAF1
VREFOUT1
CODECVREF
C939 SCD1U
C940
C941
C943
C942
C944
C945
SC1000P50V2KX
SC1U10V3KX
SC10U10V5ZY
C614
C617
C616
C615
C602
U98
AFILT1
AFILT2
VRDA
VRAD
VREF
VREFOUT
FRONT-MIC
NC#33
NC#40
AVDD
VDD
AUX-L
AUX-R
JD2
JD1/GPIO1
SURR-OUT-L
SURR-OUT-R
LINE-L
LINE-R
FRONT-OUT-L
FRONT-OUT-R
MIC1
MIC2
XTL-IN
XTL-OUT
SPDIFO
SPDIF/EAPD
SDIN
SDOUT
JD0/GPIO0
XTLSEL
BITCLK
SYNC
RESET#
CD-L
CD-R
CD-GND
MONO-OUT-R
CEN-OUT
LFE-OUT
PC-BEEP
PHONE
AGND
GND
ALC655-U
XTALIN_CODEC
CLK14_AUDIO 3
0R0402-PAD
R689
R449
SPDIF_OUT
EAPD 33
SC 0308
SPDIF 33,57
EC5
C910
SC22P50V2JN
AC97_DATIN
R690 22R2
AC97_DIN0 21
AC97_DOUT 21,22,24
R450
AC97_CBITCLK
R415 33R2
R414 10KR2
BITCLK_BUFF
AC97_SYNC 21,24
AC97_RST# 21,24
XTSEL HI: USE 24.576M XTAL
XTSEL LOW: USE 14.318M CLK FROM CLK GEN
33 AUD_LINL
33 AUD_LINR
C920
C946
AUDLINL
AUDLINR
33 AUD_LOL
33 AUD_LOR
C937 SC1000P50V2KX
C938 SC1000P50V2KX
33 AUD_MICIN
C923 SC1U10V3ZY
AUD_MICIN1
25 CD_AUDL
25 CD_AGND
25 CD_AUDR
R700 75R2F
R451
GAP-CLOSE-PWR
R699 75R2F
CDAUDL
CDAGND
CDAUDR
C924 SC1U10V3KX
C925 SC1U10V3KX
C922 SC1U10V3KX
CDAUD_L
CDAUD_GND
CDAUD_R
R704 100KR2
R703 100KR2
R702 100KR2
AUD_PC_BEEP
C921 SCD1U
AUD_SYS_BEEP
C926 SC2200P50V2KX
R701 2K2R2
R691 4K7R2
R692 4K7R2
R693 4K7R2
C911 SC4D7U10V5ZY
C912 SC4D7U10V5ZY
C913 SC4D7U10V5ZY
CB_SPKR 26
SPKR_SB 21
KBC_BEEP 34
G105 GAP-CLOSE
G106 GAP-CLOSE
G107 GAP-CLOSE
G108 GAP-CLOSE
SC 0308
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO (1/2) -- CODEC ALC655
Size A3
Document Number
Bolsena
Rev -1
Date: Thursday, March 31, 2005
Sheet 32 of 58


Internal Speaker
SPK1
ETY-CON4-S
20.D0122.104
2ND : 20.D0012.104
ME : 20.D0122.104
2ND : 20.D0012.104
Dummy when no EZ4
LINE IN/MIC IN
Dummy when no EZ4
LIN1
AUDIO-JK30-U
22.10088.571
22.10271.011 - 2ND
ME : 22.10088.571
2ND : 22.10271.011
LINE OUT
SYS_LOUT_IN#=LOW after PLUG-IN
ME : 22.10133.561
2ND : 22.10257.001
2ND : 56.1549C.011
LOUT1
MINDIN10-1-U2
22.10257.001
1ST CHANGE TO 22.10147.031 - 22.10251.031 2ND
79.10711.4C1
79.10711.4C1
Dummy when 'USE EZ4'
Dummy when no EZ4
LEVEL SHIFT
close to diode
LOW OFF
Internal Mic
MIC1
CON2-10-U2
ME : 20.D0012.102
20.D0012.102
Dummy when no EZ4
U57
G1421BF3U
TSAHCT125
BAT54C-U
U56
RB731U
Q21
PDTA124EU
Q23
DTC124EUA-U1
Q22
DTC124EUA-U1
Q20
DTC124EUA-U1
D21
BAW56-1
By GMT suggest.
Change from
74.01421.01G
to 74.01421.A1G
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO (2/2)
Bolsena
Rev -1
Date: Thursday, March 31, 2005
Sheet 33 of 58


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
U20
KB3910SF
CHANGE TO 71.03910.B0G
100K PULL 3.3V AT EZ4 SIDE
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC KB3910
Size A3
Document Number
Bolsena
Rev -1
Date: Thursday, March 31, 2005
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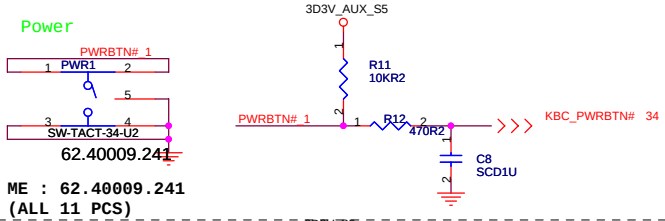
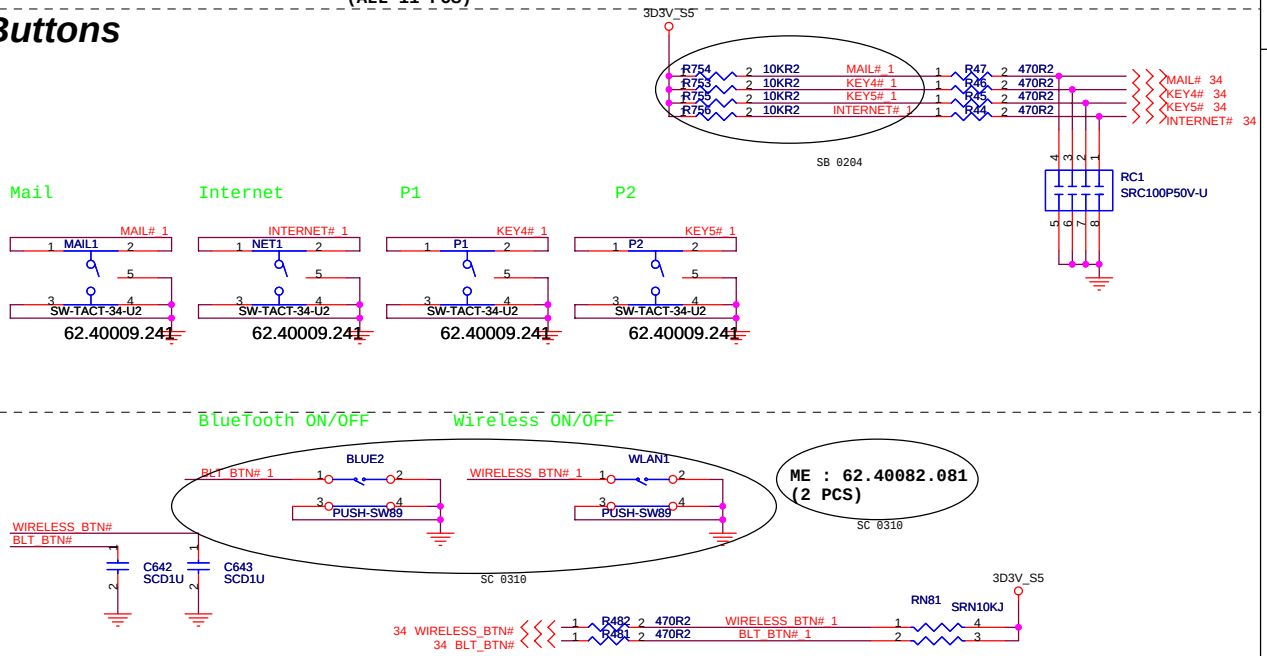
POWER BUTTON

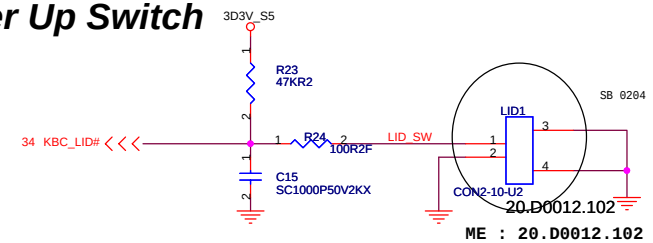


ME : 62.40009.241
(ALL 11 PCS)

Buttons

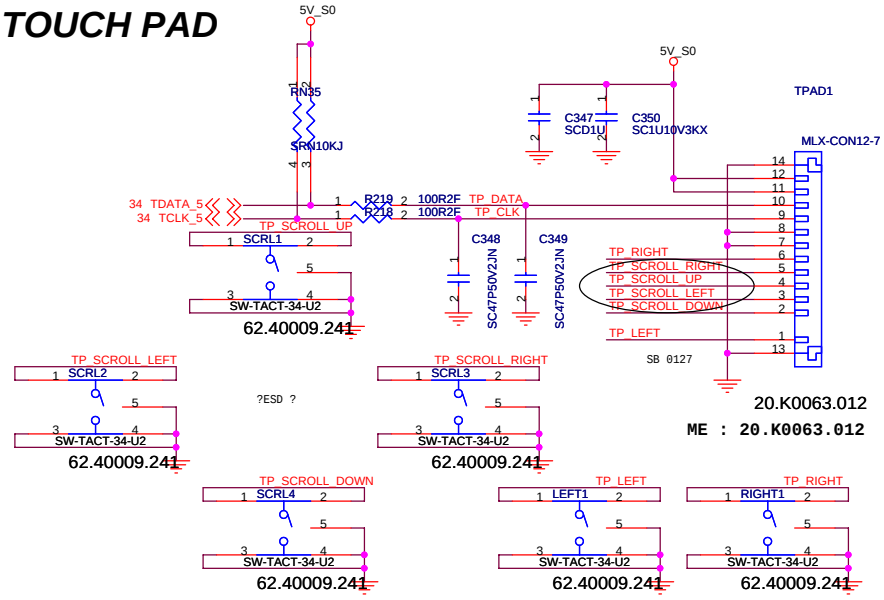


Cover Up Switch



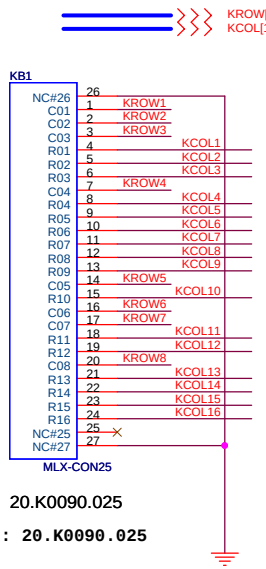
ME : 20.D0012.102

TOUCH PAD



ME : 20.K0063.012

Internal KeyBoard CONN

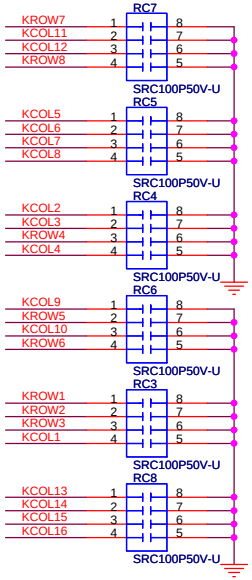


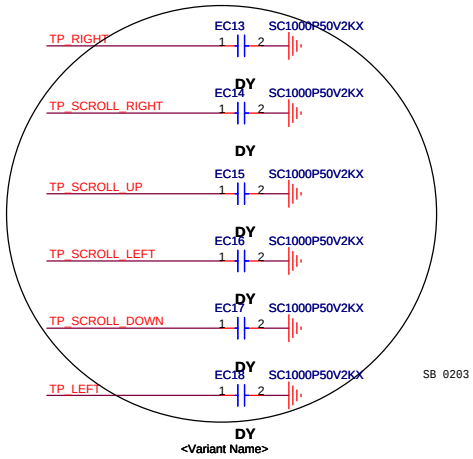
20.K0090.025

ME : 20.K0090.025

Pin1 ==>*R01
Pin2 ==>*R02
Pin3 ==>*R03
Pin4 ==> C01
Pin5 ==> C02
Pin6 ==> C03
Pin7 ==>*R04
Pin8 ==> C04
Pin9 ==> C05
Pin10 ==> C06
Pin11 ==> C07
Pin12 ==> C08
Pin13 ==> C09
Pin14 ==>*R05
Pin15 ==> C10
Pin16 ==>*R06
Pin17 ==>*R07
Pin18 ==> C11
Pin19 ==> C12
Pin20 ==>*R08
Pin21 ==> C13
Pin22 ==> C14
Pin23 ==> C15
Pin24 ==> C16
Pin25 ==> NC

EMI Bypass cap.



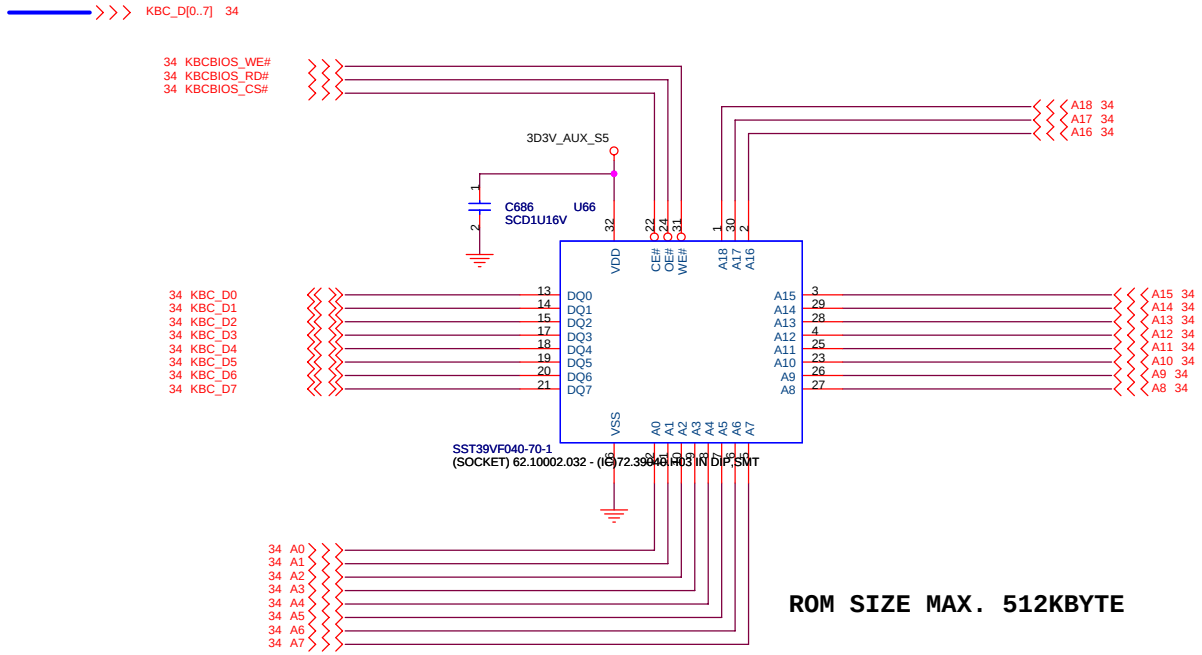


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BUTTONs / KB / TOUCHPAD

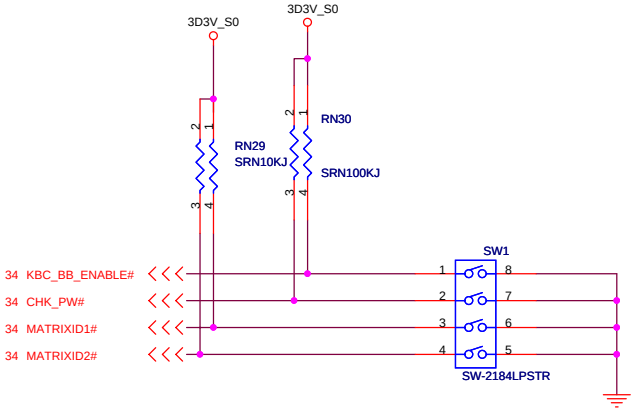
Size	Document Number	Rev
A3	Bolsena	-1

Date: Thursday, March 31, 2005 Sheet 35 of 58



ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032



Keyboard matrix (from vendor)

		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0

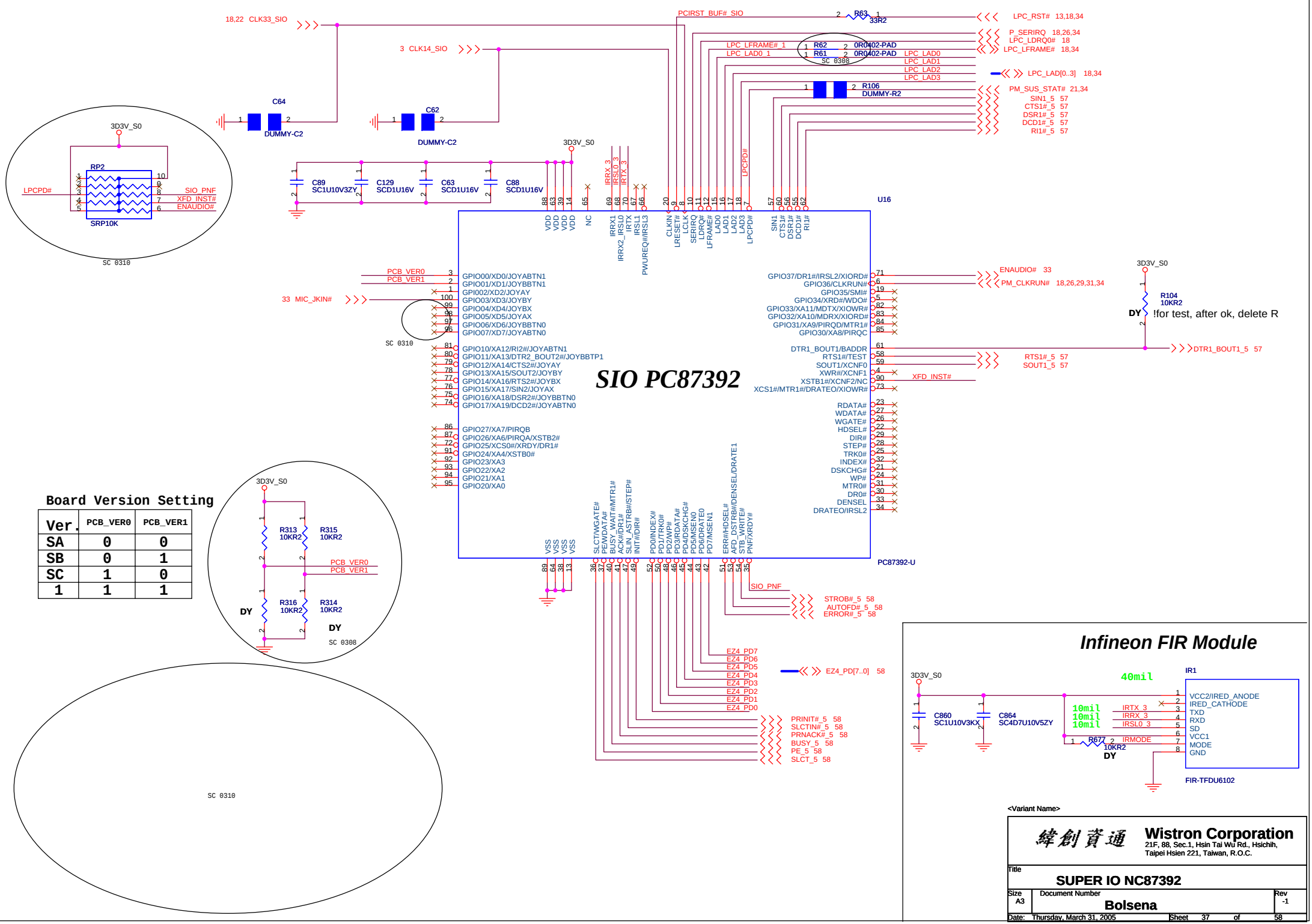
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS ROM**

Size: A3 | Document Number: **Bolsena** | Rev: -1

Date: Thursday, March 31, 2005 | Sheet 36 of 58


SIO PC87392
PC87392-U
U16
Board Version Setting
Ver. | PCB_VER0 | PCB_VER1
SA | 0 | 0
SB | 0 | 1
SC | 1 | 0
1 | 1 | 1
Infineon FIR Module
FIR-TFDU6102
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SUPER IO NC87392
Bolsena
Thursday, March 31, 2005
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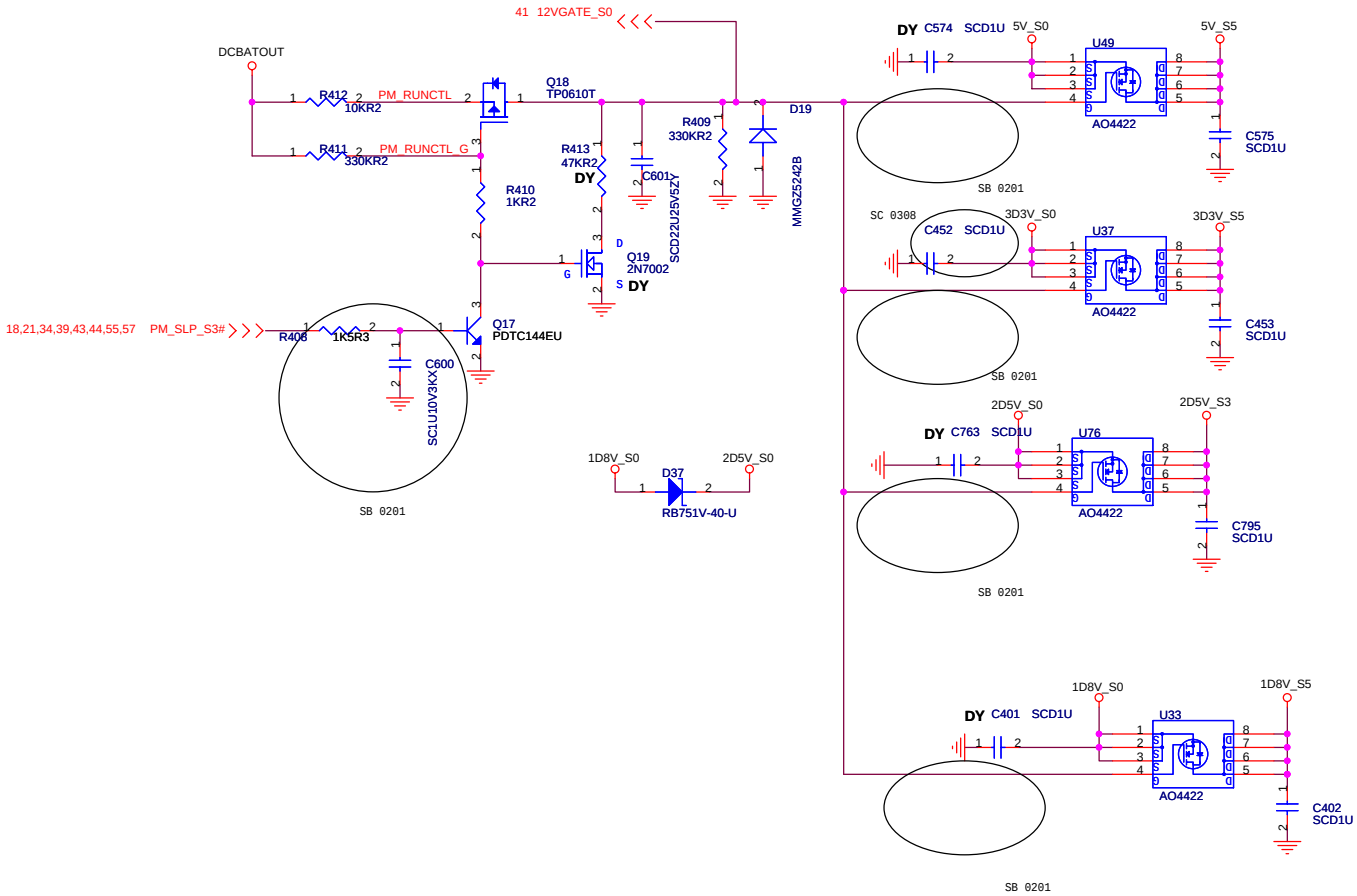
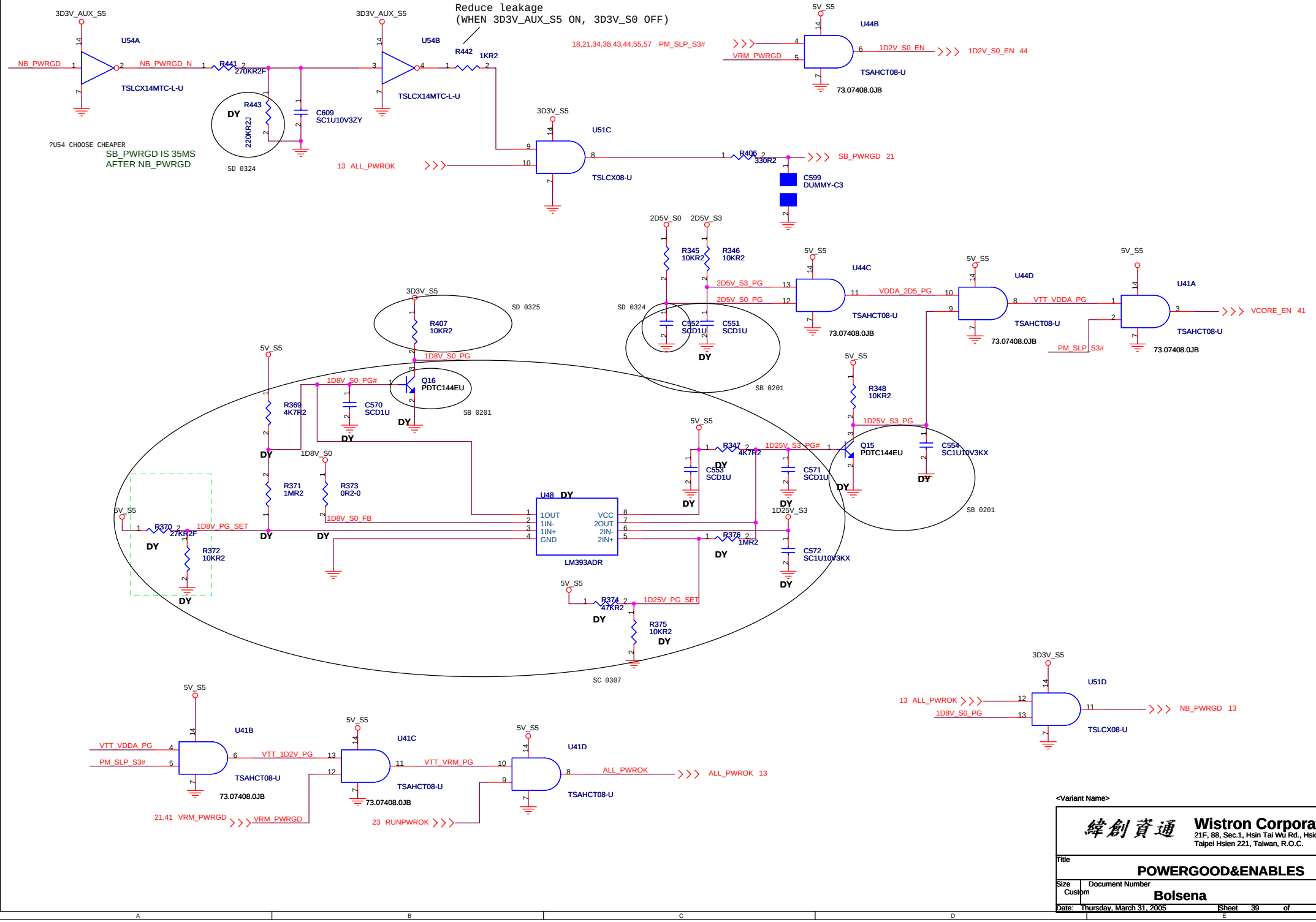
for test, after ok, delete R

Run Power



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**PWR CTL LOGIC / PWR PLANE**
Size: A3	Document Number: **Bolsena**
Rev: -1	
Date: Thursday, March 31, 2005	Sheet 38 of 58



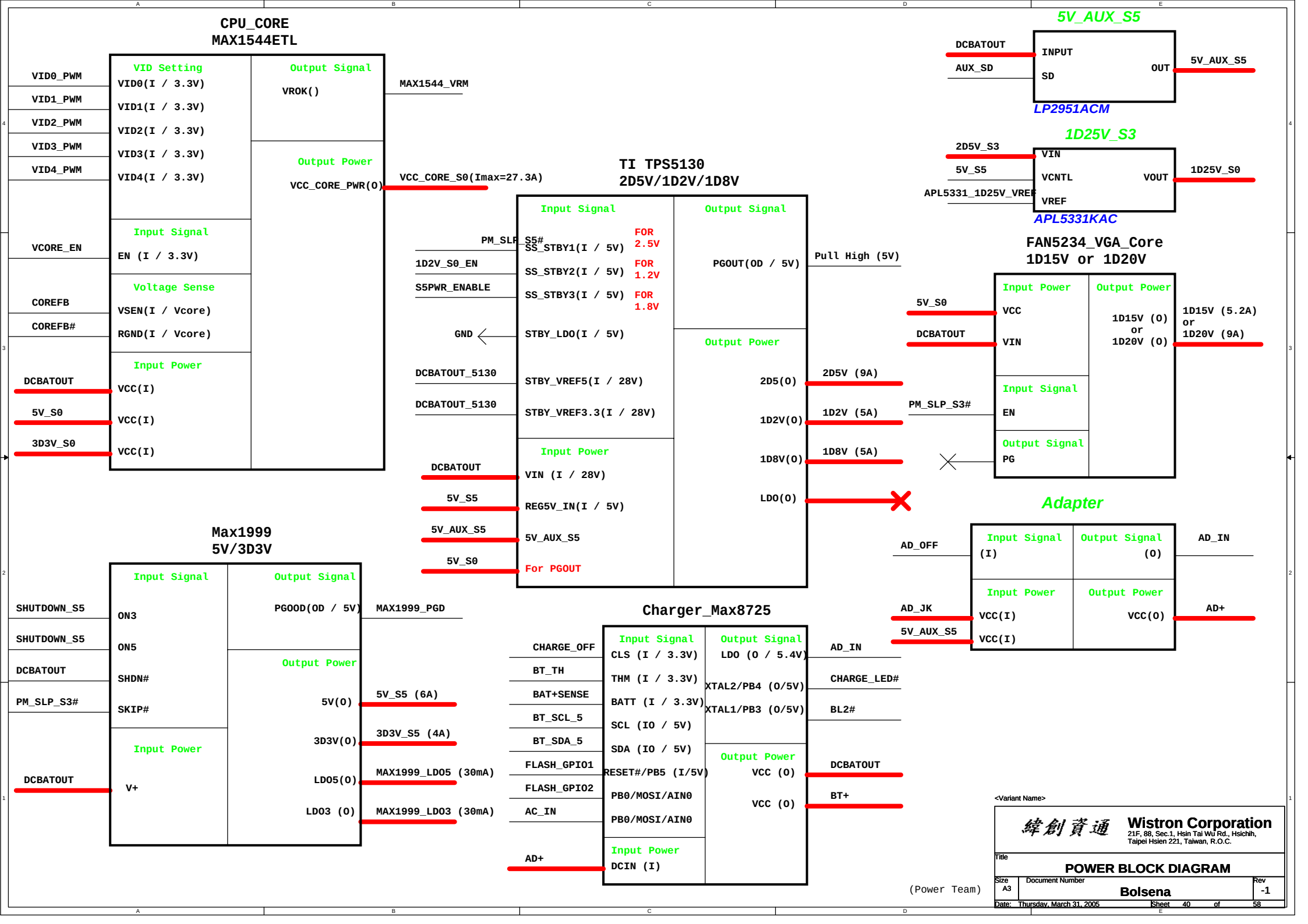
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWERGOOD&ENABLES

Size: Custom | Document Number: Bolsena | Rev: -1

Date: Thursday, March 31, 2005 | Sheet 39 of 58


CPU_CORE
MAX1544ETL
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
Output Signal
VROK()
Output Power
VCC_CORE_PWR(O)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
VID0_PWM
VID1_PWM
VID2_PWM
VID3_PWM
VID4_PWM
VCORE_EN
COREFB
COREFB#
DCBATOUT
5V_S0
3D3V_S0
MAX1544_VRM
VCC_CORE_S0(Imax=27.3A)
5V_AUX_S5
DCBATOUT
AUX_SD
INPUT
SD
OUT
5V_AUX_S5
LP2951ACM
1D25V_S3
2D5V_S3
5V_S5
APL5331_1D25V_VREF
VIN
VCNTL
VREF
VOUT
1D25V_S0
APL5331KAC
TI TPS5130
2D5V/1D2V/1D8V
Input Signal
SS_STBY1(I / 5V) FOR 2.5V
SS_STBY2(I / 5V) FOR 1.2V
SS_STBY3(I / 5V) FOR 1.8V
STBY_LDO(I / 5V)
STBY_VREF5(I / 28V)
STBY_VREF3.3(I / 28V)
Input Power
VIN (I / 28V)
REG5V_IN(I / 5V)
5V_AUX_S5
For PGOUT
Output Signal
PGOUT(OD / 5V)
Output Power
2D5(O)
1D2V(O)
1D8V(O)
LDO(O)
PM_SLP_S5#
1D2V_S0_EN
S5PWR_ENABLE
GND
DCBATOUT_5130
DCBATOUT_5130
DCBATOUT
5V_S5
5V_AUX_S5
5V_S0
Pull High (5V)
2D5V (9A)
1D2V (5A)
1D8V (5A)
FAN5234_VGA_Core
1D15V or 1D20V
Input Power
VCC
VIN
Input Signal
EN
Output Signal
PG
Output Power
1D15V (O)
or
1D20V (O)
5V_S0
DCBATOUT
PM_SLP_S3#
1D15V (5.2A)
or
1D20V (9A)
Adapter
Input Signal
(I)
Output Signal
(O)
Input Power
VCC(I)
VCC(I)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN
AD+
Max1999
5V/3D3V
Input Signal
ON3
ON5
SHDN#
SKIP#
Input Power
V+
Output Signal
PGOOD(OD / 5V)
Output Power
5V(O)
3D3V(O)
LDO5(O)
LDO3 (O)
SHUTDOWN_S5
SHUTDOWN_S5
DCBATOUT
PM_SLP_S3#
DCBATOUT
MAX1999_PGD
5V_S5 (6A)
3D3V_S5 (4A)
MAX1999_LDO5 (30mA)
MAX1999_LDO3 (30mA)
Charger_Max8725
Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0
Input Power
DCIN (I)
Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)
Output Power
VCC (O)
VCC (O)
CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN
AD+
AD_IN
CHARGE_LED#
BL2#
DCBATOUT
BT+
(Power Team)
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
POWER BLOCK DIAGRAM
Size A3
Document Number
Bolsena
Rev -1
Date: Thursday, March 31, 2005
Sheet 40 of 58

CPU_VCORE
VID=1.20V
Iomax=27.3A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

TON:	Frequency:
GND	550KHz
REF	300KHz
OPEN	200KHz
VCC	100KHz

For Dummy Phase 2

For alone test==>short C395 pin1 and pin2

SC:
1. Change R246 and R228 to 511R3F(64.51105.651).
2. Change R224 to 26K7R2F(64.26725.6D1).
3. Cut off a trace between pin7 and pin8 of U29.

VCC_CORE_S0 feedback

From KBC

(Power Team)

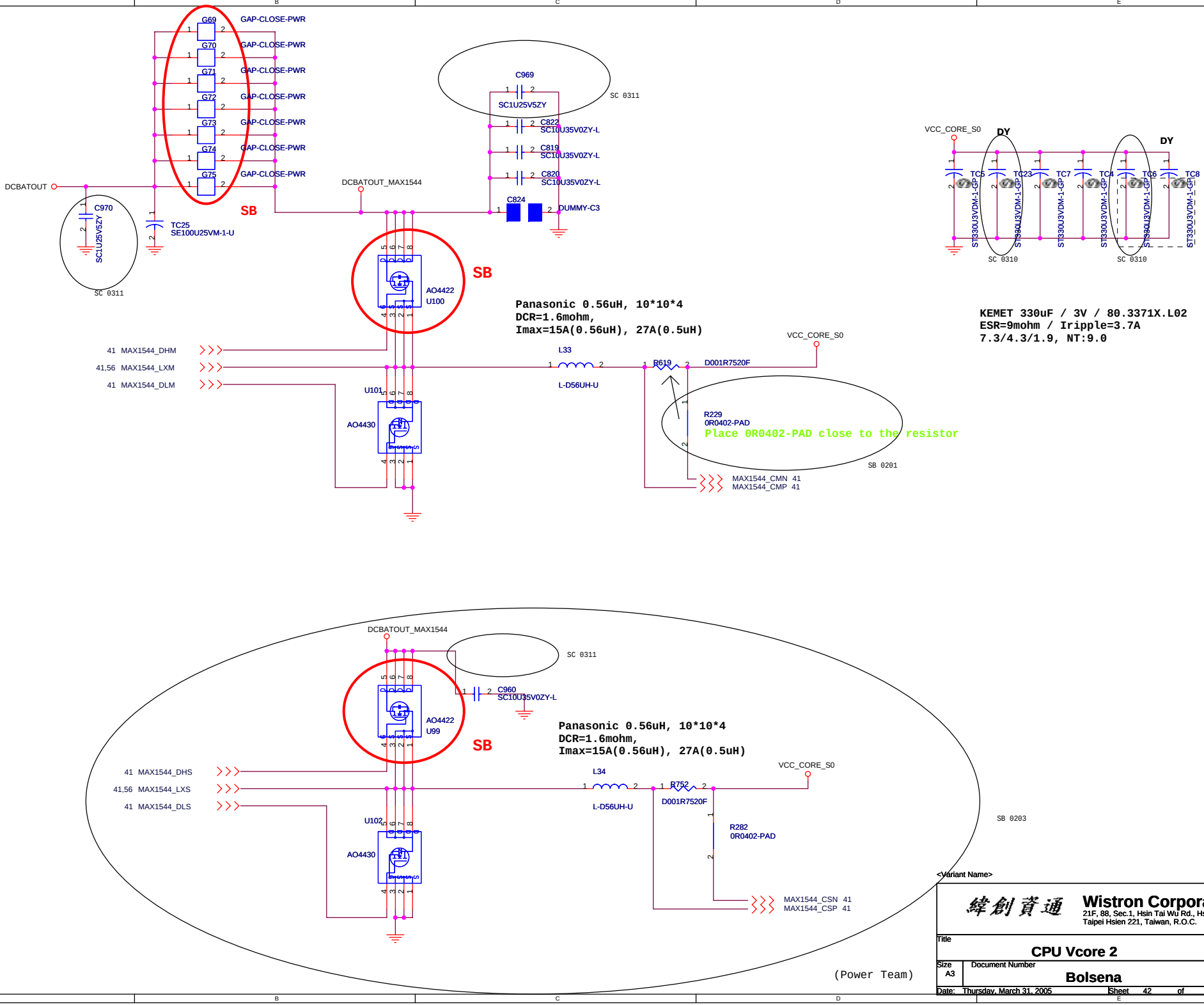
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

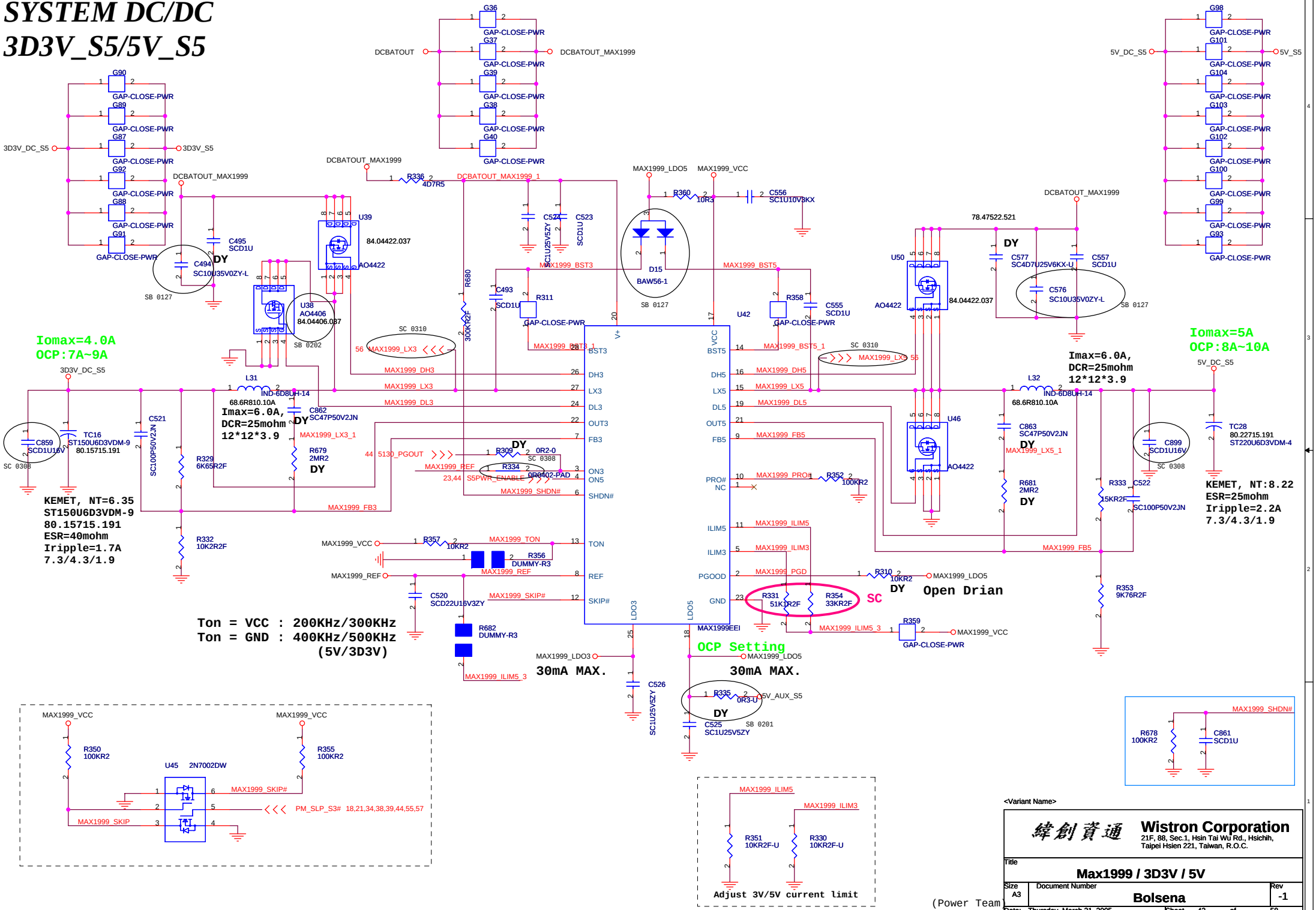
Title: CPU Vcore 1

Size: A3 | Document Number: Bolsena | Rev: -1

Date: Thursday, March 31, 2005 | Sheet 41 of 58


G69 GAP-CLOSE-PWR
G70 GAP-CLOSE-PWR
G71 GAP-CLOSE-PWR
G72 GAP-CLOSE-PWR
G73 GAP-CLOSE-PWR
G74 GAP-CLOSE-PWR
G75 GAP-CLOSE-PWR
SB
DCBATOUT
C970
SC1U25V5ZY
SC 0311
TC25
SE100U25VM-1-U
DCBATOUT_MAX1544
C969
SC1U25V5ZY
SC 0311
C822
SC10U35V0ZY-L
C819
SC10U35V0ZY-L
C820
SC10U35V0ZY-L
C824
DUMMY-C3
SB
AO4422
U100
Panasonic 0.56uH, 10*10*4
DCR=1.6mohm,
Imax=15A(0.56uH), 27A(0.5uH)
41 MAX1544_DHM
41,56 MAX1544_LXM
41 MAX1544_DLM
U101
AO4430
L33
L-D56UH-U
R619
D001R7520F
VCC_CORE_S0
R229
0R0402-PAD
Place 0R0402-PAD close to the resistor
SB 0201
MAX1544_CMN 41
MAX1544_CMP 41
VCC_CORE_S0
DY
DY
TC5
TC23
TC7
TC4
TC6
TC8
ST330U3VDM-1-GP
SC 0310
SC 0310
KEMET 330uF / 3V / 80.3371X.L02
ESR=9mohm / Iripple=3.7A
7.3/4.3/1.9, NT:9.0
DCBATOUT_MAX1544
SC 0311
C960
SC10U35V0ZY-L
AO4422
U99
SB
Panasonic 0.56uH, 10*10*4
DCR=1.6mohm,
Imax=15A(0.56uH), 27A(0.5uH)
41 MAX1544_DHS
41,56 MAX1544_LXS
41 MAX1544_DLS
U102
AO4430
L34
L-D56UH-U
R752
D001R7520F
VCC_CORE_S0
R282
0R0402-PAD
SB 0203
MAX1544_CSN 41
MAX1544_CSP 41
(Power Team)
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU Vcore 2
Size
A3
Document Number
Bolsena
Rev
-1
Date: Thursday, March 31, 2005
Sheet 42 of 58

SYSTEM DC/DC
3D3V_S5/5V_S5



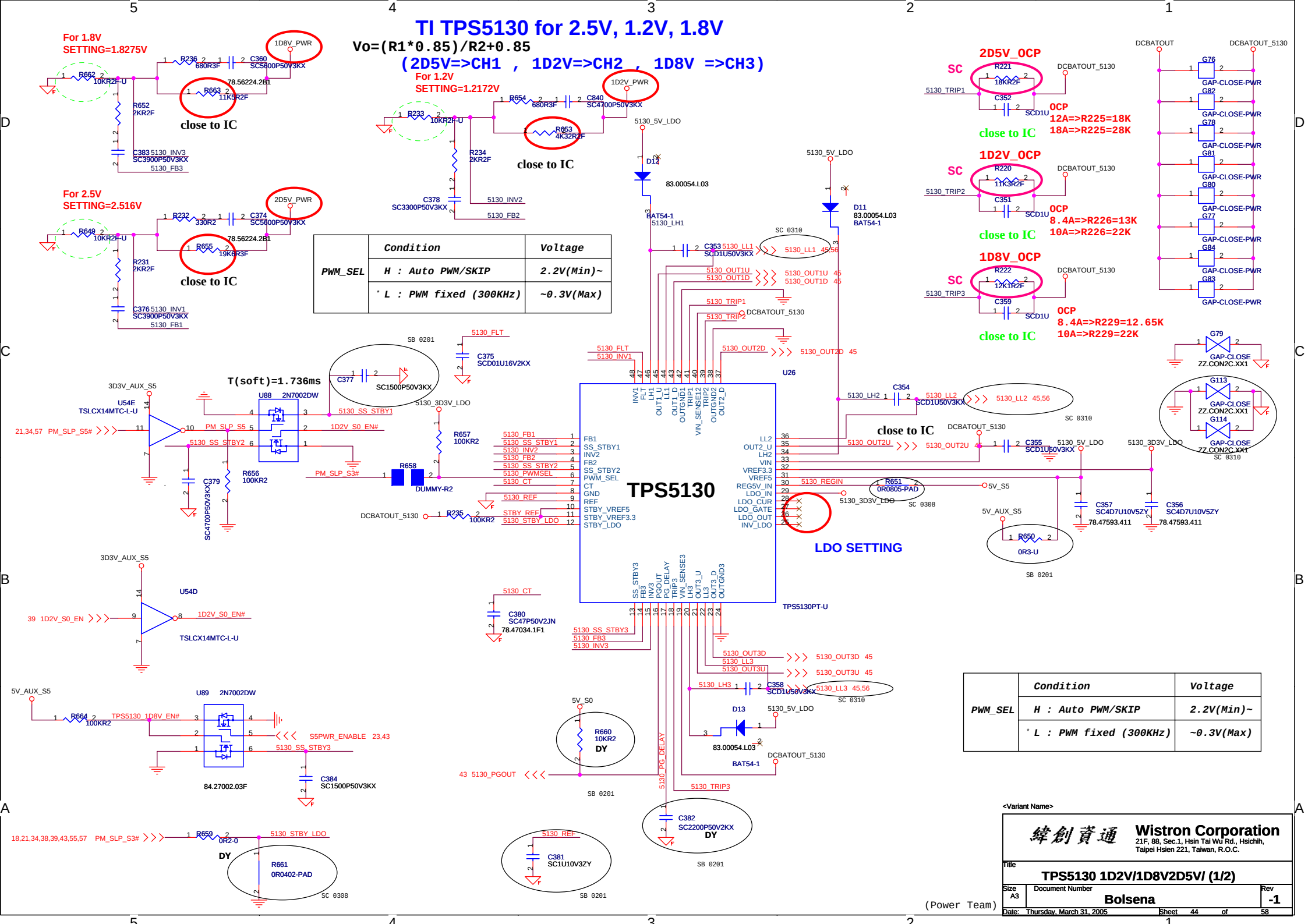
<variant_name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Max1999 / 3D3V / 5V**	
Size: A3	Document Number: **Bolsena**	Rev: -1
Date: Thursday, March 31, 2005	Sheet 43 of 58	

TI TPS5130 for 2.5V, 1.2V, 1.8V

Vo=(R1*0.85)/R2+0.85

(2D5V=>CH1 , 1D2V=>CH2 , 1D8V =>CH3)



PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS5130 1D2V/1D8V2D5V/ (1/2)

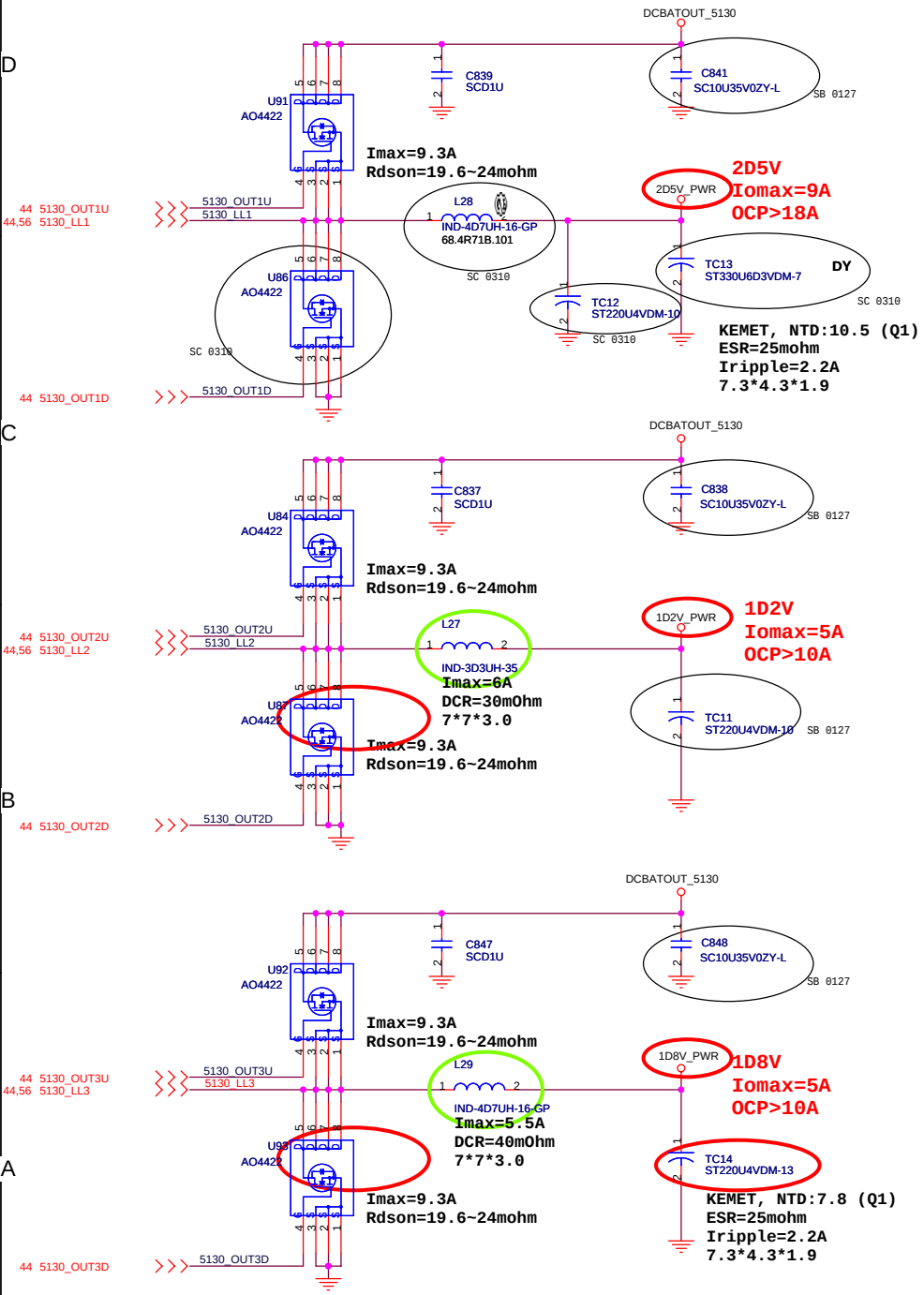
Size: A3 | Document Number: Bolsena | Rev: -1

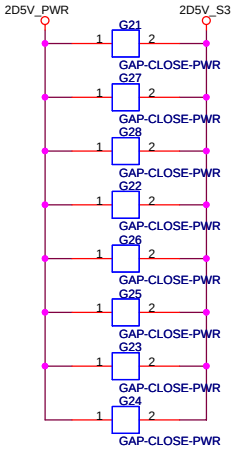
Date: Thursday, March 31, 2005 | Sheet 44 of 58

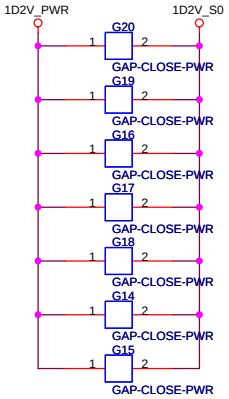
(Power Team)

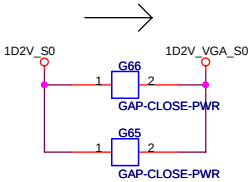
TI TPS5130 for 2D5V, 1D2V, 1D8V

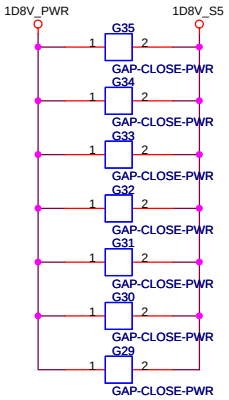
(2D5V=>CH1 , 1D2V=>CH2 , 1D8V =>CH3)











(Power Team)

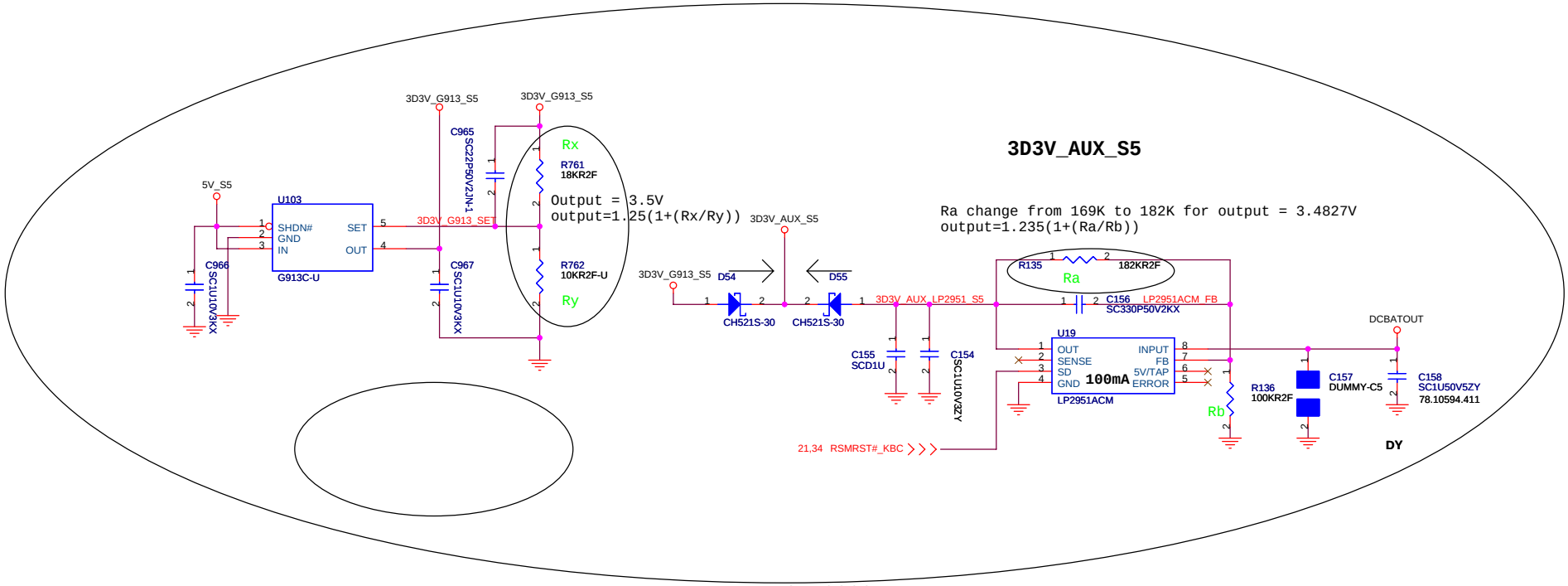
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

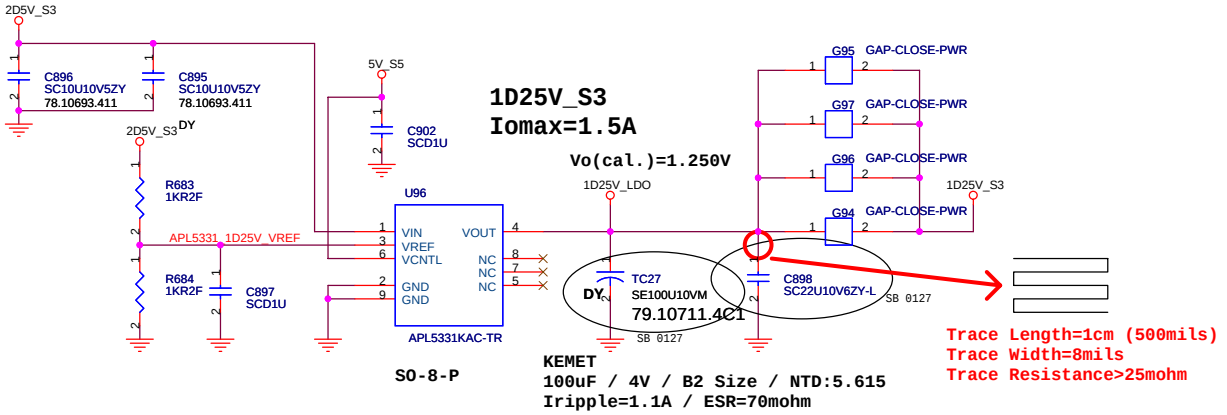
Title: **TPS5130 1D2V/1D8V2D5V/ (2/2)**

Size	Document Number	Rev
A3	**Bolsena**	-1

Date: Thursday, March 31, 2005 Sheet 45 of 58



SD 0303



(Power Team)

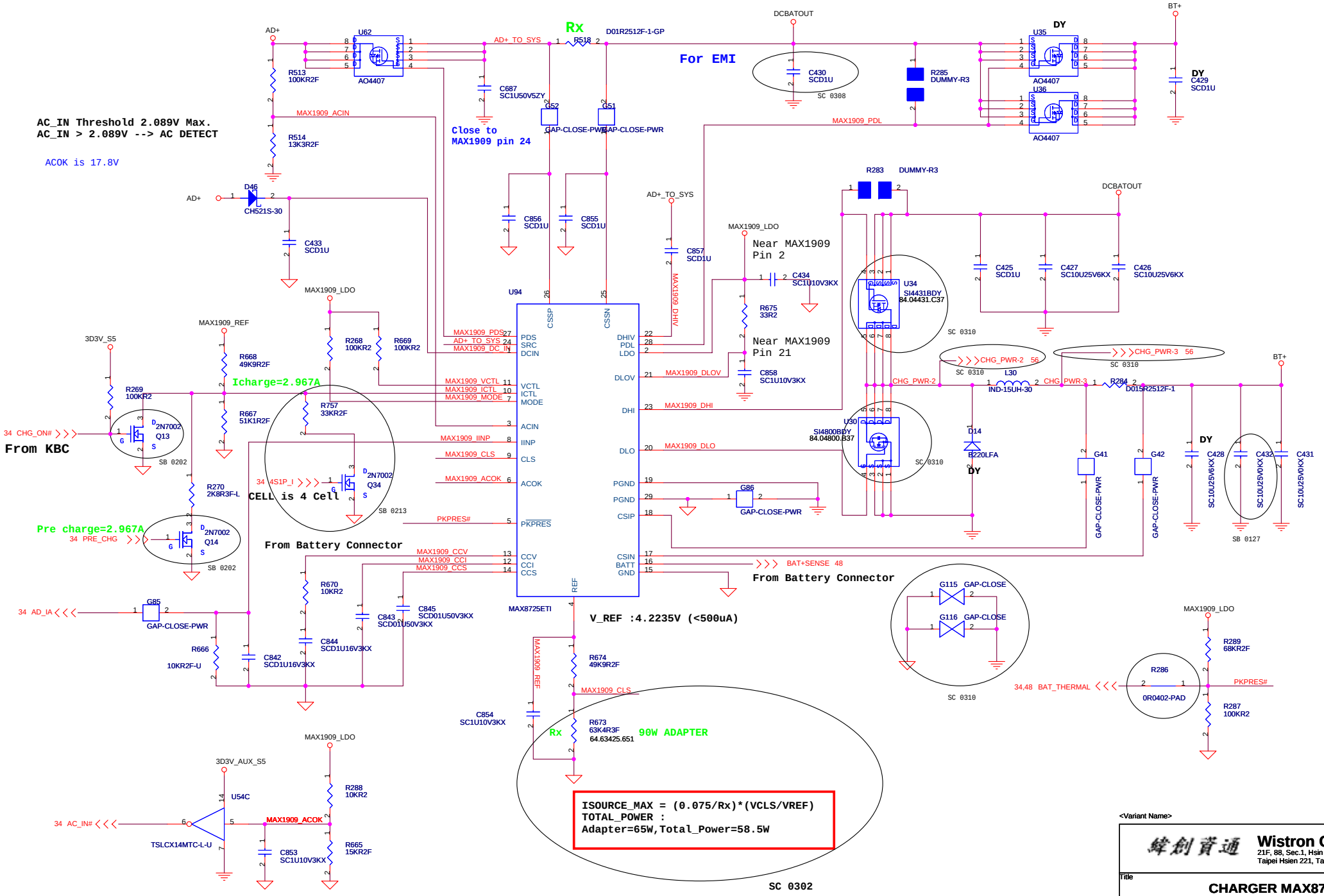
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D2V_S3 / 3D3V_AUX

Size	Document Number	Rev
A3	Bolsena	-1

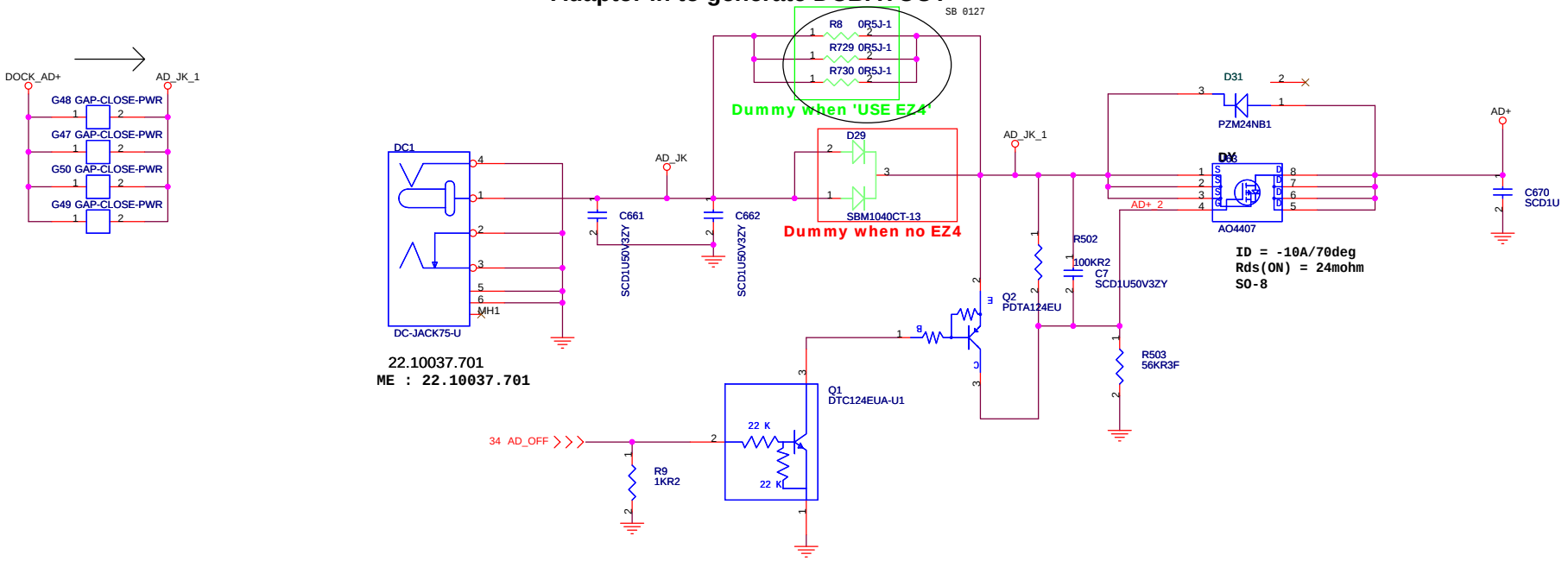
Date: Thursday, March 31, 2005 Sheet 46 of 58



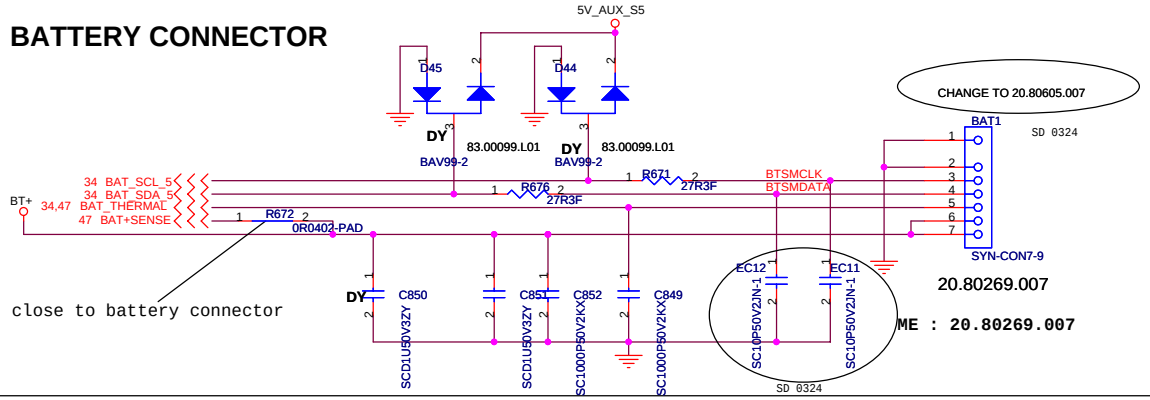
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>
Title: CHARGER MAX8725
Size: Custom | Document Number: Bolsena | Rev: -1
Date: Thursday, March 31, 2005 | Sheet 47 of 58
(Power Team)

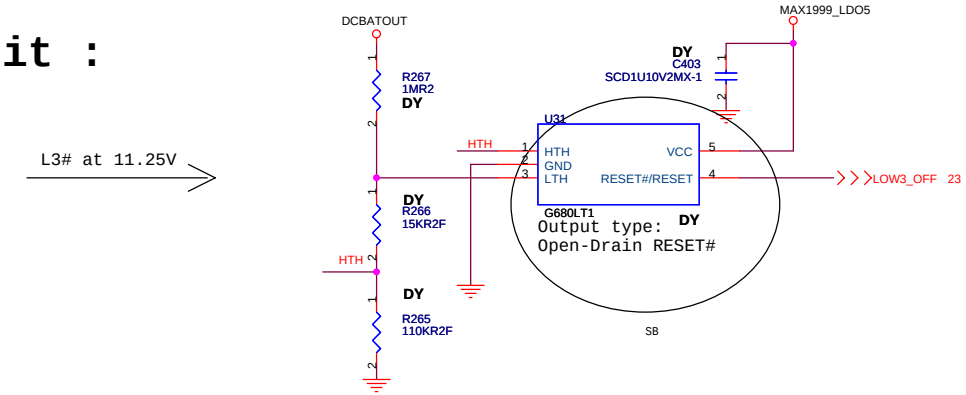
Adaptor in to generate DCBATOUT

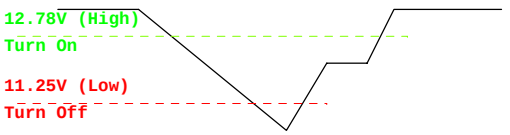


BATTERY CONNECTOR



Low3 Circuit :





<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size A3	Document Number Bolsena	Rev -1
Date: Thursday, March 31, 2005	Sheet 48 of 58	

Dummy when use UMA (WHOLE PAGE)

U14
P2779A-08ST
71.02779.00A
ORIGNAL
P2779A-08TT
USE W180-01
GEOMETRY

adjust SWING at 1.2v

U70A

Part 1 of 6

PCI EXPRESS

DVO / EXT TMDS / GPIO

LVDS

TMDS

DAC2

DAC1

CLK $S

THERM

MUST TO CHECK

DVOMODE=VSS	3.3V MODE
DVOMODE=VDDC to 1.8V	1.8V MODE
DVOMODE=GND	NO USE DVPDATA

STRAPS	PIN	DEFAULT
CAL_BG_BACKUP	GPIO0	1
PLL_CAL_FORCE_EN	GPIO1	1
PCIE_MODE(1:0)	GPIO(3:2)	00
CAL_OFF	GPIO4	1
BYPASS_PLL	GPIO5	0
ICOMP	GPIO6	0
DEBUG_ACCESS	GPIO8	0
ROMIDCFG(3:0)	GPIO(9,13:11)	0000
MULTIFUNC(1:0)	LCDDATA(17:16)	00
VIP_DEVICE	LCDDATA(20)	0
DWNGR0	LCDDATA(21) (internal pull-down)	0

M26 : HYNIX 128MB 1.8V,64MB 1.8V
M24 : HYNIX 64MB 1.8V

ATI Ref. Datasheets(page 3-32)
DOC.NO.:CHS-216M24-03
GPIO[0..13] are internal pull-down.

DVPDATA 2, 1, 0		
0 0 0	64MB Hynix	FOR M24
0 0 1	64MB Samsung	
0 1 0	64MB X brand	
0 1 1	64MB Y brand	
1 0 0	128MB Hynix	FOR M26
1 0 1	128MB Samsung	
1 1 0	128MB X brand	
1 1 1	128MB Y brand	

The PERSTB must deplay 4ms from M24 bug.

Place Near To EZPORT4

Dummy when use "M24"

M26-P-1
(M24)71.00M24.C0U - (M26)71.0M26P.00U

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M26 PCIE LVDS (1/3)

Size: A3 | Document Number: Bolsena | Rev: 1

Date: Thursday, March 31, 2005 | Sheet 49 of 58

Dummy when use UMA (WHOLE PAGE)

current of power to VDDC on M26 is up to 10A + margin (25% or more).

U70D

Part 4 of 6

I/O POWER

PCIE_VDDR_12
1.6A + margin (transition, 4us duration) and
1.1A + margin (continuous).

PCIE_PVDD_12
150mA + margin (transition, 4us duration) and
90mA + margin (continuous).

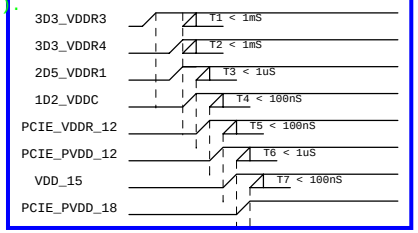
PCIE_PVDDR_18
800mA + margin (transition, 4us duration) and
330mA + margin (continuous).

DIODE SUPPLIES POWER TO VDDC RAIL WHILE VDDC REGULATOR STABALIZES DURING POWER ON

DIODE SUPPLIES POWER TO VDDC RAIL WHILE VDDC REGULATOR STABALIZES DURING POWER ON

CHANGE TO 74.05308.E31

M22 Power UP Squence



ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED PLACED CLOSE TO THE POWER/GND PINS WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC

M26-P-1
(M24)71.00M24.C0U - (M26)71.0M26P.00U

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M26 POWER (2/3)

Size: A3 | Document Number: Bolsena | Rev: -1

Date: Thursday, March 31, 2005 | Sheet 50 of 58

Dummy when use UMA (WHOLE PAGE)

52 MDA[63..0]

U70B — Part 2 of 6 — MEMORY INTERFACE A

MDA0 H28 … MDA63 F8 → DQA0 … DQA63

MAA0 E22 … MAA13 C19 → MAA[13..0] 52

DQMA#0 J25 … DQMA#7 E11 → DQMA[7..0] 52

QSA0 J27 … QSA7 F10 → QSA[7..0] 52

RASA# A19 → RASA# 52

CASA# E18 → CASA# 52

WEA# E19 → WEA# 52

CSA0# E20 → CSA#0 52

CSA1# F20 → CSA#1 52

CKEA B19 → CKEA 52

CLKA0 B21 / CLKA0# C20 → CLKA0 52 / CLKA0# 52

CLKA1 C18 / CLKA1# A18 → CLKA1 52 / CLKA1# 52

MVREFD B7 — ATI_MVREFD

MVREFS B8 — ATI_MVREFS

DIMA_0 D30 — DIMA_1 B13

M26-P-1
(M24)71.00M24.C0U - (M26)71.0M26P.00U

MEMORY CHANNEL A

M22,24,26P
:Not
connected

CKEA — R90 10KR2 — 1D8V_S0

CKEB — R78 10KR2 — 1D8V_S0

SB 0201

R70 100R2F

R71 100R2F

C73 SCD1U16V

R68 100R2F

R89 100R2F

C91 SCD1U16V

TP16 TP12

As close to
CHIP as
possible

53 MDB[63..0]

U70C — Part 3 of 6 — MEMORY INTERFACE B

MDB0 D7 … MDB63 AE3 → DQB0 … DQB63

MAB0 N5 … MAB13 P2 → MAB[13..0] 53

DQMB#0 E6 … DQMB#7 AD2 → DQMB[7..0] 53

QSB0 F6 … QSB7 AD1 → QSB[7..0] 53

RASB# R2 → RASB# 53

CASB# T5 → CASB# 53

WEB# T6 → WEB# 53

CSB0# R5 → CSB#0 53

CSB1# R6 — CSB#1 → CSB#1 53

CKEB R3 → CKEB 53

CLKB0 N1 / CLKB0# N2 → CLKB0 53 / CLKB0# 53

CLKB1 T2 / CLKB1# T3 → CLKB1 53 / CLKB1# 53

DIMB_0 E3 — DIMB_1 AA3

TP3 TP4 TPAD30

M22,24,26P
:Not
connected

ROMCS# AE5 — TP7 TPAD30

MEMVMODE_0 C6

MEMVMODE_1 C7

MEMTEST C8

R74 10KR2 DY

R73 10KR2

R72 10KR2 DY

R75 45R2F

R51 10KR2

R76 240R2F

M26-P-1
(M24)71.00M24.C0U - (M26)71.0M26P.00U

MEMORY CHANNEL B

M24 use 45ohm 1%

M26 use 240ohm 1%

Dummy when use "M24"

Dummy when use "M26"

*When use M26, pin C6 = GPIO_17, C7 = NC

When use M22/24P

PIN	C6	C7
1.8V =	PD	PU
2.5V =	PU	PD

VGA_CORE_S0

U70F — Part 6 of 6 — CENTER ARRAY

VDDC#P17 … VDDC#W19 → VSS#M16 … VSS#T16

VDDC1#W16 … VDDC1#T12

M26-P-1
(M24)71.00M24.C0U - (M26)71.0M26P.00U

VGA_CORE_S0 — R91 0R0603-PAD — VGA_CORE_VDDCI

SC 0308

C108 SC330P50V2KX

1D8V_S0

U70E — Part 5 of 6 — CORE GND

VSS#U4 … VSS#AH29 → PCIE_VSS#K28 … PCIE_VSS#AH29

VSS#A2 … VSS#T1

MVDDQ=
1.8v/ 2.5v

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

SB 0127

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

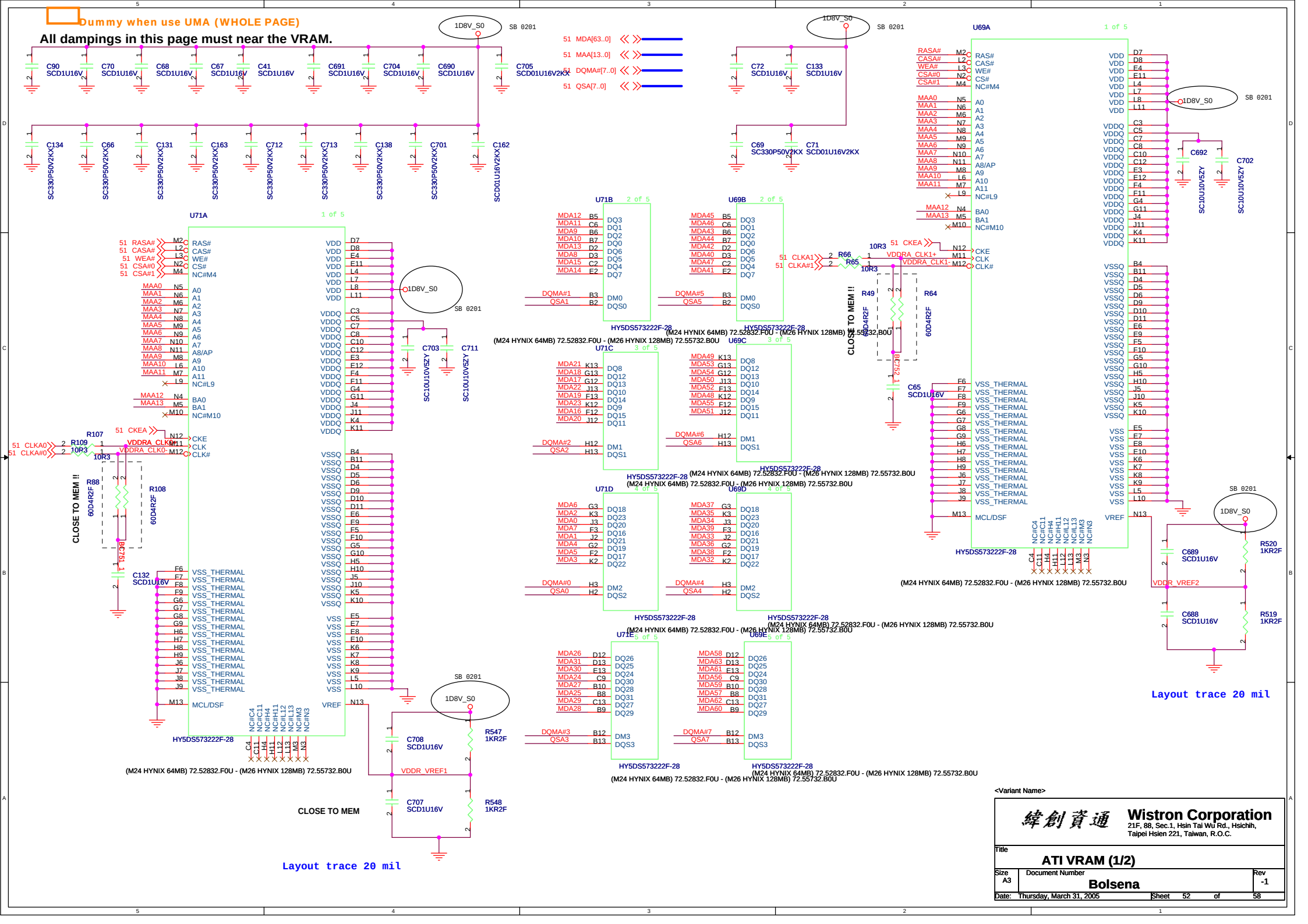
Title: ATI M26 MEM (3/3)

Size: A3 | Document Number: Bolsena | Rev: -1

Date: Thursday, March 31, 2005 | Sheet 51 of 58

Dummy when use UMA (WHOLE PAGE)

All dampings in this page must near the VRAM.



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

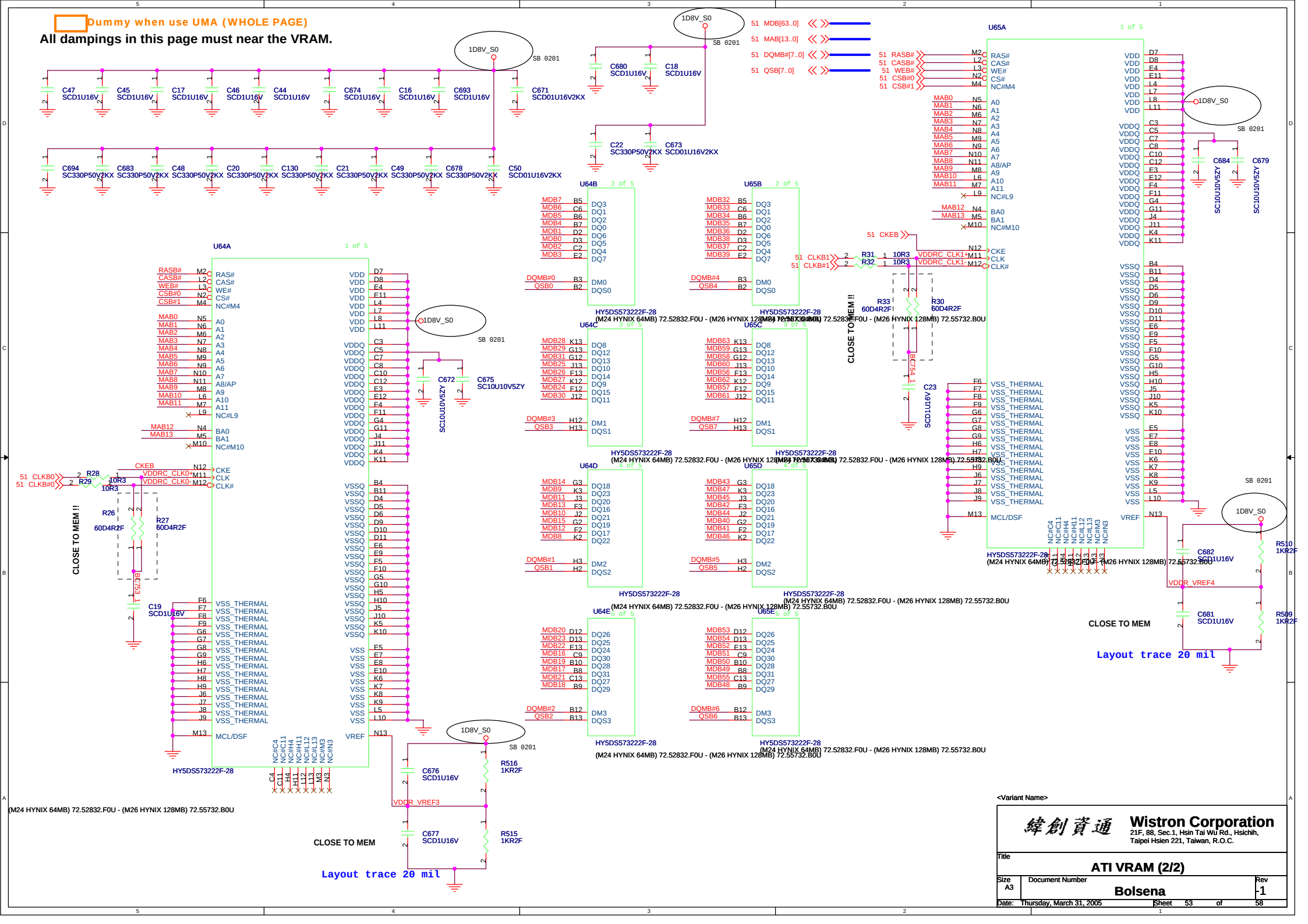
Title: **ATI VRAM (1/2)**

Size	Document Number	Rev
A3	**Bolsena**	-1

Date: Thursday, March 31, 2005 Sheet 52 of 58

Dummy when use UMA (WHOLE PAGE)

All dampings in this page must near the VRAM.



(M24 HYNIX 64MB) 72.52832.F0U - (M26 HYNIX 128MB) 72.55732.B0U

<Variant Name>

緯創資通 **Wistron Corporation**

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Title	ATI VRAM (2/2)	
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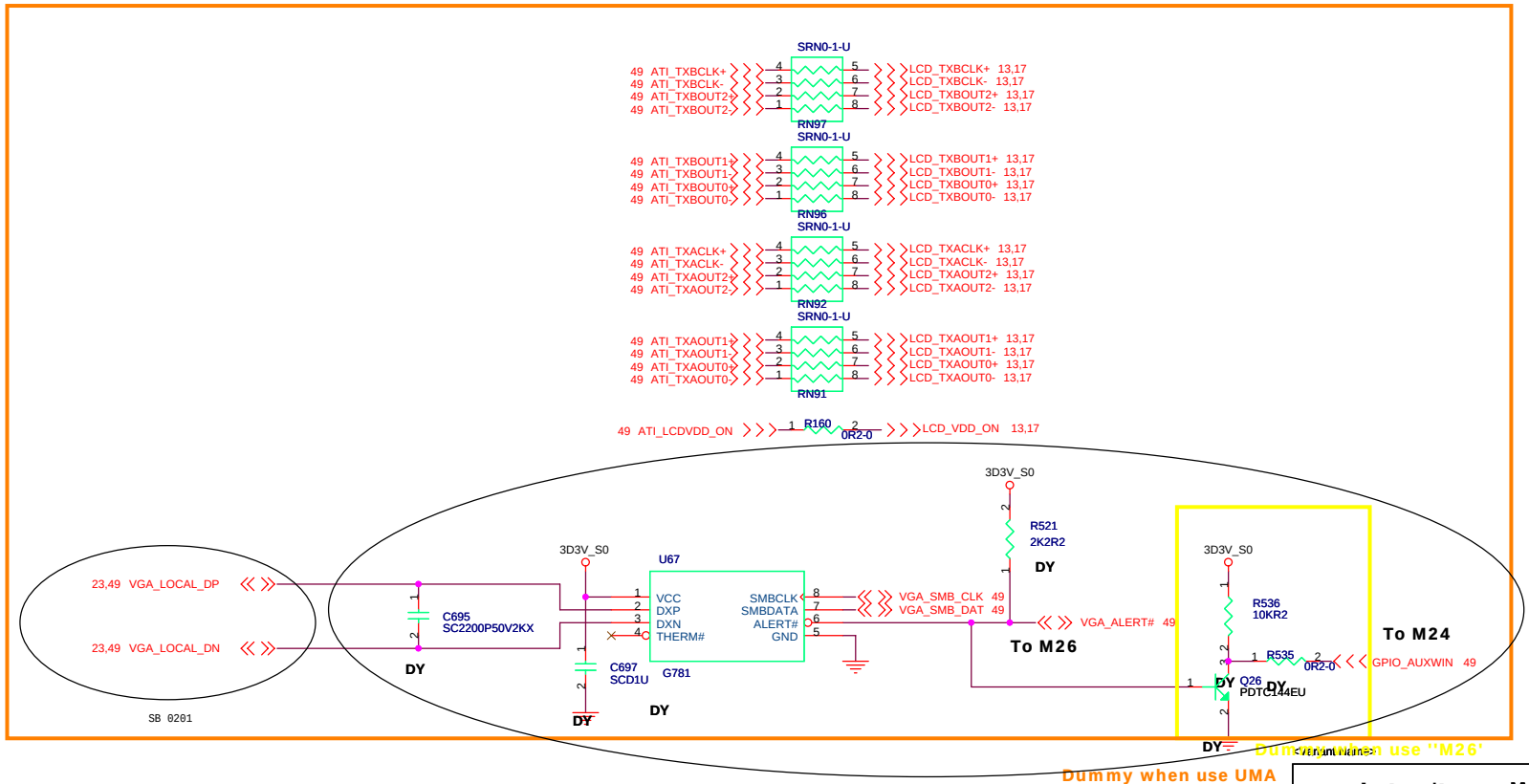
Date: Thursday, March 31, 2005	Sheet 53 of 58	

SB 0201



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Title: VGA SELECTOR

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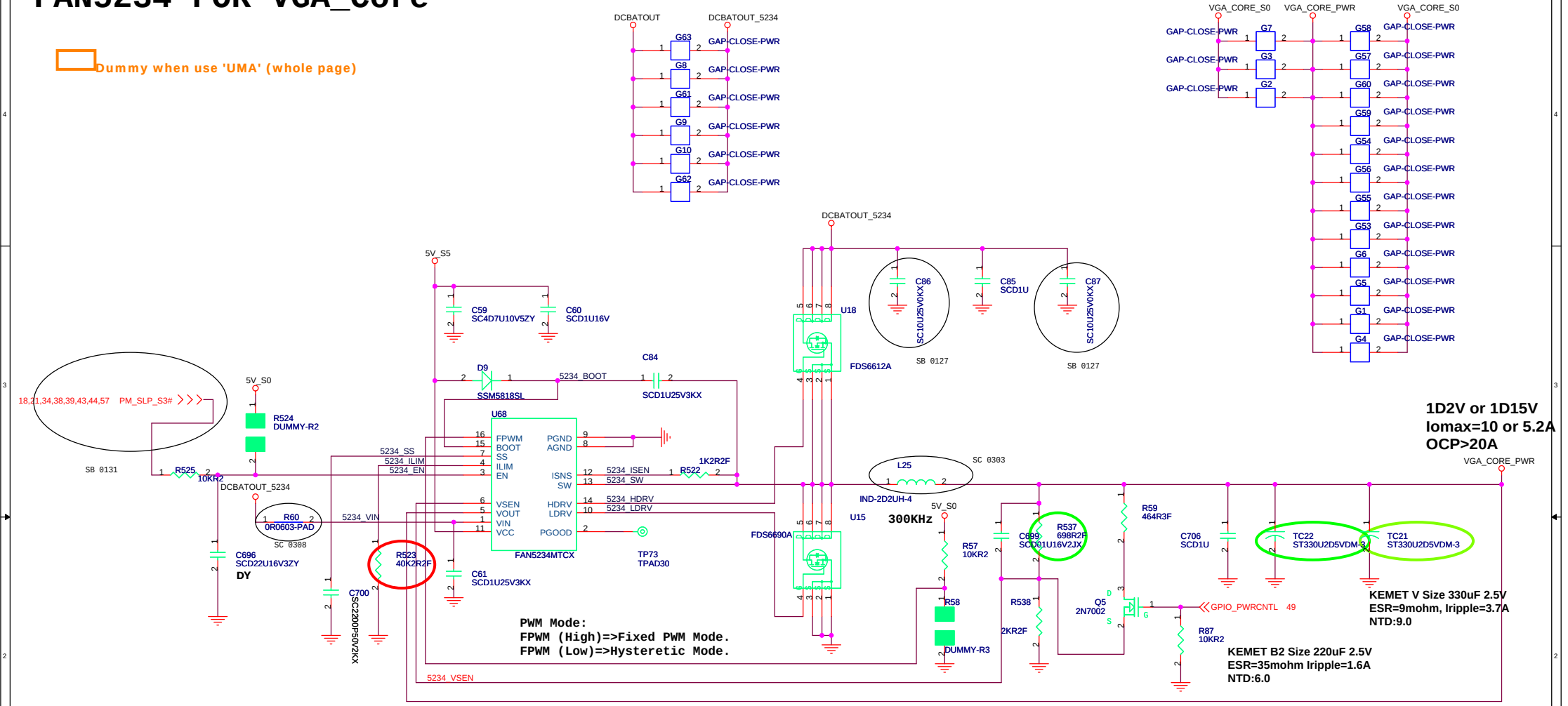
FAN5234 FOR VGA_Core

Dummy when use 'UMA' (whole page)

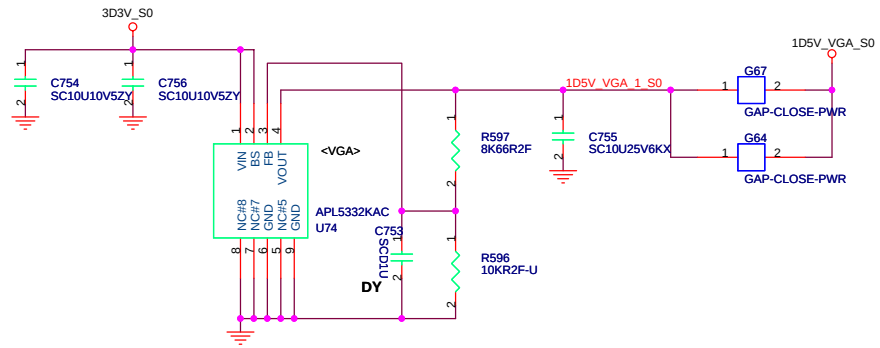


Rilim=(11.2/Iilim)*((100+Rsense)/Rdson)

High(3.3V)=>Vo=1.0V
Low(0V)=>Vo=1.2V

Vout Setting:
0.9V/Rlow=(Vout-0.9V)/Rhigh

M24/M26 POWER PLAY (GPIO_PWRCNTL)
high (3.3V) = set lower core voltage (VDDC = 1.0V)
low (0V) = set higher core voltage (VDDC = 1.2V)



(Power Team)

<Variant Name>

緯創資通 Wistron Corporation
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Title: VGA CORE 1D2V or 1D0V

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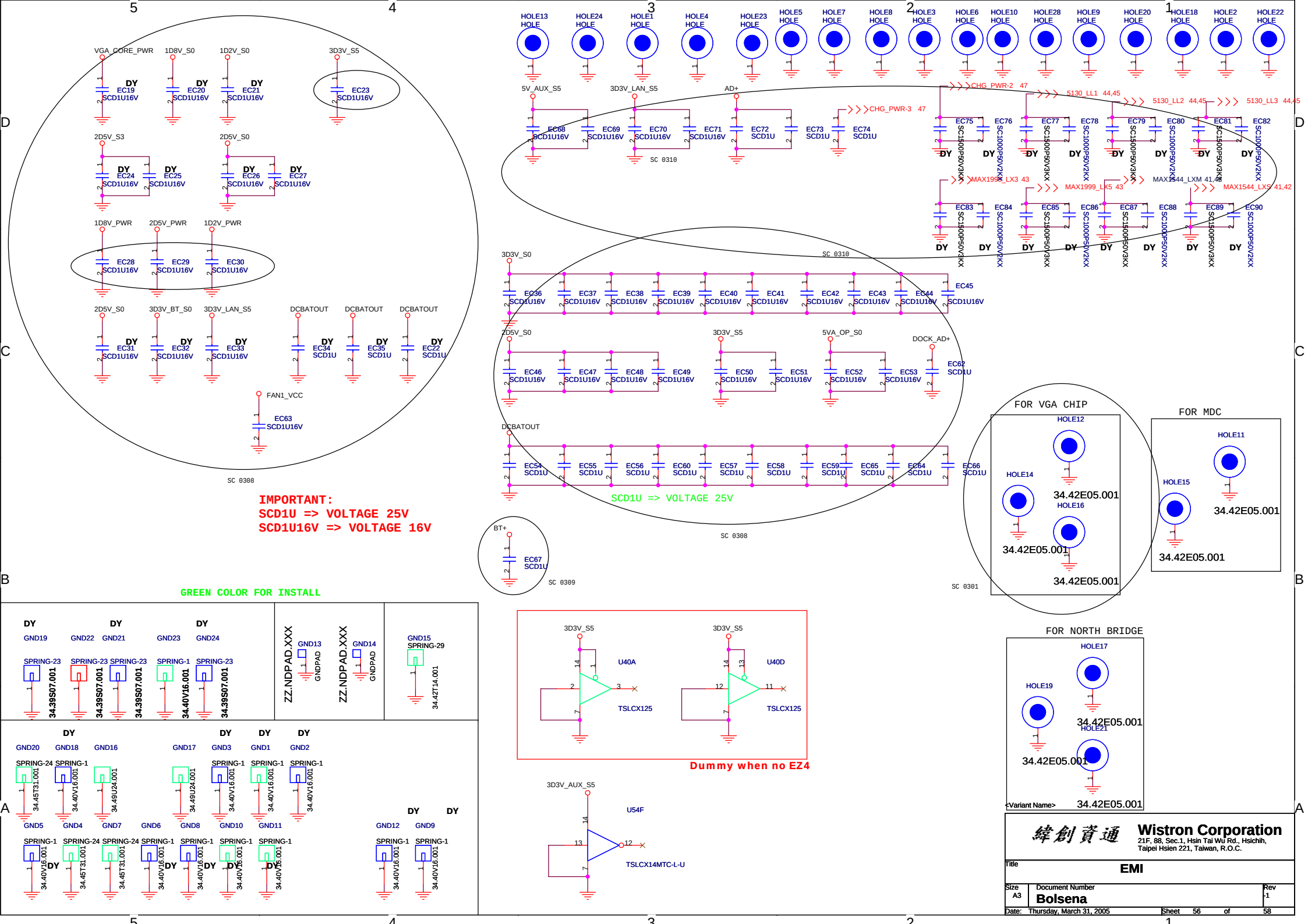
VGA_CORE_PWR
1D8V_S0
1D2V_S0
3D3V_S5
EC19 SCD1U16V
EC20 SCD1U16V
EC21 SCD1U16V
EC23 SCD1U16V
2D5V_S3
2D5V_S0
EC24 SCD1U16V
EC25 SCD1U16V
EC26 SCD1U16V
EC27 SCD1U16V
1D8V_PWR
2D5V_PWR
1D2V_PWR
EC28 SCD1U16V
EC29 SCD1U16V
EC30 SCD1U16V
2D5V_S0
3D3V_BT_S0
3D3V_LAN_S5
DCBATOUT
EC31 SCD1U16V
EC32 SCD1U16V
EC33 SCD1U16V
EC34 SCD1U
EC35 SCD1U
EC22 SCD1U
FAN1_VCC
EC63 SCD1U16V
SC 0308
IMPORTANT:
SCD1U => VOLTAGE 25V
SCD1U16V => VOLTAGE 16V
HOLE13 HOLE
HOLE24 HOLE
HOLE1 HOLE
HOLE4 HOLE
HOLE23 HOLE
HOLE5 HOLE
HOLE7 HOLE
HOLE8 HOLE
HOLE3 HOLE
HOLE6 HOLE
HOLE10 HOLE
HOLE28 HOLE
HOLE9 HOLE
HOLE20 HOLE
HOLE18 HOLE
HOLE2 HOLE
HOLE22 HOLE
5V_AUX_S5
3D3V_LAN_S5
AD+
EC68 SCD1U16V
EC69 SCD1U16V
EC70 SCD1U16V
EC71 SCD1U16V
EC72 SCD1U
EC73 SCD1U
EC74 SCD1U
CHG_PWR-3 47
SC 0310
CHG_PWR-2 47
5130_LL1 44,45
5130_LL2 44,45
5130_LL3 44,45
EC75 SC1500P50V3KX
EC76 SC1000P50V2KX
EC77 SC1500P50V3KX
EC78 SC1000P50V2KX
EC79 SC1500P50V3KX
EC80 SC1000P50V2KX
EC81 SC1500P50V3KX
EC82 SC1000P50V2KX
MAX1999_LX3 43
MAX1999_LX5 43
MAX1544_LXM 41,42
MAX1544_LXS 41,42
EC83 SC1500P50V3KX
EC84 SC1000P50V2KX
EC85 SC1500P50V3KX
EC86 SC1000P50V2KX
EC87 SC1500P50V3KX
EC88 SC1000P50V2KX
EC89 SC1500P50V3KX
EC90 SC1000P50V2KX
3D3V_S0
EC36 SCD1U16V
EC37 SCD1U16V
EC38 SCD1U16V
EC39 SCD1U16V
EC40 SCD1U16V
EC41 SCD1U16V
EC42 SCD1U16V
EC43 SCD1U16V
EC44 SCD1U16V
EC45 SCD1U16V
2D5V_S0
3D3V_S5
5VA_OP_S0
DOCK_AD+
EC46 SCD1U16V
EC47 SCD1U16V
EC48 SCD1U16V
EC49 SCD1U16V
EC50 SCD1U16V
EC51 SCD1U16V
EC52 SCD1U16V
EC53 SCD1U16V
EC62 SCD1U
DCBATOUT
EC54 SCD1U
EC55 SCD1U
EC56 SCD1U
EC60 SCD1U
EC57 SCD1U
EC58 SCD1U
EC59 SCD1U
EC65 SCD1U
EC64 SCD1U
EC66 SCD1U
SCD1U => VOLTAGE 25V
SC 0308
BT+
EC67 SCD1U
SC 0309
FOR VGA CHIP
HOLE12
HOLE14
34.42E05.001
HOLE16
34.42E05.001
34.42E05.001
SC 0301
FOR MDC
HOLE11
HOLE15
34.42E05.001
34.42E05.001
GREEN COLOR FOR INSTALL
GND19
GND22
GND21
GND23
GND24
SPRING-23
SPRING-1
34.39S07.001
34.40V16.001
ZZ.NDPAD.XXX
GND13
GND14
GNDPAD
GND15
SPRING-29
34.42T14.001
GND20
GND18
GND16
GND17
GND3
GND1
GND2
SPRING-24
34.45T31.001
34.49U24.001
GND5
GND4
GND7
GND6
GND8
GND10
GND11
GND12
GND9
3D3V_S5
U40A
U40D
TSLCX125
Dummy when no EZ4
3D3V_AUX_S5
U54F
TSLCX14MTC-L-U
FOR NORTH BRIDGE
HOLE17
HOLE19
34.42E05.001
HOLE21
34.42E05.001
<Variant Name>
34.42E05.001
緯創資通
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI
Size
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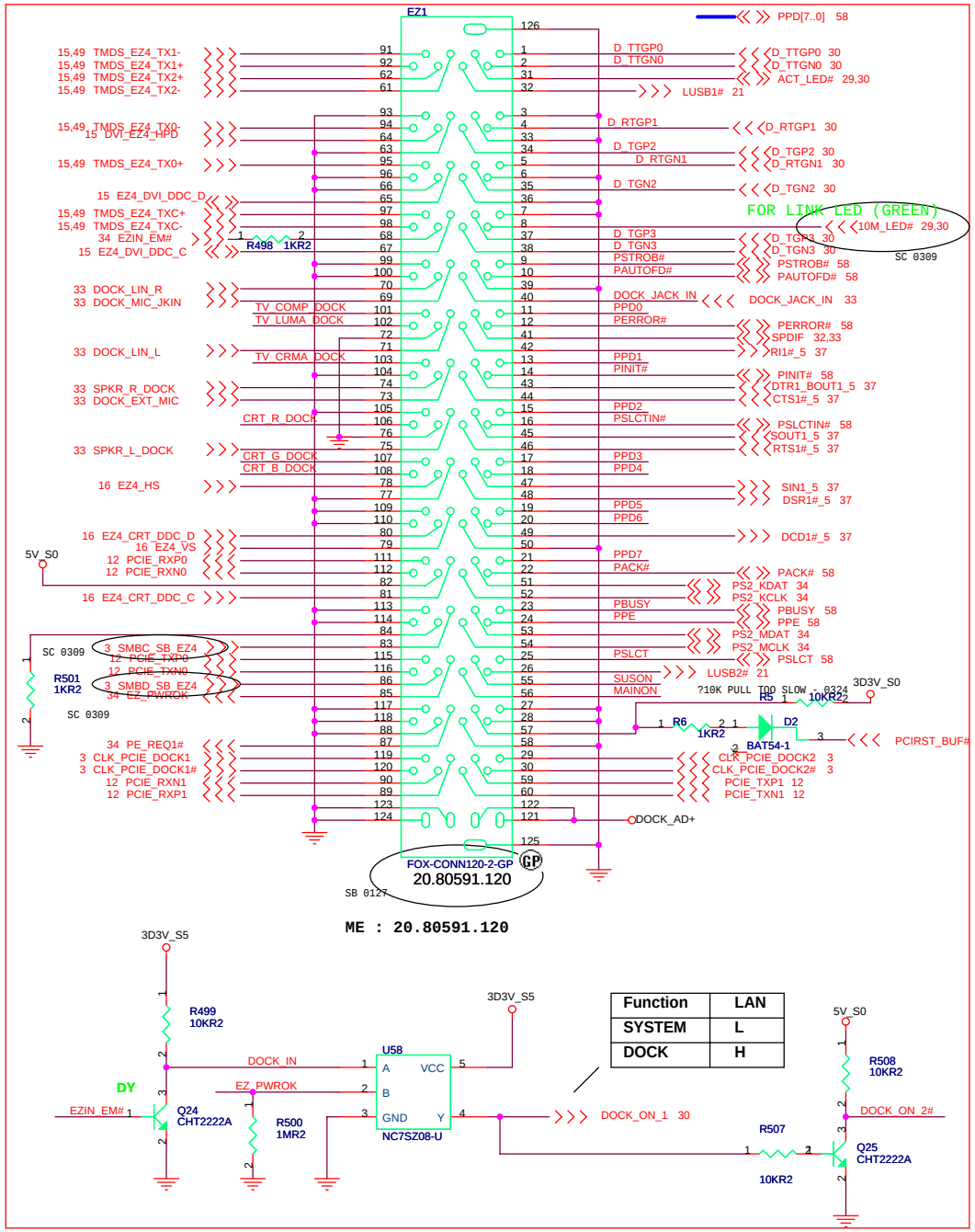
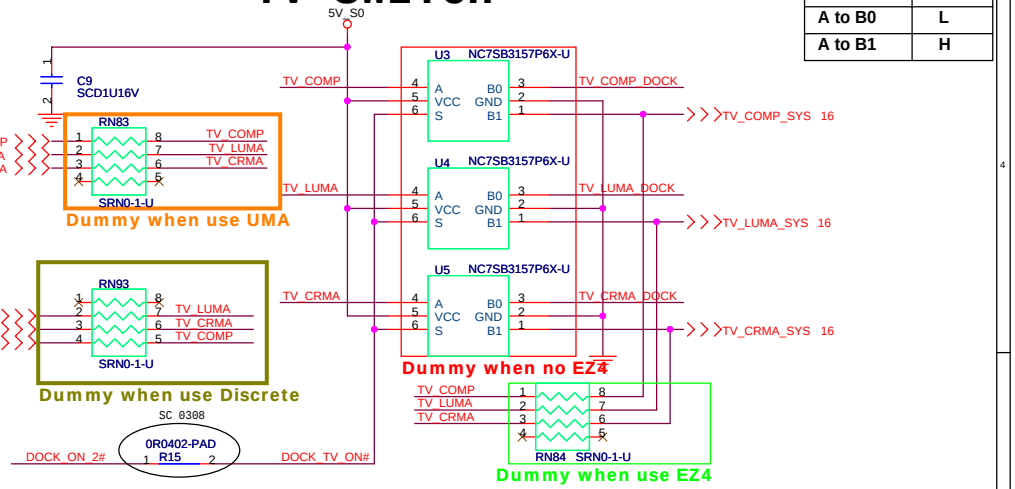


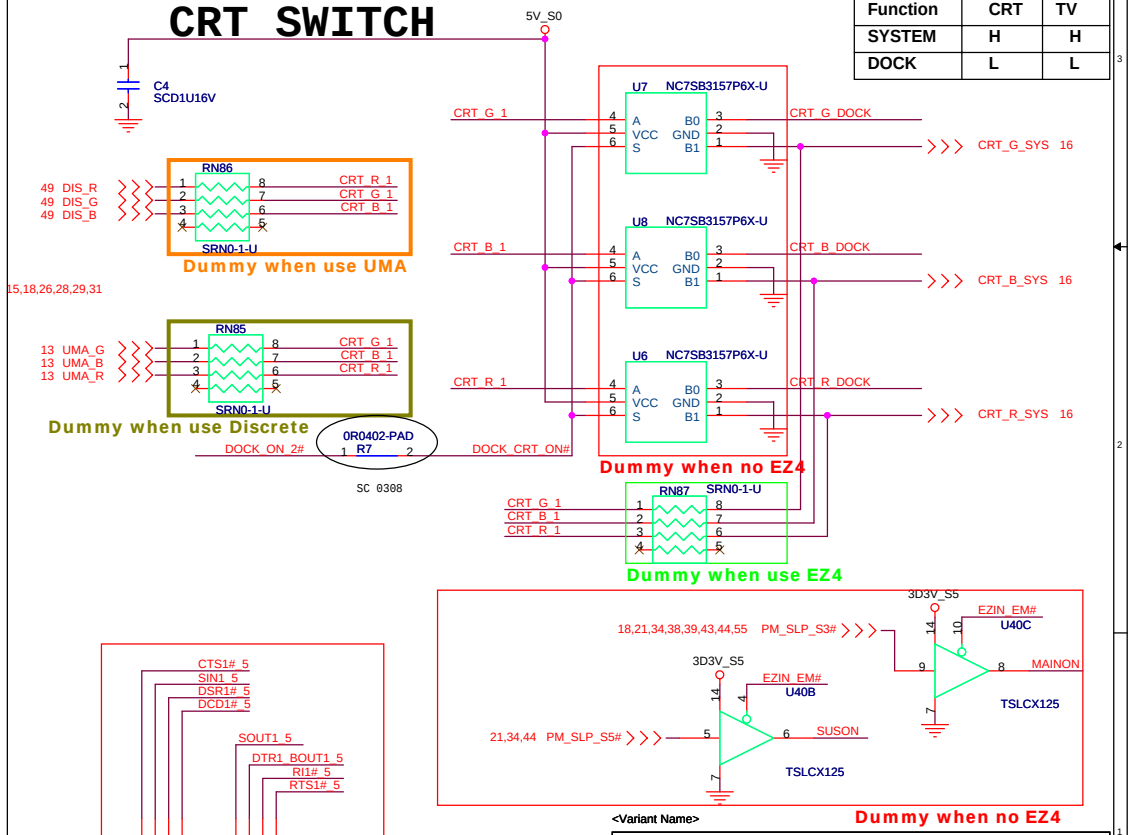
TV SWITCH

Function	S
A to B0	L
A to B1	H



CRT SWITCH

Function	CRT	TV
SYSTEM	H	H
DOCK	L	L



<variant_name>

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Title: EASY PORT4 (1/2)

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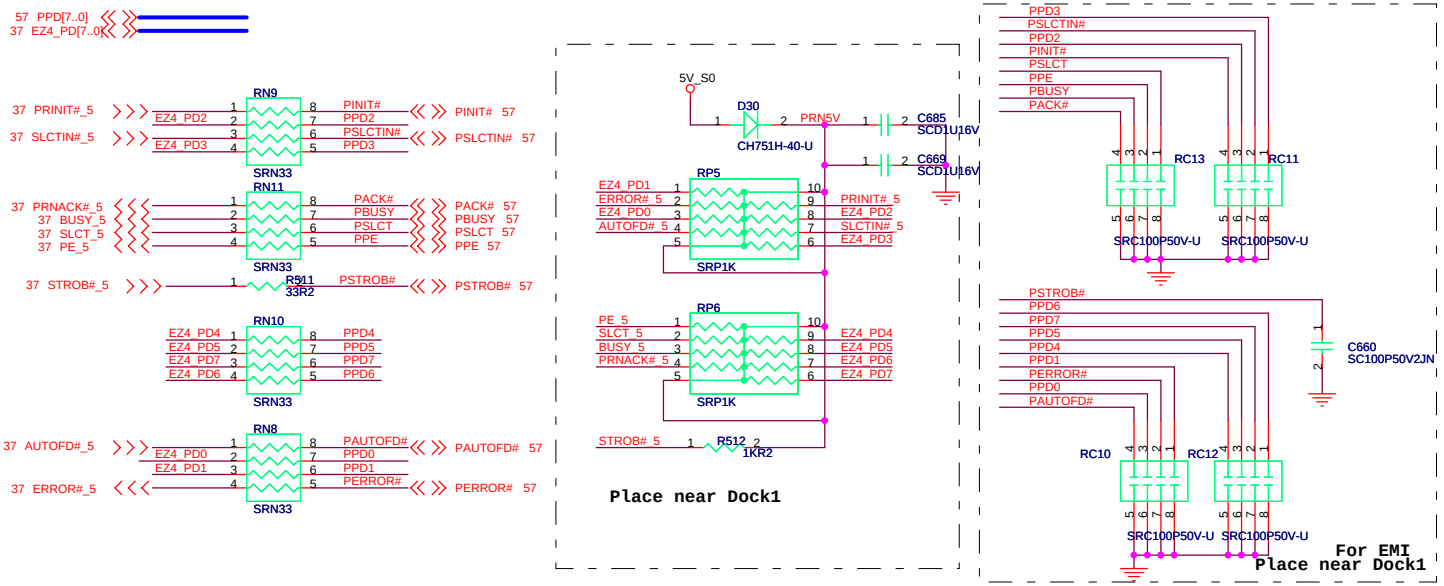
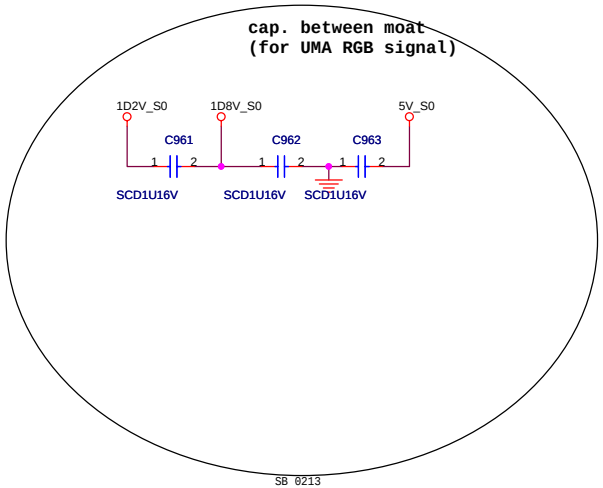
PRINT PORT



Dummy when no EZ4



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***EASY PORT4 (2/2)***	
Size A3	Document Number Bolsena	Rev -1
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