

# ACLU1&ACLU2


(G40-70 & G50-70)

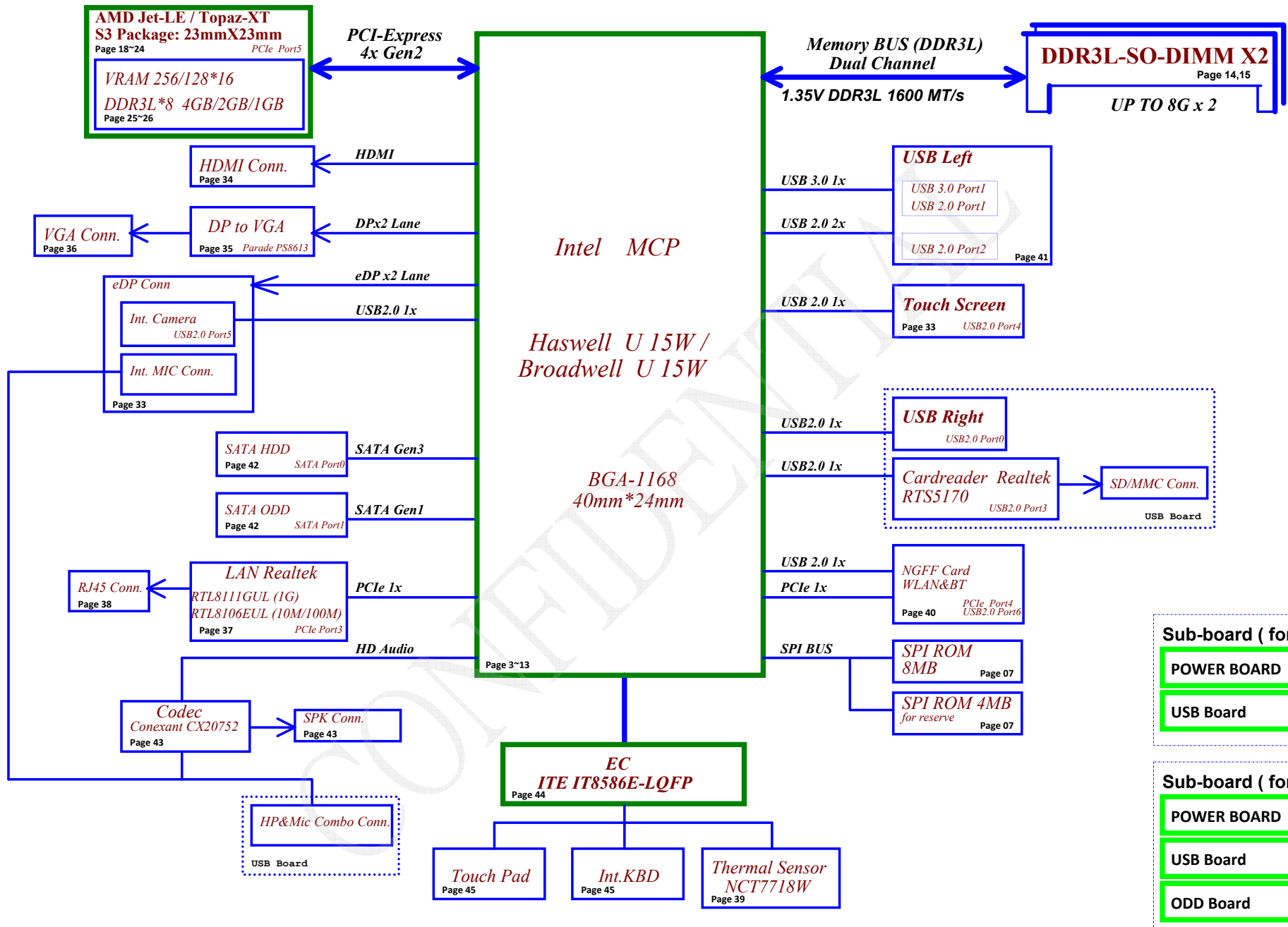
NM-A271 Rev 1.0 Schematic

Intel Haswell/Broadwell U-Processor with DDRIII L + AMD Jet-LE/Topaz-XT GPU

2013-12-17

REV: 1.0

Security Classification		LC Future Center Secret Data		Title			
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Cover Page		Size	Document Number
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	Block Diagram	
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Voltage Rails ( O --> Means ON , X --> Means OFF )

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.35V	+5VS +3VS +1.5VS +1.35VS +1.05VS +0.675VS CPU_CORE  +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0 EHCI1		USB 3.0 XHCI	
0	USB Port (Right Side)		
1	USB Port1 (Left Side)	1	USB Port1 (Left Side)
2	USB Port2 (Left Side)	2	
3	Cardreader	3	
4	TOUCH PANEL	4	
5	Camera		
6	NGFF(WLAN)		
7			

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
100M@	100M LAN Part
14@	For 14" part
15@	For 15" part
AOAC@	AOAC support part
GIGA@	GIGA LAN Part
JET@	For AMD Jet GPU part
ME@	ME part(connector, hole)
PX@	Discrete GPU SKU part
RANKA@	For VRAM RankA part
RANKB@	For VRAM RankB part
TOPAZ@	For AMD Topaz GPU part
TS@	For support touch panel sku part
UMA@	UMA SKU part
H2@	Hynix 128Mx16 VRAM part
H4@	Hynix 256Mx16 VRAM part
M2@	Micron 128Mx16 VRAM part
M4@	Micron 256Mx16 VRAM part
S2@	Samsung 128Mx16 VRAM part
S4@	Samsung 256Mx16 VRAM part
H2GX8@	Hynix 128Mx16 VRAM x8pcs sku
H4GX4@	Hynix 256Mx16 VRAM x4pcs sku
M4GX4@	Micron 256Mx16 VRAM x4pcs sku
CD@	Cost down part

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

PCIe PORT LIST

Port	Device
1	
2	
3	LAN
4	WLAN
5	Discrete GPU
6	

EC SM Bus1 address

EC SM Bus2 address

PCH SM Bus address

Device	Address	Device	Address	Device	Address
Smart Battery	0X16	Thermal Sensor NCT7718W	1001_100xb	DDR DIMMA	1010 000Xb
Charger	0001 0010 b	VGA	0x41(default)	DDR DIMMB	1010 010Xb
		PCH	need to update	Wlan	Rsvd

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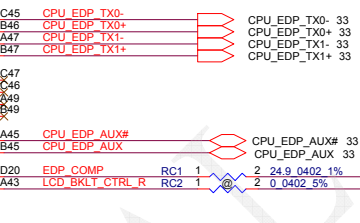
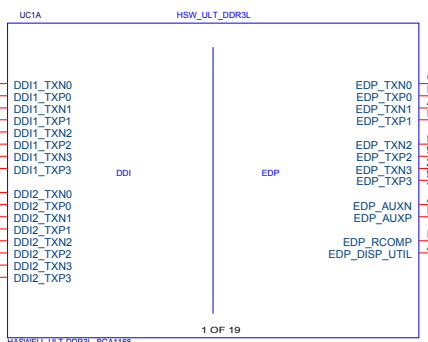
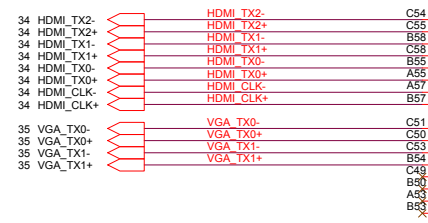
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Title	Notes List
ACL1 & ACLU2	

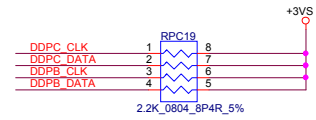
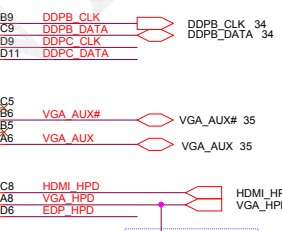
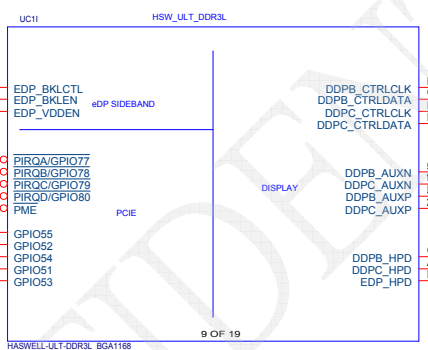
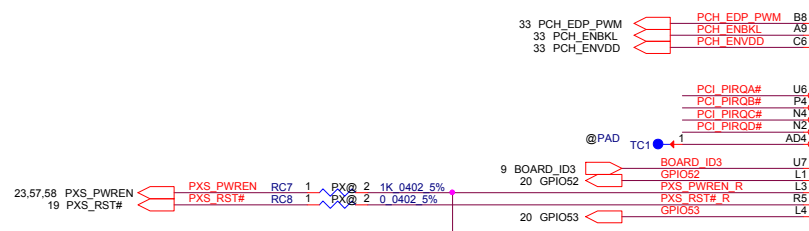
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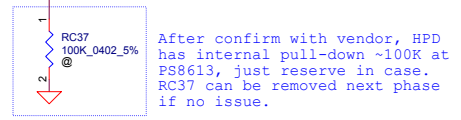
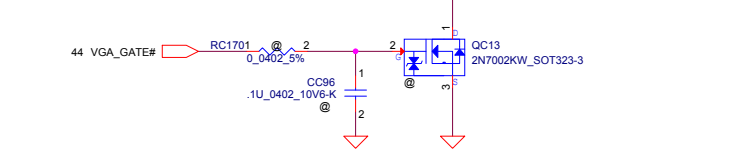
HDMI D2  
HDMI D1  
HDMI D0  
HDMI CLK  
DP TO VGA Converter



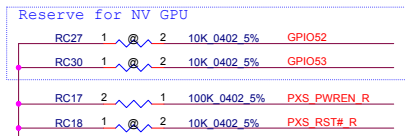
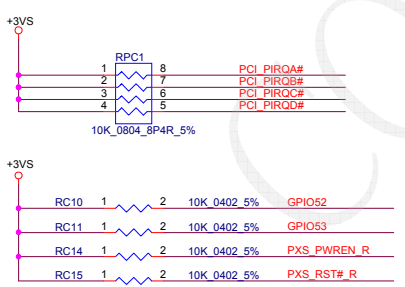
+VCCIOA\_OUT & EDP\_COMP :  
Trace Width: 20mil  
Space: 25mil  
Max length: 100mil



DDPx\_CTRLDATA  
The signal has a weak internal pull-down.  
\* H Port is detected.  
L Port is not detected.



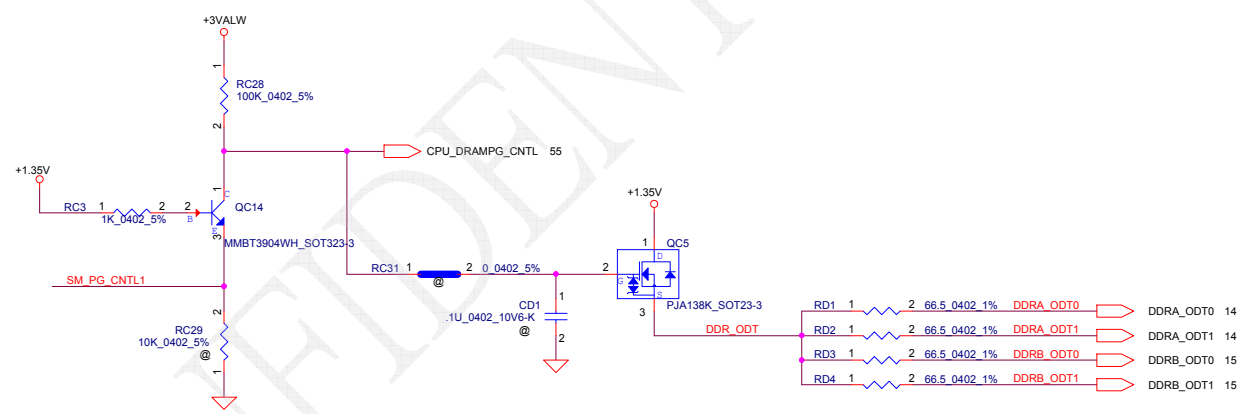
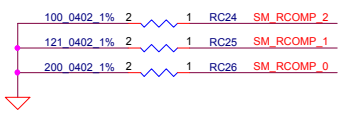
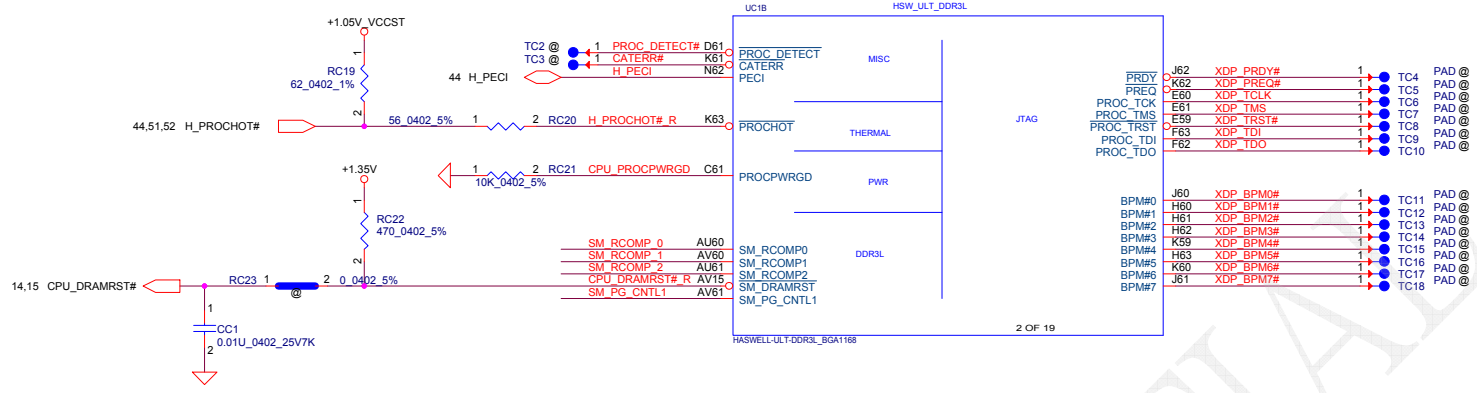
After confirm with vendor, HPD has internal pull-down ~100K at P88613, just reserve in case. RC37 can be removed next phase if no issue.



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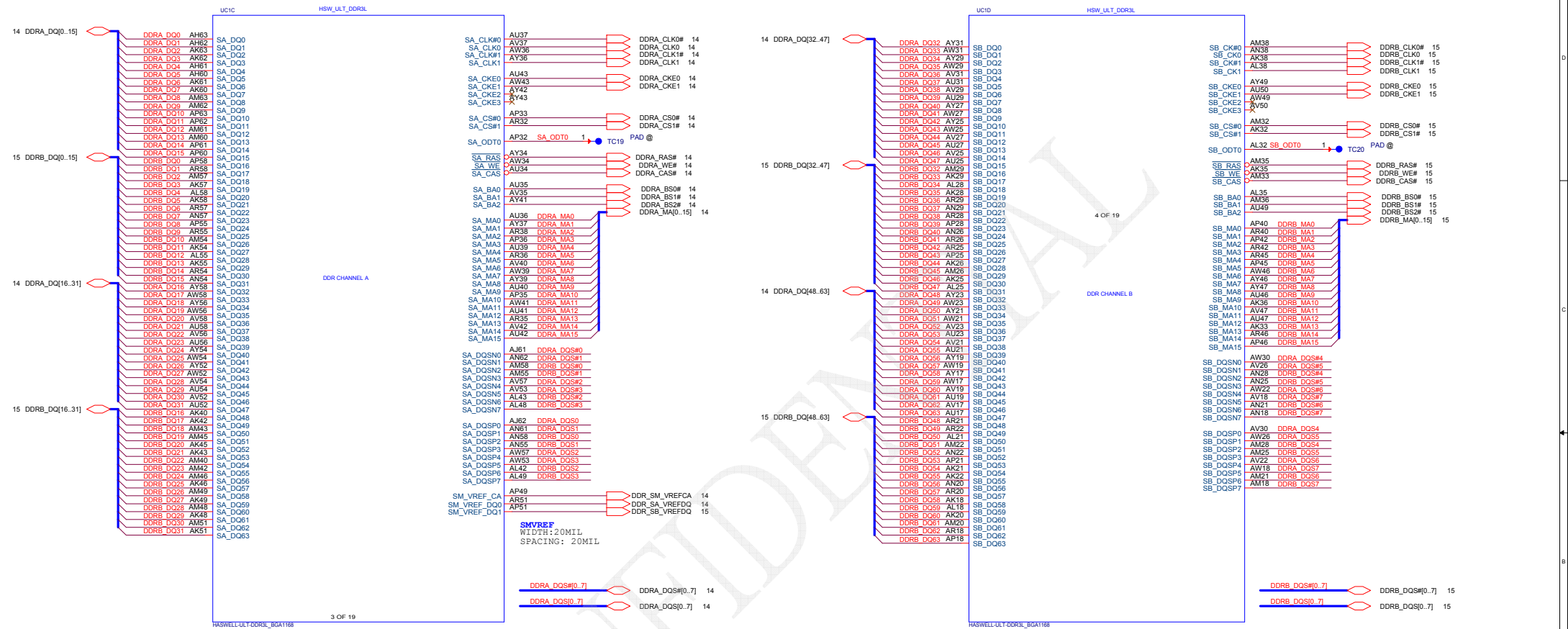
Title	MCP (DDI,EDP)		
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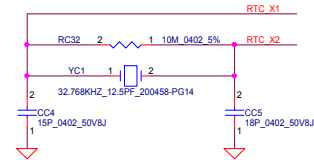
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Size	Document Number	Rev
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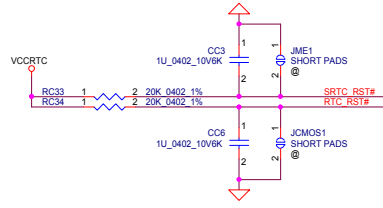
HASWELL\_ULT\_DDR3L\_BGA1168 3 OF 19

HASWELL\_ULT\_DDR3L\_BGA1168 4 OF 19

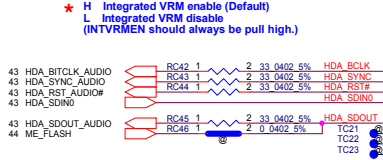
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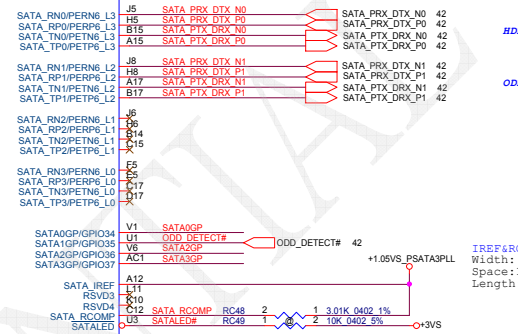
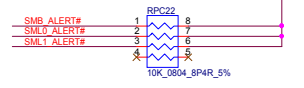
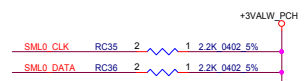
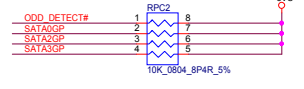
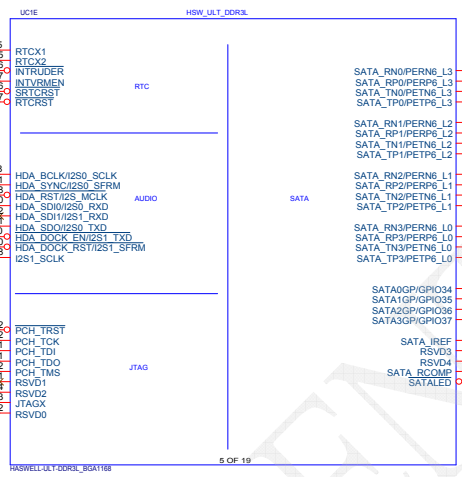
**CRYSTAL**  
 1. Space 15mil  
 2. No trace under crystal  
 3. Place on opposite side of MCP for temp influence



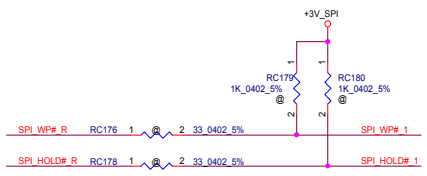
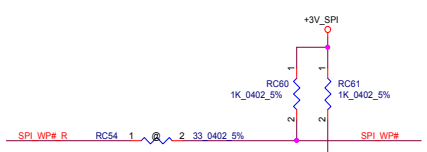
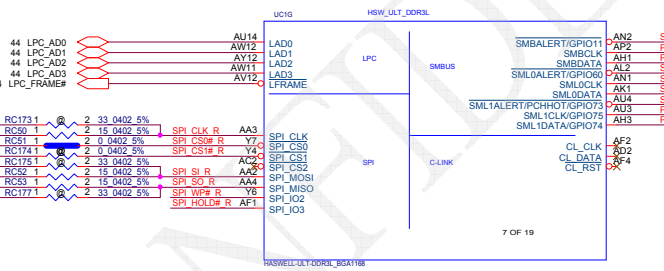
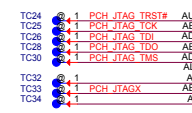
**INTVRMEN**  
 H Integrated VRM enable (Default)  
 L Integrated VRM disable (INTVRMEN should always be pull high.)



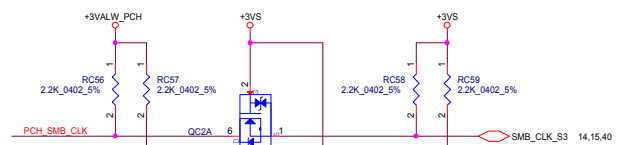
**HDA\_SDO** This signal has a weak internal pull-down.  
 0 = Enable security measures defined in the Flash Descriptor.  
 1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.



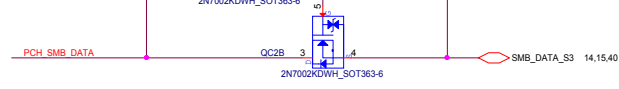
IREF6RCOMP  
 Width: 12-15mil  
 Space: 12mil  
 Length: 500mil



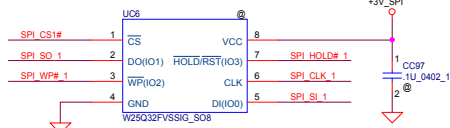
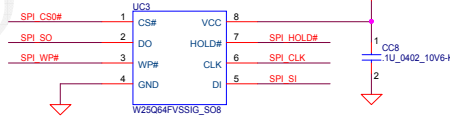
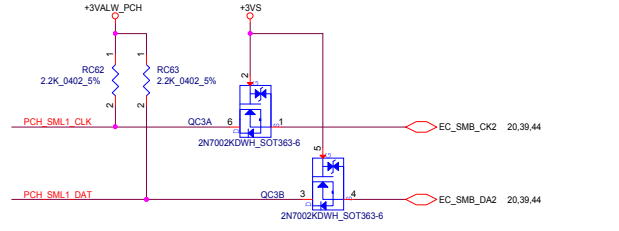
**+3V\_SPI**  
 1. If support DS3, connect to +3VS and don't support EC mirror code;  
 2. If don't support DS3, connect to +3VALW\_PCH and support EC mirror code.



DIMM1, DIMM2, NGFF

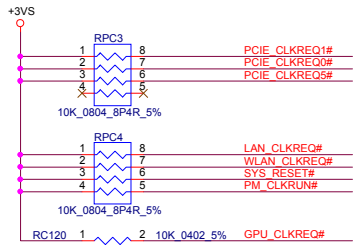


GPU, EC, Thermal Sensor

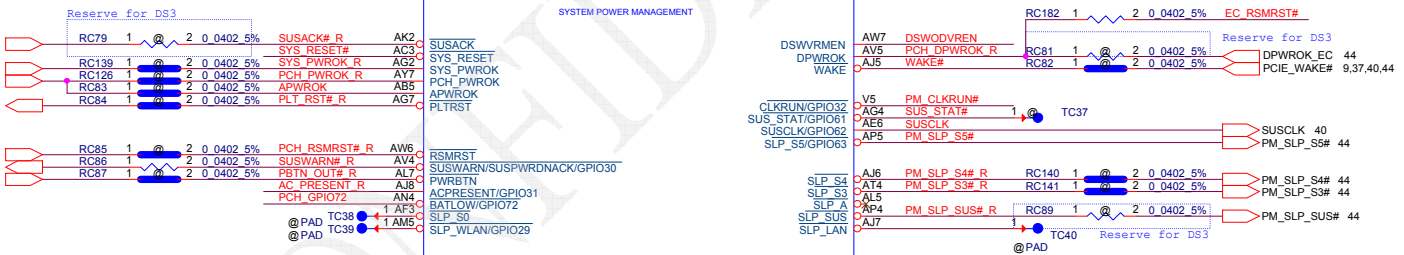
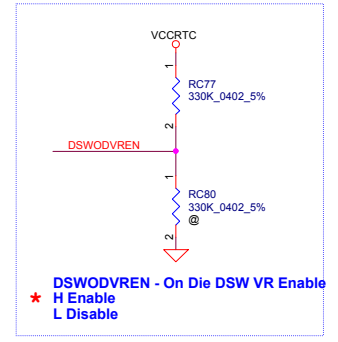
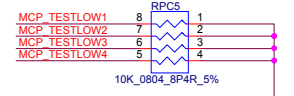
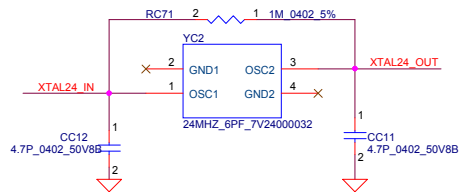
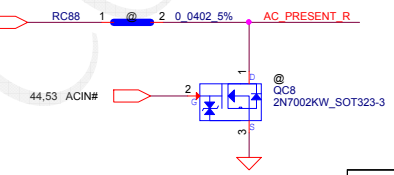
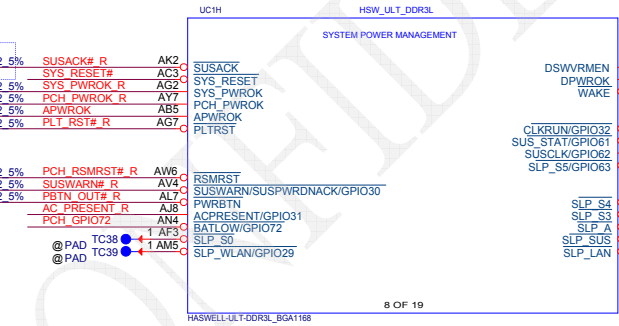
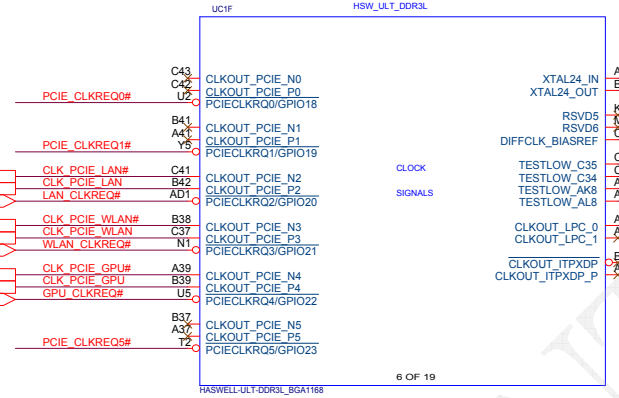
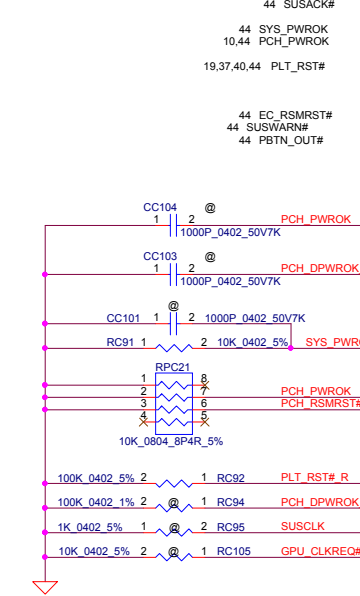
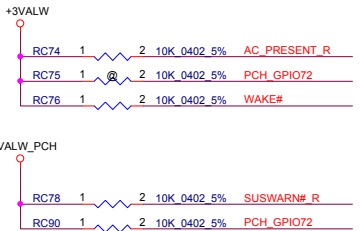


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Size	Document Number	MCP (RTC&AUDIO&SATA&S) <b>ACLU1 &amp; ACLU2</b>	
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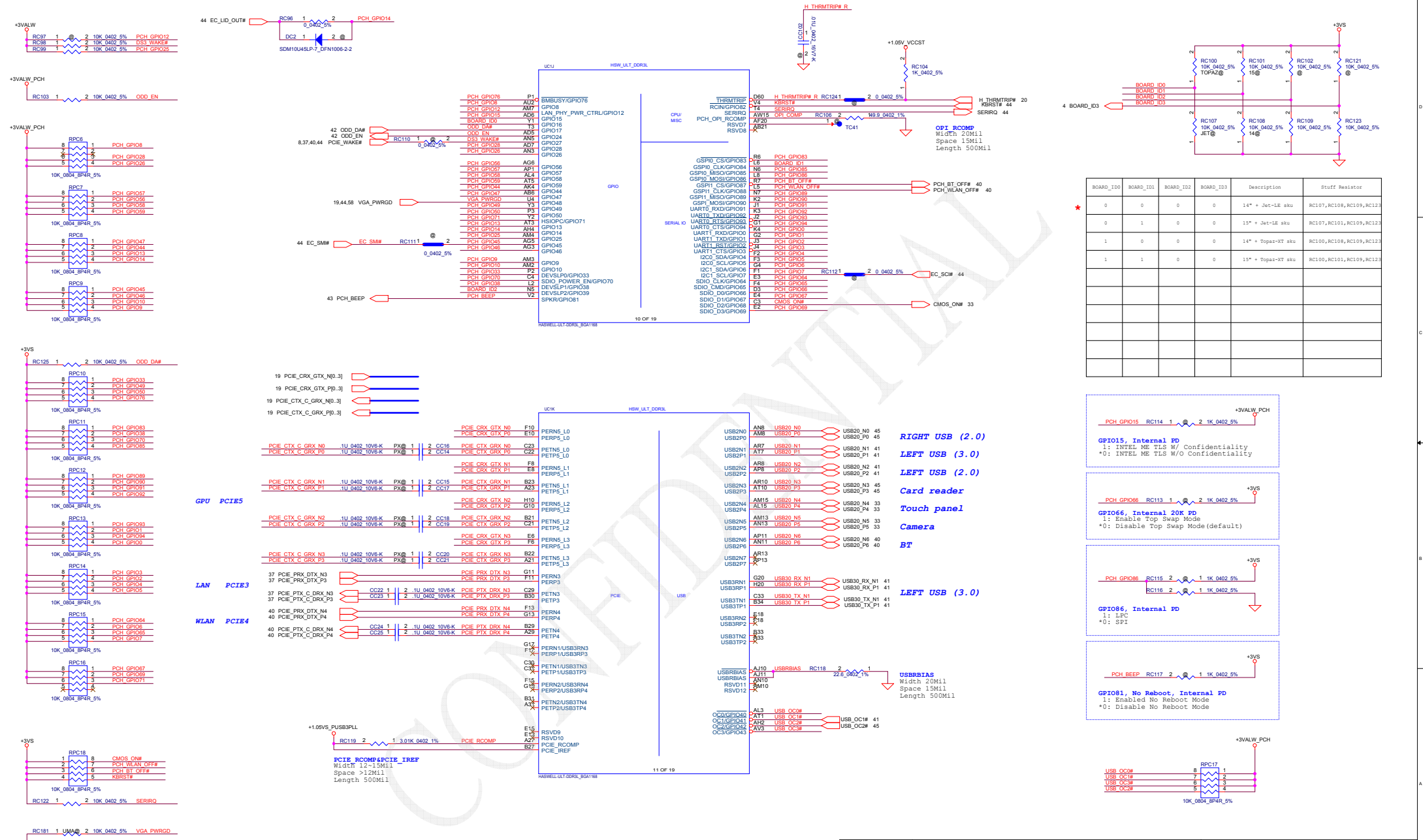
PCIE CLK2 LAN  
PCIE CLK3 WLAN  
PCIE CLK4 GPU



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Title	MCP (Clock,PM)	
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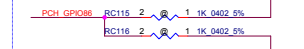
BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description	Staff Baseline
0	0	0	0	14" + Jet-LE sku	RC107,RC108,RC109,RC113
0	0	0	0	10" + Jet-LE sku	RC107,RC109,RC109,RC113
1	0	0	0	14" + Topaz-XT sku	RC109,RC108,RC109,RC113
1	1	0	0	15" + Topaz-XT sku	RC109,RC101,RC109,RC113



**GPIO15, Internal PD**  
 1: INTEL ME TLS W/ Confidentiality  
 \*0: INTEL ME TLS W/O Confidentiality



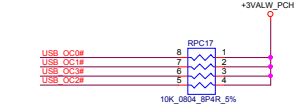
**GPIO66, Internal 20K PD**  
 1: Enable Top Swap Mode  
 \*0: Disable Top Swap Mode (default)



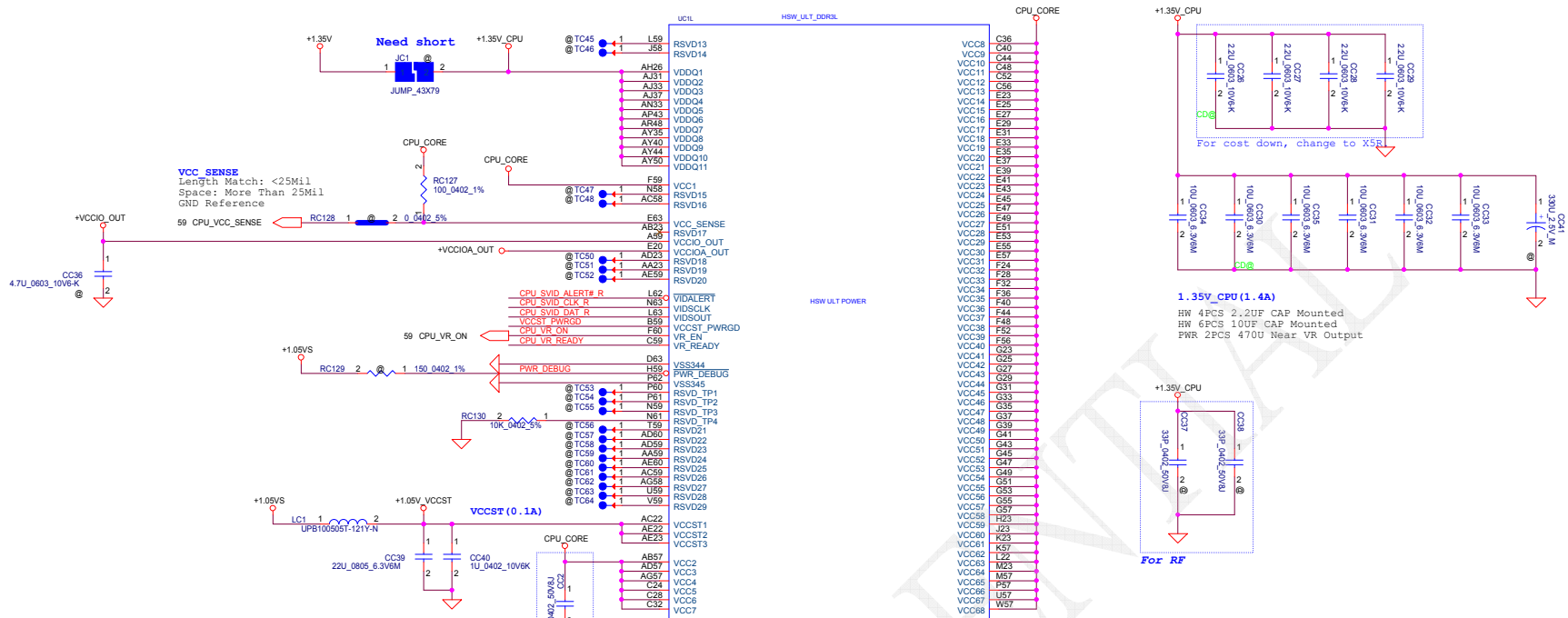
**GPIO86, Internal PD**  
 1: I2C  
 \*0: SPI



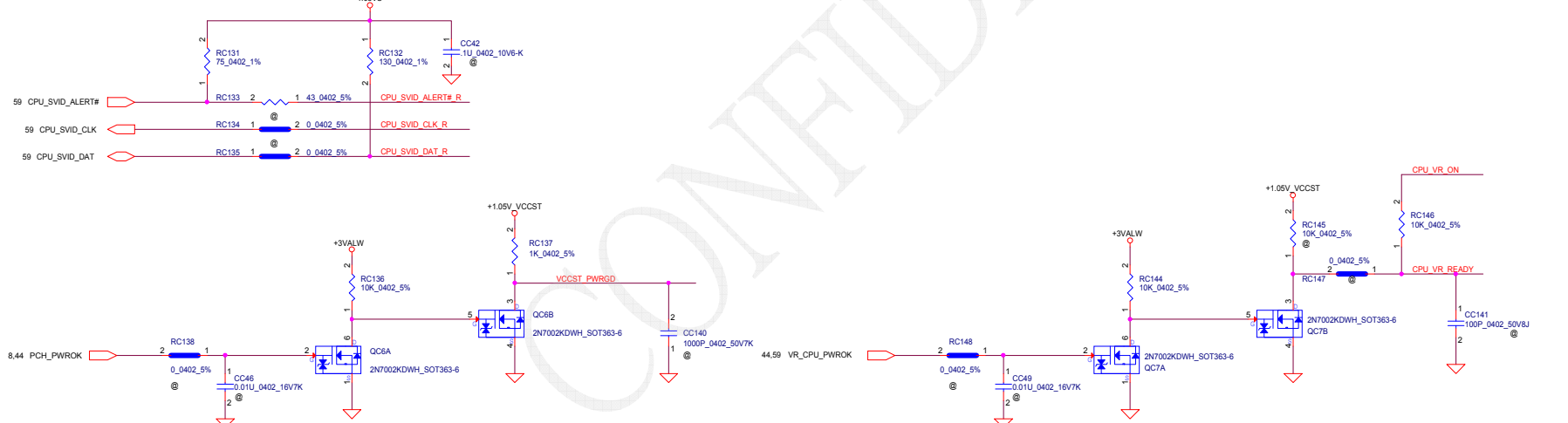
**GPIO81, No Reboot, Internal PD**  
 1: Enabled No Reboot Mode  
 \*0: Disable No Reboot Mode



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<b>Date</b>	Thursday, December 19, 2013	<b>Sheet</b>	9	<b>of</b> 56

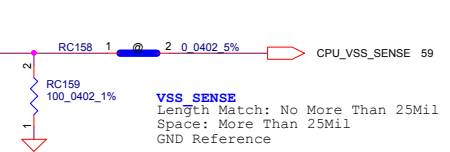
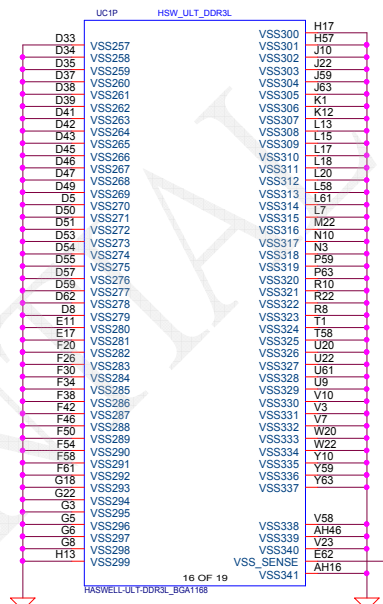
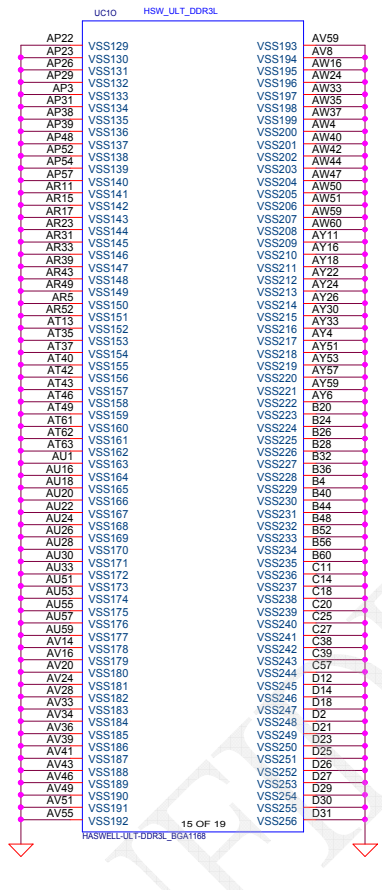
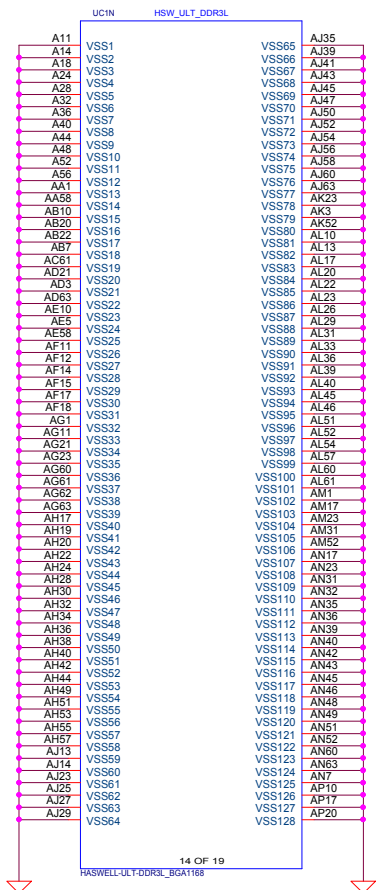


**SVID**  
1, Stripline Line, No More Than 6000Mil  
2, Alert# Route Between CLK and Data  
3, CLK Length<Data Length<CLK Length + 2000Mil  
4, Space at least 18Mil



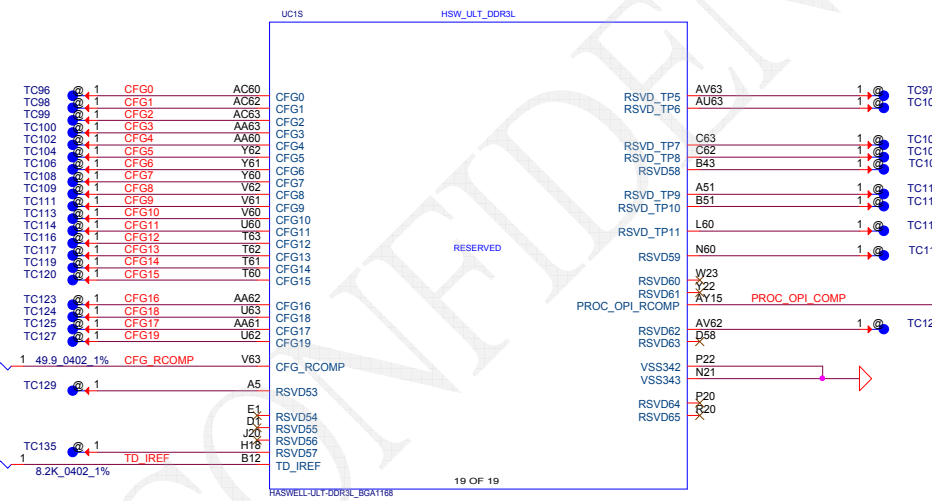
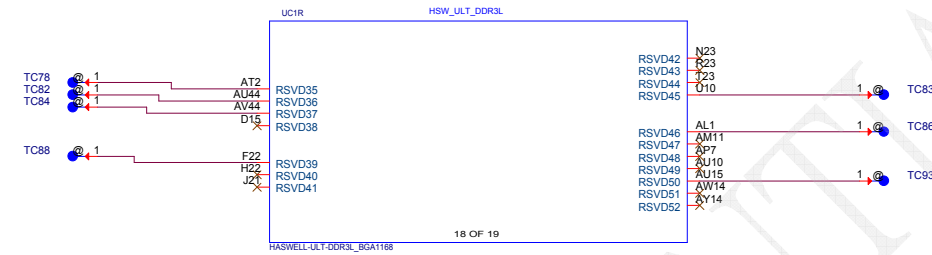
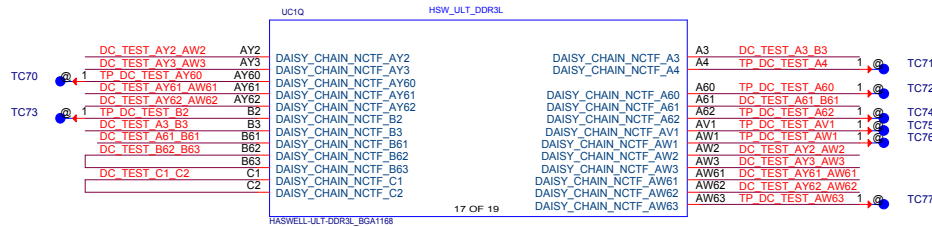
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	
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**VSS SENSE**  
 Length Match: No More Than 25Mil  
 Space: More Than 25Mil  
 GND Reference

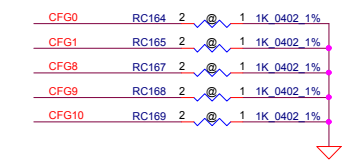
Security Classification	LC Future Center Secret Data		Title
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**CFG\_RCOMP&TD\_IREF**  
Width 20Mil  
Space 15Mil  
Length 500Mil

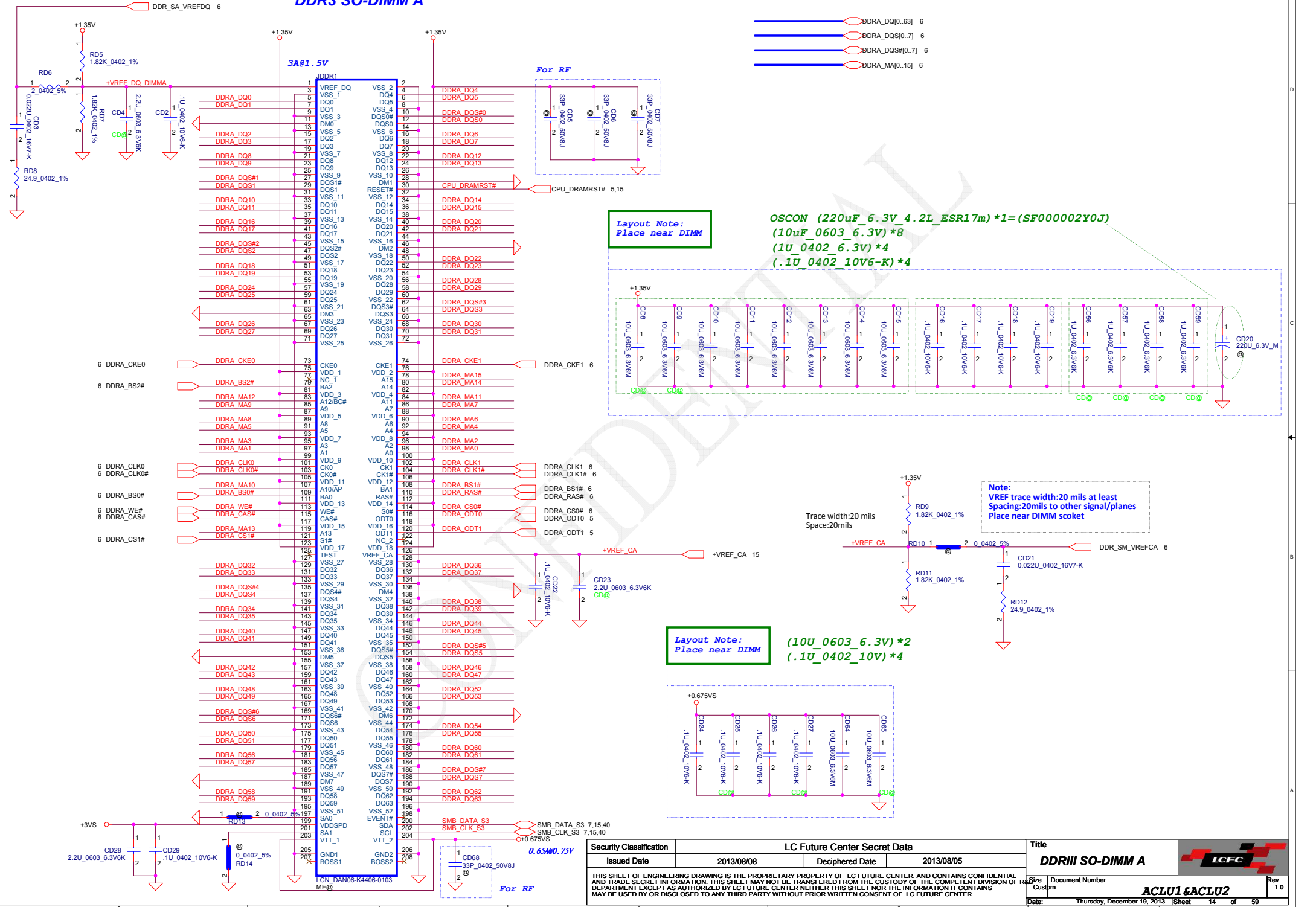
**CFG3**  
\*1: Disable  
0: Enable, Set DFX Enabled BIT  
In Debug Interface MSR

**CFG4**  
\*L: eDP enable  
H: eDP disable



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Size	Document Number	ACLU1 & ACLU2		Rev	1.0
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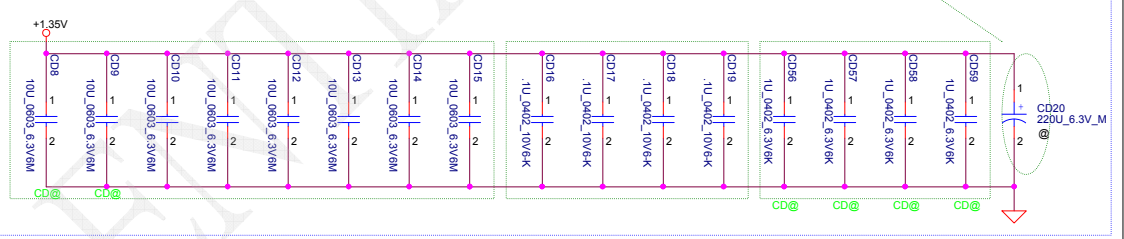
# DDR3 SO-DIMM A



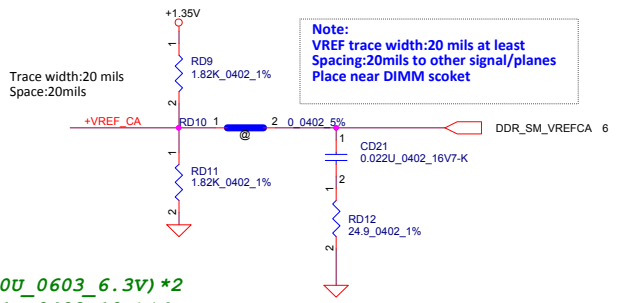
- DDR3\_DQ[0..63] 6
- DDR3\_DQS[0..7] 6
- DDR3\_DQS# [0..7] 6
- DDR3\_MA[0..15] 6

**Layout Note:**  
Place near DIMM

**OSCON** (220uF\_6.3V\_4.2L\_ESR17m) \*1=(SF000002Y0J)  
(10uF\_0603\_6.3V) \*8  
(1U\_0402\_6.3V) \*4  
(.1U\_0402\_10V6-K) \*4

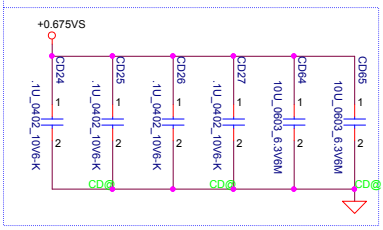


**Note:** VREF trace width: 20 mils at least  
Spacing: 20mils to other signal/planes  
Place near DIMM socket



**Layout Note:**  
Place near DIMM

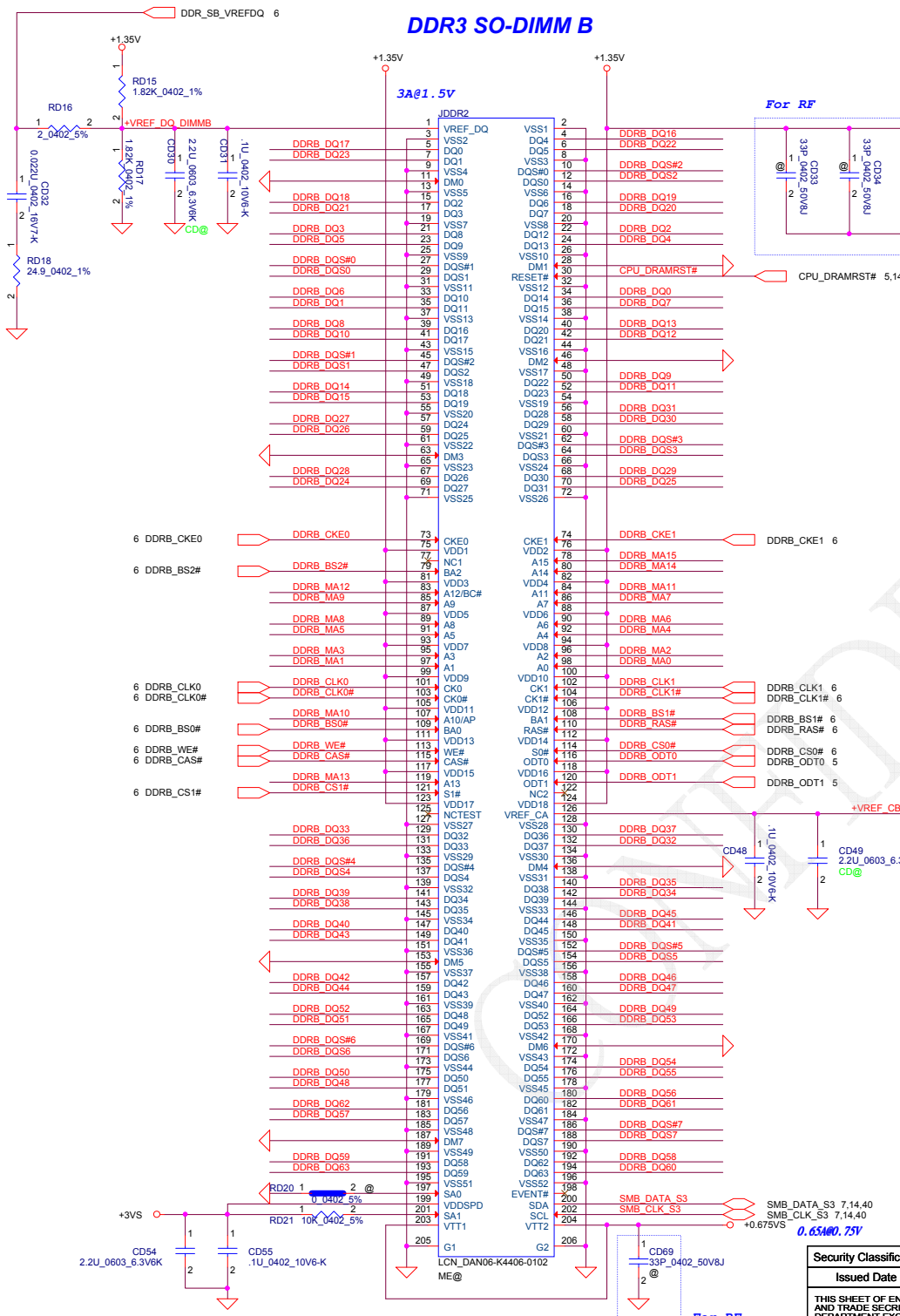
(10U\_0603\_6.3V) \*2  
(.1U\_0402\_10V) \*4



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				<b>ACLU1 &amp; ACLU2</b>	
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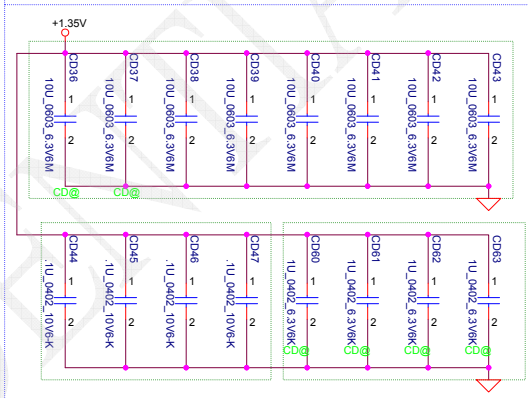
# DDR3 SO-DIMM B



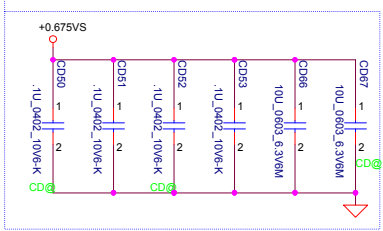
## Swap Table

Pin Number	Pin Name	Net Name
5	DQ0	DDR3_DQ17
7	DQ1	DDR3_DQ23
15	DQ2	DDR3_DQ18
17	DQ3	DDR3_DQ21
4	DQ4	DDR3_DQ16
6	DQ5	DDR3_DQ22
16	DQ6	DDR3_DQ19
18	DQ7	DDR3_DQ20
10	DQS#0	DDR3_DQS#2
12	DQS#0	DDR3_DQS#2
21	DQ8	DDR3_DQ3
23	DQ9	DDR3_DQ5
33	DQ10	DDR3_DQ6
35	DQ11	DDR3_DQ1
22	DQ12	DDR3_DQ2
24	DQ13	DDR3_DQ4
34	DQ14	DDR3_DQ0
36	DQ15	DDR3_DQ7
27	DQS#1	DDR3_DQS#0
29	DQS#1	DDR3_DQS#0
39	DQ16	DDR3_DQ8
41	DQ17	DDR3_DQ10
51	DQ18	DDR3_DQ14
53	DQ19	DDR3_DQ15
40	DQ20	DDR3_DQ13
42	DQ21	DDR3_DQ12
50	DQ22	DDR3_DQ9
52	DQ23	DDR3_DQ11
45	DQS#2	DDR3_DQS#1
47	DQS#2	DDR3_DQS#1
57	DQ24	DDR3_DQ27
59	DQ25	DDR3_DQ26
67	DQ26	DDR3_DQ28
69	DQ27	DDR3_DQ24
56	DQ28	DDR3_DQ31
58	DQ29	DDR3_DQ30
68	DQ30	DDR3_DQ29
70	DQ31	DDR3_DQ25
62	DQS#3	DDR3_DQS#3
64	DQS#3	DDR3_DQS#3
129	DQ32	DDR3_DQ33
131	DQ33	DDR3_DQ36
141	DQ34	DDR3_DQ39
143	DQ35	DDR3_DQ38
130	DQ36	DDR3_DQ37
132	DQ37	DDR3_DQ32
140	DQ38	DDR3_DQ35
142	DQ39	DDR3_DQ34
135	DQS#4	DDR3_DQS#4
137	DQS#4	DDR3_DQS#4
147	DQ40	DDR3_DQ40
149	DQ41	DDR3_DQ43
157	DQ42	DDR3_DQ42
159	DQ43	DDR3_DQ44
146	DQ44	DDR3_DQ45
148	DQ45	DDR3_DQ41
158	DQ46	DDR3_DQ46
160	DQ47	DDR3_DQ47
152	DQS#5	DDR3_DQS#5
154	DQS#5	DDR3_DQS#5
163	DQ48	DDR3_DQ52
165	DQ49	DDR3_DQ51
175	DQ50	DDR3_DQ50
177	DQ51	DDR3_DQ48
164	DQ52	DDR3_DQ49
166	DQ53	DDR3_DQ53
174	DQ54	DDR3_DQ54
176	DQ55	DDR3_DQ55
169	DQS#6	DDR3_DQS#6
171	DQS#6	DDR3_DQS#6
181	DQ56	DDR3_DQ62
183	DQ57	DDR3_DQ57
191	DQ58	DDR3_DQ59
193	DQ59	DDR3_DQ63
180	DQ60	DDR3_DQ56
182	DQ61	DDR3_DQ61
192	DQ62	DDR3_DQ58
194	DQ63	DDR3_DQ60
186	DQS#7	DDR3_DQS#7
188	DQS#7	DDR3_DQS#7

Layout Note: Place near DIMM (10uF\_0603\_6.3V)\*8 (1U\_0402\_6.3V)\*8 (.1U\_0402\_10V6-K)\*4



Layout Note: Place near DIMM (10U\_0603\_6.3V)\*2 (.1U\_0402\_10V)\*4




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Date:	Thursday, December 19, 2013	Sheet	17	of 59

## Power-Up/Down Sequence

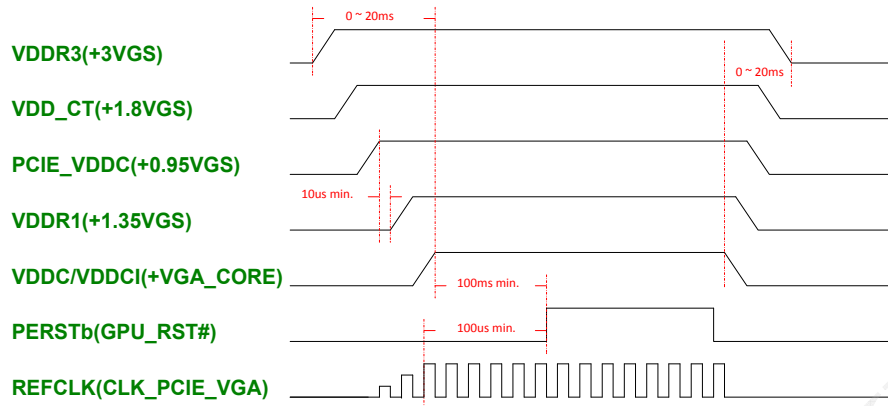
"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.

It is recommended that the 3.3-V rail ramp up first. The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μs before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as  $\leq 50$  mV/μs).

For power down, reversing the ramp-up sequence is recommended.



## CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

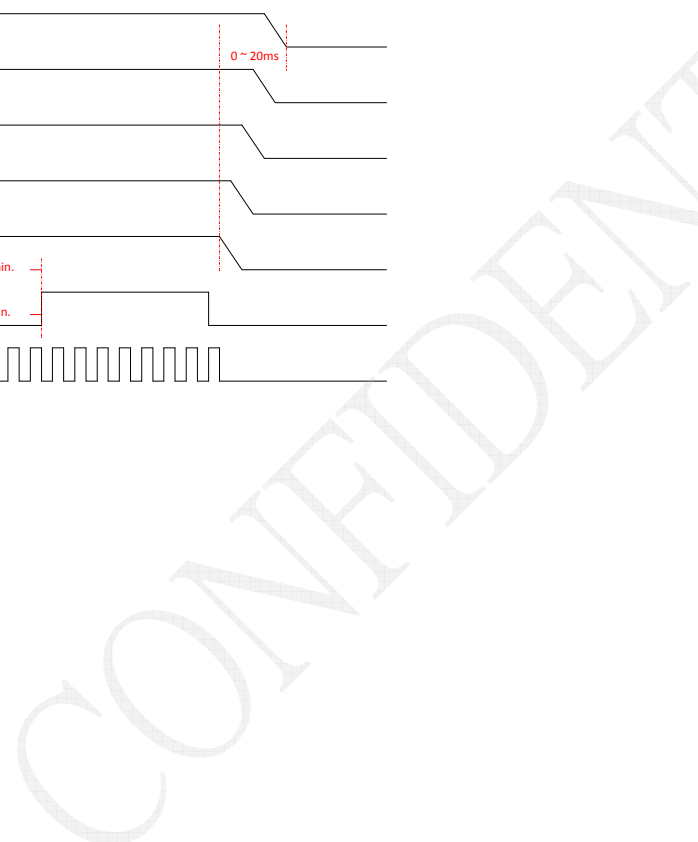
RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1= INSTALL 10K RESISTOR  
X = DESIGN DEPENDANT  
NA = NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0.  100 = 256MB	X
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 0= Not support	X
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	X
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	X
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 000 = Hynix 256M*16 001 = Hynix 128M*16 100 = Samsung 256M*16 011 = Samsung 128M*16 010 = Micron 256M*16 111 = Micron 128M*16	X
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	11

## VRAM ID config

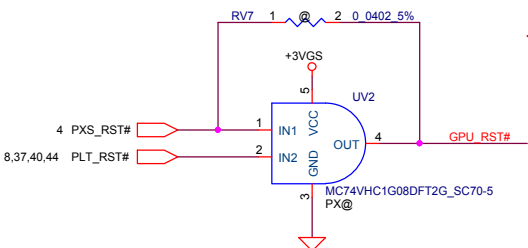
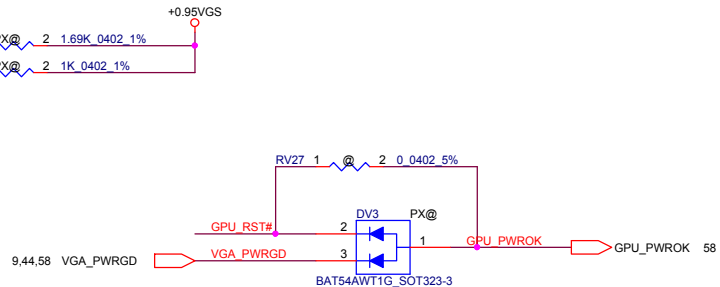
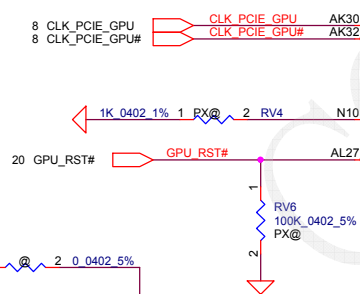
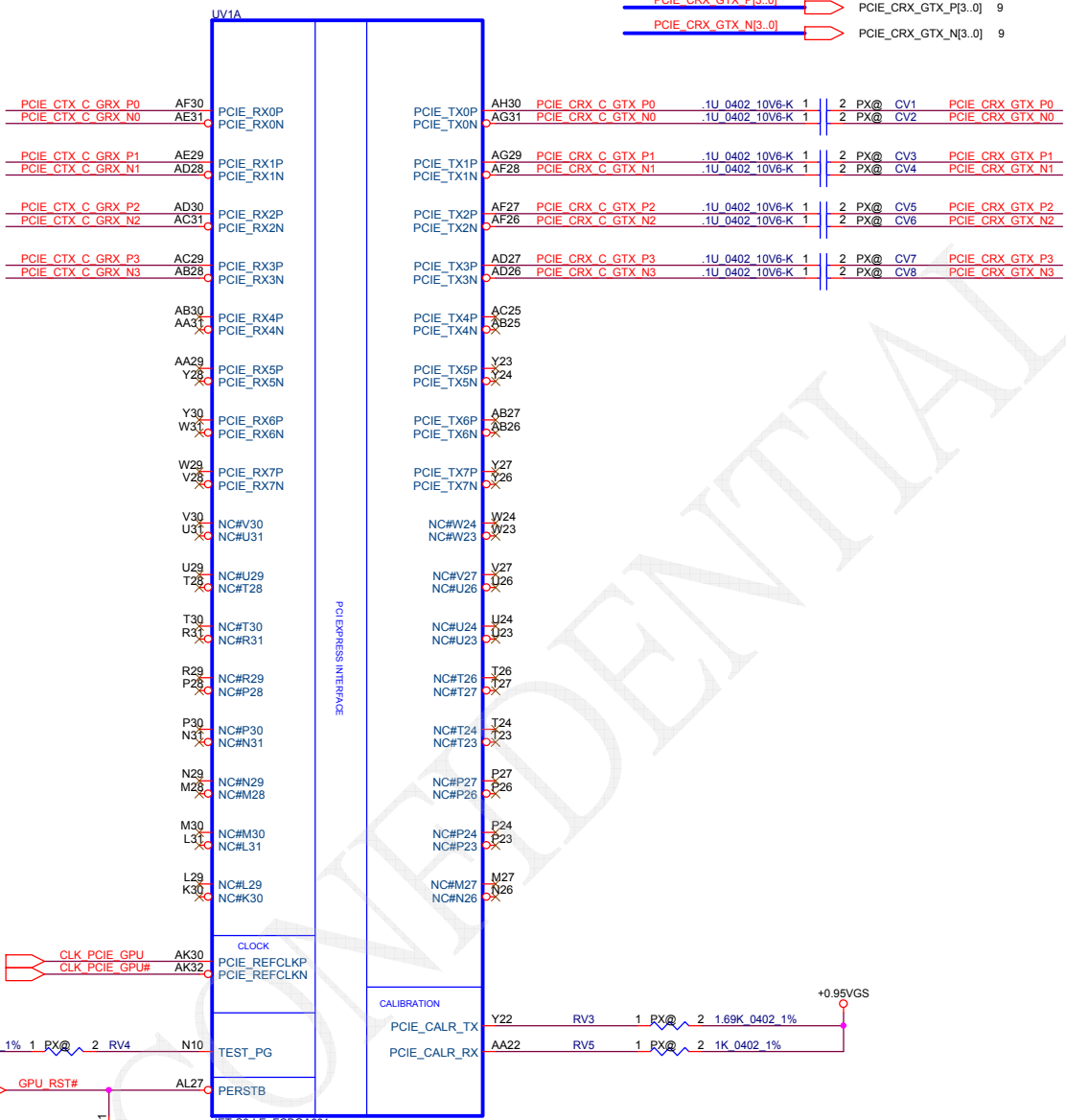
Memory Type		VRAM ID PS_3[3:1]	PU resistor RV33	PD resistor RV36
128Mx16	Hynix H5TC2G63FFR-11C	100	4.53K	4.99K
	Micron MT41J128M16JT-093G	111	4.75K	NC
	Samsung K4W2G1646Q-BC1A	110	3.4K	10K
256Mx16	Hynix H5TC4G63AFR-11C	000	NC	4.75K
	Micron MT41J256M16HA-093G	010	4.53K	2K
	Samsung K4W4G1646D-BC1A	001	8.45K	2K
	Micron MT41K256M16HA-107G	011	6.98K	4.99K

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				Customer	1.0
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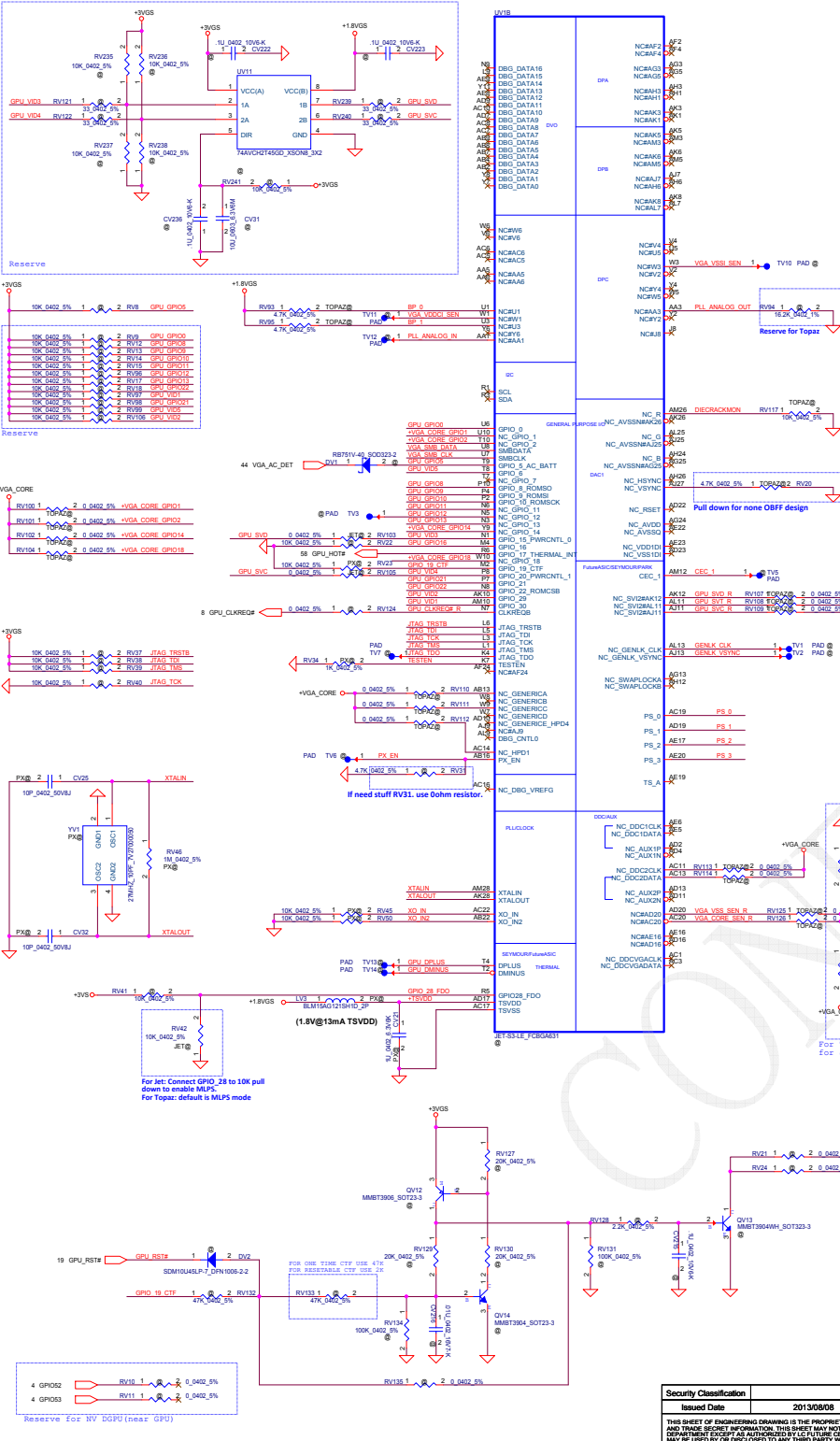


9 PCIE\_CTX\_C\_GRX\_P[3..0] PCIE\_CTX\_C\_GRX\_P[3..0]  
 9 PCIE\_CTX\_C\_GRX\_N[3..0] PCIE\_CTX\_C\_GRX\_N[3..0]

PCIE\_CRX\_GTX\_P[3..0] PCIE\_CRX\_GTX\_P[3..0] 9  
 PCIE\_CRX\_GTX\_N[3..0] PCIE\_CRX\_GTX\_N[3..0] 9



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Size A3	Document Number	ACLU1 & ACLU2		Rev	1.0
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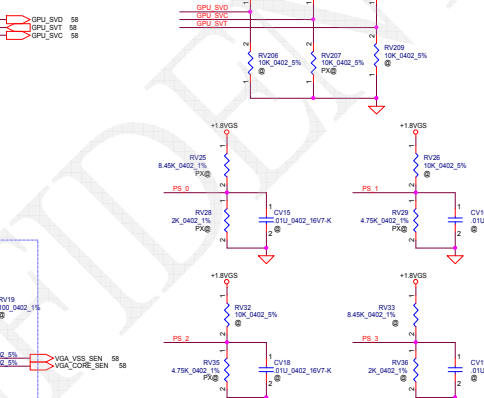


### CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

MIPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[0]	NCM_CONFIG[0]	Define the ROM type when STRAP_BIOS_ROM_EN = 1	X
PS_0[1]	NCM_CONFIG[1]	Define the primary memory architecture when STRAP_BIOS_ROM_EN = 0.	100 = 2GBRAM
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINS[0]	The LSB (least significant bit) of the strap option that indicates the number of auto-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported 0 = PCIe GEN3 is not supported.	On Not support X
PS_1[2]	STRAP_BIF_CLK_PM_LEN	0 = The CLKREQ power management capability is disabled 1 = The CLKREQ power management capability is enabled.	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CPD_DRV_FULL_SWING	0 = The transmitter full-swing is enabled 1 = The transmitter full-swing is disabled.	1
PS_1[5]	STRAP_TX_DEEMPH_LEN	0 = Tx deemphasis disabled 1 = Tx deemphasis enabled.	1 Enable X
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	1 = Disable the external BIOS ROM device 0 = Enable the external BIOS ROM device.	On Disable X
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved.	1
PS_3[1]	BOARD_CONFIG[0]	Board configuration related strap, such as for memory ID	X
PS_3[2]	BOARD_CONFIG[1]	00 = Hynix 55M16 01 = Hynix 128M16	
PS_3[3]	BOARD_CONFIG[2]	00 = Samsung 25M16 01 = Samsung 128M16 10 = Micron 25M16 11 = Micron 128M16	
PS_3[4]	AUD_PORT_CONN_PINS[1]	Determines the maximum number of digital display auto endpoints that will be presented to the OS and user (Constitute with PS_0[5])	11 = No usable endpoints. 10 = One usable endpoint. 01 = Two usable endpoints. 00 = Three usable endpoints. 00 = Four usable endpoints. 00 = Five usable endpoints. 00 = Six usable endpoints. 00 = 7+ endpoints are usable.
PS_3[5]	AUD_PORT_CONN_PINS[2]		11

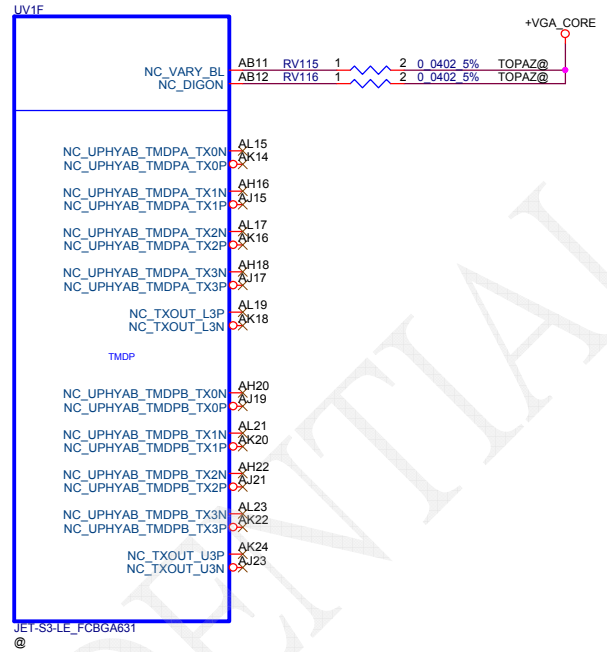
SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4900	011
4530	4900	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

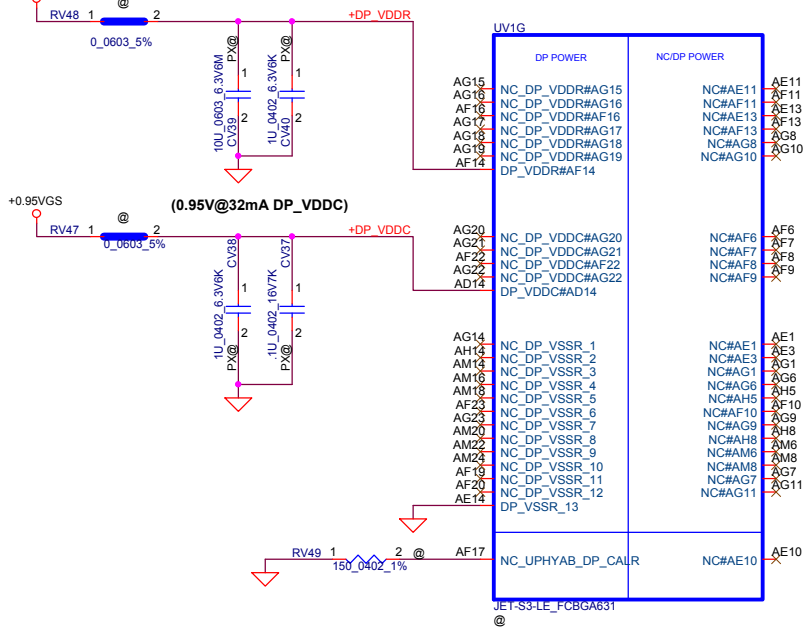


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+1.8VGS @ (1.8V@40mA DP\_VDDR)

+0.95VGS @ (0.95V@32mA DP\_VDDC)



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Date:	Thursday, December 19, 2013	Sheet	22	of 59			

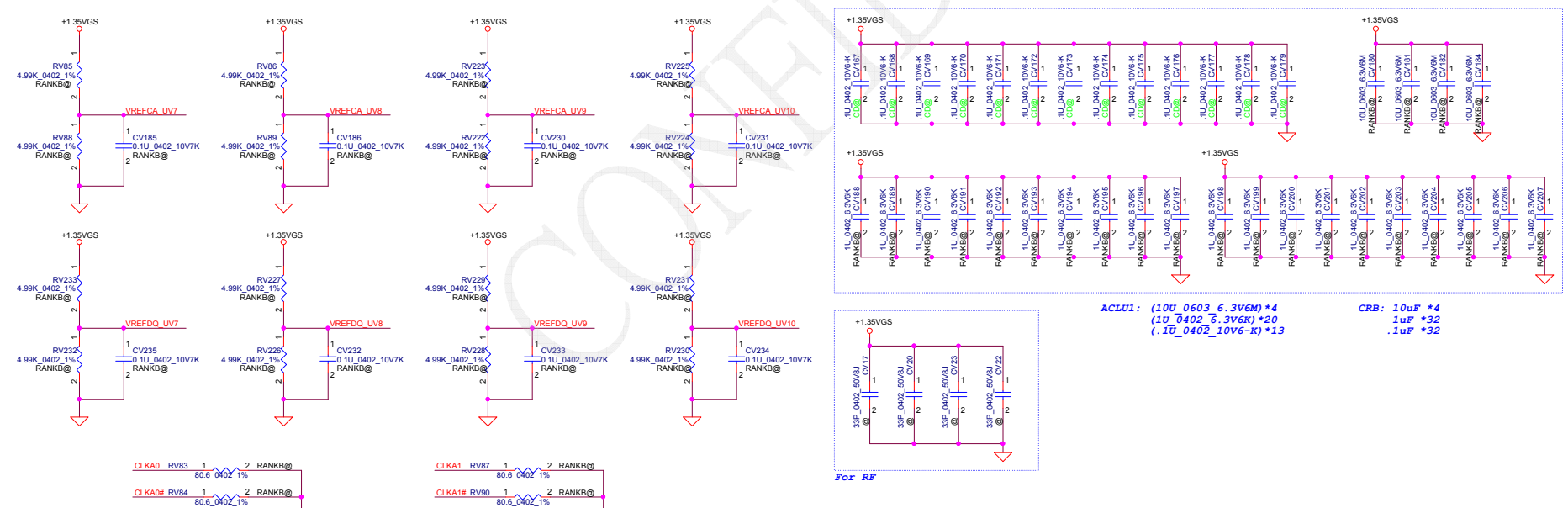
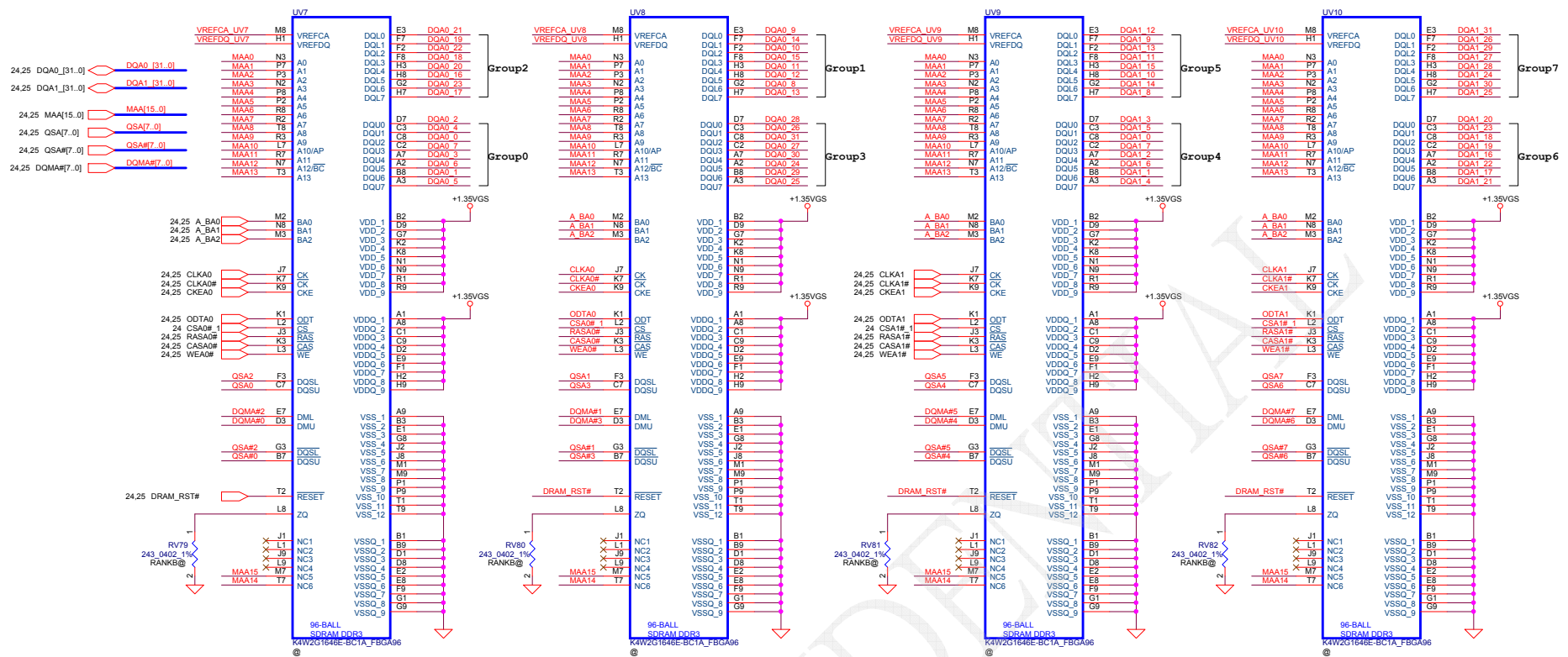













ACLUI: (10U\_0603\_6\_3V6M)\*4  
 (1U\_0402\_6\_3V6K)\*20  
 (.1U\_0402\_10V6-K)\*13

CRB: 10uF \*4  
 1uF \*32  
 .1uF \*32


For RF

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				Date:	Thursday, December 19, 2013	Sheet 29 of 59




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				Date:	Thursday, December 19, 2013	Sheet 30 of 59

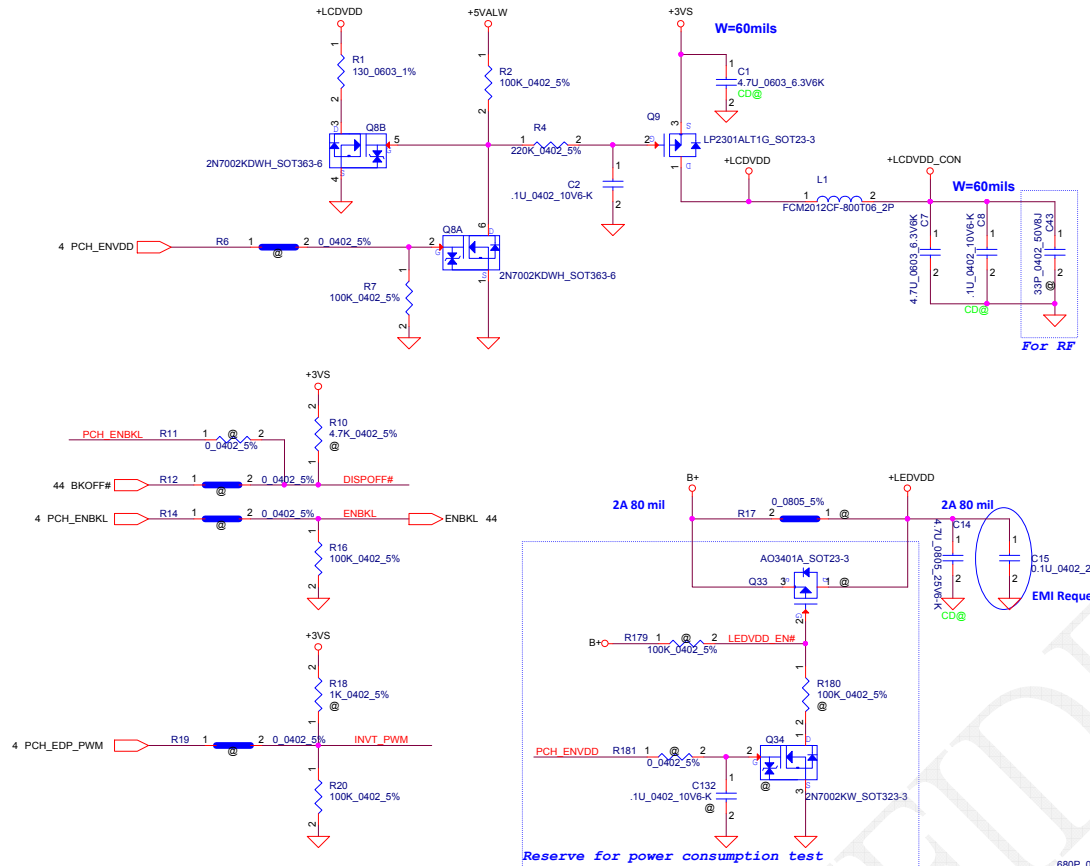
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Size	Document Number	Rev		
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Date:	Thursday, December 19, 2013	Sheet	31	of 59

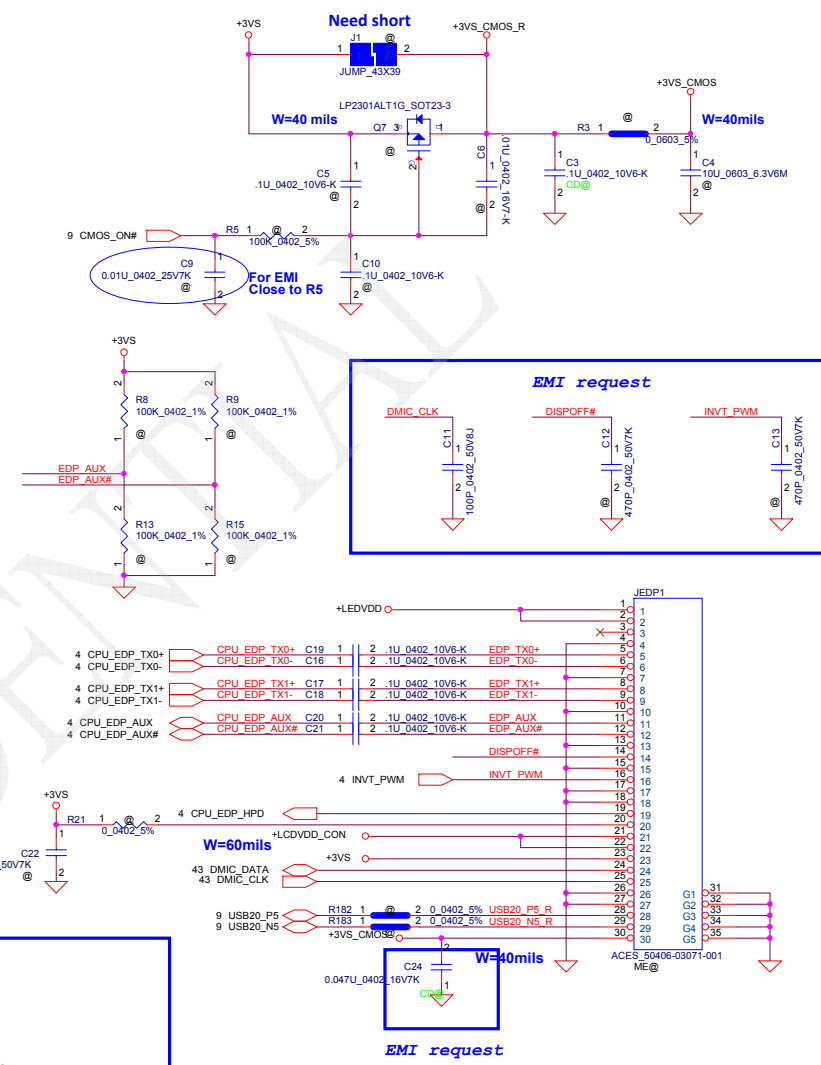
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	
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Size	Document Number	Rev		
Custom	<b>ACL01 &amp; ACL02</b>	1.0		
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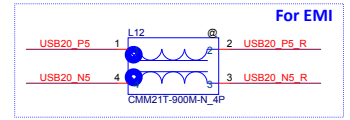
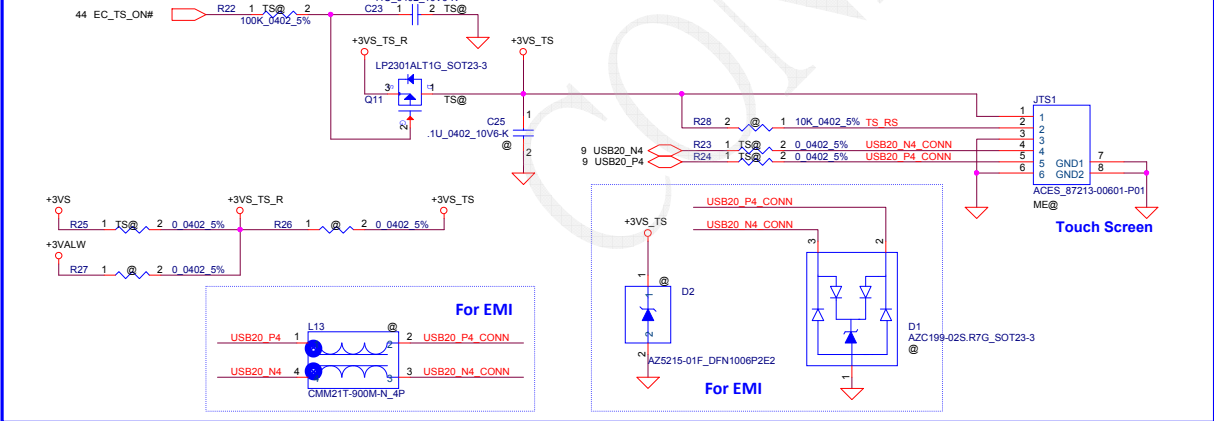
### LCD POWER CIRCUIT

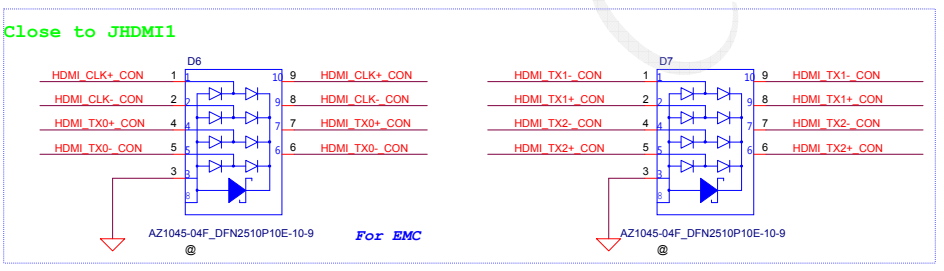
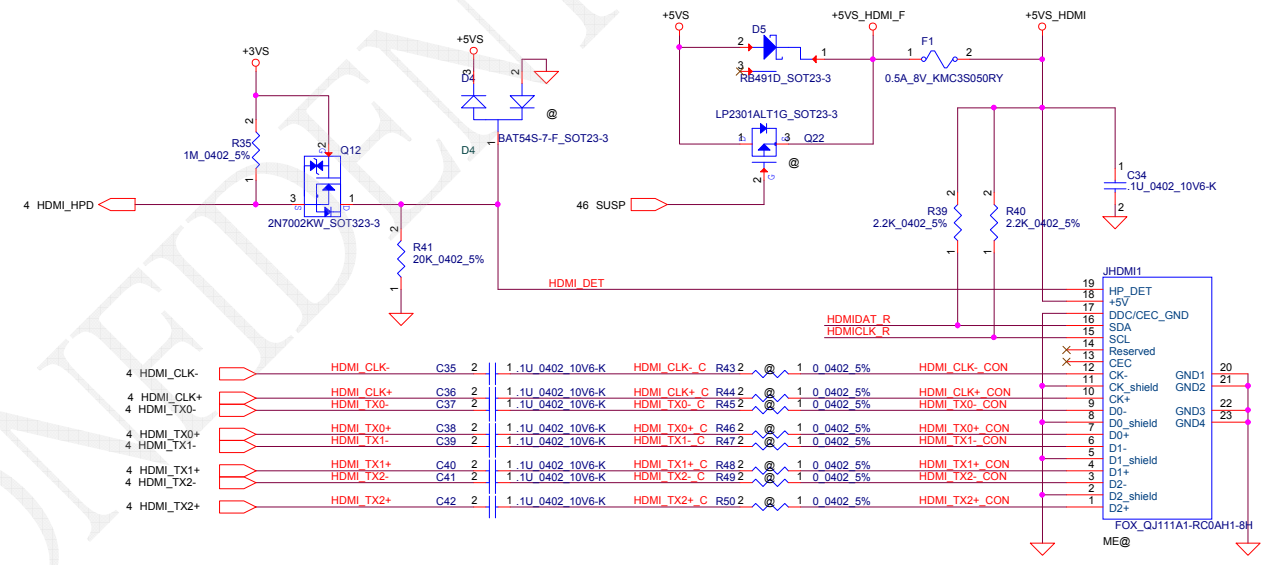
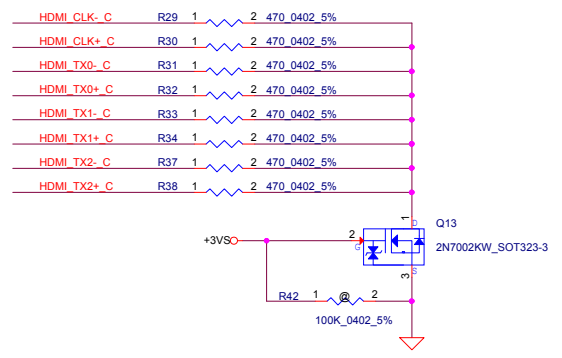
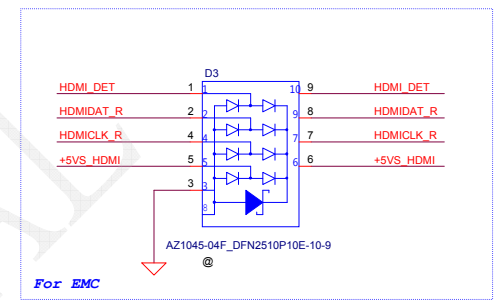
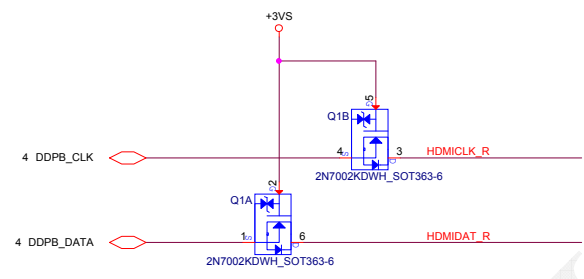
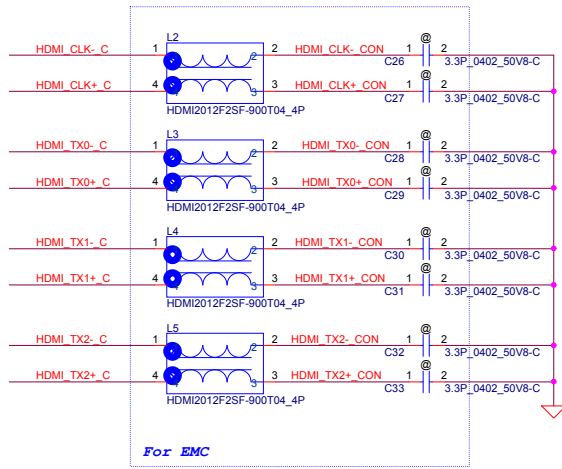


### CMOS Camera

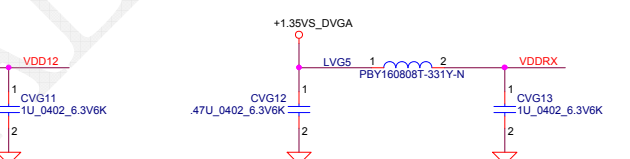
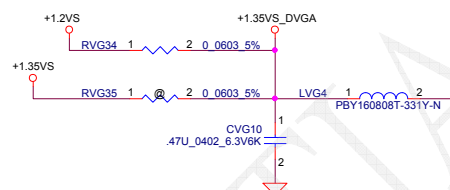
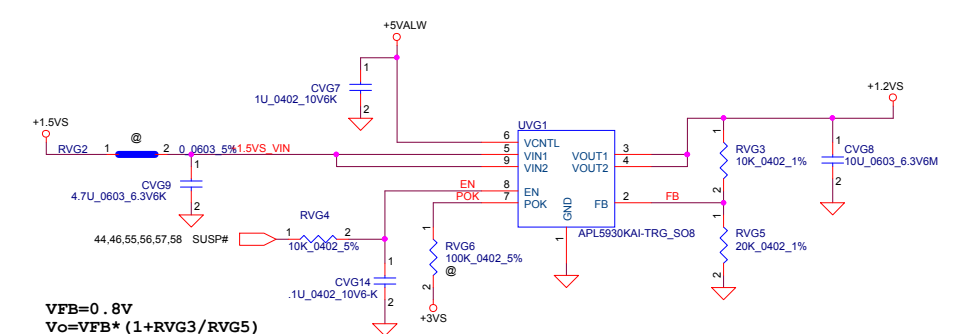
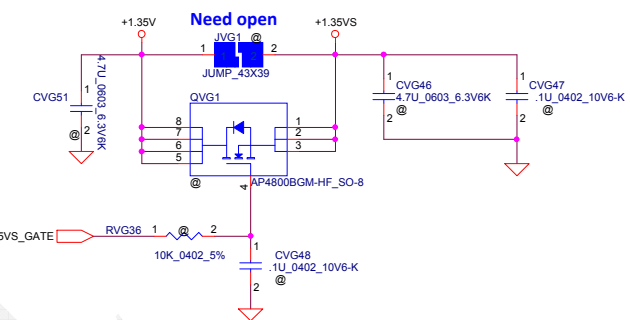
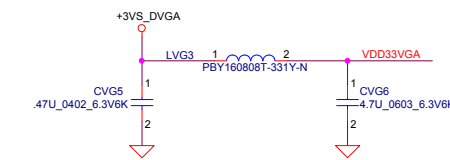
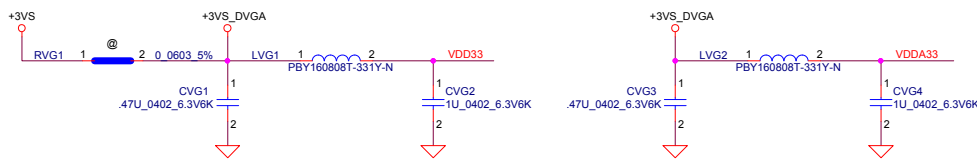


### Touch Screen

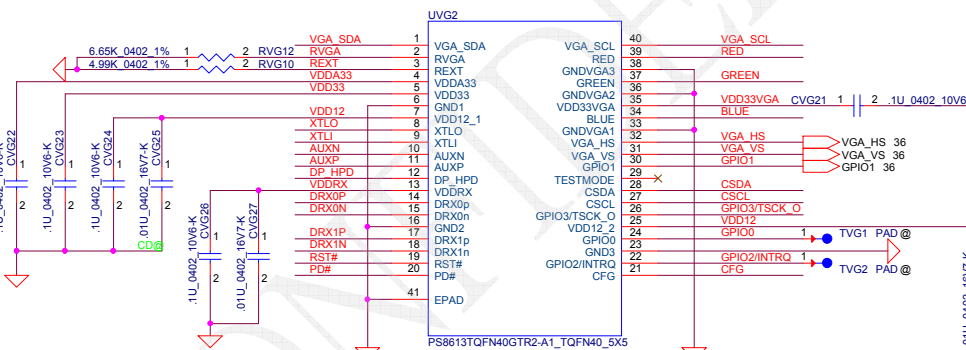
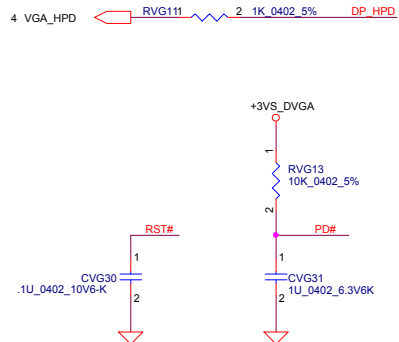
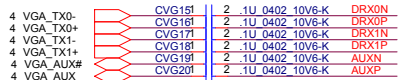




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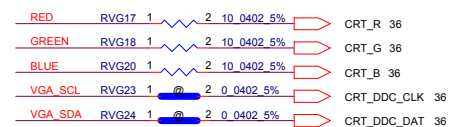
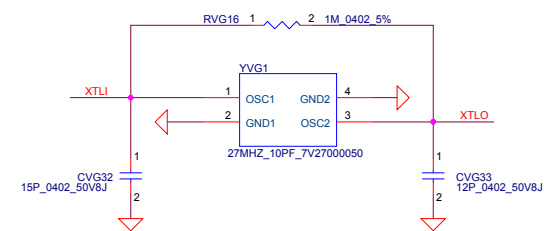
VFB=0.8V  
 $V_o = VFB * (1 + RVG3 / RVG5)$   
 OCP: Min 4A



Update DP Convert Version from A0 to A1

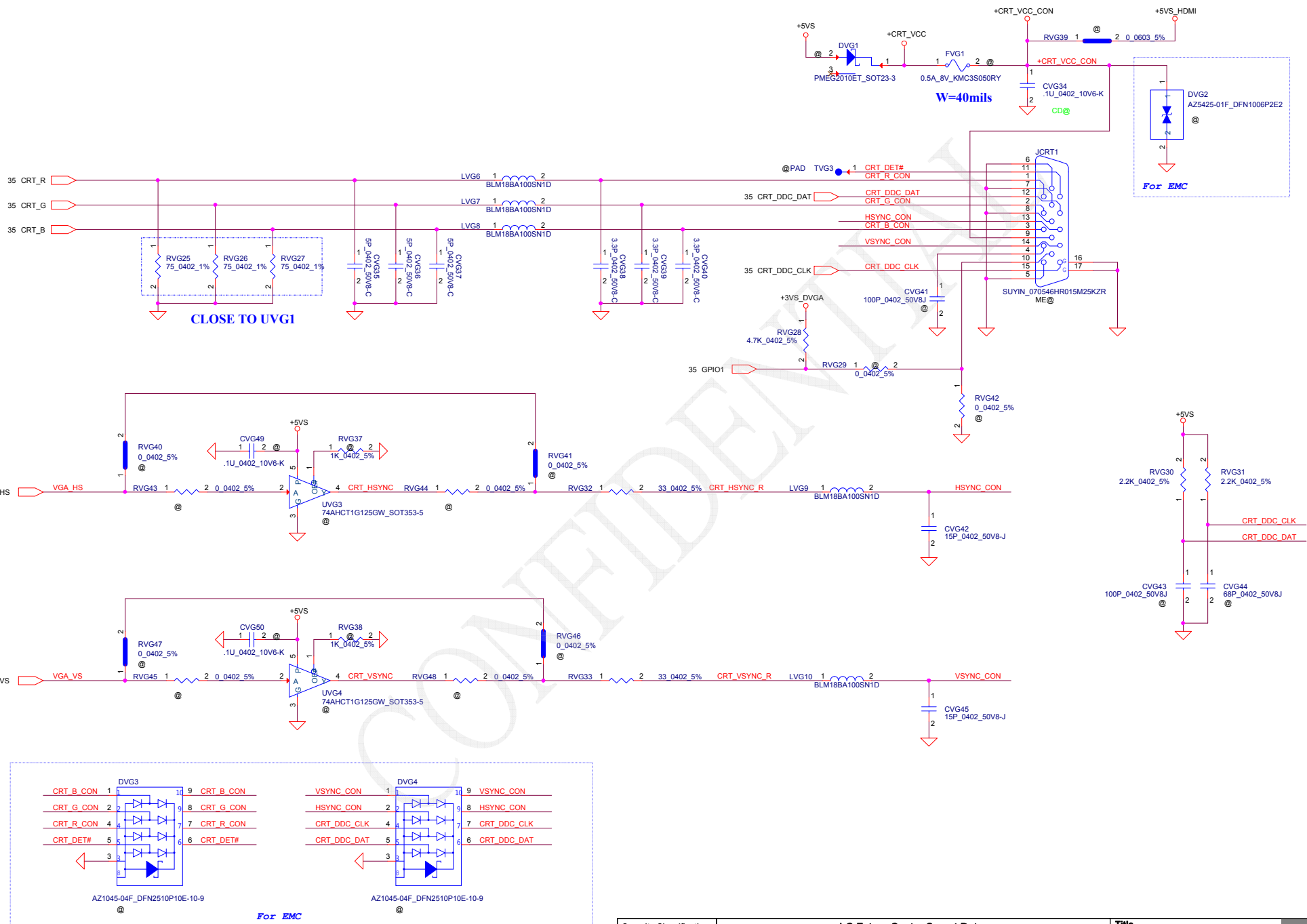
Initial code loading selection, internal pull down ~80kΩ:  
 L: Loading initial code from internal MTP ROM  
 H: No initial code loading, external I2C control is expected

I2C address, 3-state inputs:  
 L: 0x50h ~ 0x6Fh  
 M: 0x90h ~ 0xAFh  
 H: 0x30h ~ 0x4Fh



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Custom	<b>ACL U1 &amp; ACL U2</b>		Date: Thursday, December 19, 2013   Sheet 35 of 59

# CRT Connector



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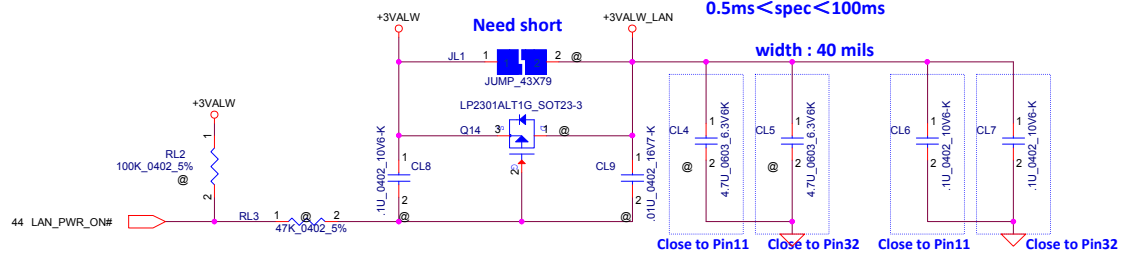
Size	Document Number	Rev
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**+3VALW TO +3VALW\_LAN**

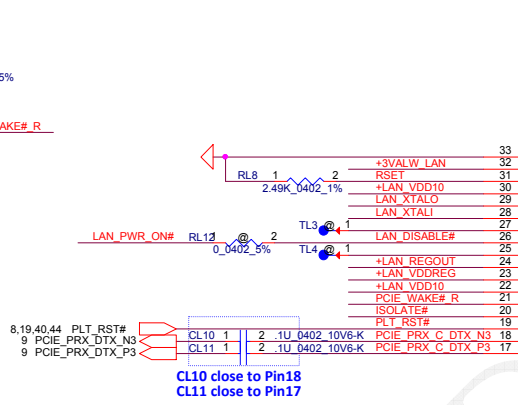
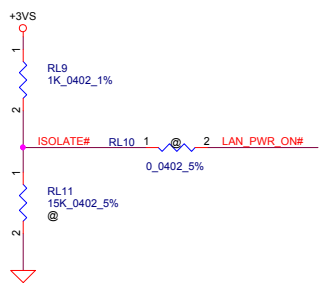
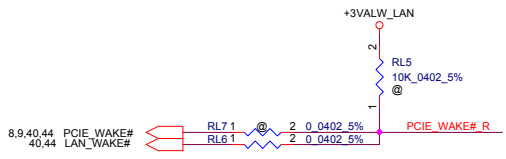
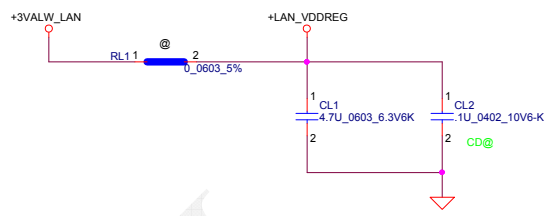
**+3VALW\_LAN rising time (10%~90%):  
0.5ms < spec < 100ms**



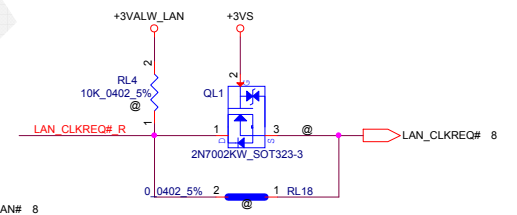
**Need short**

**width : 40 mils**

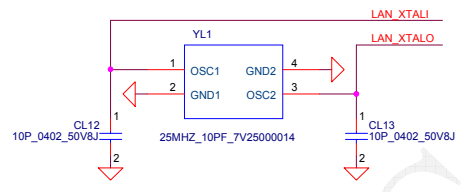
**Close to Pin11    Close to Pin32    Close to Pin11    Close to Pin32**



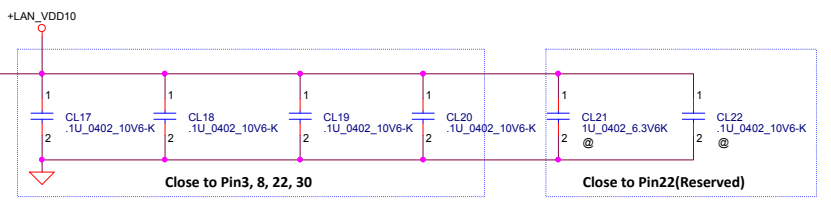
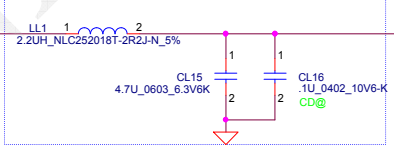
**CL10 close to Pin18  
CL11 close to Pin17**



**For RTL8111GUL/RTL8106EUL (SWR mode)**



**+LAN\_REGOUT**



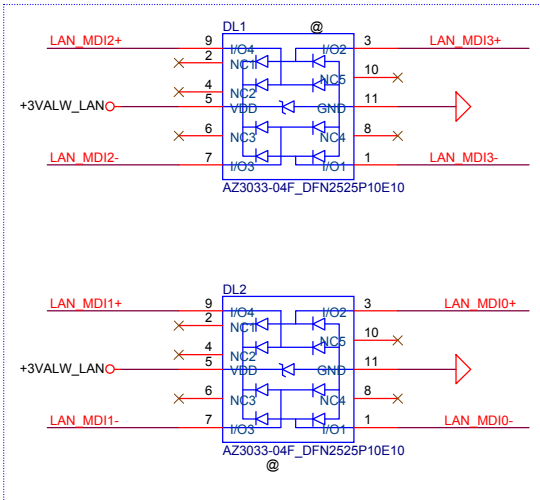
**Layout Note: LL1 must be within 200mil to Pin24,  
CL15,CL16 must be within 200mil to LL1  
+LAN\_REGOUT: Width =60mil**

**Close to Pin3, 8, 22, 30**

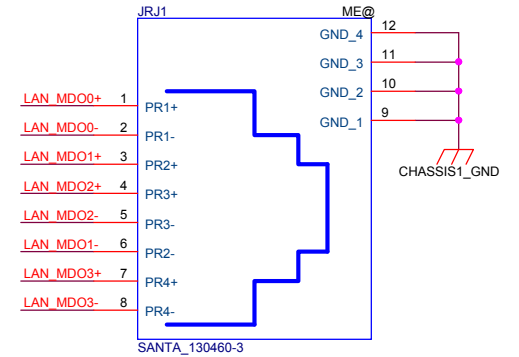
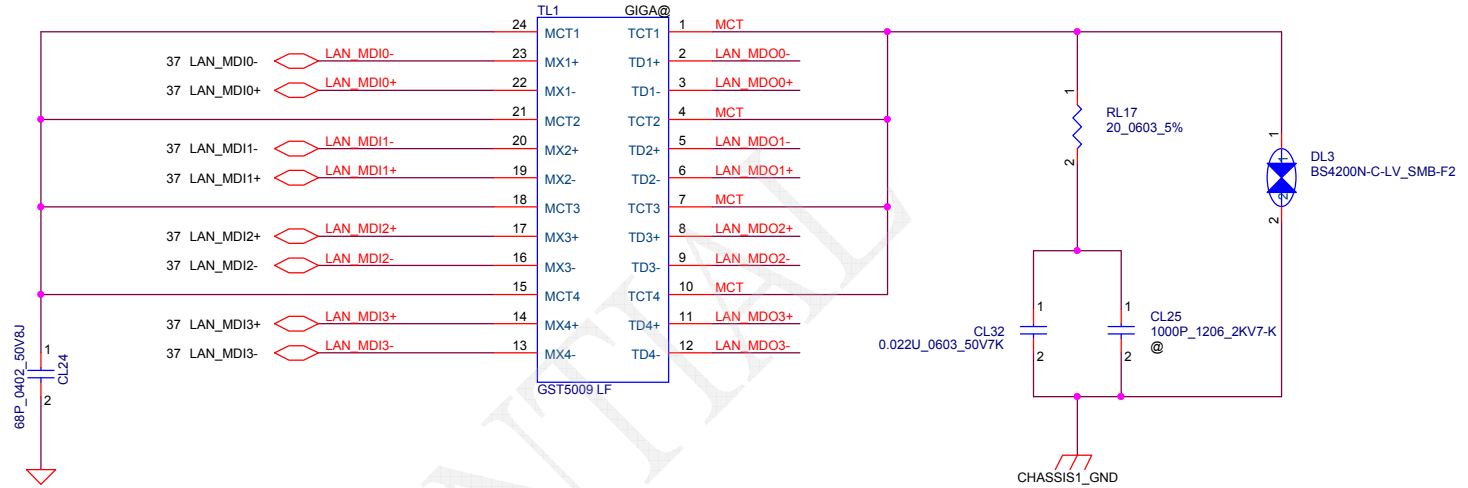
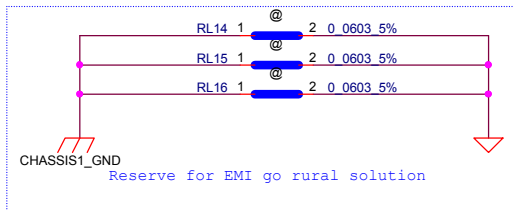
**Close to Pin22(Reserved)**

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DL1/DL2  
1'S PN:SC300003M00

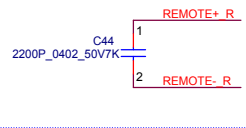


Place Close to TL1

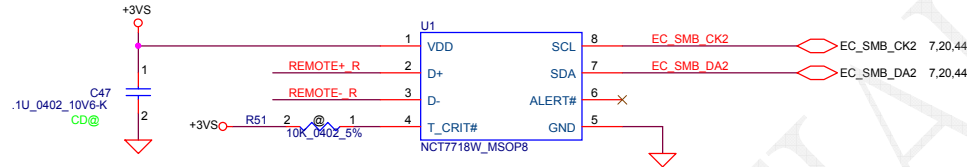


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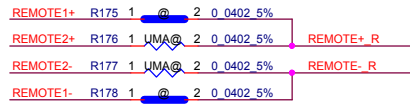
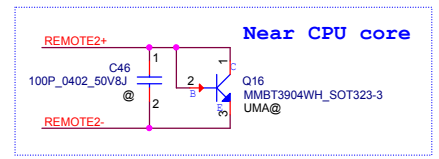
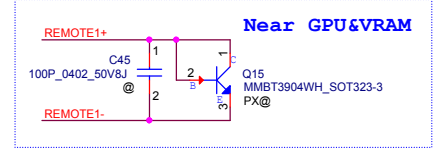
**Close to U1**



**SMSC thermal sensor placed near DIMM**

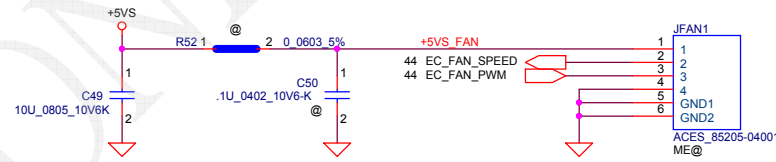


Address 1001\_100xb



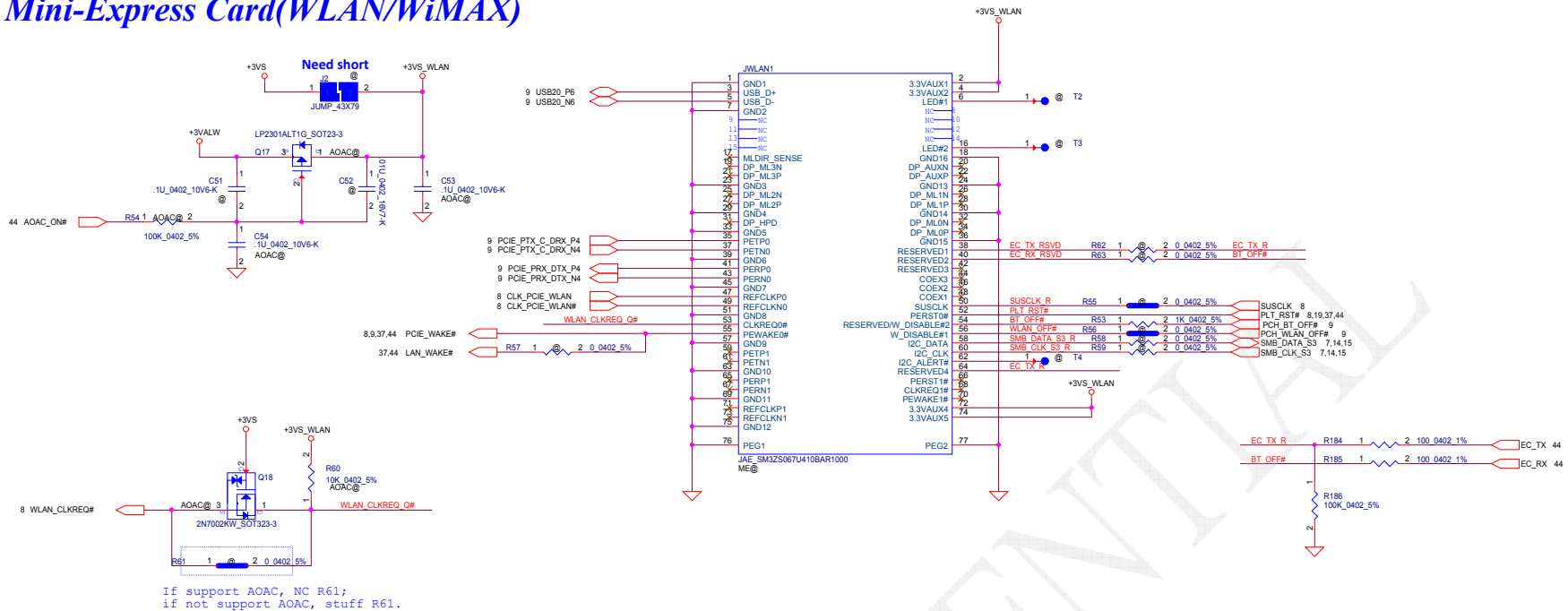
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

**FAN Conn**



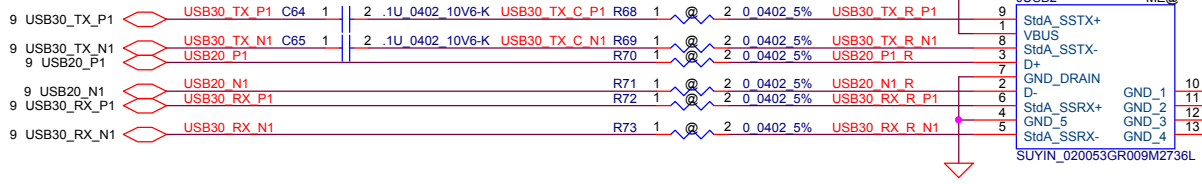
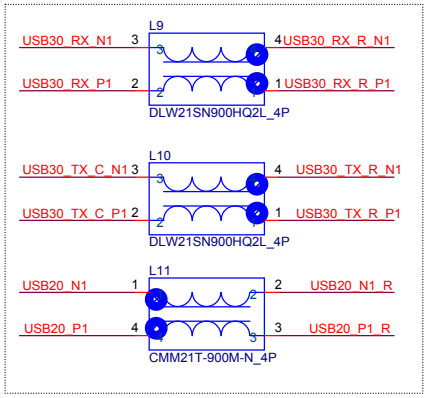
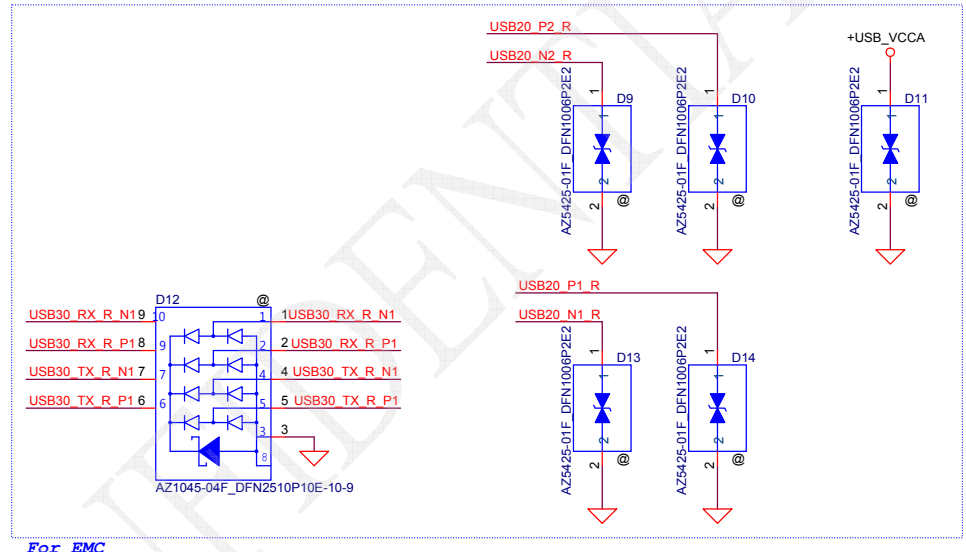
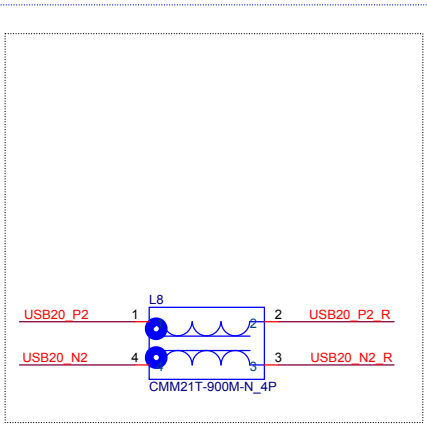
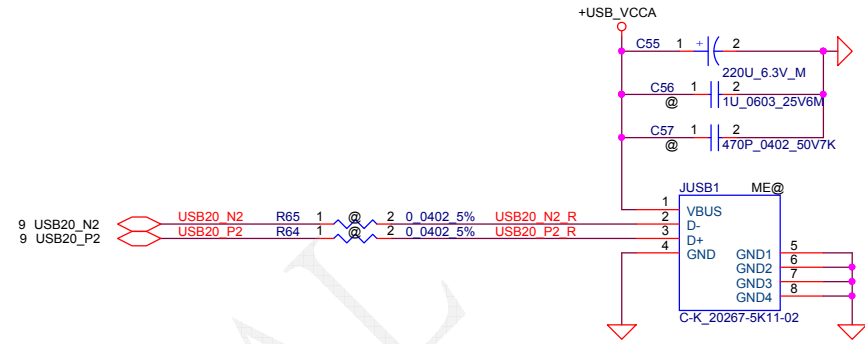
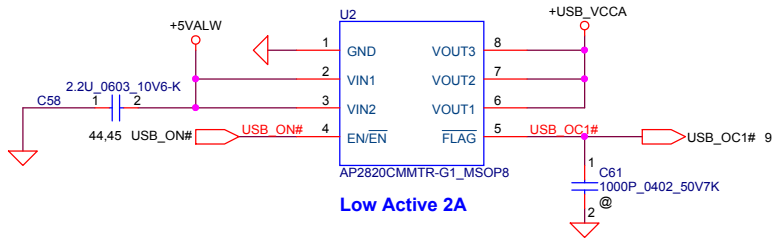
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Thermal sensor/FAN CONN	
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# Mini-Express Card(WLAN/WiMAX)



CONFIDENTIAL

# LEFT SIDE USB3.0 PORT X2



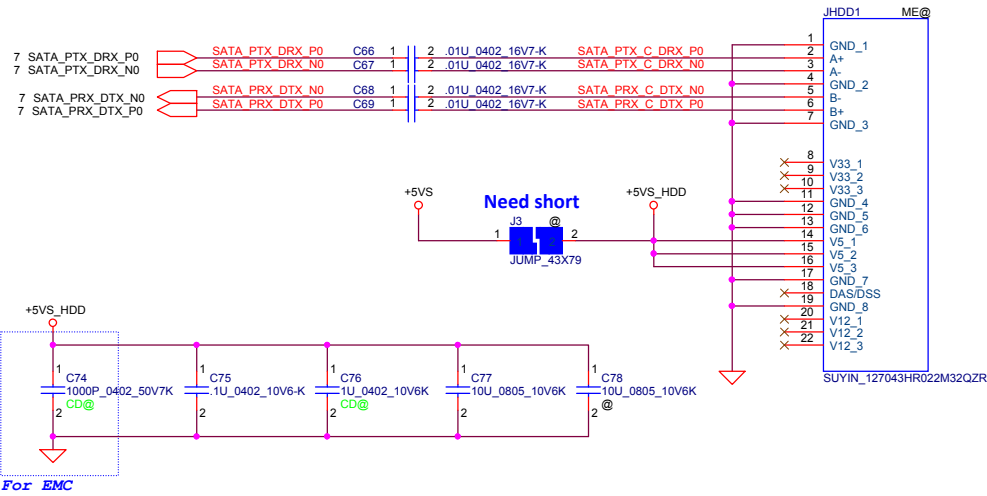
9 USB30_TX_P1	USB30_TX_P1	C64	1	2	.1U_0402_10V6-K	USB30_TX_C_P1	R68	1	@	2	0	0402	5%	USB30_TX_R_P1
9 USB30_TX_N1	USB30_TX_N1	C65	1	2	.1U_0402_10V6-K	USB30_TX_C_N1	R69	1	@	2	0	0402	5%	USB30_TX_R_N1
9 USB20_P1	USB20_P1						R70	1	@	2	0	0402	5%	USB20_P1_R
9 USB20_N1	USB20_N1						R71	1	@	2	0	0402	5%	USB20_N1_R
9 USB30_RX_P1	USB30_RX_P1						R72	1	@	2	0	0402	5%	USB30_RX_R_P1
9 USB30_RX_N1	USB30_RX_N1						R73	1	@	2	0	0402	5%	USB30_RX_R_N1

For EMC

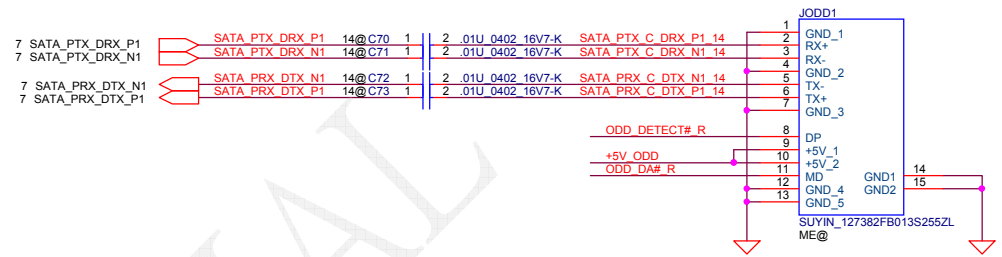
For EMC

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Issued Date		2013/08/08		Deciphered Date		2013/08/05		USB2.0/USB3.0 PORT (LEFT)			
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Size								Document Number		Rev	
Date								Thursday, December 19, 2013		Sheet 41 of 59	
								Custom		ACLU1 & ACLU2	

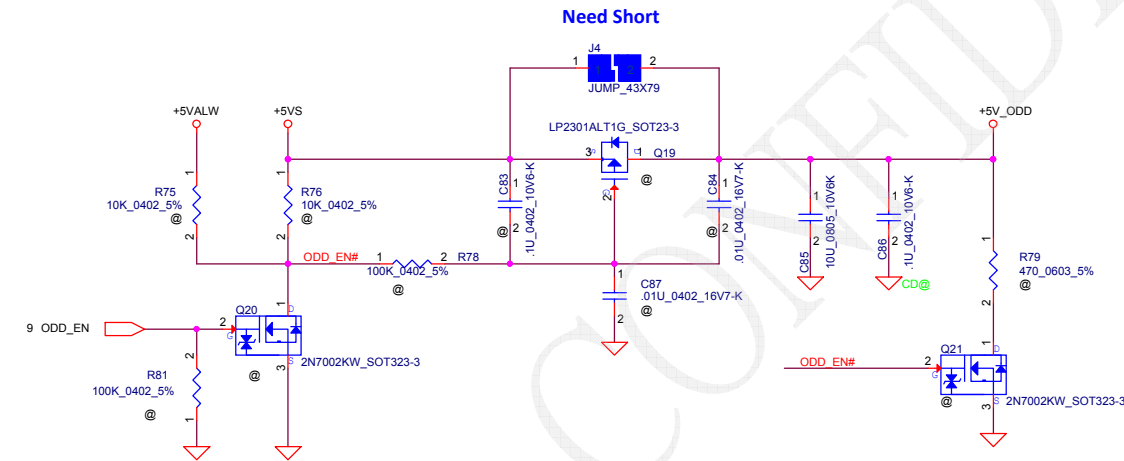
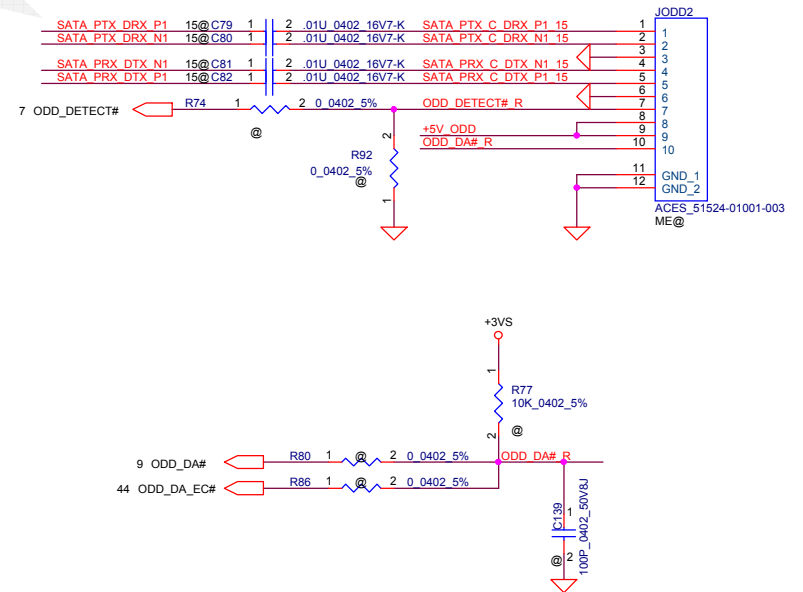
### SATA HDD Conn.



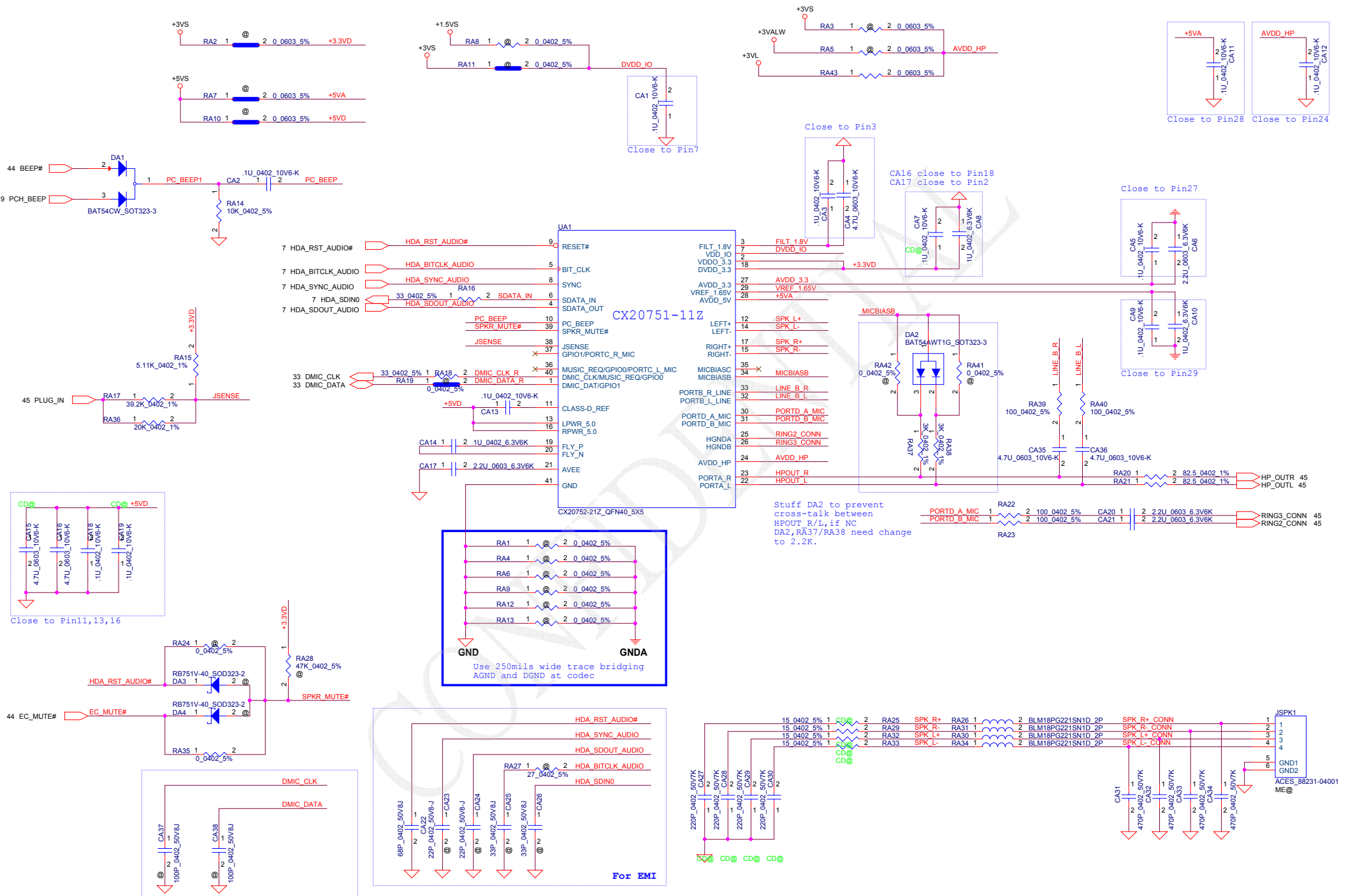
### FOR 14" SATA ODD Conn.



### FOR 15" SATA ODD FFC Conn



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				Custom		ACLU1 & ACLU2		1.0	
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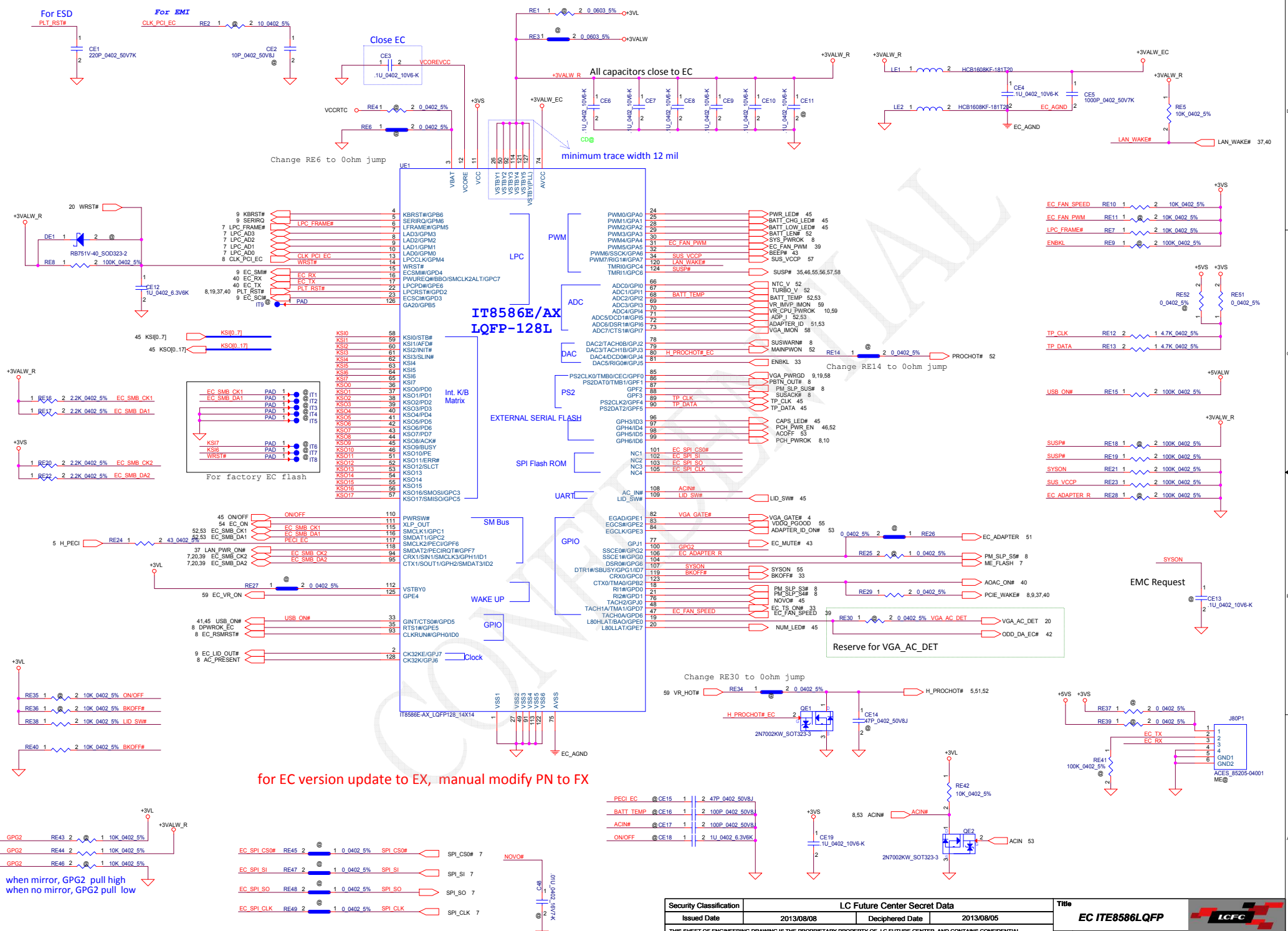
Security Classification	LC Future Center Secret Data	
Issued Date	2013/08/08	Deciphered Date
		2013/08/05

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Title	Revision
Codec_CX20752	1.0
Document Number	Rev
Custom	1.0
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ACLU1 & ACLU2



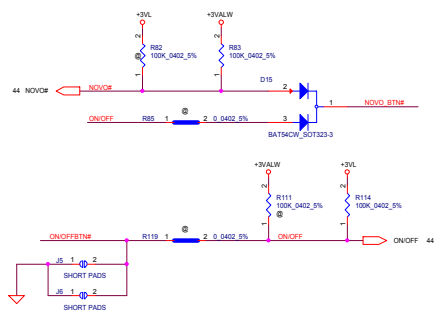
for EC version update to EX, manual modify PN to FX

when mirror, GPG2 pull high  
when no mirror, GPG2 pull low

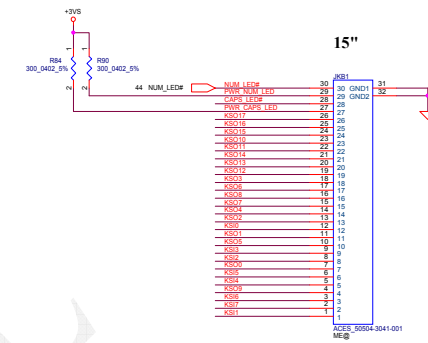
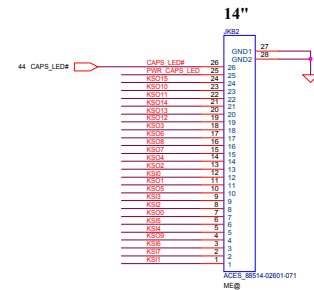
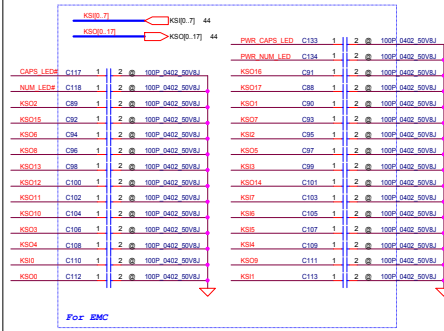
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	EC ITE8586LQFP	
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Size	C	Document Number	ACL01 & ACL02	Rev	1.0
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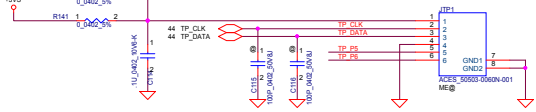
### ON/OFF switch



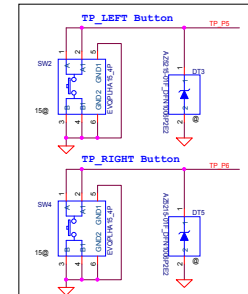
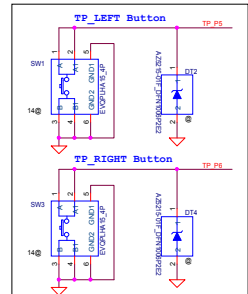
### K/B Connector



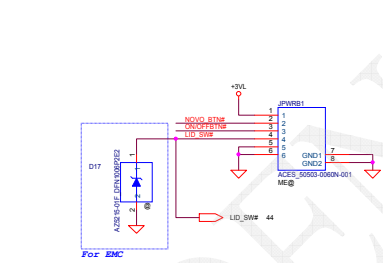
### TP/B Connector



For 14"		For 15"	
1	VDD	1	VDD
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	GND
5	TP-L	5	TP-L
6	TP-R	6	TP-R

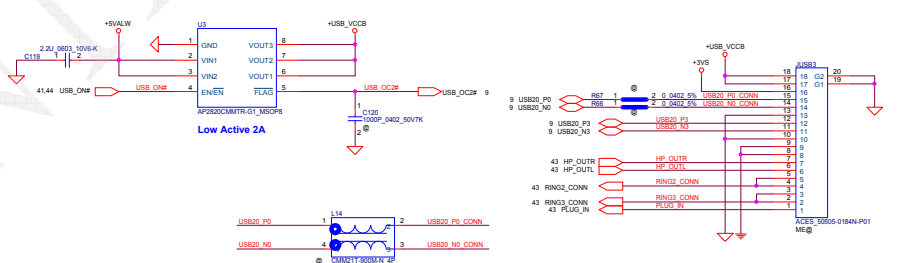


### PWR/B Connector

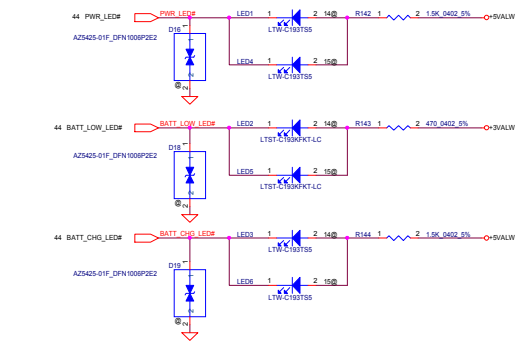


### USB I/O Connector

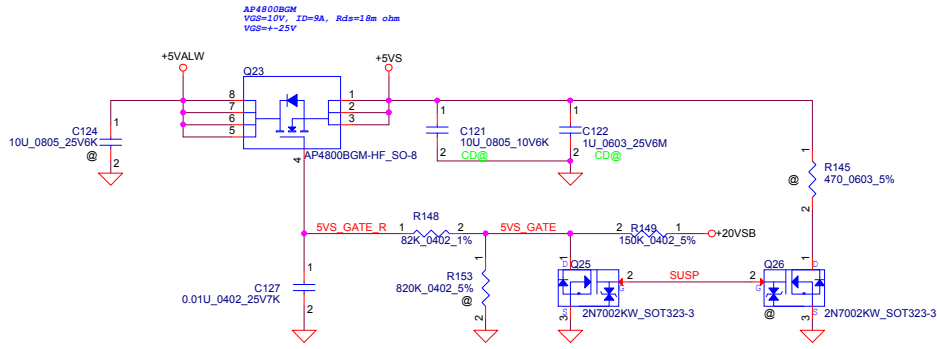
#### Right Side USB2.0 Port X 1 (USB/B)



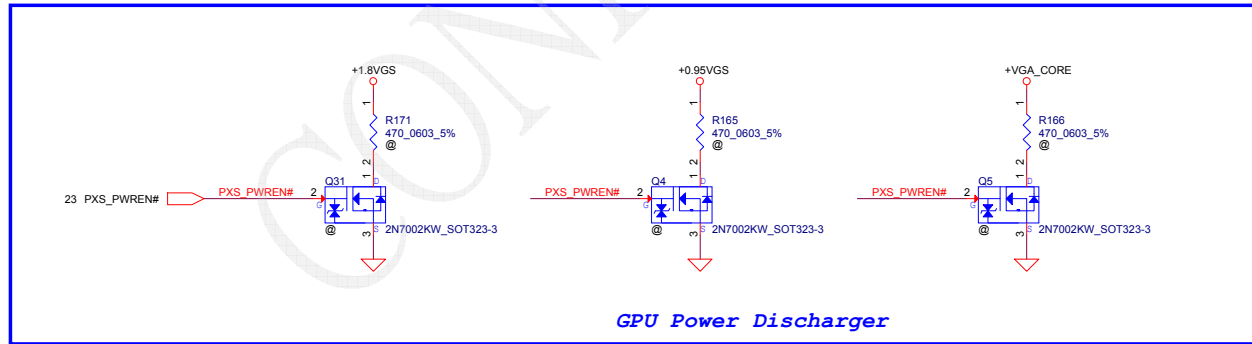
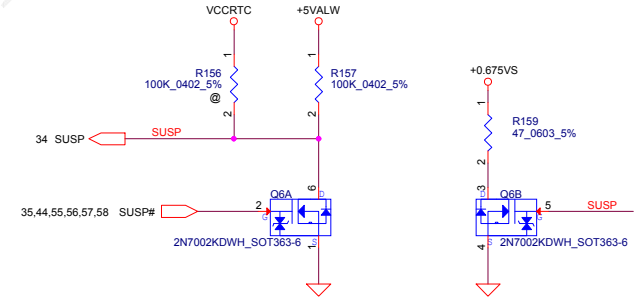
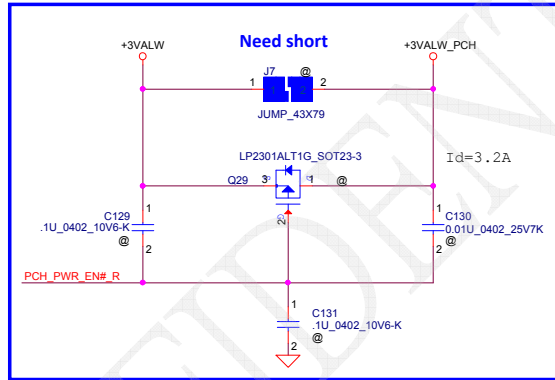
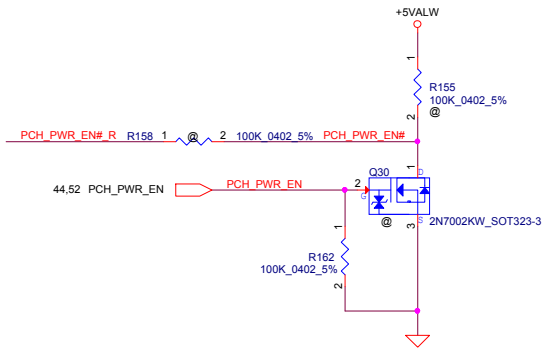
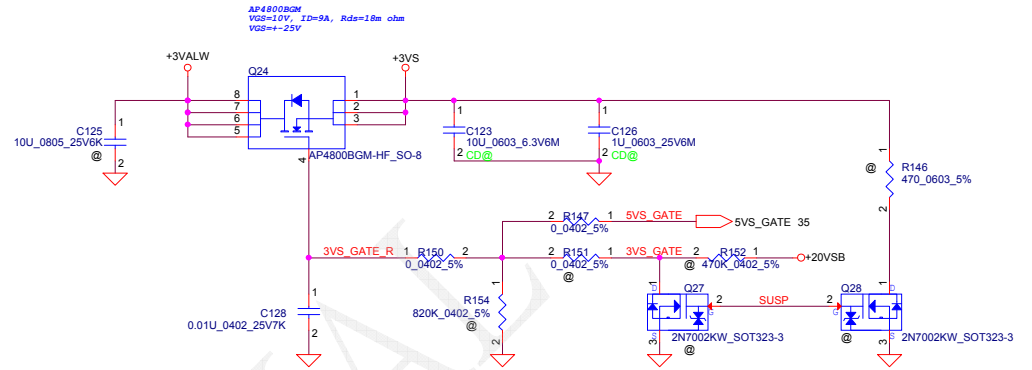
### LED




**+5VALW to +5VS**

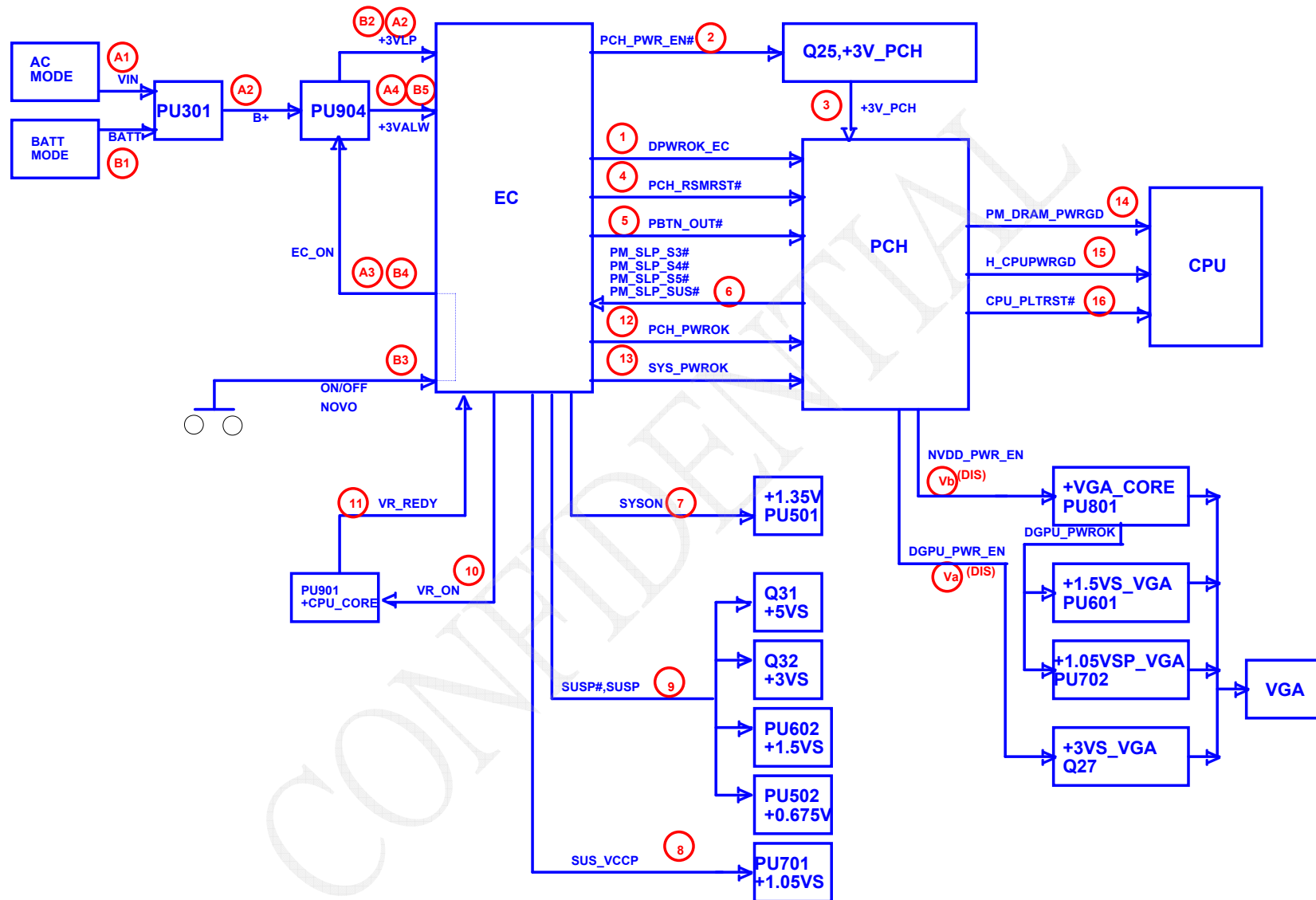


**+3VALW to +3VS**



**GPU Power Discharger**

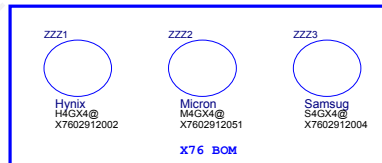
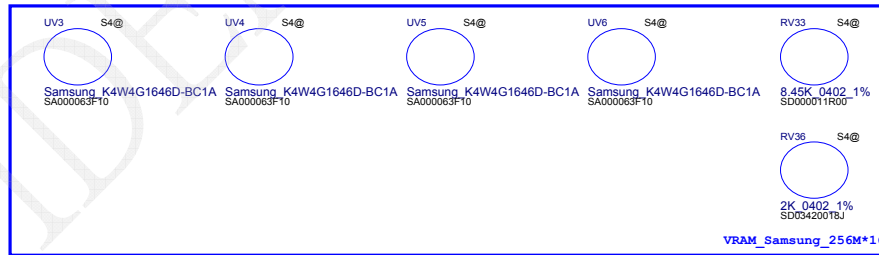
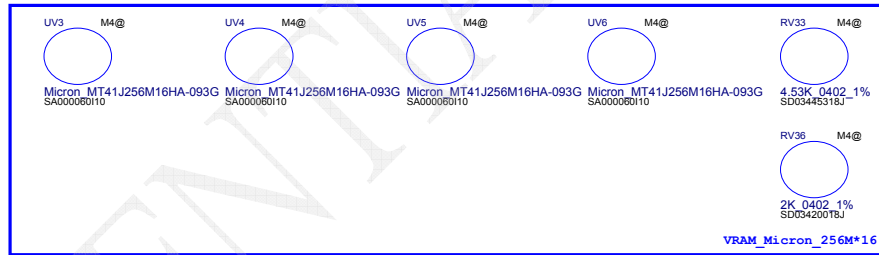
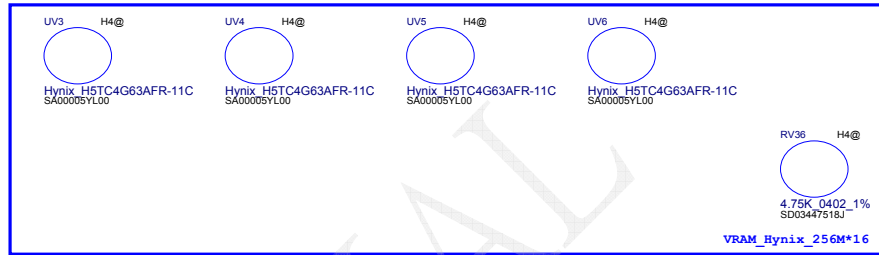
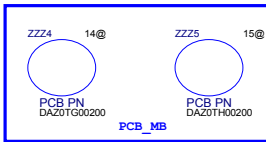
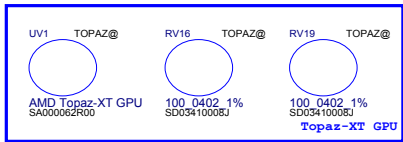
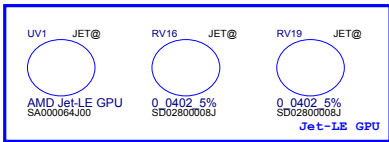
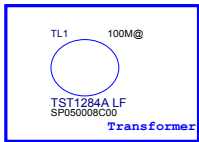
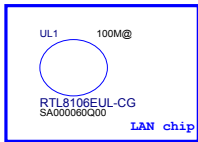
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	
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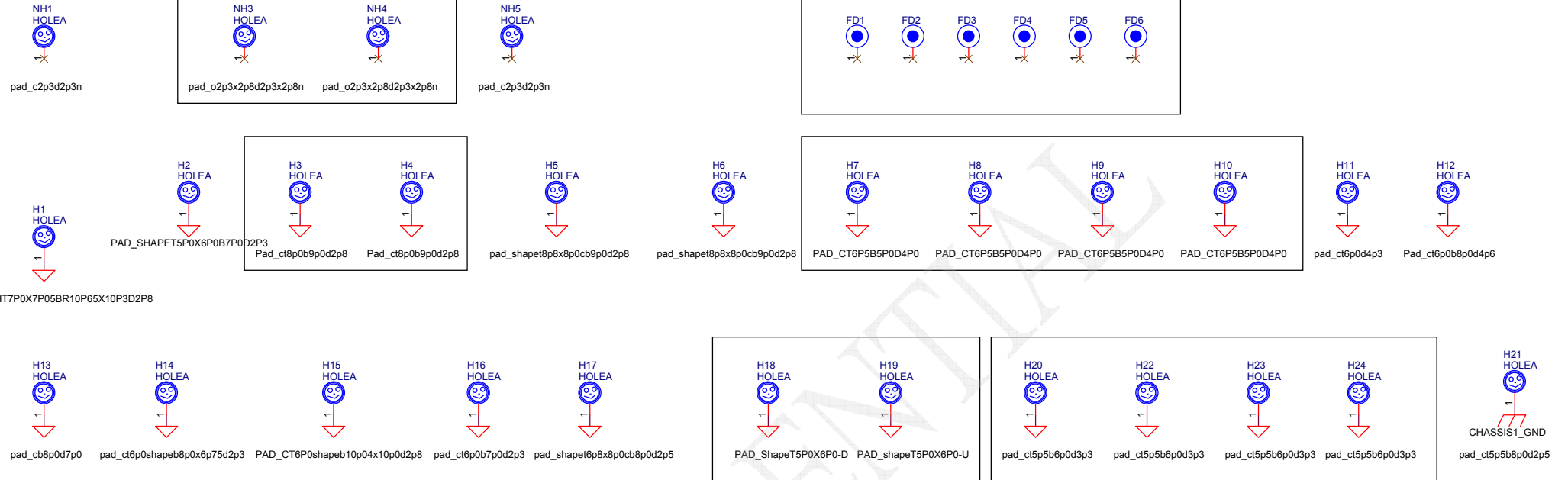
Title	Document Number	Rev
Power sequence Block	ACL1 & ACL2	1.0
Date:	Thursday, December 19, 2013	Sheet 47 of 59



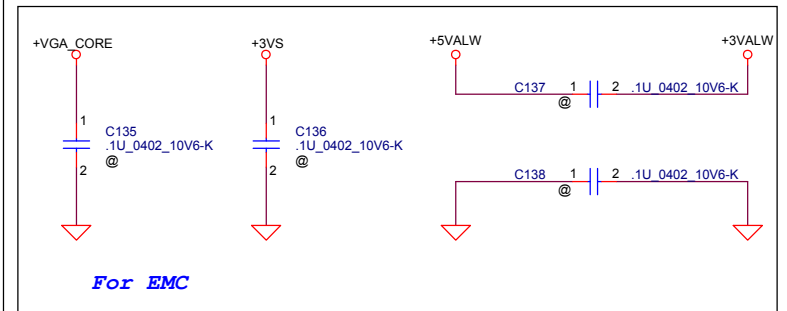



Board ID

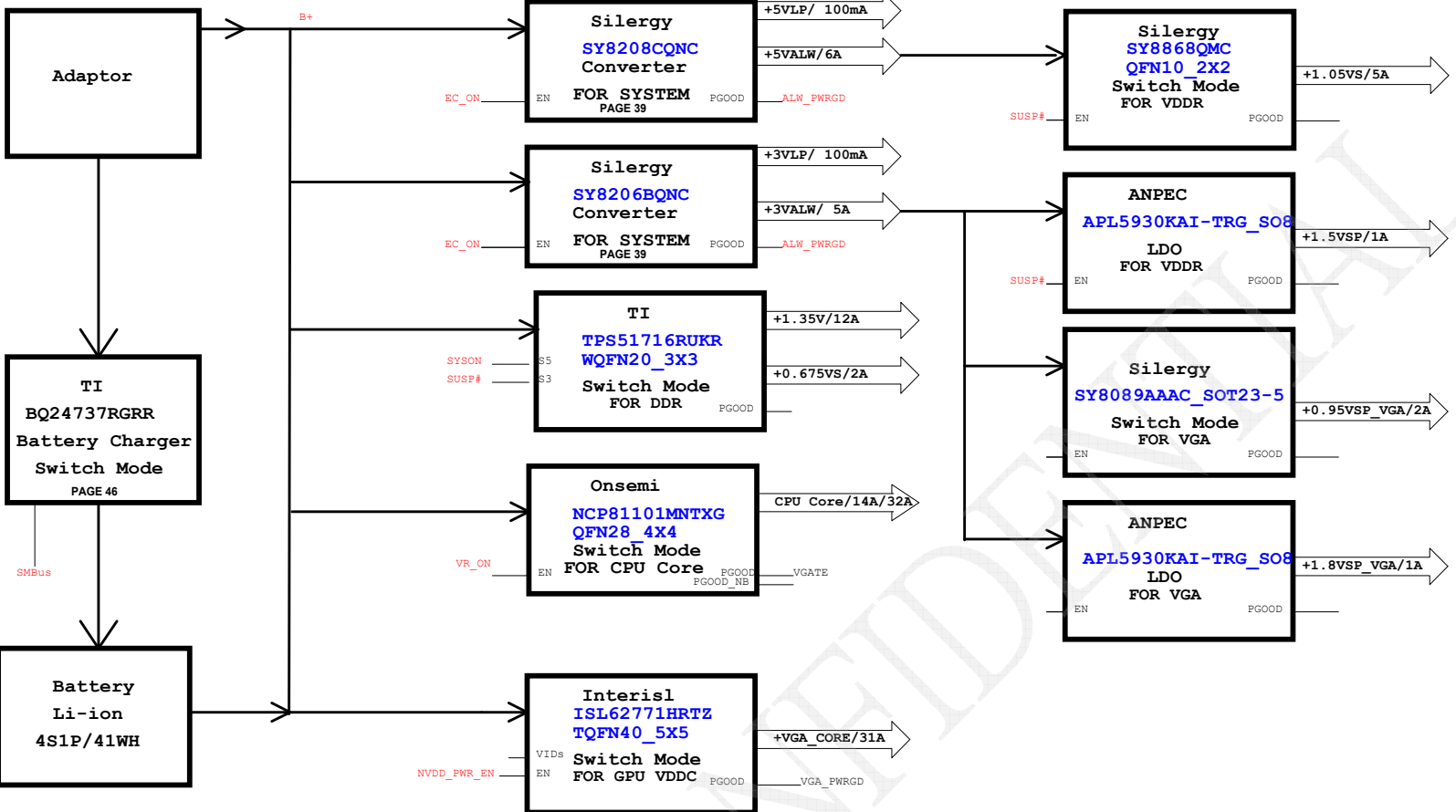
BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description	Stuff Resistor
0	0	0	0	14" + Jet-LE sku	RC107,RC108,RC109,RC123
0	1	0	0	15" + Jet-LE sku	RC107,RC101,RC109,RC123
1	0	0	0	14" + Topaz-XT sku	RC100,RC108,RC109,RC123
1	1	0	0	15" + Topaz-XT sku	RC100,RC101,RC109,RC123




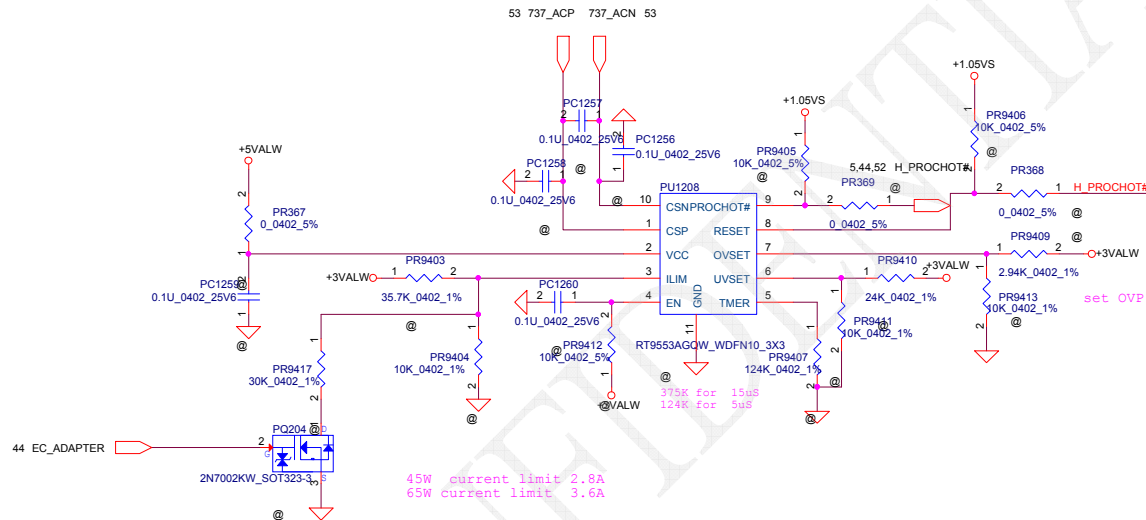
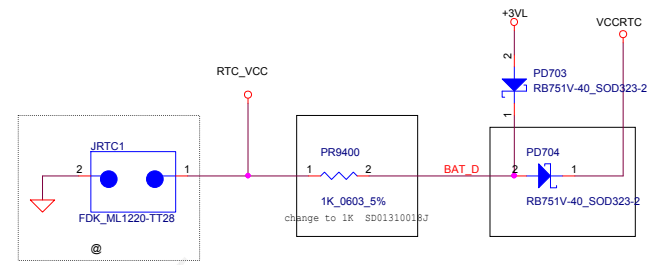
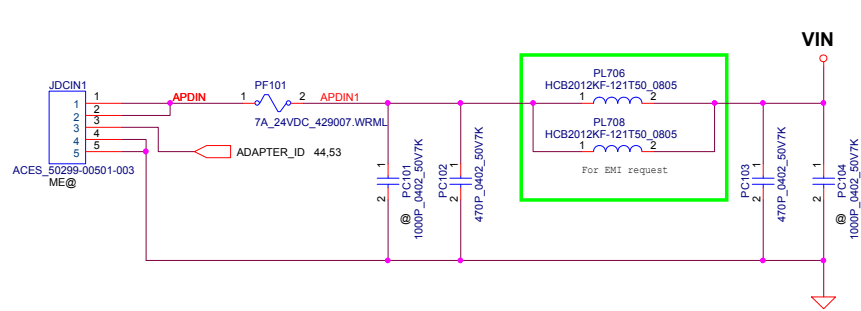
FFC CONN GROUND PAD



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				Date:	Thursday, December 19, 2013	Sheet 49 of 59



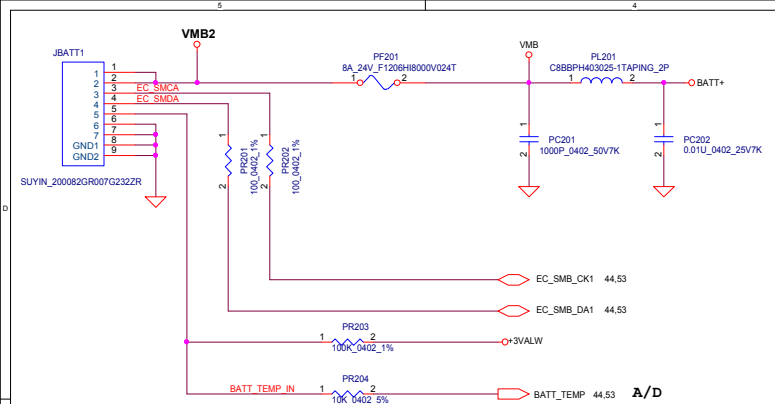
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	
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				Rev: 1.0



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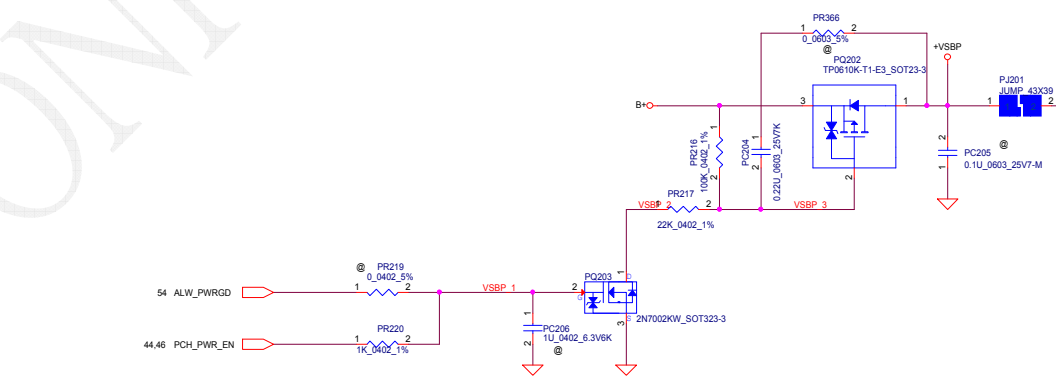
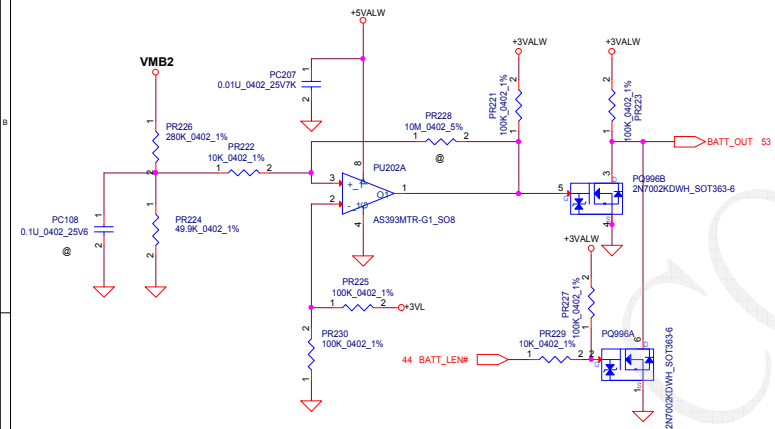
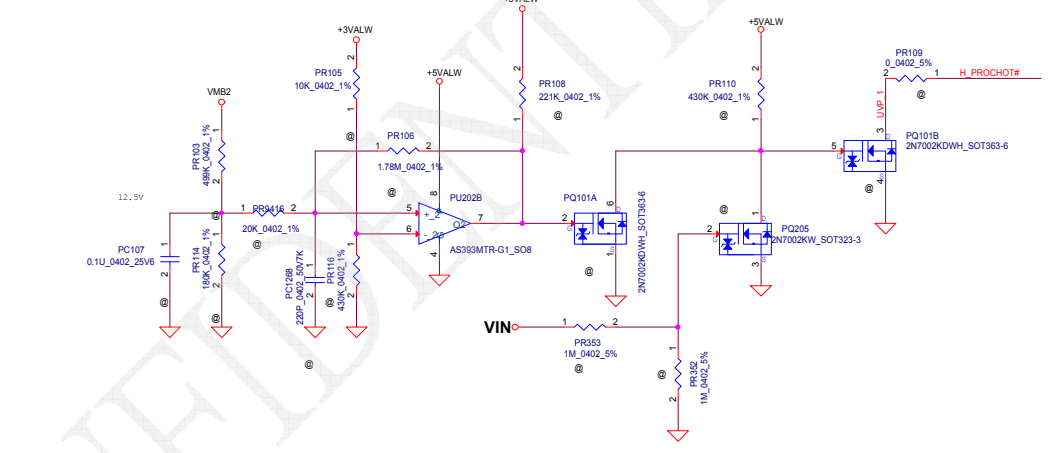
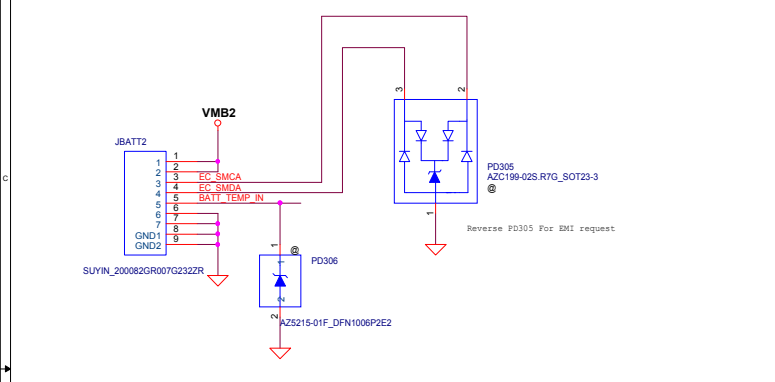
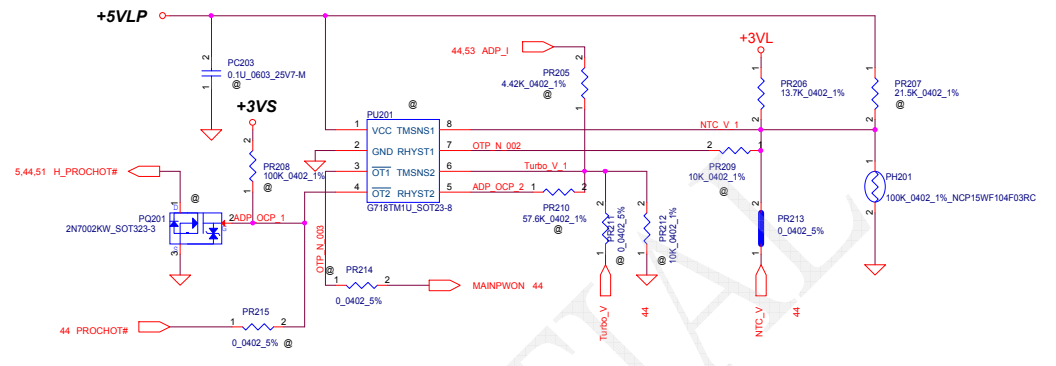
Title	DCIN / RTC	
Size	Document Number	Rev
Custom	ACLU1 & ACLU2	1.0
Date:	Thursday, December 19, 2013   Sheet 51 of 59	






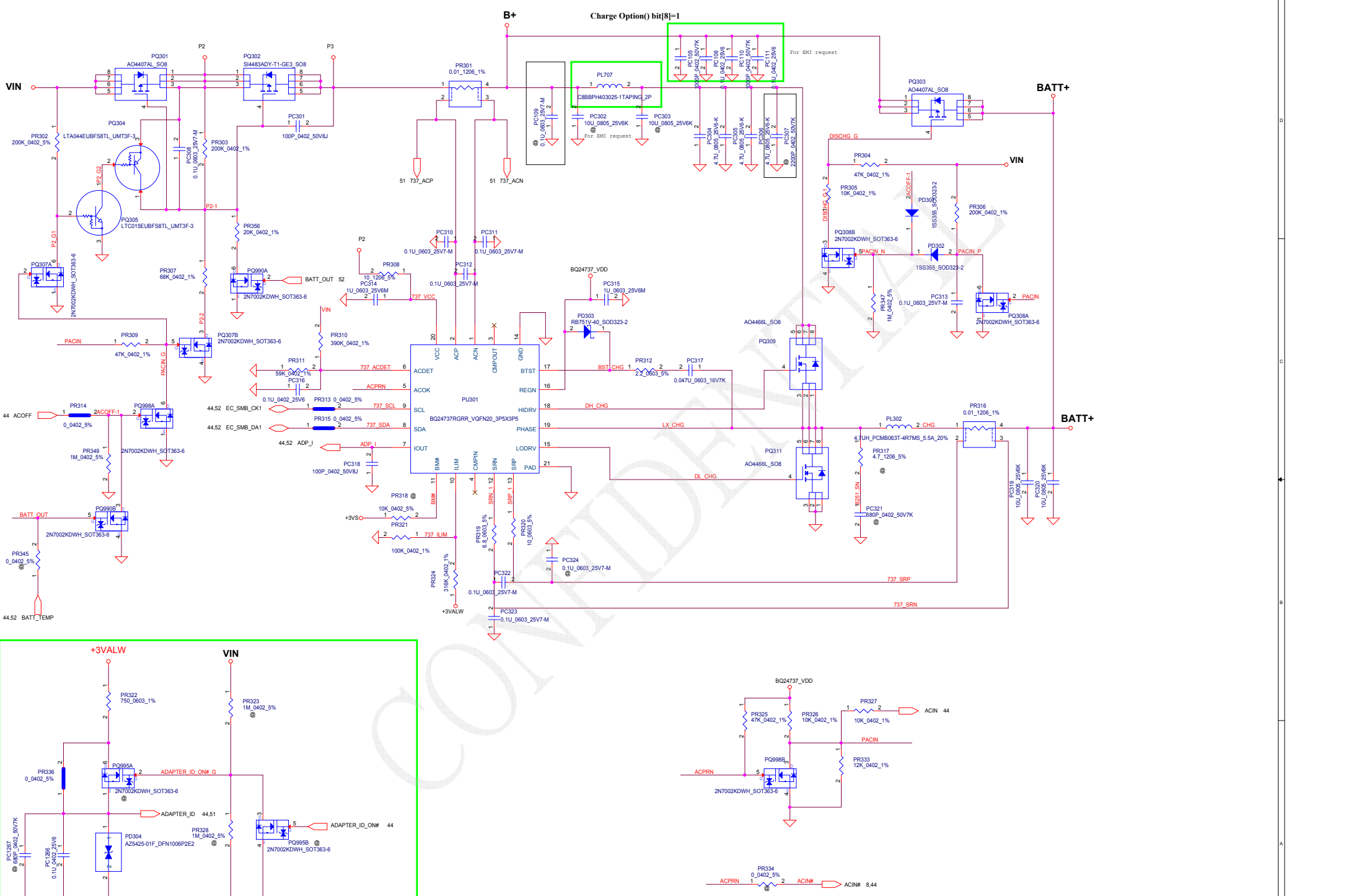
**PH201 under CPU bottom side :**  
**CPU thermal protection at 92+3 degree C**  
**Recovery at 56 +3 degree C**


**For KB930 --> Keep PU1 circuit**  
**(Vth = 0.825V)**  
**For KB912 (Red square) --> Remove PU201 circuit, but keep PR206**  
**PH201, PR205, PR211, PQ201, PR208, PR212**

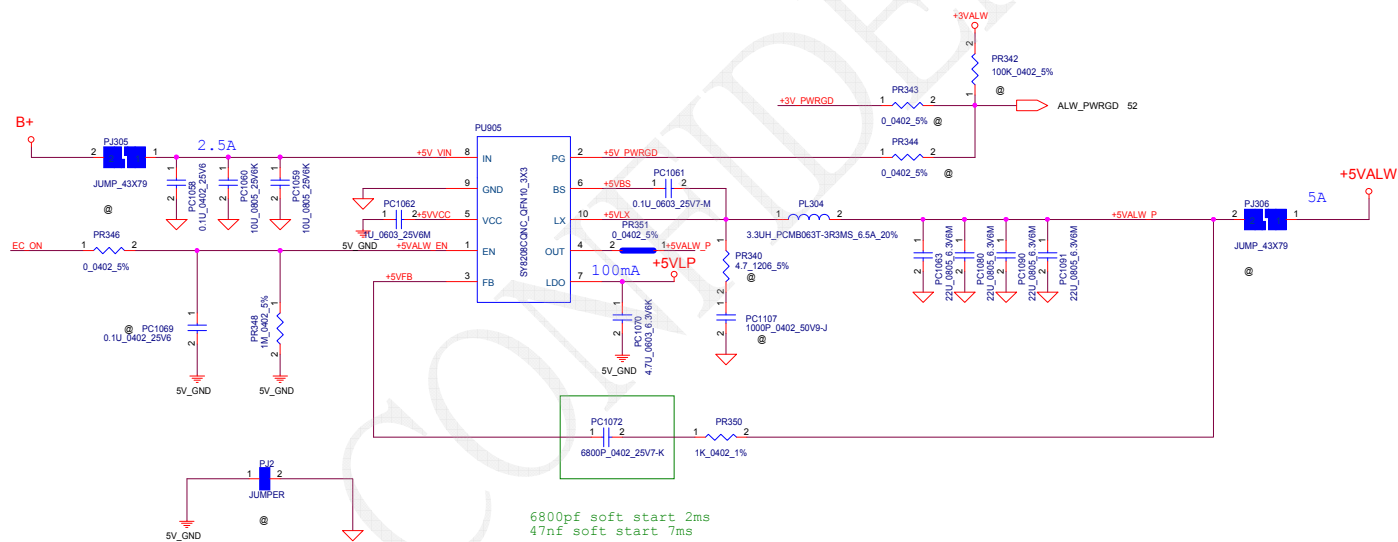
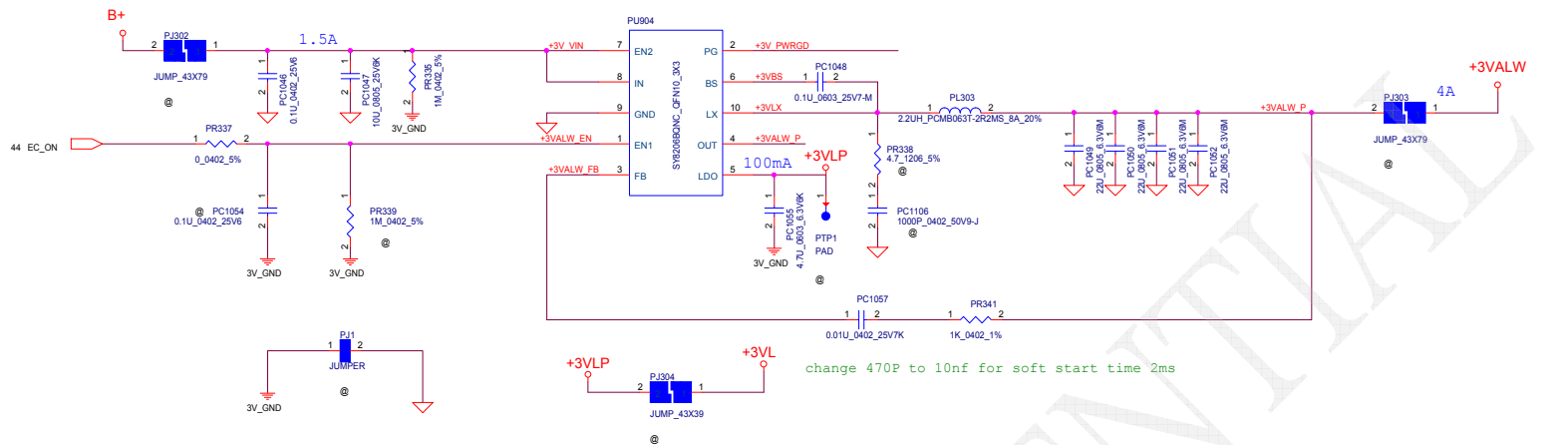



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Size	Document Number	<b>ACL01 &amp; ACL02</b>		Rev 1.0
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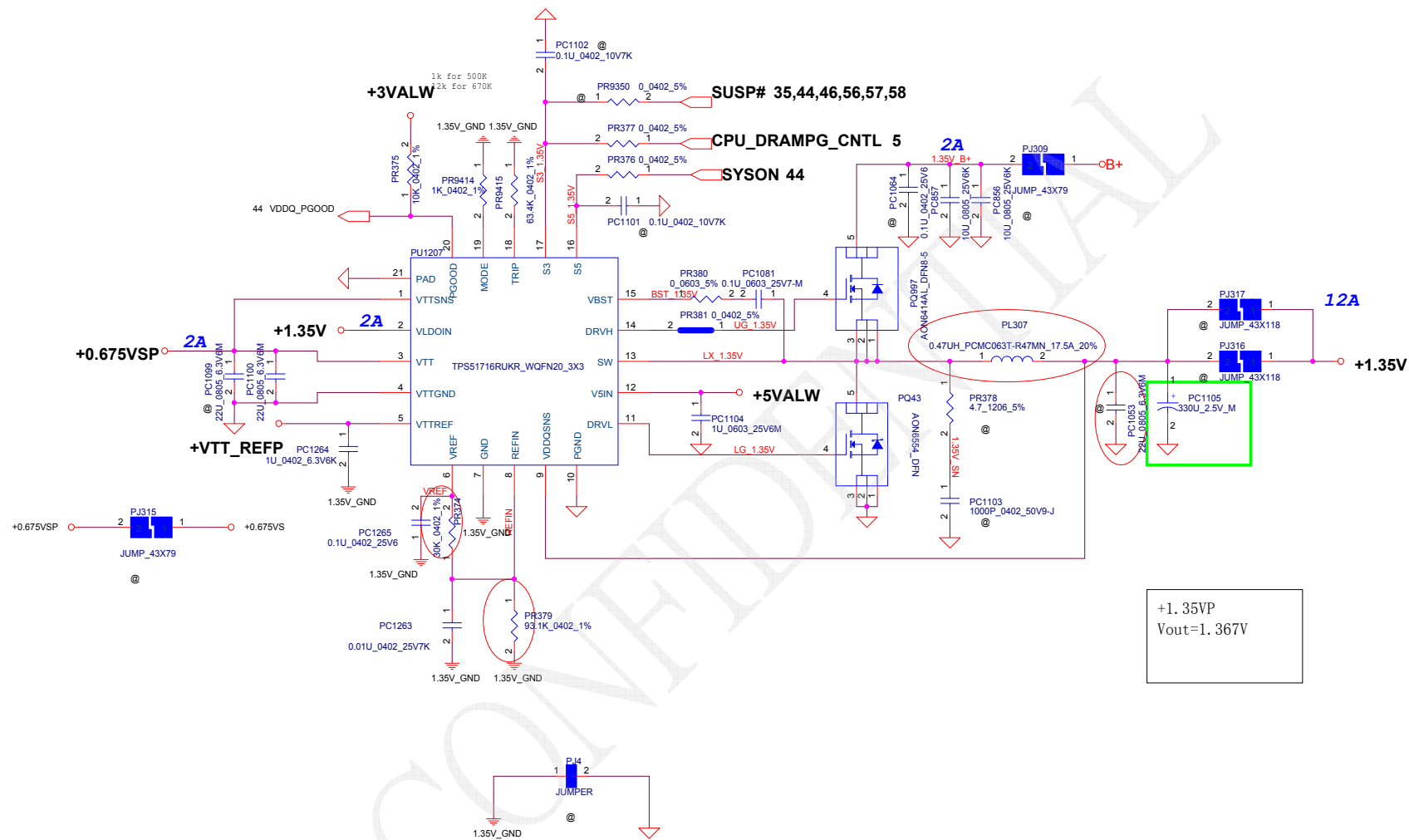




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Size	Document Number	<b>ACL01 &amp; ACL02</b>		Rev 1.0	
Date:	Friday, December 20, 2013	Sheet	53	of	59

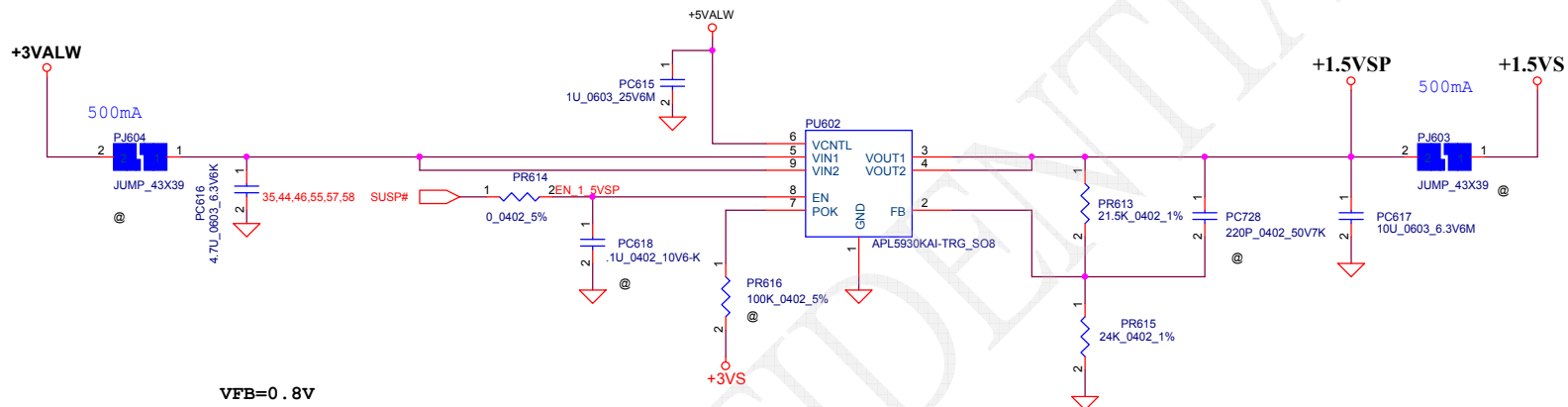


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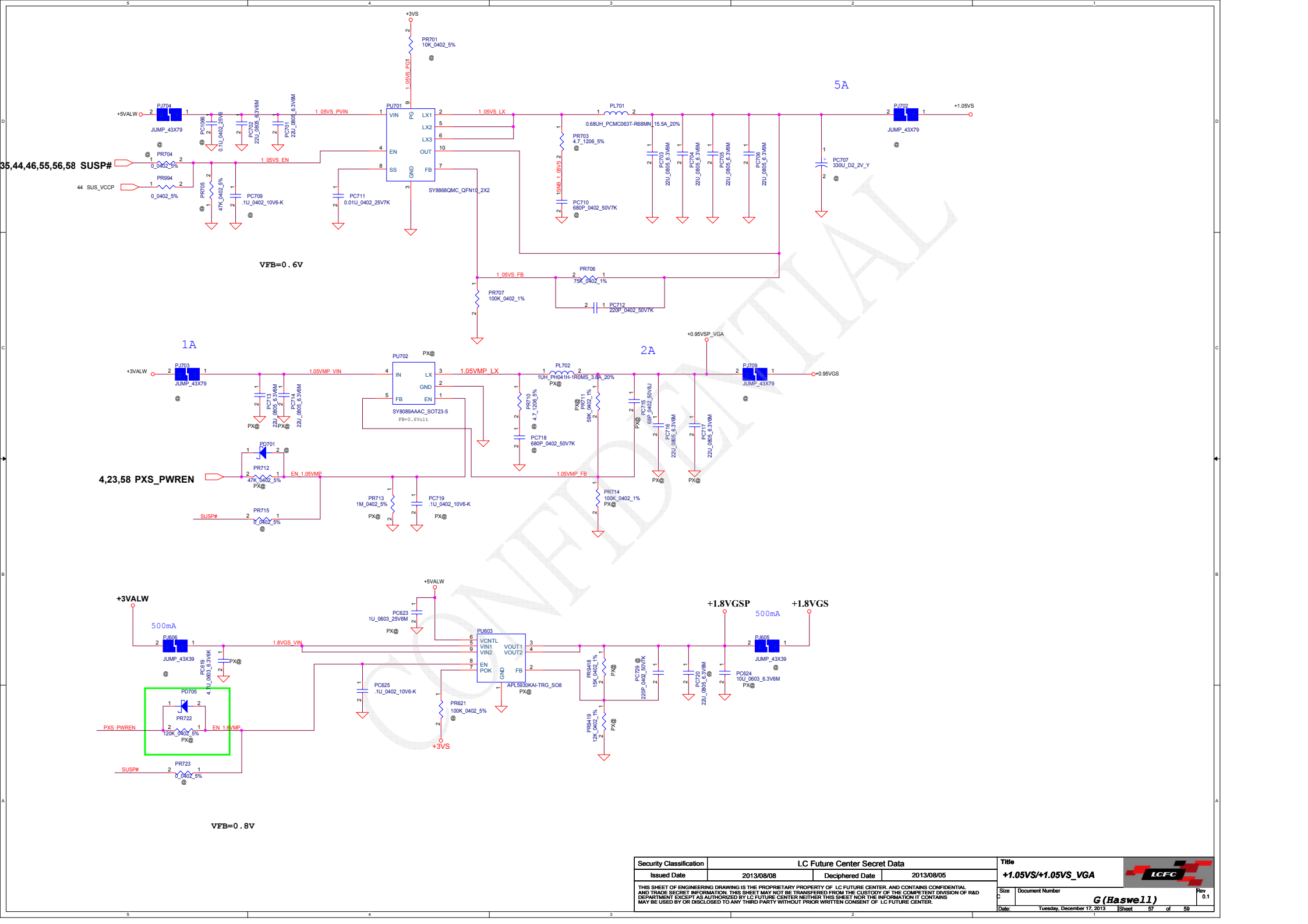
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Size	Document Number	<b>ACLU1 &amp; ACLU2</b>
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35,44,46,55,56,58 SUSP#

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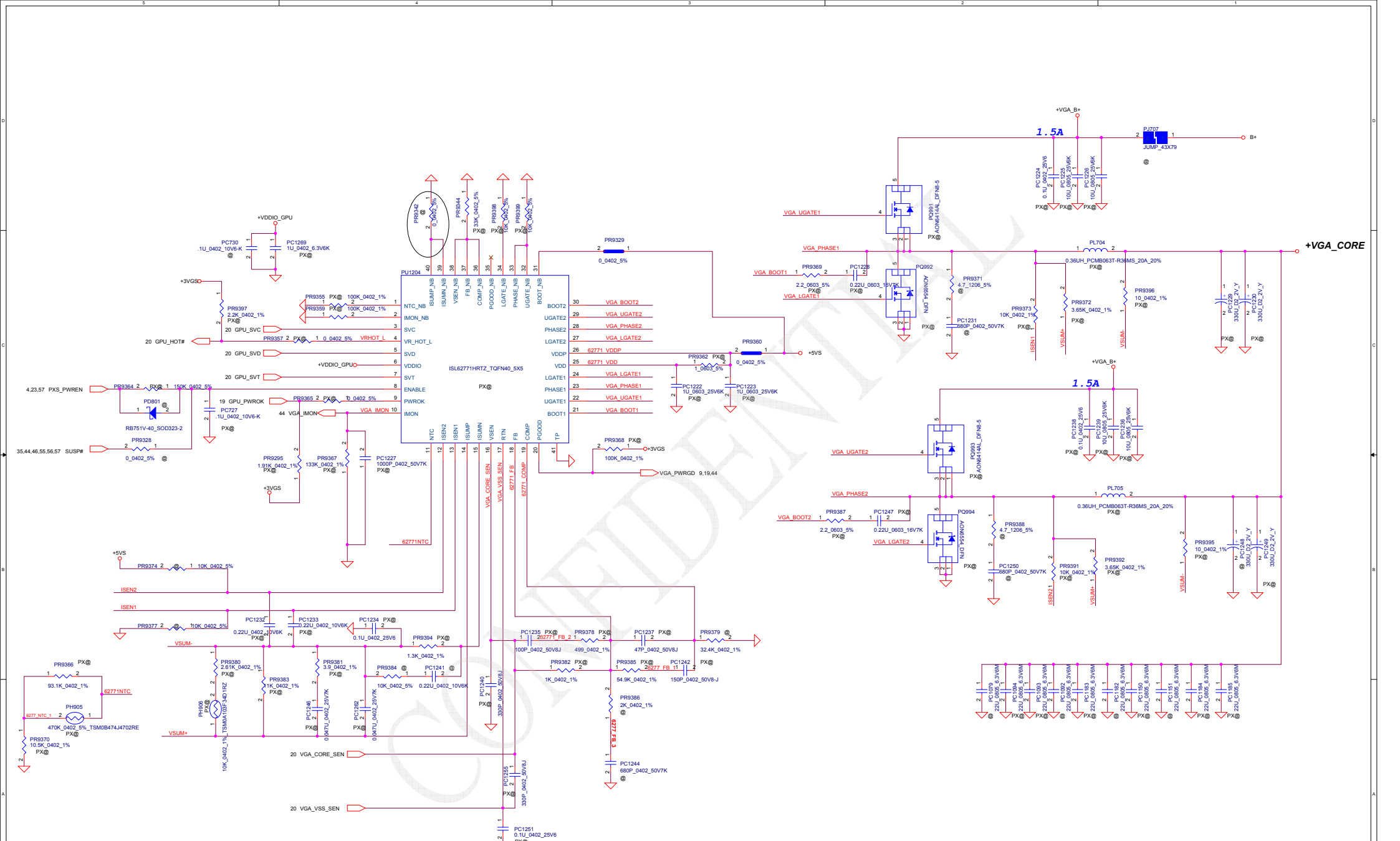
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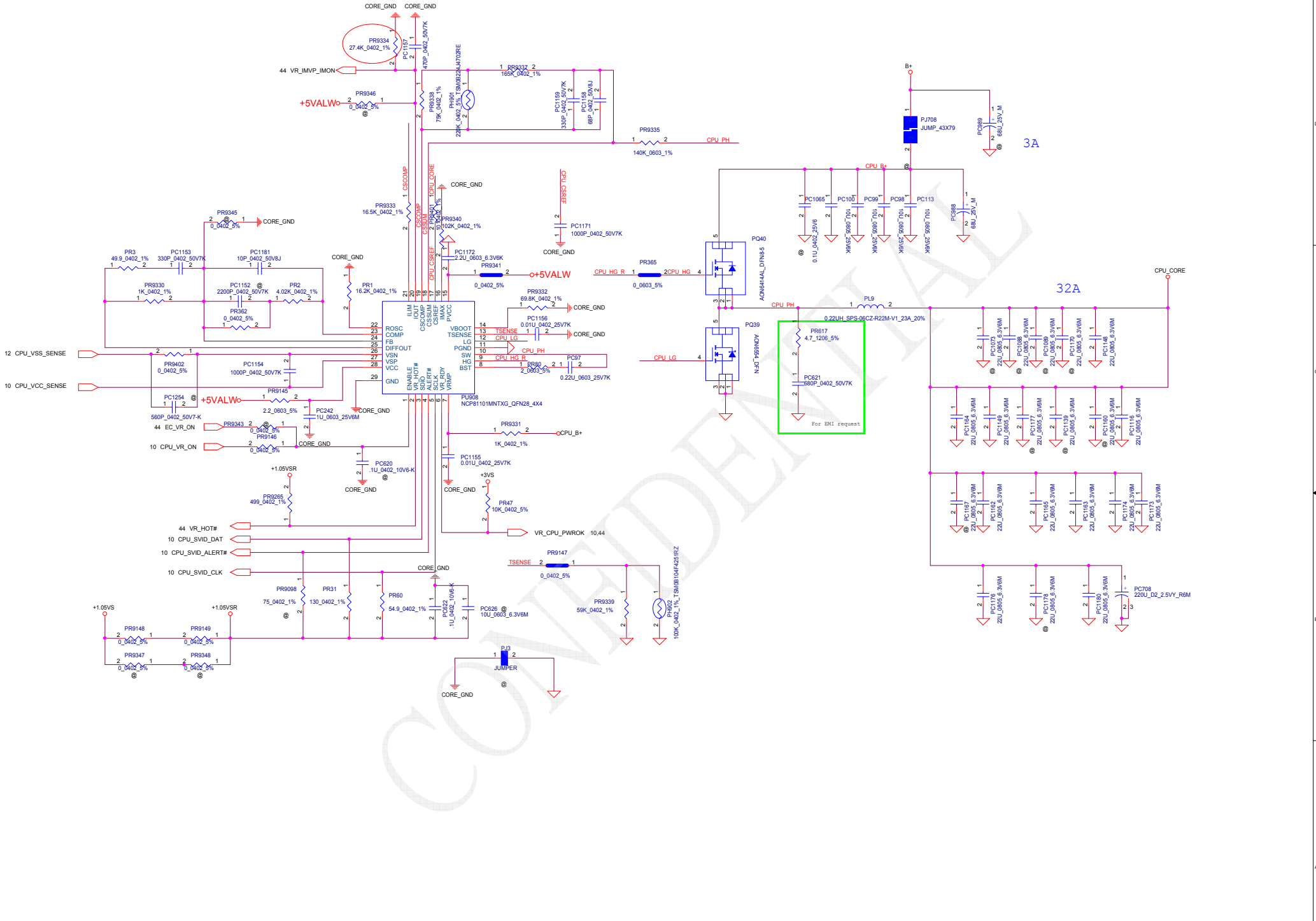
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			ACLUI & ACLU2	1.0
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