

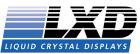
# **Specification for Approval**

PRODUCT NAME: RGS13128096FH000 PRODUCT NO.: 9910901000

CUSTOMER	
APPROVED BY	
ATE:	DATE:

RITDISPLAY CORP. APPROVED

Available From:



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## **REVISION RECORD**

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2005.01.25	
X02	<ul> <li>Modify electrical characteristics</li> <li>Modify CIE specification</li> <li>Modify reliability test conditions</li> <li>Add protective film</li> <li>Remove the outgoing inspection provision (Refer to "OQC SPEC - STD - Full Color, CF type")</li> </ul>	2005. 05. 05	Page 6, 7, 8, 15 & 16
X03	<ul> <li>■ Modify product name -         RGC13128096FH000→         RGS13128096FH000</li> <li>■ Add warranty</li> <li>■ Change COF from SSD1338U2 to         SSD1338U3</li> <li>■ Modify lifetime definition</li> <li>■ Add packing specification</li> </ul>	2005. 11. 28	Page 1, 4, 6, 16 & 17
A01	<ul> <li>Modify wide range of operating temperature</li> <li>Add the information of module weight</li> <li>Modify lifetime specification</li> <li>Modify the operating conditions for different luminance</li> <li>Modify the panel electrical specification</li> <li>Modify typical luminance</li> <li>Modify CIE specification</li> <li>Modify reliability test conditions</li> </ul>	2006. 03. 16	Page 4, 5, 6, 8, 15 & 21



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#### 1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications, which are either not addressed, or are exceptions to the supporting documents.

#### 2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

#### 3. FEATURES

- Small Molecular Organic Light Emission Diode.
- Color: 262K Full colorPanel matrix: 128\*3\*96Driver IC: SSD1338U3
- Excellent Quick response time: 10µs
- Extremely thin thickness for best mechanism design: 1.85 mm
- High contrast: 500:1
- Wide viewing angle: 160°
- Strong environmental resistance.
- 16/8-bits 6800-series Parallel Interface, 16/8-bits 8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range of operating temperature : -40 to 70 °C



## **4. MECHANICAL DATA**

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x (RxGxB) x 96 (H)	dot
2	Dot Size	0.057 (W) x 0.19 (H)	mm <sup>2</sup>
3	Dot Pitch	0.07 (W) x 0.21 (H)	mm <sup>2</sup>
4	Aperture Rate	74	%
5	Active Area	26.867 (W) x 20.14 (H)	mm <sup>2</sup>
6	Panel Size	36 (W) x 30 (H)	mm <sup>2</sup>
7	Panel Thickness	1.85 ± 0.1	mm
8	Module Size	36.0 (W) x 52.5 (H) x 1.85 (D)	mm <sup>3</sup>
9	Diagonal A/A size	1.3	inch
10	Module Weight	4.4 ± 10%	gram



## **5. MAXIMUM RATING**

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V <sub>DD</sub> )		3.5	V	Ta = 25 ℃	
Supply Voltage (V <sub>DDIO</sub> )		3.5	V		
Supply Voltage(Vcc)		15.5	V	Ta = 25 ℃	
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	℃		
Humidity	-	85	%		
Operating Life Time	6,400	-	Hrs	100 cd/m <sup>2</sup> , 50% checkerboard	Note (1)
Operating Life Time	8,000	-	Hrs	80 cd/m <sup>2</sup> , 50% checkerboard	Note (2)
Operating Life Time	10,000	-	Hrs	60 cd/m <sup>2</sup> , 50% checkerboard	Note (3)

#### Note:

- (A) Under Vcc = 15 Volts, Ta = 25 °C, 50% RH.
- (B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

#### (1) Setting of $100 \text{ cd/m}^2$ :

Master contrast setting: 0x0BH

Frame rate: 85 HzDuty setting: 1/96

#### (2) Setting of 80 cd/m<sup>2</sup>:

Master contrast setting: 0x09H

Frame rate: 85 HzDuty setting: 1/96

#### (3) Setting of 60 cd/m<sup>2</sup>:

Master contrast setting: 0x06H

Frame rate: 85 HzDuty setting: 1/96



## **6. ELECTRICAL CHARACTERISTICS**

#### **6.1 D.C ELECTRICAL CHARACTERISTICS**

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Driver power supply (for OLED panel)	Ta=-20°C to +70°C	14.5	15	15.5	V
$V_{DD}$	Logic operating voltage	Ta=-20°C to +70°C	2.4	2.7	3.5	V
$V_{DDIO}$	Logic I/O operating voltage	Ta=-20°C to +70°C	1.5	2.7	3.5	V
V <sub>OH</sub>	Hi logic output level	lout=100 uA, 3.3MHz	0.9*V <sub>DDIO</sub>		$V_{DDIO}$	V
V <sub>OL</sub>	Low logic output level	lout=100uA, 3.3MHZ	0		0.1*V <sub>DDIO</sub>	V
V <sub>IH</sub>	Hi logic input level	lout=100uA, 3.3MHZ	0.8*V <sub>DDIO</sub>		V <sub>DDIO</sub>	V
V <sub>IL</sub>	Low logic output level	lout=100uA, 3.3MHZ	0		0.2*V <sub>DDIO</sub>	V
I <sub>CC</sub>	Operating current for V <sub>CC</sub> (No panel attached)	Contrast=FF		1.3		mA
I <sub>DD</sub>	Operating current for V <sub>DD</sub> (No panel attached)	Contrast=FF		0.4		mA
		Contrast=FF		160		uA
	Segment output	Contrast=AF		110		uA
I <sub>SEG</sub>	current	Contrast=5F	_	60		uA
	(No panel attached)	Contrast=00		0		uA

Note:  $V_{DD}=2.7$  Volts;  $V_{CC}=15$  Volts; Frame rate= 85 Hz; No panel attached.

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#### **6.2 ELECTRO-OPTICAL CHARACTERISTICS**

#### PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		30	32	mA	All pixels on (1)
Standby mode current		3	4	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		450	480	mW	All pixels on (1)
Standby mode power consumption		45	60	mW	Standby mode 10% pixels on (2)
Normal mode Luminance	70	80		cd/m <sup>2</sup>	Display Average
Standby mode Luminance		20		cd/m <sup>2</sup>	
CIEx(White)	0.24	0.28	0.32		
CIEy(White)	0.28	0.32	0.36		
CIEx(Red)	0.61	0.65	0.69		
CIEy(Red)	0.30	0.34	0.38		x, y (CIE 1931)
CIEx(Green)	0.22	0.26	0.30		x, y (GIL 1931)
CIEy(Green)	0.52	0.56	0.60		
CIEx(Blue)	0.07	0.11	0.15		
CIEy(Blue)	0.13	0.17	0.21		
Dark Room Contrast	500:1				
Viewing Angle	160			degree	
Response Time		10		μs	

#### (1) Normal mode condition:

Driving Voltage : 15VContrast setting : 0x09H

Frame rate: 85 HzDuty setting: 1/96

#### (2) Standby mode condition:

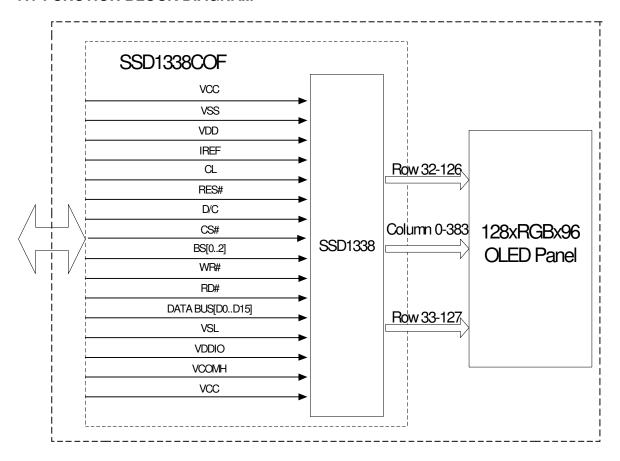
Driving Voltage: 15VContrast setting: 0x02H

Frame rate: 85 Hz
Duty setting: 1/96



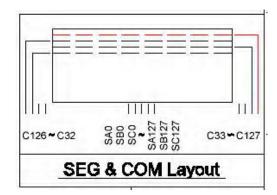
## 7. INTERFACE

#### 7.1 FUNCTION BLOCK DIAGRAM



RiTdisplay 128xRGBx96 OLED Module

#### 7.2 PANEL LAYOUT DIAGRAM



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#### 7.3 PIN ASSIGNMENTS

7.5 PIN AS		III-LI I O
PIN NAME	PIN NO	DESCRIPTION
NC	1	No connection.
VCC	2	Analog voltage power supply.
VSS	3	Ground.
TEST	4	No connection.
TEST	5	No connection.
VDD	6	Digital voltage power supply.
TEST	7	No connection.
TEST	8	No connection.
TEST	9	No connection.
IREF	10	A resistor should be connected between this pin and VSS.
CL	11	No connection.
RES#	12	Hardware Reset pin (Low active).
D/C	13	H: Data; L: Command.
CS#	14	Chip select pin.
BS2	15	Interface select pin.
BS1	16	Interface select pin.
BS0	17	Interface select pin.
R/W#	18	8080: data write enable pin; 6800: Read/Write select pin.
E/RD#	19	8080: data read enable pin; 6800: Read/Write enable pin.
D0	20	
D1	21	
D2	22	
D3	23	
D4	24	
D5	25	
D6	26	
D7	27	16 bits data bus.
D8	28	
D9	29	
D10	30	
D11	31	
D12	32	
D13	33	
D14	34	
D15	35	
VSS	36	Ground.
VSL	37	This is segment voltage reference pin.
VDDIO	38	I/O voltage power supply.
VCOMH	39	A capacitor should be connected between this pin and VSS.
VCC	40	Analog power supply.
NC	41	No connection



#### 7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

#### **Graphic Display Data RAM (GDDRAM)**

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is  $132 \times 133 \times 16$  bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display. Each pixel has 16-bit data. The arrangement of data pixel in graphic display data RAM is shown below.

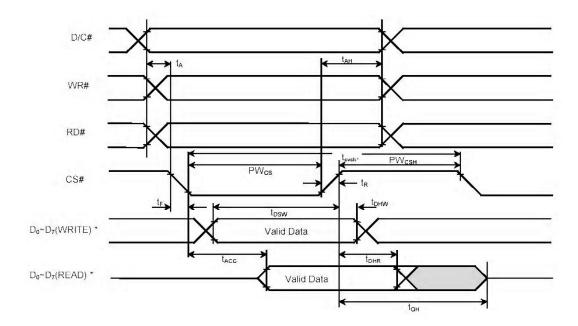
Column	Normal		0			1			2				129			130			131		
Address	Remap		131			130			129			-	2			1			0	200	
Da	ita	A5	B5	C5	A5	B5	C5	A5	B5	C5		A5	B5	C5	A5	B5	C5	A5	B5	C5	
For	mat	A4	B4	C4	A4	B4	C4	A4	B4	C4	-	A4	B4	C4	A4	B4	C4	A4	B4	C4	
1		A3	B3	C3	A3	B3	C3	A3	В3	C3		A3	B3	C3	A3	B3	C3	A3	B3	C3	
		A2	B2	C2	A2	B2	C2	A2	B2	C2		A2	B2	C2	A2	B2	C2	A2	B2	C2	
Ro		A1	B1	C1	A1	B1	C1	A1	<b>B</b> 1	C1		A1	B1	C1	A1	B1	C1	A1	B1	C1	
Add	ress	AD	B0	C0	A0	BO	CO	A0	В0	CO		A0	B0	CO	A0	B0	CO	A0	BO	CO	COM
Normal	Remap		160					-													OUTPU
0	132	6	6	6	6	6	6	6	6	6		6	6	6	6	6	6	6	6	6	COM0
1	131										13										COM1
2	130		1																		COM2
*			no. of bits of data in this cell																		
130	2									13.	-	-									COM130
131	1										2										COM131
	0													8						1	COM132



#### 7.5 INTERFACE TIMING CHART

 $(V_{DD} - V_{SS} = 2.4 \text{ to } 3.5 \text{V}, T_A = 25^{\circ}\text{C})$ 

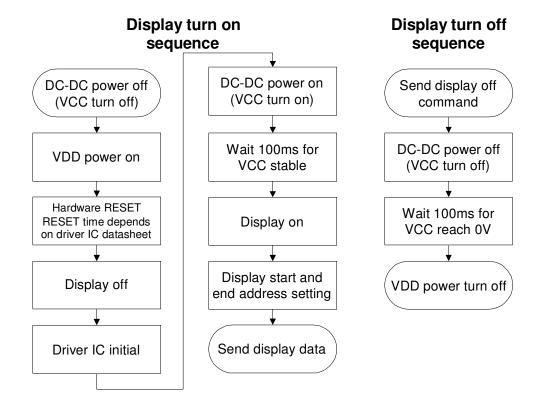
Symbol	Parameter	Min	Тур	Max	Unit
t <sub>cycle</sub>	Clock Cycle Time	300	-	-	ns
tas	Address Setup Time	0	-	-	ns
t <sub>AH</sub>	Address Hold Time	0	-	-	ns
tosw	Write Data Setup Time	40	-	-	ns
t <sub>DHW</sub>	Write Data Hold Time	15	-		ns
t <sub>DHR</sub>	Read Data Hold Time	20			ns
tон	Output Disable Time	-	-	70	ns
tacc	Access Time	-	-	140	ns
PWcsL	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW <sub>csH</sub>	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	3	-	ns
t <sub>R</sub>	Rise Time	-	-	15	ns
t <sub>F</sub>	Fall Time	-	- 4	15	ns





## 8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

#### 8.1 POWER ON / OFF SEQUENCE



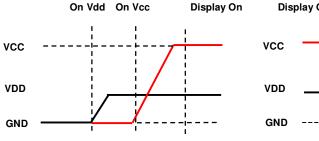
To protect OLED panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources turn on/off.

#### Power up Sequence:

- 1. Power up Vdd
- 2. Hardware RESET
- 3. Send display off command
- 4. Power up Vcc
- 5. Delay 100ms (when Vcc is stable)
- 6. Send Display on command

#### Power down Sequence:

- 1. Send Display off command
- 2. Power down Vcc
- 3. Delay 100ms (When Vcc is reach 0 and panel is completely discharges)
- 4. Power down Vdd



Display Off Off Vcc Off Vdd

VCC 

VDD 

GND 

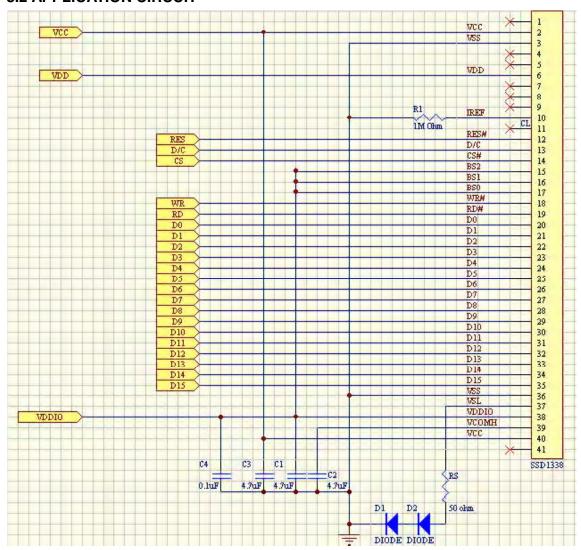
GND

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#### **8.2 APPLICATION CIRCUIT**



#### Notes:

Component:

R1: 1M ohm 1%

C1, C2, C3: 4.7 uF / 25V, C4: 0.1 uF

Rs: 50ohm 1/4W

D1 and D2: RB480K (ROHM)

This circuit is for 8080 16 bits interface.

#### **8.3 COMMAND TABLE**

Refer to IC Spec.: SSD1338

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## 9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85℃, 240hrs	5
2	High temp. (Operation)	70 °C, 120hrs	5
3	Low temp. (Operation)	-40 °C, 120hrs	5
4	High temp. / High humidity (Operation)	65℃, 90%RH, 96hrs	5
5	Thermal shock (Non-operation)	-40 °C ~85 °C (-40 °C /30min; transit /3min; 85 °C /30min; transit /3min) 1cycle: 66min, 20 cycles	5
6	Vibration	Frequency: 5~50HZ, 0.5G Scan rate: 1 oct/min Time: 2 hrs/axis Test axis: X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence: 1 angle > 3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

#### Test and measurement conditions

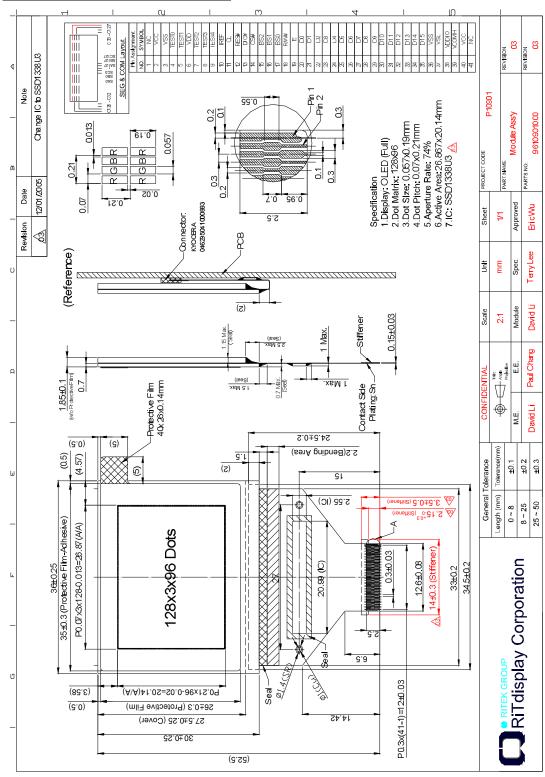
- 1. All measurements shall not be started until the specimens attain to temperature stability.
- 2. All-pixels-on is used as operation test pattern.

#### **Evaluation criteria**

- 1. The function test is OK.
- 2. No observable defects.
- 3. Luminance: > 50% of initial value.
- 4. Current consumption: within  $\pm$  50% of initial value.

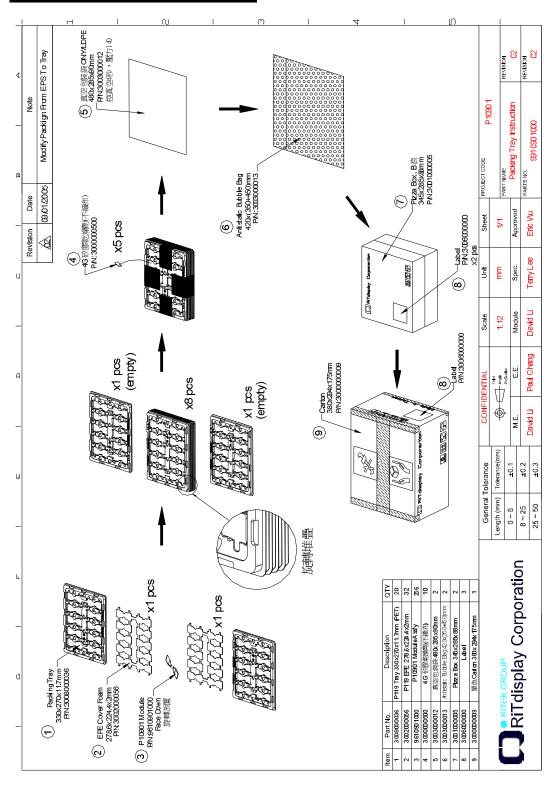


### **10. EXTERNAL DIMENSION**





## 11. PACKING SPECIFICATION



## 12. APPENDIXES

#### **APPENDIX 1: DEFINITIONS**

#### A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

#### **B. DEFINITION OF CONTRAST RATIO**

The contrast ratio is defined as the following formula:

#### C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

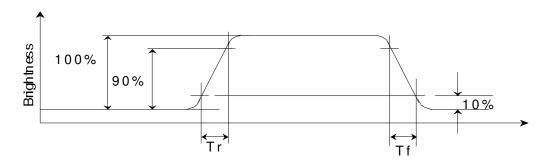


Figure 2: Response time

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## D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

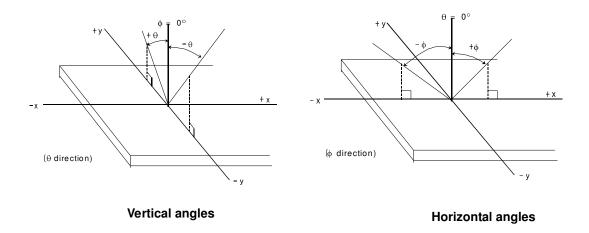


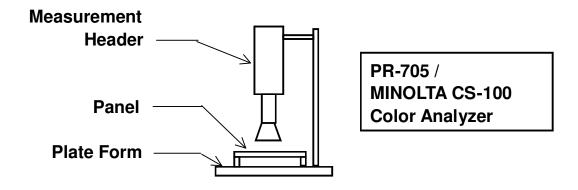
Figure 3: Viewing Angle



#### **APPENDIX 2: MEASUREMENT APPARATUS**

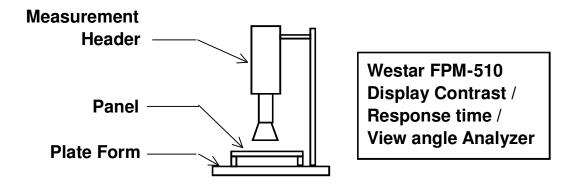
#### A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100



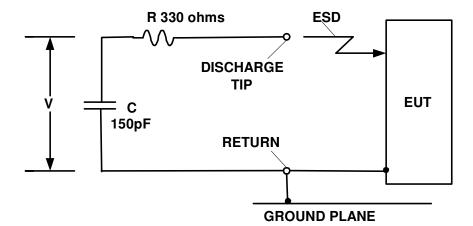
#### **B. CONTRAST / RESPONSE TIME / VIEW ANGLE**

**WESTAR CORPORATION FPM-510** 





#### C. ESD ON AIR DISCHARGE MODE





#### **APPENDIX 3: PRECAUTIONS**

#### A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.