SSD1338

Advance Information

132RGB x 132 with 2 smart Icon lines Dot Matrix OLED/PLED Segment/Common Driver with Controller

SOLOMON SYSTECH

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1. GERENAL DESCRIPTION

SSD1338 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SSD1338 consists of 396 segments (132RGB), 132 commons and 2 smart icon lines. This IC is designed for Common Cathode type OLED panel.

SSD1338 displays data directly from its internal 132x133x18 bits Graphic Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800/8000 series compatible Parallel Interface or Serial Peripheral Interface. SSD1338 has a 256 steps contrast control and 262k color control

2. FEATURES

- Support max. 132RGB x 132 matrix panel + icon line
- Power supply: VDD=2.4-3.5V
  VDDIO=1.5V - 3.5V
  VCC=7.0V - 18.0V
- OLED driving output voltage, 16V maximum
- DC-DC voltage booster controller
- Segment maximum source current: 200uA
- Common maximum sink current: 80mA
- Embedded 132x133x18 bit SRAM display buffer
- 16 step master current control, and 256 step current control for the three color components
- Smart Icon mode
- Programmable color mode of 256, 65k, 262k
- Programmable Frame Rate
- Graphic Acceleration Command Set (GAC)
- 8-bit/16 bit 6800-series Parallel Interface, 8080-series Parallel Interface and Serial Peripheral Interface.
- Wide range of operating temperature: -40 to 85 °C

3. ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1338UR1	96RGB	96	COF	Page 41	• 35mm film • 5 sprocket hole • Folding COF • 80 / 68 / SPI interface • Output lead pitch 0.06mm
SSD1338U1R1	130RGB	130	COF	Page 45	• 48mm film • 5 sprocket hole • Folding COF • 80 / 68 / SPI interface • Output lead pitch 0.05mm
SSD1338U2	128RGB	128	COF	Page 50	• Punched COF

4. BLOCK DIAGRAM

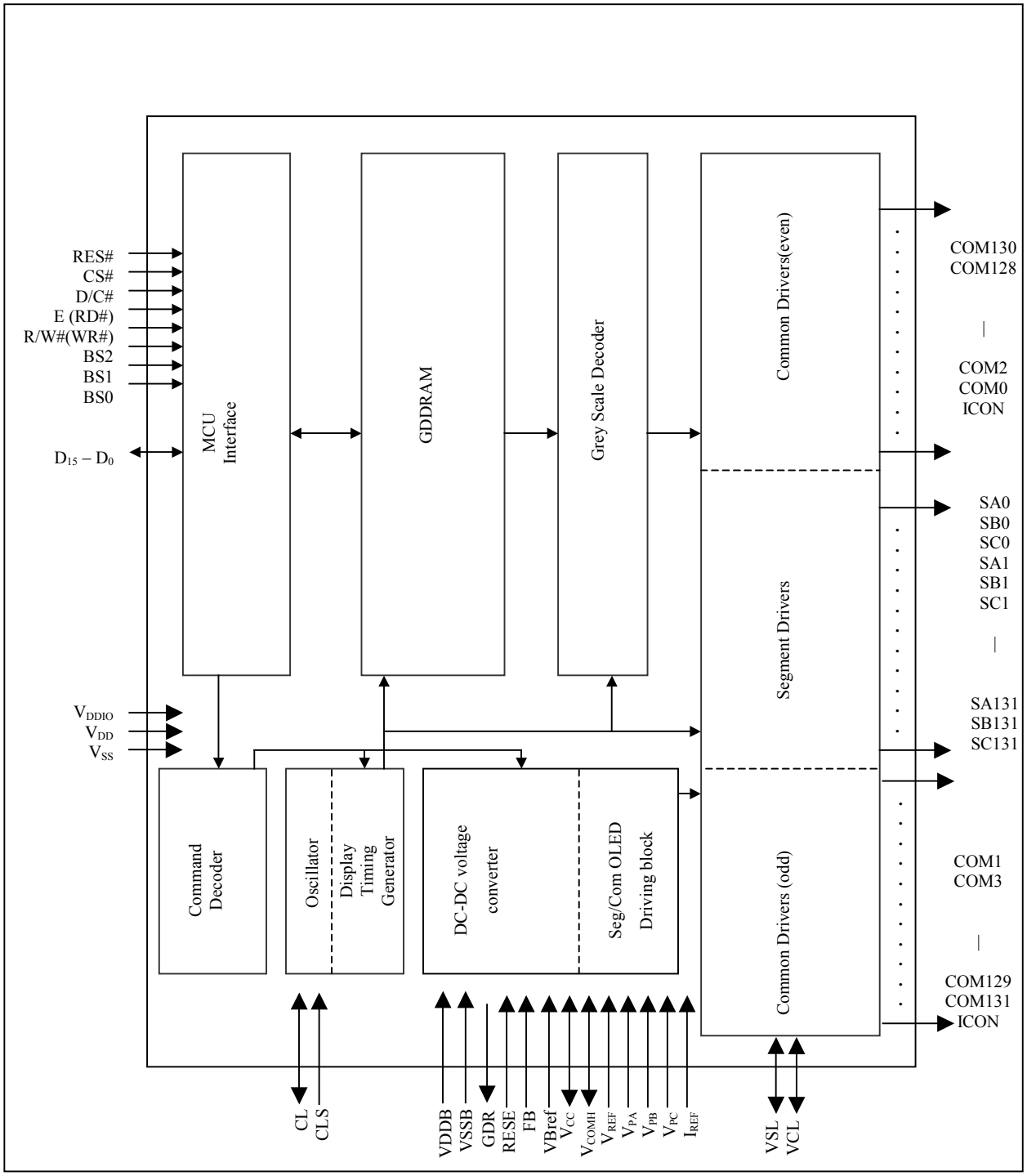


Figure 1 - Block Diagram

5. PIN DESCRIPTION

RES#
This pin is reset signal input. When the pin is low, initialization of the chip is executed.

CS#
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.

D/C#
This pin is Data/Command control pin. When the pin is pulled high, the data at D_7-D_0 is treated as display data. When the pin is pulled low, the data at D_7-D_0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.

E (RD#)
This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected.
When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and the chip is selected.

R/W#(WR#)
This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.
When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the chip is selected.

BS0, BS1, BS2
These pins are MCU interface selection input. See the following table:

	6800-parallel interface (8 bit)	6800-parallel interface (16 bit)	8080-parallel interface (8 bit)	8080-parallel interface (16 bit)	Serial interface
BS0	0	0	1	1	0
BS1	0	1	0	1	0
BS2	1	1	1	1	0

D_{15}-D_0
These pins are 16-bit bi-directional data bus to be connected to the microprocessor's data bus.

V_{DDIO}
This pin is a power supply pin of I/O buffer. It should be connected to V_{DD} or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS012, M/S, CLS, D0-D15, control signals…) pull high, they should be connected to VDDIO.

V_{DD}
Power Supply pin. It must be connected to external source.

V_{SS}
Ground. It also acts as a reference for the logic pins. It must be connected to external ground.

CL
This pin is the system clock input. When internal clock is enabled, this pin should be left open. Nothing should be connected to this pin. When internal oscillator is disabled, this pin receives display clock signal from external clock source.

CLS
This pin is internal clock enable. When this pin is pulled high, internal oscillator is selected.
The internal clock will be disabled when it is pulled low, an external clock source must be connected to CL pin for normal operation.

VDDB
This is the power supply pin for the internal buffer of the DC-DC voltage converter. It must be connected to V_{DD} when the converter is used.

VSSB
This is the GND pin for the internal buffer of the DC-DC voltage converter. It must be connected to V_{SS} when the converter is used.

GDR
This output pin drives the gate of the external NMOS of the booster circuit.

RESE
This pin connects to the source current pin of the external NMOS of the booster circuit.

FB
This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level (Vcc).

VB_{REF}
This pin is the internal voltage reference of booster circuit. A stabilization capacitor, typ. 1uF, should be connected to Vss.

V_{CC}
This is the most positive voltage supply pin of the chip. It is supplied either by external high voltage source or internal booster

V_{COMH}
This pin is the input pin for the voltage output high level for COM signals. It can be supplied externally or internally. When V_{COMH} is generated internally, a capacitor should be connected between this pin and V_{SS}.

V_{REF}
This pin is the reference for OLED driving voltages like V_{PA}, V_{PB}, V_{PC} and V_{COMH}. It can be either supplied externally or connected to V_{CC}.

V_{PA}, V_{PB}, V_{PC}
These pins are the driving voltages for OLED driving segment pins SA0-SA131, SB0-SB131 and SC0-SC131 respectively. They can be supplied externally or internally generated by VP circuit. When internal VP is used, V_{PA}, V_{PB}, V_{PC} pins should be left open.

I_{REF}
This pin is the segment output current reference pin. I_{SEG} is derived from I_{REF}

I_{SEG} = Contrast / 256 * I_{REF} * scale factor,
in which the contrast is set by command and the scale factor = master current control register setting with value from 1~16.

A resistor should be connected between this pin and V_{SS} to maintain the current around 10uA.

VSL
This is segment voltage reference pin. This pin should be connected to V_{SS} externally.

VCL
This is common voltage reference pin. This pin should be connected to V_{SS} externally.

COM0-COM131
These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is off.

SA0-SA131, SB0-SB131, SC0-SC131
These pins provide the OLED segment driving signals. These pins are in high impedance state when display is off.
The 396 segment pins are divided into 3 groups, SA, SB and SC. Each group can have different color settings for color A, B and C.

ICON
These two pins provide the Common switch signals for Icon line to the OLED panel. These pins are in high impedance state when display is off.

6. FUNCTIONAL BLOCK DISCRIPTIONS

6.1 Oscillator Circuit and Display Time Generator

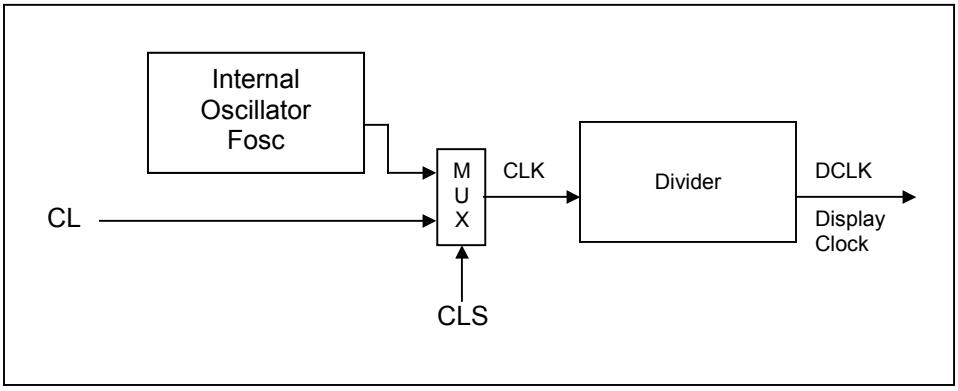


Figure 2 - Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled high, internal oscillator is chosen. Pulling CLS pin low disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command B3h.

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor can be programmed from 1 to 16 by command B3h.

6.2 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 132x132 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00H and COM0 mapped to address 00H)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80H

6.3 Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is high, data is written to Graphic Display Data RAM (GDDRAM). If it is low, the input at D_7-D_0 is interpreted as a Command and it will be decoded and be written to the corresponding command register.

6.4 MPU Parallel 6800-series Interface

The parallel interface consists of 16 bi-directional data pins (D_{15}-D_0) or 8 bi-directional data pins (D_7-D_0), R/W#(WR#), D/C#, E (RD#) and CS#. R/W#(WR#) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. RW#/(WR#) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C# input. The E(RD#) input serves as data latch signal (clock) when high provided that CS# is low and high respectively. Refer to Figure 26 of parallel timing characteristics for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 3 below.

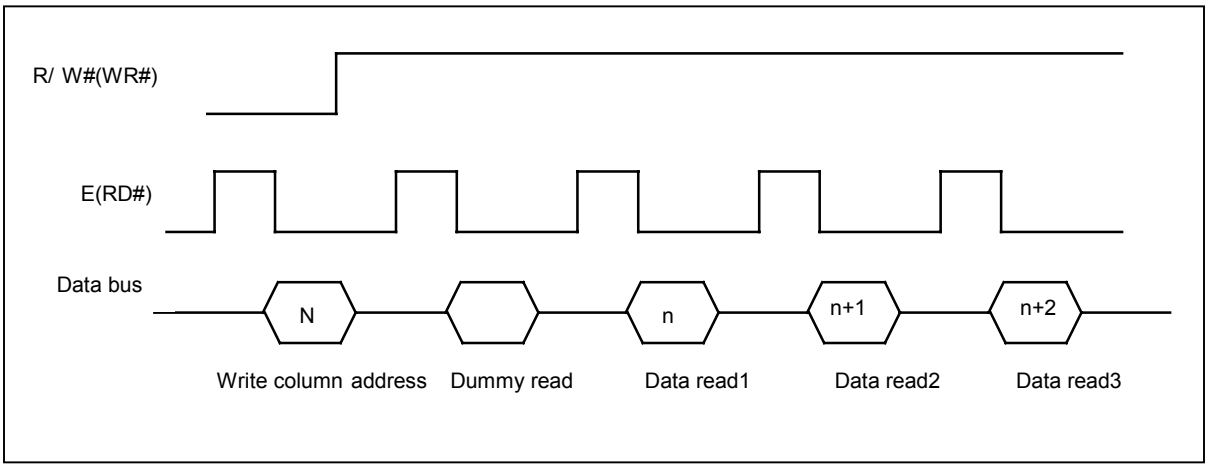


Figure 3 - Display data read back procedure - insertion of dummy read

6.5 MPU Parallel 8080-series Interface

The parallel interface consists of 16 bi-directional data pins (D_{15}-D_0) or 8 bi-directional data pins (D_7-D_0), E (RD#), R/W#(WR#), D/C# and CS#. The E(RD#) input serves as data read latch signal (clock) when low, provided that CS# is low and high respectively. Display data or status register read is controlled by D/C#.

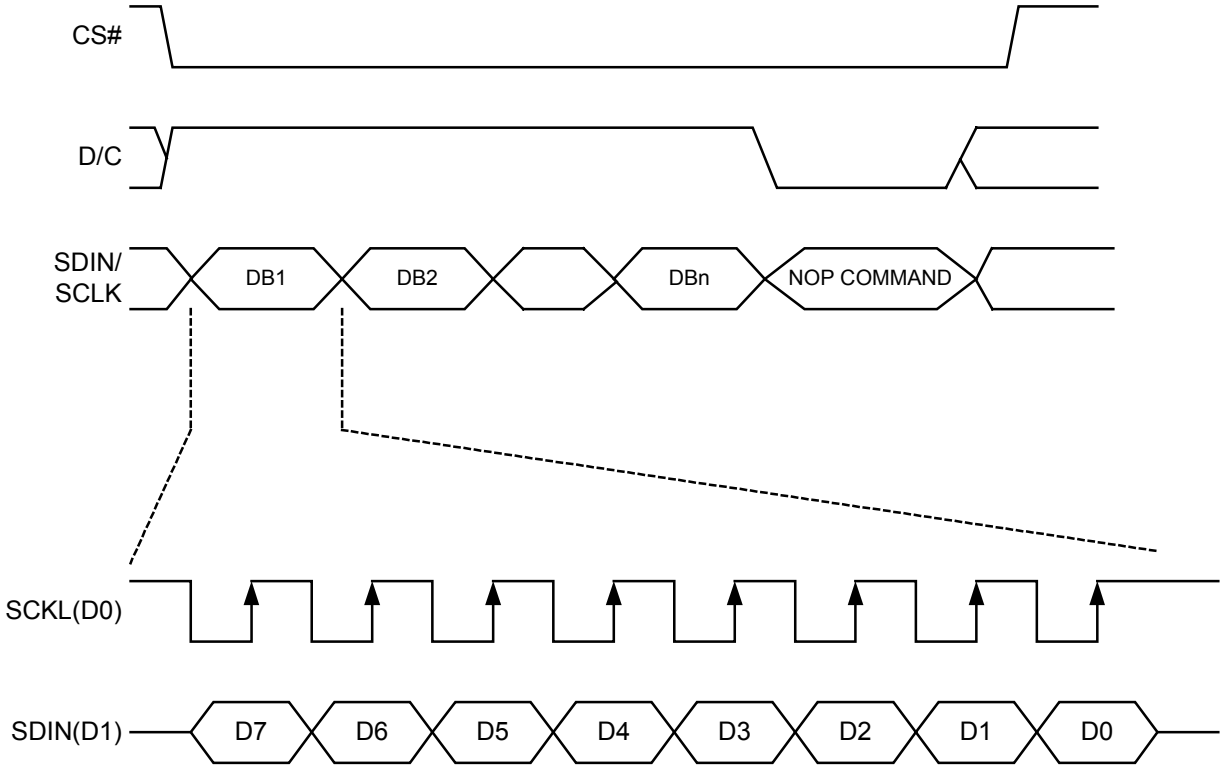
R/W#(WR#) input serves as data write latch signal (clock) when high provided that CS# is low and high respectively. Display data or command register write is controlled by D/C#. Refer to Figure 27 of parallel timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor. Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

6.6 MPU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D_7, D_6, ... D_0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

During data writing, an additional NOP command should be inserted before the CS# goes high (Refer to Figure 4.

Figure 4 - Display data write procedure in SPI mode



6.7 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 x 133 x 18bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

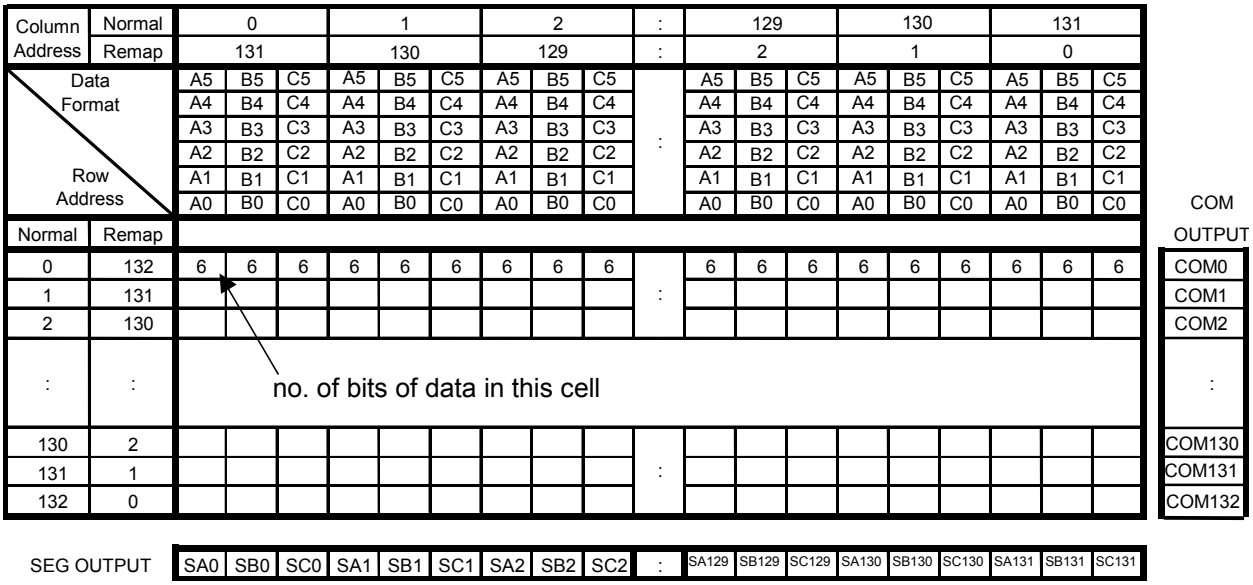


Figure 5 – 262k Color Depth Graphic Display Data RAM Structure

To send 262k, 18-bit, image data to the OLED driver in 16-bit MCU interface, the communication session is divided into two times. In below, "X" stands for don't care value.

	Bit15	Bit14	Bit13	…	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	…	Bit 1	Bit 0
1st word	X	X	X	…	X	X	X	X	C5	C4	…	C1	C0
2nd word	X	X	B5	…	B1	B0	X	X	A5	A4	…	A1	A0

Figure 6 – 262k Color Depth Graphic Display Data Writing Sequence in 16-bit MCU Interface

To send 262k, 18-bit, image data to the OLED driver in 8-bit MCU interface, the communication session is divided into three times.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1st byte	X	X	C5	C4	C3	C2	C1	C0
2nd byte	X	X	B5	B4	B3	B2	B1	B0
3rd byte	X	X	C5	C4	C3	C2	C1	C0

Figure 7 – 262k Color Depth Graphic Display Data Writing Sequence in 8-bit MCU Interface

Writing a 65K pixel in 16-bit MCU interface involves one session as follows.

	Bit15	Bit14	…	Bit11	Bit10	Bit 9	…	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1st word	C4	C3	…	C0	B5	B4	…	B0	A4	A3	A2	A1	A0

Figure 8 – 65k Color Depth Graphic Display Data Writing Sequence in 16-bit MCU Interface

The sequence of sending 65K color depth pixel in 8-bit MCU interface is divided into two 8-bit sessions as shown below.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1st byte	C4	C3	C2	C1	C0	B5	B4	B3
2nd byte	B2	B1	B0	A4	A3	A2	A1	A0

Figure 9 – 65k Color Depth Graphic Display Data Writing Sequence in 8-bit MCU Interface

In 256-color mode, each pixel is composed of 8-bit. Color A uses 2-bit while color B and color C each is represented by 3-bit. Although only 8 bits are required to represent one pixel, each pixel occupies 16-bit space inside graphic display data RAM with format as follows. In addition, only 8-bit MCU interface is available to 256-color mode.

For 256-color mode, one pixel data is sent in a 8-bit session like below.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1st byte	C2	C1	C0	B2	B1	B0	A1	A0

Figure 11 – 256 Color Depth Graphic Display Data Writing Sequence in 8-bit MCU Interface

Color C (3 bits)	RAM Content (5 bits)
000	00000
001	00100
010	01000
011	01100
100	10010
101	10110
110	11010
111	11110

Color B (3 bits)	RAM Content (6 bits)
000	000000
001	001000
010	010000
011	011000
100	100100
101	101100
110	110100
111	111100

Color A (2 bits)	RAM Content (5 bits)
00	00000
01	01000
10	10100
11	11100

Figure 10 – 256 Color Depth Graphic Display Data RAM Structure for One Pixel

6.8 Gray Scale and Gray Scale Table

Controlling the current pulse widths from the segment driver in the current drive phase produces the gray scale display. The gray scale table stores the corresponding pulse widths (PW0 ~ PW63) of the 64 gray scale levels (GS0~GS63). The wider the pulse width, the brighter the pixel will be. Therefore, the brightness of each pixel is defined in the graphic display data RAM in term of pulse width in gray scale table.

This single gray scale table supports all the three colors A, B and C. The pulse widths are entered by software commands.

In 262k-color depth, 6 bits represent each color. So color A, B and C each has 64 gray scale levels.

Color A, B, C RAM data (6 bits)	Gray Scale
0	GS 0
1	GS 1
2	GS 2
3	GS 3
4	GS 4
:	:
:	:
:	:
60	GS 60
61	GS 61
62	GS 62
63	GS 63

Figure 11 – Relation between graphic data RAM value and gray scale table entry for three colors in 262K-color mode

However, the situation is different in 65k color depth mode. As shown in figure below, color B sub-pixel RAM data has 6 bits, represent the 64 gray scale levels from GS0 to GS63. color A and color C sub-pixel RAM data has only 5 bits, represent 32 gray scale levels from GS0, GS2, …, GS62.

Color A, C RAM data (5 bits)	Color B RAM data (6 bits)	Gray Scale
0	0	GS0
-	1	GS 1
1	2	GS 2
-	3	GS 3
2	4	GS 4
:	:	:
:	:	:
:	:	:
30	60	GS 60
-	61	GS 61
31	62	GS 62
-	63	GS 63

Figure 12 – Relation between graphic data RAM value and gray scale table entry for three colors in 65K-color mode

In *65k* color depth mode, the meaning of values inside data RAM with respect to the gray scale level is best to be illustrated in an example below.

Gray Scale (Pulse Width)	Value/DCLKs
PW0	0
PW1	2
PW2	5
:	:
PW62	120
PW63	125

Gray Scale Table

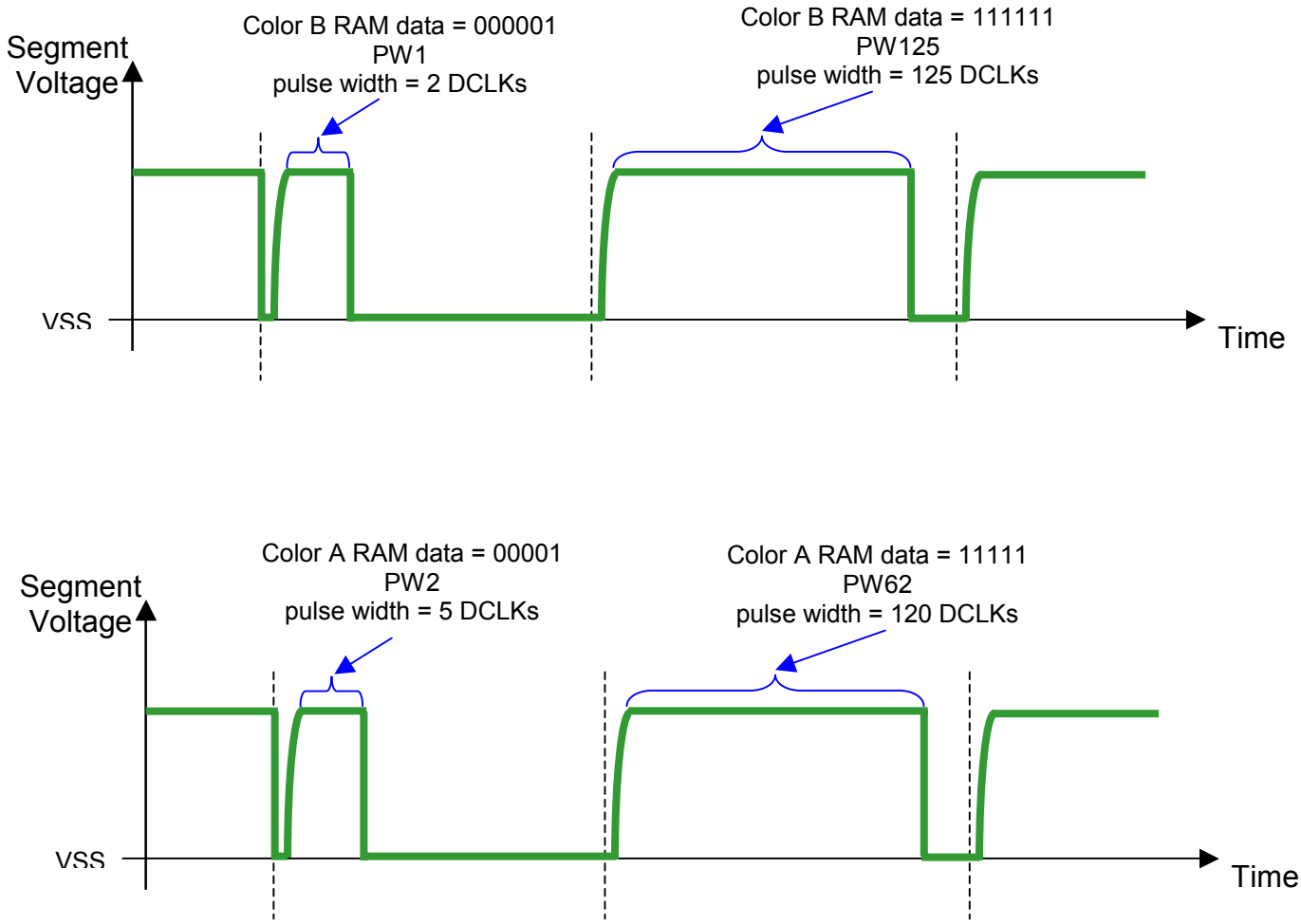


Figure 13 – illustration of relation between graphic display RAM value and gray scale control in 65K color depth mode

6.9 Current Control and Voltage Control

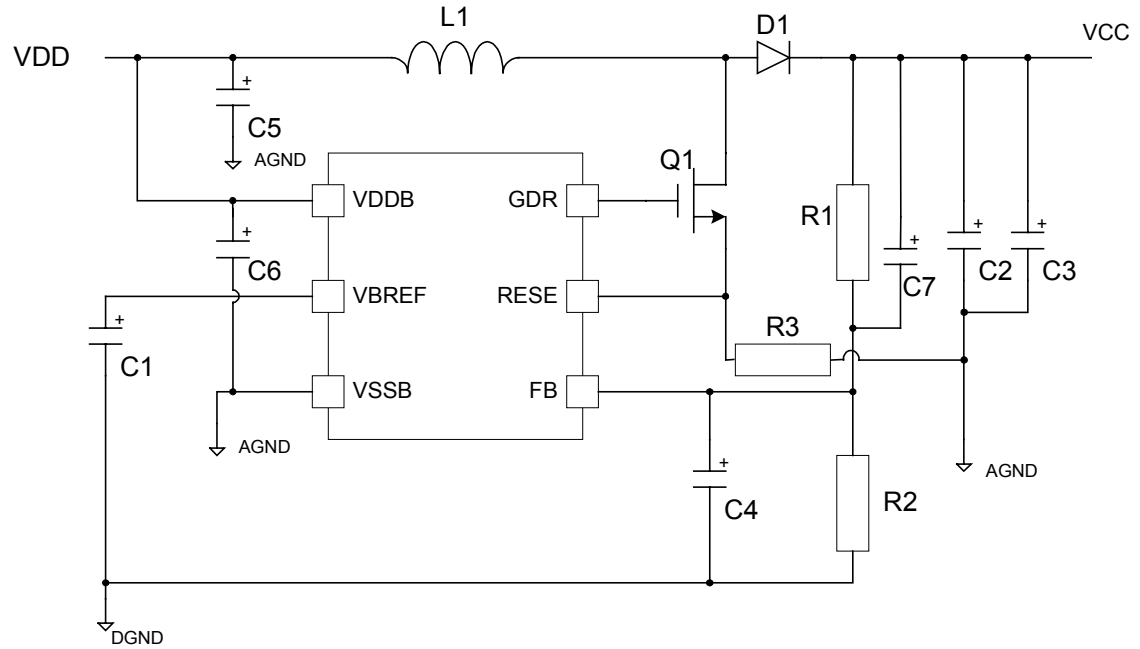
This block is used to derive the incoming power sources into the different levels of internal use voltage and current. V_{CC} and V_{DD} are external power supplies. V_{REF} is reference voltage, which is used to derive driving voltage for segments and commons. I_{REF} is a reference current source for segment current drivers.

6.10 Segment Drivers/Common Drivers

Segment drivers deliver 396 current sources to drive OLED panel. The driving current can be adjusted from 0 to 200uA with 256 steps. Common drivers generate voltage scanning pulse.

6.11 DC-DC Voltage Converter

It is a switching voltage generator circuit, designed for handheld applications. In SSD1338, internal DC-DC voltage converter accompanying with an external application circuit (shown in below figure) can generate a high voltage supply V_{CC} from a low voltage supply input V_{DD}. V_{CC} is the voltage supply to the OLED driver block. Below application circuit is an example for the input voltage of 3V VDD to generate V_{CC} of 12V @20mA ~ 30mA application.



*ALL PATHS TO AGND SHOULD BE CONNECTED AS SHORT AS POSSIBLE

Passive components selection:

Components	Typical Value	Remark
L1	Inductor, 22μH	2A
D1	Schottky diode	2A, 25V e.g. 1N5822
Q1	MOSFET	N-FET with low R_{DS}(on) and low Vth voltage. e.g. MGSF1N02LT1 [ON SEMICONDUCTOR]
R1, R2	Resistor	1%,1/10W
R3	Resistor, 1.5Ω	1%, 1/2W
C1	Capacitor, 1μF	16V
C2	Capacitor, 22μF	Low ESR, 25V
C3	Capacitor, 1μF	16V
C4	Capacitor, 10nF	16V
C5	Capacitor, 1 ~ 10 μF	16V
C6	Capacitor, 0.1 ~ 1μF	16V
C7	Capacitor, 15nF	16V

The VCC output voltage level can be adjusted by R1and R2, the reference formula is:

VCC = 1.2 x (R1+R2) / R2

7. COMMAND TABLE

Table 2 - Command table

(**D/$\overline{C}$** = 0, **R/$\overline{W}$** (**$\overline{WR}$**) = 0, E(**$\overline{RD}$**) = 1) unless specific setting is stated
Single byte command (D/$\overline{C}$ = 0), Multiple byte command (D/$\overline{C}$ = 0 for first byte, D/$\overline{C}$ = 1 for other bytes)

D/C	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	15	0	0	0	1	0	1	0	1	Set Column Address	A[7:0]: Start Address, reset=0d
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[7:0]: End Address, reset=131d
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		Range from 0d to 131d
0	75	0	1	1	1	0	1	0	1	Set Row Address	A[7:0]: Start Address, reset=0d
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[7:0]: End Address, reset=131d
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		Range from 0d to 131d
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0	A0	1	0	1	0	0	0	0	0	Set Re-map / Color Depth(Display RAM to Panel)	A[0]=0, Horizontal address increment (POR) A[0]=1, Vertical address increment A[1]=0, Column address 0 is mapped to SEG0 (POR) A[1]=1, Column address 95 is mapped to SEG0 A[2]=0, Color A , C normal (POR) A[2]=1, Color A and C is swapped A[4]=0, Scan from COM 0 to COM [N –1] (POR) A[4]=1, Scan from COM [N-1] to COM0. Where N is the Multiplex ratio. A[5]=0, Disable COM Split Odd Even (POR) A[5]=1, Enable COM Split Odd Even A[7:6] Set Color Depth, 00 256 color 01 65K color, (POR) 10 262k color in 8-bit MCU interface 11 262k color in 16-bit MCU interface
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	A1	1	0	1	0	0	0	0	1	Set Display Start Line	Set vertical scroll by RAM from 0~131 [reset=00d]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

D/C	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	A2	1	0	1	0	0	0	1	0	Set Display Offset	Set vertical scroll by Row from 0-131. [reset=00b]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	A4~A7	1	0	1	0	0	1	X_1	X_0	Set Display Mode	A4: All Off A5: All On (All pixels have GS15) A6 : Reset to normal display (POR) A7: Inverse Display (GS0 -> GS63, GS1 -> GS62, ...)
0	AD	1	0	1	0	1	1	0	1	Master Configuration	A[7:0] should be set as 100011A[1]A[0]b A[0]= 0 Select external VCC supply at master ON A[0] = 1 Select internal booster at master ON [reset] A[1]= 0 Select external VCOMH voltage supply at master ON A[1] = 1 Select internal VCOMH regulator at master ON [reset]
1	A[7:0]	1	0	0	0	1	1	A_1	A_0		
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Sleep mode On/Off	AE = Sleep mode On (Display off) AF = Sleep mode Off (Display on)
0	B1	1	0	1	1	0	0	0	1	Set Reset (Phase 1) /Pre-charge (Phase 2) period	A[3:0] Phase 1 period of 1~16 dclk clocks [reset=4h]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:4] Phase 2 period of 1~16 dclk clocks [reset=7h]
0	B3	1	0	1	1	0	0	1	1	Front Clock Divider (DivSet)/ Oscillator Frequency	A[3:0] [reset=0], divide by DIVSET+1 (i.e. 1 to 16)
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:4] Osc frequency, frequency increase as level increase [reset=1001b]
0	B8	1	0	1	1	1	0	0	0	Look Up Table for Gray Scale Pulse width	The next 32 bytes of command set the current drive pulse width of gray scale level GS1, GS3, GS5 …GS63 as below in unit of DCLK. A[7:0] : PW1, POR =1 DCLK
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[7:0] : PW3, POR = 5 DCLK
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		C[7:0] : PW5, POR = 9 DCLK
1	.	.	.	.	.	.	.	.	.		.
1	.	.	.	.	.	.	.	.	.		.
1	.	.	.	.	.	.	.	.	.		AE[7:0] : PW61, POR = 121 DCLK
1	.AE[7:0]	AE_7	AE_6	AE_5	AE_4	AE_3	AE_2	AE_1	AE_0		AF[7:0] : PW63, POR = 123 DCLK
1	AF[7:0]	AF_7	AF_6	AF_5	AF_4	AF_3	AF_2	AF_1	AF_0		where PW1 must > 0 PW3 must > PW1+1 PW5 must > PW3+1 Note: GS0 has no pre-charge and current drive stages. For GS2 GS4…GS62, they are derived by driver itself with: PWn = (PW_{n-1}+PW_{n+1})/2 Max pulse width is 125

D/C	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	B9	1	0	1	1	1	0	0	1	Use Built-in Linear LUT (reset= linear)	Reset to default Look Up Table: PW1 = 1 PW2 = 3 PW3 = 5 PW4 = 7 ... PW62 = 123 PW63 = 125
0 1 1 1	BB A[7:0] B[7:0] C[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	1 A_3	0 A_2	1 A_1	1 A_0	Set Pre-charge voltage of Color A B C	A[7:0] Pre-charge Color A [reset = 00011100] B[7:0] Pre-charge Color B [reset = 00011100] C[7:0] Pre-charge Color C [reset = 00011100] 00000000 0.51*Vref ..... 00011111 0.84*Vref 01011111 1.0*Vref 1xxxxxxx connects to VCOMH
0 1	BE A[6:0]	1 *	0 A_6	1 A_5	1 A_4	1 A_3	1 A_2	1 A_1	0 A_0	Set VCOMH	A[6:0] 0000000 0.51*Vref ..... 0011111 0.84*Vref [VCOMHSET, reset] 1011111 1.0*Vref
0 1 1 1	C1 A[7:0] B[7:0] C[7:0]	1 A_7 B_7 C_7	1 A_6 B_6 C_6	0 A_5 B_5 C_5	0 A_4 B_4 C_4	0 A_3 B_3 C_3	0 A_2 B_2 C_2	0 A_1 B_1 C_1	1 A_0 B_0 C_0	Contrast Current for Color A,B,C	A[7:0] Contrast Value Color A [reset=1000000b] B[7:0] Contrast Value Color B [reset=1000000b] C[7:0] Contrast Value Color C [reset=1000000b]
0 1	C7 A[3:0]	1 *	1 *	0 *	0 *	0 A_3	1 A_2	1 A_1	1 A_0	Master Contrast Current Control	A[3:0] : 0000 reduce output currents for all colors to 1/16 0001 reduce output currents for all colors to 2/16 .... 1110 reduce output currents for all colors to 15/16 1111 no change [reset = 1111b]
0 1	CA A[7:0]	1 A_7	1 A_6	0 A_5	0 A_4	1 A_3	0 A_2	1 A_1	0 A_0	Set Mux Ratio	A[7:0] mux ratio 16MUX ~ 132MUX, [reset=131d], (Range from 15d to 131d)
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

Table 3 - Graphic Acceleration Command

Set (GAC) (**D/$\overline{C}$** = 0, **R/$\overline{W}$** (**$\overline{WR}$**) = 0, E(**$\overline{RD}$**) = 1) unless specific setting is stated
Single byte command (D/$\overline{C}$ = 0), Multiple byte command (D/$\overline{C}$ = 0 for first byte, D/$\overline{C}$ = 1 for other bytes)

D/C	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	83	1	0	0	0	0	0	1	1	Draw Line	A[7:0] : Column Address of Start
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[7:0] : Row Address of Start
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		C[7:0] : Column Address of End
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		D[7:0] : Row Address of End
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		E[7:0] : Line Color - CCCCCBBB
1	E[7:0]	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		F[7:0] : Line Color - BBBAAAAA
1	F[7:0]	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		* A < C < 132
											* B < D < 132
0	84	1	0	0	0	0	1	0	0	Draw Rectangle	A[7:0] : Column Address of Start
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[7:0] : Row Address of Start
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		C[7:0] : Column Address of End
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		D[7:0] : Row Address of End
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		E[7:0] : Line Color - CCCCCBBB
1	E[7:0]	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		F[7:0] : Line Color - BBBAAAAA
1	F[7:0]	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		G[7:0] : Fill Color - CCCCCBBB
1	G[7:0]	G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		H[7:0] : Fill Color - BBBAAAAA
1	H[7:0]	H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		* A < C < 132
											* B < D < 132
0	86	1	0	0	0	0	1	1	0	Draw Circle	A[7:0] : Column Address of Centre
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[7:0] : Row Address of Centre
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		C[7:0] : Radius
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		D[7:0] : Line Color - CCCCCBBB
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		E[7:0] : Line Color - BBBAAAAA
1	E[7:0]	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		F[7:0] : Fill Color - CCCCCBBB
1	F[7:0]	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		G[7:0] : Fill Color – BBBAAAAA
1	G[7:0]	G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	8A	1	0	0	0	1	0	1	0	Copy	A[7:0] : Column Address of Start
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[7:0] : Row Address of Start
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		C[7:0] : Column Address of End
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		D[7:0] : Row Address of End
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		E[7:0] : Column Address of New Start
1	E[7:0]	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		F[7:0] : Row Address of New Start
1	F[7:0]	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		* A < C < 132
											* B < D < 132

D/C	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	8C	1	0	0	0	1	1	0	0	Dim Window	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End * A < C < 132 * B < D < 132
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	8E	1	0	0	0	1	1	1	0	Clear Window	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End * A < C < 132 * B < D < 132
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	92	1	0	0	1	0	0	1	0	Fill Enable / Disable	A0 0 : Disable Fill for Draw Rectangle/Circle Command [reset] 1 : Enable Fill for Draw Rectangle/Circle Command A4 0 : Disable reverse copy, reset] 1 : Enable reverse during copying. A5 0 : Disable x-wrap, [reset] 1 : Enable wrap around in x-direction during copying
1	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	96	1	0	0	1	0	1	1	0	Horizontal Scroll	A[7:0] : 1~131 horizontal offset in number of Column 0 no horizontal scroll B[7:0] : start row address C[7:0] : number of rows to be H-scrolled B+C <= 132 D[7:0] : Reserved E[1:0] : scrolling time interval 0 test mode (~0.1 seconds) 1 64 frames (~0.6 seconds) 2 128 frames (~1.3 seconds) 3 256 frames (~2.6 seconds) Note : operates during display on.
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[1:0]	*	*	*	*	*	*	E_1	E_0		
0	9E	1	0	0	1	1	1	1	0	Stop Moving	
0	9F	1	0	0	1	1	1	1	1	Start Moving	

8. COMMAND DESCRIPTIONS

Set Column Address (15h)
This command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address.

Set Row Address (75h)
This command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

For example, column start address is set to 2 and column end address is set to 129, row start address is set to 1 and row end address is set to 130. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 129 and from row 1 to row 130 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation. Whenever the column address pointer finishes accessing the end column 129, it is reset back to column 2 and row address is automatically increased by 1. While the end row 130 and end column 129 RAM location is accessed, the row address is reset back to 1. The diagram below shows the way of column and row address pointer movement for this example.

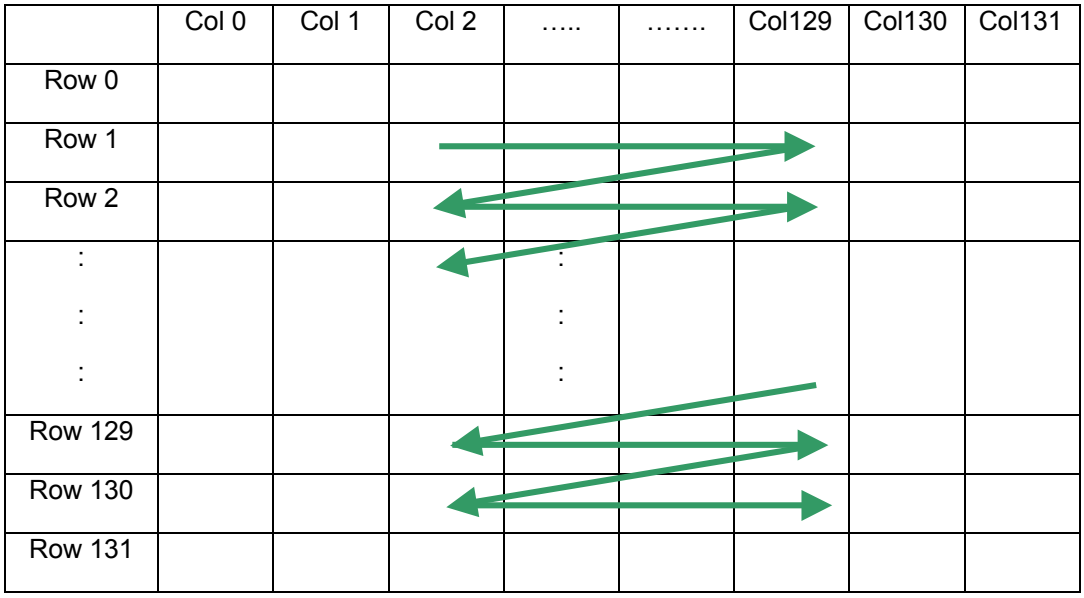


Figure 14 – Example of Column and Row Address Pointer Movement

Write RAM Command (5Ch)
After this single byte command, data entries will be written into the display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before write data into RAM.

Read RAM Command (5Dh)
After this single byte command, data is read from display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before read data from RAM.

Set Re-map & Color Depth (A0h)
This command has multiple configurations and each bit setting is described as follows.

- Address increment mode (A[0])
  When it is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 15.

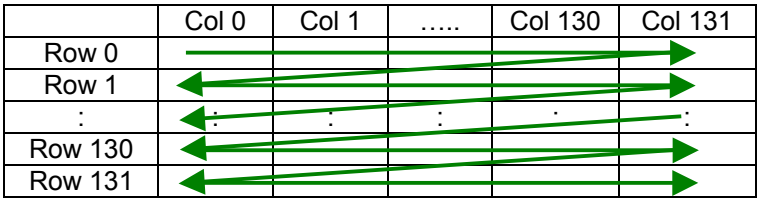


Figure 15 – Address Pointer Movement of Horizontal Address Increment Mode

When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read/written, the row address pointer is increased automatically by 1. if the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 16.

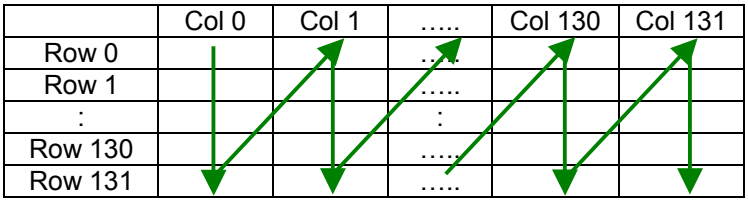


Figure 16 – Address Pointer Movement of Vertical Address Increment Mode

- Column Address Mapping (A[1])
  This command bit is made for flexible layout of segment signals in OLED module with segment arranged from left to right or vice versa.

- COM Remap (A[4])
  This bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa.

- Odd even split of COM pins (A[5])
  This bit can set the odd even arrangement of COM pins.
  A[5] = 0: Disable COM split odd even, pin assignment of common is in sequential as

COM131 COM129 .... COM 33 COM32..SC131..SA0..COM0 COM1.... COM30 COM31

A[5] = 1: Enable COM split odd even, pin assignment of common is in odd even split as
COM131 COM129.... COM3 COM1..SC131..SA0..COM0 COM2.... COM60 COM62

- Display color mode (A[7:6])
  Select either 262k, 65k or 256 color mode. The display RAM data format in different mode is described in section "Graphic Display Data RAM (GDDRAM)".

Set Display Start Line (A1h)

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 131. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

	132	132	130	130	Mux ratio
COM Pin	0	4	0	4	Display start line
COM0	Row0	Row4	Row0	Row4	
COM1	Row1	Row5	Row1	Row5	
COM2	Row2	Row6	Row2	Row6	
COM3	Row3	Row7	Row3	Row7	
:	:	:	:	:	
:	:	:	:	:	
COM125	Row125	Row129	Row125	Row129	
COM126	Row126	Row130	Row126	Row130	
COM127	Row127	Row131	Row127	Row131	
COM128	Row128	Row0	Row128	Row0	
COM129	Row129	Row1	Row129	Row1	
COM130	Row130	Row2	-	-	
COM131	Row131	Row3	-	-	

Figure 17 – Example of Set Display Start Line with no Remap

Set Display Offset (A2h)

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-131. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

	132	132	130	130	Mux ratio
COM Pin	0	4	0	4	Display offset
COM0	Row0	Row4	Row0	Row4	
COM1	Row1	Row5	Row1	Row5	
COM2	Row2	Row6	Row2	Row6	
COM3	Row3	Row7	Row3	Row7	
:	:	:	:	:	
:	:	:	:	:	
COM125	Row125	Row129	Row125	Row129	
COM126	Row126	Row130	Row126	-	
COM127	Row127	Row131	Row127	-	
COM128	Row128	Row0	Row128	Row0	
COM129	Row129	Row1	Row129	Row1	
COM130	Row130	Row2	-	Row2	
COM131	Row131	Row3	-	Row3	

Figure 18 – Example of Set Display Offset with no Remap

Set Display Mode (A4h ~ A7h)
These are single byte command and they are used to set Normal Display, Entire Display On, Entire Display Off and Inverse Display.

- Set Entire Display On (A5h)
  Forces the entire display to be at "GS63" regardless of the contents of the display data RAM.
- Set Entire Display Off (A6h)
  Forces the entire display to be at gray level "GS0" regardless of the contents of the display data RAM.
- Inverse Display (A7h)
  The gray level of display data are swapped such that "GS0" <-> "GS63", "GS1" <-> "GS62", ….
- Normal Display (A4h)
  Reset the above effect and turn the data to ON at the corresponding gray level.

Master Configuration (ADh)
This command contains multiple bits to control several functionalities of the driver.

- Select DC-DC converter (A[0])
  0 = Disable selection of DC-DC converter and VCC is supplied externally.
  1 (POR) = Enable selection of DC-DC converter to supply high voltage to VCC. The output voltage of the converter is set by values of external resistors. Please refer to section "DC-DC Voltage Converter" for details.
- Select V_{COMH} supply (A[1])
  0 = Select external V_{COMH} voltage from V_{COMH} pin for the common waveform high voltage level supply. It is recommended to set the voltage of V_{COMH} such that the OLED pixel diode is not turned on (prefer in reverse bias state) when the segment pin is either driven to V_{PA}, V_{PB} or V_{PC} level.
  1 = Select internal V_{COMH} voltage generated by regulator from V_{REF}. The level of V_{COMH} can be programmed by command BEh.
- Select pre-charge voltage supply (A[2])
  0 = Select pre-charge voltage sources from external pins V_{PA}, V_{PB}, V_{PC} for color A, B and C respectively.
  1 = Select pre-charge voltage supply internally. The level of V_{PA}, V_{PB}, V_{PC} can be set by command BBh for color A, B and C respectively.

Set Sleep mode On/Off (AEh/AFh)
These single byte commands are used to turn the OLED panel display on or off. When the display is on, the selected circuits by Set Master Configuration command will be turned on. When the display is off, those circuits will be turned off and the segment and common output are in high impedance state.

Set Reset (Phase 1)/ Pre-charge (Phase 2) period (B1h)
This command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period from 1 to 16 in the unit of DCLKs. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 1 to 16 in the unit of DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_{PA}, V_{PB}, V_{PC} for color A, B and C respectively.

Front Clock Divider (DivSet)/ Oscillator Frequency (B3h)
This command consists of two functions:

- Display Clock Divide Ratio (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with power on reset value = 1. Please refer to section "Oscillator Circuit and Display Time Generator" for the details of DCLK and CLK.
- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc which is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency setting available as shown below. The default value is 1101b.

Look Up Table for Gray Scale Pulse width (B8h)
This command is used to set the gray scale table for the display. Except gray scale entry 0, which is zero as it has no pre-charge and current drive, each odd entry gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter is the OLED pixel when it's turned on. Please refer to section "Graphic Display Data RAM (GDDRAM)" for more detailed explanation of relation of display data RAM, gray scale table and the pixel brightness.

Following the command B8h, the user has to set the pulse width from PW1, PW3, PW5, …, PW59, PW61, PW63 one by one in sequence and complies the following conditions.

$$PW1 > 0; PW3 > PW1 + 1; PW5 > PW3 + 1; \ldots\ldots$$

Afterwards, the driver automatically derives the pulse width of even entry of gray scale table PW2, PW4, …, PW62 with the formula like below.

$$PWn = (PWn-1 + PWn+1) / 2$$

For example, if PW1 = 3 DCLKs and PW3 = 7 DCLKs, PW2 = (3+7)/2 = 5 DCLKs

The setting of gray scale table entry can perform gamma correction on OLED panel display. Normally, it is desired that the brightness response of the panel is linearly proportional to the image data value in display data RAM. However, the OLED panel is somehow responded in non-linear way. Appropriate gray scale table setting like example below can compensate this effect.

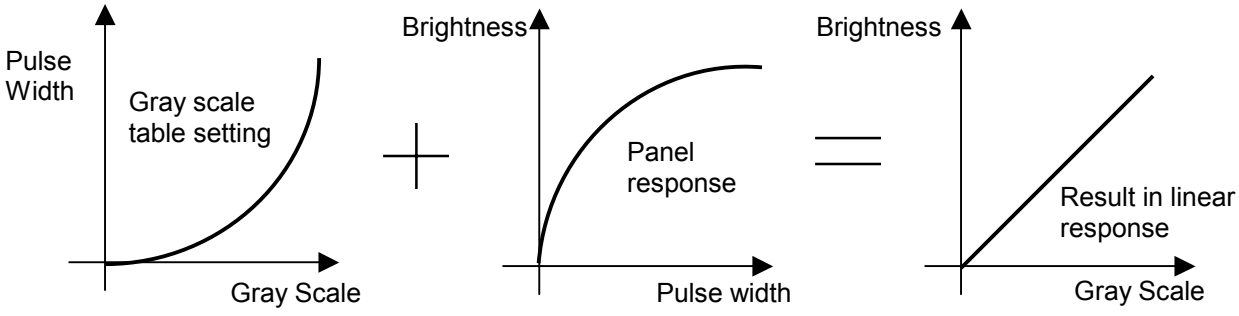


Figure 19 – Example of gamma correction by gray scale table setting

Use Built-in Linear LUT (B9h)
This command reloads the preset linear gray scale table as PW1 = 1, PW2 = 3, PW3 = 5, …., PW62 = 123, PW63 = 125 DCLKs.

Set Pre-charge voltage of Color A, B and C (BBh)
This command is used to set V_{PA}, V_{PB} and V_{PC} phase 2 voltage level for color A, B and C respectively. The command is valid in condition that these voltages are selected to generate internally by command ADh. It can be programmed to set the pre-charge voltage reference to V_{REF} or V_{COMH}.

Set V_{COMH} (BEh)
This command sets the high voltage level of common pins, V_{COMH}, when it is selected to generate internally by command ADh. The level of V_{COMH} is programmed with reference to V_{REF}.

Contrast Current for Color A, B, C (C1h)
This command is to set Contrast Current of each color A, B and C. The chip has three contrast control circuits for color A, B and C. Each contrast circuit has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases linearly with the contrast step, which results in brighter of the color. This relation is shown in Figure 20. In many situations, the output brightness of color A, B and C pixels are different under the same segment current condition. The contrasts of color A, B and C are set such that the brightness of each color are the same on the OLED panel

Master Contrast Current Control (C7h)

This command is to control the segment output current by a scale factor. This factor is common to color A, B and C. The chip has 16 master control steps. The factor is ranged from 1 [0000] to 16 [1111]. POR is 16 [1111]. The smaller the master current value, the dimmer the OLED panel display is set. For example, if original segment output current of a color is 160uA at scale factor = 16, setting scale factor to 8 to reduce the current to 80uA. Please see Figure 20.

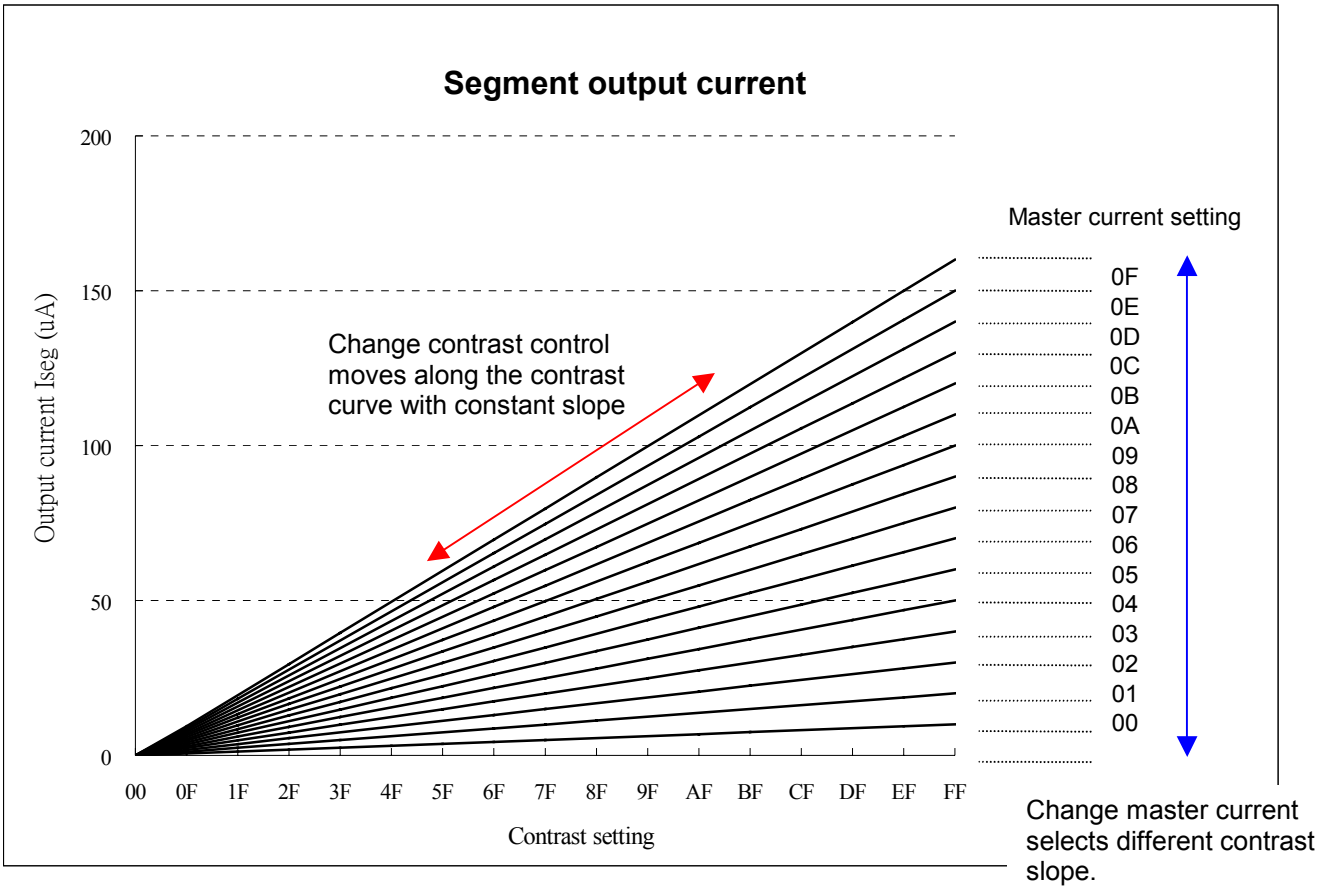


Figure 20 – Segment Output Current for Different Contrast Control and Master Current Setting

Set Multiplex Ratio (CAh)

This command switches default 1:132 multiplex mode to any multiplex mode from 16 to 132. For example, when multiplex ratio is set to 16, only 16 common pins are enabled. The starting and the ending of the enabled common pins are depended on the setting of "Display Offset" register programmed by command A2h.

Graphic Acceleration command set description

Draw Line (83h)
This command draws a line by the given start, end column and row coordinates and the color of the line.

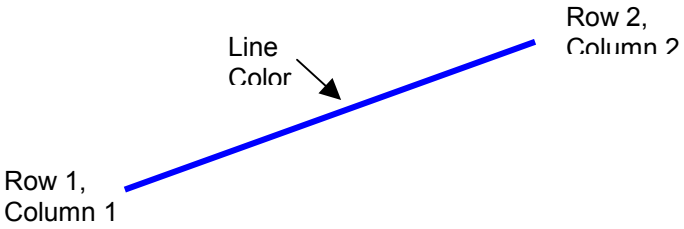


Figure 21 – Example of Draw Line Command

For example, the line above can be drawn by the following command sequence.

1. Enter into draw line mode by command 21h
2. Send column start address of line, column1, for example = 1h
3. Send row start address of line, row 1, for example = 10h
4. Send column end address of line, column 2, for example = 28h
5. Send row end address of line, row 2, for example = 4h
6. Send color C, B and A of line, for example = 35d, 0d, 0d for blue color

Draw Rectangle (84h)
Given the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2), specify the outline and fill area colors, a rectangle that will be drawn with the color specified. Remarks: If fill color option is disabled, the enclosed area will not be filled.

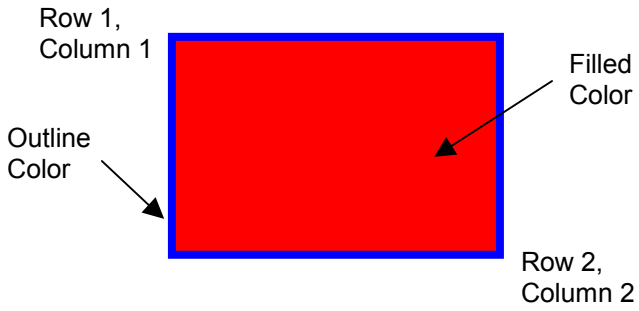


Figure 22 – Example of Draw Rectangle Command

The following example illustrates the rectangle drawing command sequence.

1. Enter the “draw rectangle mode” by execute the command 22h
2. Set the starting column coordinates, Column 1. e.g., 03h.
3. Set the starting row coordinates, Row 1. e.g., 02h.
4. Set the finishing column coordinates, Column 2. e.g., 12h
5. Set the finishing row coordinates, Row 2. e.g., 15h
6. Set the outline color C, B and A. e.g., (28d, 0d, 0d) for blue color
7. Set the filled color C, B and A. e.g., (0d, 0d, 40d) for red color

Draw Circle (86h)
By providing the center coordination (column and row address) and radius length, specify the outline and fill area colors, a circle will be drawn with the colors specified.

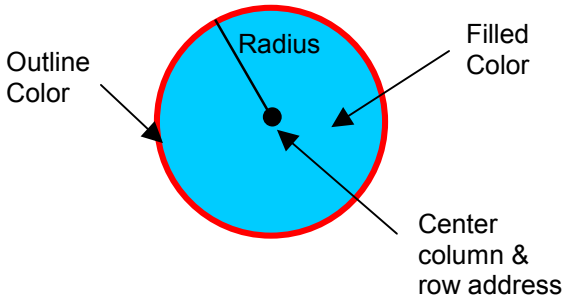


Figure 23 – Example of Draw Circle Command

The following example illustrates the circle drawing command sequence.

1. Enter the “draw circle mode” by execute the command 86h
2. Set the circle center column coordinates, e.g., 03h.
3. Set the circle center row coordinates. e.g., 10h.
4. Set the radius of circle. e.g., 12h
5. Set the outline color C, B and A. e.g., (0d, 0d, 40d) for red color
6. Set the filled color C, B and A. e.g., (28d, 0d, 0d) for blue color

Copy (8Ah)
Copy the rectangular region defined by the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to location (Row 3, Column 3). If the new coordinates are smaller than the ending points, the new image will overlap the original one.

The following example illustrates the copy procedure.

1. Enter the “copy mode” by execute the command 23h
2. Set the starting column coordinates, Column 1. E.g., 00h.
3. Set the starting row coordinates, Row 1. E.g., 00h.
4. Set the finishing column coordinates, Column 2. E.g., 05h
5. Set the finishing row coordinates, Row 2. E.g., 05h
6. Set the new column coordinates, Column 3. E.g., 03h
7. Set the new row coordinates, Row 3. E.g., 03h

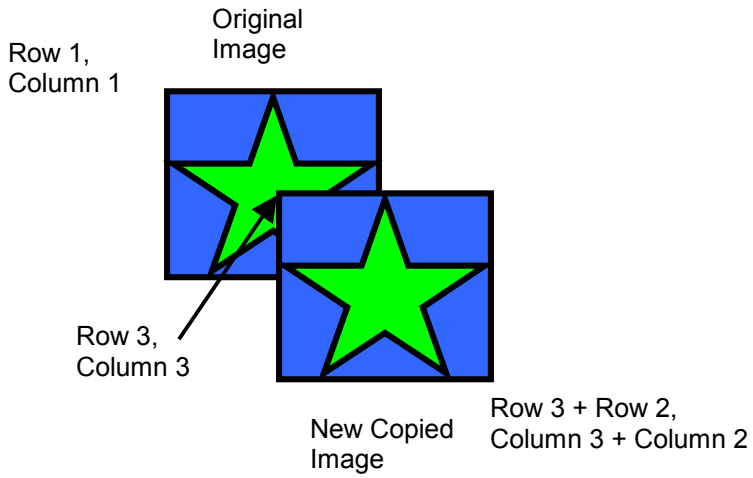


Figure 24 – Example of Copy Command

Dim Window (8Ch)
This command will dim the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2). After the execution of this command, the selected window area will become darker as follow.

Table 4 – Result of Change of Brightness by Dim Window Command

Original gray scale	New gray scale after dim window command
GS0 ~ GS15	No change
GS16 ~ GS19	GS4
GS20 ~ GS23	GS5
:	:
GS60 ~ GS63	GS15

Additional execution of this command over the same window area will not change the data content.

Clear Window (8Eh)
This command sets the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to clear the window display. The graphic display data RAM content of the specified window area will be set to zero.

This command can be combined with Copy command to make as a "move" result. The following example illustrates the copy plus clear procedure and results in moving the window object.

1. Enter the "copy mode" by execute the command 23h
2. Set the starting column coordinates, Column 1. E.g., 00h.
3. Set the starting row coordinates, Row 1. E.g., 00h.
4. Set the finishing column coordinates, Column 2. E.g., 05h
5. Set the finishing row coordinates, Row 2. E.g., 05h
6. Set the new column coordinates, Column 3. E.g., 06h
7. Set the new row coordinates, Row 3. E.g., 06h
8. Enter the "clear mode" by execute the command 24h
9. Set the starting column coordinates, Column 1. E.g., 00h.
10. Set the starting row coordinates, Row 1. E.g., 00h.
11. Set the finishing column coordinates, Column 2. E.g., 05h
12. Set the finishing row coordinates, Row 2. E.g., 05h

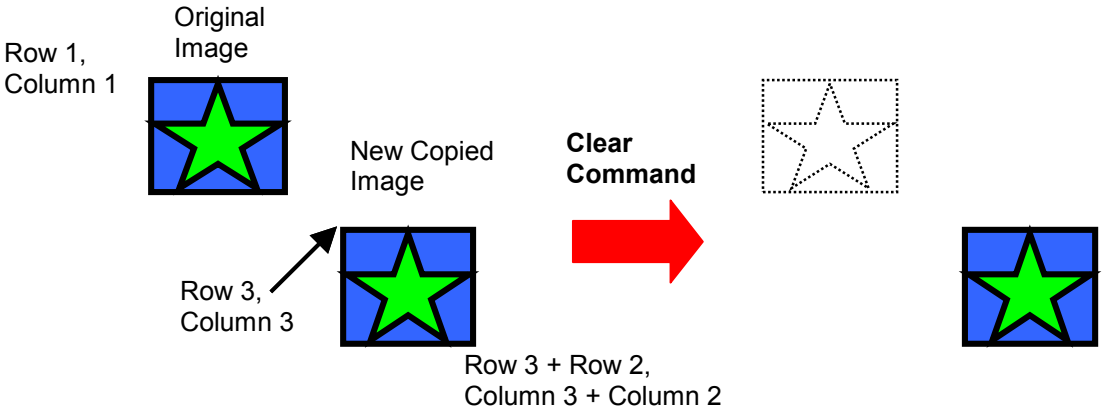


Figure 25 – Example of Copy + Clear = Move Command

Fill Enable/Disable (92h)
This command has two functions.

- Enable/Disable fill (A[0])
  0 = Disable filling of color into rectangle in draw rectangle command. (POR)
  1 = Enable filling of color into rectangle in draw rectangle command.
- Enable/Disable reverse copy (A[4])
  0 = Disable reverse copy (POR)
  1 = During copy command, the new image colors are swapped such that "GS0" <-> "GS63", "GS1" <-> "GS62", ….

Horizontal Scroll (96h)
This command consists of 5 consecutive bytes to set up the horizontal scroll parameters. It determined the scrolling start page, end page and the scrolling speed.

Before issuing this command, the horizontal scroll must be deactivated (9Eh). Otherwise, ram content may be corrupted.

Stop Moving (9Eh)
Stop motion of horizontal scrolling.

Start Moving (9Fh)
Start motion of horizontal scrolling. This command should only be issued after Horizontal scroll setup parameters are defined.

The following actions are prohibited after the horizontal scroll is activated

1. RAM access (Data write or read)
2. Changing horizontal scroll setup parameters

The SSD1338 horizontal scroll is designed for 132 columns scrolling

9. MAXIMUM RATINGS

Table 5 - Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{CC}		0 to 18	V
V_{REF}		0 to 18	V
V_{COMH}	Supply Voltage/Output voltage	0 to 16	V
-	SEG/COM output voltage	0 to 16	V
V_{in}	Input voltage	Vss-0.3 to Vdd+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

10. DC CHARACTERISTICS

Table 6 - DC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{cc}	Operating Voltage		7	11	18	V
V_{DD}	Logic Supply Voltage		2.4	2.7	3.5	V
V_{DDIO}	Power Supply for I/O pins		1.5	2.7	3.5	V
V_{OH}	High Logic Output Level	Iout =100uA, 3.3MHz	0.9*V_{DDIO}	-	V_{DDIO}	V
V_{OL}	Low Logic Output Level	Iout =100uA, 3.3MHz	0	-	0.1*V_{DDIO}	V
V_{IH}	High Logic Input Level	Iout =100uA, 3.3MHz	0.8*V_{DDIO}	-	V_{DDIO}	V
V_{IL}	Low Logic Input Level	Iout =100uA, 3.3MHz	0	-	0.2*V_{DDIO}	V
I_{SLEEP}	Sleep mode Current	VDD=2.7V, Display OFF, No panel attached	-	-	5	uA
I_{CC}	Vcc Supply Current	VDD=2.7V, Display ON Contrast =FF, No panel attached	-	-	-	uA
I_{DD}	V_{DD} Supply Current	VDD=2.7V, Display ON Contrast =FF, No panel attached	-	-	-	uA
I_{SEG}	Segment Output Current Setting VDD=2.7V, VCC=11V, IREF=10uA, All one pattern, Display on, Segment pin under test is connected with a 20KΩ resistive load to Vcc.	Contrast = FF	-	160	-	uA
		Contrast = AF		110		
		Contrast = 5F	-	60	-	
		Contrast = 00	-	0	-	
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG}[0:395] = Segment current at contrast = FF	-	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-	±2.0	--	%
Vcc	Booster output voltage (Vcc)	Vin=3V, L=22uH; R1=450Kohm; R2=50Kohm; Icc = 30mA(soaking)	-	12	-	V

11. AC CHARACTERISTICS

Table 7 - AC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C.)

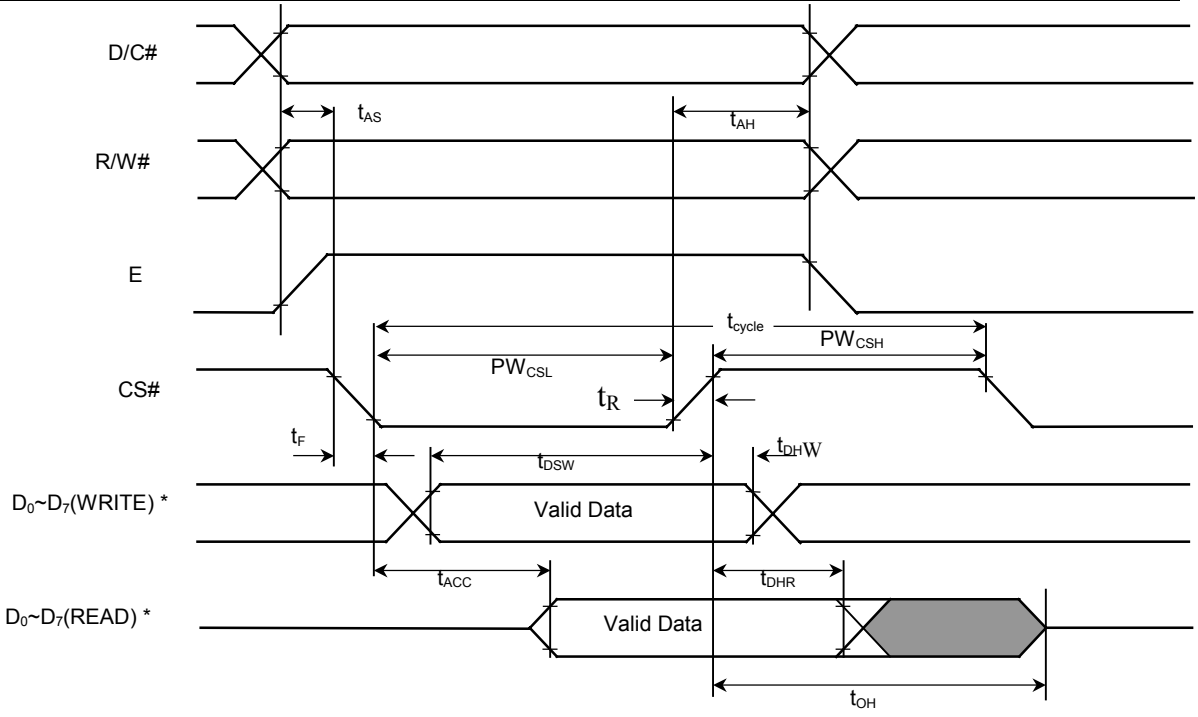
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	Vdd = 2.7V	-	2.0	-	MHz
F_{FRM}	Frame Frequency for 132 MUX Mode	132RGB x 132 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} X 1/(D*K*132)	-	Hz

D: divide ratio (POR =1)
K: number of display clocks (POR=136, i.e. phase1 dclk+phase2 dclk+ phase3 dclk=4+7+125)
Refer to command table for detail description

Table 8 - 6800-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



* when 16 bit used: D_0 ~ D_{15} instead

Figure 26 - 6800-series MPU parallel interface characteristics

Table 9 - 8080-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

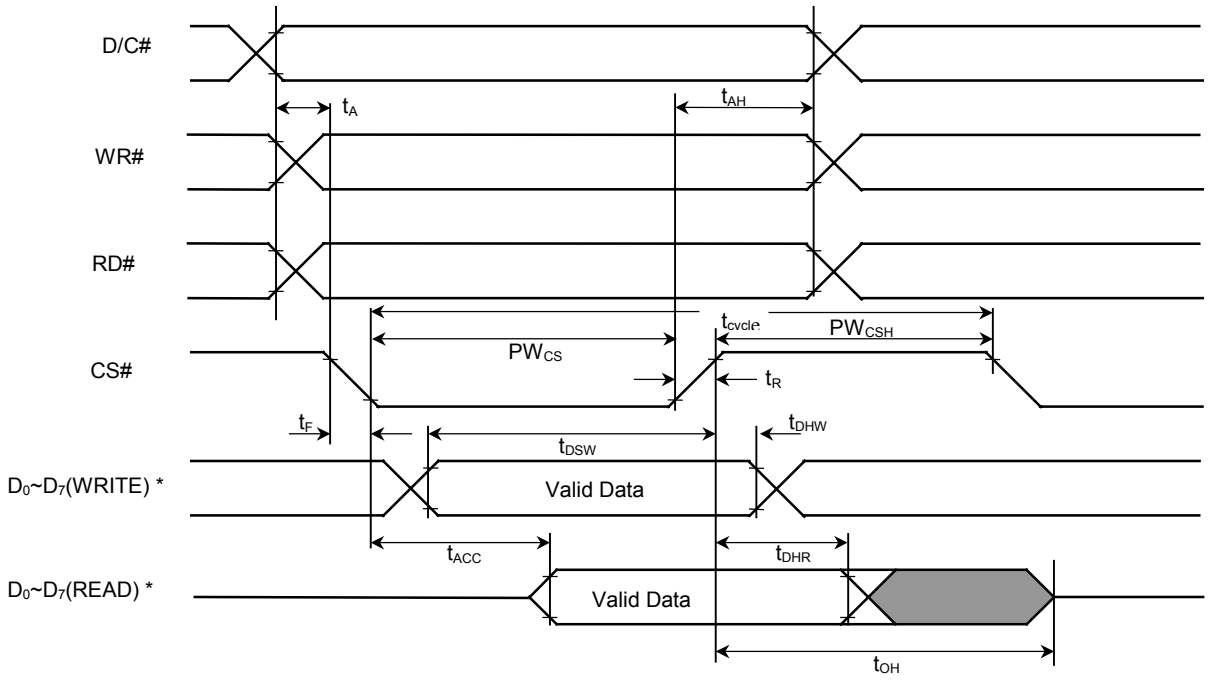


Figure 27 - 8080-series MPU parallel interface characteristics

* when 16 bit used: D_0 ~ D_{15} instead

Table 10 - Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

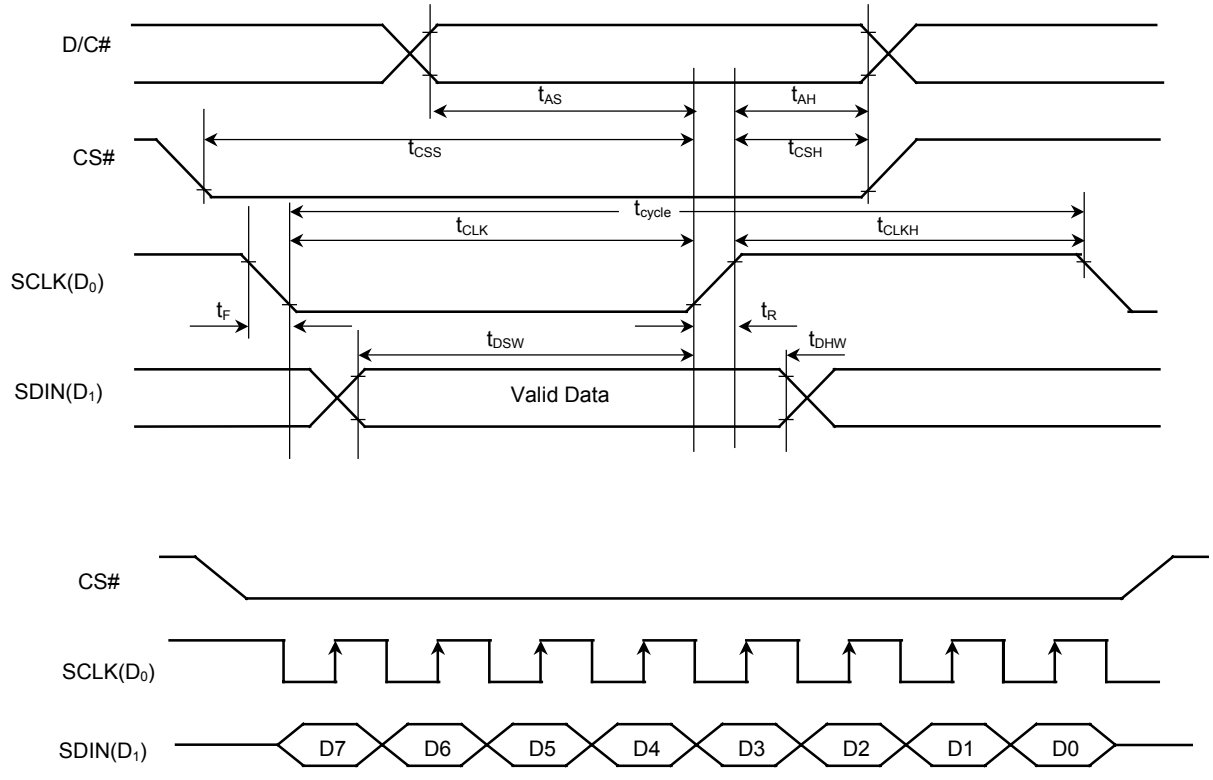
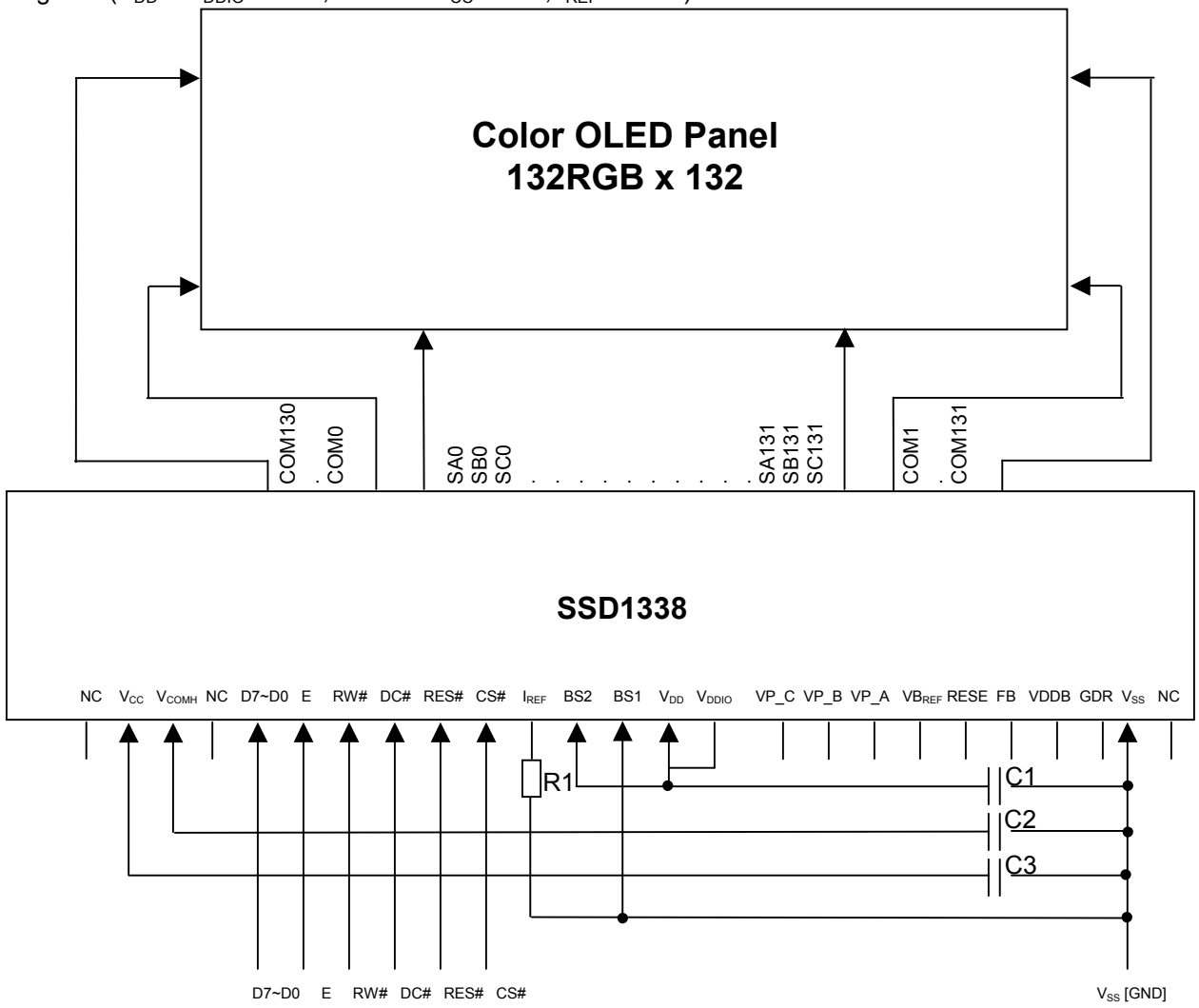


Figure 28 - Serial interface characteristics

12. APPLICATION EXAMPLE

The configuration for 8-bit 6800-parallel interface mode, externally V_{CC} is shown in the following diagram: (V_{DD} = V_{DDIO} = 3.0V, external V_{CC} = 12V, I_{REF} = 10uA)



Pin connected to MCU interface: D0~D7, E, R/W#, D/C#, RES#, CS#
Pin internally connected to VDD: M/S#, CLS
Pin internally connected to VSS: VSSB, BGGND
Pin internally connected to VCC: VREF
Pin externally connected to VDD: BS0,1
Pin externally connected to VSS: BS2
Pin floated: VP_C, VP_B, VP_A, VB_{REF}, RESE, FB, VDDB, GDR

C1~C3: 4.7uF
Voltage at I_{REF} = VCC – 3V
R1 = (Voltage at I_{REF} - VSS) / I_{REF} = 910KΩ

Figure 29 - Application Example for 8-bit 6800-parallel interface mode

13. SSD1338 COF PACKAGE

SSD1338UR1 pin assignment

Figure 30 - SSD1338UR1 pin assignment

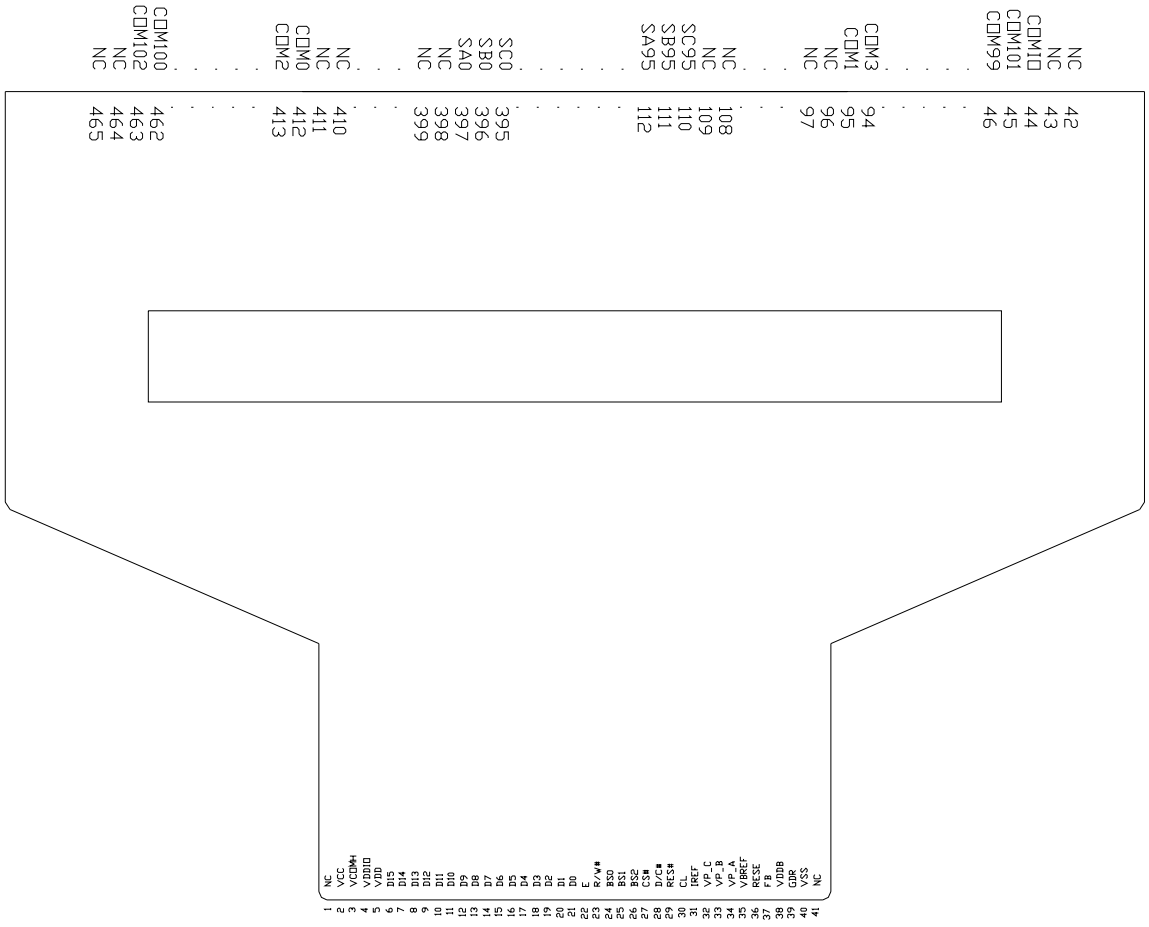


Table 11 - SSD1338UR1 Pin Assignment

Pad #	Pad Name
1	NC
2	VCC
3	VCOMH
4	VDDIO
5	VDD
6	D15
7	D14
8	D13
9	D12
10	D11
11	D10
12	D9
13	D8
14	D7
15	D6
16	D5
17	D4
18	D3
19	D2
20	D1
21	D0
22	E
23	R/W#
24	BS0
25	BS1
26	BS2
27	CS#
28	DC
29	RES#
30	CL
31	IREF
32	VP_C
33	VP_B
34	VP_A
35	VBREF
36	RESE
37	FB
38	VDDB
39	GDR
40	VSS
41	NC
42	NC
43	NC
44	COMIO
45	COM101
46	COM99
47	COM97
48	COM95
49	COM93
50	COM91
51	COM89
52	COM87
53	COM85
54	COM83
55	COM81
56	COM79
57	COM77
58	COM75
59	COM73
60	COM71
61	COM69
62	COM67
63	COM65
64	COM63
65	COM61
66	COM59
67	COM57
68	COM55
69	COM53
70	COM51
71	COM49
72	COM47
73	COM45
74	COM43
75	COM41
76	COM39
77	COM37
78	COM35
79	COM33
80	COM31

Pad #	Pad Name
81	COM29
82	COM27
83	COM25
84	COM23
85	COM21
86	COM19
87	COM17
88	COM15
89	COM13
90	COM11
91	COM9
92	COM7
93	COM5
94	COM3
95	COM1
96	NC1
97	NC2
98	NC3
99	NC4
100	NC5
101	NC6
102	NC7
103	NC8
104	NC9
105	NC10
106	NC11
107	NC12
108	NC13
109	NC14
110	SC95
111	SB95
112	SA95
113	SC94
114	SB94
115	SA94
116	SC93
117	SB93
118	SA93
119	SC92
120	SB92
121	SA92
122	SC91
123	SB91
124	SA91
125	SC90
126	SB90
127	SA90
128	SC89
129	SB89
130	SA89
131	SC88
132	SB88
133	SA88
134	SC87
135	SB87
136	SA87
137	SC86
138	SB86
139	SA86
140	SC85
141	SB85
142	SA85
143	SC84
144	SB84
145	SA84
146	SC83
147	SB83
148	SA83
149	SC82
150	SB82
151	SA82
152	SC81
153	SB81
154	SA81
155	SC80
156	SB80
157	SA80
158	SC79
159	SB79
160	SA79

Pad #	Pad Name
161	SC78
162	SB78
163	SA78
164	SC77
165	SB77
166	SA77
167	SC76
168	SB76
169	SA76
170	SC75
171	SB75
172	SA75
173	SC74
174	SB74
175	SA74
176	SC73
177	SB73
178	SA73
179	SC72
180	SB72
181	SA72
182	SC71
183	SB71
184	SA71
185	SC70
186	SB70
187	SA70
188	SC69
189	SB69
190	SA69
191	SC68
192	SB68
193	SA68
194	SC67
195	SB67
196	SA67
197	SC66
198	SB66
199	SA66
200	SC65
201	SB65
202	SA65
203	SC64
204	SB64
205	SA64
206	SC63
207	SB63
208	SA63
209	SC62
210	SB62
211	SA62
212	SC61
213	SB61
214	SA61
215	SC60
216	SB60
217	SA60
218	SC59
219	SB59
220	SA59
221	SC58
222	SB58
223	SA58
224	SC57
225	SB57
226	SA57
227	SC56
228	SB56
229	SA56
230	SC55
231	SB55
232	SA55
233	SC54
234	SB54
235	SA54
236	SC53
237	SB53
238	SA53
239	SC52
240	SB52

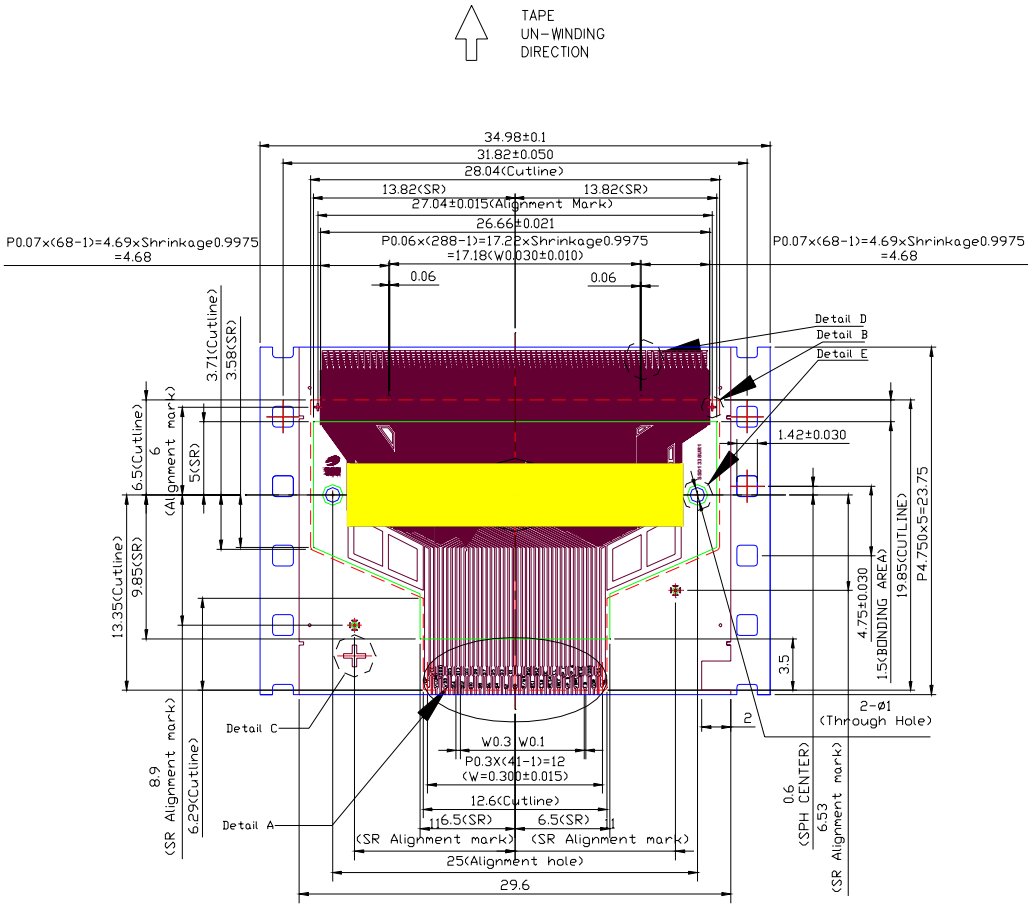
Pad #	Pad Name
241	SA52
242	SC51
243	SB51
244	SA51
245	SC50
246	SB50
247	SA50
248	SC49
249	SB49
250	SA49
251	SC48
252	SB48
253	SA48
254	SC47
255	SB47
256	SA47
257	SC46
258	SB46
259	SA46
260	SC45
261	SB45
262	SA45
263	SC44
264	SB44
265	SA44
266	SC43
267	SB43
268	SA43
269	SC42
270	SB42
271	SA42
272	SC41
273	SB41
274	SA41
275	SC40
276	SB40
277	SA40
278	SC39
279	SB39
280	SA39
281	SC38
282	SB38
283	SA38
284	SC37
285	SB37
286	SA37
287	SC36
288	SB36
289	SA36
290	SC35
291	SB35
292	SA35
293	SC34
294	SB34
295	SA34
296	SC33
297	SB33
298	SA33
299	SC32
300	SB32
301	SA32
302	SC31
303	SB31
304	SA31
305	SC30
306	SB30
307	SA30
308	SC29
309	SB29
310	SA29
311	SC28
312	SB28
313	SA28
314	SC27
315	SB27
316	SA27
317	SC26
318	SB26
319	SA26
320	SC25

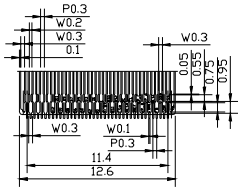
Pad #	Pad Name
321	SB25
322	SA25
323	SC24
324	SB24
325	SA24
326	SC23
327	SB23
328	SA23
329	SC22
330	SB22
331	SA22
332	SC21
333	SB21
334	SA21
335	SC20
336	SB20
337	SA20
338	SC19
339	SB19
340	SA19
341	SC18
342	SB18
343	SA18
344	SC17
345	SB17
346	SA17
347	SC16
348	SB16
349	SA16
350	SC15
351	SB15
352	SA15
353	SC14
354	SB14
355	SA14
356	SC13
357	SB13
358	SA13
359	SC12
360	SB12
361	SA12
362	SC11
363	SB11
364	SA11
365	SC10
366	SB10
367	SA10
368	SC9
369	SB9
370	SA9
371	SC8
372	SB8
373	SA8
374	SC7
375	SB7
376	SA7
377	SC6
378	SB6
379	SA6
380	SC5
381	SB5
382	SA5
383	SC4
384	SB4
385	SA4
386	SC3
387	SB3
388	SA3
389	SC2
390	SB2
391	SA2
392	SC1
393	SB1
394	SA1
395	SC0
396	SB0
397	SA0
398	NC14
399	NC13
400	NC12

Pad #	Pad Name
401	NC11
402	NC10
403	NC9
404	NC8
405	NC7
406	NC6
407	NC5
408	NC4
409	NC3
410	NC2
411	NC1
412	COM0
413	COM2
414	COM4
415	COM6
416	COM8
417	COM10
418	COM12
419	COM14
420	COM16
421	COM18
422	COM20
423	COM22
424	COM24
425	COM26
426	COM28
427	COM30
428	COM32
429	COM34
430	COM36
431	COM38
432	COM40
433	COM42
434	COM44
435	COM46
436	COM48
437	COM50
438	COM52
439	COM54
440	COM56
441	COM58
442	COM60
443	COM62
444	COM64
445	COM66
446	COM68
447	COM70
448	COM72
449	COM74
450	COM76
451	COM78
452	COM80
453	COM82
454	COM84
455	COM86
456	COM88
457	COM90
458	COM92
459	COM94
460	COM96
461	COM98
462	COM100
463	COM102
464	NC
465	NC

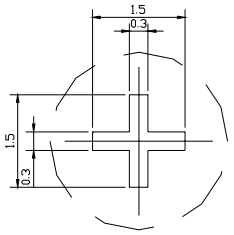
SSD1338UR1 COF details dimensions

Figure 31 - SSD1338UR1 detail dimensions

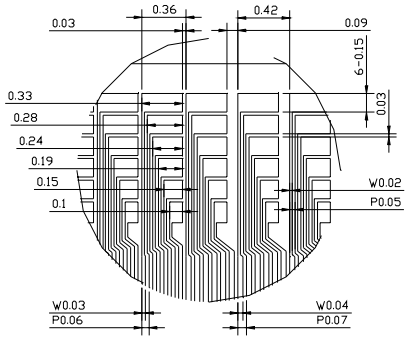




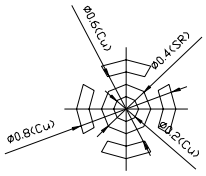
Scale: 1:1
Detail A



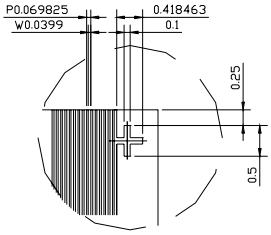
Scale: 5:1
Detail C*



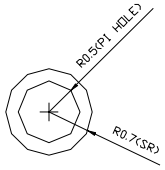
Scale: 10:1
Detail D



Scale: 10:1
SR Alignment mark



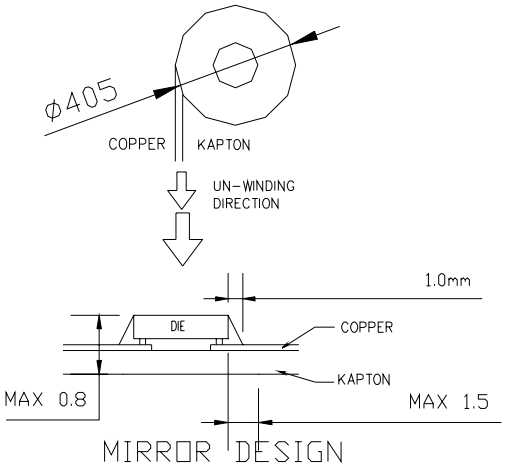
Scale: 5:1
Detail B



Scale: 5:1
Detail E

* Optional feature for Solomon Systech internal use only which may be replaced by punching hole

NOTE:
1. GENERAL TOLERANCE: ±0.05mm
2. CUTLINE TOLERANCE: ±0.15mm
3. MATERIAL
   PI: 38±4um
   CU: 8±2um
   SR: 15±10um
   OTHER TOLERANCE: ±0.200
4. SN PLATING: 0.20±0.05um
5. TAPSITE: 5 SPH, 23.75mm
6. SOLOMON SYSTECH INTERNAL USE ONLY WHICH MAY BE REPLACED BY PUNCHING HOLE



MIRROR DESIGN

SSD1338U1R1 pin assignment

Figure 32 - SSD1338U1R1 pin assignment

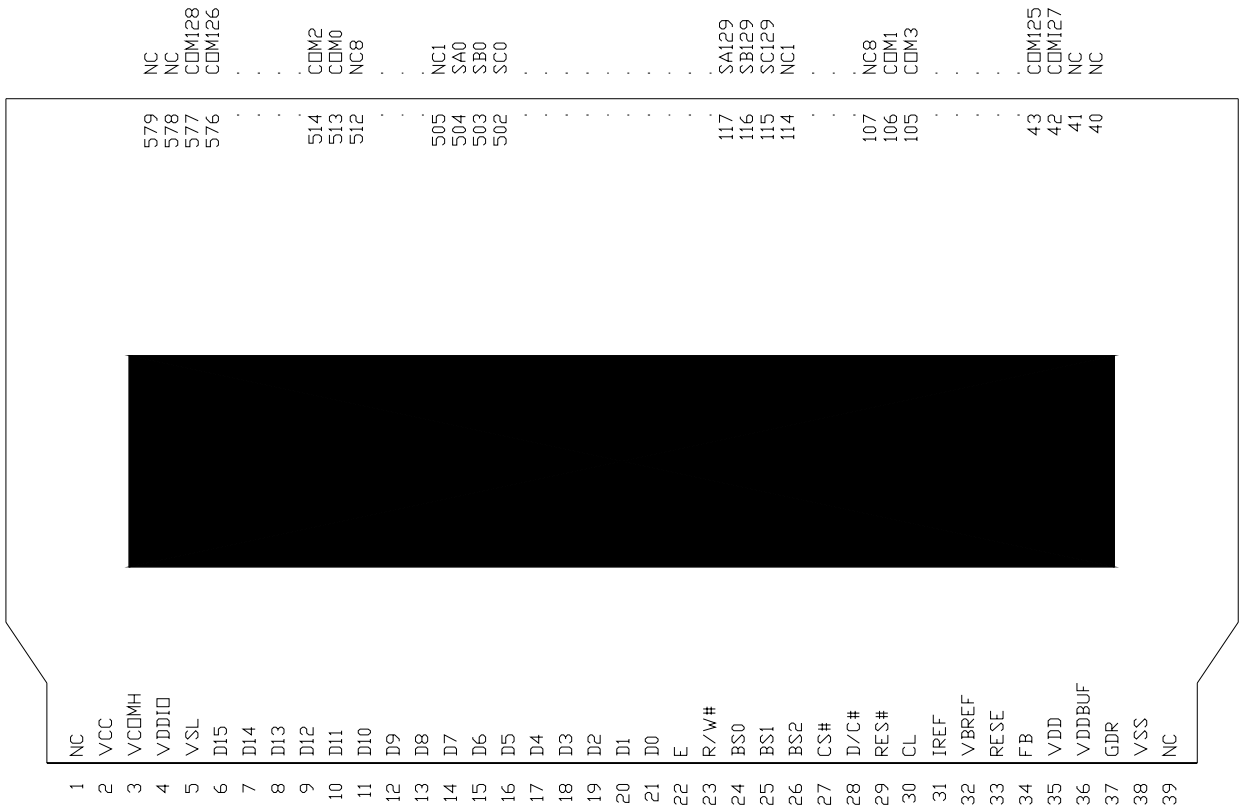


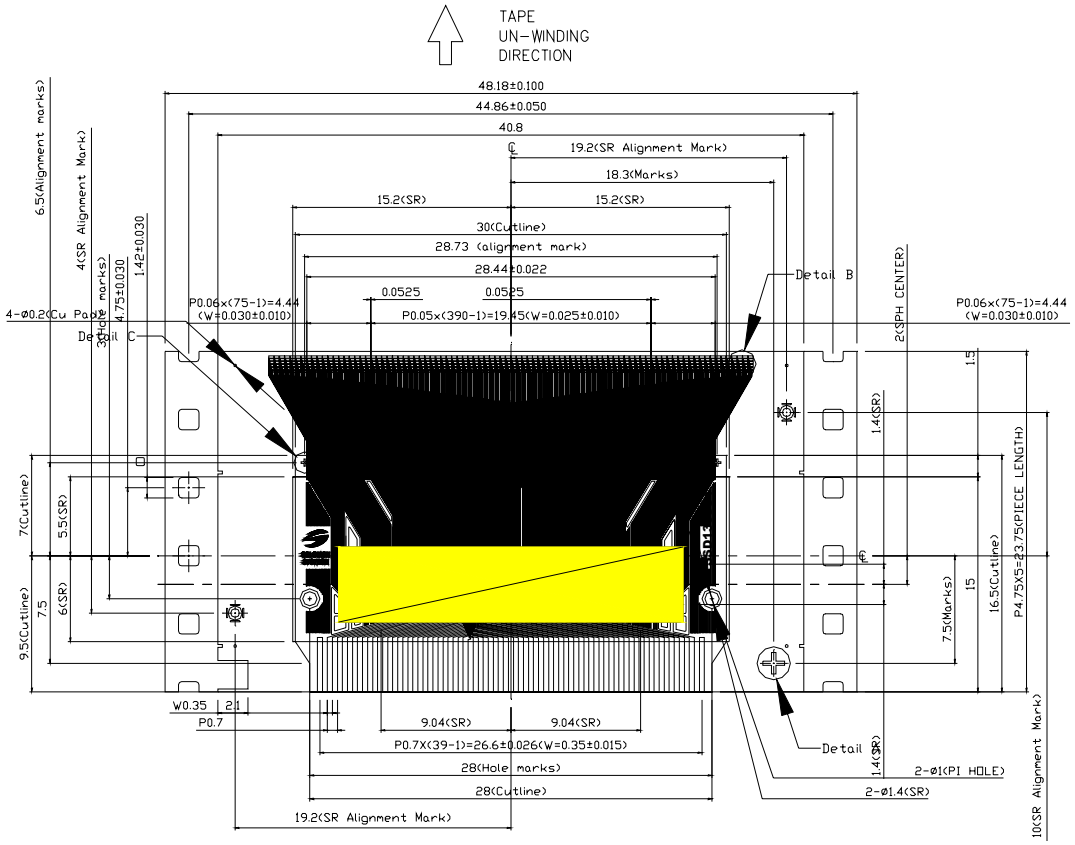
Table 12 - SSD1338U1R1 Pin Assignment

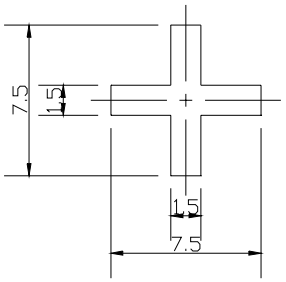
Pad.no	Pad.name	Pad.no	Pad.name	Pad.no	Pad.name	Pad.no	Pad.name	Pad.no	Pad.name	Pad.no	Pad.name	Pad.no	Pad.name
1	NC	40	NC	79	COM55	118	SC128	157	SC115	196	SC102	235	SC89
2	VCC	41	NC	80	COM53	119	SB128	158	SB115	197	SB102	236	SB89
3	VCOMH	42	COM129	81	COM51	120	SA128	159	SA115	198	SA102	237	SA89
4	VDDIO	43	COM127	82	COM49	121	SC127	160	SC114	199	SC101	238	SC88
5	VSL	44	COM125	83	COM47	122	SB127	161	SB114	200	SB101	239	SB88
6	D15	45	COM123	84	COM45	123	SA127	162	SA114	201	SA101	240	SA88
7	D14	46	COM121	85	COM43	124	SC126	163	SC113	202	SC100	241	SC87
8	D13	47	COM119	86	COM41	125	SB126	164	SB113	203	SB100	242	SB87
9	D12	48	COM117	87	COM39	126	SA126	165	SA113	204	SA100	243	SA87
10	D11	49	COM115	88	COM37	127	SC125	166	SC112	205	SC99	244	SC86
11	D10	50	COM113	89	COM35	128	SB125	167	SB112	206	SB99	245	SB86
12	D9	51	COM111	90	COM33	129	SA125	168	SA112	207	SA99	246	SA86
13	D8	52	COM109	91	COM31	130	SC124	169	SC111	208	SC98	247	SC85
14	D7	53	COM107	92	COM29	131	SB124	170	SB111	209	SB98	248	SB85
15	D6	54	COM105	93	COM27	132	SA124	171	SA111	210	SA98	249	SA85
16	D5	55	COM103	94	COM25	133	SC123	172	SC110	211	SC97	250	SC84
17	D4	56	COM101	95	COM23	134	SB123	173	SB110	212	SB97	251	SB84
18	D3	57	COM99	96	COM21	135	SA123	174	SA110	213	SA97	252	SA84
19	D2	58	COM97	97	COM19	136	SC122	175	SC109	214	SC96	253	SC83
20	D1	59	COM95	98	COM17	137	SB122	176	SB109	215	SB96	254	SB83
21	D0	60	COM93	99	COM15	138	SA122	177	SA109	216	SA96	255	SA83
22	E(RD#)	61	COM91	100	COM13	139	SC121	178	SC108	217	SC95	256	SC82
23	R/W#(WR#)	62	COM89	101	COM11	140	SB121	179	SB108	218	SB95	257	SB82
24	BS0	63	COM87	102	COM9	141	SA121	180	SA108	219	SA95	258	SA82
25	BS1	64	COM85	103	COM7	142	SC120	181	SC107	220	SC94	259	SC81
26	BS2	65	COM83	104	COM5	143	SB120	182	SB107	221	SB94	260	SB81
27	CS#	66	COM81	105	COM3	144	SA120	183	SA107	222	SA94	261	SA81
28	D/C#	67	COM79	106	COM1	145	SC119	184	SC106	223	SC93	262	SC80
29	RES#	68	COM77	107	NC8	146	SB119	185	SB106	224	SB93	263	SB80
30	CL	69	COM75	108	NC7	147	SA119	186	SA106	225	SA93	264	SA80
31	IREF	70	COM73	109	NC6	148	SC118	187	SC105	226	SC92	265	SC79
32	VBREF	71	COM71	110	NC5	149	SB118	188	SB105	227	SB92	266	SB79
33	RESE	72	COM69	111	NC4	150	SA118	189	SA105	228	SA92	267	SA79
34	FB	73	COM67	112	NC3	151	SC117	190	SC104	229	SC91	268	SC78
35	VDD	74	COM65	113	NC2	152	SB117	191	SB104	230	SB91	269	SB78
36	VDDB	75	COM63	114	NC1	153	SA117	192	SA104	231	SA91	270	SA78
37	GDR	76	COM61	115	SC129	154	SC116	193	SC103	232	SC90	271	SC77
38	VSS	77	COM59	116	SB129	155	SB116	194	SB103	233	SB90	272	SB77
39	NC	78	COM57	117	SA129	156	SA116	195	SA103	234	SA90	273	SA77

Pad.no	Pad.name	Pad.no	Pad.name	Pad.no	Pad.name	Pad.no	Pad.name	Pad.no	Pad.name	Pad.no	Pad.name	Pad.no	Pad.name	Pad.no	Pad.name
274	SC76	313	SC63	352	SC50	391	SC37	430	SC24	469	SC11	508	NC4	547	COM68
275	SB76	314	SB63	353	SB50	392	SB37	431	SB24	470	SB11	509	NC5	548	COM70
276	SA76	315	SA63	354	SA50	393	SA37	432	SA24	471	SA11	510	NC6	549	COM72
277	SC75	316	SC62	355	SC49	394	SC36	433	SC23	472	SC10	511	NC7	550	COM74
278	SB75	317	SB62	356	SB49	395	SB36	434	SB23	473	SB10	512	NC8	551	COM76
279	SA75	318	SA62	357	SA49	396	SA36	435	SA23	474	SA10	513	COM0	552	COM78
280	SC74	319	SC61	358	SC48	397	SC35	436	SC22	475	SC9	514	COM2	553	COM80
281	SB74	320	SB61	359	SB48	398	SB35	437	SB22	476	SB9	515	COM4	554	COM82
282	SA74	321	SA61	360	SA48	399	SA35	438	SA22	477	SA9	516	COM6	555	COM84
283	SC73	322	SC60	361	SC47	400	SC34	439	SC21	478	SC8	517	COM8	556	COM86
284	SB73	323	SB60	362	SB47	401	SB34	440	SB21	479	SB8	518	COM10	557	COM88
285	SA73	324	SA60	363	SA47	402	SA34	441	SA21	480	SA8	519	COM12	558	COM90
286	SC72	325	SC59	364	SC46	403	SC33	442	SC20	481	SC7	520	COM14	559	COM92
287	SB72	326	SB59	365	SB46	404	SB33	443	SB20	482	SB7	521	COM16	560	COM94
288	SA72	327	SA59	366	SA46	405	SA33	444	SA20	483	SA7	522	COM18	561	COM96
289	SC71	328	SC58	367	SC45	406	SC32	445	SC19	484	SC6	523	COM20	562	COM98
290	SB71	329	SB58	368	SB45	407	SB32	446	SB19	485	SB6	524	COM22	563	COM100
291	SA71	330	SA58	369	SA45	408	SA32	447	SA19	486	SA6	525	COM24	564	COM102
292	SC70	331	SC57	370	SC44	409	SC31	448	SC18	487	SC5	526	COM26	565	COM104
293	SB70	332	SB57	371	SB44	410	SB31	449	SB18	488	SB5	527	COM28	566	COM106
294	SA70	333	SA57	372	SA44	411	SA31	450	SA18	489	SA5	528	COM30	567	COM108
295	SC69	334	SC56	373	SC43	412	SC30	451	SC17	490	SC4	529	COM32	568	COM110
296	SB69	335	SB56	374	SB43	413	SB30	452	SB17	491	SB4	530	COM34	569	COM112
297	SA69	336	SA56	375	SA43	414	SA30	453	SA17	492	SA4	531	COM36	570	COM114
298	SC68	337	SC55	376	SC42	415	SC29	454	SC16	493	SC3	532	COM38	571	COM116
299	SB68	338	SB55	377	SB42	416	SB29	455	SB16	494	SB3	533	COM40	572	COM118
300	SA68	339	SA55	378	SA42	417	SA29	456	SA16	495	SA3	534	COM42	573	COM120
301	SC67	340	SC54	379	SC41	418	SC28	457	SC15	496	SC2	535	COM44	574	COM122
302	SB67	341	SB54	380	SB41	419	SB28	458	SB15	497	SB2	536	COM46	575	COM124
303	SA67	342	SA54	381	SA41	420	SA28	459	SA15	498	SA2	537	COM48	576	COM126
304	SC66	343	SC53	382	SC40	421	SC27	460	SC14	499	SC1	538	COM50	577	COM128
305	SB66	344	SB53	383	SB40	422	SB27	461	SB14	500	SB1	539	COM52	578	NC
306	SA66	345	SA53	384	SA40	423	SA27	462	SA14	501	SA1	540	COM54	579	NC
307	SC65	346	SC52	385	SC39	424	SC26	463	SC13	502	SC0	541	COM56		
308	SB65	347	SB52	386	SB39	425	SB26	464	SB13	503	SB0	542	COM58		
309	SA65	348	SA52	387	SA39	426	SA26	465	SA13	504	SA0	543	COM60		
310	SC64	349	SC51	388	SC38	427	SC25	466	SC12	505	NC1	544	COM62		
311	SB64	350	SB51	389	SB38	428	SB25	467	SB12	506	NC2	545	COM64		
312	SA64	351	SA51	390	SA38	429	SA25	468	SA12	507	NC3	546	COM66		

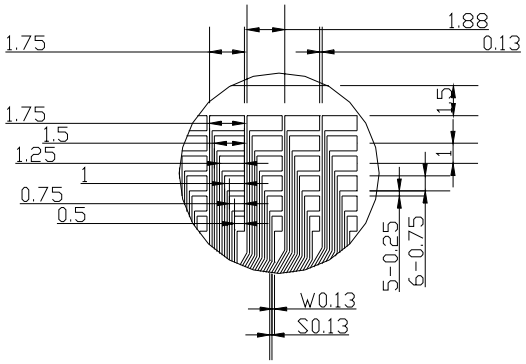
SSD1338U1R1 COF details dimensions

Figure 33 - SSD1338U1R1 detail dimensions

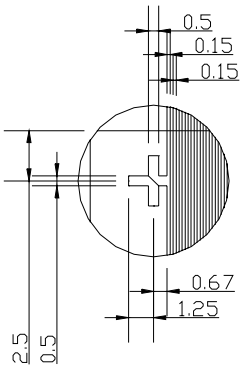




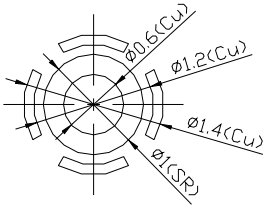
Scale 5:1
Detail A



Scale 5:1
Detail B

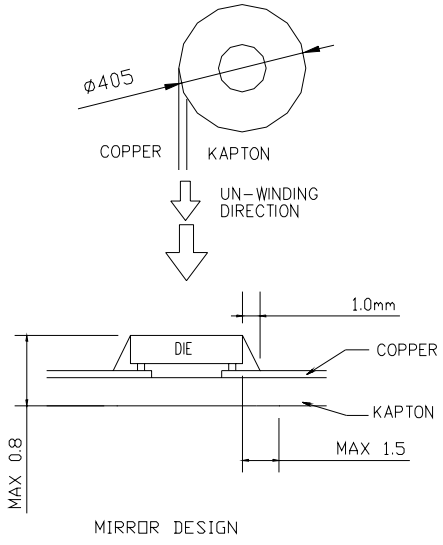


Scale: 5:1
Detail C*



* Optional feature for Solomon Systech internal use only which may be replaced by punching hole

NOTE:
1. GENERAL TOLERANCE: ±0.05MM
2. CUTLINE TOLERANCE: ±0.15MM
3. MATERIAL
   PI: 38±4UM
   CU: 8±2UM
   SR: 15±10UM
   OTHER TOLERANCE: ±0.200
4. SN PLATING: 0.20±0.05UM
5. TAPSITE: 5 SPH, 23.75MM
6. OPTIONAL FEATURE FOR SOLOMON SYSTECH INTERNAL USE ONLY WHICH MAYBE REPLACED BY PUNCHING HOLE



MIRROR DESIGN

SSD1338U2 Pin Assignment

Figure 34 - SSD1338U2 pin assignment

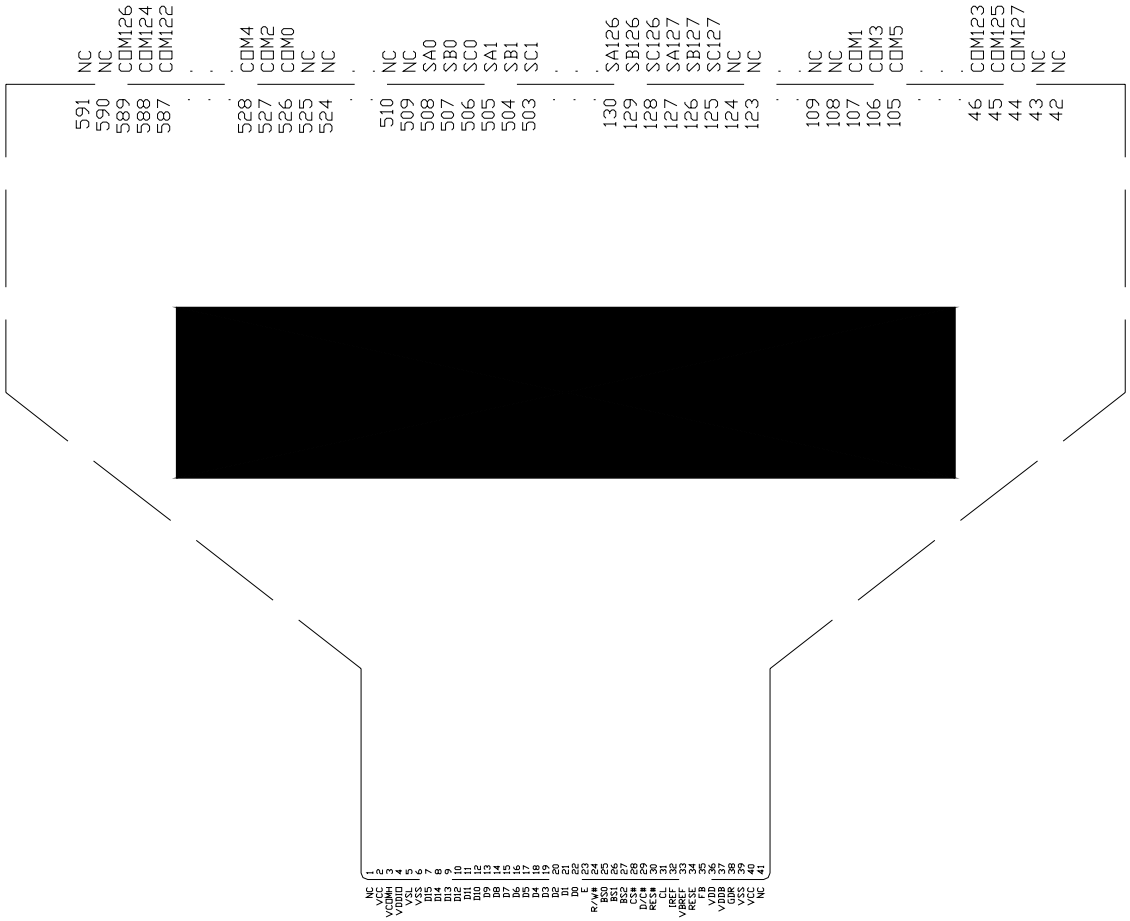


Table 13 - SSD1338U2 pin assignment

Pad #	Pad Name
1	NC
2	NC
3	VCC
4	VCOMH
5	VDDIO
6	VSL
7	D15
8	D14
9	D13
10	D12
11	D11
12	D10
13	D9
14	D8
15	D7
16	D6
17	D5
18	D4
19	D3
20	D2
21	D1
22	D0
23	E
24	R/W#
25	BS0
26	BS1
27	BS2
28	CS#
29	D/C#
30	RES#
31	CL
32	IREF
33	VBREF
34	RESE
35	FB
36	VDDIO
37	VDDB
38	GDR
39	VSS
40	NC
41	NC
42	NC
43	NC
44	COM127
45	COM125
46	COM123
47	COM121
48	COM119
49	COM117
50	COM115
51	COM113
52	COM111
53	COM109
54	COM107
55	COM105
56	COM103
57	COM101
58	COM99
59	COM97
60	COM95
61	COM93
62	COM91
63	COM89
64	COM87
65	COM85
66	COM83
67	COM81
68	COM79
69	COM77
70	COM75
71	COM73
72	COM71
73	COM69
74	COM67
75	COM65
76	COM63
77	COM61
78	COM59
79	COM57
80	COM55

Pad #	Pad Name
81	COM53
82	COM51
83	COM49
84	COM47
85	COM45
86	COM43
87	COM41
88	COM39
89	COM37
90	COM35
91	COM33
92	COM31
93	COM29
94	COM27
95	COM25
96	COM23
97	COM21
98	COM19
99	COM17
100	COM15
101	COM13
102	COM11
103	COM9
104	COM7
105	COM5
106	COM3
107	COM1
108	NC
109	NC
110	NC
111	NC
112	NC
113	NC
114	NC
115	NC
116	NC
117	NC
118	NC
119	NC
120	NC
121	NC
122	NC
123	NC
124	NC
125	SC127
126	SB127
127	SA127
128	SC126
129	SB126
130	SA126
131	SC125
132	SB125
133	SA125
134	SC124
135	SB124
136	SA124
137	SC123
138	SB123
139	SA123
140	SC122
141	SB122
142	SA122
143	SC121
144	SB121
145	SA121
146	SC120
147	SB120
148	SA120
149	SC119
150	SB119
151	SA119
152	SC118
153	SB118
154	SA118
155	SC117
156	SB117
157	SA117
158	SC116
159	SB116
160	SA116

Pad #	Pad Name
161	SC115
162	SB115
163	SA115
164	SC114
165	SB114
166	SA114
167	SC113
168	SB113
169	SA113
170	SC112
171	SB112
172	SA112
173	SC111
174	SB111
175	SA111
176	SC110
177	SB110
178	SA110
179	SC109
180	SB109
181	SA109
182	SC108
183	SB108
184	SA108
185	SC107
186	SB107
187	SA107
188	SC106
189	SB106
190	SA106
191	SC105
192	SB105
193	SA105
194	SC104
195	SB104
196	SA104
197	SC103
198	SB103
199	SA103
200	SC102
201	SB102
202	SA102
203	SC101
204	SB101
205	SA101
206	SC100
207	SB100
208	SA100
209	SC99
210	SB99
211	SA99
212	SC98
213	SB98
214	SA98
215	SC97
216	SB97
217	SA97
218	SC96
219	SB96
220	SA96
221	SC95
222	SB95
223	SA95
224	SC94
225	SB94
226	SA94
227	SC93
228	SB93
229	SA93
230	SC92
231	SB92
232	SA92
233	SC91
234	SB91
235	SA91
236	SC90
237	SB90
238	SA90
239	SC89
240	SB89

Pad #	Pad Name
241	SA89
242	SC88
243	SB88
244	SA88
245	SC87
246	SB87
247	SA87
248	SC86
249	SB86
250	SA86
251	SC85
252	SB85
253	SA85
254	SC84
255	SB84
256	SA84
257	SC83
258	SB83
259	SA83
260	SC82
261	SB82
262	SA82
263	SC81
264	SB81
265	SA81
266	SC80
267	SB80
268	SA80
269	SC79
270	SB79
271	SA79
272	SC78
273	SB78
274	SA78
275	SC77
276	SB77
277	SA77
278	SC76
279	SB76
280	SA76
281	SC75
282	SB75
283	SA75
284	SC74
285	SB74
286	SA74
287	SC73
288	SB73
289	SA73
290	SC72
291	SB72
292	SA72
293	SC71
294	SB71
295	SA71
296	SC70
297	SB70
298	SA70
299	SC69
300	SB69
301	SA69
302	SC68
303	SB68
304	SA68
305	SC67
306	SB67
307	SA67
308	SC66
309	SB66
310	SA66
311	SC65
312	SB65
313	SA65
314	SC64
315	SB64
316	SA64
317	SC63
318	SB63
319	SA63
320	SC62

Pad #	Pad Name
321	SB62
322	SA62
323	SC61
324	SB61
325	SA61
326	SC60
327	SB60
328	SA60
329	SC59
330	SB59
331	SA59
332	SC58
333	SB58
334	SA58
335	SC57
336	SB57
337	SA57
338	SC56
339	SB56
340	SA56
341	SC55
342	SB55
343	SA55
344	SC54
345	SB54
346	SA54
347	SC53
348	SB53
349	SA53
350	SC52
351	SB52
352	SA52
353	SC51
354	SB51
355	SA51
356	SC50
357	SB50
358	SA50
359	SC49
360	SB49
361	SA49
362	SC48
363	SB48
364	SA48
365	SC47
366	SB47
367	SA47
368	SC46
369	SB46
370	SA46
371	SC45
372	SB45
373	SA45
374	SC44
375	SB44
376	SA44
377	SC43
378	SB43
379	SA43
380	SC42
381	SB42
382	SA42
383	SC41
384	SB41
385	SA41
386	SC40
387	SB40
388	SA40
389	SC39
390	SB39
391	SA39
392	SC38
393	SB38
394	SA38
395	SC37
396	SB37
397	SA37
398	SC36
399	SB36
400	SA36

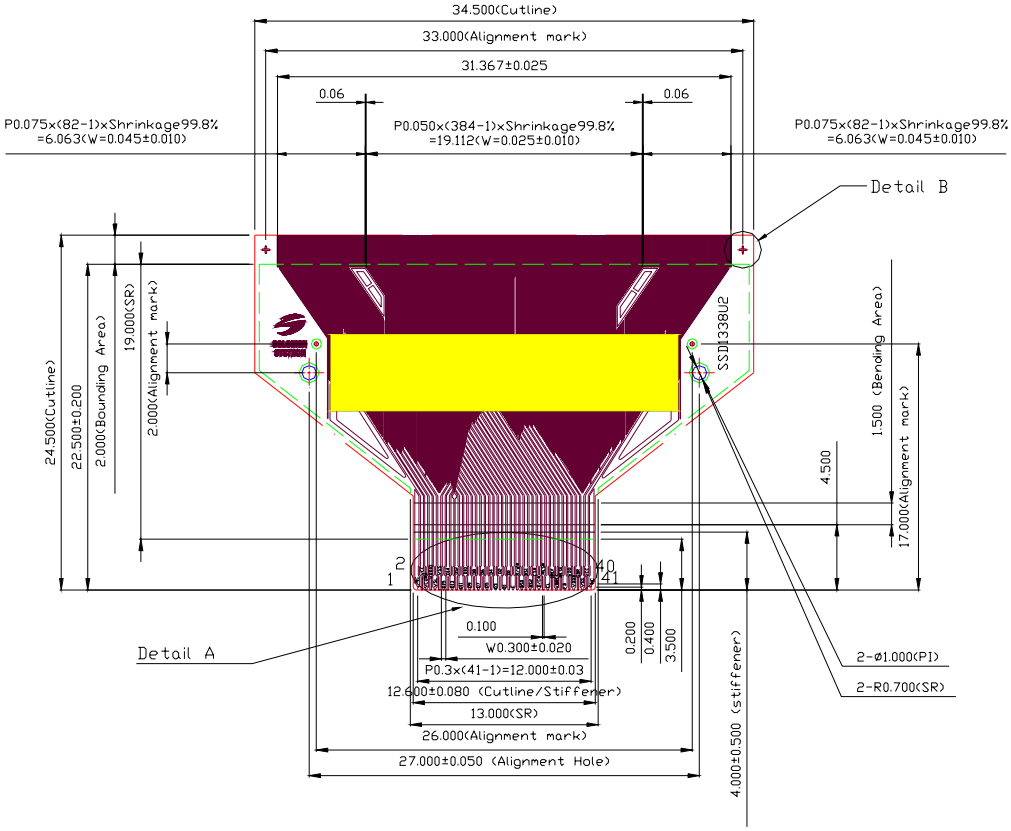
Pad #	Pad Name
401	SC35
402	SB35
403	SA35
404	SC34
405	SB34
406	SA34
407	SC33
408	SB33
409	SA33
410	SC32
411	SB32
412	SA32
413	SC31
414	SB31
415	SA31
416	SC30
417	SB30
418	SA30
419	SC29
420	SB29
421	SA29
422	SC28
423	SB28
424	SA28
425	SC27
426	SB27
427	SA27
428	SC26
429	SB26
430	SA26
431	SC25
432	SB25
433	SA25
434	SC24
435	SB24
436	SA24
437	SC23
438	SB23
439	SA23
440	SC22
441	SB22
442	SA22
443	SC21
444	SB21
445	SA21
446	SC20
447	SB20
448	SA20
449	SC19
450	SB19
451	SA19
452	SC18
453	SB18
454	SA18
455	SC17
456	SB17
457	SA17
458	SC16
459	SB16
460	SA16
461	SC15
462	SB15
463	SA15
464	SC14
465	SB14
466	SA14
467	SC13
468	SB13
469	SA13
470	SC12
471	SB12
472	SA12
473	SC11
474	SB11
475	SA11
476	SC10
477	SB10
478	SA10
479	SC9
480	SB9

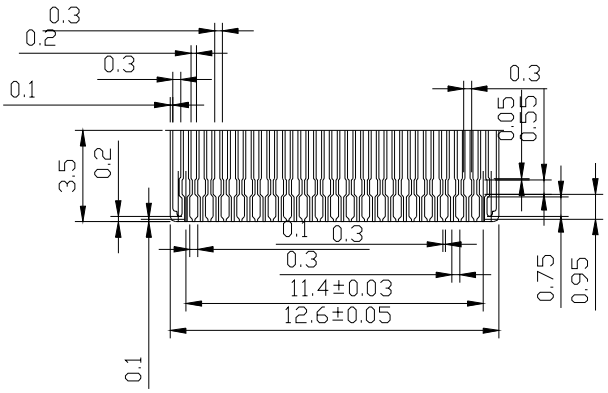
Pad #	Pad Name
481	SA9
482	SC8
483	SB8
484	SA8
485	SC7
486	SB7
487	SA7
488	SC6
489	SB6
490	SA6
491	SC5
492	SB5
493	SA5
494	SC4
495	SB4
496	SA4
497	SC3
498	SB3
499	SA3
500	SC2
501	SB2
502	SA2
503	SC1
504	SB1
505	SA1
506	SC0
507	SB0
508	SA0
509	NC
510	NC
511	NC
512	NC
513	NC
514	NC
515	NC
516	NC
517	NC
518	NC
519	NC
520	NC
521	NC
522	NC
523	NC
524	NC
525	NC
526	COM0
527	COM2
528	COM4
529	COM6
530	COM8
531	COM10
532	COM12
533	COM14
534	COM16
535	COM18
536	COM20
537	COM22
538	COM24
539	COM26
540	COM28
541	COM30
542	COM32
543	COM34
544	COM36
545	COM38
546	COM40
547	COM42
548	COM44
549	COM46
550	COM48
551	COM50
552	COM52
553	COM54
554	COM56
555	COM58
556	COM60
557	COM62
558	COM64
559	COM66
560	COM68

Pad #	Pad Name
561	COM70
562	COM72
563	COM74
564	COM76
565	COM78
566	COM80
567	COM82
568	COM84
569	COM86
570	COM88
571	COM90
572	COM92
573	COM94
574	COM96
575	COM98
576	COM100
577	COM102
578	COM104
579	COM106
580	COM108
581	COM110
582	COM112
583	COM114
584	COM116
585	COM118
586	COM120
587	COM122
588	COM124
589	COM126
590	NC
591	NC

SSD1338U2 COF details dimensions

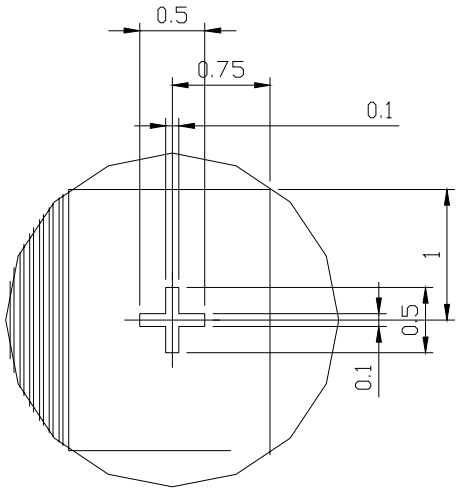
Figure 35 - SSD1338U2 detail dimensions





Scale: 5:1

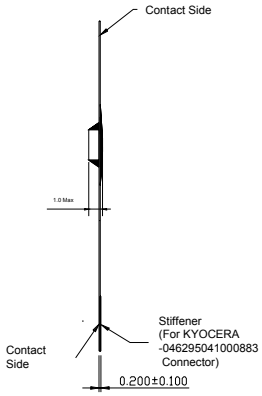
Detail A

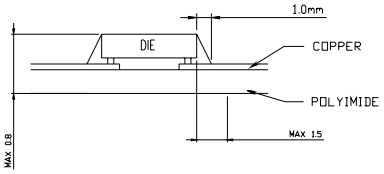


Scale: 5:1

Detail B

NOTE:
1. GENERAL TOLERANCE: ±0.20mm
2. CUTLINE TOLERANCE: ±0.15mm
3. MATERIAL
   PI: 38±4um
   CU: 8±2um
   SR: 15±10um
   OTHER TOLERANCE: ±0.200
4. SN PLATING: 0.20±0.05um
5. SOLOMON SYSTECH INTERNAL USE ONLY WHICH MAY BE REPLACED BY PUNCHING HOLE





MIRROR DESIGN

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