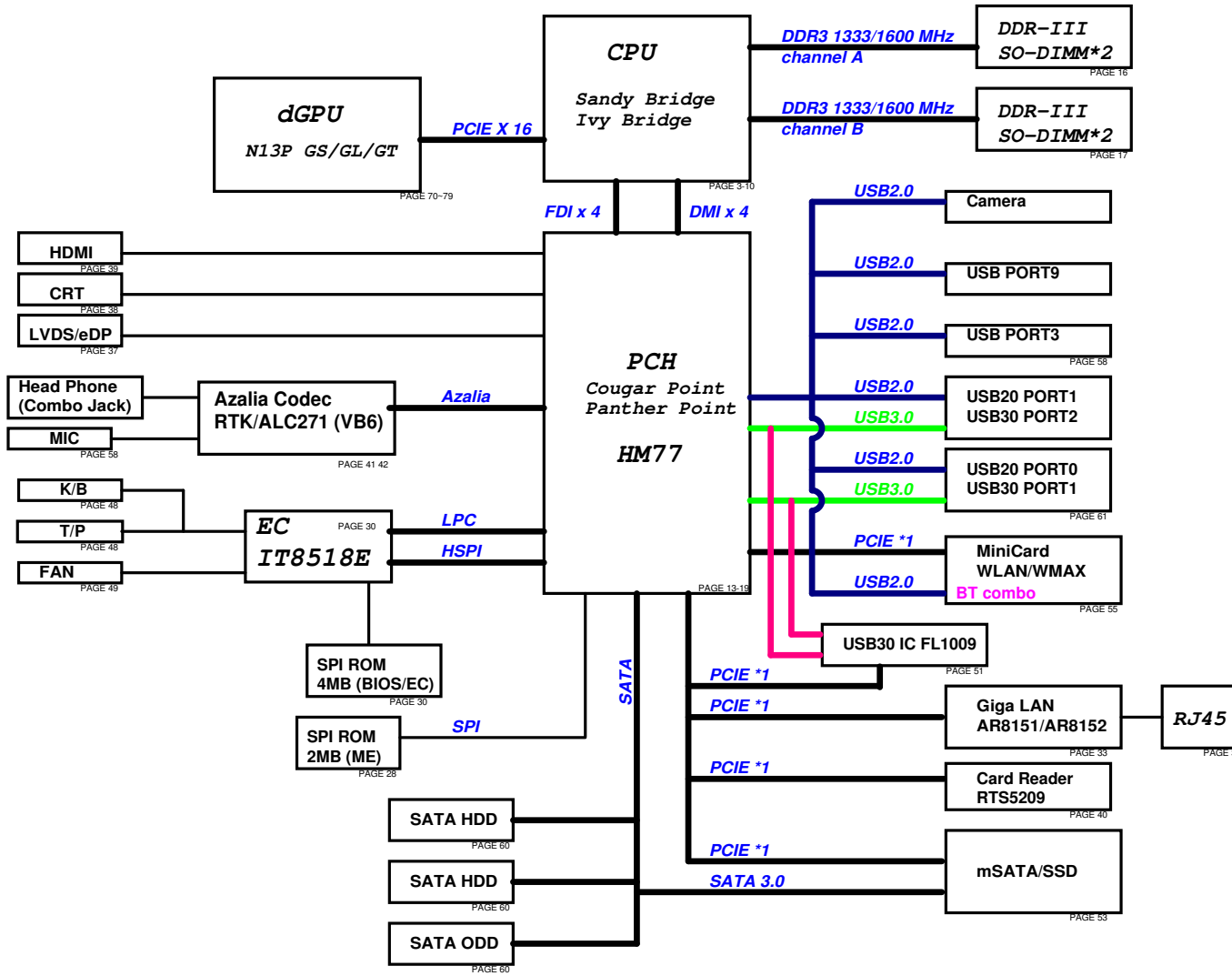


VA70 BLOCK DIAGRAM



POWER

CPU VCORE	PAGE 80
SYSTEM, +3V, +5V	PAGE 81
+VCCP & +VCCP_VT	PAGE 82
DDR & VTT	PAGE 83
2.5V & 1.5VS & 1.1VS	PAGE 84
SMART CHARGER	PAGE 88
POWER DETECT	PAGE 90
LOAD SWITCH	PAGE 91
POWER PROTECT	PAGE 92

VGA POWER

GPU VCORE	PAGE 80
+1.05VS_VGA	
+1.5VS_VGA	
+3VS_VGA	
+12VS_VGA	
LOAD SWITCH	PAGE 91
POWER PROTECT	PAGE 92

Power Rails

Sleep State	RTC	VA	VSUS	V	VS
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4	ON	ON	ON	OFF	OFF
SS/ AC	ON	ON	ON	OFF	OFF
SS/ DC	ON	ON	OFF	OFF	OFF

PCIe Port

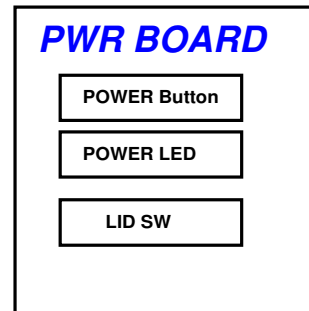
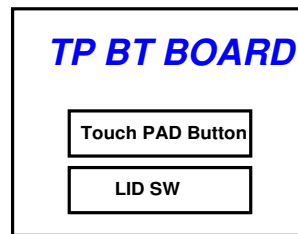
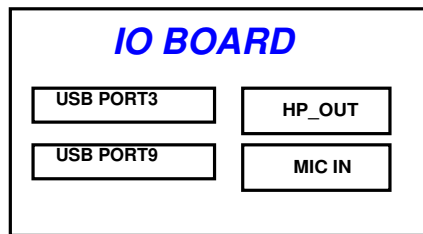
PCIe_P1	CARDREADER
PCIe_P2	Mini CARD (WLAN)
PCIe_P3	mSATA
PCIe_P4	USB30
PCIe_P5	
PCIe_P6	LAN

USB20 PORT

USB P00	External MB
USB P01	External MB
USB P02	
USB P03	External DB
USB P04	
USB P05	BT
USB P08	Camera
USB P09	External DB
USB P10	
USB P11	SSD
USB P12	
USB P13	

SATA PORT

SATA P0	HDD 1
SATA P1	HDD 2
SATA P2	ODD 3
SATA P3	mSATA
SATA P4	
SATA P5	

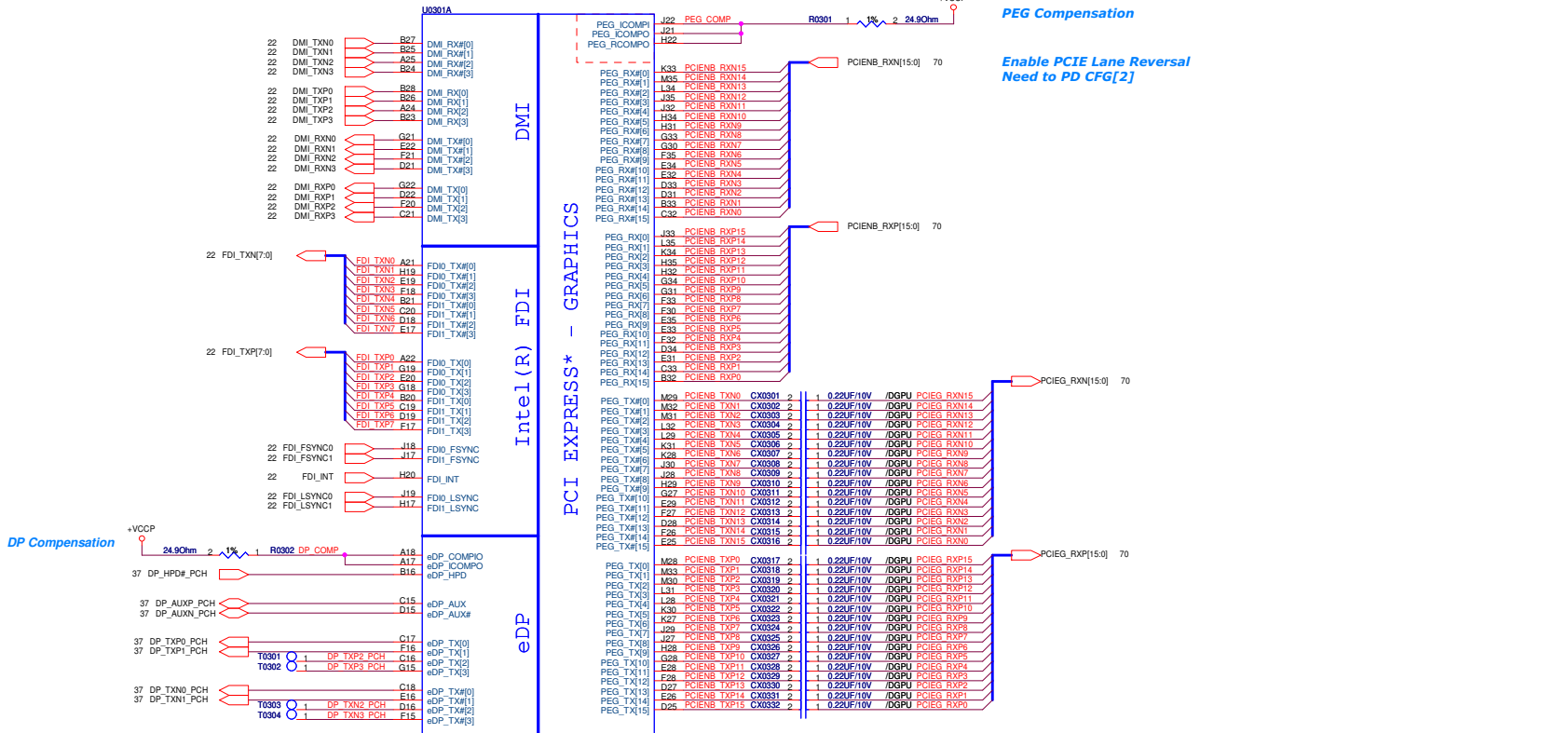


BOM optional	Remark
N/A	For 上件
/ABCT	For ABCT, 上件
/niAMT	For no iAMT, 上件
/HOME	For 上件
/HR	For Huron River, 上件
/Non_HSPI	For ROM SETTING, 上件
Entry	For 上件
Main	For 上件
/USB20	For USB 2.0, 上件
/HSPI	For 不上件
/HDMI	For HDMI用, 不上件
/TP1_AUD	For power control, 不上件
/TP1_BT	For power control, 不上件
/TP1_CAMERA	For power control, 不上件
/TP1_CR	For power control, 不上件
/TP1_LAN	For power control, 不上件
/TP1_ODD	For power control, 不上件
/TP1_WLAN	For power control, 不上件
/THERM	For Palm Rest温度, 不上件
/usb30	For USB 3.0, 不上件
/ZPODD	For ODD battery saving使用Mount R5108, 不上件
@	For 不上件
@/MP	For debug port, MP不上件
/BT270	視keypat list而定
/COMBO_BT	視keypat list而定
/SATA+	For Sata Repeater, SR先上件

PEGATRON		Title : System Setting
PEGATRON COMPUTER INC		Engineer: Wing_Cheng
Size A	Project Name BA52HR/CR	Rev 1.0
Date: Friday, February 03, 2012		Sheet 2 of 94

PEG Compensation

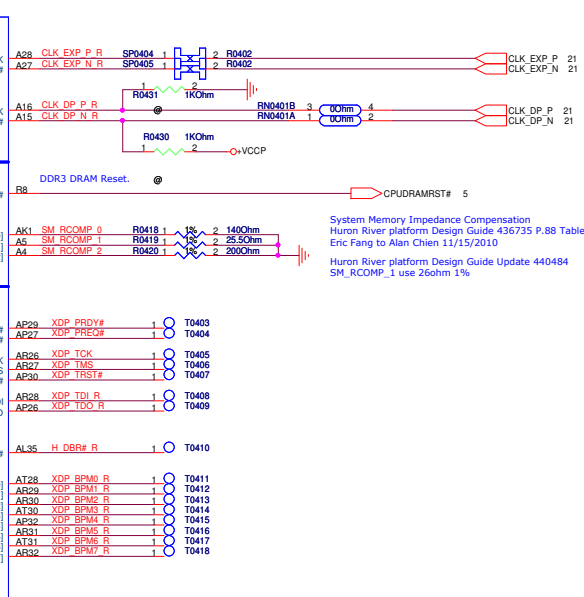
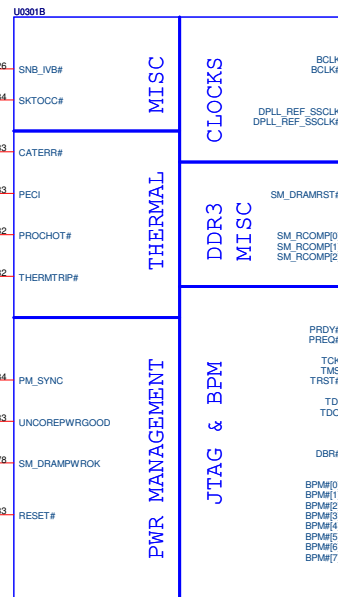
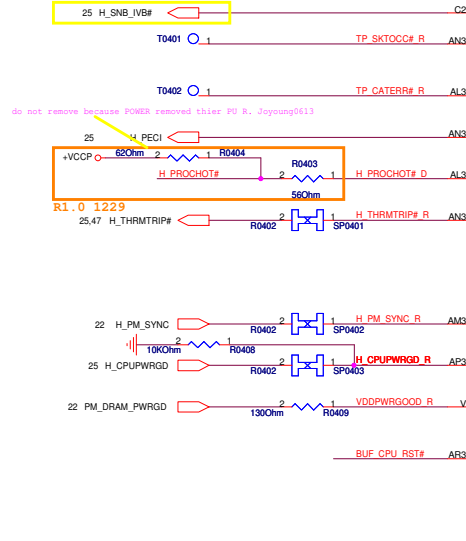
Enable PCIe Lane Reversal
Need to PD CFG[2]



If Support PCIe Gen3, change AC Cap to 0.22uF

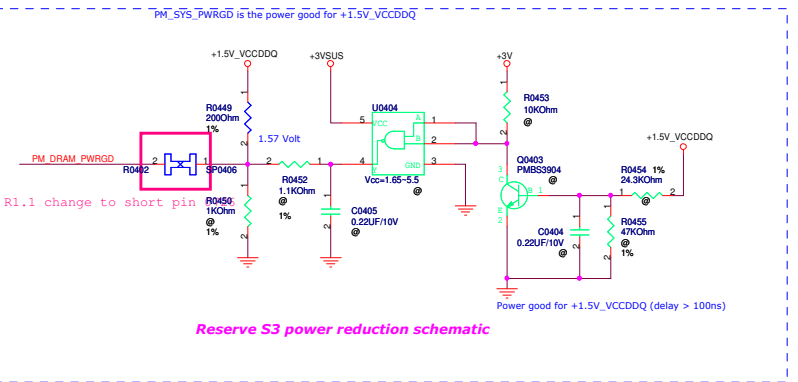
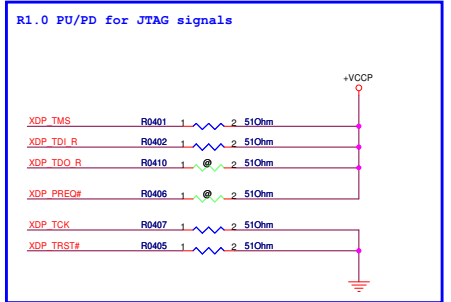
1201-006D000 - 988B for Huron River

Select the termination voltage of DMI and FDI Tx/Rx (PCH Strap)
H_SNB_IVB# connected to DF_TVS via 1Kohm
DF_TVS needs PU via 2.2Kohm to +1.8VS



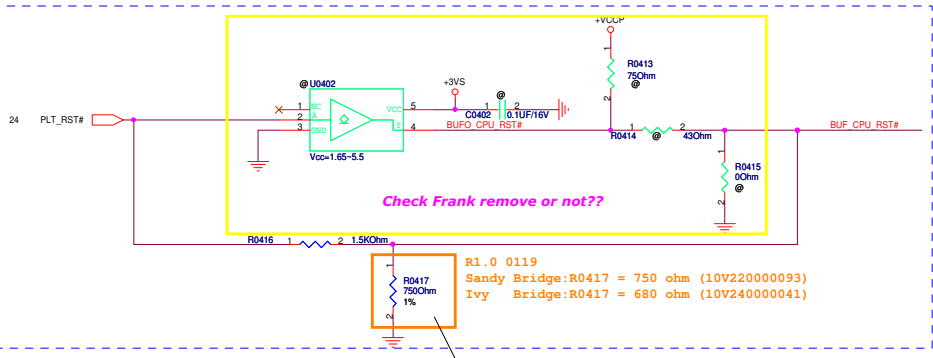
+1.5V_VCCDDQ	+1.5V_VCCDDQ	7
+3VS	+3VS	16,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92
+3VSUS	+3VSUS	22,24,27,28,30,33,65,81,85,92
+VCCP	+VCCP	3,6,7,25,26,27,37,47,63,82
+3V	+3V	24,37,51,63,65,91

System Memory Impedance Compensation
Huron River platform Design Guide 436735 P.88 Table 37.
Eric Fang to Alan Chien 11/15/2010
Huron River platform Design Guide Update 440484
SM_RCMP_1 use 26ohm 1%



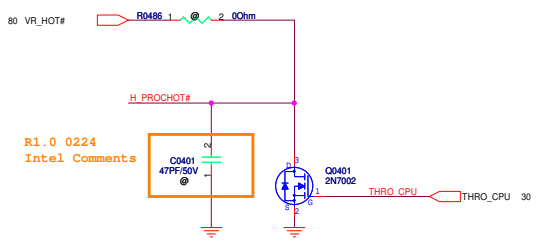
- If don't support S3 power reduction
1. Unmount R0450, R0452, U0404, R0453, Q0403, C0404, R0455, R0454, C0405
 2. Change R0449 to 200ohm from 1kohm, change R0409 to 130ohm from 0ohm - Design Guide 1.0 page 106
 3. Unmount Q0501, C0501, R0506, R0504, R0507
 4. Mount R0501, change r0508 to 0ohm from 1kohm
 5. Unmount Q0701, R0703, R0705, Q0702
 6. Mount R0702 and short J0701
 7. Unmount R2232, R2231, Q2203

Reserve S3 power reduction schematic

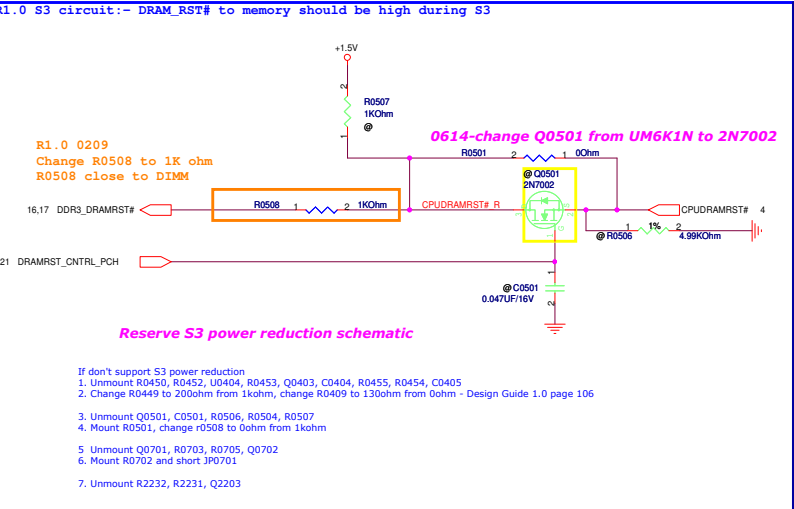
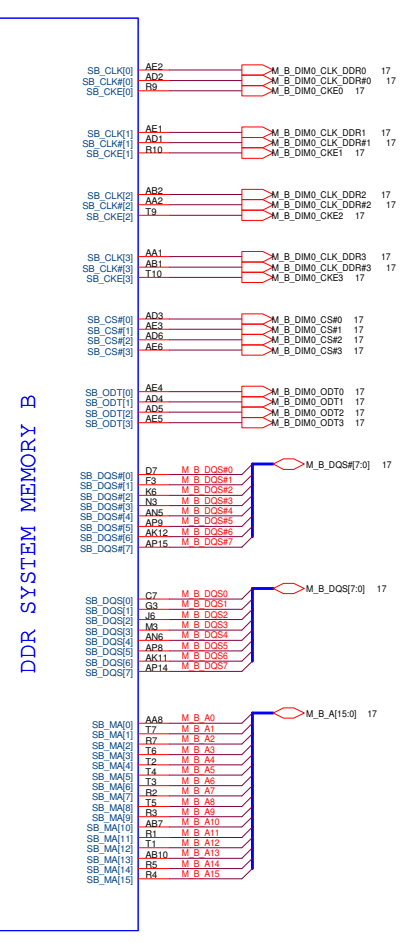
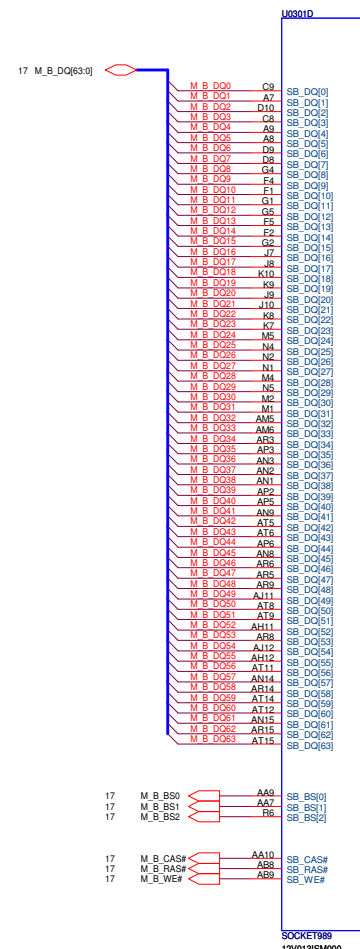
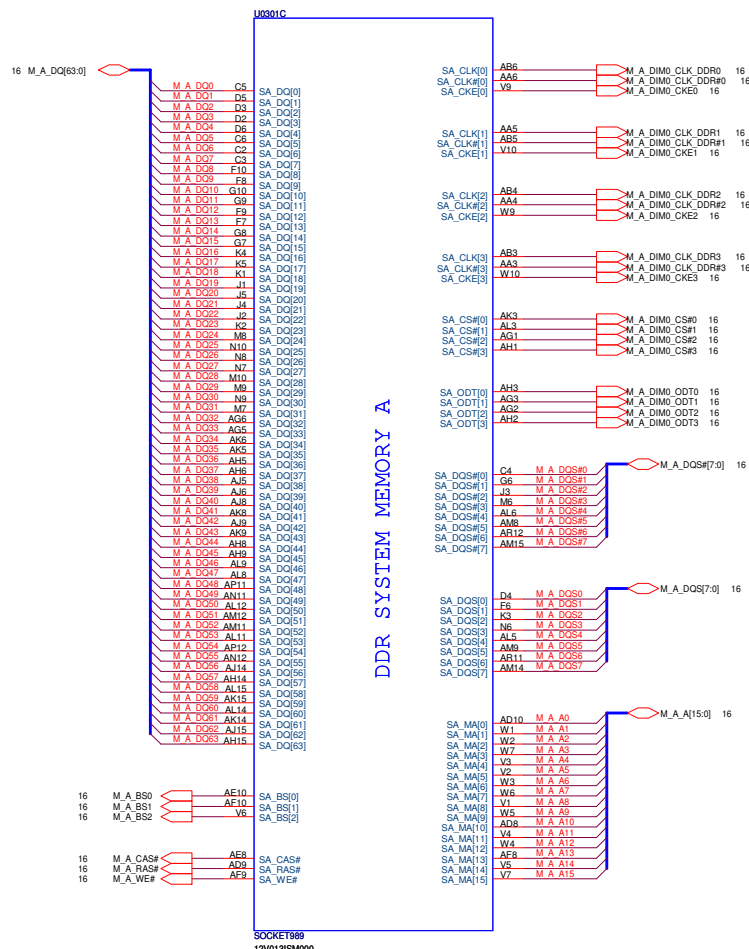


R1.0 0119
Sandy Bridge: R0417 = 750 ohm (10V220000093)
Ivy Bridge: R0417 = 680 ohm (10V240000041)

Frank
0506 EVERST check



R1.0 0224
Intel Comments



Vcc for processor core
Voltage range: 0.3 - 1.52V

POWER

- SV-QC IOCMAX 94A
- SV-QC IOCMAX 53A
- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AG25 VCC11
- AF35 VCC12
- AF34 VCC13
- AF33 VCC14
- AF32 VCC15
- AF31 VCC16
- AF30 VCC17
- AF29 VCC18
- AF28 VCC19
- AF27 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y32 VCC54
- Y31 VCC55
- Y30 VCC56
- Y29 VCC57
- Y28 VCC58
- Y27 VCC59
- Y26 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- V26 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- U26 VCC80
- R35 VCC81
- R34 VCC82
- R33 VCC83
- R32 VCC84
- R31 VCC85
- R30 VCC86
- R29 VCC87
- R28 VCC88
- R27 VCC89
- R26 VCC90
- P35 VCC91
- P34 VCC92
- P33 VCC93
- P32 VCC94
- P31 VCC95
- P30 VCC96
- P29 VCC97
- P28 VCC98
- P27 VCC99
- P26 VCC100

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

Voltage for the memory controller and shared cache defined at the motherboard VCCIO_SENSE and VSS_SENSE_VCCIO

ICCMAX_VCCIO 8.5A

R1.0 0126
Intel Comments

R1.0 0126
Intel Comments

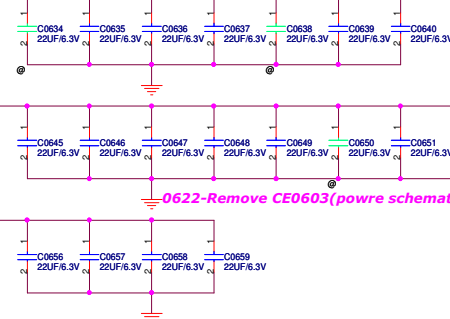
R1.0 0126
Intel Comments

Frank
20110602 check pull up/pull down reserve power schematic or not.

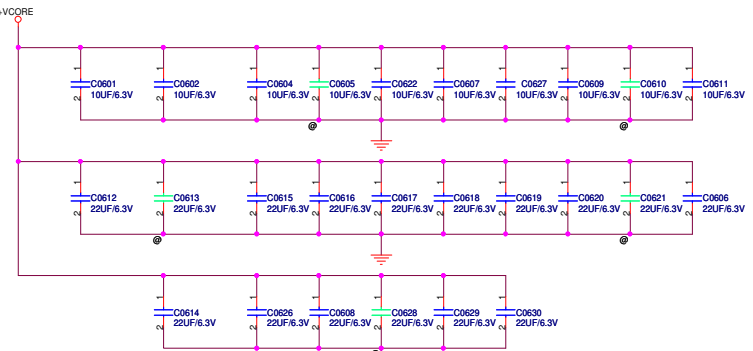
Frank
20110516 Change VCCP_SENSE to VCCIO_SENSE and change VSSP_SENSE to VSSIO_SENSE for meet power schematic.

Frank
20110516 Remove R0601 and R0604, because Power is already reserved

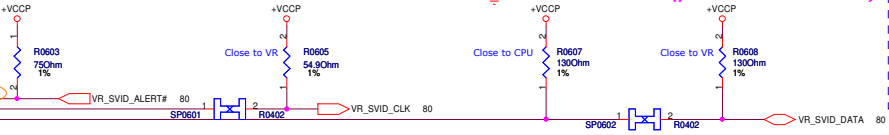
0614-Remove C0641 and nostuff C0651,C0647,C0658



0622-Remove CE0603(powre schematic reserve)



0622-Remove CE0601(powre schematic reserve)



+VCCP 3.4,7,25,26,27,37,47,63,82
+VCCORE 63,80

Check net name??

HR_Decoupling guide from Intel (POWER + EE)
+VCCP 22uF * 19pcs (7 nostuff)
330uF * 3pcs

EIH31/30 (EE)
+VCCP 10uF * 19pcs (2pcs no stuff)
22uF * 10 pcs (total no stuff)
330 uF * 1pcs Power support

CR_Decoupling guide from Intel (POWER + EE)
+VCCP 22uF * 19pcs (7 nostuff)
330uF * 3pcs

Decoupling guide for Everest (EE)
+VCCP 22uF * 19pcs (7 no stuff)
330uF * 1pcs (1 no stuff)=>JE31HR/CR power support

HR_Decoupling guide from Intel (POWER + EE)
+VCC_CORE 22uF * 16pcs
10uF * 10pcs
470uF * 4pcs

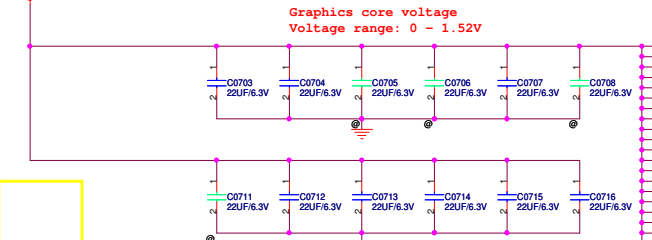
EIH31/30
+VCC_CORE 22uF * 14pcs(6pcs unmount)
10uF * 16pcs (4pcs unmount)
470uF * 2pcs (Power support)

CR_Decoupling guide from Intel (POWER + EE)
+VCC_CORE 22uF * 16pcs
10uF * 10pcs
470uF * 4pcs

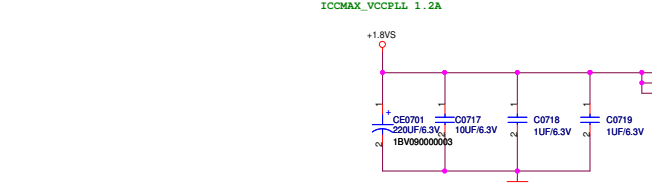
Decoupling guide for Everest (EE)
+VCC_CORE 22uF * 16pcs (8 nostuff)
10uF * 10pcs (3 nostuff)
470uF * 1pcs=>JE31HR/CR power support

SV-QC ICCMAX_VA_XG 33A
 SV-DC ICCMAX_VA_XG 33A
 +VGFX_CORE

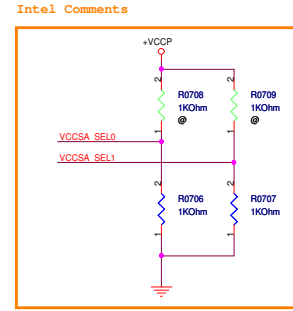
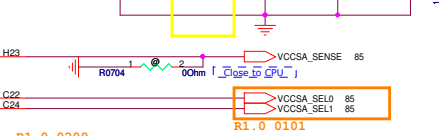
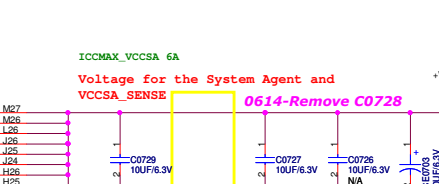
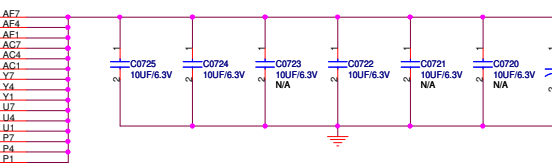
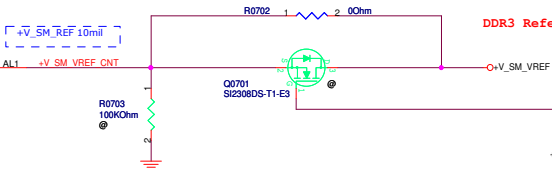
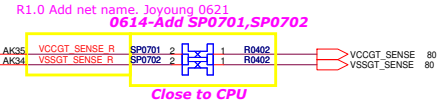
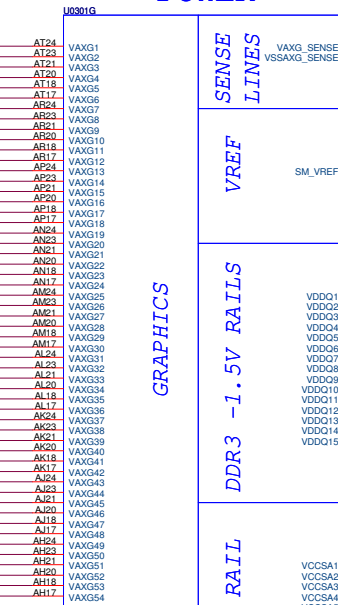
POWER



- 0622-Remove CE0705(powre schematic reserve)**
- HR_Decoupling guide from Intel (POWER + EE)**
 +VGFX_CORE 22uF * 12pcs
 470uF * 2pcs
- EIH31/30**
 +VCCP 22uF * 16 pcs (6 unmount)
 330uF * 1pcs (power support)
 470uF * 1pcs (EIH31 Del 470uF For Layout)
- CR_Decoupling guide from Intel (POWER + EE)**
 +VGFX_CORE 22uF * 12pcs
 470uF * 2pcs
- Decoupling guide for Everest (EE)**
 +VGFX_CORE 22uF * 12pcs (2 nostuff)
 470uF * 1pcs (JE31HR/CR power support)
- PLL supply voltage (DC + AC specification)**



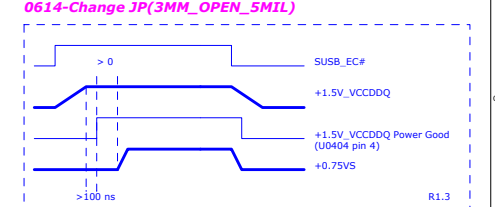
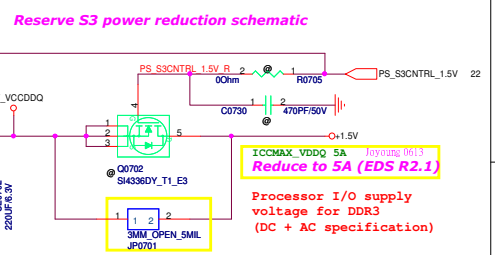
- HR_Decoupling guide from Intel (POWER + EE)**
 +1.8VS 1uF * 2pcs
 10uF * 1pcs
 330uF * 1pcs
- EIH31/30**
 +1.8VS 1uF * 2pcs
 10uF * 1pcs
 2.2uF*1pcs
 4.7uF*1pcs
 22uF * 1pcs (un-mount)
- CR_Decoupling guide from Intel (POWER + EE)**
 +1.8VS 1uF * 2pcs
 10uF * 1pcs
 330uF * 1pcs
- Decoupling guide from Everest (EE)**
 +1.8VS 1uF * 2pcs
 10uF * 1pcs
 100uF * 1pcs



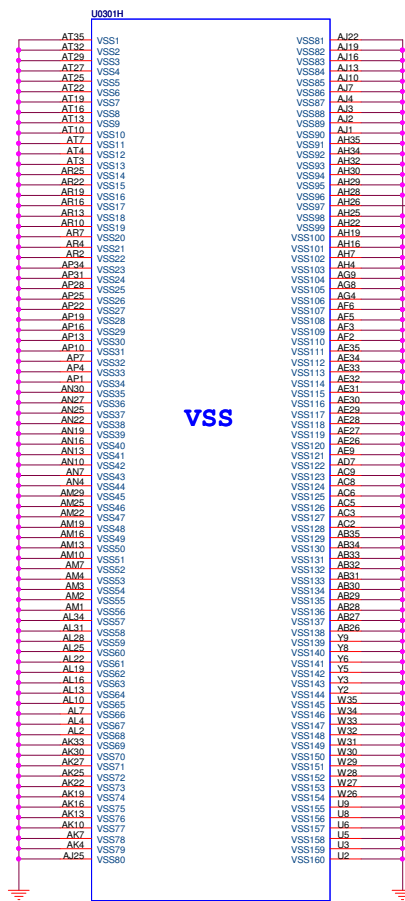
+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

- HR_Decoupling guide from Intel (POWER + EE)**
 +VCCSA 10uF * 3pcs
 330uF * 1pcs
- EIH31/30**
 +VCCSA 10uF * 4pcs (2 nostuff)
 100uF * 1pcs
- CR_Decoupling guide from Intel (POWER + EE)**
 +VCCSA 10uF * 3pcs
 330uF * 1pcs
- Decoupling guide for Everest (EE)**
 +VCCSA 10uF * 3pcs (1 nostuff)
 100uF * 1pcs

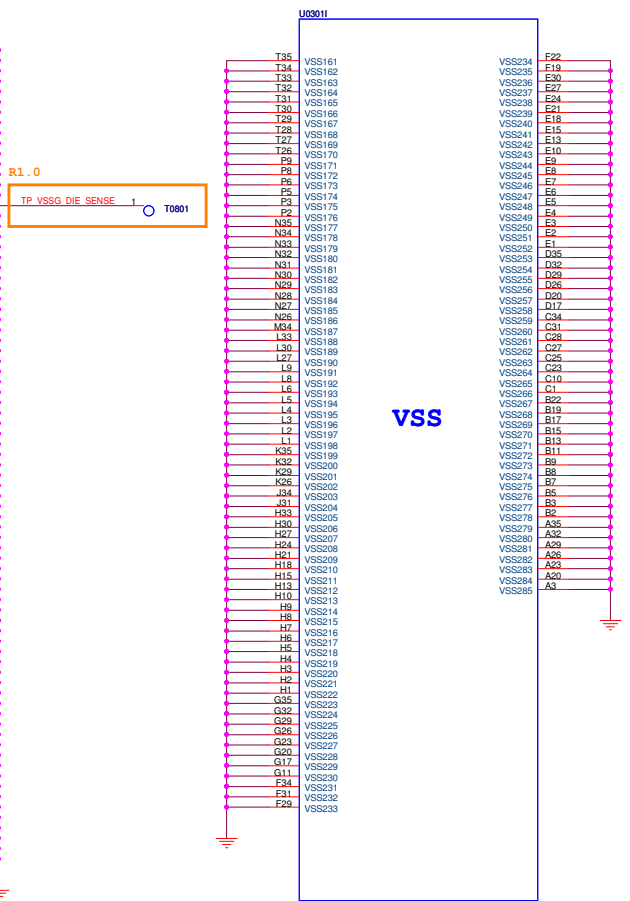
- +VCCP 3.4,6,25,26,27,37,47,63,82
- +1.5V 5,16,51,63,83
- +VCCSA 85
- +1.8VS 25,26,63,84
- +VGFX_CORE 63,80
- +1.5V_VCCDDQ 4
- +V_SM_VREF 18



- HR_Decoupling guide from Intel (POWER + EE)**
 +VDDQ 10uF * 6pcs
 330uF * 1pcs
- EIH31**
 +VDDQ 10uF * 6pcs (3 nostuff)
 220uF * 1pcs
- CR_Decoupling guide from Intel (POWER + EE)**
 +VDDQ 10uF * 6pcs
 330uF * 1pcs
- Decoupling guide for Everest (EE)**
 +VDDQ 10uF * 6pcs (3 nostuff)
 220uF * 1pcs



VSS



VSS

R1.0
TP VSSG DIE SENSE 1 70801

CFG strapping information:

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches socket pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection

- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded DisplayPort

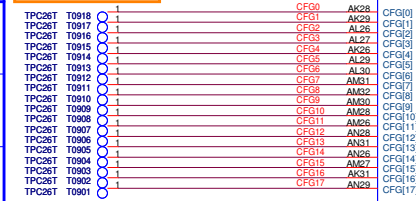
CFG[6:5]: PCI Express Port Bifurcation Straps

- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

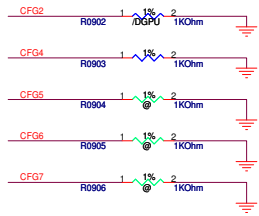
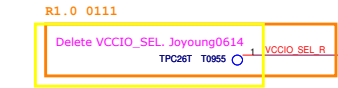
CFG[7]: PEG DEFER TRAINING

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training

R1.0
Add CFG0
Frank
0516 Remove CFG0 to XDP



DIMM0_VREF_DQ_R Pull Down 1k ohm
DIMM1_VREF_DQ_R Pull Down 1k ohm
Design Guide 1.0 P.89 Figure 44 (436735)



This model is UMA, unmount R0902 (use Default)

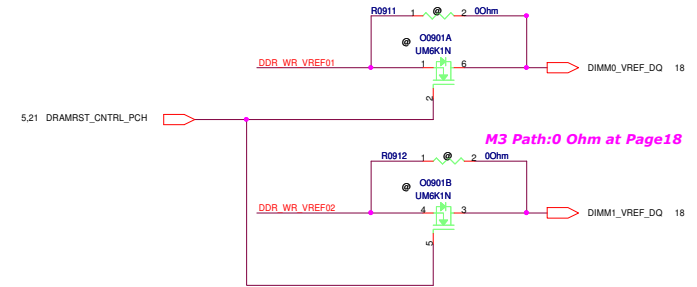
Power schematic reserve 1.0V or not??

+VCCIO_SEL	
1	1.05V
0	1.00V

IVB VCCIO for Mobile and Desktop is changed from 1.0v to 1.05v, same as PPT VCCIO. (461017 WW23'11)

Frank
20110516 Change VCCP_SEL to VCCIO_SEL for meeting Power schematic defined

PROCESSOR DRIVEN Vref PATH WAS STUFFED BY DEFAULT:







Reserve S3 power reduction schematic

M3: Processor Generated SO-DIMM VREFDQ - New Requirement

Sandy Bridge CPU Only: M1 Implementation
Sandy Bridge/Ivy Bridge CPU: M1 and M3 Implementation

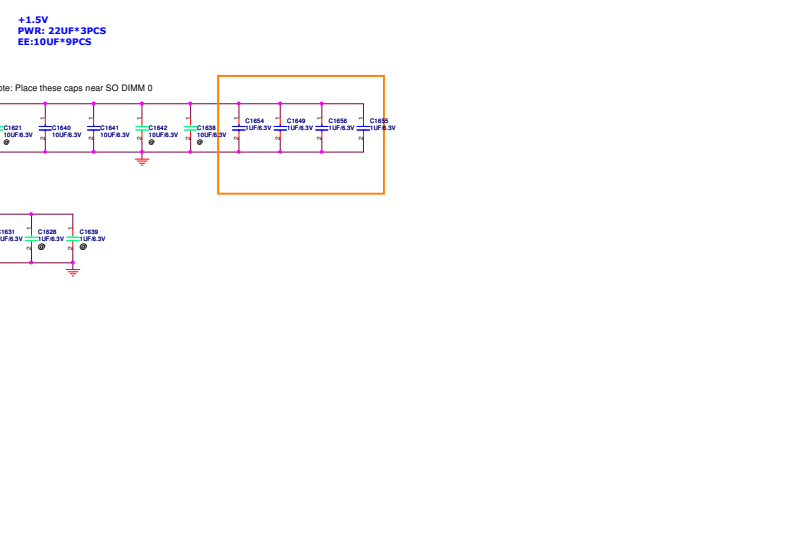
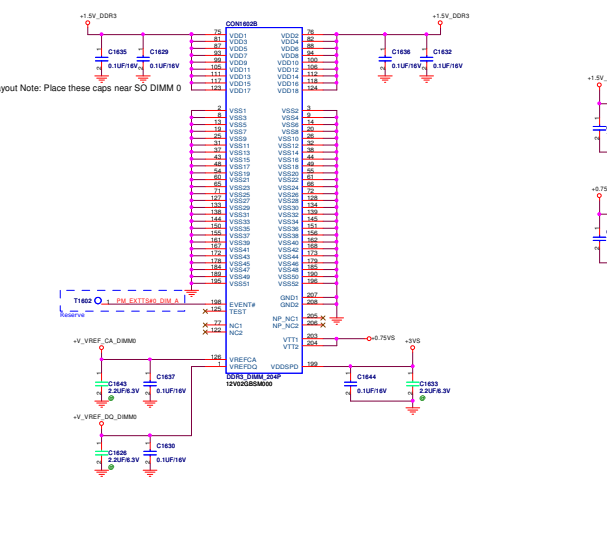
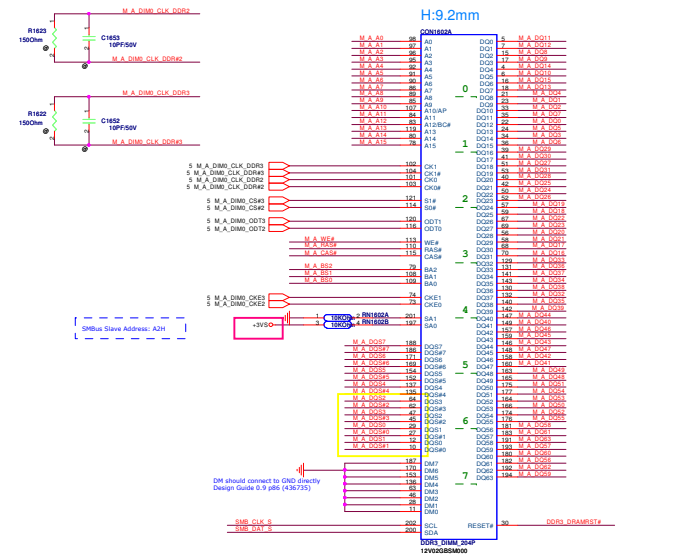
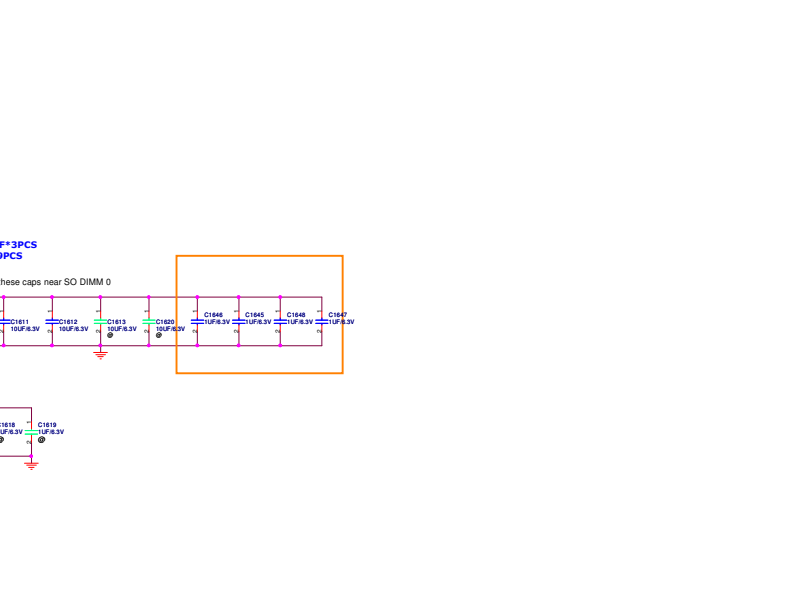
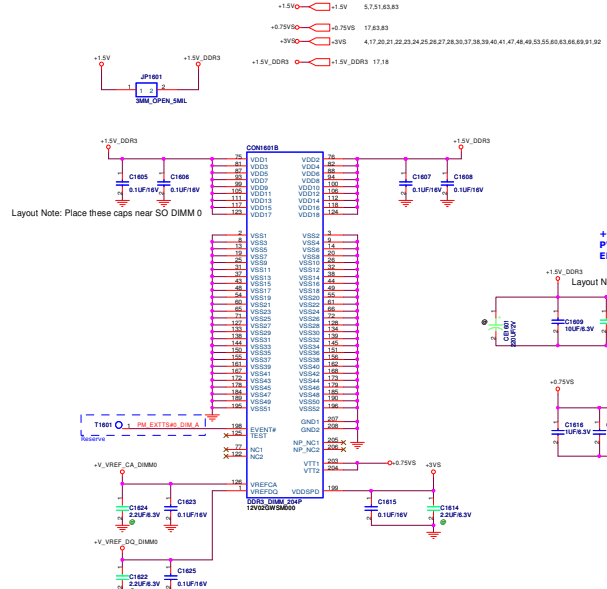
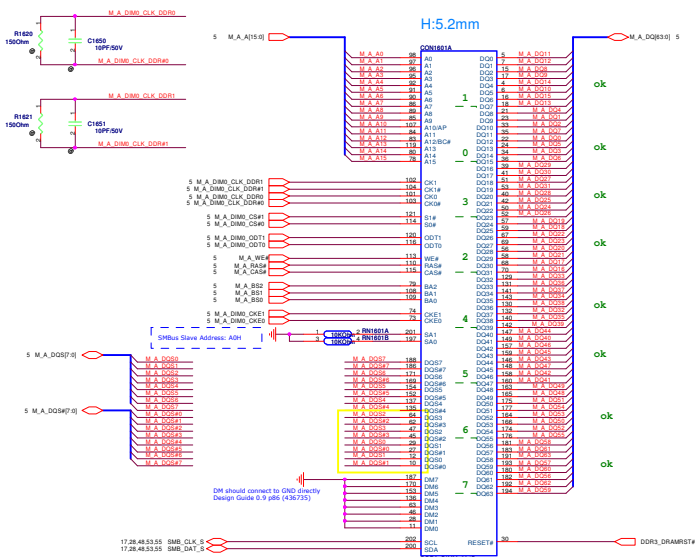
RESERVED

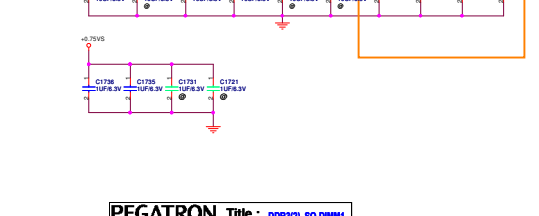
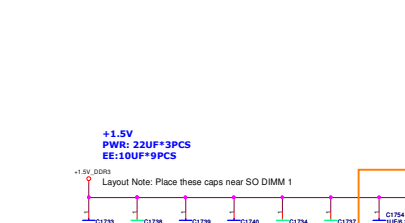
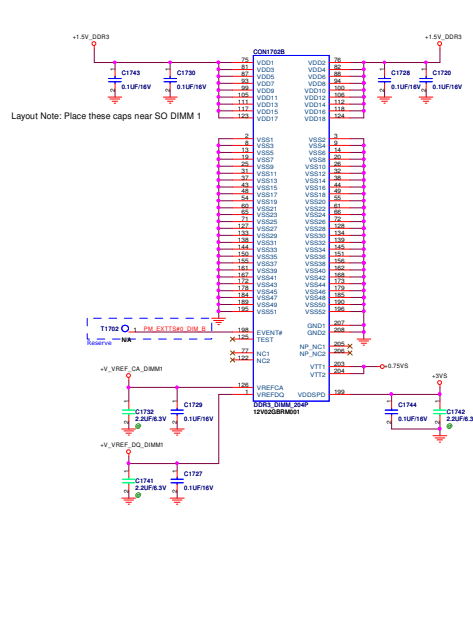
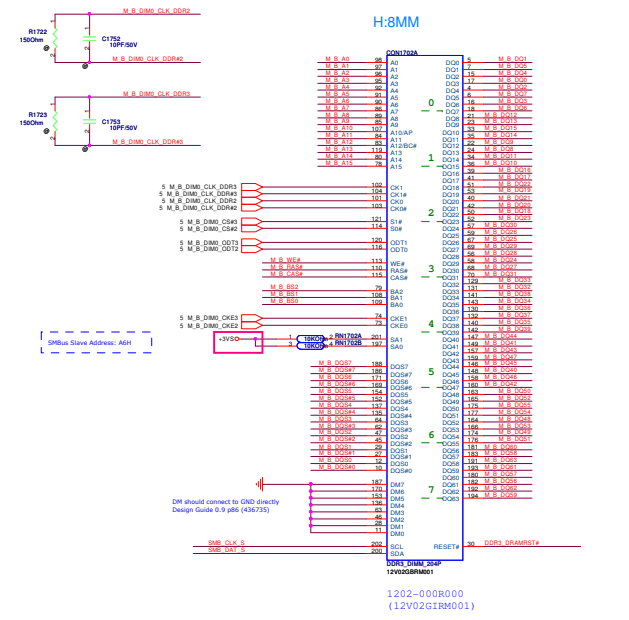
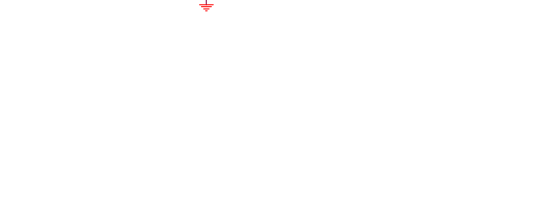
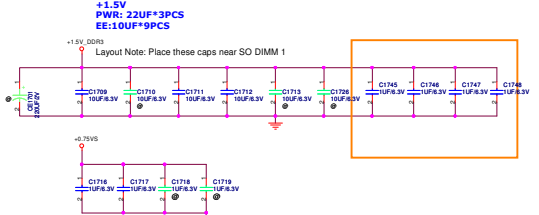
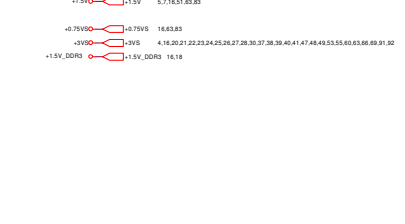
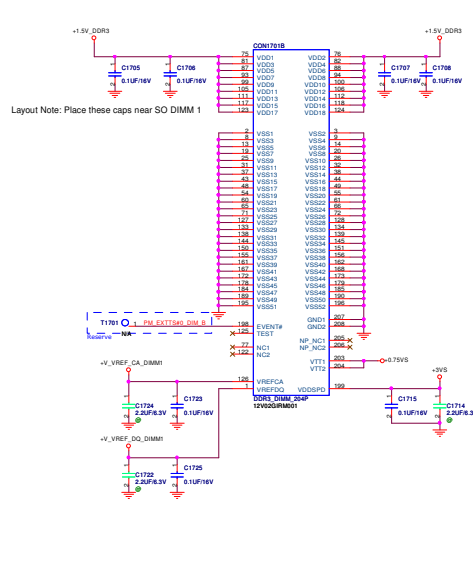
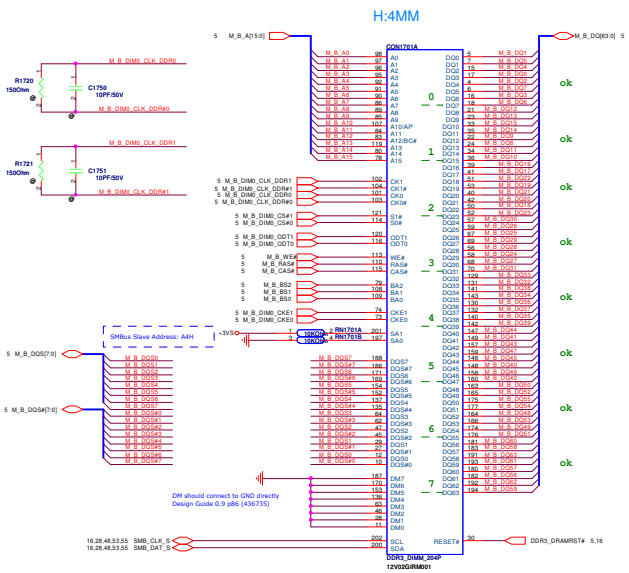
KEY

+VTT_PCH_ORG  +VTT_PCH_ORG 22,26,27
 +3VSUS  +3VSUS 4,22,24,27,28,30,33,65,81,85,92
 +VCCP  +VCCP 3,4,6,7,25,26,27,37,47,63,82
 +3VS  +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92

CPU XDP connector

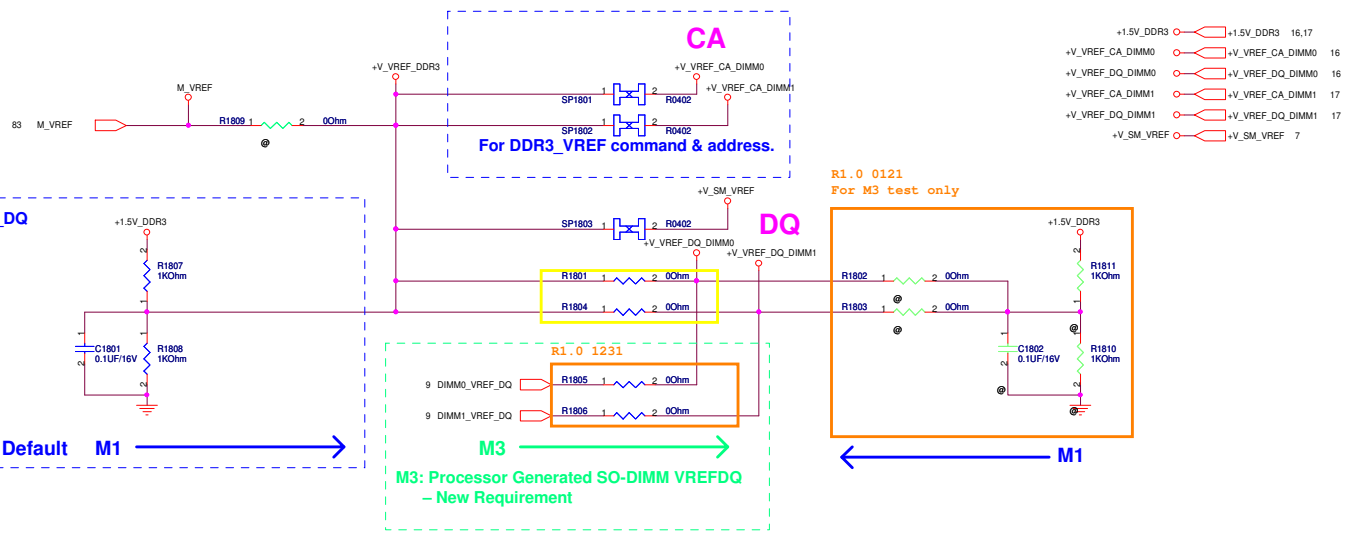
PCH XDP connector





PEGATRON Title : DDC3Q1 SO-DIMM1	
B01-C0000-Rev1.00	
Rev	1.2
Proj	PLFG
Eng	Alvaro_cdm
Appr	Alvaro_cdm

DDR3 Vref



If support M1 :(Sandy Bridge CPU Only)
 1. Un mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
 2. Mount R1801,R1804
 ==>CA and DQ are the same path

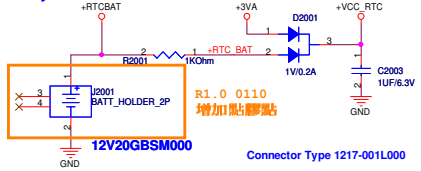
If support M1 and M3 :(Sandy Bridge/Ivy Bridge CPU)
 1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
 2. Un mount R1801,R1804
 ==> CA and DQ are separate path

Sandy Bridge CPU Only: M1 Implementation
Sandy Bridge/Ivy Bridge CPU: M1 and M3 Implementation

R1.4--2

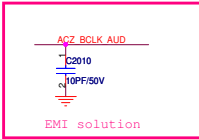
PEGATRON		Title : VID Controller	
PEGATRON COMPUTER INC		Engineer: <i>Wing Cheng</i>	
Size	Project Name	Rev	
C	BA52HR/CR	1.0	
Date: <i>Friday, February 03, 2012</i>		Sheet	19 of 94

RTC battery

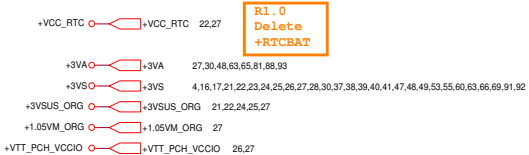


Connector Type 1217-001L000

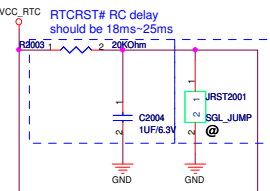
Request by CSC for CMOS clear function



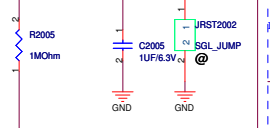
EMI solution



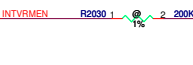
R1.0 Delete +RTC_BAT



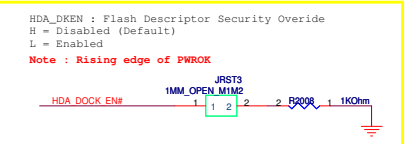
CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)



INTVRMEN: Integrated SUS 1.05V VRM Enables Low: Enable External VRs High: Enable Internal VRs

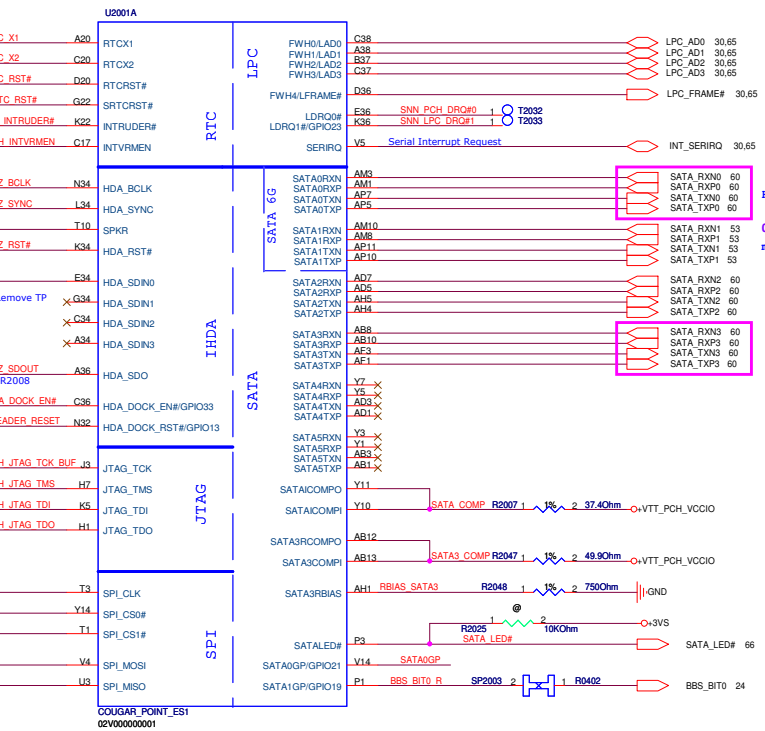
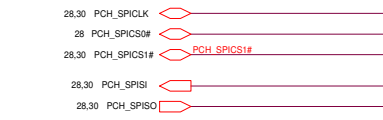
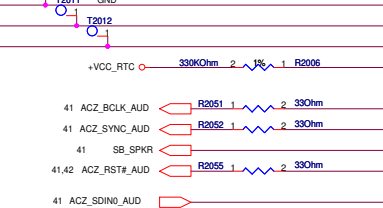
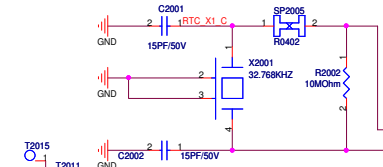


TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

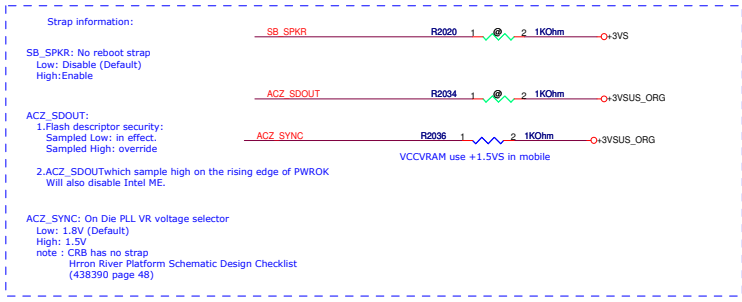


HDA_DKEN : Flash Descriptor Security Override
H = Disabled (Default)
L = Enabled
Note : Rising edge of PWROK

R1.0 add JRST3 to follow BIC50. Joyoung 0628



0200-00HU000 C.S. 907552 A1 QM-VY BGA942 INTEL/COUGAR POINT PCH



Strap information:

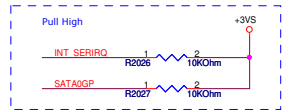
SB_SPKR: No reboot strap
Low: Disable (Default)
High: Enable

ACZ_SDOUT:

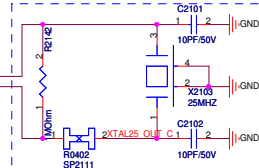
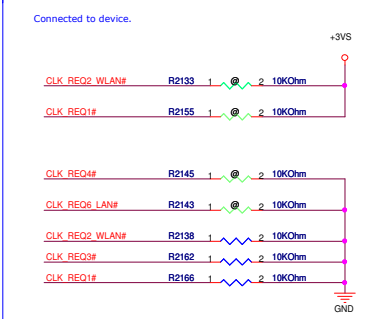
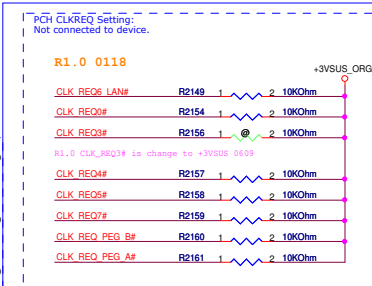
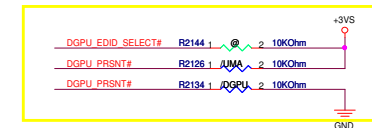
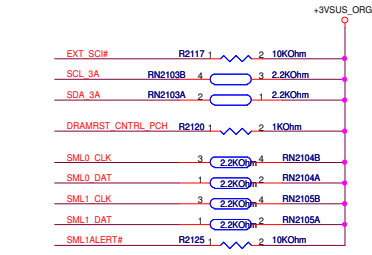
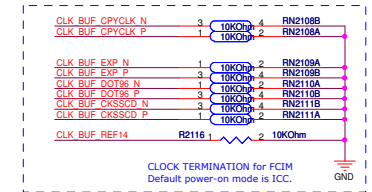
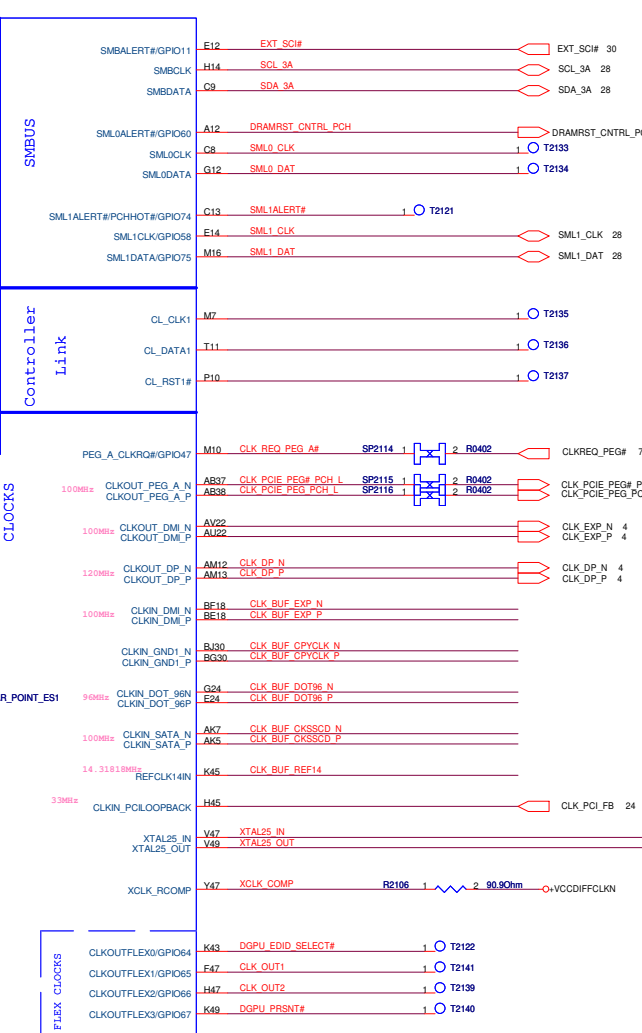
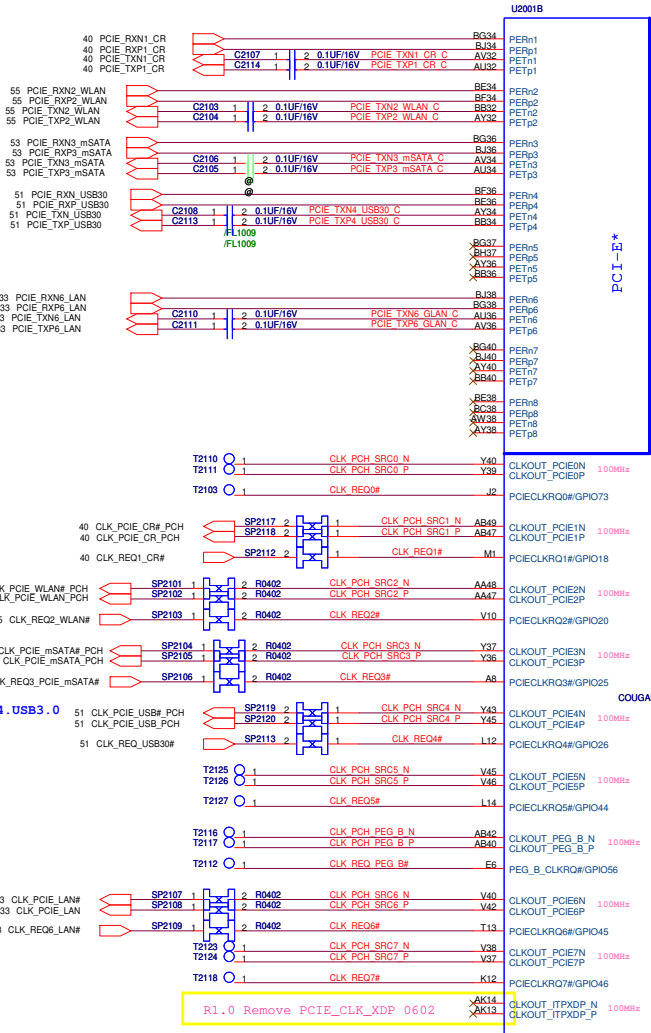
1. Flash descriptor security:
Sampled Low: in effect,
Sampled High: override

2. ACZ_SDOUT which sample high on the rising edge of PWROK
Will also disable Intel ME.

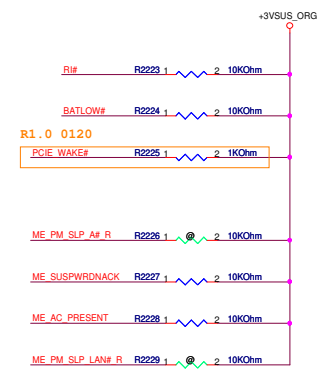
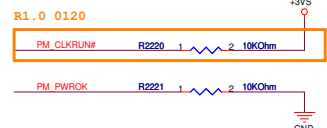
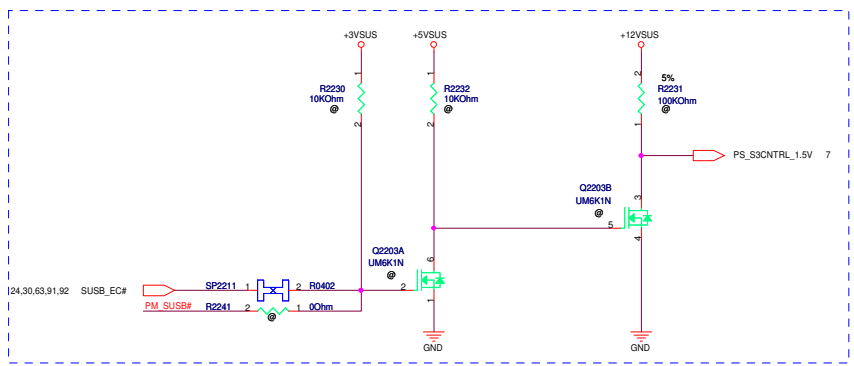
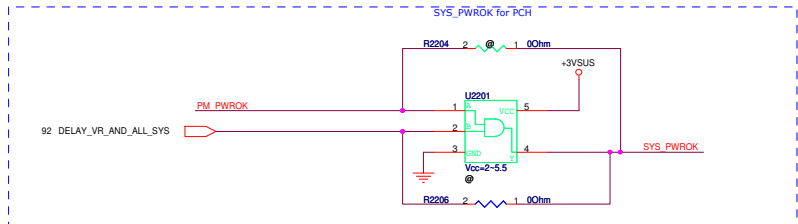
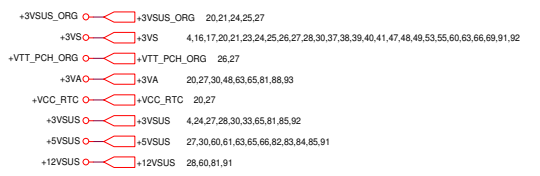
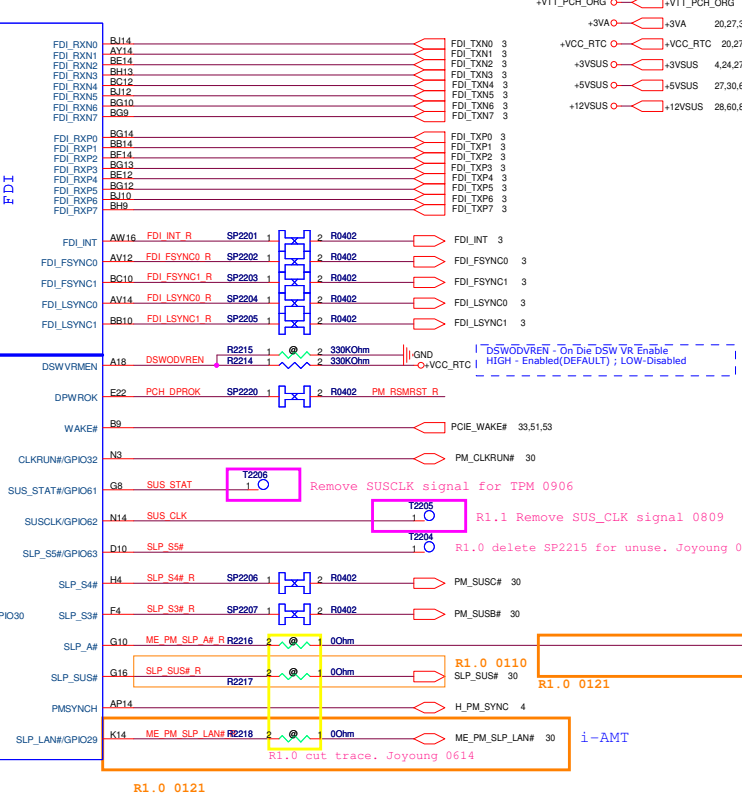
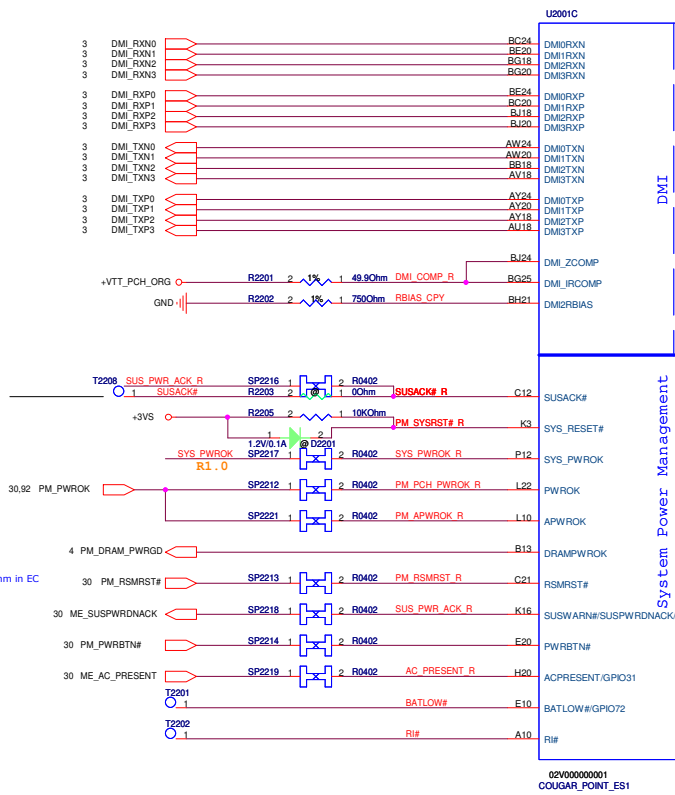
ACZ_SYNC: On Die PLL VR voltage selector
Low: 1.8V (Default)
High: 1.5V
note : CR8 has no strap
Hiron River Platform Schematic Design Checklist
(458390 page 48)

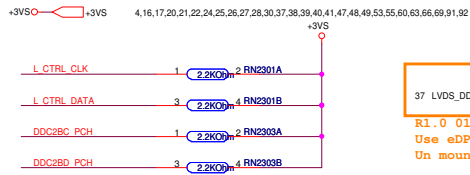


+3VS +3VS 4,16,17,20,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92
 +VTT_PCH_ORG +VTT_PCH_ORG 22,26,27
 +3VSUS_ORG +3VSUS_ORG 20,22,24,25,27

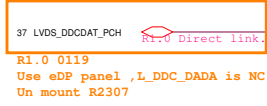


R1.0 Remove PCIE_CLK_XDP 0602

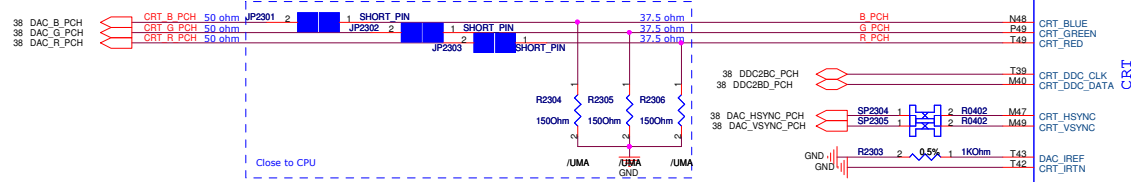




Frank
0506 Pull up 2.2k ohm in DDC bus for CRT and LVDS .



Frank
0426 modify CRT net name.



COUGAR_POINT_ES1
02/00000001

CRT Disable: (For discrete graphic)

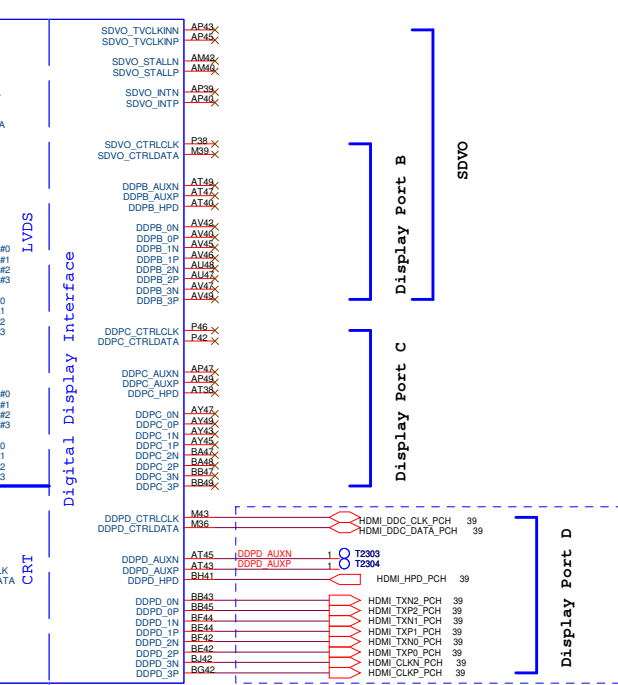
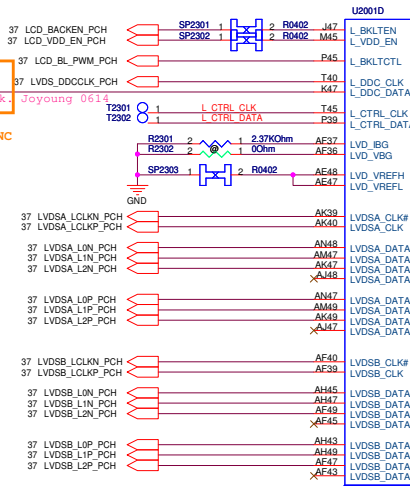
1. NC:
CRT_RED,CRT_GREEN,CRT_BLUE
CRT_HSYNC,CRT_VSYNC
2. 1-kΩ ±0.5% pull-down to GND:
DAC_IREF
3. Connected to GND:
CRT_ITRN
4. Connect to +V3.3:
VCCADAC

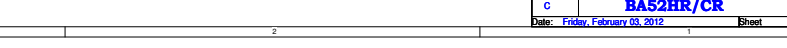
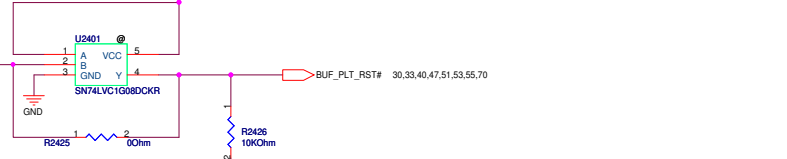
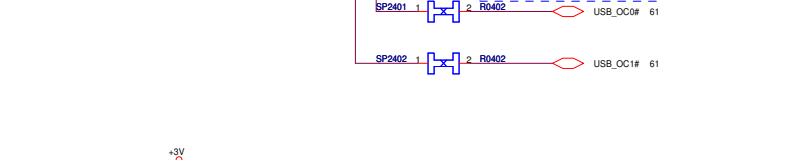
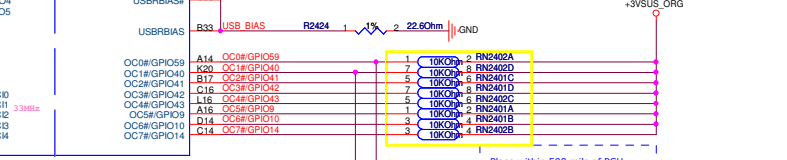
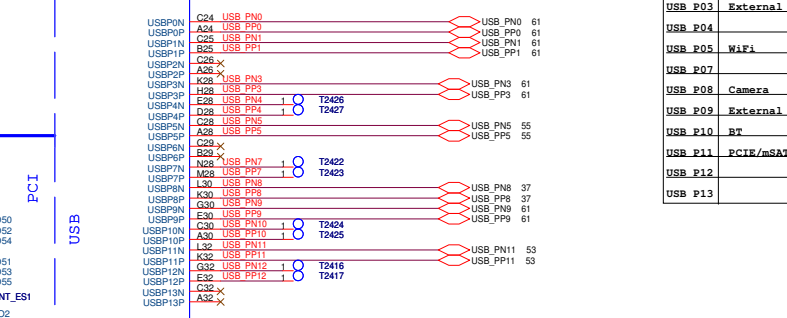
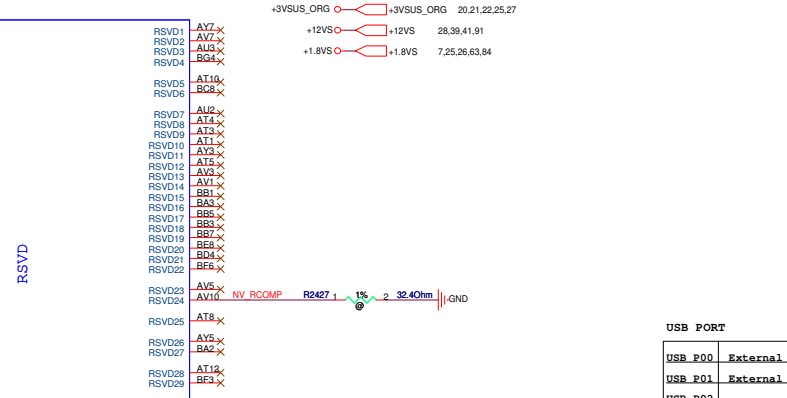
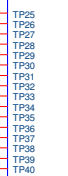
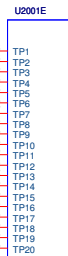
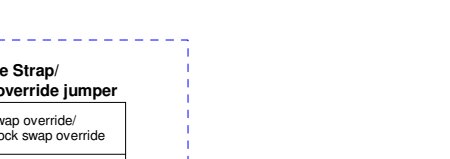
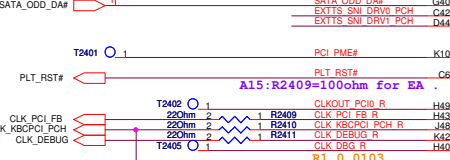
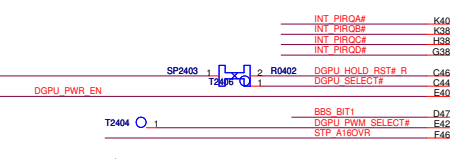
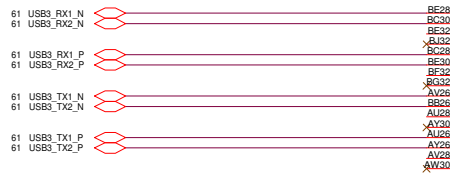
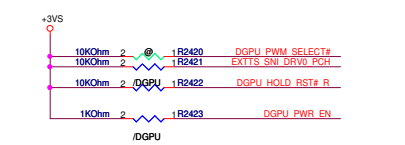
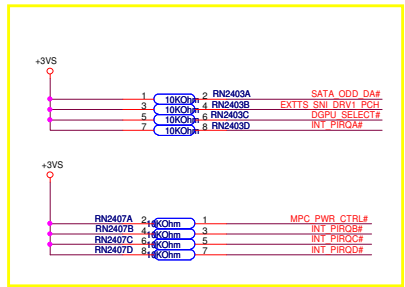
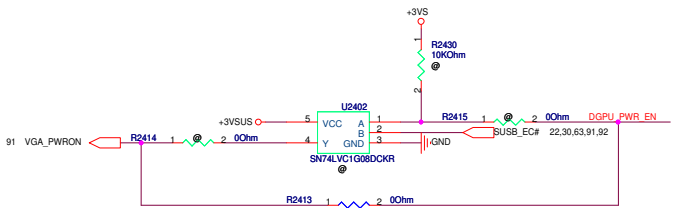
Display Port Disable: (For discrete graphic)

1. NC:
ALL

LVDS Disable: (For discrete graphic)

1. NC:
LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
LVD_VREFL, LVD_IBG, LVD_VBG
2. Connected to GND:
VccALVDS, VccTX_LVDS



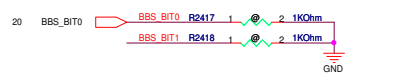


USB PORT	
USB P00	External 2.0/3.0
USB P01	External 2.0/3.0
USB P02	
USB P03	External 2.0
USB P04	
USB P05	Wifi
USB P07	
USB P08	Camera
USB P09	External 2.0
USB P10	BT
USB P11	PCIe/msATA
USB P12	
USB P13	

BBS_BIT0, BBS_BIT1 : Boot BIOS Strap

Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	Reserved
1	1	SPI (PCH)

Sampled on rising edge of PWROK.



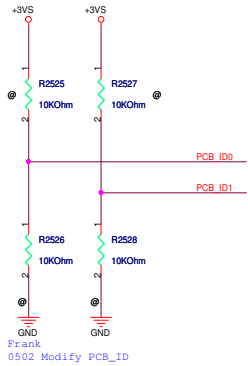
STP_A16OVR: A16 swap override/ Top-Block swap override jumper

Low=Enabled A16 swap override/
Top-Block swap override

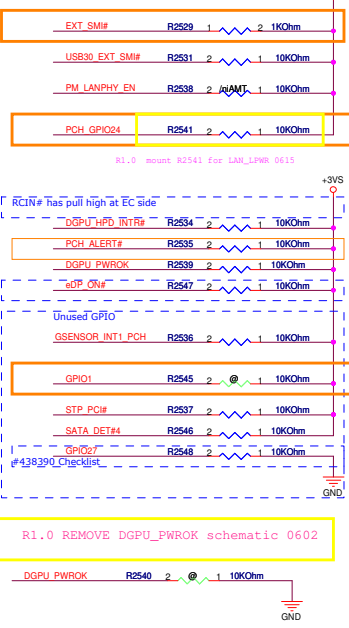
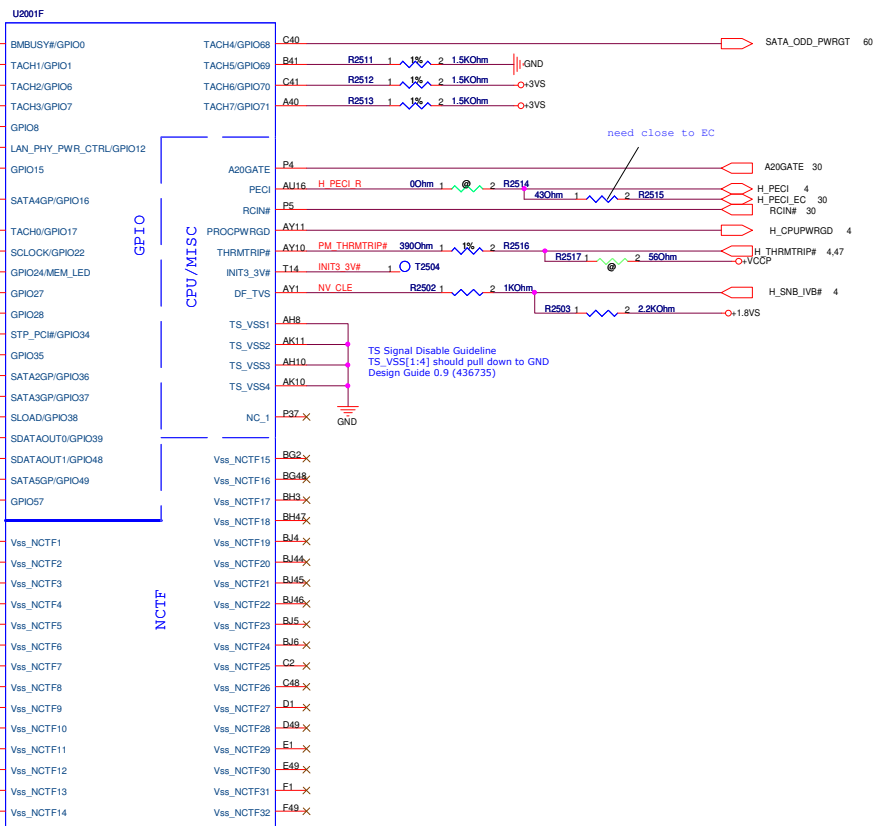
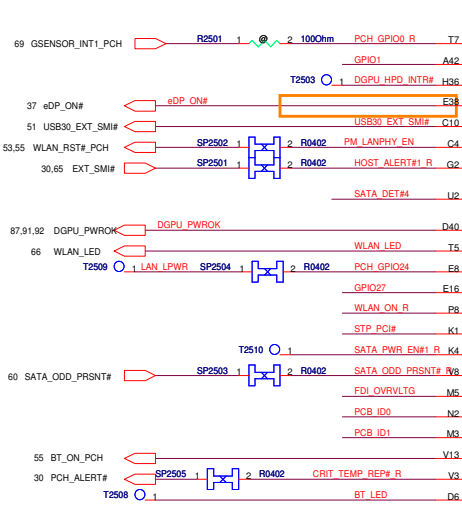
High=Default



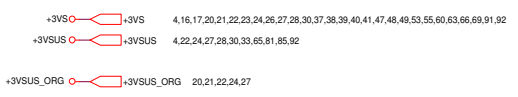
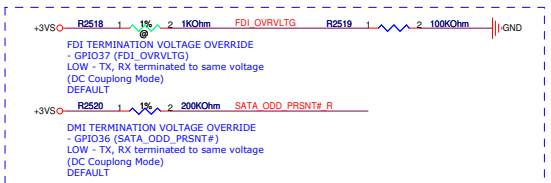
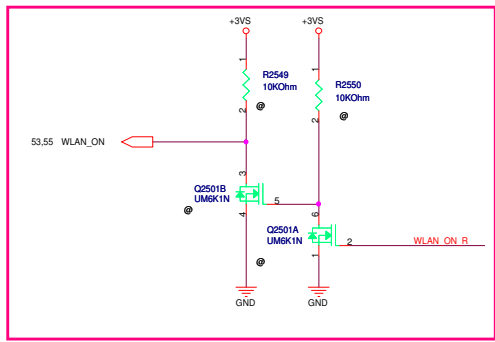
	PCB_ID1	PCB_ID0
A	L	L
B	L	H
C	H	L
MP		

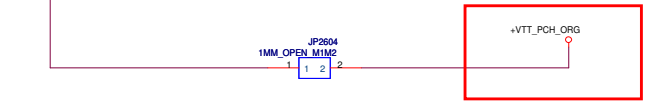
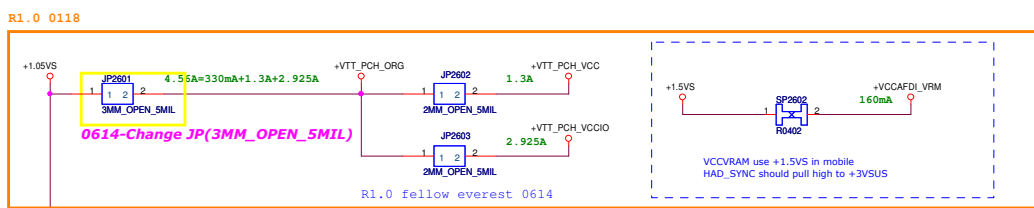
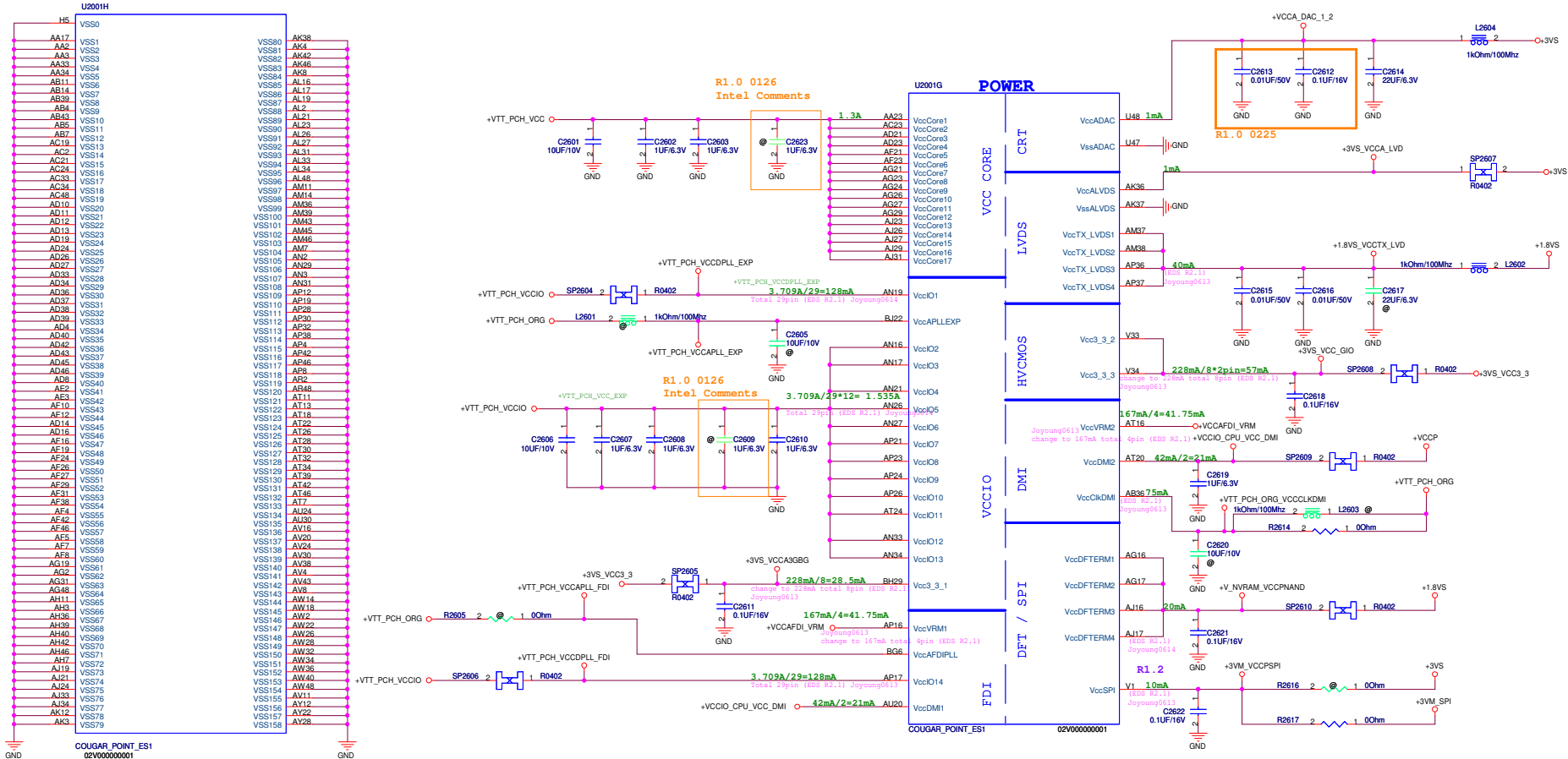


- R1.0**
- Add PCH_GPIO0_R.
 - Delete ICC_EN#.
 - Add PM_LANPHY_EN
 - Add HOST_ALERT#1_R.
 - Add SATA_DET#4_R.
 - DGPU_PWROK has 100 ms software delay, no hardware delay requirement
 - Reserve PCH_GPIO24
 - Add PLL_ODVVR_EN.
 - Add PSATA_PWR_EN#1_R.
 - Add SATA_ODD_PRSN#_R and FDI_OVRVLTG.
 - Add CRIT_TEMP_REP#_R.



- R1.0 0126 Intel Comments
- R1.0 0120
- R1.0 0119
- R1.0 0119



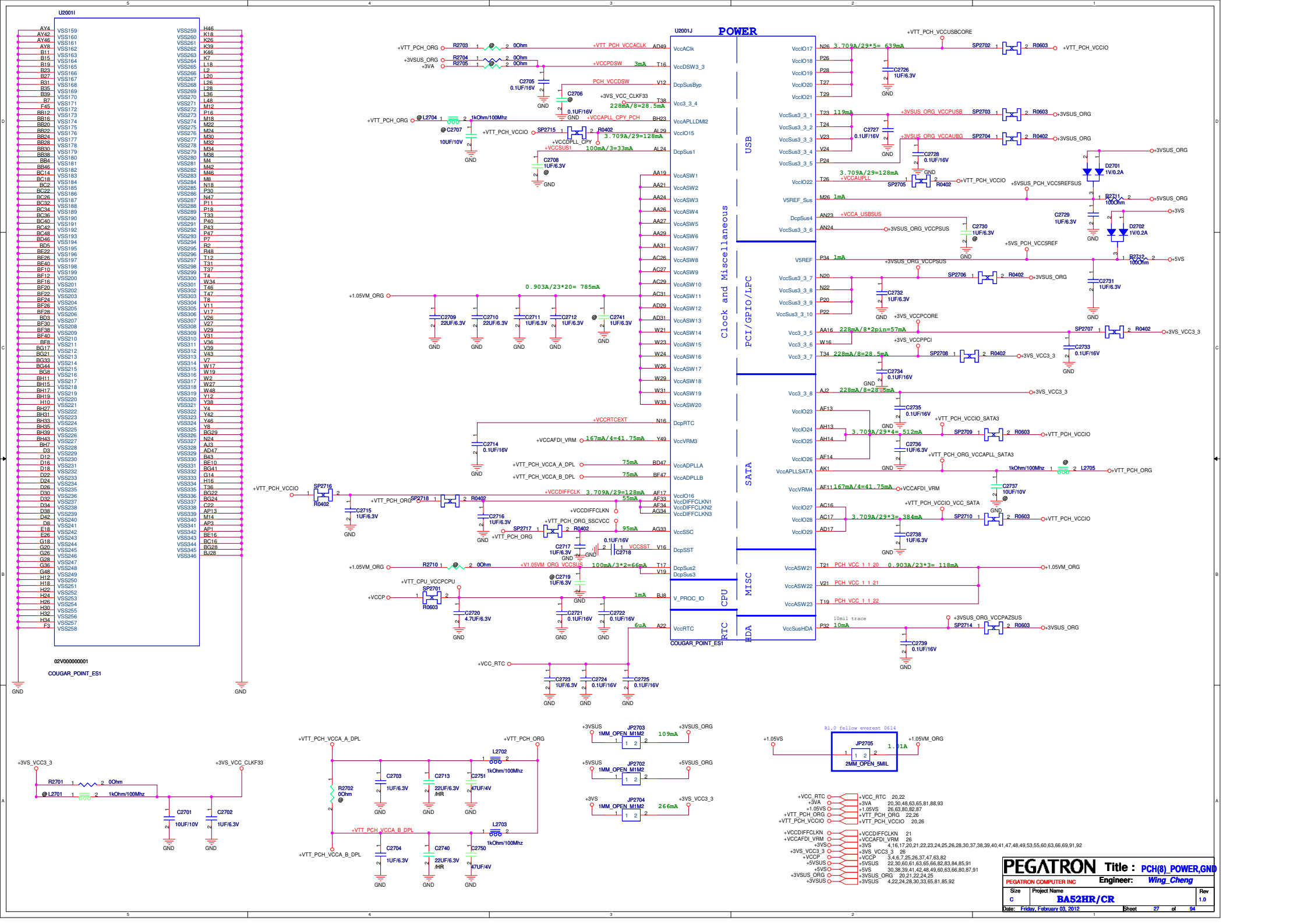


Pin list for power distribution:

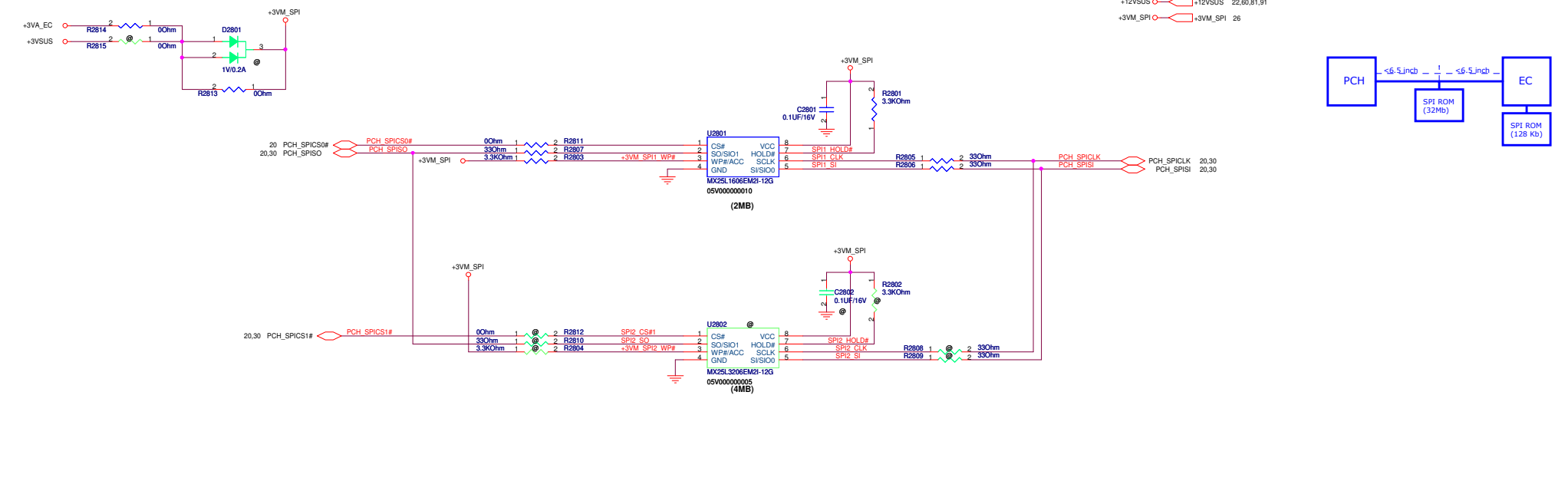
+VTT_PCH_VCCIO	+VTT_PCH_VCCIO	20,27
+VTT_PCH_ORG	+VTT_PCH_ORG	22,27
+1.05VS	+1.05VS	27,63,80,82,87
+1.5VS	+1.5VS	53,55,63,91
+VCCAFDI_VRM	+VCCAFDI_VRM	27
+3VS	+3VS	4,16,17,20,21,22,23,24,25,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92
+3VS_VCC3_3	+3VS_VCC3_3	27
+3VM_SPI	+3VM_SPI	28
+1.8VS	+1.8VS	7,25,63,84
+VCCP	+VCCP	3,4,6,7,25,27,37,47,63,82

R1.0 Delete

- +VTT_PCH_VCC
- +VTT_PCH_VCCDPLL_EXP
- +VTT_PCH_VCCAPLL_EXP
- +VTT_PCH_VCCDPLL_FDI
- +VTT_PCH_VCCAPLL_FDI
- +3VS_VCCA3GBG
- +3VS_VCC_GIO
- +VCCA_DAC_1_2
- +3VS_VCCA_LVDS
- +3VM_VCCPSPI
- +V_NVRAM_VCCPNAND
- +1.8VS_VCCCTX_LVD
- +VCCIO_CPU_VCC_DMI
- +VTT_PCH_ORG_VCCCLKDMI



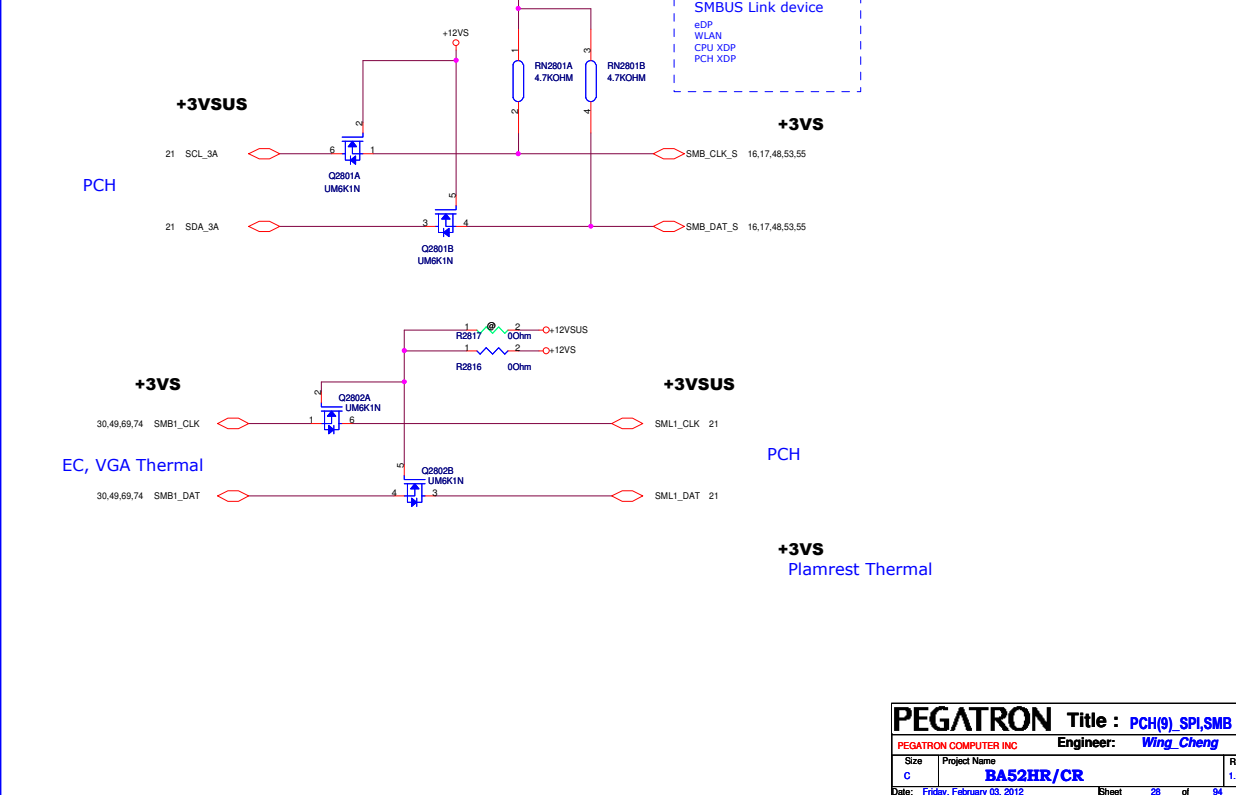
PCH SPI ROM



SPI Debug Connector

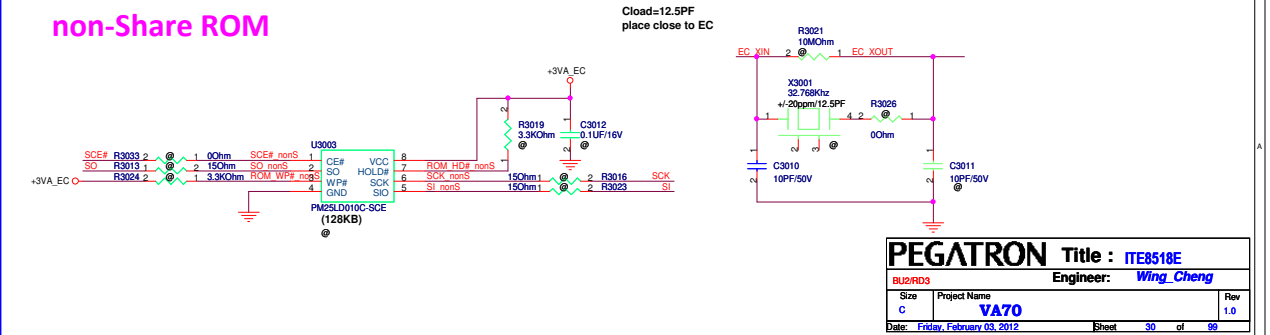
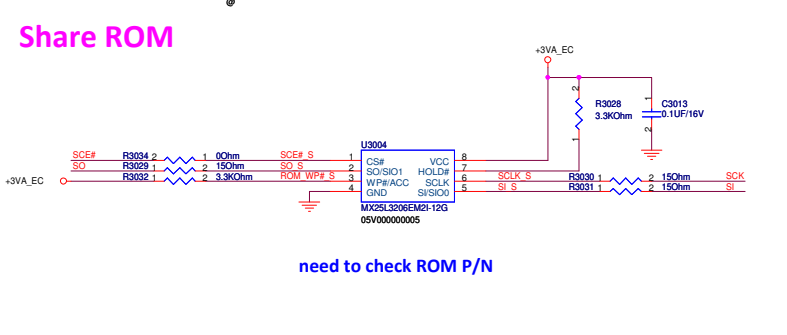
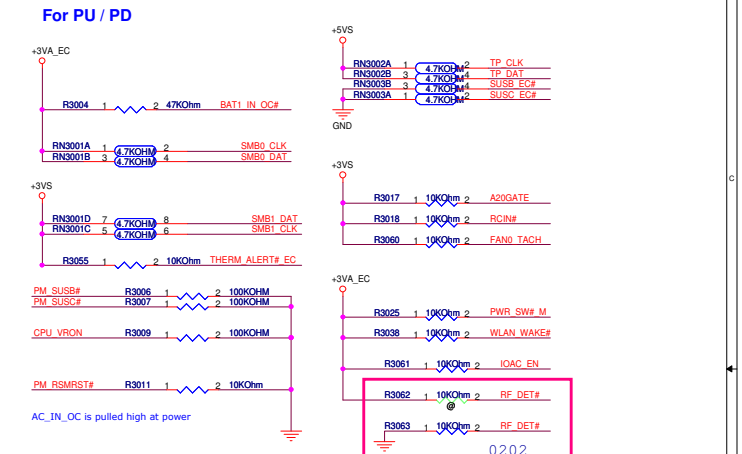
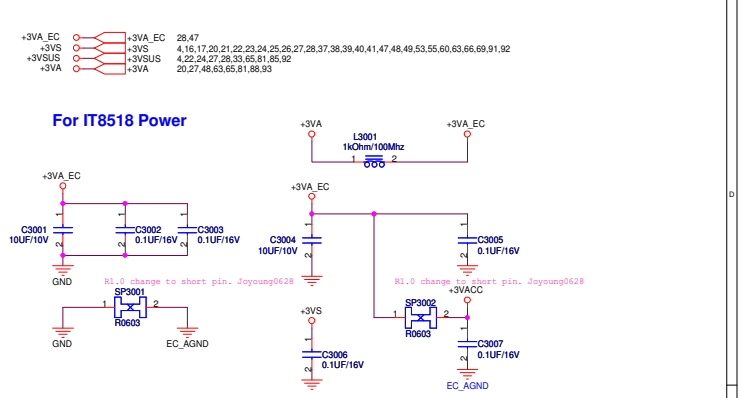
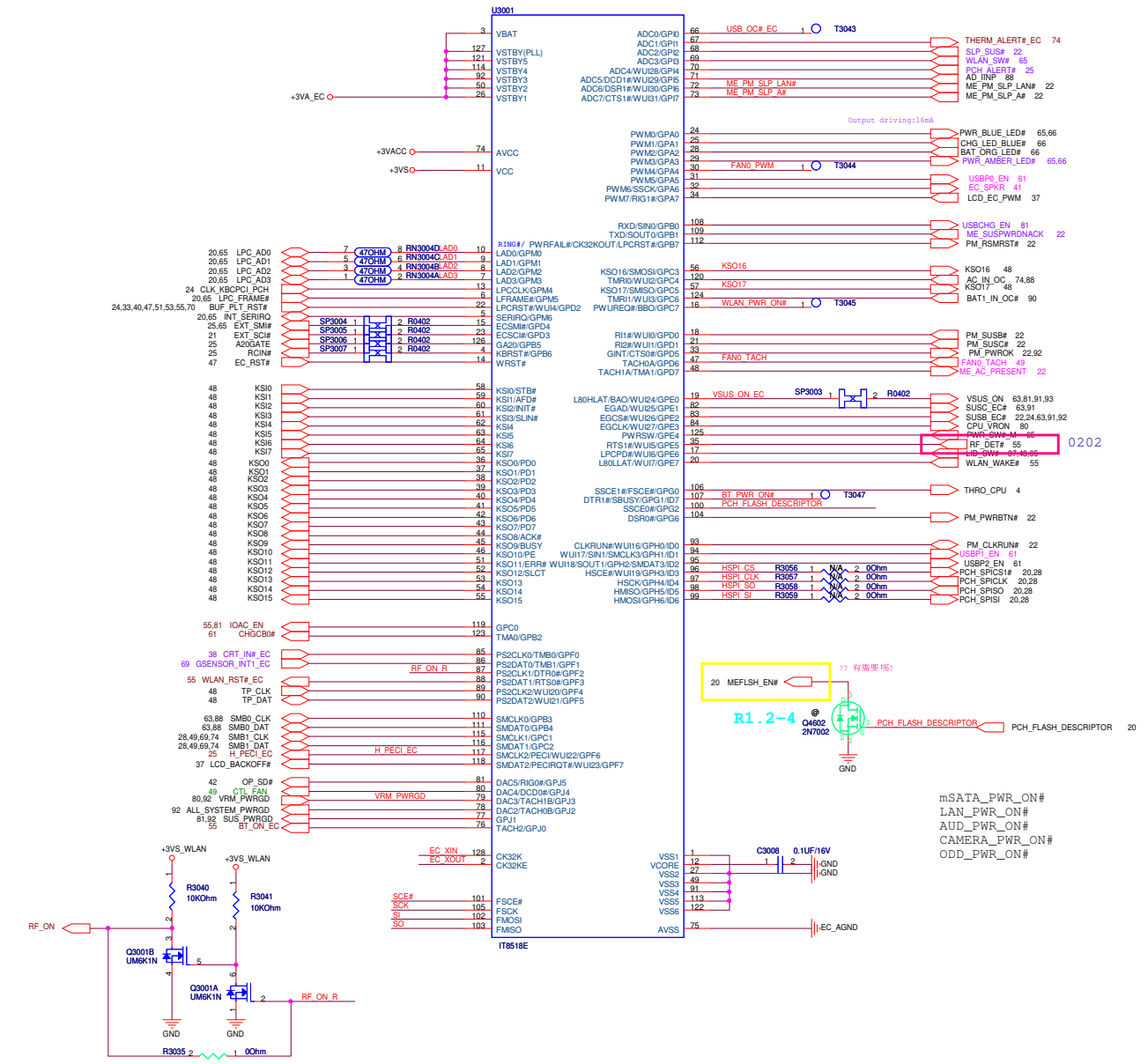


PCH SMBus





PEGATRON		Title : CLK_JCS9LRS3197	
PEGATRON COMPUTER INC		Engineer: Wing_Cheng	
Size	Project Name	Rev	
Custom	BA52HR/CR	1.0	
Date: Friday, February 03, 2012	Sheet	29	of 94



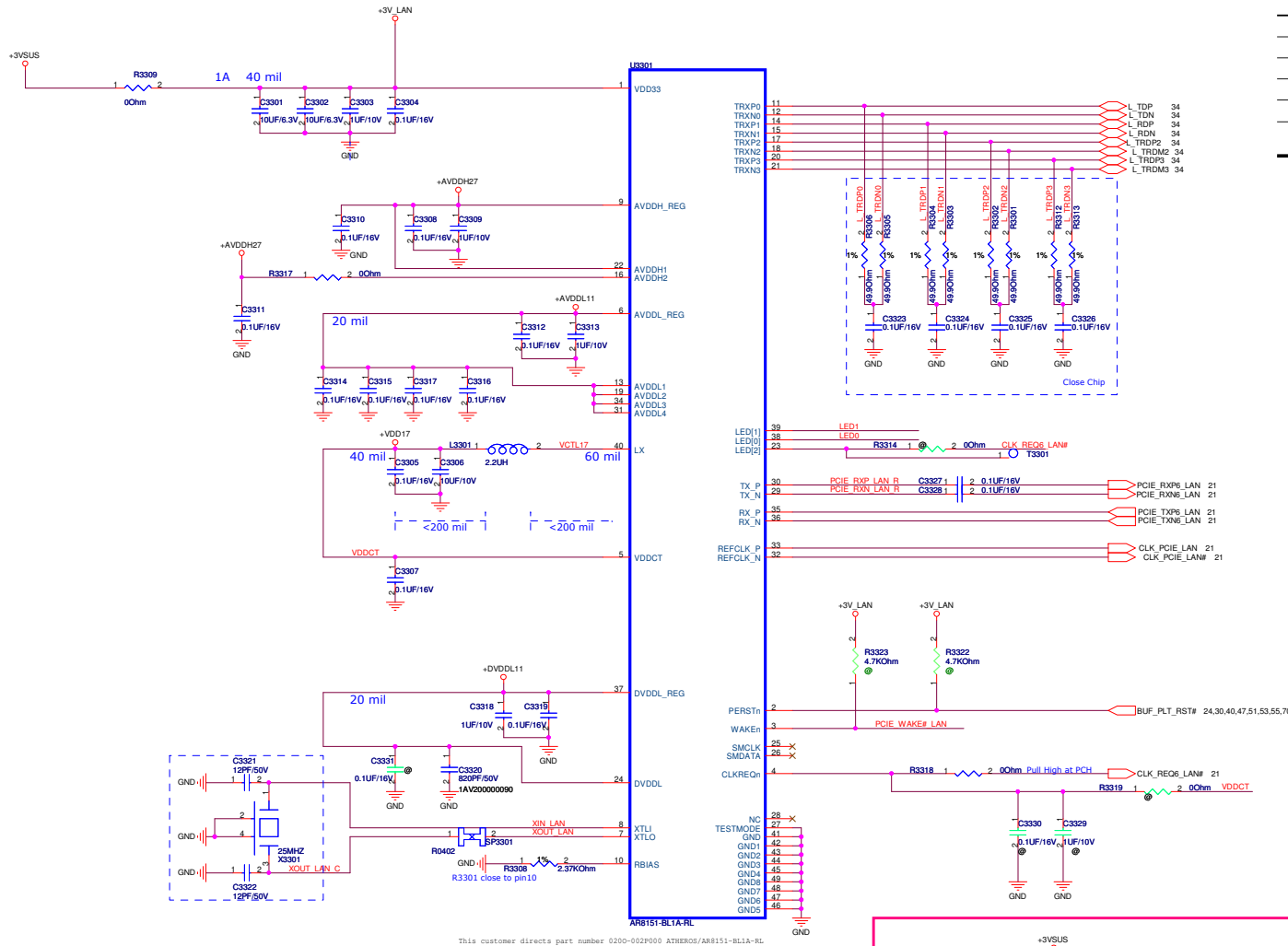
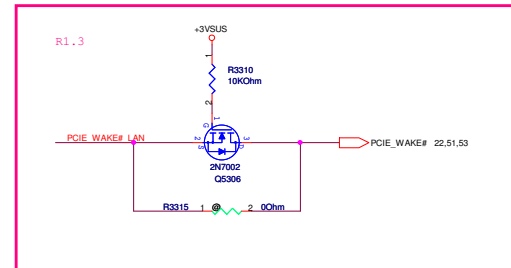
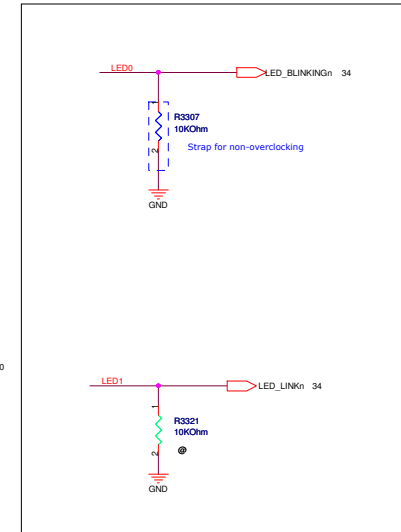


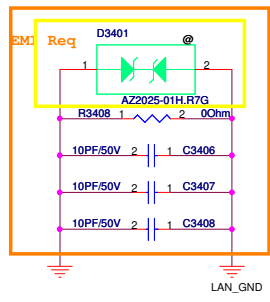
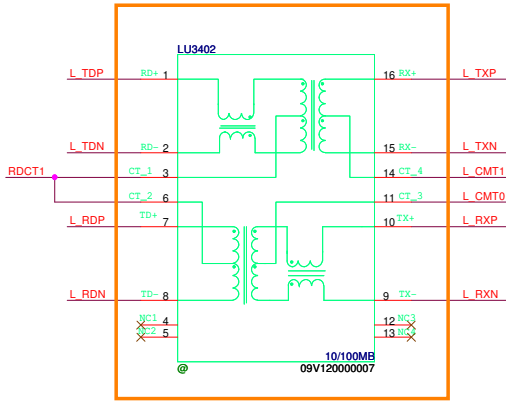
Table 2-6. LED Link Table

LED[0] LED_ACT	LED[1] LED_LINK	LED[2] LED_LINK_1000	Selected Speed	Link Status
High	High	High	Any Speed	Link Down
Blink	High	High	10 Mbps; Half-Duplex	Link Up
Blink	Low	High	10 Mbps; Full-Duplex	Link Up
Blink	Low	High	100 Mbps; Half-Duplex	Link Up
Blink	Low	High	100 Mbps; Full-Duplex	Link Up
Blink	Low	Low	Auto, 1000 Mbps, Full-Duplex	Link Up



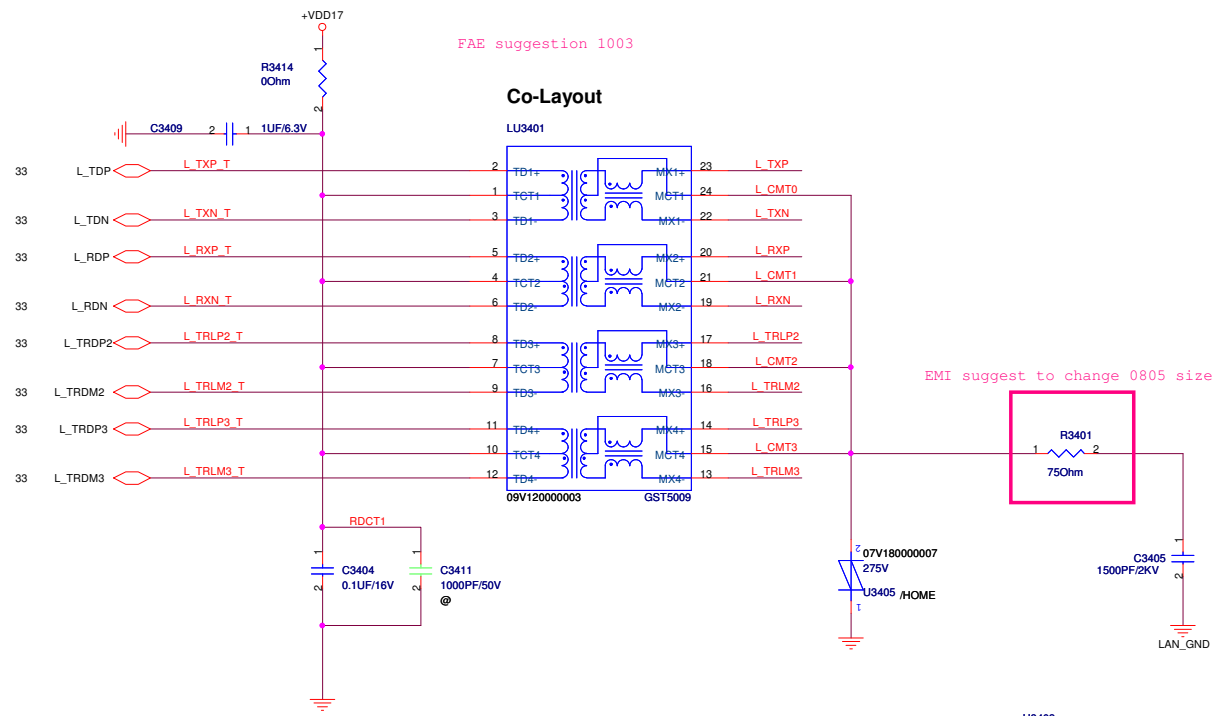
This customer directs part number 0200-002P000 ATR800/AR8151-BL1A-RL

11/30 Swap for LU3401/LU3402 co-lay (Elmer)

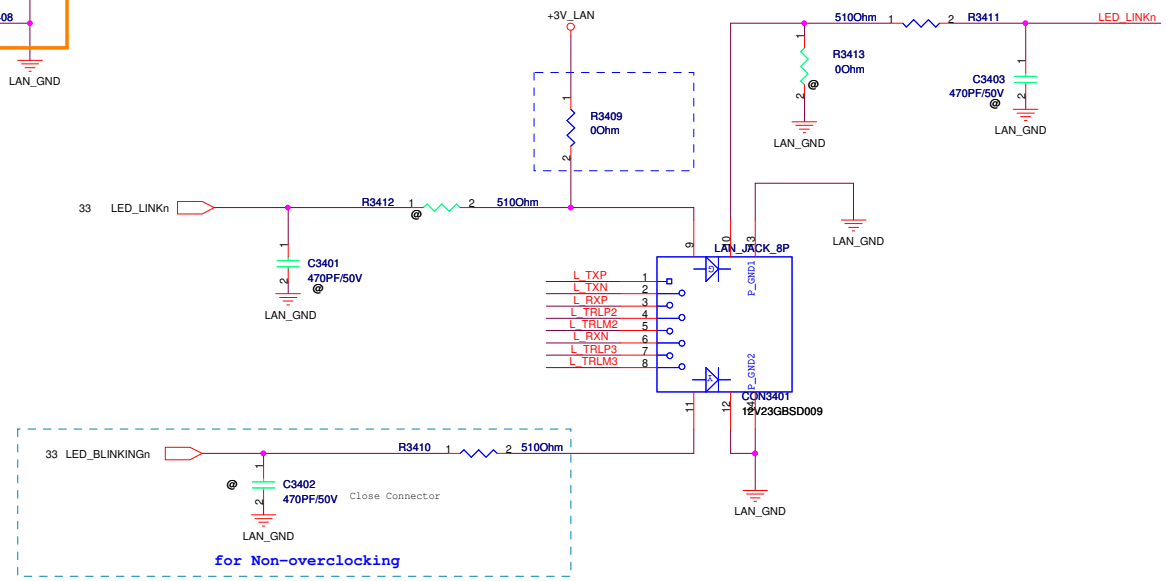
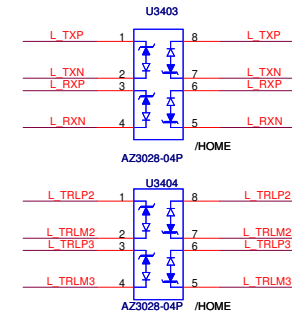


FAE suggestion 1003

Co-Layout



EMI suggest to change 0805 size 0921

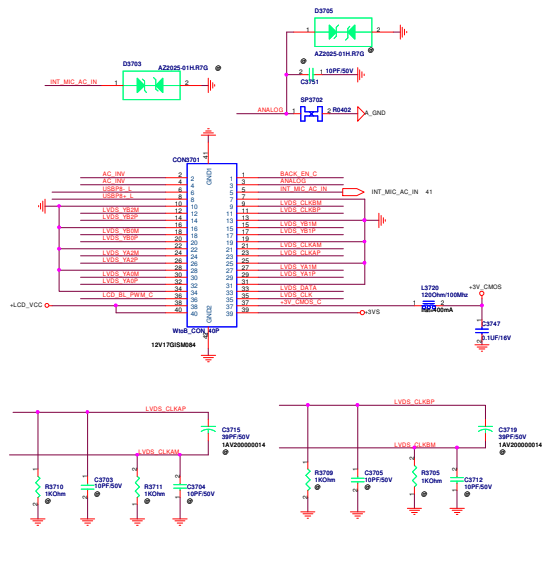
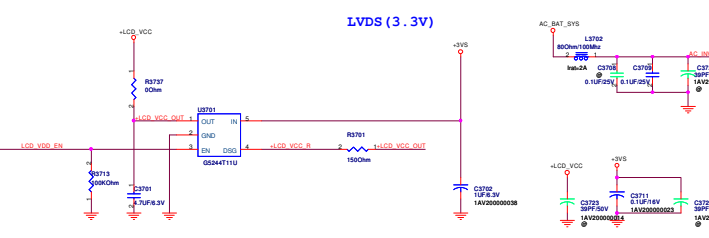


for Non-overclocking

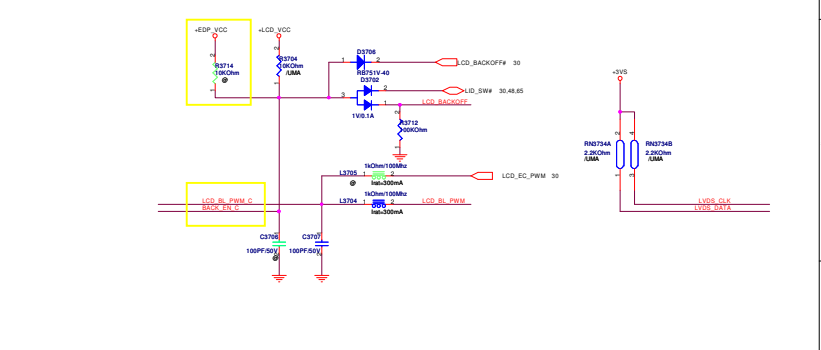
<Variant Name>

PEGATRON Title :RJ45/RJ11	
BG1-CSC-HW R&D Dept.5 Engineer: Ahren_chen	
Size	Project Name
Custom	PLFG
Date: Friday, February 03, 2012	Sheet 34 of 99

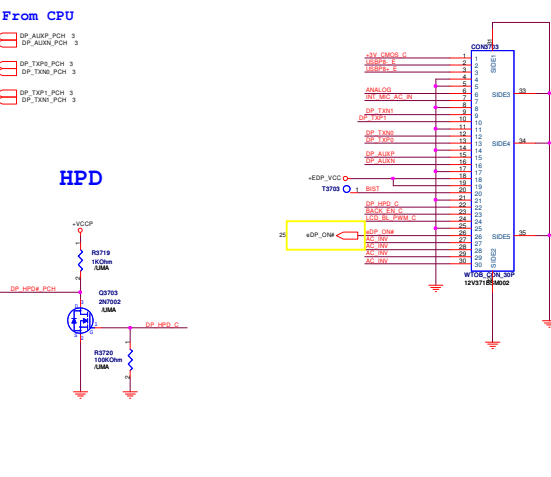
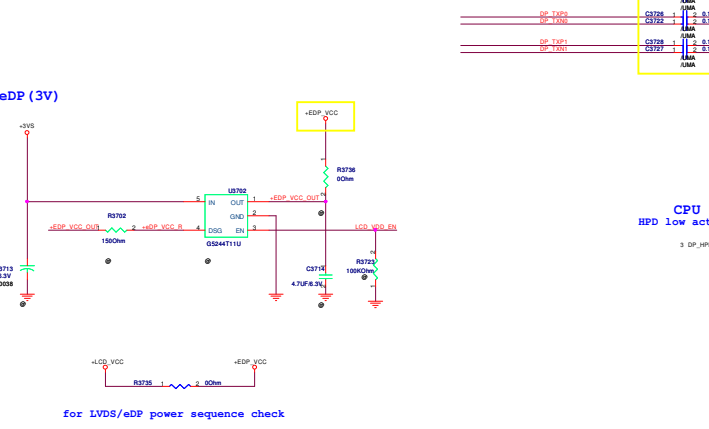
LVDS



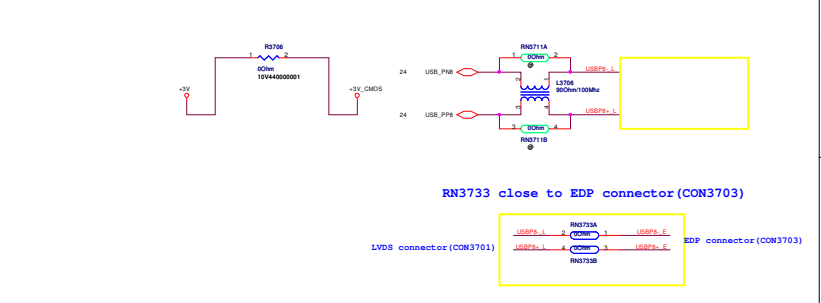
LVDS/eDP control signal



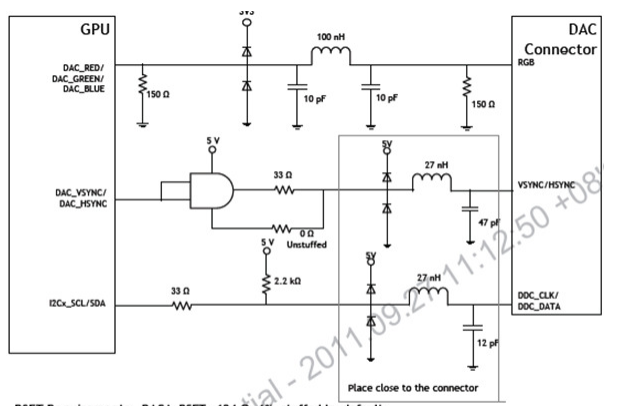
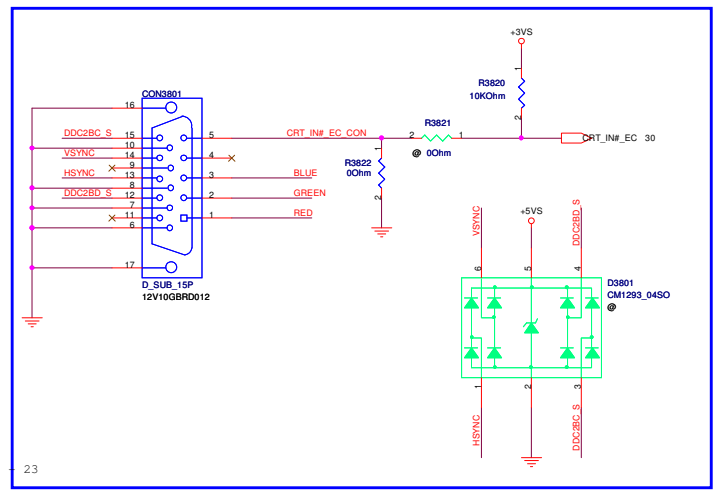
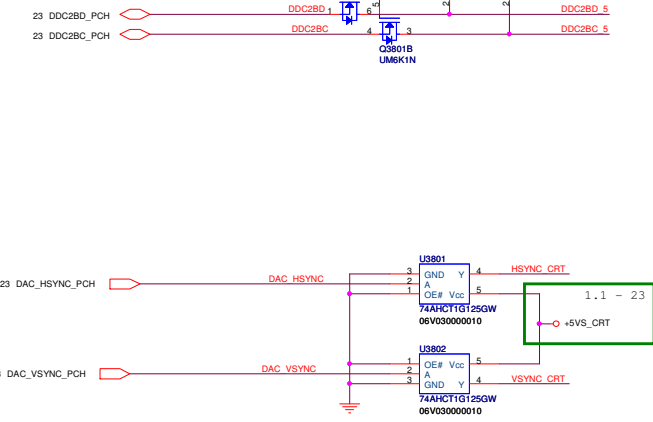
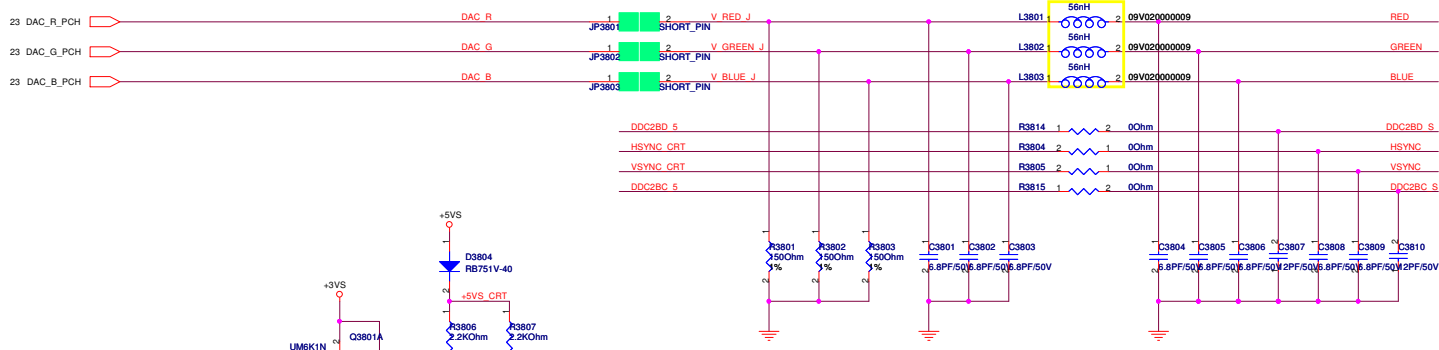
eDP



USB Camera



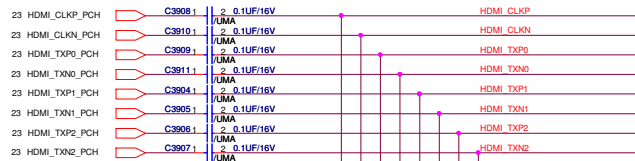
Check UMA and DSC inductor value



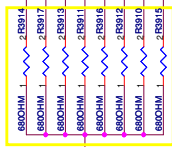
RSET Requirements: DACA_RSET= 124 Ω, 1%, stuffed by default.

Figure 71. GPU-DAC Connections

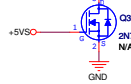
The LC filter circuit (NV DSC only)
 DDC:L=27nH, C=12PF
 HSYNC/VSYNC : L=27nH, C=47PF
 RGB:L=100nH, C=10PF



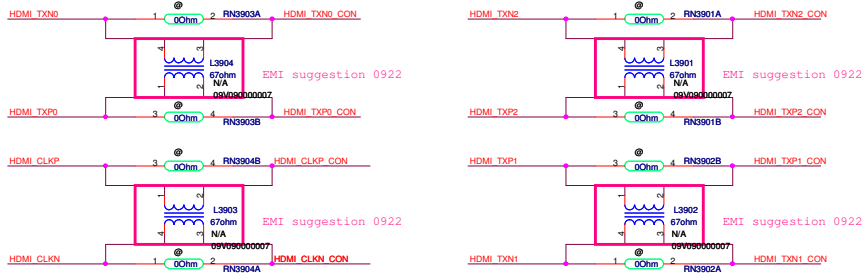
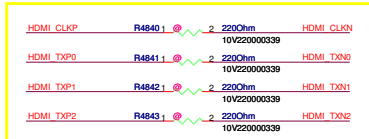
Close to connector and do T routing



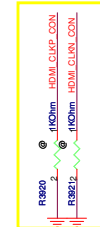
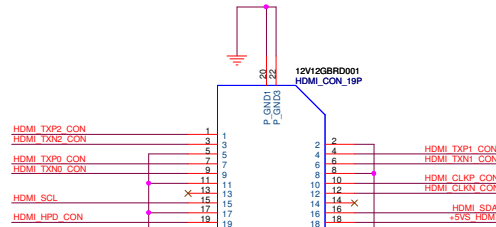
R3910, R3911, R3912, R3913, R3914, R3915, R3916, R3917
 Intel design guide : 680ohm /UMA
 NV reference schematics : 499ohm /DGPUO



EMI solution

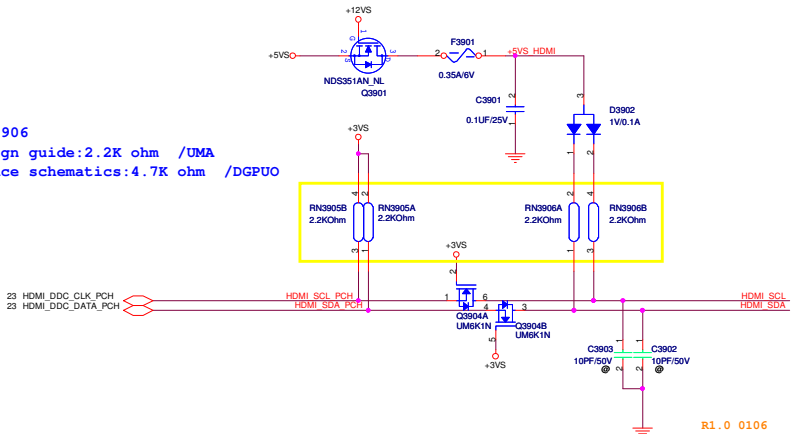


HDMI_SCL & HDMI_SDA : no via , trace length should be as short as possible

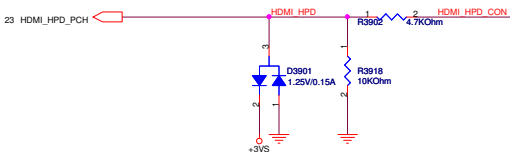


EMI solution

RN3905, RN3906
 Intel design guide: 2.2K ohm /UMA
 NV reference schematics: 4.7K ohm /DGPUO



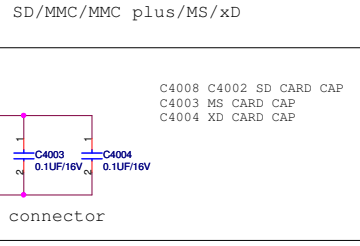
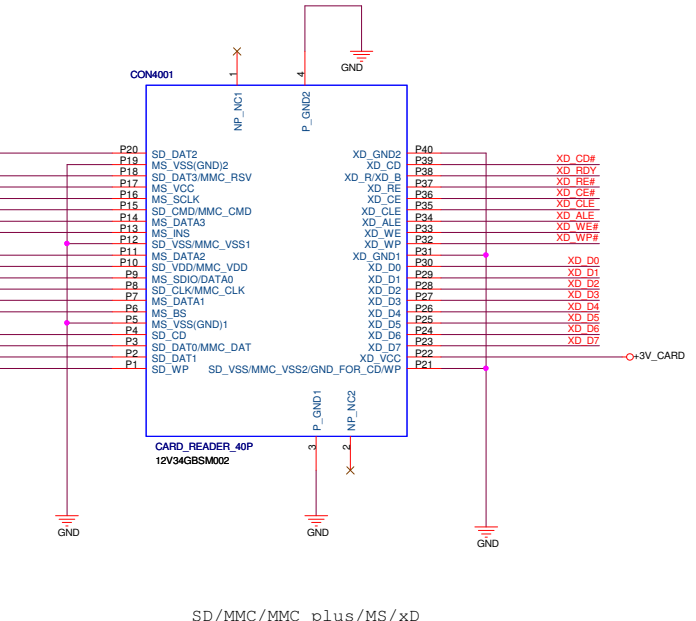
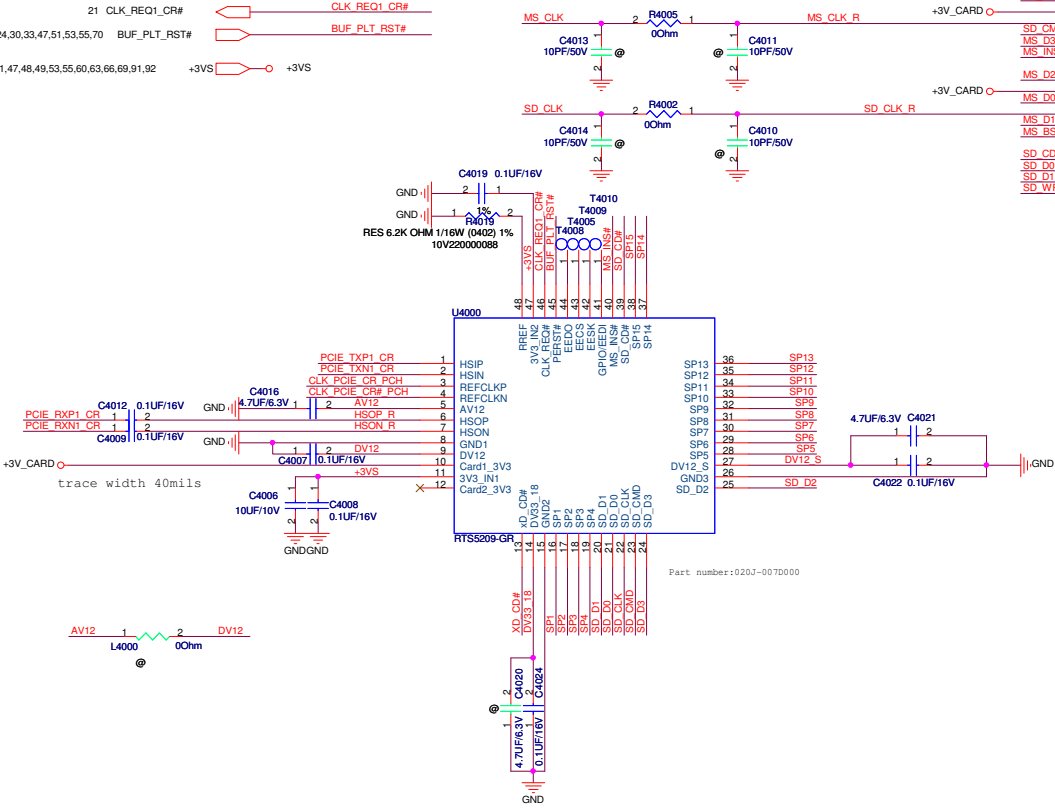
R1.0 0106
 HDMI HPD Cost Reduced Level Shifter Design Recommendation



From System's PCIe interface

- 21 PCIe_TXP1_CR PCIe_TXP1_CR
- 21 PCIe_TXN1_CR PCIe_TXN1_CR
- 21 PCIe_RXP1_CR PCIe_RXP1_CR
- 21 PCIe_RXN1_CR PCIe_RXN1_CR
- 21 CLK_PCIE_CR_PCH CLK_PCIE_CR_PCH
- 21 CLK_PCIE_CR#_PCH CLK_PCIE_CR#_PCH
- 21 CLK_REQ1_CR# CLK_REQ1_CR#
- 24,30,33,47,51,53,55,70 BUF_PLT_RST# BUF_PLT_RST#

+3VS +3VS



Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

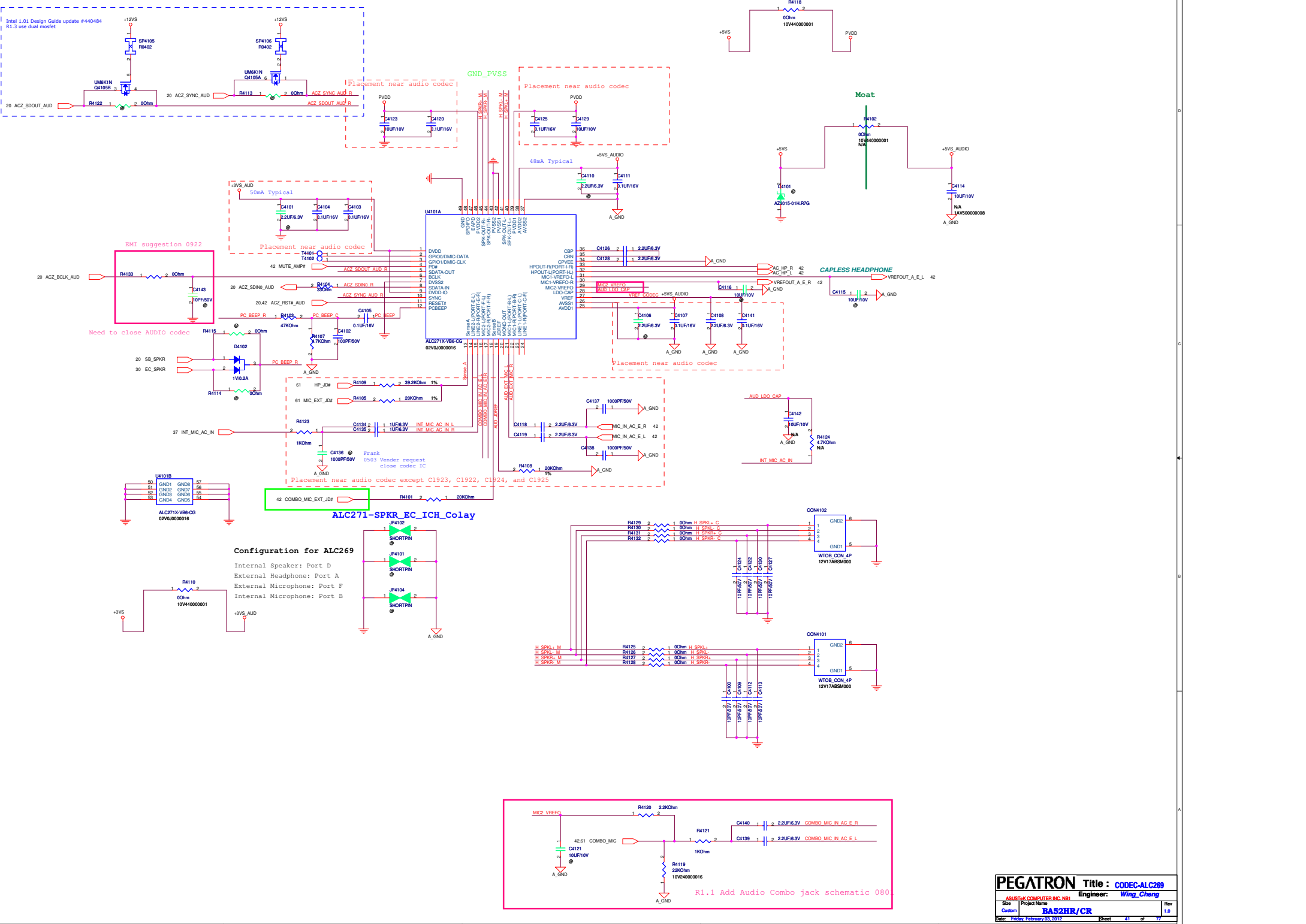
SP1	SD_D7	XD_RDY
SP2	SD_D6	XD_RE#
SP3	SD_D5	XD_CE#
SP4	SD_D4	XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15	SD_WP	XD_D7

Remove Serial Flash

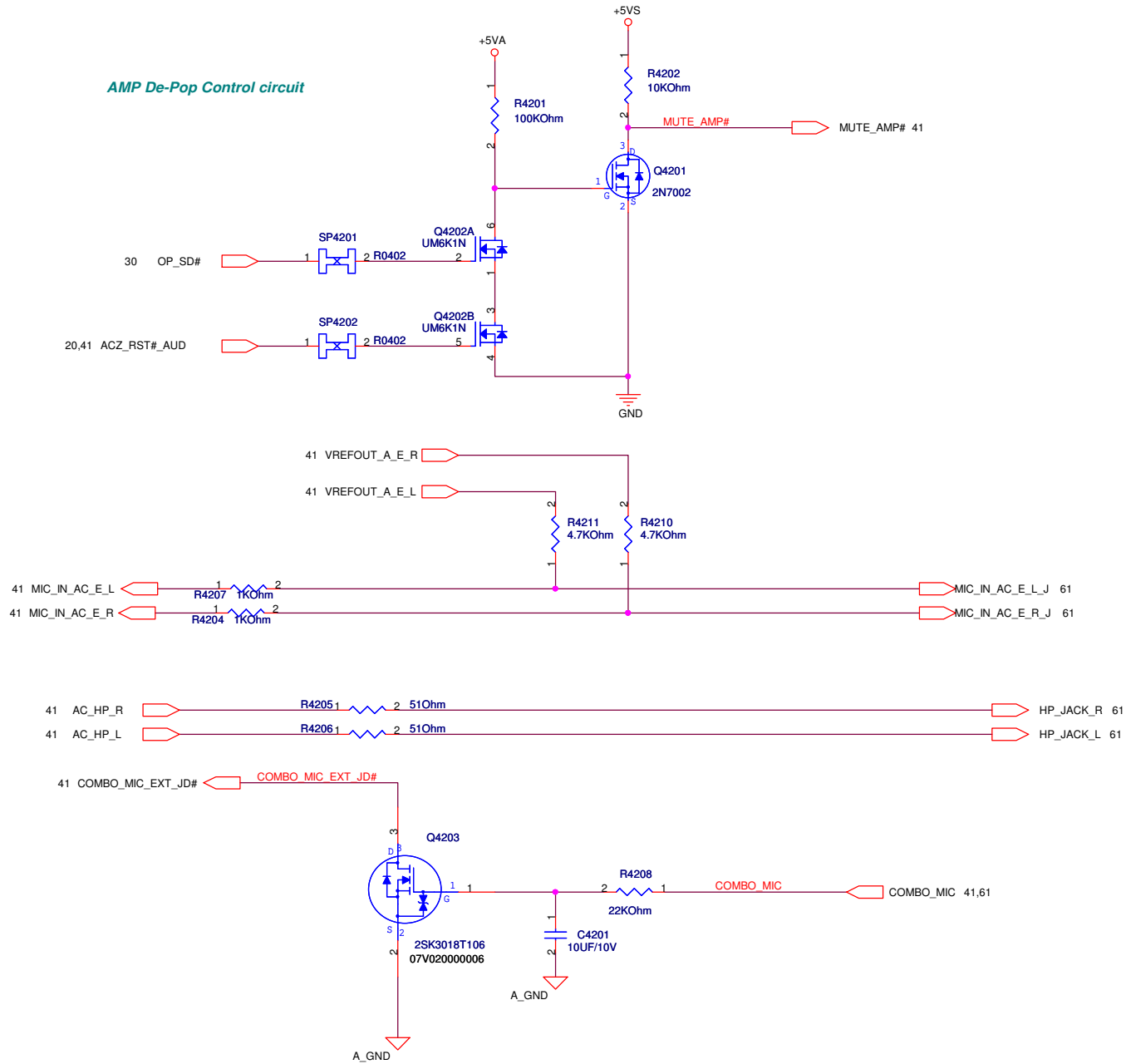
Reserve for BIOS boot function

When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

Share Pin



AMP De-Pop Control circuit



PEGATRON Title :AUDIO ALC269		Rev
BU1-RD Div.1-HW RD Dept.1		1.0
Engineer: Wing Cheng		
Size	Project Name	
B	BA52HR/CR	
Date: Friday, February 03, 2012	Sheet 42 of 77	

PEGATRON		Title : MDC CONN	
BG1-HW RD Dw:2-NB RD Dept.5		Engineer: <i>Wing Cheng</i>	
Size	Project Name	Rev	
C	BA52HR/CR	1.0	
Date: Friday, February 03, 2012		Sheet	43 of 77

5

4

3

2

1

D

D

C

C

B

B

A

A

Del Entry audio circuit

SR-8
0121-11

PEGATRON		Title : CODEC-ALC269	
ASUSTeK COMPUTER INC. NB1		Engineer: Wing_Cheng	
Size Custom	Project Name BA52HR/CR	Date: Friday, February 03, 2012	Rev 1.0
		Sheet	44 of 77

5

4

3

2

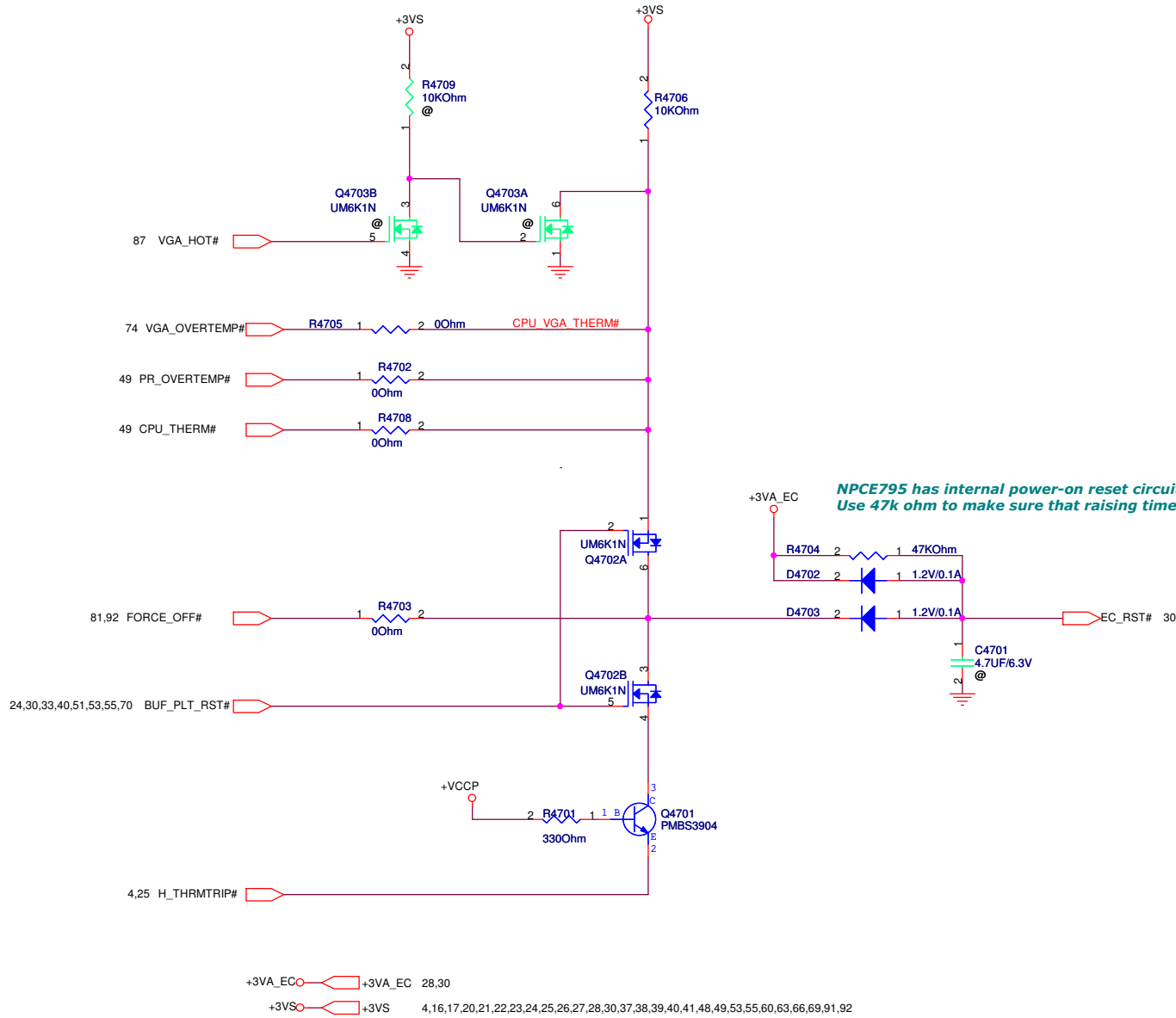
1

Del Entry audio circuit

SR-8
0121-11

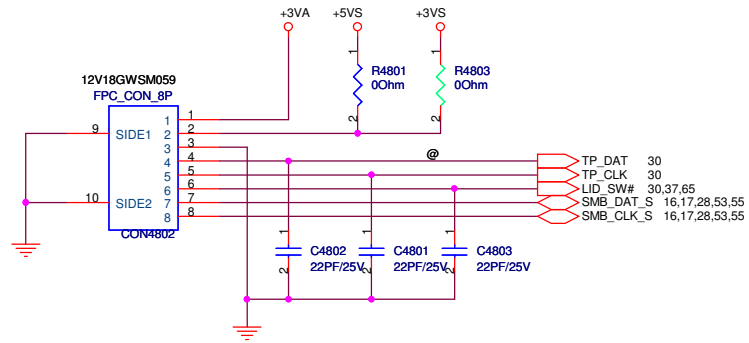
PEGATRON		Title : AUDIO ALC269	
BU1-RD Div.1-HW RD Dept.1		Engineer: Wing_Cheng	
Size Custom	Project Name BA52HR/CR	Date: Friday, February 03, 2012	Rev 1.0
Date: Friday, February 03, 2012		Sheet 45 of 77	

Thermal Policy

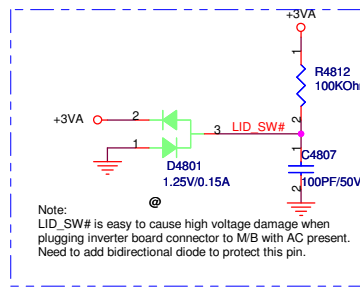


PEGATRON Title : RST_Reset Circuit		
BG1-HW RD Div.2-NB RD Dept.5		Engineer: Wing_Cheng
Size B	Project Name BA52HR/CR	Rev 1.0
Date: Friday, February 03, 2012		Sheet 47 of 77

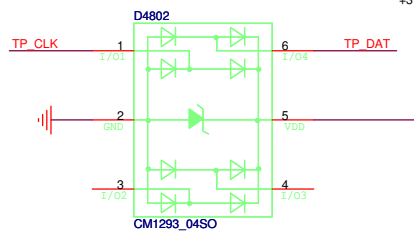
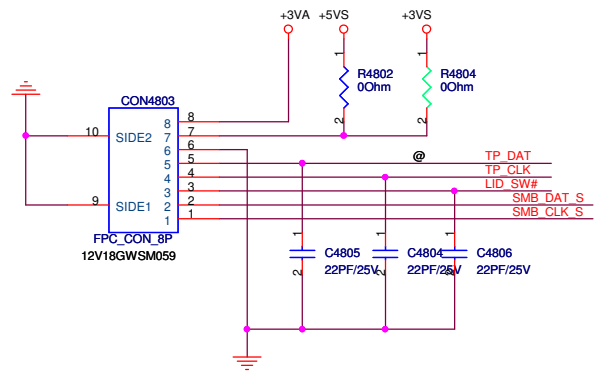
Touch Pad Button/ Hall Sensor



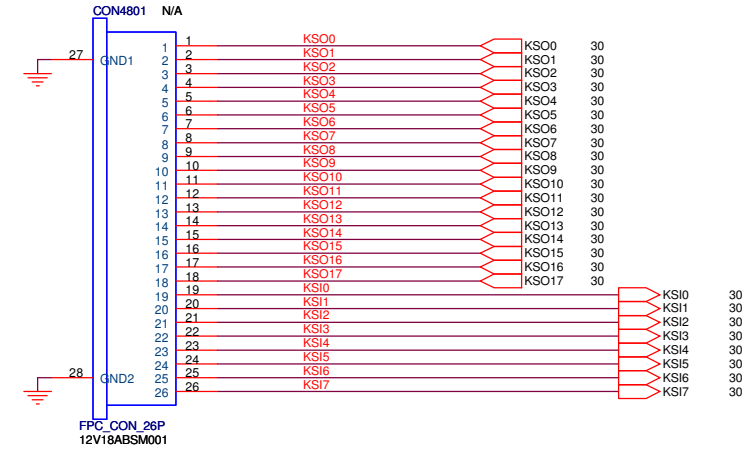
close to U4601



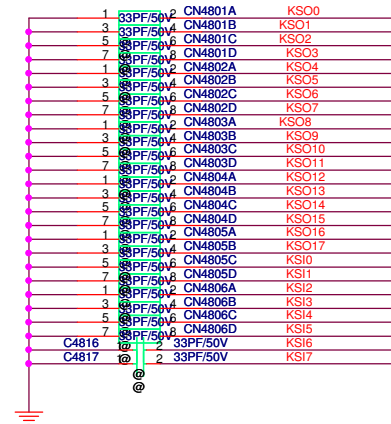
Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.



Keyboard



1218-00MW000



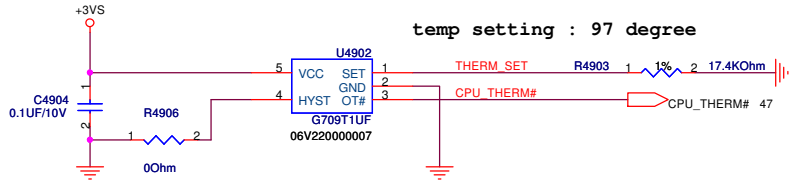
PEGATRON Title : KBI/TP/FLASH

BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng

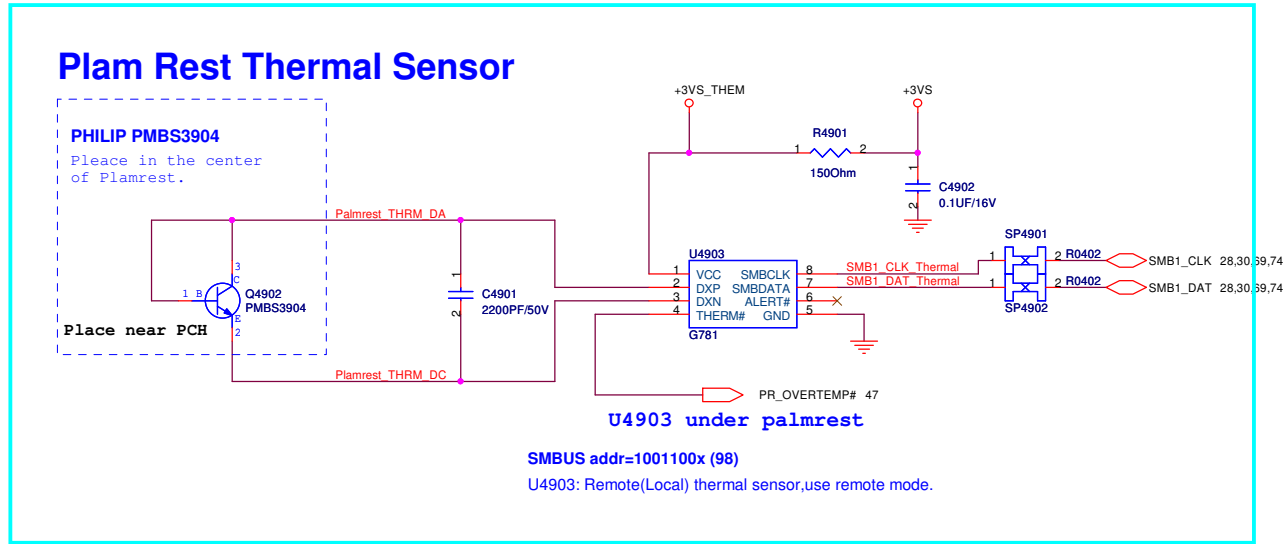
Size	Project Name	Rev
Custom	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 48 of 77

U5001 Close to CPU

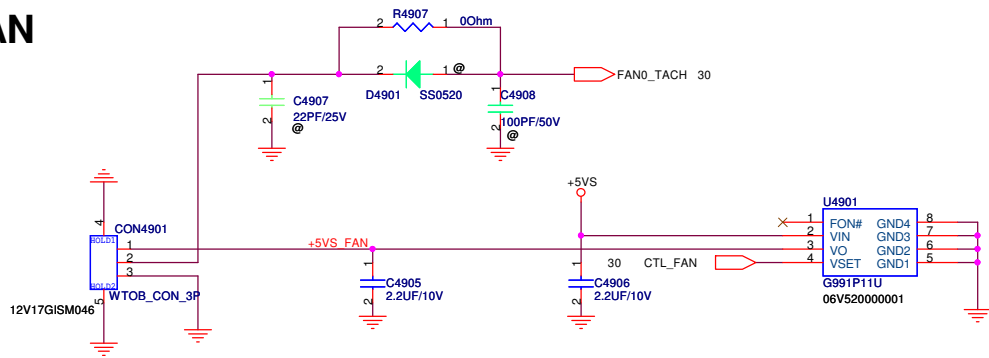


Plam Rest Thermal Sensor



R1.2-10

FAN



5

4

3

2

1

D

D

C

C

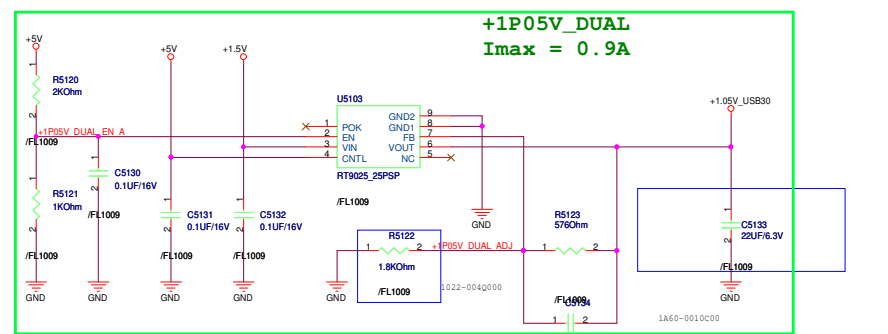
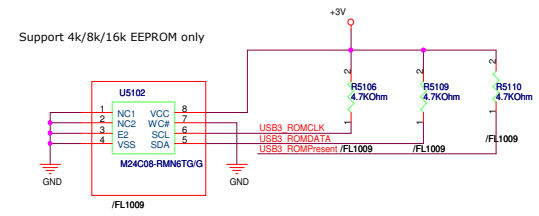
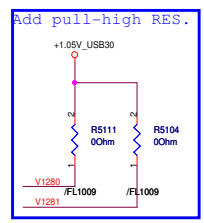
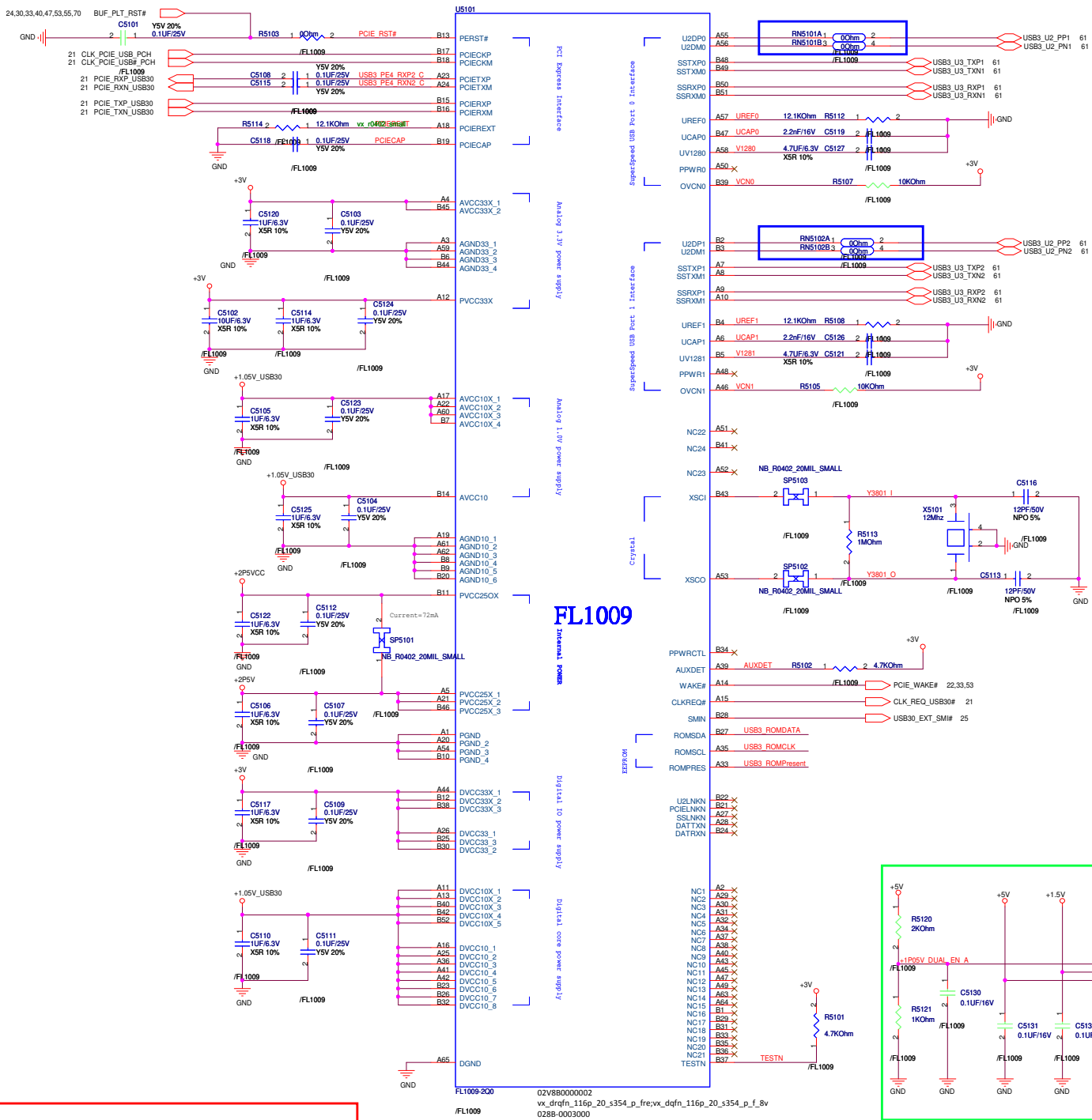
B

B

A

A

PEGATRON		Title : <i>Realtek_RT55138</i>	
<small>BG1-HW RD Dw:2-NB RD Dept.5</small>		Engineer: <i>Wing_Cheng</i>	
<small>Size</small>	<small>Project Name</small>	<small>Rev</small>	
C	BA52HR/CR	1.0	
<small>Date: Friday, February 03, 2012</small>		<small>Sheet</small>	<small>50 of 77</small>



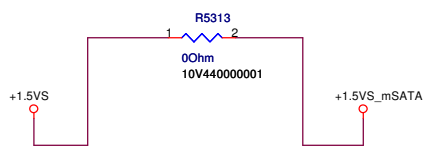
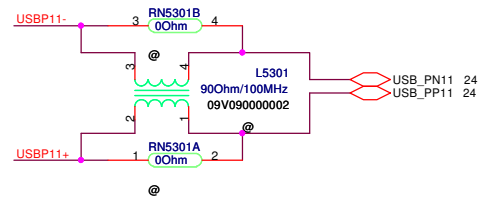
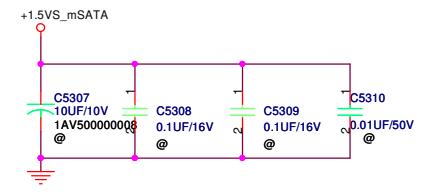
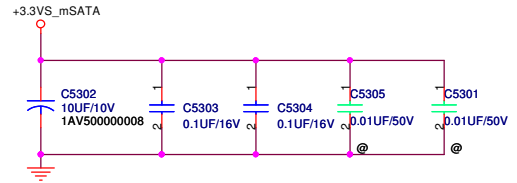
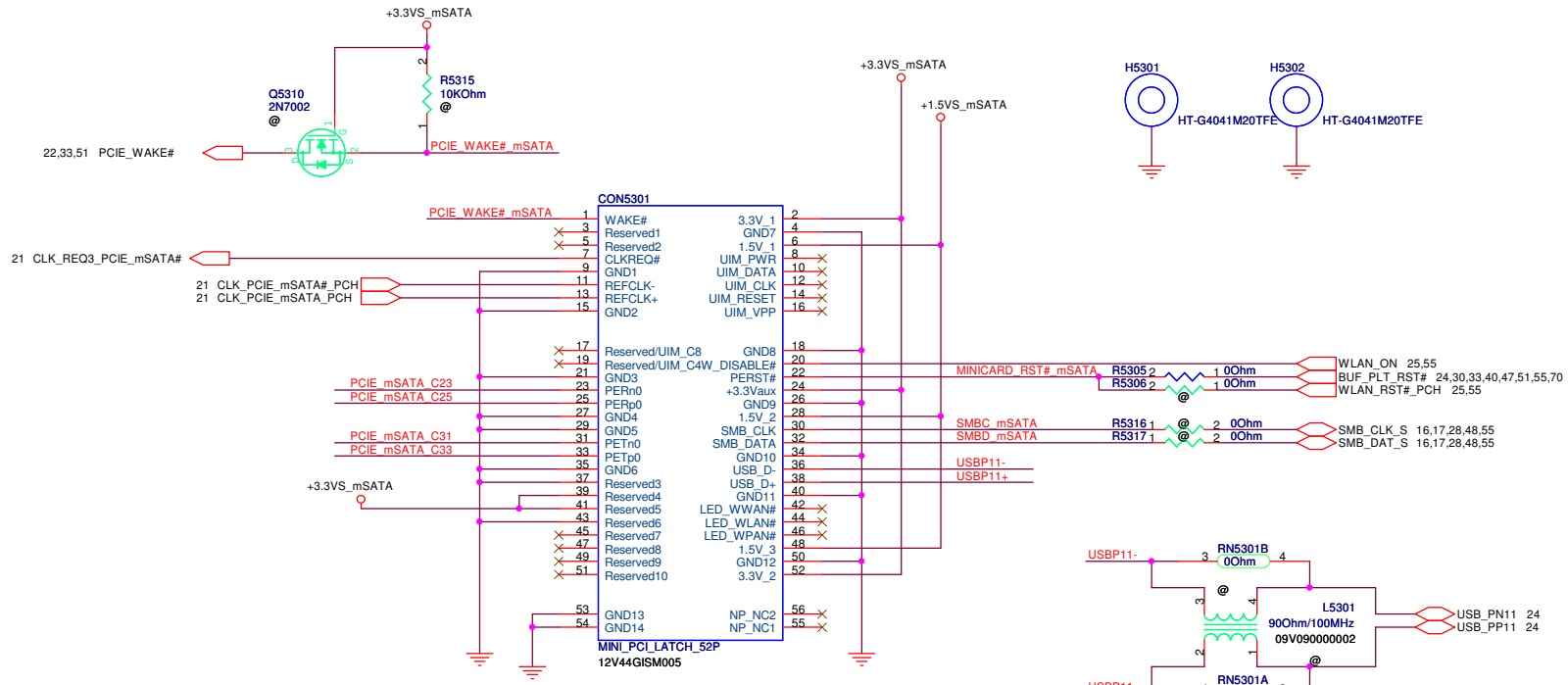
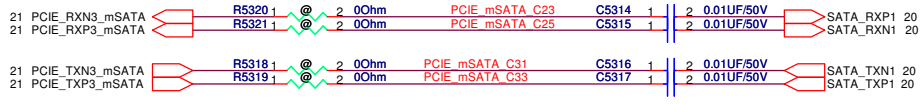
Follow Fresco SPEC, Change +3VSUS to +3V (1.05v must not be removed earlier than 3.3V supply removed.)



PEGATRON		Title : PCIE NEW CARD	
BU1-RD Div.1-HW RD Dept.1		Engineer: Wing_Cheng	
Size Custom	Project Name BA52HR/CR	Date: Friday, February 03, 2012	Rev 1.0
Date: Friday, February 03, 2012		Sheet 52 of 77	

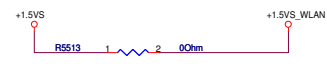
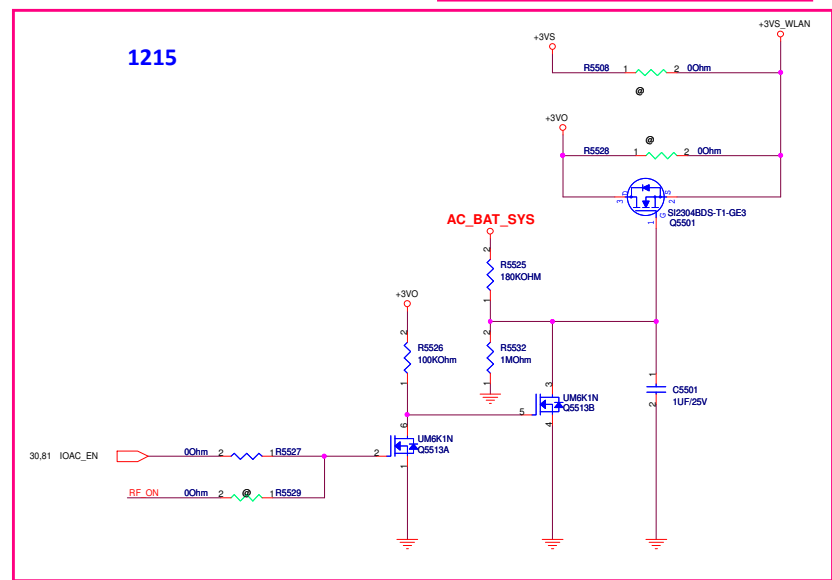
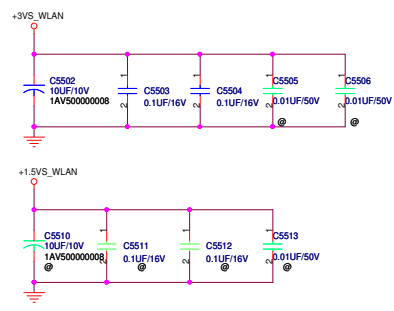
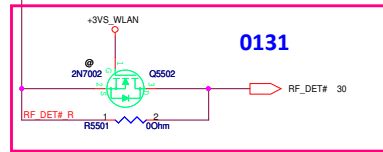
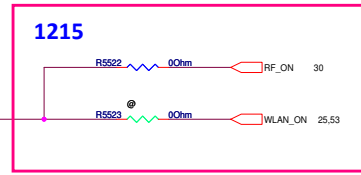
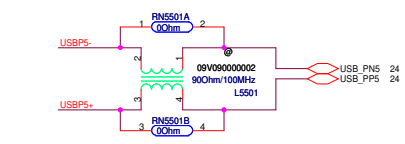
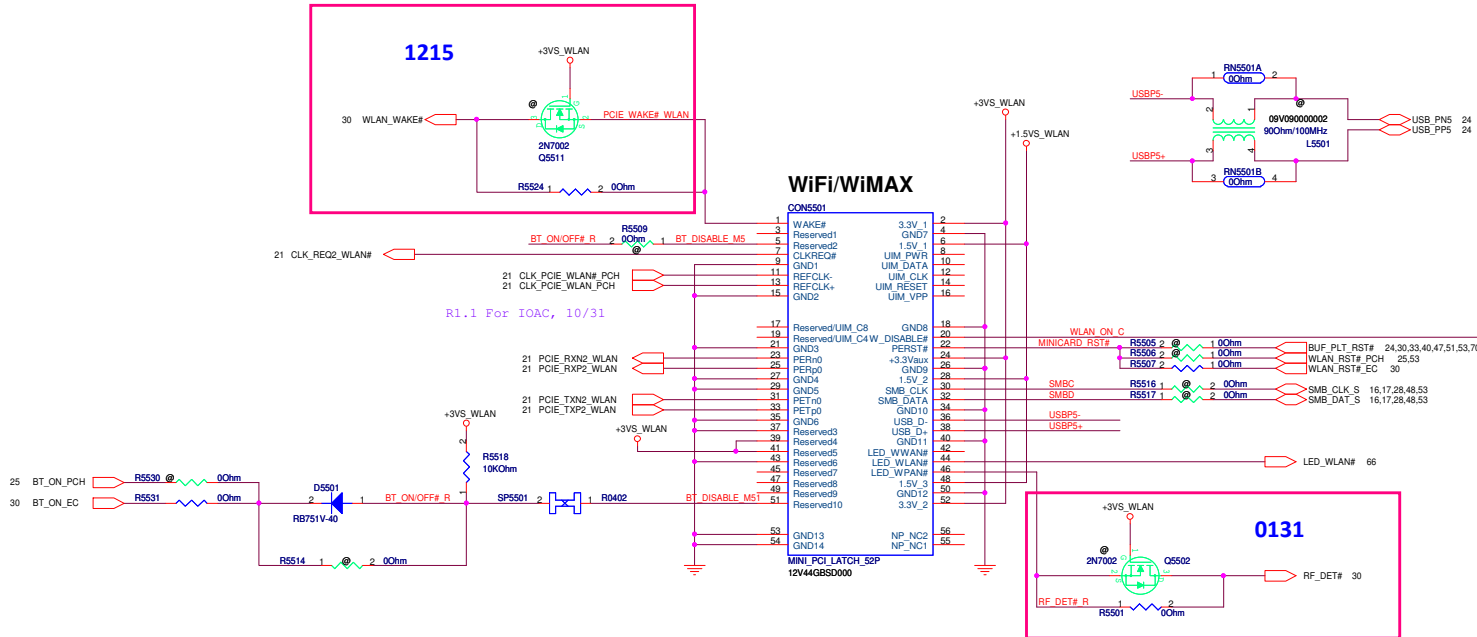
PCIE/mSATA

Select PCIE or mSATA IF select mSATA (only +3VAUX)

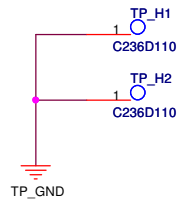




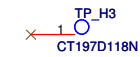
PEGATRON		Title : MINICARD (WUSB /UPCONVERT)	
BU1-RD Div.1+HW RD Dept.1		Engineer: Wing_Cheng	
Size Custom	Project Name BA52HR/CR	Rev 1.0	
Date: Friday, February 03, 2012		Sheet	54 of 77



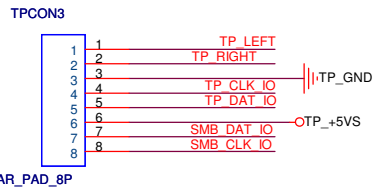
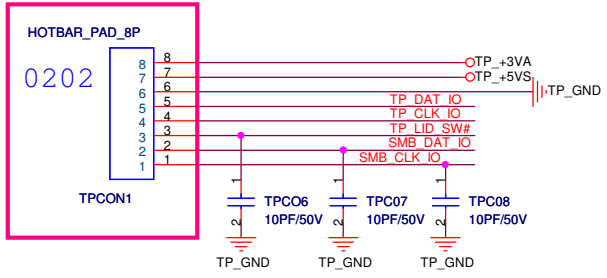
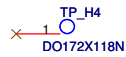
Screw M x 2



Fix Hole J x 1

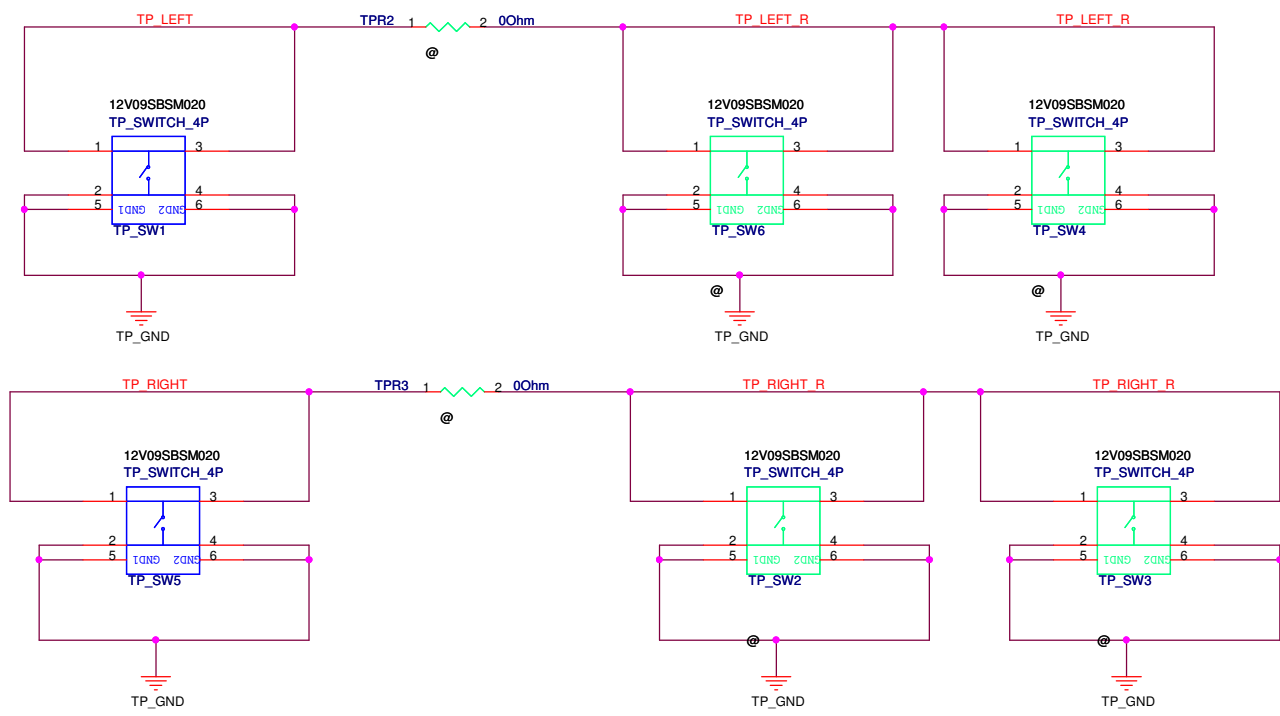
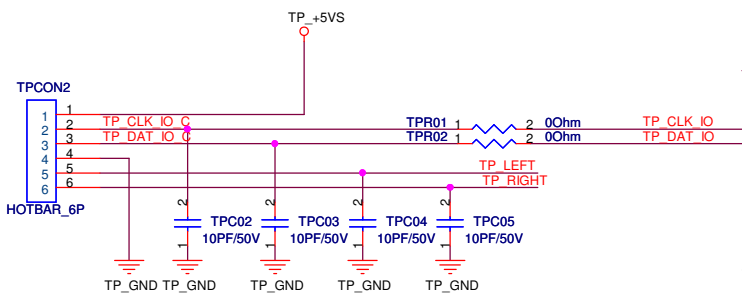


Fix Hole K x 1

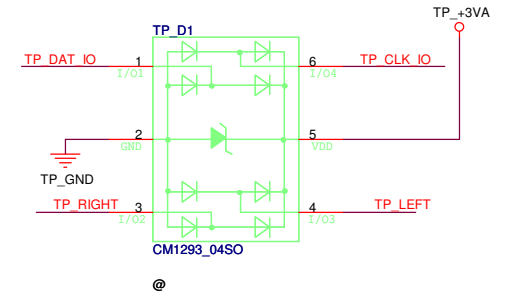
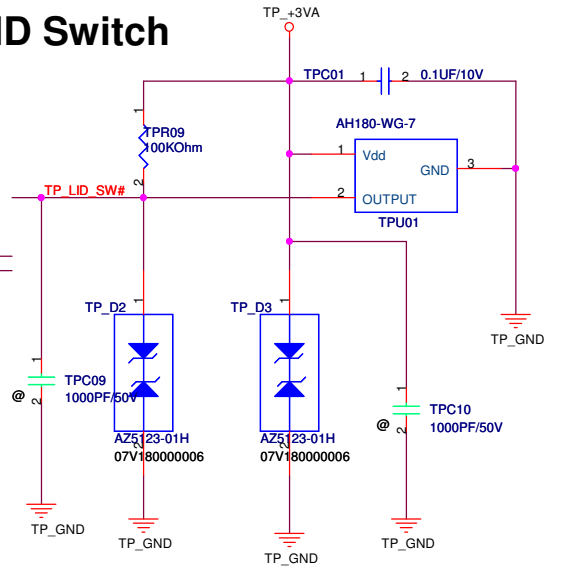


Touch Pad WIN8

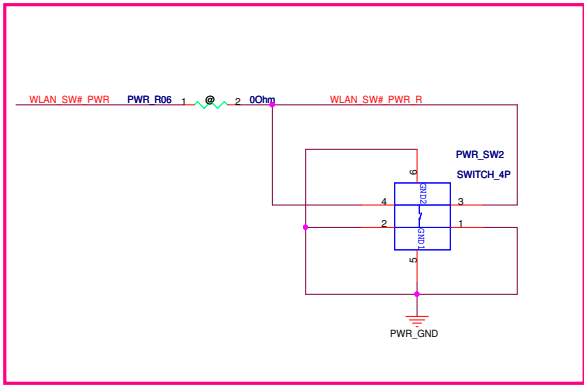
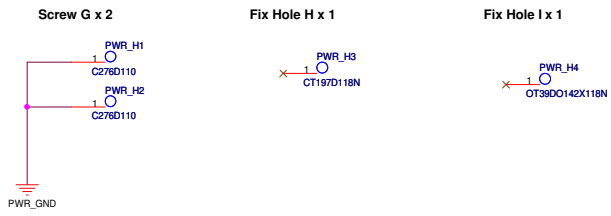
Touch Pad WIN7



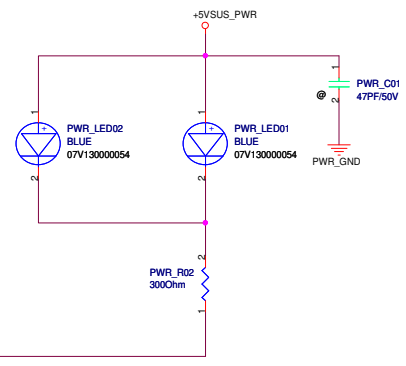
LID Switch



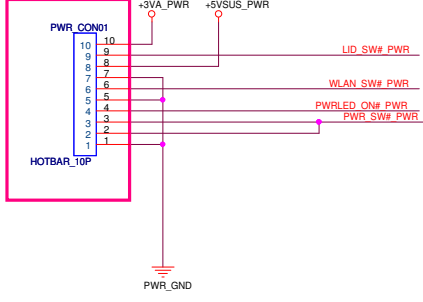
PEGATRON Title :TP_M		
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Wing_Cheng		
Size	Project Name	Rev
B	BA52HR/CR	1.0
Date: Friday, February 03, 2012	Sheet	56 of 77



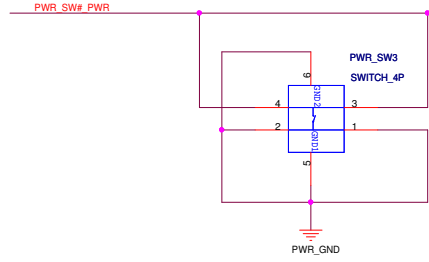
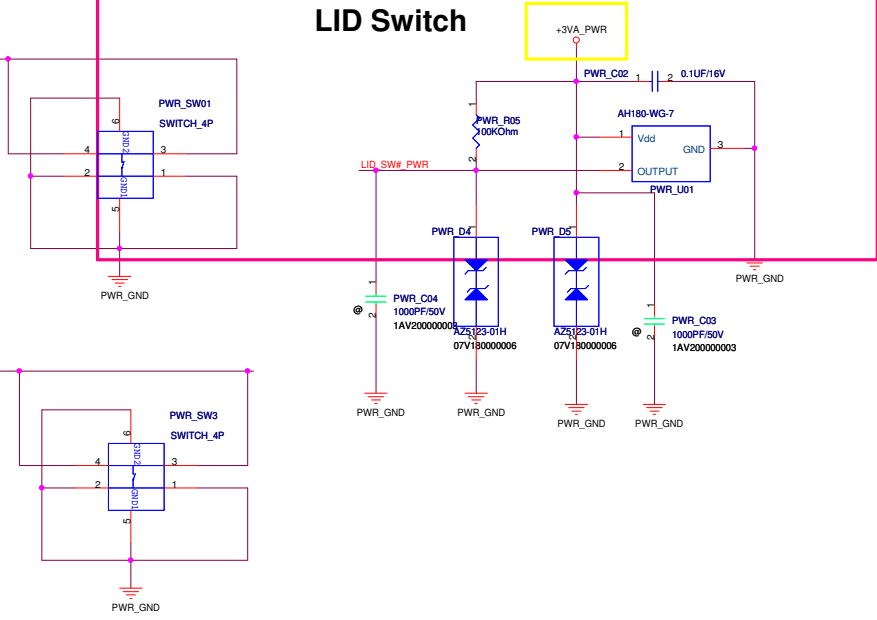
POWER Button LED

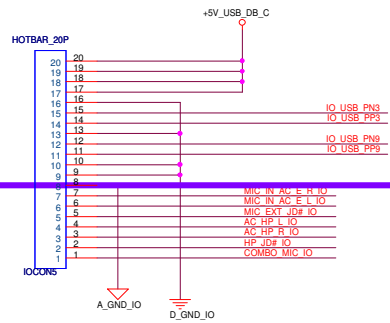


R1.1 reverse PWR_CON01 and change pin 1~4 pin define 1024



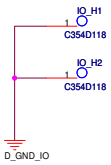
LID Switch





D_GND_IO Moat
A_GND_IO

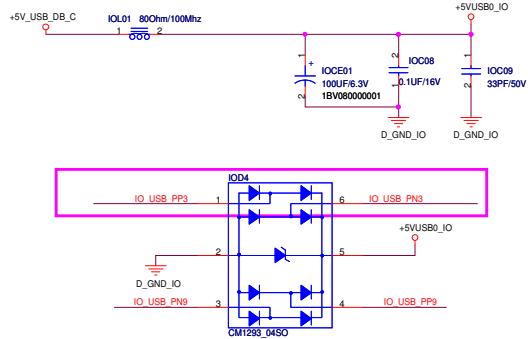
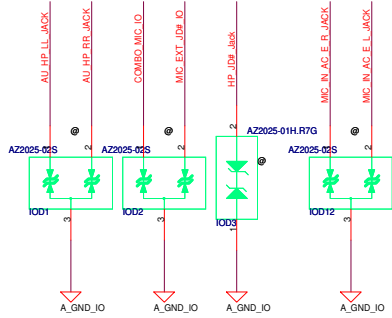
Screw L x 2



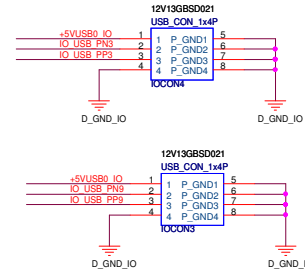
Fix Hole F x 1



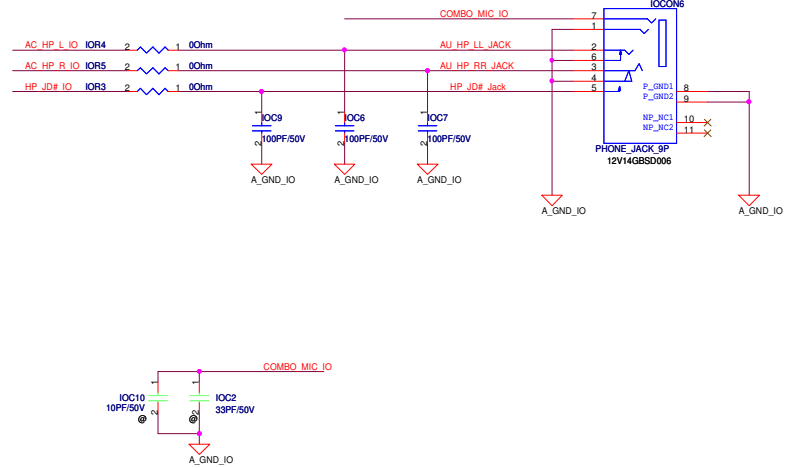
Fix Hole E x 1



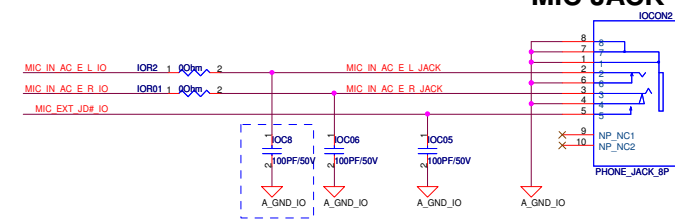
USB 2.0



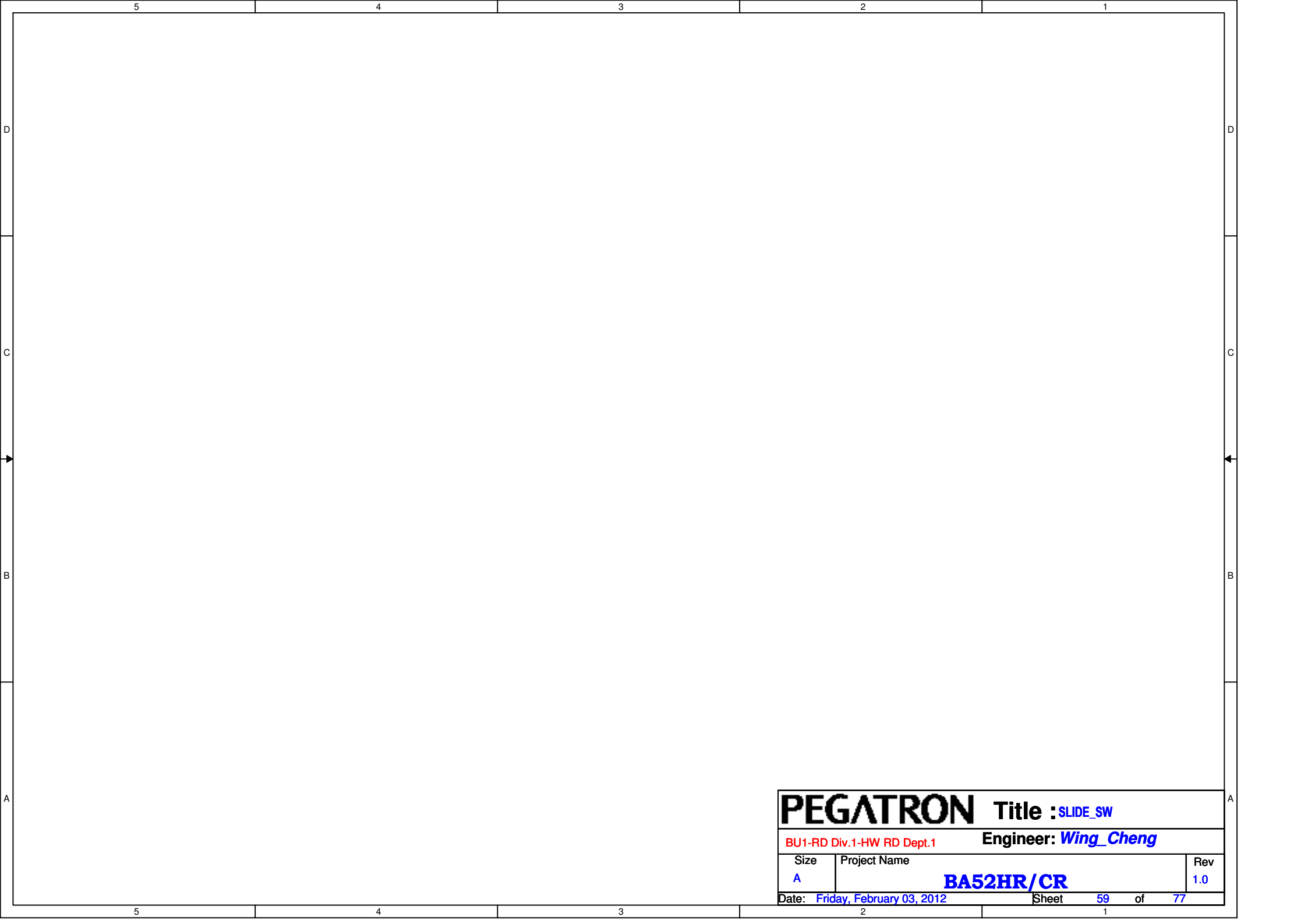
Headphone & MIC combo Jack



MIC JACK

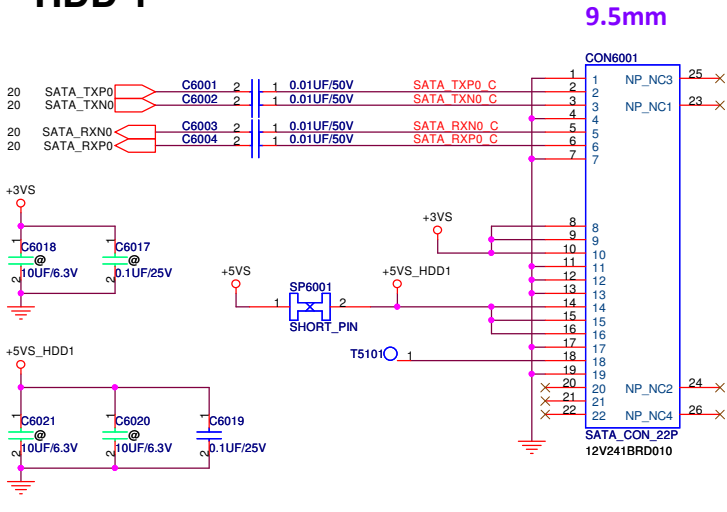


R1.1 Add 2nd MIC schematic 0804

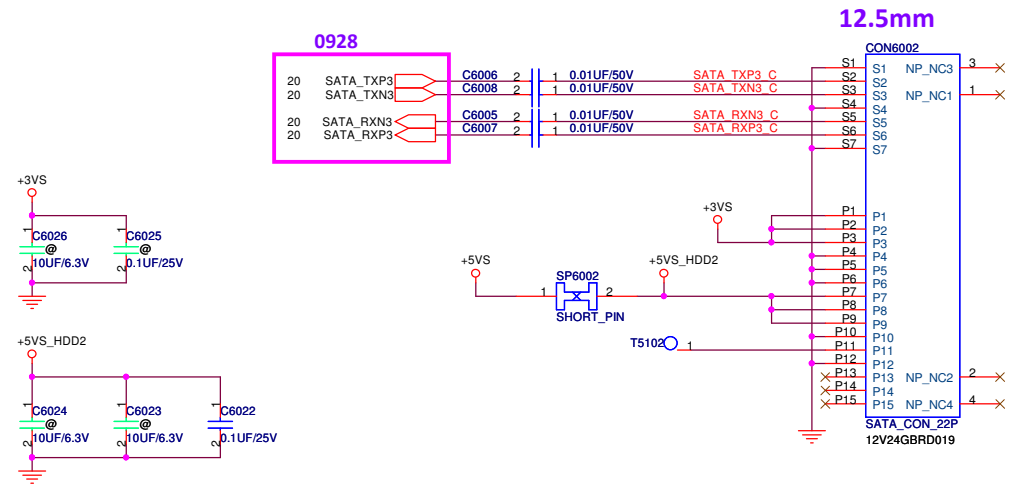


PEGATRON Title : SLIDE_SW		
BU1-RD Div.1-HW RD Dept.1		Engineer: Wing_Cheng
Size A	Project Name BA52HR/CR	Rev 1.0
Date: Friday, February 03, 2012		Sheet 59 of 77

HDD 1

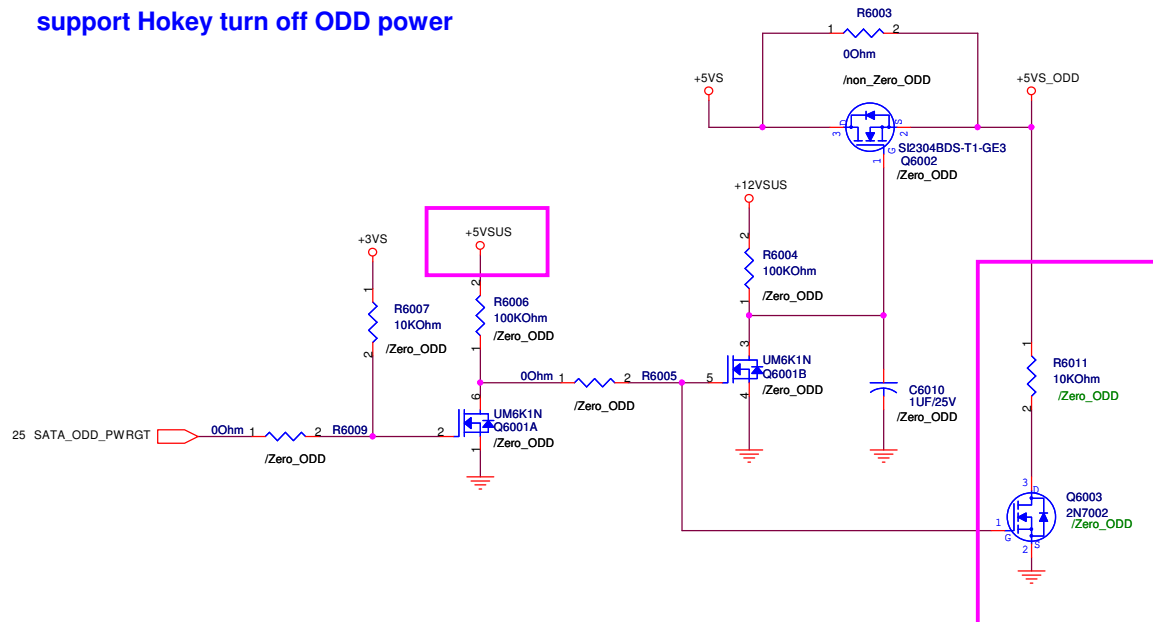
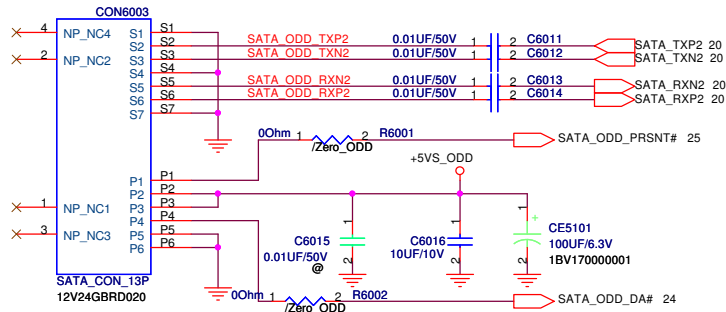


HDD 2



ODD

ZERO POWER ODD SUPPORT support Hokey turn off ODD power



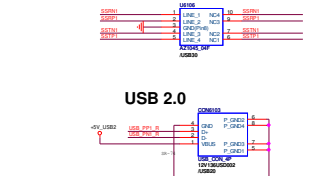
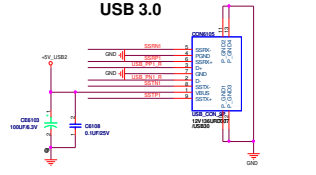
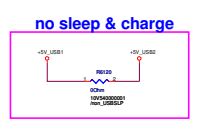
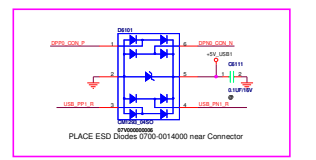
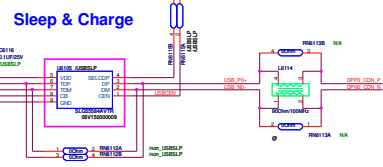
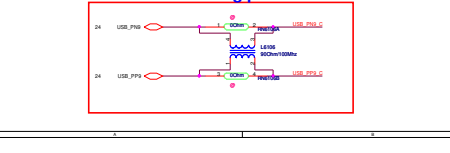
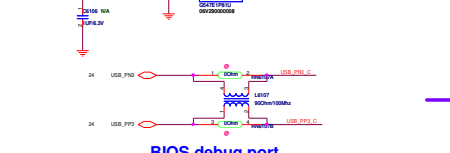
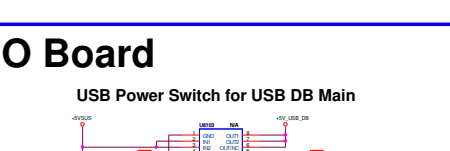
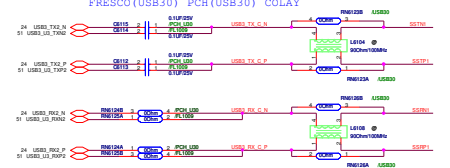
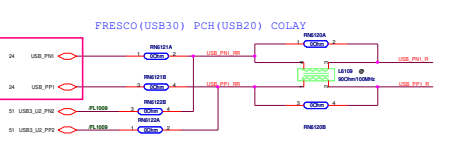
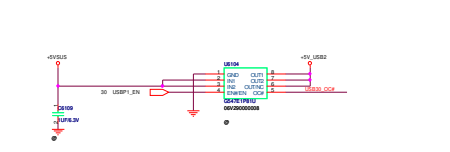
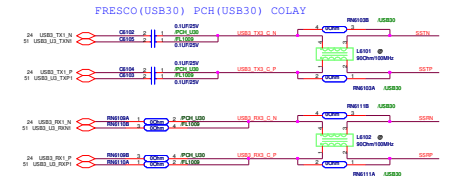
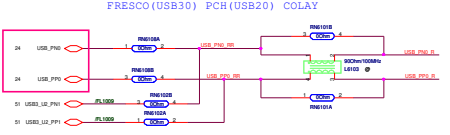
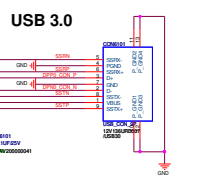
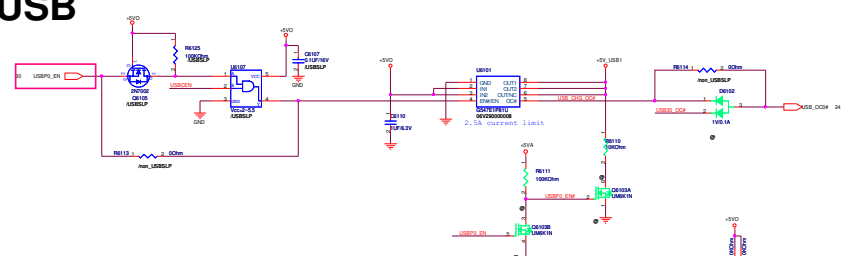
PEGATRON Title : SATA HDD/ ODD

BU1-RD Div.1-HW RD Dept.1 Engineer: *Wing_Cheng*

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

Date: Friday, February 03, 2012 Sheet 60 of 77

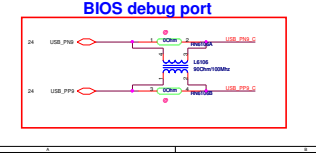
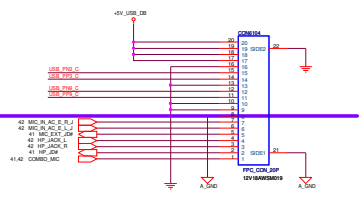
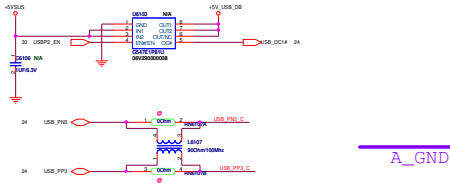
MB USB

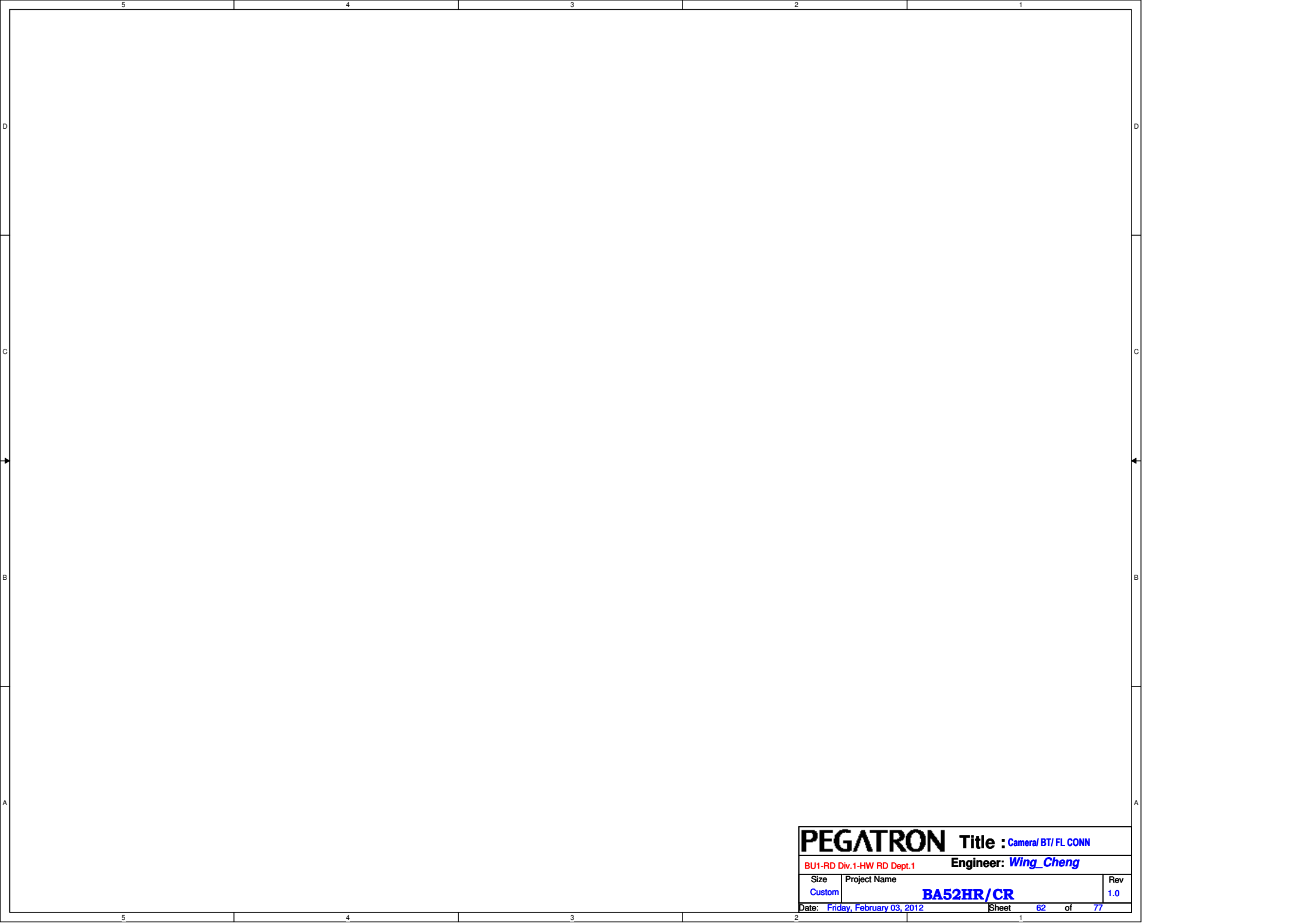


IO Board

AUDIO BOARD/w USB2.0 x2

USB Power Switch for USB DB Main



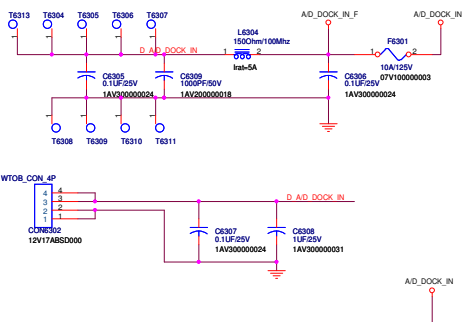


PEGATRON Title : Camera/ BT/ FL CONN

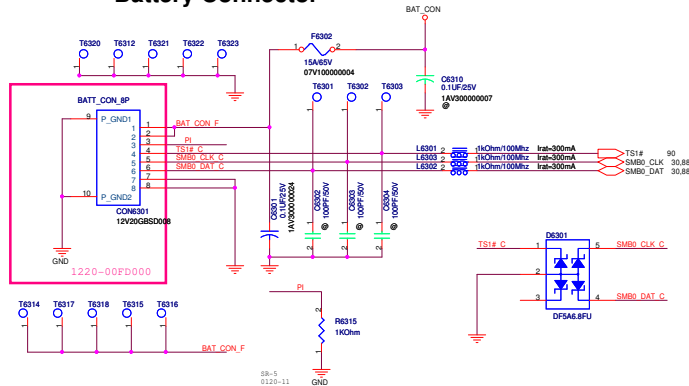
BU1-RD Div.1-HW RD Dept.1 Engineer: *Wing_Cheng*

Size	Project Name	Rev
Custom	BA52HR/CR	1.0

DC IN

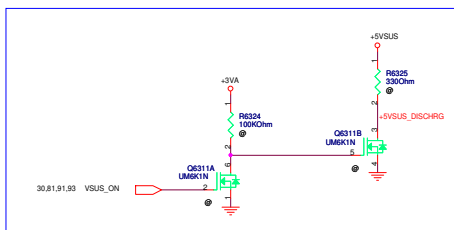
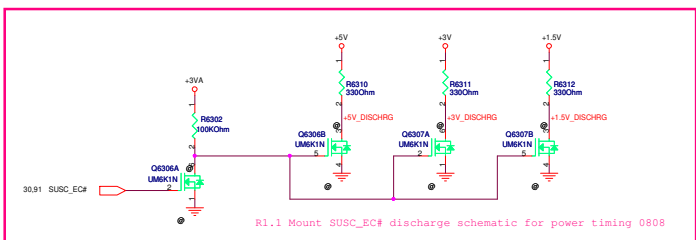
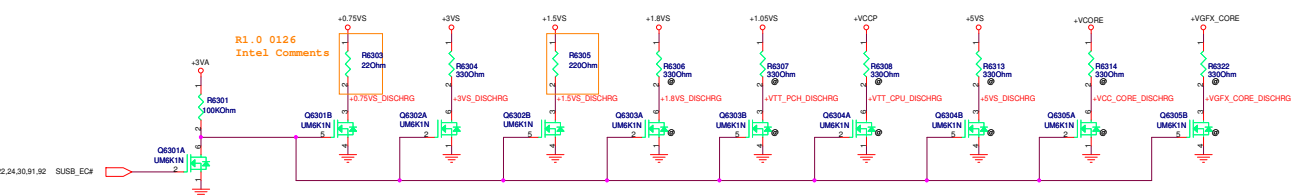


Battery Connector

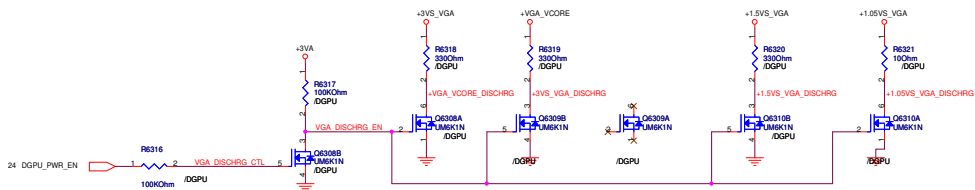


Discharge Circuit

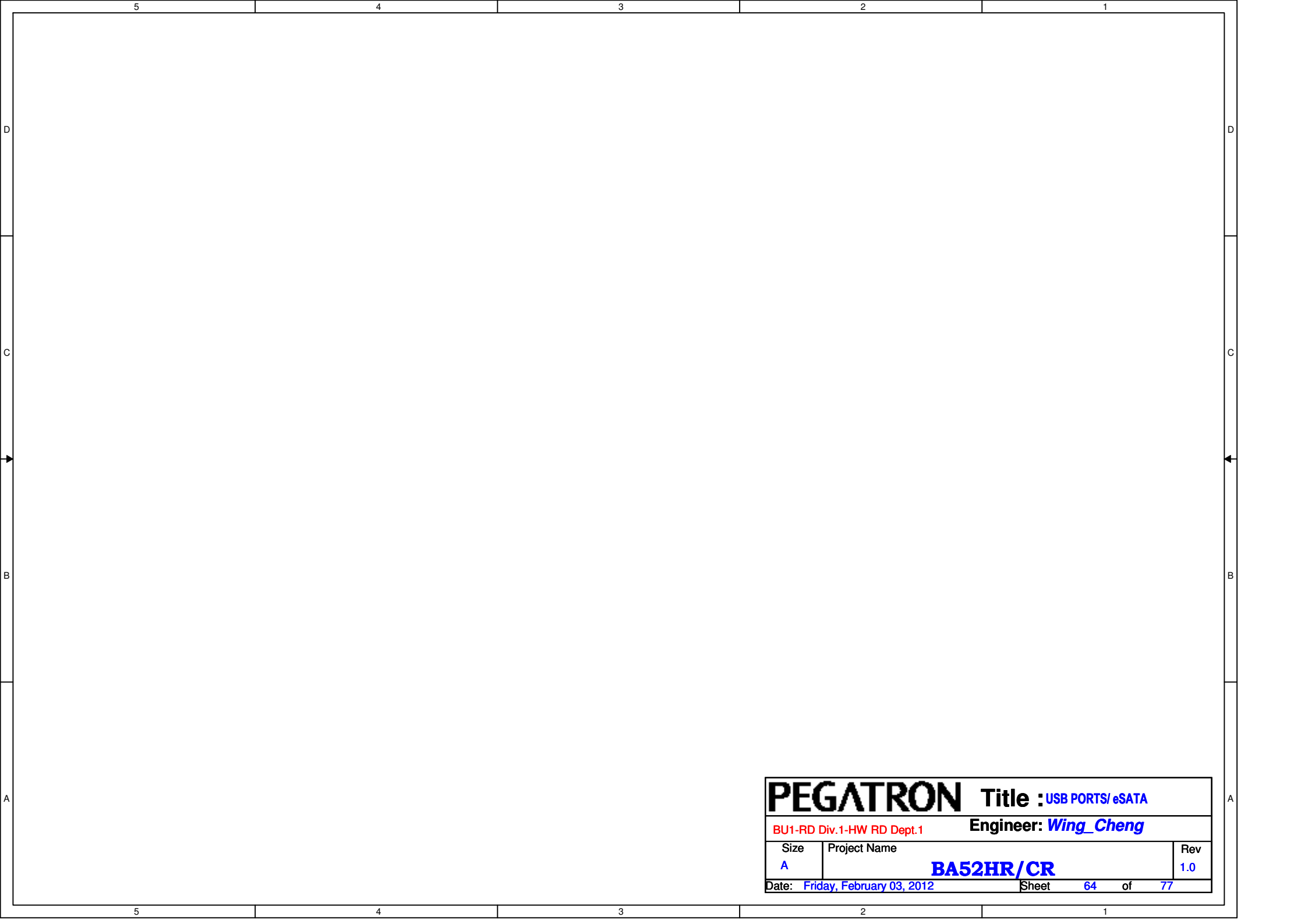
Frank 0505 Follow EVEREST



VGA Discharge Circuit

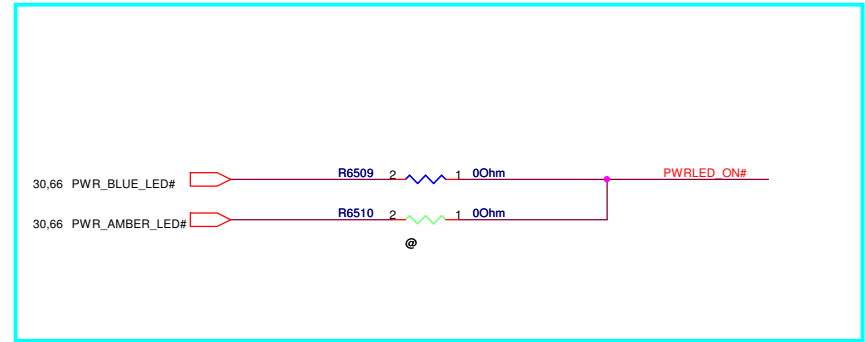
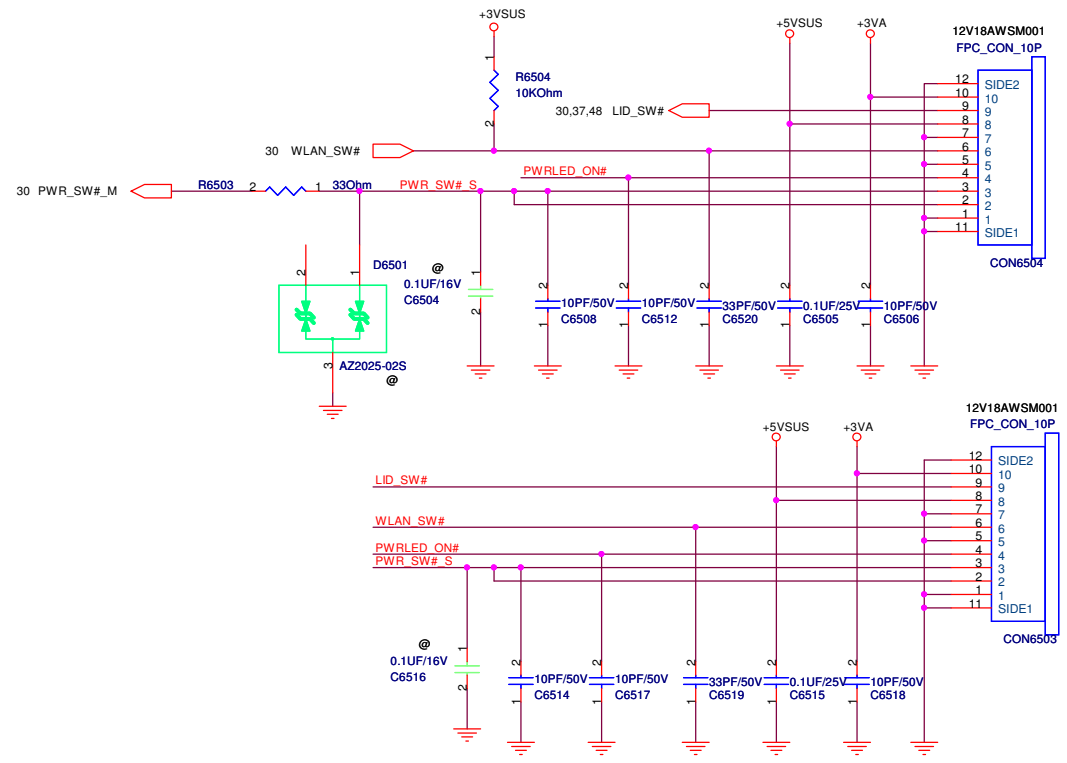


Unmount +VGA_Vcore discharg



PEGATRON			Title : USB PORTS/ eSATA		
BU1-RD Div.1-HW RD Dept.1			Engineer: Wing Cheng		
Size	Project Name			Rev	
A	BA52HR/CR			1.0	
Date: Friday, February 03, 2012			Sheet 64 of 77		

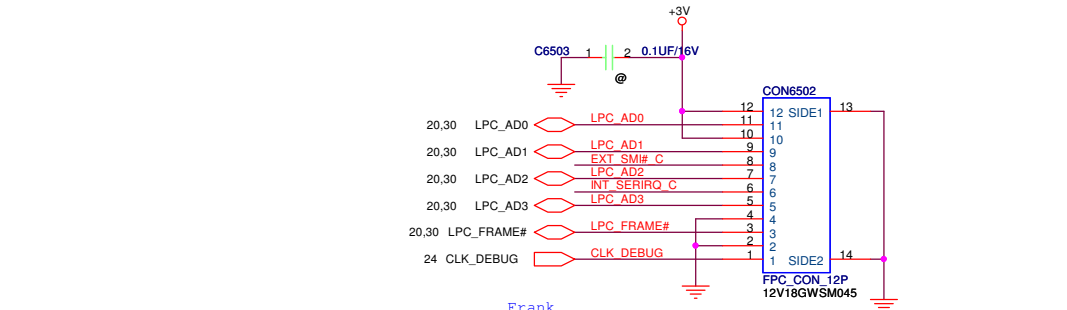
PWR BRD/ AMBIENT/ HALL CONN.



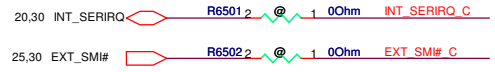
R1.2-28

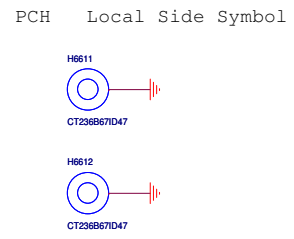
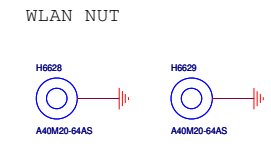
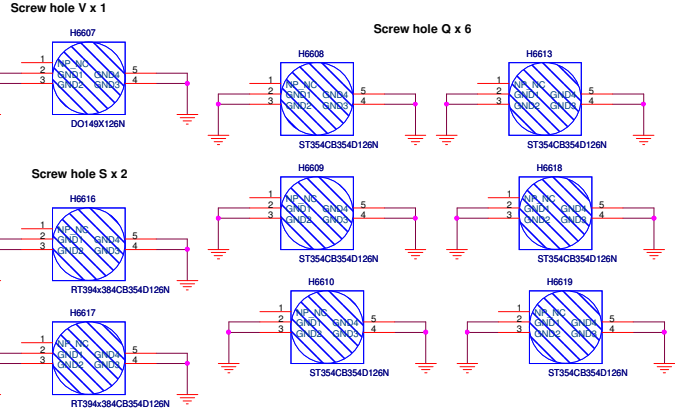
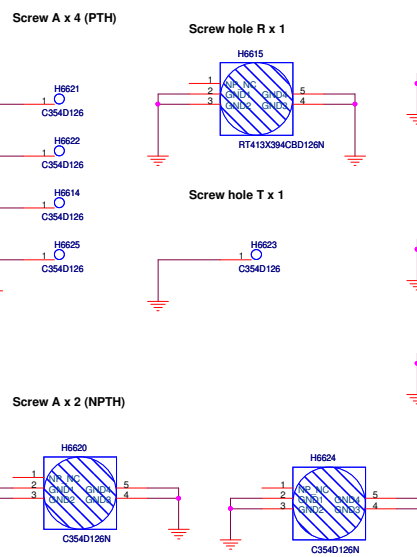
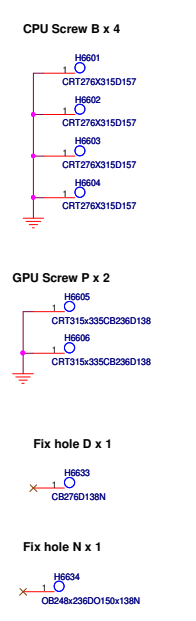
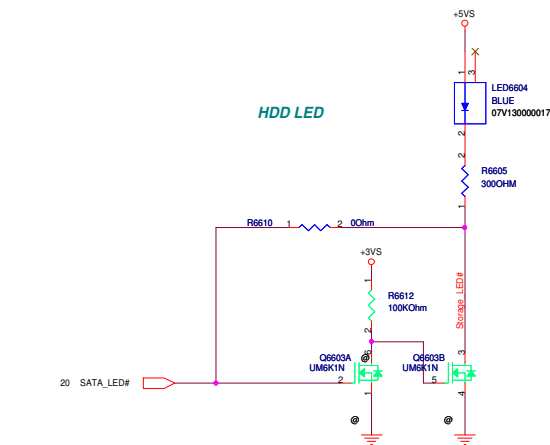
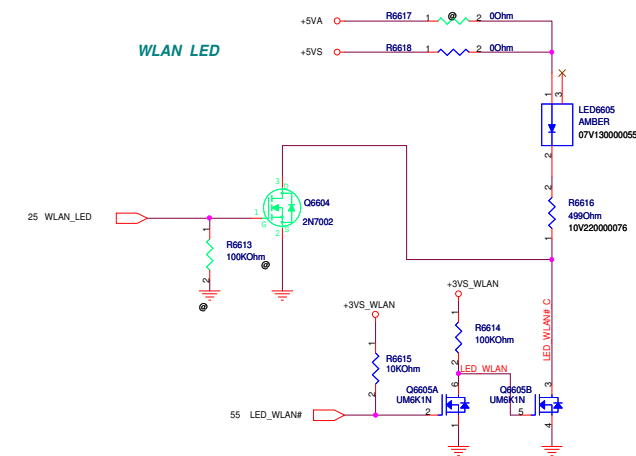
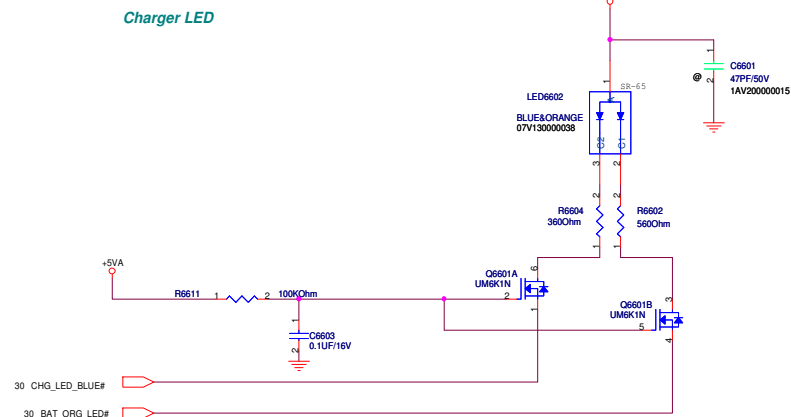
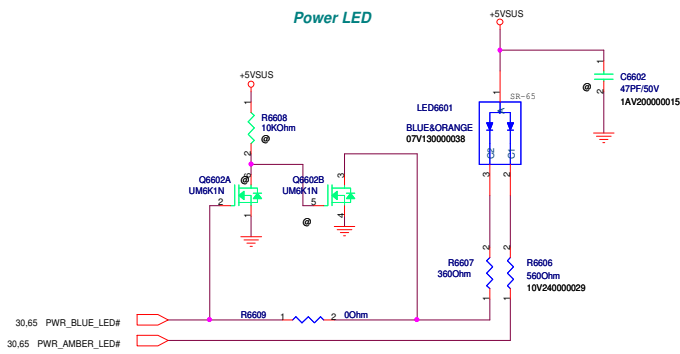
change Power LED CON6503 circuit

DEBUG CARD CONN.



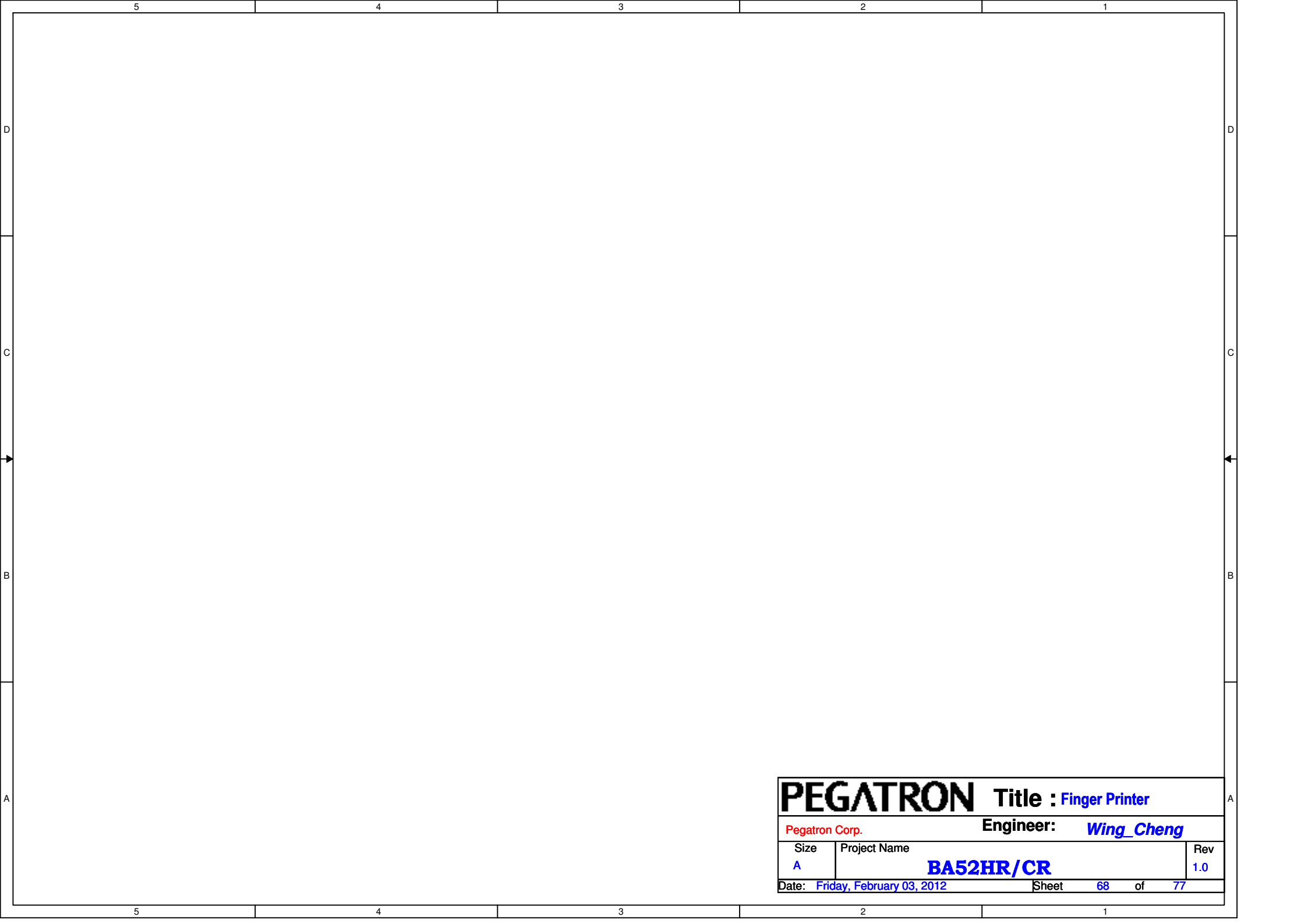
Frank
 0425_modify Debug port
 (add EXT_SMI#_C and INT_SERIRQ_C)
 CR R1.0 change part for EOL. Joyoung0803
 PS. Pin define is reverse.



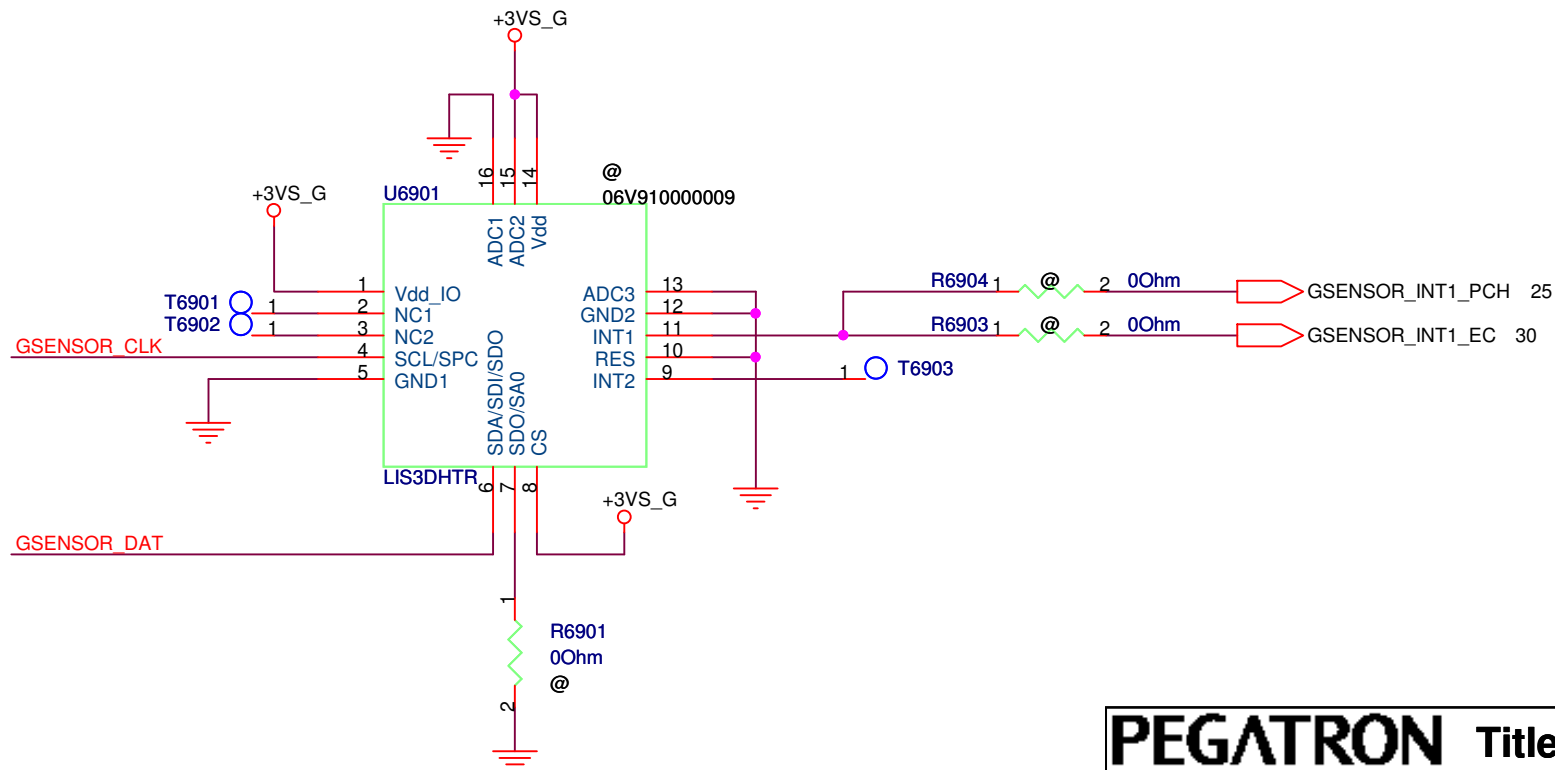
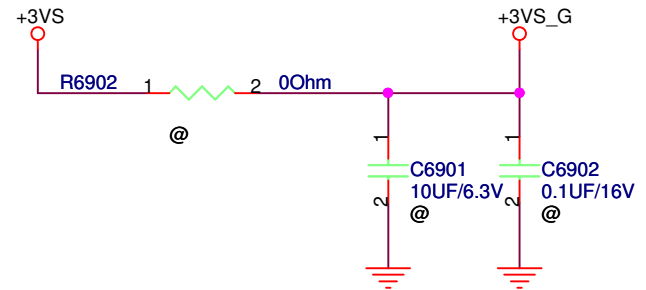
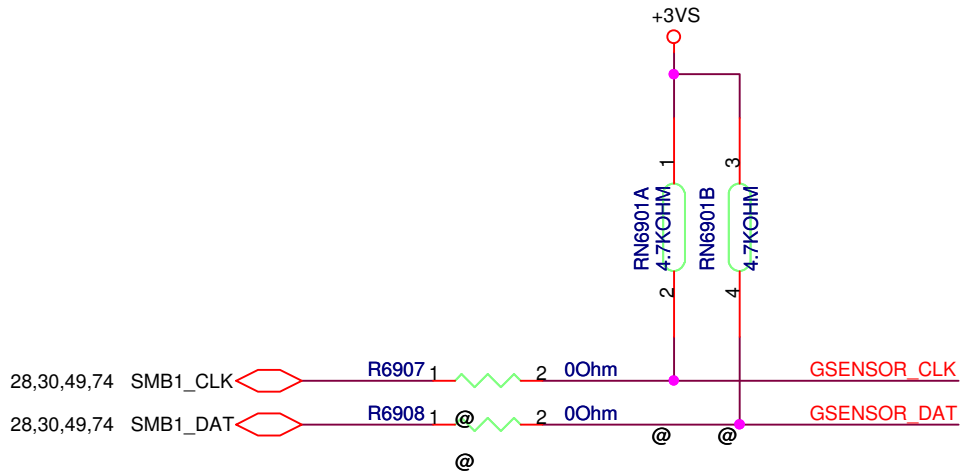




PEGATRON		Title : TPM	
Pegatron Corp.		Engineer: Wing_Cheng	
Size	Project Name		Rev
B	BA52HR/CR		1.0
Date: Friday, February 03, 2012		Sheet 67 of 77	

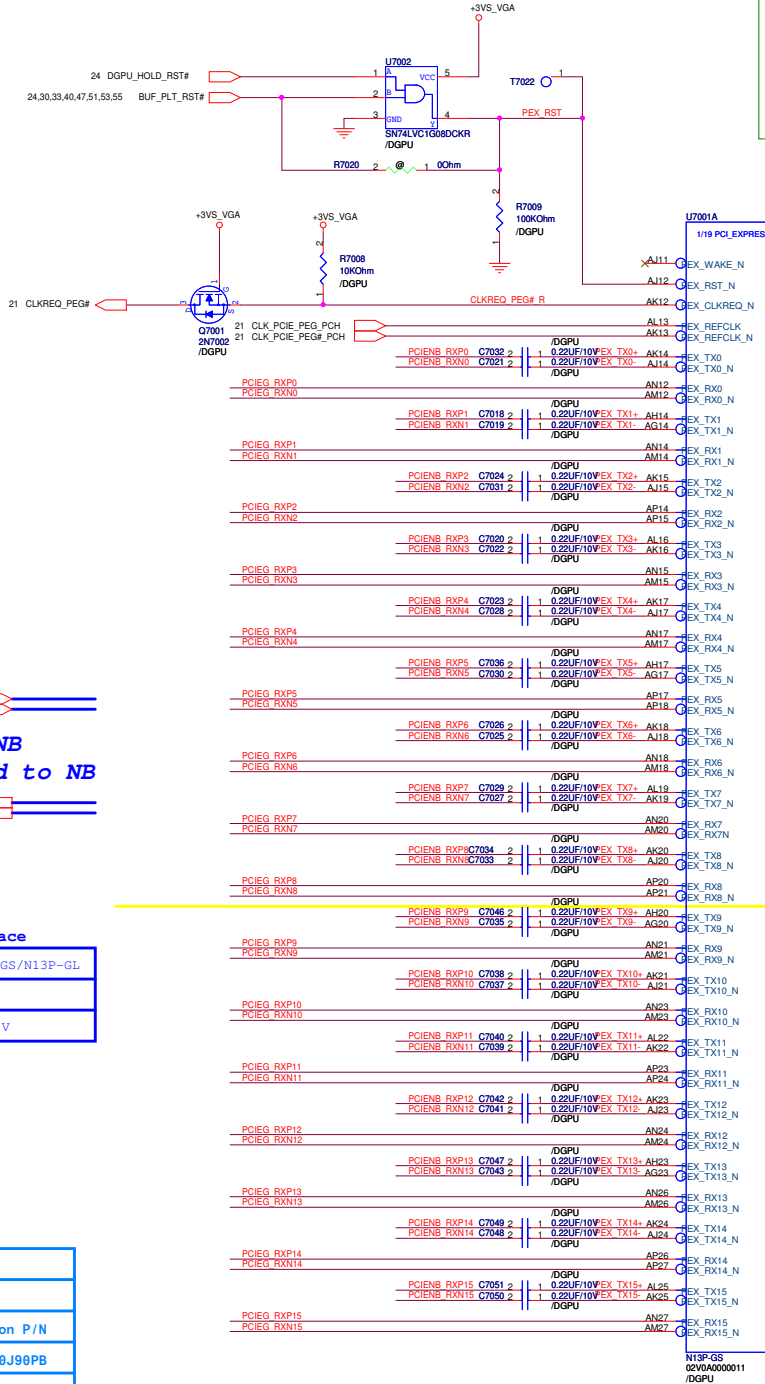


PEGATRON Title : Finger Printer		
Pegatron Corp.		Engineer: Wing Cheng
Size A	Project Name BA52HR/CR	Rev 1.0
Date: Friday, February 03, 2012		Sheet 68 of 77



PEGATRON Title : G-Sensor TSH35TR		
BU1-RD Div.1-HW RD Dept.1		Engineer: <i>Wing Cheng</i>
Size A	Project Name	Rev 1.0
Date: Friday, February 03, 2012	Sheet 69	of 77

Frank
20110513 Change N13P GPU.



**PEX=> From NB
EXP: VGA Card to NB**

3 PCIEB_RXP[0..15]
3 PCIEB_RXN[0..15]

3 PCIEG_RXP[0..15]
3 PCIEG_RXN[0..15]

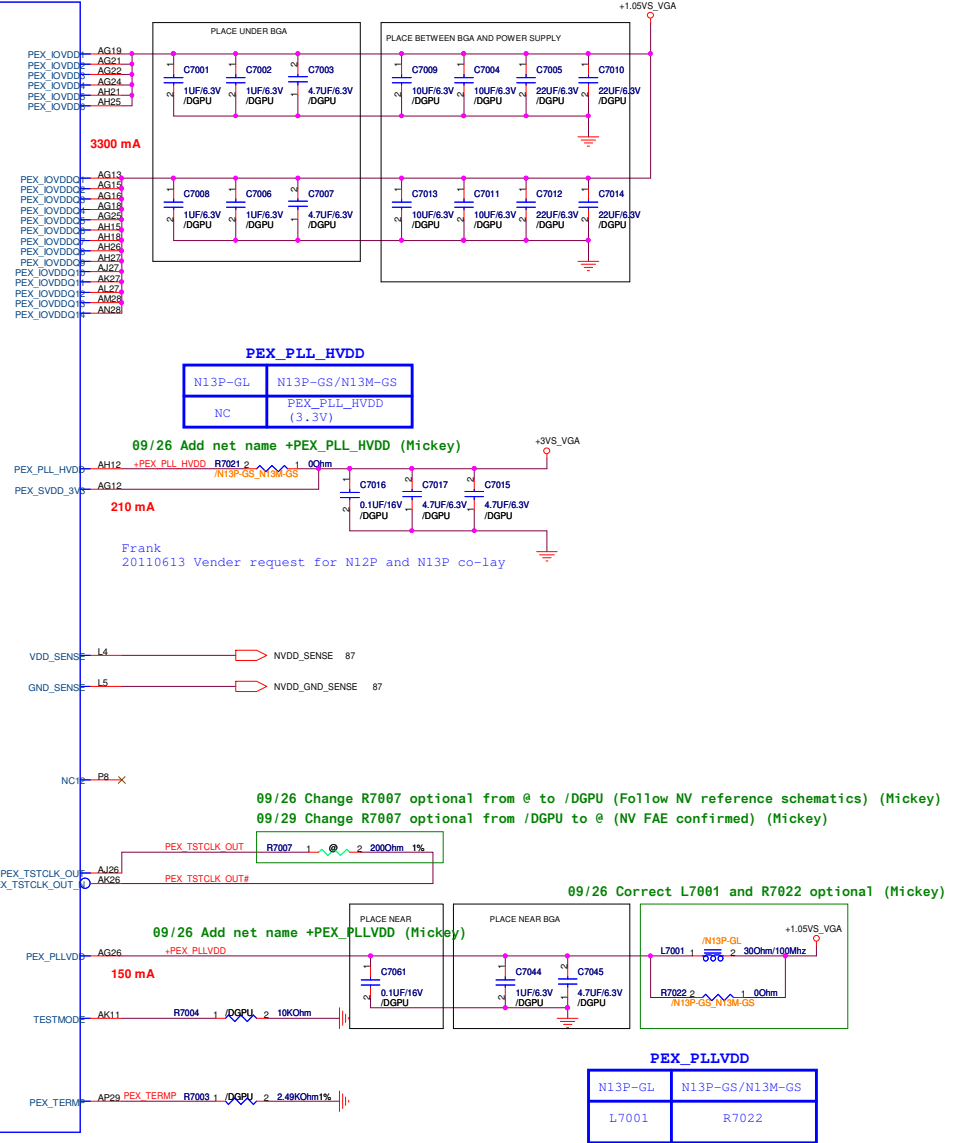
PCIe interface

	N13M-GS	N13P-GS/N13P-GL
8 Lane	V	
16 Lane		V

GPU Information		
GPU Location : U7001		
Type	Version	Pegatron P/N
N13P-GS	ES	020A-00J90PB
N13P-GL	QS	020A-00K60PB
N13M-GS	ES	020A-00JD0PB

GPU BOM Optional Definition

@ => Unmount.
/DGPU => Discrete and Optimus SKU.
/DGPU0 => Discrete SKU only.
/OPT => Optimus SKU only.
/N13P-GS => When N13P-GS is mounted, we need to mount this optional.
/N13P-GL => When N13P-GL is mounted, we need to mount this optional.
/N13P-GS_N13M-GS => When N13P-GS or N13M-GS are mounted, we need to mount this optional.
/N13P-GS_N13P-GL => When N13P-GS or N13P-GL are mounted, we need to mount this optional.



3300 mA

PEX_PLL_HVDD	
N13P-GL	N13P-GS/N13M-GS
NC	PEX_PLL_HVDD (3.3V)

09/26 Add net name +PEX_PLL_HVDD (Mickey)

210 mA

Frank
20110613 Vender request for N12P and N13P co-lay

VDD_SENS# L4 NVDD_SENS# 87
GND_SENS# L5 NVDD_GND_SENS# 87

09/26 Change R7007 optional from @ to /DGPU (Follow NV reference schematics) (Mickey)
09/29 Change R7007 optional from /DGPU to @ (NV FAE confirmed) (Mickey)

09/26 Correct L7001 and R7022 optional (Mickey)

09/26 Add net name +PEX_PLLVDD (Mickey)

150 mA

PEX_PLLVDD	
N13P-GL	N13P-GS/N13M-GS
L7001	R7022

FBB channel

	N13M-GS	N13P-GS/N13P-GL
FBB	X	V
FBA	V	V

FB CLAMP

N13P-GL	N13P-GS/N13M-GS
NC	PD 10K

09/26 Change R7120 optional from /DGPU to /N13P-GS,N13M-GS (Mickey)
 09/27 Change net name from +FB_DLL_AVDD to +FB_PLL_AVDD (Mickey)

FB_DLL_AVDD

N13P-GL	N13P-GS/N13M-GS
NC	FB_DLL_AVDD (1.05V)

09/26 Add net name +FB_DLL_AVDD_R (Mickey)

11/14 Delete T7102, T7103, T7105, T7106, T7107, T7108 (NV Recommend) (Mickey)

FB CLAMP

N13P-GL	N13P-GS/N13M-GS
NC	PD 10K

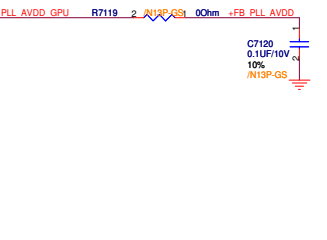
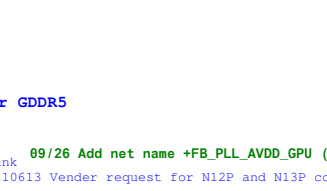
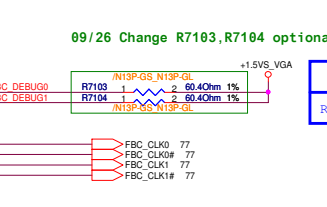
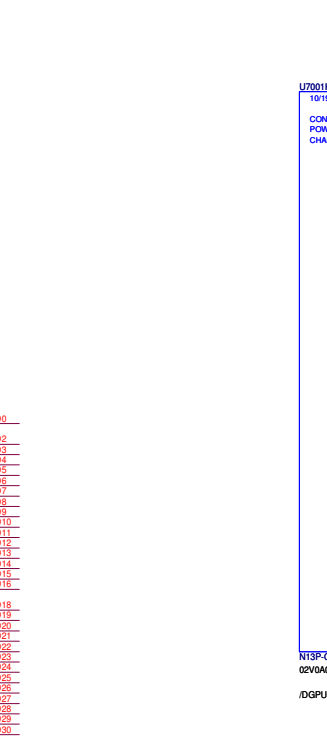
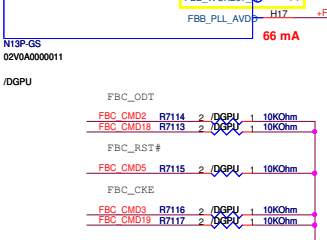
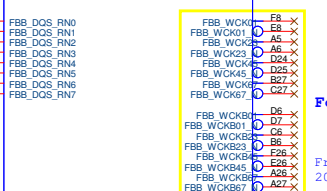
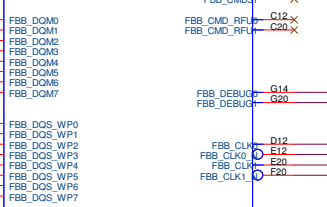
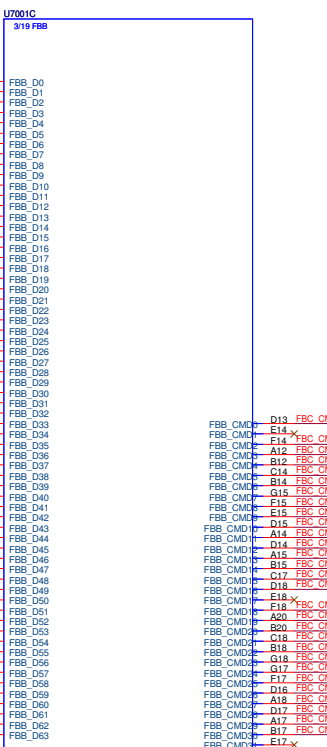
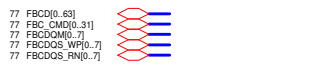
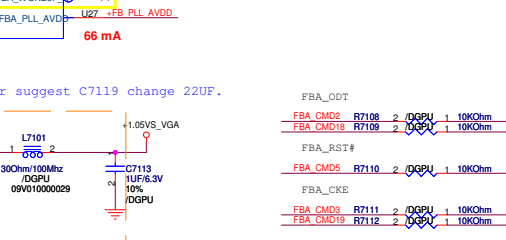
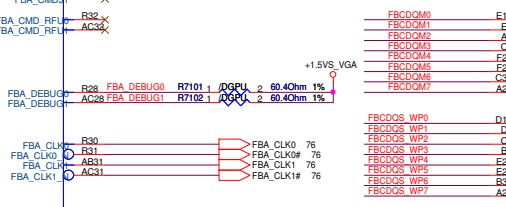
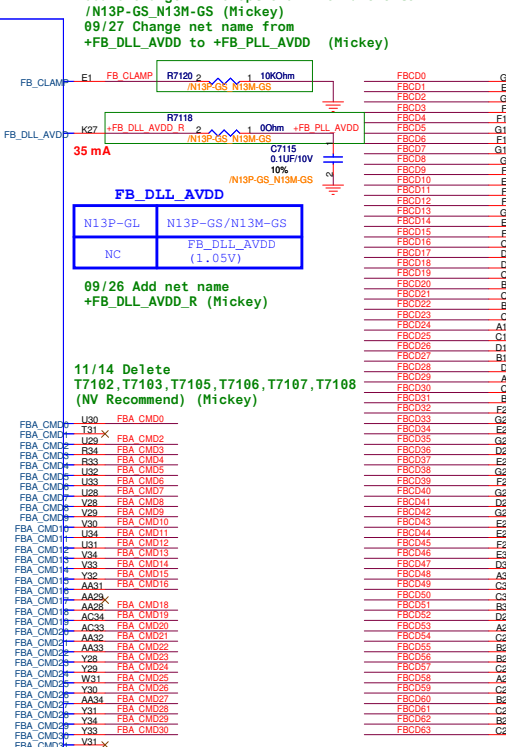
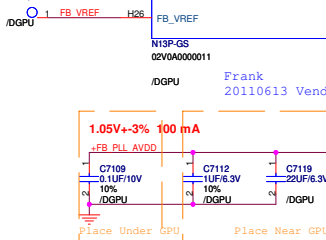
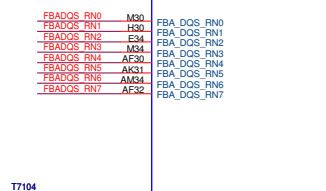
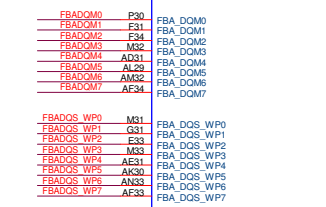
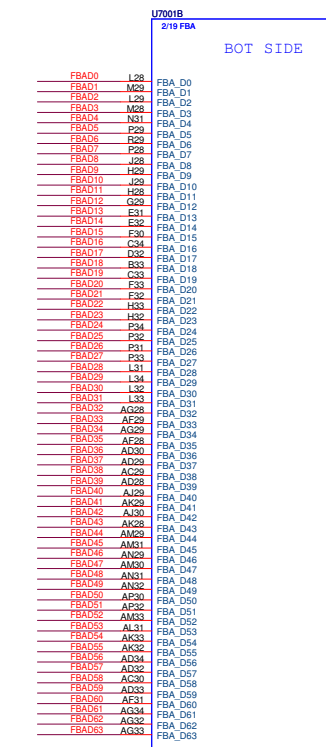
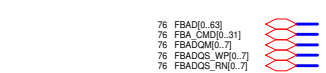
09/26 Change R7103, R7104 optional from /DGPU to /N13P-GS,N13P-GL (Mickey)

FBB_PLL_AVDD

N13P-GL/N13M-GS	N13P-GS
NC	FBB_PLL_AVDD (1.05V)

09/26 Add net name +FB_PLL_AVDD_GPU (Mickey)

Frank 20110613 Vender request for N12P and N13P co-lay



U7001H

1019 XVDD

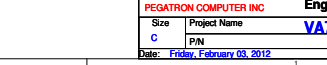
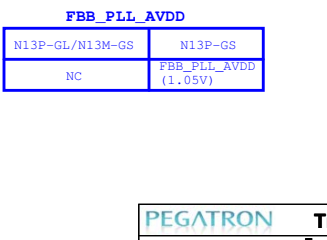
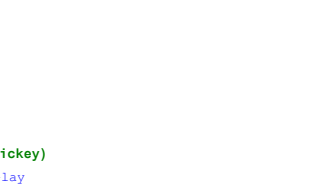
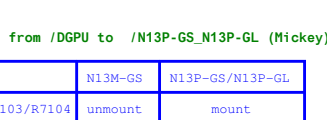
CONFIGURABLE POWER CHANNELS

XVDD_1	U1 X
XVDD_2	U2 X
XVDD_3	U3 X
XVDD_4	U4 X
XVDD_5	U5 X
XVDD_6	U6 X
XVDD_7	U7 X
XVDD_8	U8 X
XVDD_9	U9 X
XVDD_10	U10 X
XVDD_11	U11 X
XVDD_12	U12 X
XVDD_13	U13 X
XVDD_14	U14 X
XVDD_15	U15 X
XVDD_16	U16 X
XVDD_17	U17 X
XVDD_18	U18 X
XVDD_19	U19 X
XVDD_20	U20 X
XVDD_21	U21 X
XVDD_22	U22 X
XVDD_23	U23 X
XVDD_24	U24 X
XVDD_25	U25 X
XVDD_26	U26 X
XVDD_27	U27 X
XVDD_28	U28 X
XVDD_29	U29 X
XVDD_30	U30 X
XVDD_31	AA1 X
XVDD_32	AA2 X
XVDD_33	AA3 X
XVDD_34	AA4 X
XVDD_35	AA5 X
XVDD_36	AA6 X
XVDD_37	AA7 X
XVDD_38	AA8 X

N13P-GS 02V0A0000011

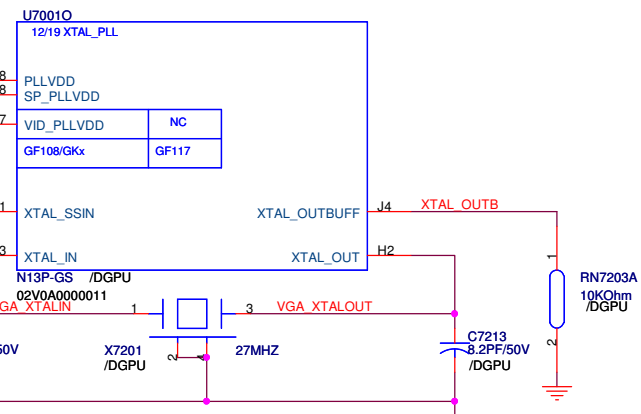
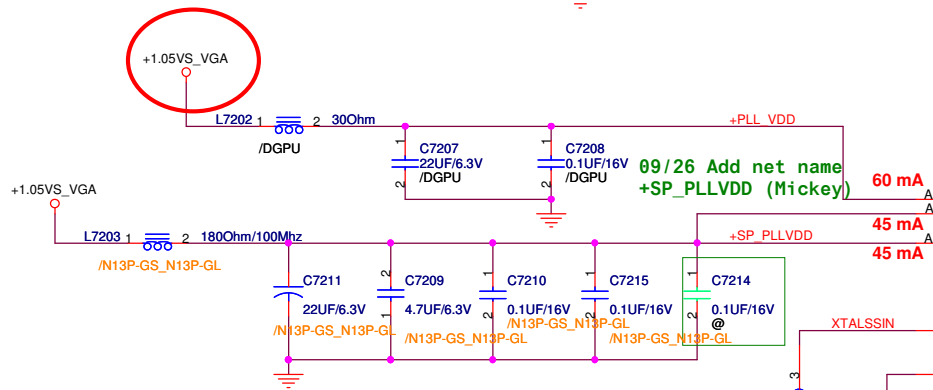
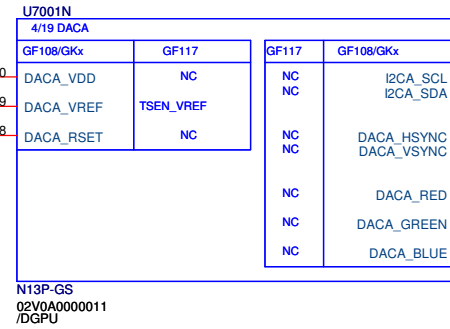
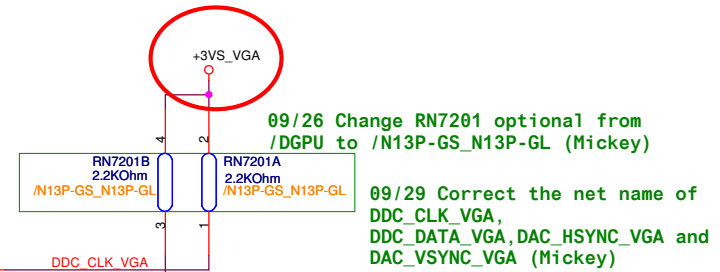
/DGPU

FBB channel



- 10/03 Change C7203 optional from /DGPU to @ (Follow NV FAE recommend) (Mickey)
- 09/27 Change L7201 from 300ohm bead to 220ohm bead (Follow NV design guide) (Mickey)
- 09/27 Change R7202,C7206 optional from /DGPU to /N13P-GS_N13P-GL (Mickey)
- 09/26 Change R7201 optional from /DGPU to /OPT (Mickey)
- 09/26 Change C7201~7205,L7201 optional from /DGPU to /DGPU (Mickey)

RGB	
N13M-GS	N13P-GL/N13P-GS
NC	RGB Function



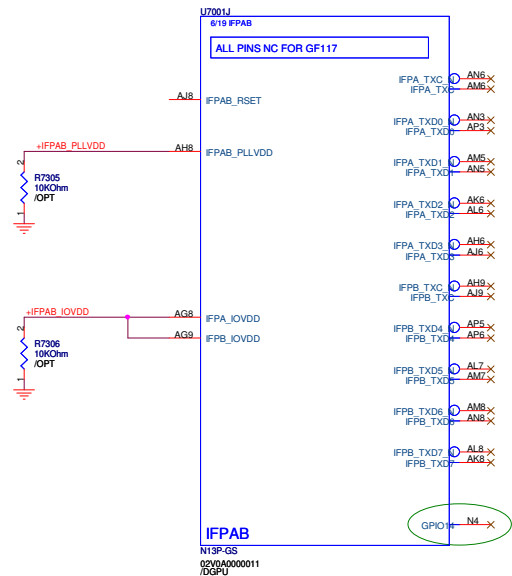
VID_PLLVDD	
N13M-GS	N13P-GL/N13P-GS
NC	VID_PLLVDD (1.05V)

Frank
20110613 Follow Vender and spec suggest

- 10/03 Change C7214 optional from /N13P-GS_N13P-GL to @ (Follow NV FAE recommend) (Mickey)
- 11/14 Change C7211 from 0805 to 0603 (The height limit for thermal module) (Mickey)

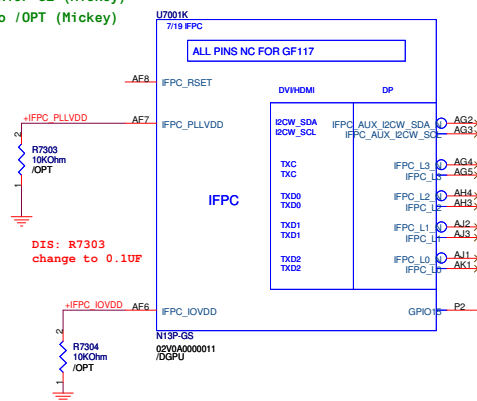
PEGATRON		Title : GPU_RGB/XTAL	
PEGATRON COMPUTER INC		Engineer: Mickey_Yu	
Size	Project Name	Rev	
B	VA70_N13P-GDDR3	1.0	
Date: Friday, February 03, 2012		Sheet 72 of 99	

LVDS

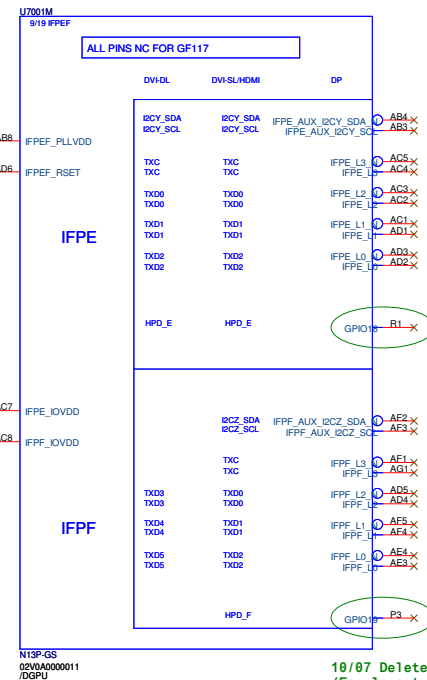
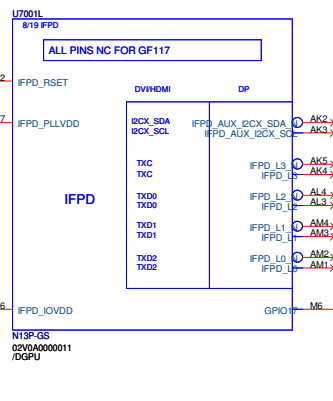


HDMI

09/27 Change R7302 optional from /DGPU to /N13P-GS_N13P-GL (Mickey)
 09/26 Change R7303,R7304 optional from /DGPU_ONLY to /OPT (Mickey)
 09/26 Change C7307-7315, L7303, L7305 optional from /DGPU_ONLY to /DGPUO (Mickey)



DIS: R7303 change to 0.10F



10/07 Delete T7310, T7311 (For layout spacing) (Mickey)

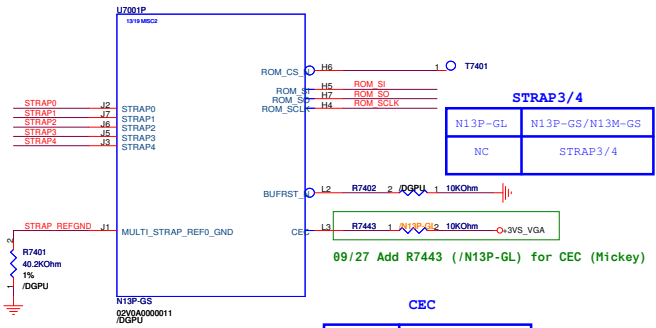
GPIO

	N13M-GS	N13P-GS/N13P-GL
GPIO14	X	V
GPIO15	X	V
GPIO16	X	V
GPIO17	X	V
GPIO18	X	V
GPIO19	X	V

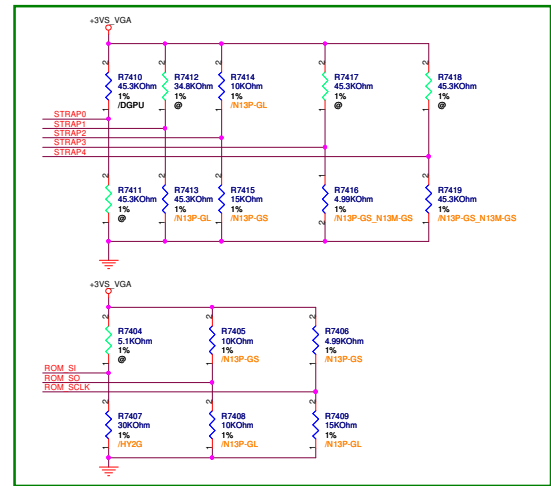
IFPX channel

	N13M-GS	N13P-GS/N13P-GL
IFPA/B	X	V
IFPC	X	V
IFPD	X	V
IFPE/F	X	V

LVDS
HDMI
EDP



CEC	
N13P-GL	N13P-GS/N13M-GS
PU 10K (3V3)	NC



N13P-GS ES2/QS	
DEVICE ID	0xFDB
STRAP0	45K PU
STRAP1	35K PU
STRAP2	15K PD
STRAP3	5K PD
STRAP4	10K PD
ROM_SCLK	5K PU
ROM_SI	Hynix 128Mx16 35K PD
ROM_S0	Hynix 64Mx16 15K PD R7407
ROM_S1	10K PU

N13P-GL QS	
DEVICE ID	0xDE9
STRAP0	45K PU
STRAP1	45K PD
STRAP2	10K PU R7414
STRAP3	NC
STRAP4	NC
ROM_SCLK	15K PD
ROM_SI	Hynix 128Mx16 35K PD
ROM_S0	Hynix 64Mx16 15K PD R7407
ROM_S1	10K PD

STRAP2--GPU TYPE		
N13M-GS	N13P-GL	N13P-GS

ROM_SI--VRAM TYPE			
HYNIX		SAMSUNG	
64Mx16	128Mx16	64Mx16	128Mx16

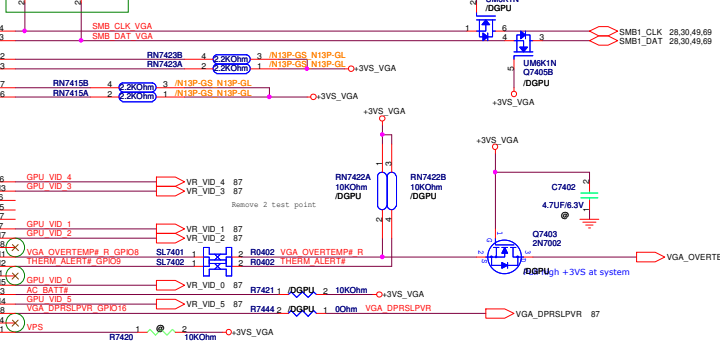
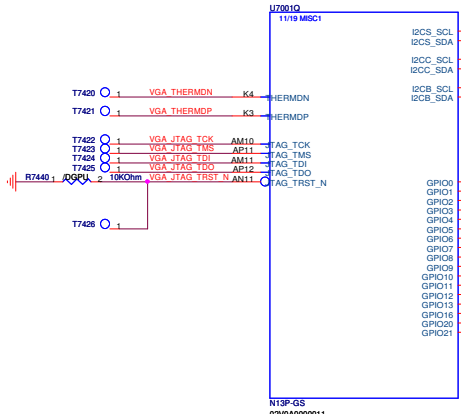
STRAP1 R7413	N13P-GS ES2/QS	N13P-GL QS
	35K	45K

ROM_SI R7407	Hynix 128Mx16	Hynix 64Mx16
	35K	15K

I2CB_SCL/SDA		
N13M-GS	N13P-GS	N13P-GL
RN7415	unmount	mount

09/26 Change RN7413 from 2.2kohm to 100kohm(R7441,R7442) (Follow NV reference schematics) (Mickey)
 10/03 Change R7441,R7442 from 100kohm to 2.2kohm(Follow NV FAE recommend) (Mickey)

11/28 Change R7413 from /DGPU to /N13P-GS (Follow NV FAE recommend) (Mickey)
 11/28 Change R7414 from 20kohm to 10kohm(/N13P-GL) (Follow NV FAE recommend) (Mickey)
 11/28 Change R7415 from 5kohm to 15kohm(/N13P-GS) (Follow NV FAE recommend) (Mickey)

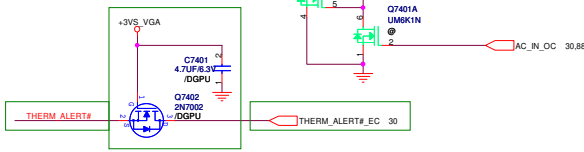


09/29 Add net name VGA_OVERTEMP#_R_GPI08 and THERM_ALERT#_GPI09 on U7001Q_H1/H2 (GPI08/9) (Mickey)
 09/29 Delete T7427, add R7444 (0ohm) and VGA DPRSLPVR off-page on U7001Q_R8 (GPI016) (Mickey)
 10/07 Delete T7428,T7433,T7435 (For layout spacing) (Mickey)

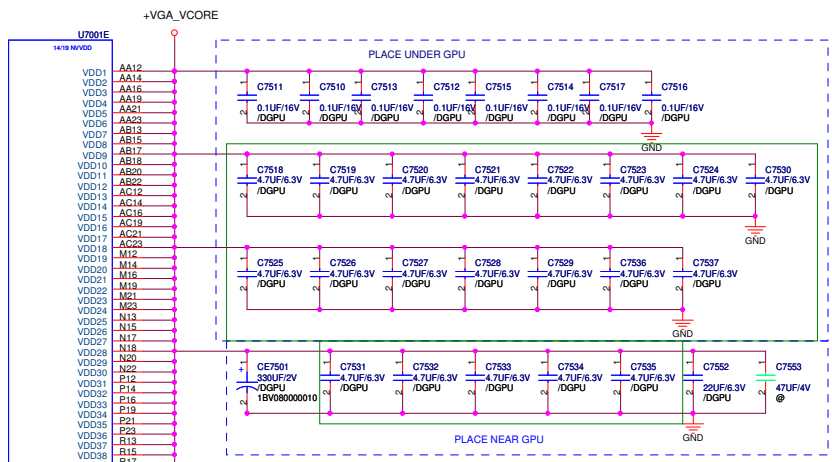
N13P-GT ES2/QS	
DEVICE ID	0xFD1
STRAP0	45K PU
STRAP1	35K PD
STRAP2	10K PD
STRAP3	5K PD
STRAP4	10K PD
ROM_SCLK	5K PU
ROM_SI	Hynix 128Mx16 35K PD
ROM_S0	Hynix 64Mx16 15K PD R7407
ROM_S1	10K PU

GPIO		
GPI020	N13M-GS	N13P-GS/N13P-GL
	X	X
GPI021	X	X

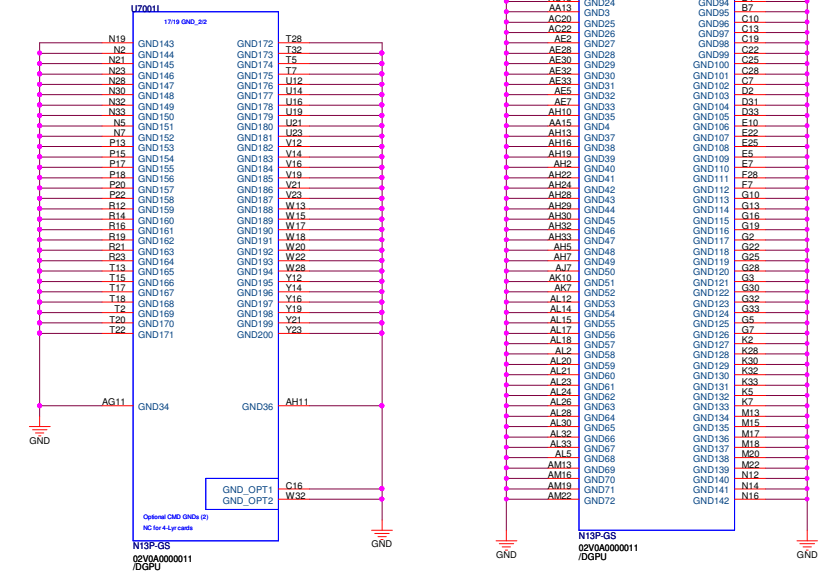
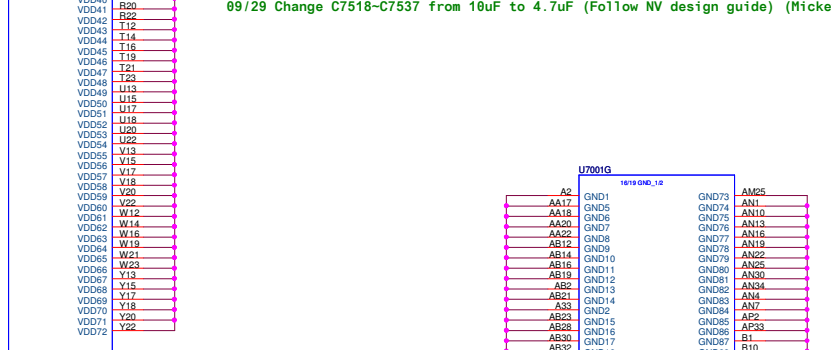
GPIO 8		
Q7403	N13P-GL	N13P-GS/N13M-GS
	unmount	NV suggestion mount



09/29 Change Q7401,Q7402 optional from @ to /DGPU(Mickey)
 09/29 Change net name from VPS to THERM_ALERT# on Q7402.2 (Mickey)
 09/29 Change net name from VPS_EC to THERM_ALERT#_EC on Q7402.3 (Mickey)

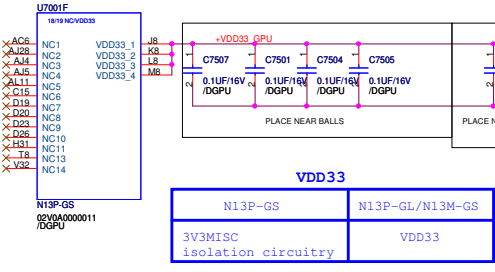


09/29 Change C7518-C7537 from 10uF to 4.7uF (Follow NV design guide) (Mickey)



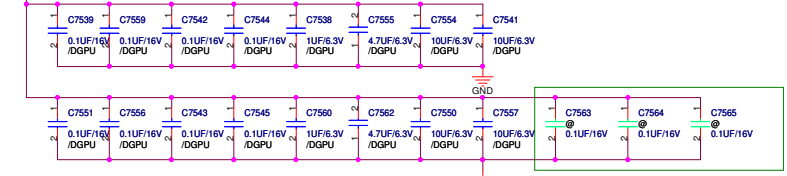
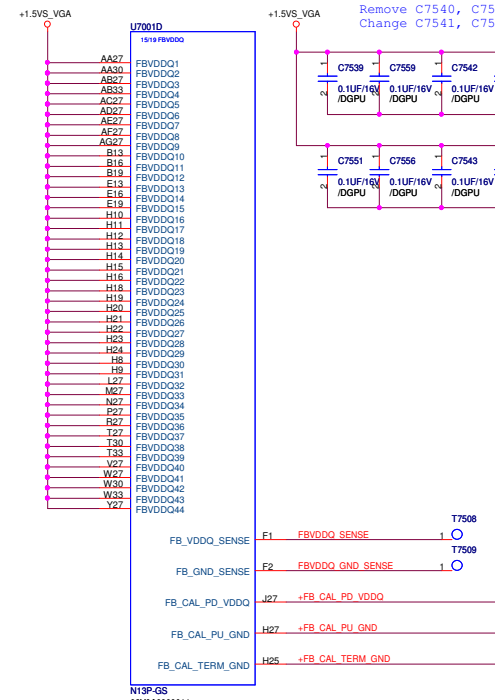
09/26 Add net name +VDD33_GPU (Mickey)

09/26 Add C7506,C7508,C7509 (Follow NV reference schematics) (Mickey)
09/27 Remove C7506,C7508,C7509 (Follow NV design guide) (Mickey)

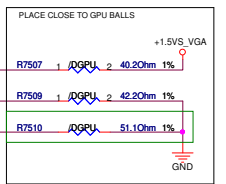


check with NV==>可先不用Isolation circuitry

Frank
20110613 Follow Vender and spec suggest
=> Add C7542, C7543, C7544, C7545 and C7556 mount
Remove C7540, C7561, C7558, C7649
Change C7541, C7557 to 10uF



11/21 Add C7563,C7564,C7565 (0.1uF) at +1.5VS_VGA (EMI Recommend) (Mickey)



09/28 Change R7510 from 60.4ohm to 51.1ohm (Follow NV design guide) (Mickey)

Frank
20110613 Follow Vender and spec suggest=>Remove R7509 change 42.2 ohm

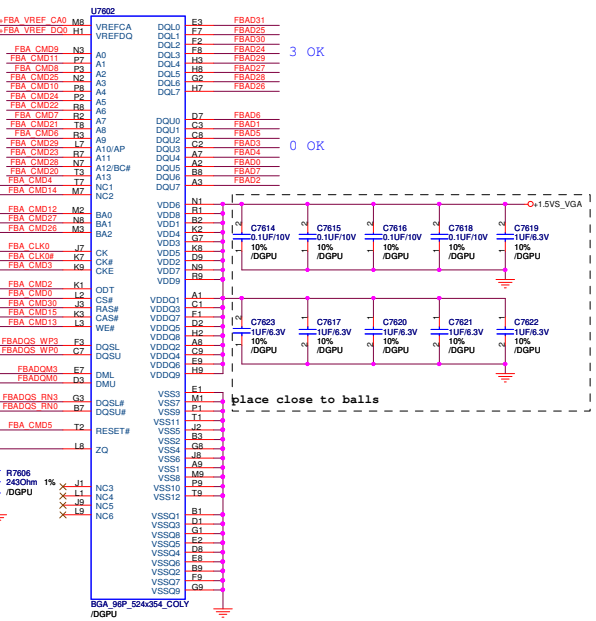
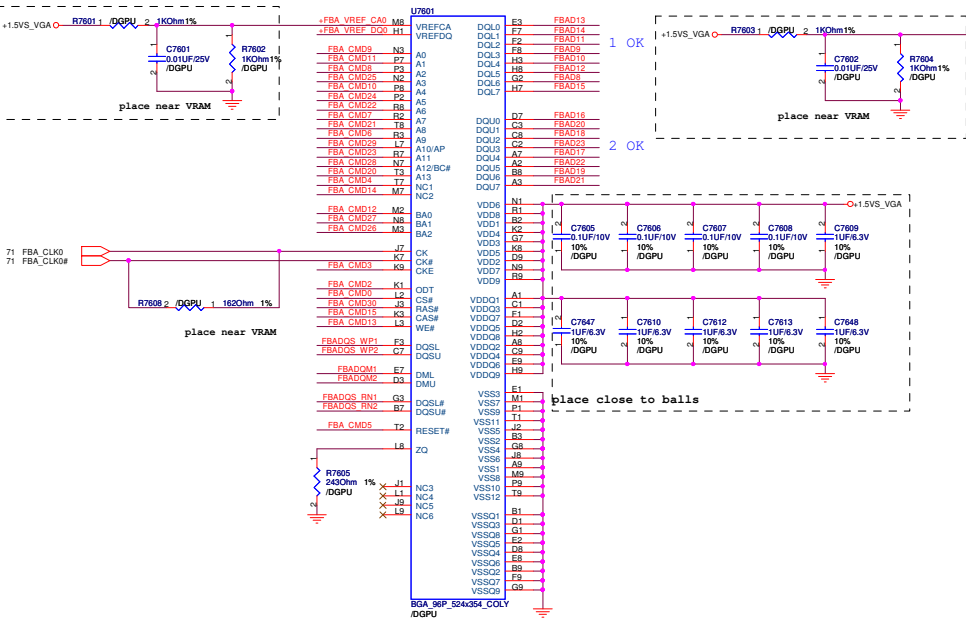
VRAM CH A

TOP SIDE

BOT SIDE

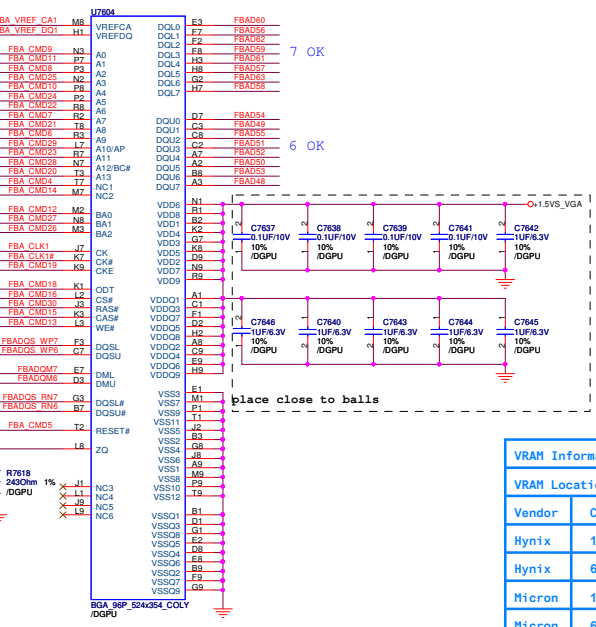
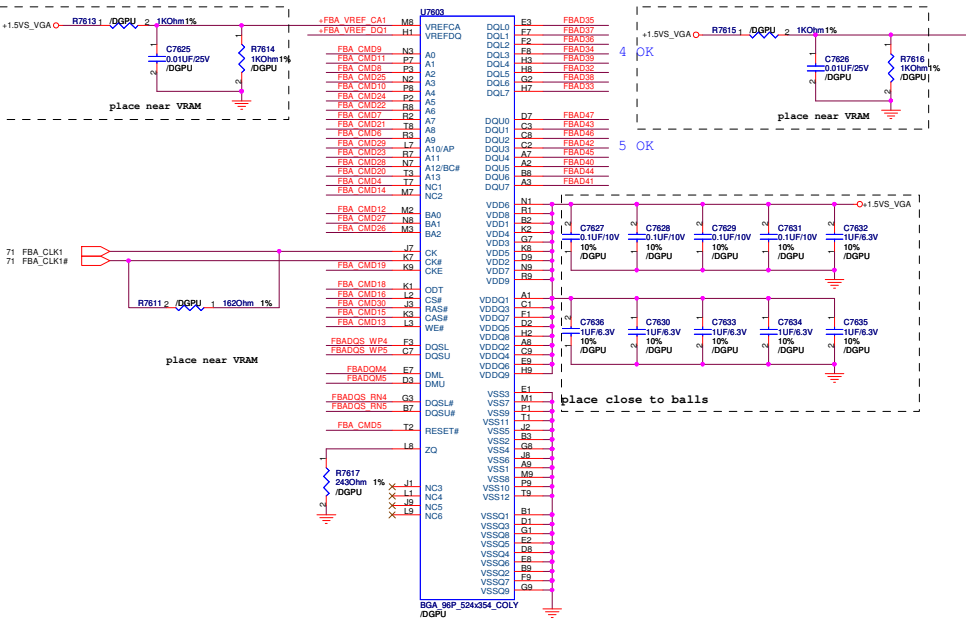
09/27 Swap VRAM data signal. (Mickey)

M1X3 DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
CMD0	CS0#	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE#	WE#
CMD14	A15	A15
CMD15	CAS#	CAS#
CMD16		CS0#
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS#	RAS#
CMD31		



TOP SIDE

BOT SIDE



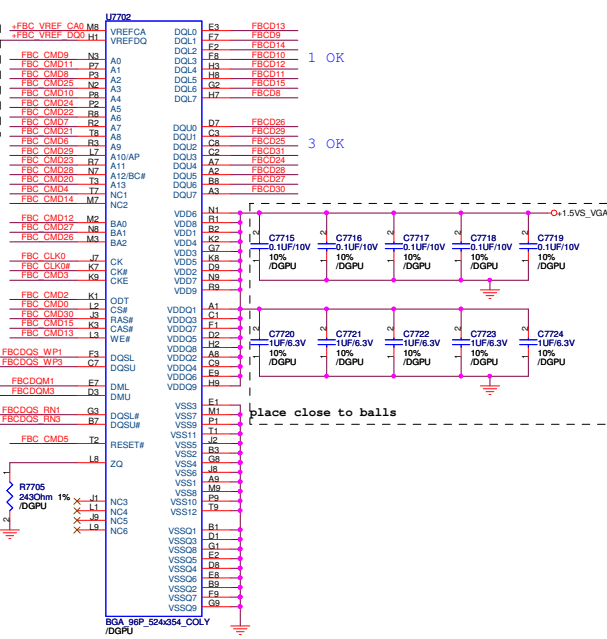
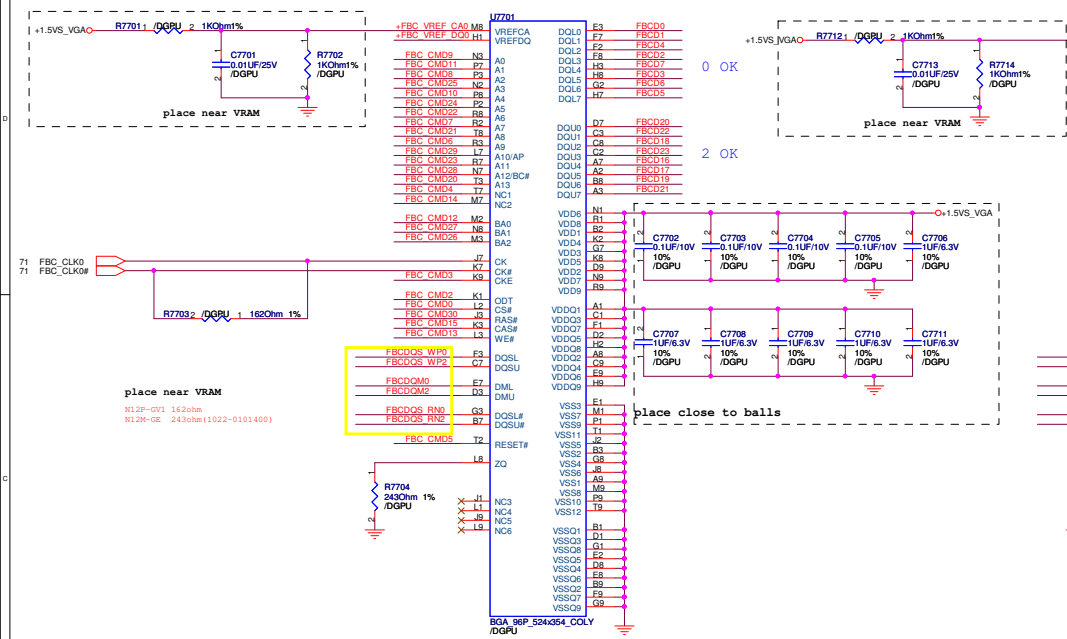
VRAM Information				VRAM Strap	
VRAM Location : U7601,U7602,U7603,U7604,U7701,U7702,U7703,U7704				VRAM Strap Location : R7487	
Vendor	Configuration	Pegatron P/N	Manufacturer P/N		
Hynix	128Mx16	0315-09ND0PB	H5TQ2G63BFR-11C	0x6	35K
Hynix	64Mx16	0315-09NF0PB	H5TQ1G63DFR-11C	0x2	15K
Micron	128Mx16	TBD	MT41J128M16JT-107G:K	TBD	TBD
Micron	64Mx16	0315-09S0PB	MT41J64M16JT-107G:G	TBD	TBD

VRAM CH C

TOP SIDE

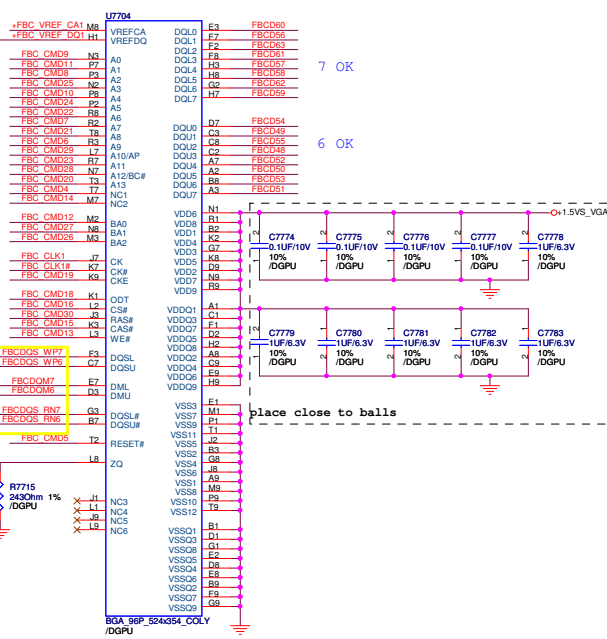
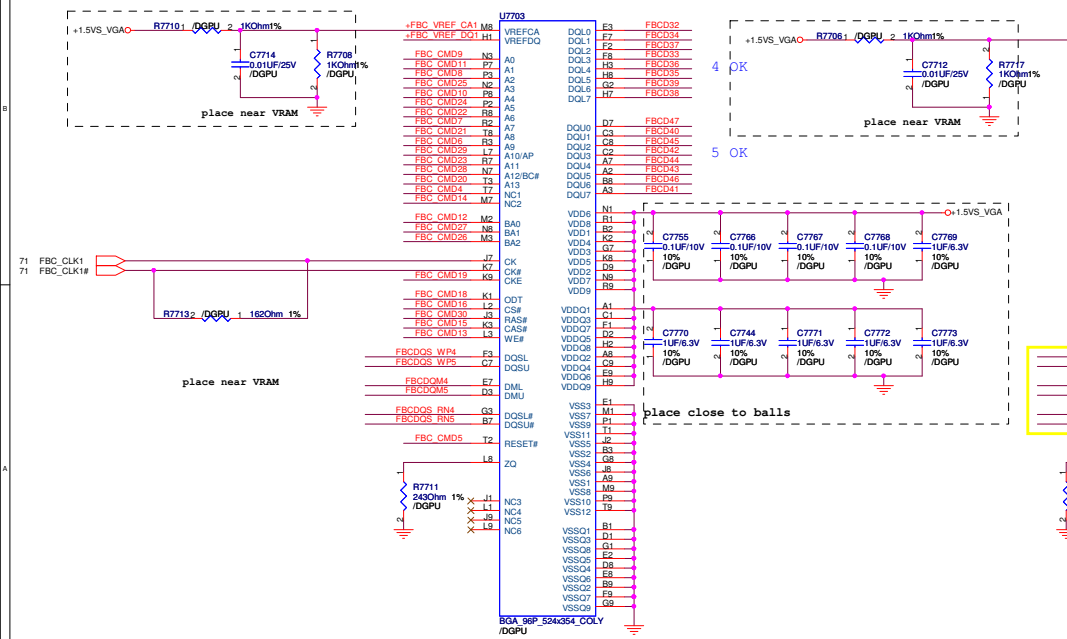
BOT SIDE

09/27 Swap VRAM data signal. (Mickey)



TOP SIDE

BOT SIDE



M13X DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
CMD0	CS0#	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE#	WE#
CMD14	A15	A15
CMD15	CAS#	CAS#
CMD16		CS0#
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS#	RAS#
CMD31		

PEGATRON		Title :	
PEGATRON COMPUTER INC		Engineer: Mickey_Yu	
Size	Project Name	Rev	
C	P/N	1.0	
Date: Friday, February 03, 2012		Sheet	78 of 99

5

4

3

2

1

D

D

C

C

B

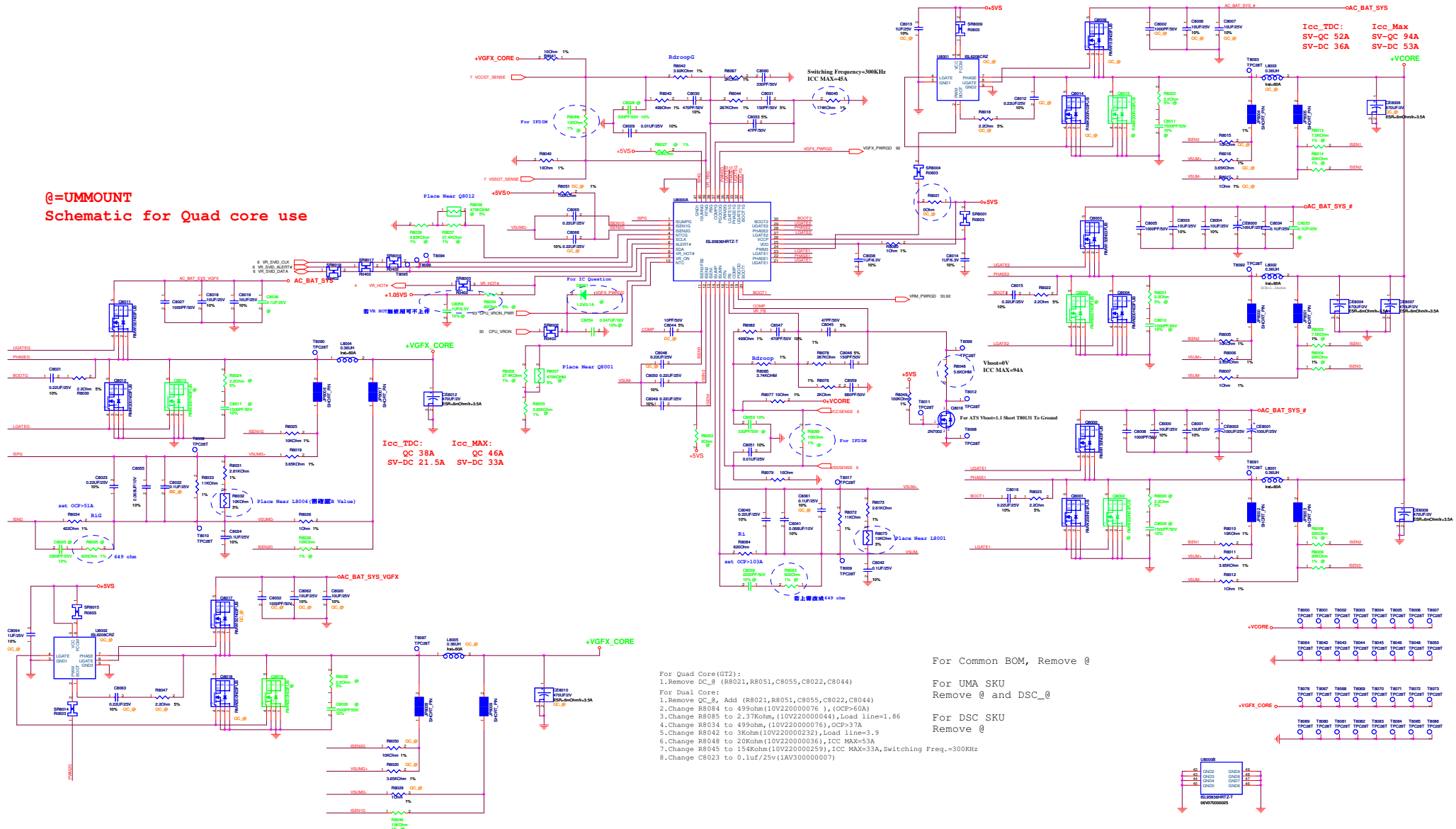
B

A

A

PEGATRON		Title : GPU_PEG*16	
PEGATRON COMPUTER INC		Engineer: Mickey_Yu	
Size	Project Name	Rev	
C	VA79_N13P-GDDR3	1.0	
Date: Friday, February 03, 2012		Sheet	79 of 99

@=UMMOUNT
Schematic for Quad core use



Icc_TDC: QC 38A
 Icc_MAX: QC 46A
 SV-DC 21.5A SV-DC 33A

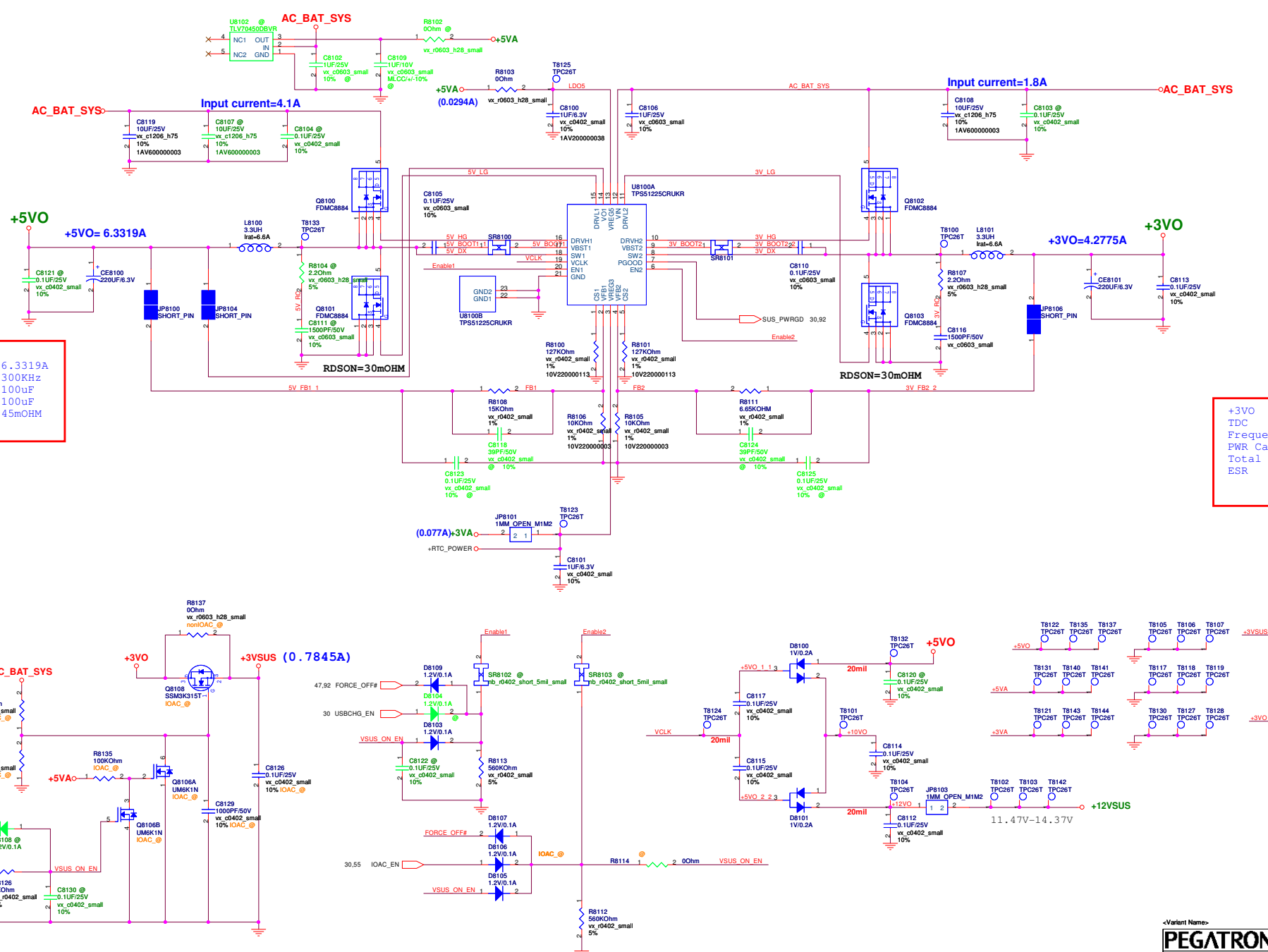
Icc_TDC: SV-QC 52A
 Icc_Max: SV-QC 94A
 SV-DC 36A SV-DC 53A

- For Quad Core (GT2):
 1.Remove OC_@ (R8021,R8051,C8055,C8022,C8044)
 For Dual Core:
 1.Remove QC_@, Add (R8021,R8051,C8055,C8022,C8044)
 2.Change R8084 to 499ohm (10V220000076), (OCP>60A)
 3.Change R8085 to 2.37Kohm, (10V220000044), Load line=1.86
 4.Change R8034 to 499ohm, (10V220000076), OCP>37A
 5.Change R8042 to 3Kohm (10V220000232), Load line=3.9
 6.Change R8048 to 20Kohm (10V220000036), ICC MAX=53A
 7.Change R8045 to 154Kohm (10V220000259), ICC MAX=33A, Switching Freq.=300KHz
 8.Change C8023 to 0.1uF/25v (1AV30000007)

For Common BOM, Remove @
 For UMA SKU
 Remove @ and DSC_@
 For DSC SKU
 Remove @



+5VO & +3VO POWER SUPPLY

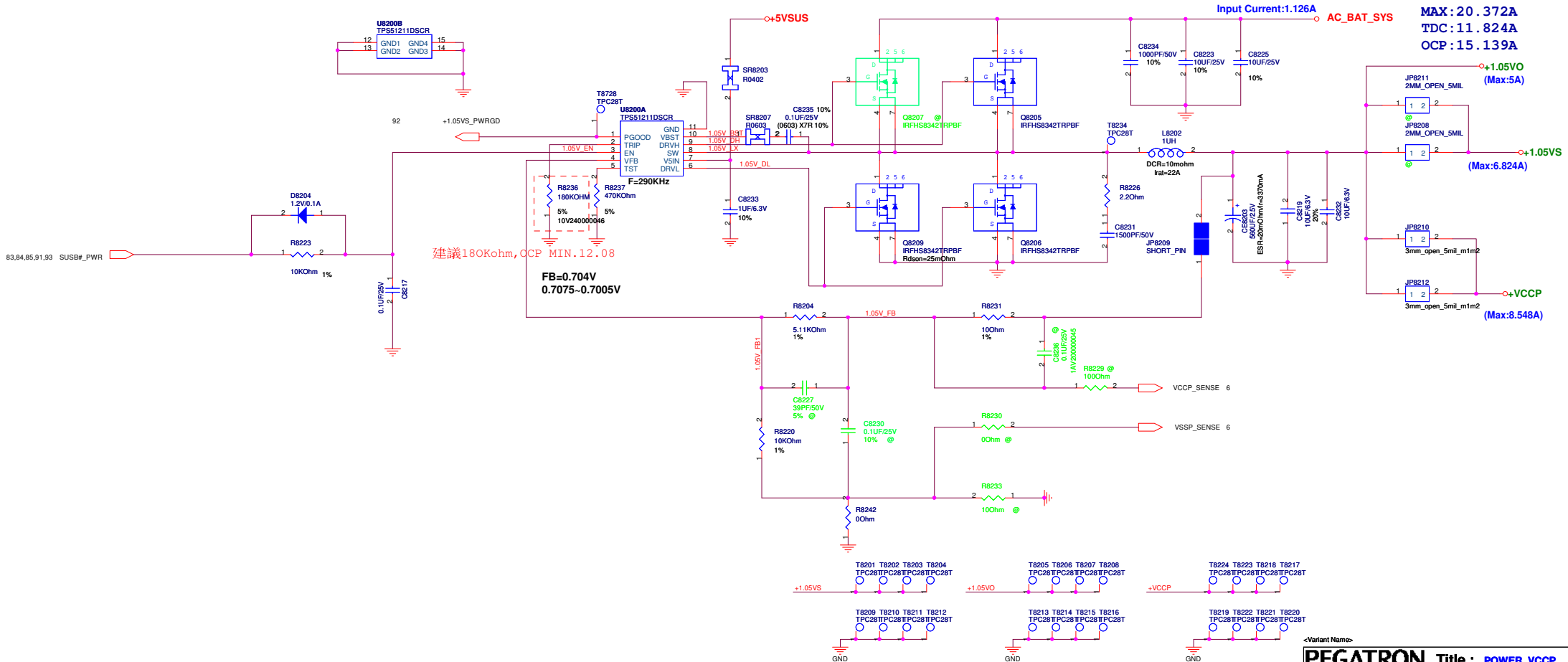


+5VO
 TDC : 6.3319A
 Frequency : 300KHz
 PWR Cap. : 100uF
 Total Cap. : 100uF
 ESR : 45mOHM

+3VO
 TDC : 4.2775A
 Frequency : 350KHz
 PWR Cap. : 100uF
 Total Cap. : 100uF
 ESR : 45mOHM

$TRIP\ V\ (mV) = TRIP\ R\ (k) * TRIP\ I\ (mA)$
 TRIPI current, which is 10uA
 $VOCP = TRIP\ V / (8 / R_{dson}) + (I\ ripple / 2)$

Used for testing purpose in production line.
 Pull down to GND with a resistor of 470 kΩ or less



MAX : 20.372A
 TDC : 11.824A
 OCP : 15.139A

Input Current: 1.126A AC_BAT_SYS

+1.05VO (Max:5A)

+1.05VS (Max:6.824A)

+VCCP (Max:8.548A)

建議180Kohm, CCP MIN.12.08

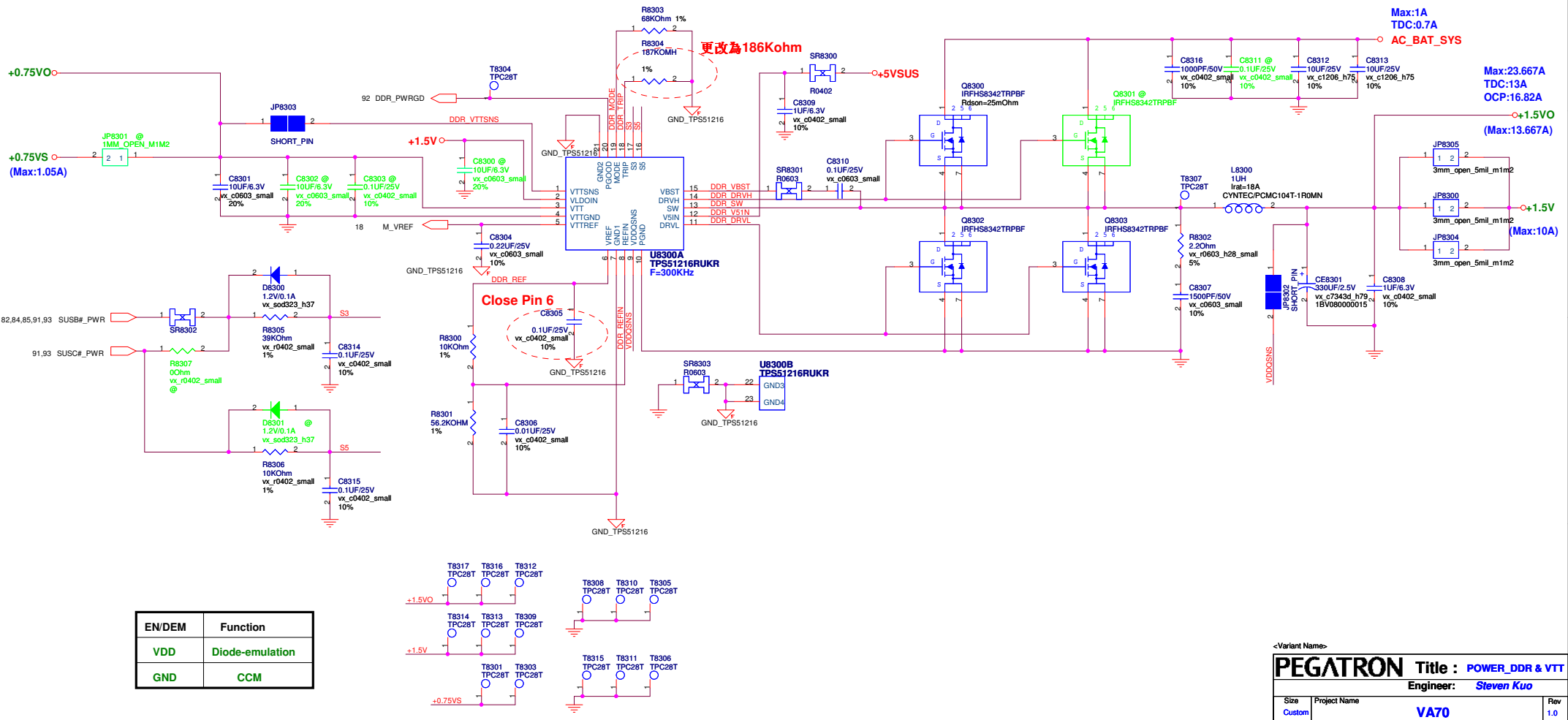
FB=0.704V
0.7075-0.7005V

Size		Project Name	Rev
Custom		VA70	1.1
Date: Friday, February 03, 2012 Sheet 82 of 94			

<Variant Name>

PEGATRON Title : POWER_VCCP
 Engineer: Steven Kuo

DDR & VTT POWER SUPPLY



<Variant Name>

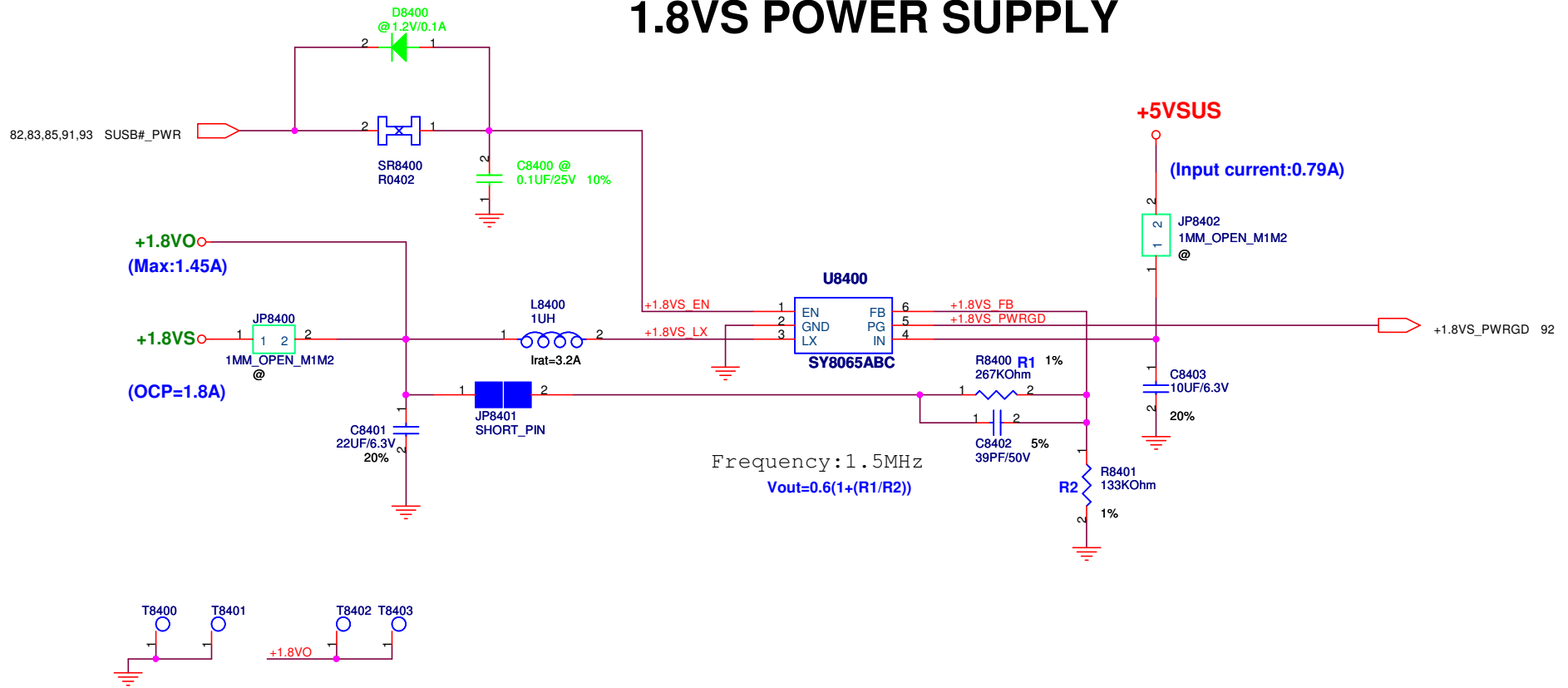
PEGATRON Title : **POWER_DDR & VTT**

Engineer: **Steven Kuo**

Size	Project Name	Rev
Custom	VA70	1.0

Date: **Friday, February 03, 2012** Sheet **83** of **94**

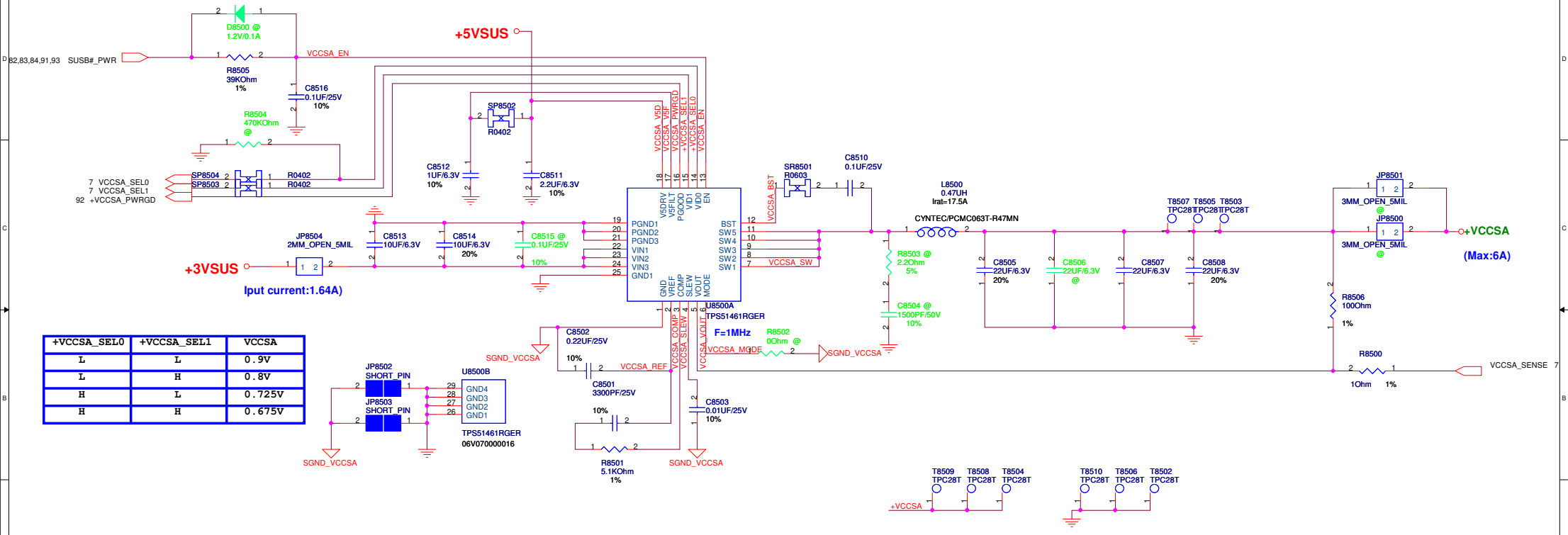
1.8VS POWER SUPPLY



<Variant Name>

PEGATRON		Title : POWER_1.8VS	
		Engineer: Steven Kuo	
Size Custom	Project Name	VA70	Rev 1.0
Date: Friday, February 03, 2012		Sheet	84 of 94

VCCSA POWER SUPPLY



+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Variant Name>

PEGATRON Title : **POWER_VCCSA**
 Engineer: **Steven Kuo**

Size	Project Name	Rev
Custom	VA70	1.0

Date: Friday, February 03, 2012 Sheet 85 of 94



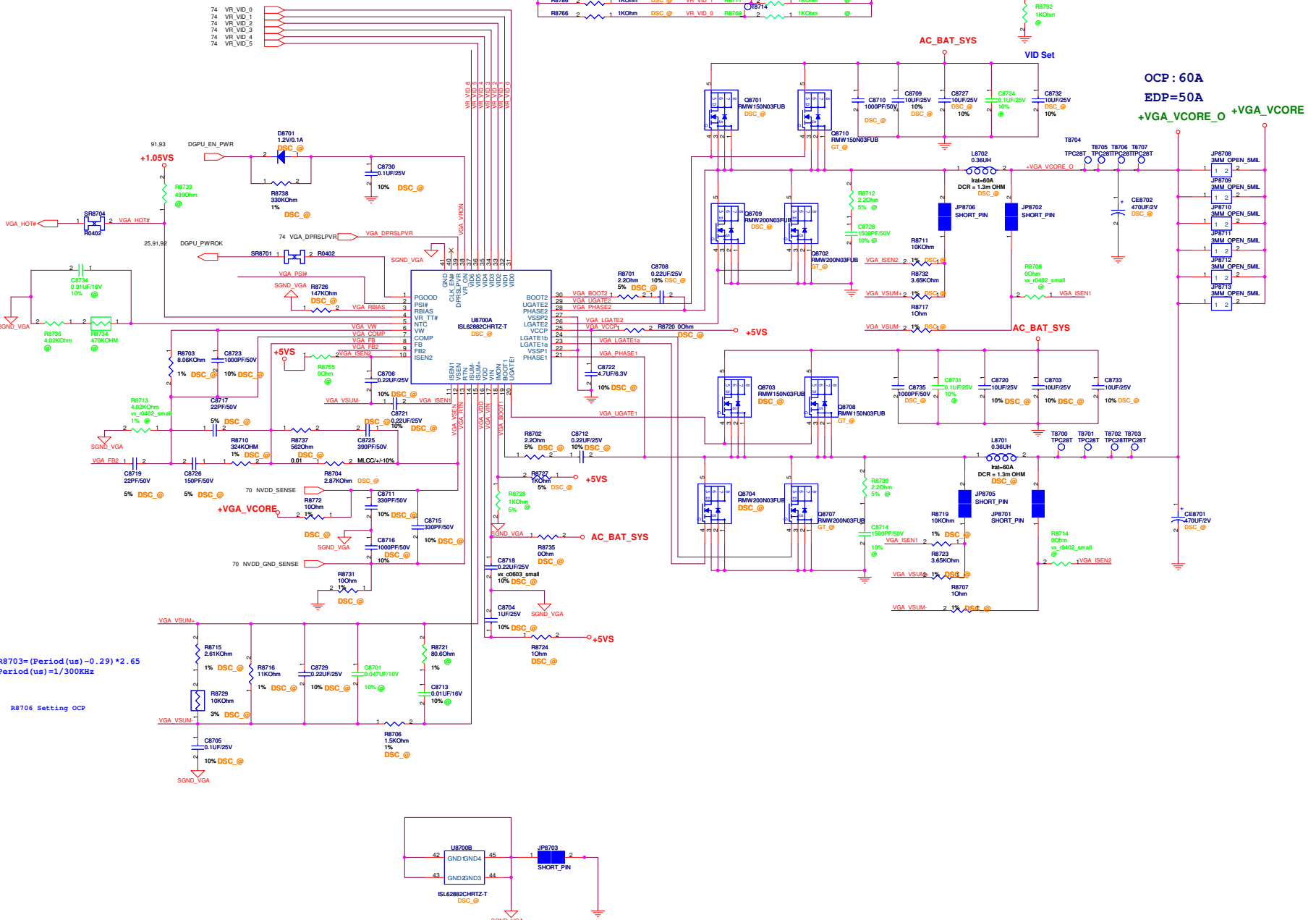
<Variant Name>		
PEGATRON		Title : POWER_
		Engineer: Steven Kuo
Size	Project Name	Rev
Custom	VA70	1.0
Date: Friday, February 03, 2012		Sheet 86 of 94

VGA_CORE POWER SUPPLY

VID Set 0.9V

+3VS_VGA

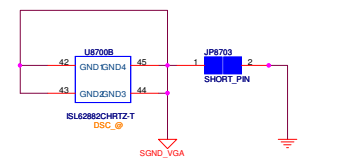
VGA_DPRSPLVVR	VGA_PSI#	VO_action
L	L	1 Phase CCM
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE



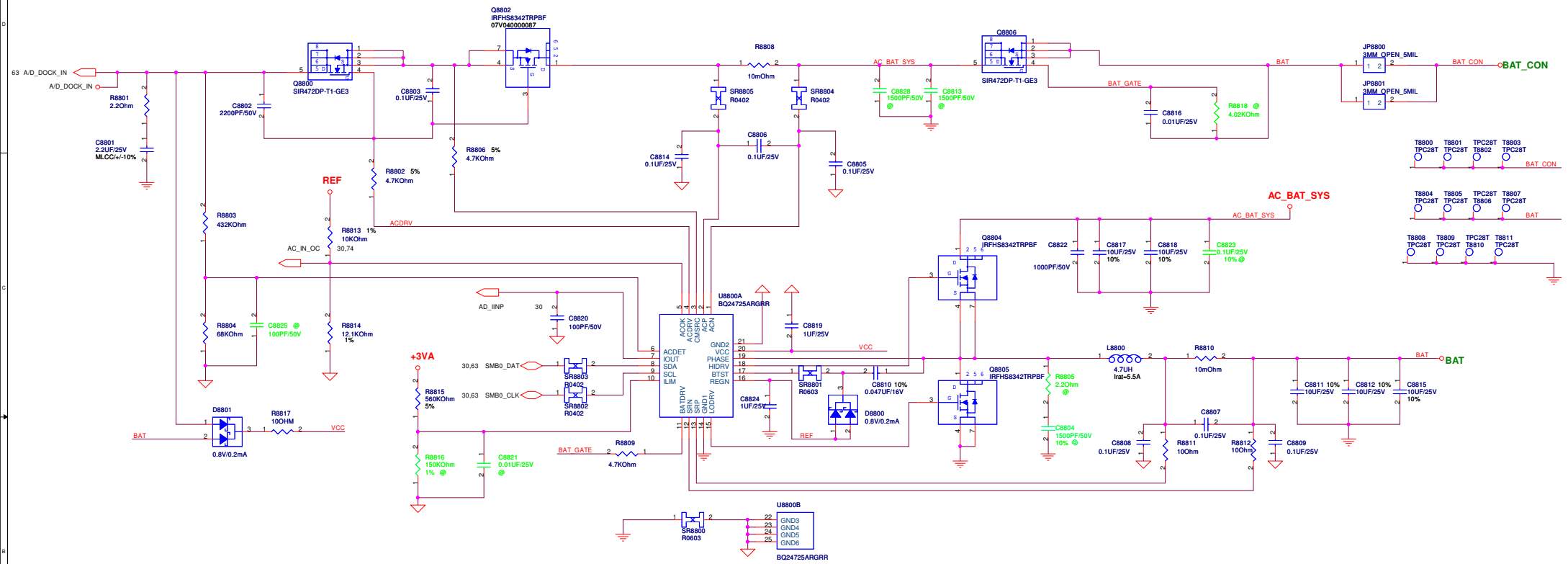
OCV : 60A
EDP=50A
+VGA_VCORE_O +VGA_VCORE

R8703=(Period(us)-0.29)*2.65
Period(us)=1/300KHz

R8706 Setting OCP



BATTERY CHARGER



5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>

PEGATRON Title : POWER_N/A		
Engineer:		
Size A	Project Name	Rev 1.1
Date: Friday, February 03, 2012	Sheet	89 of 99

5

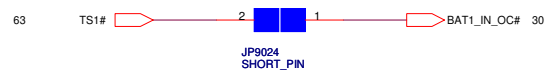
4

3

2

1

BATTERY IN DETECT

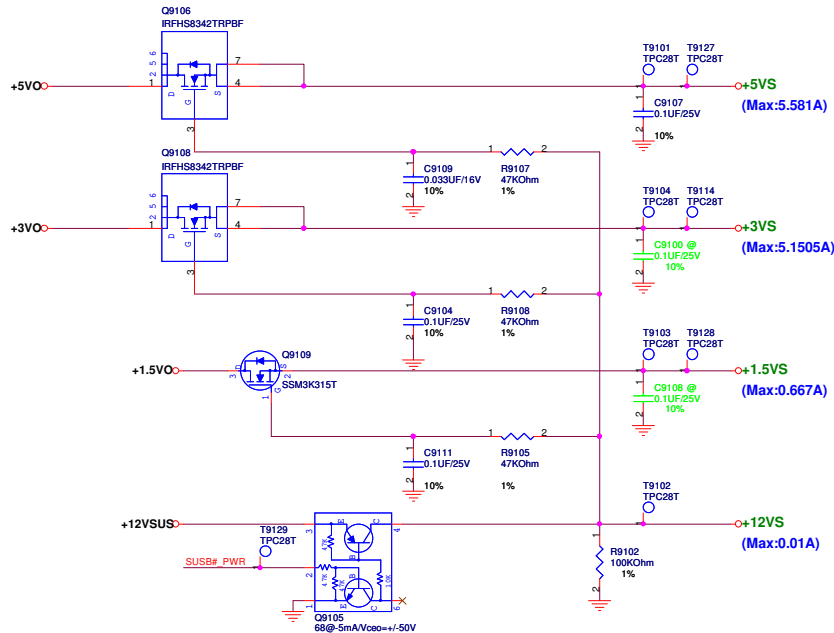


<Variant Name>

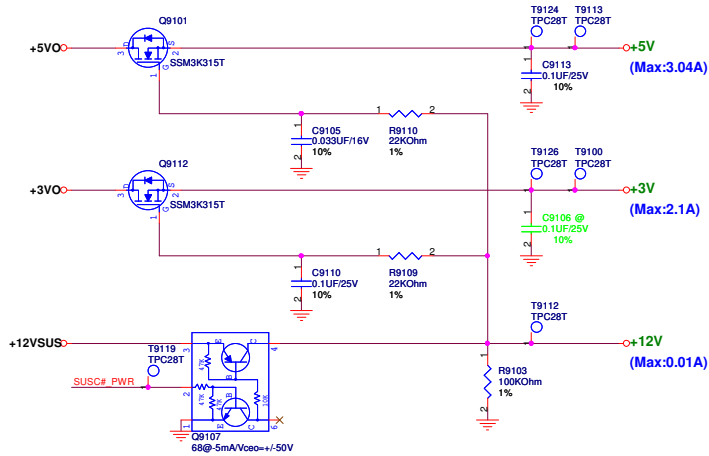
PEGATRON Title : **POWER_DETECT**
Engineer: *Steven Kuo*

Size	Project Name	Rev
Custom	VA70	1.0
Date: <i>Friday, February 03, 2012</i>		Sheet 90 of 99

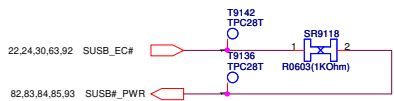
SUSB#_PWR POWER



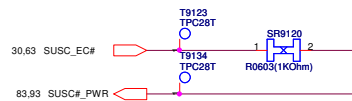
SUSC#_PWR POWER



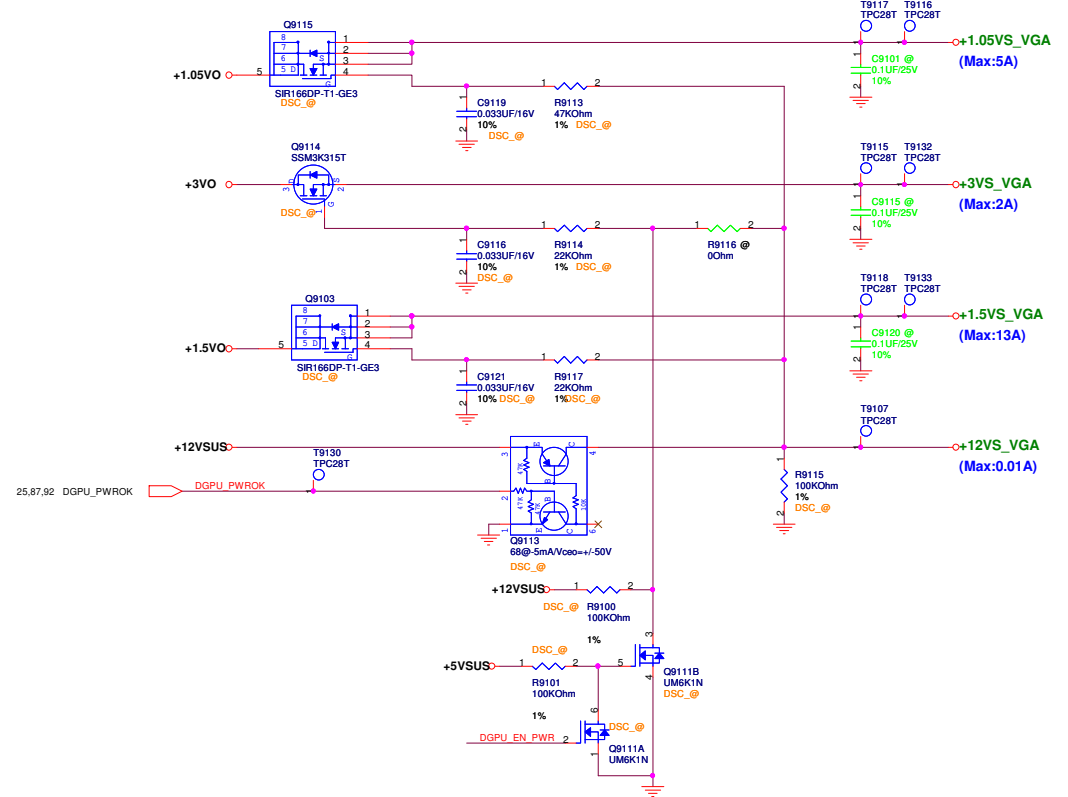
SUSB#_PWR POWER Control



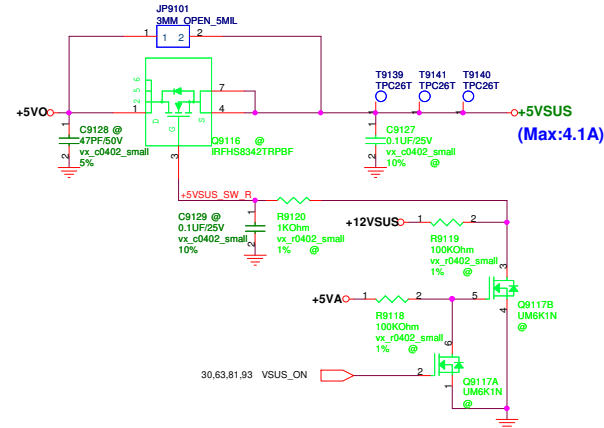
SUSC#_PWR POWER Control



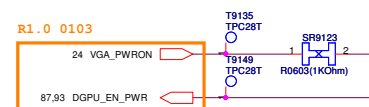
DSC#_PWR POWER(DGPU)



USBCHG#_PWR POWER

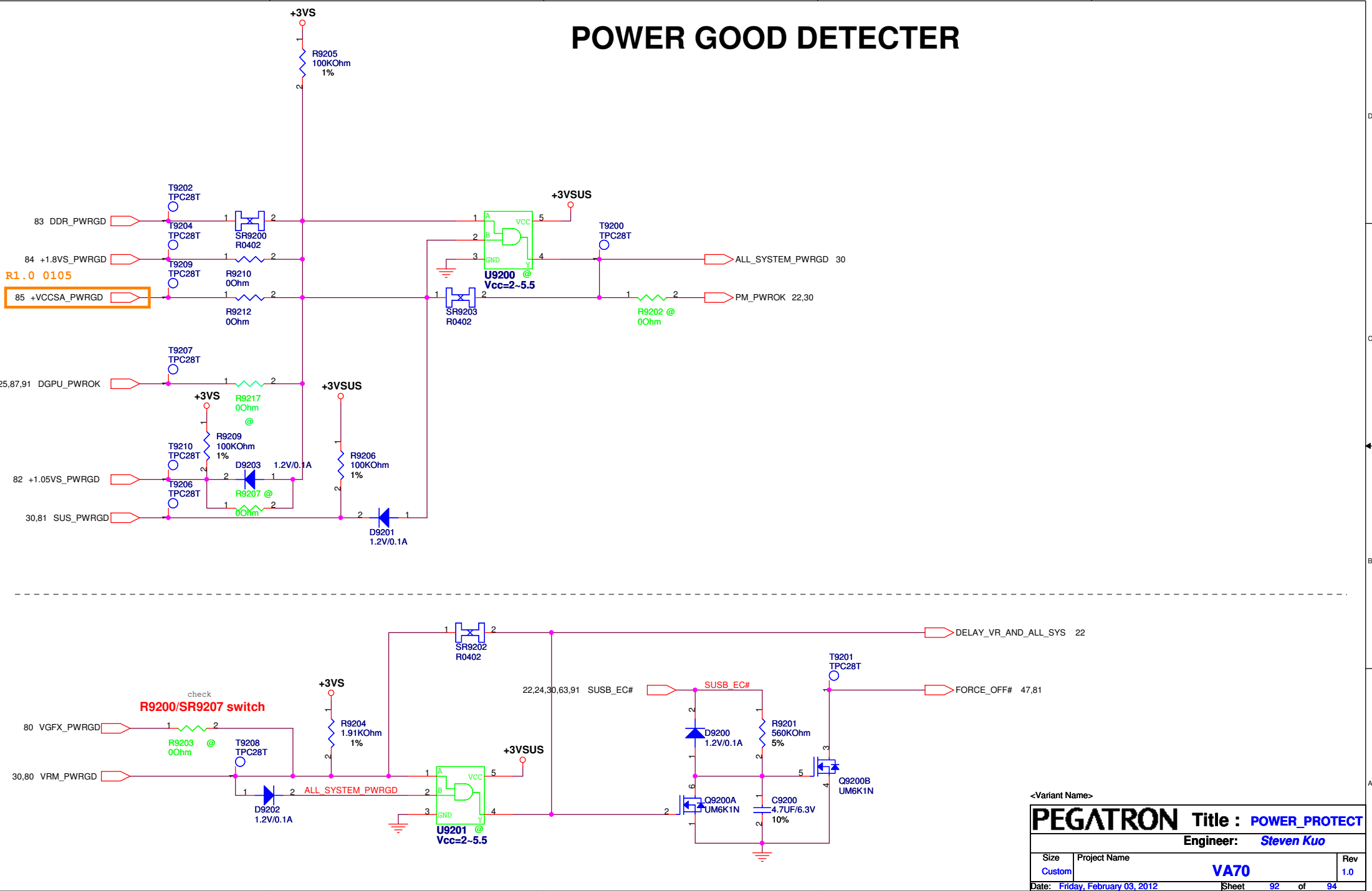


DSC_VGA_PWR POWER Control



Variant Name:		PEGATRON Title: POWER_LOAD SWITCH	
		Engineer: Steven Kuo	
Size	Project Name	VA70	Rev 1.0
Custom			
Date: Friday, February 03, 2012		Sheet 91 of 94	

POWER GOOD DETECTOR

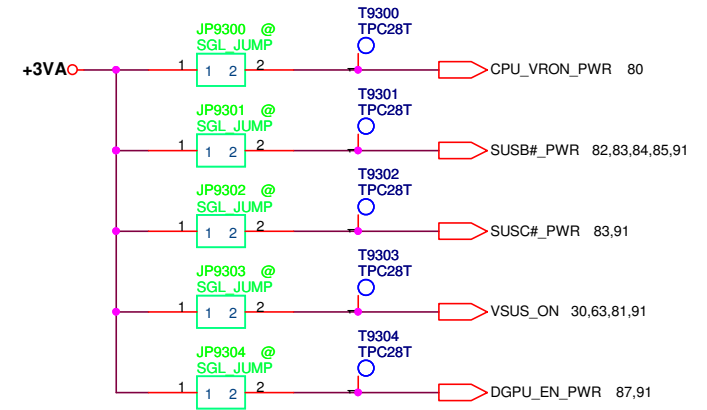


<Variant Name>

PEGATRON Title : POWER_PROTECT		
Engineer: Steven Kuo		
Size Custom	Project Name VA70	Rev 1.0
Date: Friday, February 03, 2012	Sheet 92 of 94	

AC_BAT_SYS	AC_BAT_SYS	37,55,80,81,82,83,87,88
BAT_CON	BAT_CON	63,88
+5VA	+5VA	30,42,61,66,81,91
+3VA	+3VA	20,27,30,48,63,65,81,88
+5VO	+5VO	61,81,91
+3VO	+3VO	55,81,91
+1.8VO	+1.8VO	84
+1.5VO	+1.5VO	83,91
+1.05VO	+1.05VO	82,91
+12VSUS	+12VSUS	22,28,60,81,91
+5VSUS	+5VSUS	22,27,30,60,61,63,65,66,82,83,84,85,91
+3VSUS	+3VSUS	4,22,24,27,28,30,33,65,81,85,92
+12V	+12V	91
+5V	+5V	51,63,91
+3V	+3V	4,24,37,51,63,65,91
+1.5V	+1.5V	5,7,16,51,63,83
+12VS	+12VS	28,39,41,91
+5VS	+5VS	27,30,38,39,41,42,48,49,60,63,66,80,87,91
+3VS	+3VS	4,16,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92
+1.8VS	+1.8VS	7,25,26,63,84
+1.5VS	+1.5VS	26,53,55,63,91
+1.05VS	+1.05VS	26,27,63,80,82,87
+0.75VS	+0.75VS	16,17,63,83
+VCCSA	+VCCSA	7,85
+VCCP	+VCCP	3,4,6,7,25,26,27,37,47,63,82
+12VS_VGA	+12VS_VGA	91
+3VS_VGA	+3VS_VGA	63,70,72,74,75,87,91
+1.5VS_VGA	+1.5VS_VGA	63,71,75,76,77,91
+1.05VS_VGA	+1.05VS_VGA	63,70,71,72,91
+VGA_VCORE	+VGA_VCORE	63,75,87
+VGFX_CORE	+VGFX_CORE	7,63,80
+VCORE	+VCORE	6,63,80

FOR POWER TEST



<Variant Name>

PEGATRON		Title : POWER_SIGNAL	
		Engineer: Steven Kuo	
Size	Project Name	A35	Rev
Custom			1.0
Date: Friday, February 03, 2012		Sheet 93 of 94	

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