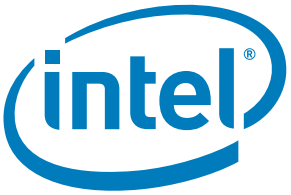


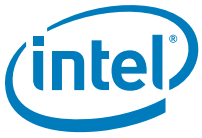
Intel® Pentium® and Celeron® Processor N- and J- Series

Datasheet - Volume 2 of 3

For Volume 1 of 3, refer to Document ID:334817
For Volume 3 of 3, refer to Document ID:334819

September 2016

Document Number: 334818-001



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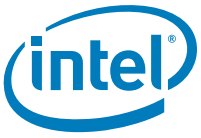

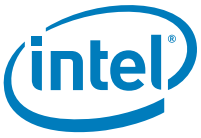

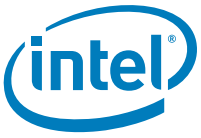

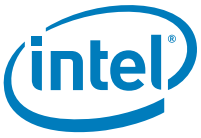

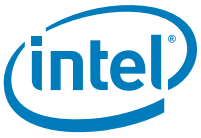

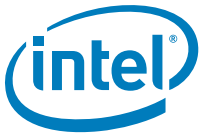

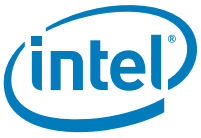

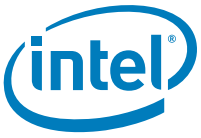

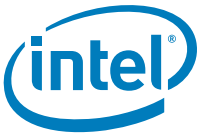

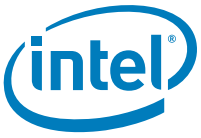

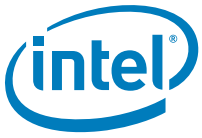

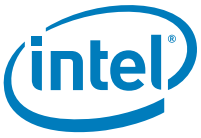

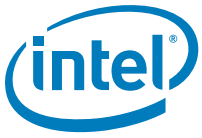

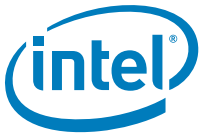

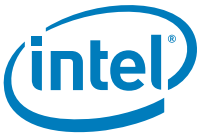

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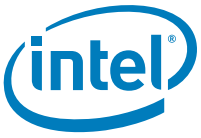

Revision History

Revision Number	Description	Revision Date
001	Initial Release	September 2016

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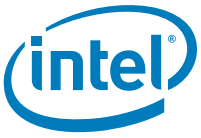
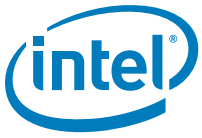




1 SoC Address Map

Note: Throughout this document Intel® Pentium® and Celeron® Processor N- and J- Series is referred as SoC.

Note: Throughout this document Intel® Pentium® and Celeron® Processor N- and J- Series processor families refers to:

- Intel® Pentium® N4200
- Intel® Pentium® J4205
- Intel® Celeron® N3350 and N3450
- Intel® Celeron® J3455 and J3355

1.1 Root Spaces

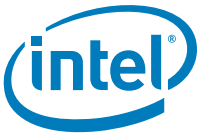
The SoC supports two root spaces: Host and CSE. Each root space contains an orthogonal address map. The Host address space is associated with the Atom CPUs. The CSE root space is associated with the CSE minute IA CPU.

Each root space supports an independent IA system. Within a given IA system (Host or CSE), the IA architecture defines several distinct address spaces that are accessible through different mechanisms. Some of these spaces have clean architectural definitions and others are less clean and overlap. It is not uncommon for a window in one address space to allow access to resources in another space. This is true both for address spaces within one root space (For example, a Host Memory Address Space window to Host PCI config space) and between Root spaces (For example, a CSE Memory Address Space window to DRAM that is also accessible from the Host Memory Space).

1.2 Super Set Architecture Definition

This Address MAP covers a super set of possible SoC configurations. Specifically, it refers to various address ranges that can be mapped to LPC or SPI. However, not all SoC instances will allow all of these configurations.

Note: The term “IAFW” is used throughout this document as a generic term for platform specific code that runs on the IA cores before the OS is loaded, often referred to as “BIOS”. The term “BIOS” is typically used for PC platforms, whereas mobile and Android* based platforms typically refer to IAFW.



1.3 References

Documents	Document Number
Intel® 64 and IA-32 Architectures Software Developer's Manuals Volume 1: Basic Architecture Volume 2A: Instruction Set Reference, A-M Volume 2B: Instruction Set Reference, N-Z Volume 3A: System Programming Guide Volume 3B: System Programming Guide	http://www.intel.com/products/processor/manuals/index.htm
Intel® Pentium® and Celeron® Processor N- and J- Series Specification Update	334820-001
Intel® Pentium® and Celeron® Processor N- and J- Series Volume 1 of 3	334817-001
Intel® Pentium® and Celeron® Processor N- and J- Series Volume 3 of 3	334819-001

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2 Host Root Space

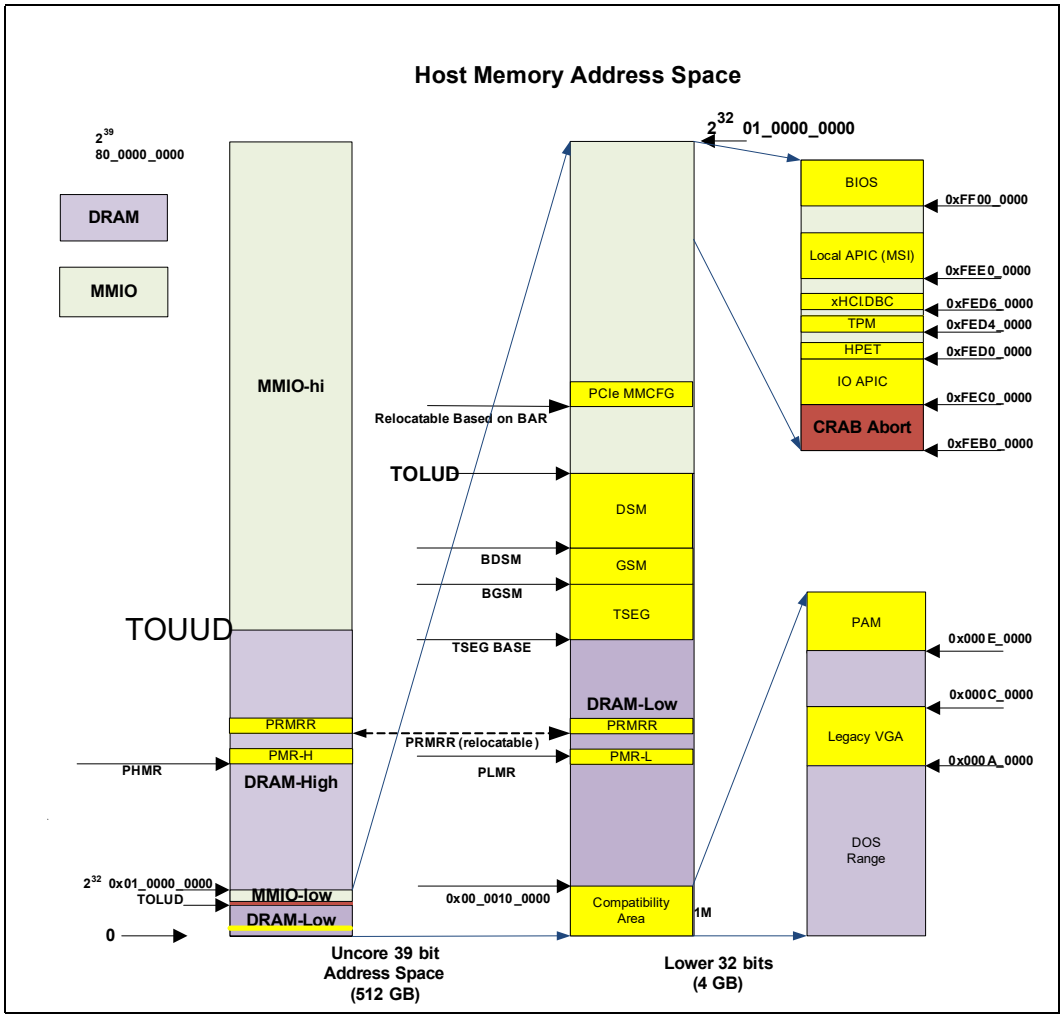
The following address spaces are available within the Host Root space:

- Memory
- I/O
- PCI Configuration
- Funny I/O
- IOSF SB Private CR space

2.1 Host Memory Address Space

The SoC implements 39 address bits providing 512 GiB of addressable memory space for use by the CPU and devices. This is the address space accessible by memory reads and writes and is the set of addresses as presented to the System Controllers or devices from either the CPU or devices. For PCI compliance the devices and IOSF fabric implement a full 64 b address space. Addresses greater than 512 GiB never address a physical resource in the SoC and are always terminated with an error.

Figure 2-1. Host Memory Address Map

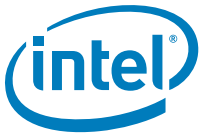


System DRAM memory is split into multiple independent architectural physical memory segments. In order to enable System DRAM to be addressed contiguously at the memory controller we define the “System DRAM address space”. A transformation is applied to the physical address to obtain the System DRAM address. Section 2.2, "System DRAM Address Space" provides details on Physical to System DRAM transformation. The SoC memory protection, security and coherency checks are performed on the Physical memory address before transformation.

VT-d adds the concept of Guest Physical Address or GPA and Host Physical address space or HPA. The Physical Address Space defined in this section corresponds to the HPA. A GPA is an un-translated address.

2.1.1 Host Memory Space Address Decode and Routing

Transactions in the Host Memory Space originate from two classes of sources: IDI attached and IOSF attached. These transactions must be routed, by address, to the appropriate resources. Address decode responsibilities are divided between the System



Agent and the IOSF fabric. This section will cover the details of System Agent address decode logic. The System Agent address decode logic is implemented in two parts. The B-Unit implements the majority of the address decode logic, with the A-Unit also implementing a first level address decode for upstream requests from IOSF.

The B-Unit system address decode logic will positively decode transactions to the following locations:

DRAM

- C-unit (Host Bridge functionality: Dev0 Fun0)
- SPI (BIOS, dTPM)
- LPC (BIOS, dTPM, misc non-standard ranges)
- CSE (BIOS and fTPM)
- Display
- I-Unit

Any transaction that arrives at the B-Unit from the A-Unit and is decoded to return to the A-Unit will be aborted. Transactions that are not positively decoded will be routed to PSF1.

The A-Unit system decode logic will positively decode upstream requests from IOSF agents as follows:

- Within MSI address range (0xFEEx_xxxx) ⇒ route to Tunit
- Within DRAM memory aperture ⇒ route to Bunit
- Otherwise ⇒ abort

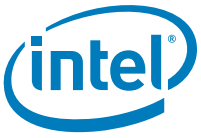
The Host memory address space is configurable. This document does not provide the detailed register definitions. This following table provides the names and a description of the primary registers used to control the memory configuration.

Table 2-1. Memory Map Configuration Registers

Register Name	Definition
TOUUD	Top of Upper Usable DRAM. Address above TOUUD target High MMIO. Address from 4 GiB up to TOUUD target DRAM.
TOLUD	Top of Low Usable DRAM. As a rule addresses below TOLUD target DRAM target DRAM and addresses between TOLUD and 4 GiB target devices in MMIO space. There are exceptions to the rule.
BDSM	Base of graphics Data Stolen Memory. A region used by the Integrated Graphics Device (IGD). BDSM specifies the base and TOLUD specifies the DSM region.
BGSM	Base of Graphics Stolen Memory. A region used by the IGD. BGSM specifies the base, and BDMS specifies the limit of the GSM region.
TSEGMB	T segment Memory Base. The region used for SMM protected DRAM. TSEGMB specifies the base, and BGSM specifies the limit.
BMISC	Contains fields for enabling various legacy regions including VGA and the BIOS PAM regions.

2.1.2 Abort Handling

The term “abort” is used in this document to handle a few different error handling mechanisms.



2.1.2.1 B-Unit Abort Handling

Non-posted Transactions that are aborted in the B-Unit will have a completion returned: to the IDI originator with bogus data (all '1's), to IOSF agents the completion is a UR with no data. Posted transactions that are aborted in the B-Unit are dropped without altering the contents of system memory. Depending on the reason for the abort, the B-Unit will follow different error logging behaviors.

2.1.2.2 IOSF Abort Handling

Transactions routed to IOSF will be aborted in the fabric or in the P2SB. Non-posted transactions are completed with a UR completion. The A-Unit converts the zero-length UR completion into a completion with all '1's. Posted transactions that are aborted are dropped. Error handling in the IOSF fabric follows the rules of the IOSF fabric and if errors are detected in the fabric the error message is sent to the ITSS error collector logic over sideband.

2.1.3 Low DRAM Address Range (0 to (TOLUD - 1)

As a rule all addresses from 0 to Top of Low Usable DRAM (TOLUD - 1) are routed to DRAM. There are exceptions to this rule. The following sub sections describe the exceptions to the rule.

Table 2-2. Low DRAM Default Address Decode Rule

Name	Low DRAM
Range	0 to (TOLUD – 1)
From IDI	DRAM, unless a specific rule supersedes this rule.
From IOSF	DRAM, unless a specific rule supersedes this rule.
Security	IMR ranges are SAI protected.

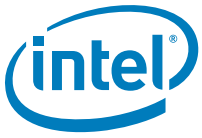
2.1.3.1 Legacy Video Area (A_0000h to B_FFFFh)

The legacy 128 KiB VGA memory range, (000A_0000h to 000B_FFFFh, also known as ASEG and BSEG) can be mapped to IGD or to a PCIe root port; the mapping is configured in the B-Unit BMISC register. The appropriate mapping depends on which devices are enabled and the programming of the VGA steering bits. If the VGA region is enabled and the transactions are not targeting the IGD, then they will be routed to the PCIe root port with the VGA enable bit of the bridge control register set.

The VGA range can be divided into three sub-ranges. Each range is either routed to the IGD or a PCIe root port based on the steering bits.

The following conditions are used to determine where to route addresses within this range:

- ABSegInDRAM:
  BMISC.ABSegInDRAM = 1
- IGDEnabled:
  (0.0.0.PCI.DEVEN.D2F0EN = 1)
  AND (0.2.0.PCI.PMCSR.PSRSTAT = 2'b00)
  AND (0.2.0.PCI.PCICMD2.MAE = 1)



- VGAAtoIGD:
  ((VGAAtoIGD1 = 1) OR (VGAAtoIGD2 = 1))
- VGAAtoIGD1:
  (GGC.GGMS ≠ 5'b00000)
  AND (GGC.IVD = 0)
  AND (VGADEC.VGAMSR1 = 1)
  AND (VGADEC.VGAGR10 = 1)
- VGAAtoIGD2:
  (!VGAAtoIGD1)
  AND ((VGADEC.VGAGR6 = 2'b00) OR (VGADEC.VGAGR6 = 2'b01))
- MDAtoIGD:
  (!VGAAtoIGD1)
  AND (VGADEC.VGAGR6 = 2'b10)
- VGABtoIGD:
  (!VGAAtoIGD1)
  AND (VGADEC.VGAGR6 = 2'b11)

Table 2-3. Legacy VGA A

Name	VGA A
Range	0xA_0000 to 0xA_FFFF

From IDI	IF (ABSegInDRAM)
	Route to DRAM
	ELSE IF (IGDEnabled and VGAAtoIGD)
	Route to Display
	ELSE
	Route to PSF1

From IOSF	IF (ABSegInDRAM)
	Route to DRAM
	ELSE
	Abort: Send to System Agent.
	
	Note: No A-Unit decode is required for this range.

Security	No restrictions

Table 2-4. Legacy MDA (Sheet 1 of 2)

Name	MDA (Monochrome Display Adaptor)
Range	0xB_0000 to 0xB_7FFF

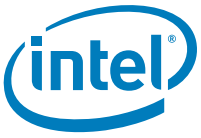


Table 2-4. Legacy MDA (Sheet 2 of 2)

Name	MDA (Monochrome Display Adaptor)

From IDI	IF (ABSegInDRAM)
	  Route to DRAM
	ELSE IF (IGDEnabled and MDAtoIGD)
	  Route to Display
	ELSE
	  Route to PSF1

From IOSF	IF (ABSegInDRAM)
	  Route to DRAM
	ELSE
	  Abort: Send to System agent.
	
	Note: No A-Unit decode is required for this range.

Security	No restrictions

Table 2-5. Legacy VGA B

Name	VGA B
Range	0xB_8000 to 0xB_FFFF

From IDI	IF (ABSegInDRAM)
	  Route to DRAM
	ELSE IF (IGDEnabled and VGABtoIGD)
	  Route to Display
	ELSE
	  Route to PSF1

From IOSF	IF (ABSegInDRAM)
	  Route to DRAM
	ELSE
	  Abort: Send to System agent.
	
	Note: No A-Unit decode is required for this range.

Security	No restrictions

2.1.3.1.1 Legacy VGA and Compatible Mode SMM

The SoC does not support legacy SMM usage of the VGA range.

2.1.3.2 Expansion Area (C_0000h to D_FFFFh)

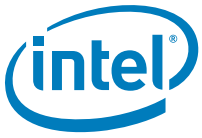
The SoC does not Support the ISA Expansion region. This area always maps to system DRAM.

2.1.3.3 PAM Memory Area (E_0000h to F_FFFFh)

The SoC does NOT support the PAM regions. The PAM Memory Area has historically been used for accessing IAFW code from flash.

ISA Hole (15 MiB to 16 MiB)

The SoC Does **NOT** support the ISA Hole Feature. This range is always mapped to DRAM.



2.1.3.4 Protected Memory Range (PMR-L: Programmable)

VT-d defines a protected memory range. This range is re-locatable. This range must be protected by IMRs to ensure only the IA core has access to this range before VT-d translation is enabled.

There is one range per VT-d engine. So the SoC has two PMR-L ranges.

In addition to PMR-L (below 4 GiB) there is a PMR-H above 4 GiB with the same access restrictions.

Table 2-6. PMR-L

Name	PMR-L
Range	0.0.0.DefVTdBAR.PMRLBASE to 0.0.0DefVTdBAR.PMRLLIMIT and 0.0.0.GfxVTdBAR.PMRLBASE to 0.0.0GfxVTdBAR.PMRLLIMIT
From IDI	DRAM
From IOSF	DRAM or ABORT (based on security)
Security	GT has a copy of GfxVTd PMR. It will make sure that only VT-d walks are allowed to touch PMR and hence get onto IDI. Other tnx that hit PMR are killed before they get onto IDI. Display will add GfxVTd PMR. It will make sure that only VTd walks are allowed to go to PMR range and all other tnx will be killed before they get onto IOSF primary. DefVTd PMR will be implemented in Bunit.

2.1.3.5 DMA Protected Range (DPR: Programmable)

The SoC Address map does not support DPR. This range is used in big core systems as part of the TXT security model.

2.1.3.6 TSEG SMM Range (Programmable)

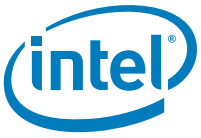
This range is set up by IAFW and must match the range specified for SMM in the core MSRs. TSEGMB is the base of the range, and the limit is defined by BGSM (Bottom of Graphics Stolen Memory). This range is SAI protected and only transactions originating in SMM mode from the IA cores are allowed access. See Section 2.3, "System Management Mode (SMM)" for further discussion on SMM and access restrictions.

Table 2-7. TSEG

Name	TSEG
Range	0.0.0.TSEGMB to (0.0.0.BGSM - 1)
From IDI	DRAM or ABORT
From IOSF	DRAM or ABORT (Abort if enabled by SAI check)
Security	SAI protected.

2.1.3.7 Graphics Stolen Memory (Programmable)

The base of graphics stolen memory is defined by BGSM (Base of Graphics Stolen Memory). The limit is defined by TOLUD. This region is SAI protected and only Display and GT are allowed access.



The IGD further subdivides this range, however outside of the IGD the access protections are the same and the system is not aware of the further sub-division. These divisions include a Data segment and a PCM segment. The enforcement of access restrictions within GSM to the data segment or the PCM segment is the responsibility of the GT logic and Display.

Table 2-8. GSM

Name	GSM
Range	0.0.0.MCHBAR.BGSM to (0.0.0.MCHBAR.TOLUD - 1)
From IDI	DRAM or ABORT
From IOSF	DRAM or ABORT
Security	SAI protected.

2.1.4 Low MMIO Address Range (TOLUD to 4 GiB)

This address range, from BUNIT.BMBOUND to 4 GiB is primarily used for devices in MMIO space. Section 2.1.6, "High MMIO Address Range (TOUUD to 0x7F_FFFF_FFFF)" provides a summary of all legacy fixed and programmable MMIO address ranges in the SoC.

Root complex integrated PCI devices have memory space BARs that can be configured to claim memory within this region. Root Ports (PCIe or Mobile Express) have Base and limit range registers that can be configured to claim memory within this region. IAFW and the OS ensure that the PCI BARs are not programmed to overlap with any of the legacy address ranges.

Table 2-9. Low MMIO Address Range

Name	Low MMIO
Range	0.0.0.MCHBAR.TOLUD to 0xFFFF_FFFF
From IDI	PSF1 on VC0b, unless a specific rule supersedes this rule.

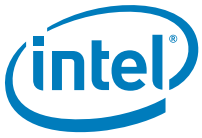
From IOSF	IF (VC0a)
	PSF1 on VC0b, unless a specific rule supersedes this rule.
	ELSE IF (VC0b)
	Abort, Send to system agent, unless a specific rule supersedes this rule.
	ELSE

Security	No restrictions, unless a specific rule supersedes this rule.

2.1.4.1 PCIe Memory Mapped Config Range (Programmable)

A 256 MiB range used to access PCI configuration registers. See Section 2.5.1.2, "PCI Express Enhanced Configuration Mechanism".

Note: A fixed PCI config MM space of 256 MiB is overkill and would waste DRAM space on a 32 b (4 GiB) system. Ideally the MM window would be configurable to match the needs of the system and minimize DRAM waste. This needs to be investigated for future derivatives.



The System Agent is responsible for converting the transactions to PCI config transactions. The B-Unit does some address decode of PCI config space, but most transactions are forwarded subtractively to PSF1 and the IOSF fabric is responsible for decode.

Note: When I-Unit is configured as a "child of graphics", the I-Unit PCI config space will be disabled and configuration transactions to B/D/F 0/3/0 will be routed to the IOSF fabric and aborted.

Table 2-10. PCIe MMCFG

Name	PCIeMMCFG
Range	BAR: 0.0.0.MCHBAR.PCIEXBAR (size 256 MiB)

From IDI	IF (0.0.0.MCHBAR.PCIEXBAR.ECEnable = 1)
	  Convert to PCI configuration cycle
	
	IF (B/D/F = 0/0/0)
	  C-unit on VC0b
	ELSE IF ((B/D/F = 0/2/0) AND (DEVEN.D2F0EN))
	  Display on VC0a
	ELSE IF ((B/D/F = 0/3/0) AND (DEVEN.D3F0EN))
	  I-Unit on VC0a
	ELSE
	  PSF1

From IOSF	Default (see Low MMIO range)
Security	GT is not allowed to access this range. If GT does attempt access the transaction is forwarded to IOSF as a Memory transaction.

2.1.4.2 Host Bridge

The host bridge located at Bus0, Dev0, Fn0 contains three non-standard BARs. MCHBAR is defined in a PCI configuration register. The Two VTd BARs are MMIO registers in the MCHBAR range. Each of these BARs has an enable bit. If the BAR is not enabled, the address decoder should ignore the value programmed in the upper bits of the BAR.

MCHBAR is the BAR for all System Agent memory mapped registers. Transactions are routed on IOSF primary to the C-unit and from the C-unit they are distributed as needed on IOSF SB.

The A-Unit TAD should not decode for MCHBAR, DefVTDBAR or GFxVTdBAR. This will prevent P2P transactions from VC0a targeting the C-unit. These 3 BARs are source decoded by B-Unit.

Table 2-11. MCHBAR (Sheet 1 of 2)

Name	MCHBAR
Range	BAR: 0.0.0.PCI.MCHBAR size (32 KiB)

Table 2-11. MCHBAR (Sheet 2 of 2)

Name	MCHBAR

From IDI	IF (0.0.0.PCI.MCHBAR.MCHBAREnable = 1)
	C-unit
	ELSE

From IOSF	Default (see Low MMIO range)
Security	B-Unit

The Default VTd BAR is the BAR for the Default IOMMU memory mapped registers. Transactions are routed on IOSF primary to the C-unit. The C-unit forwards the transaction to the Default IOMMU on IOSF SB.

Table 2-12. Default VTd BAR

Name	DefVTdBAR
Range	BAR: 0.0.0.MCHBAR.DefVTdBAR (4 KiB)

From IDI	IF (0.0.0.PCI.DefVTdBAR.DefVtdBAREnable = 1)
	C-unit
	ELSE

From IOSF	Default (see Low MMIO range)
Security	No restrictions.

The Graphics VTd BAR is the BAR for the Graphics IOMMU memory mapped registers. Transactions are routed on IOSF primary to Display.

Although this is a dev0 owned memory BAR, the registers live in dev2 and dev2 must be enabled to access this memory range.

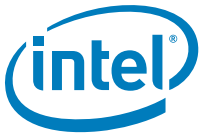
- IGDEnabled:
  (0.0.0.PCI.DEVEN.D2F0EN = 1)
  AND (0.2.0.PCI.PMCSR.PSRSTAT = 2'b00)
  AND (0.2.0.PCI.PCICMD2.MAE = 1)

Table 2-13. Graphics VTd BAR

Name	GfxVTdBAR
Range	BAR: 0.0.0.MCHBAR.GfxVTdBAR (4 KiB)

From IDI	IF (0.0.0.MCHBAR.GFxVTdBAR.VtdBAREnable = 1) && IGDEnabled
	Display
	ELSE

From IOSF	Default (see Low MMIO range)
Security	No restrictions.



2.1.4.3 Integrated Graphics Device (IGD)

Notes:

1. The IGD BARs are not restricted to Low MMIO space and could be programmed in High MMIO space.
2. The Integrated graphics device has two Host Memory Space BARs. These are standard PCI BARs.
3. Address decode to these BARs are valid if the Integrated Graphics device is enabled and system software has enabled the Memory Access to the device:

- IGDEnabled:
  (0.0.0.PCI.DEVEN.D2F0EN = 1)
  AND (0.2.0.PCI.PMCSR.PSRSTAT = 2'b00)
  AND (0.2.0.PCI.PCICMD2.MAE = 1)
- MCHBARAlias:
  offsets 0x14_0000 to 0x14_7FFF from GTTMADDR BASE

The registers in the IGD that live behind the GTTMMADR BAR are accessible in three ways:

- By IA or peer transactions through the MMIO BAR described in Section 2.4.2.1, "Integrated Graphics Device (IGD)")
- By GT using Funny I/O transactions (see Section 2.6, "Funny I/O Space")
- By IA using an I/O BAR. (see Section 2.1.4.3, "Integrated Graphics Device (IGD)")

Table 2-14. GTTMMADR

Name	GTTMMADR
Range	BAR: 0.2.0.PCI.GTTMMADR (16 MiB)

From IDI	IF (IGDEnabled)
	IF (MCHBARAlias and Read)
	Cunit
	ELSE IF (MCHBARAlias and Write)
	Abort
	ELSE
	Display
	ELSE

From IOSF	IF (VC0a)
	PSF1
	ELSE IF (VC0b and IGDEnabled)
	Display
	ELSE

Security	No Restrictions.

Table 2-15. GMADR (Sheet 1 of 2)

Name	GMADR
Range	BAR: 0.2.0.PCI.GMADR (re-sizeable by 0.2.0.PCI.MSAC 128 MiB to 4 GiB)

Table 2-15. GMADR (Sheet 2 of 2)

Name	GMADR

From IDI	IF (IGDEnabled)
	Display
	ELSE

From IOSF	Default (see Low MMIO range)
Security	No restrictions.

2.1.4.4 I-Unit

The I-Unit contains one standard PCI BAR.

Note: The I-Unit BARs are not restricted to Low MMIO space and could be programmed in High MMIO space.

Table 2-16. I-Unit BAR

Name	IBAR
Range	BAR: 0.3.0.PCI.IBAR (16 MiB)

From IDI	IF ((0.0.0.PCI.DEVEN.D3F0EN = 1)
	AND (0.3.0.PCI.PMCSR.PSRSTAT = 2'b00)
	AND (0.3.0.PCI.PCICMD2.MAE = 1))
	I-Unit
	ELSE
	Default (See Low MMIO Range)

From IOSF	Default (see Low MMIO range)
Security	No restrictions.

2.1.4.5 LPC Generic Memory Range

The LPC logic has a non-standard memory range. The system agent performs source decoding on this range. The destination is LPC. If the SoC has no LPC, then these ranges are n/a.

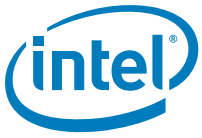
LPC Generic Memory Range. Enable via setting bit[0] of the LPC Generic Memory Range register (D31:F0:offset 98h).

Table 2-17. LPC Generic Memory Range

Name	LPC Generic Memory Range
Range	BAR: 0.31.0.PCI.LGMR (offset 98h)

From IDI	IF (0.31.0.PCI.LGMR.bit0 = 1)
	IF (LPC enabled)
	LPC
	ELSE
	Default (See Low MMIO Range)
	ELSE

From IOSF	Default (see Low MMIO range)
Security	No restrictions.



2.1.4.6 CRAB_ABORT (0xFEB0_0000 to 0xFEBF_FFFF)

The CPU will re-map various access violations to target the CRAB_ABORT page.

Table 2-18. CRAB_ABORT

Name	CRAB ABORT
Range	0xFEB0_0000 to 0xFEBF_FFFF
From IDI	Abort
From IOSF	Abort—Route to B-Unit no decode required in A-Unit
Security	No restrictions.

2.1.4.7 IOAPIC (0xFEC0_0000 to 0xFECF_FFFF)

The IOAPIC has a small MMIO window that is located at 0xFECX_X000-FECX_X040. IAFW configures the exact location using the APIC Range Select (ASEL) field and APIC Enable (AEN) bit. For the SoC only ASEL programming placing the range at 0xFEC0_0000 to 0xFEC0_0040 will be validated.

Table 2-19. IOAPIC

Name	IOAPIC
Range	0xFECX_X000 to 0xFECX_X040
From IDI	Subtractive to PSF1
From IOSF	Default (see Low MMIO range)
Security	No restrictions.

2.1.4.8 HPET (0xFED0_0000 – 0xFED0_33FF)

IAFW can configure the HPET timers to be located at one of four locations: 0xFED0_X000 to 0xFED0_X3FF where X = {0, 1, 2, or 3}. For the SoC we will only validate with X = 0.

Table 2-20. HPET

Name	HPET
Range	0xFFD0_X000 to 0xFED0_X3FF (X = {0, 1, 2, or 3})
From IDI	PSF1
From IOSF	Default (see Low MMIO range)
Security	No restrictions.

2.1.4.9 TPM (0xFED4_0000 to 0xFED4_0FFF)

The range from 0xFED4_0000 to 0xFED4_0FFF is reserved for use by the TPM. The location of the TPM is determined by a strap and transactions to this address are routed towards the TPM (CSE, SPI or LPC).

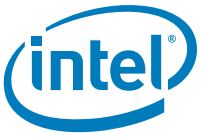


Table 2-21. TPM locality 0

Name	TPM
Range	0xFED4_0000 to 0xFED4_0FFF

From IDI	IF (TPM at CSE)
	  CSE
	ELSE IF (TPM_at_LPC)
	  LPC
	ELSE
	  PSF error handler.

From IOSF	Default (see Low MMIO range)
Security	No restrictions.

2.1.4.10 TXT (0xFED2_0000 to 0xFED3_FFFF)

The range from 0xFED2_0000 to 0xFED3_FFFF is the TXT public and private ranges. This range is not used on the SoC and is aborted in the system agent.

Table 2-22. TPM Locality 1-3

Name	TPM
Range	0xFED2_0000 to 0xFED3_FFFF
From IDI	Abort
From IOSF	Default (see Low MMIO range)
Security	Always aborted

2.1.4.11 TPM (0xFED4_1000 to 0xFED4_3FFF)

The range from 0xFED4_1000 to 0xFED4_3FFF is the TPM locality 1 to 3 range. These are not used on the SoC and are aborted in the system agent.

Table 2-23. TPM Locality 1-3

Name	TPM
Range	0xFED4_1000 to 0xFED4_3FFF
From IDI	Abort
From IOSF	Default (see Low MMIO range)
Security	Always aborted

2.1.4.12 xHCI.DBC (0xFED6_0000 to 0xFED6_0FFF)

The range from 0xFED6_0000 to 0xFED6_0FFF is reserved for P2P traffic targeting the xHCI DBC endpoint. The OS must be informed that this address range is reserved, and no other MMIO address should overlap with this range. There is not address decode awareness of this address range. Addresses in this range must use source decode on the PSF fabric. A transaction in this range without source decode will be subtractively aborted.

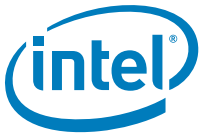


Table 2-24. xHCI.DBC

Name	TPM
Range	0xFED6_0000 to 0xFED6_0FFF
From IDI	Default (see Low MMIO range)
From IOSF	Default (see Low MMIO range)
Security	Always aborted

2.1.4.13 Local APIC (0xFEE0_0000 to 0xFEEF_FFFF)

The range from 0xFEE0_0000 to 0xFEEF_FFFF is reserved signaling interrupts to the local APICs inside the CPU cores. Accesses to this range from I/O devices are routed upstream to the cores.

Table 2-25. IOAPIC

Name	Local APIC
Range	0xFEE0_0000 to 0xFEEF_FFFF
From IDI	Subtractive to PSF1
From IOSF	T-Unit
Security	No requirements

2.1.4.14 IAFW (BIOS) (0xFFXX_0000 to 0xFFFF_FFFF)

The range of memory at the top of Low MMIO is used to access IAFW (aka BIOS) during boot. The size of this range is configurable from 256 KiB to 16 MiB. The range is always aligned to end at 4 GiB - 1. The first instruction fetch after reset targets address 0xFFFF_FFF0.

The on die SRAM size is limited to 256 KiB. When booting from LPC or SPI, the controls to configure the size of the region are in either the BIOS Decode Register in LPC or SPI (depending on which is enabled).

The IAFW region can be mapped to one of three physical locations: CSE SRAM, LPC, or SPI flash.

- BIOSinSRAM
- BIOSinLPC
- BIOSinSPI

The IAFW range is broken into four sub-ranges. BIOS1 always is used for BIOS. BIOS2, BIOS3 and BIOS4 may be used for BIOS or may be used as default MMIO addresses.

The BIOS3 and BIOS4 range is controlled by the BDE (BIOS Decode Enable) register. When LPC is enabled the system agent should use the LPC BDE register. When SPI is enabled the LPC should use the SPI BDE register.

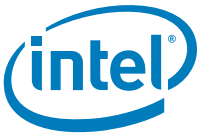


Table 2-26. BIOS1

Name	BIOS
Range	0xFFFC_0000 to 0xFFFF_FFFF

From IDI	IF (BIOSinLPC)
	  LPC
	ELSE IF (BIOSinSPI)
	  SPI
	ELSE
	  CSE SRAM (note use IOSF DestID for CSE)

From IOSF	Default (see Low MMIO range)
Security	Perform SAI Completion check in system agent. Perform SAI check at CSE SRAM.

Table 2-27. BIOS2

Name	BIOS2
Range	0xFFF8_0000 to 0xFFFB_FFFF

From IDI	IF (BIOSinLPC)
	  LPC
	ELSE IF (BIOSinSPI)
	  SPI
	ELSE
	  PSF1

From IOSF	Default (see Low MMIO range)
Security	No Requirements

Table 2-28. BIOS3

Name	BIOS3
Range	0xFF80_0000 to 0xFFF7_FFFF

From IDI	IF (BIOSinLPC AND (BDE[14:8] = 7'b111_1111))
	  LPC
	ELSE IF (BIOSinSPI AND (BDE[14:8] = 7'b111_1111))
	  SPI
	ELSE
	  PSF1

From IOSF	Default (see Low MMIO range)
Security	No requirements.

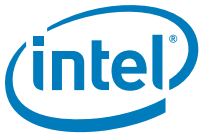


Table 2-29. BIOS4

Name	BIOS4
Range	0xFF00_0000 to 0xFF7F_FFFF

From IDI	IF (BIOSinLPC AND (BDE[3:0] = 4'b1111))
	LPC
	ELSE IF (BIOSinSPI AND (BDE[3:0] = 4'b1111))
	SPI
	ELSE
	PSF1

From IOSF	Default (see Low MMIO range)
Security	No requirements.

2.1.4.14.1 BIOS Decode Enable Register Restrictions

To simplify the decoder in the B-Unit we restricting the legal programming of BDE.

BDE[14:8] must be set or cleared together. This creates one region from 0xFF80_0000 to 0xFFF7_FFFF (7.5 MiB in size).

- BDE[3:0] must be set or cleared together. This creates one 8 MiB range from 0xFF00_0000 to 0xFF7F_FFFF.

Base	Limit	Enable
0xFFF8_0000	0xFFFB_FFFF	
0xFFF0_0000	0xFFF7_FFFF	bde[14]
0xFFE8_0000	0xFFEF_FFFF	bde[13]
0xFFE0_0000	0xFFE7_FFFF	bde[12]
0xFFD8_0000	0xFFDF_FFFF	bde[11]
0xFFD0_0000	0xFFD7_FFFF	bde[10]
0xFFC8_0000	0xFFCF_FFFF	bde[9]
0xFFC0_0000	0xFFC7_FFFF	bde[8]
0xFFB8_0000	0xFFBF_FFFF	
0xFFB0_0000	0xFFB7_FFFF	bde[14]
0xFFA8_0000	0xFFAF_FFFF	bde[13]
0xFFA0_0000	0xFFA7_FFFF	bde[12]
0xFF98_0000	0xFF9F_FFFF	bde[11]
0xFF90_0000	0xFF97_FFFF	bde[10]
0xFF88_0000	0xFF8F_FFFF	bde[9]
0xFF80_0000	0xFF87_FFFF	bde[8]
0xFF70_0000	0xFF7F_FFFF	bde[3]
0xFF60_0000	0xFF6F_FFFF	bde[2]
0xFF50_0000	0xFF5F_FFFF	bde[1]
0xFF40_0000	0xFF4F_FFFF	bde[0]
0xFF30_0000	0xFF3F_FFFF	bde[3]

Base	Limit	Enable
0xFF20_0000	0xFF2F_FFFF	bde[2]
0xFF10_0000	0xFF1F_FFFF	bde[1]
0xFF00_0000	0xFF0F_FFFF	bde[0]

2.1.5 High DRAM (0x1_0000_0000 to (TOUUD - 1))

The range from 4 GiB (1_0000_0000h) to (TOUUD - 1) is mapped to DRAM. When there is no DRAM above 4 GiB, TOUUD may be programmed to a value below 4 GiB. In that case this range is effectively disabled.

Table 2-30. High DRAM

Name	Mapping
Range	0x1_0000_0000 to (TOUUD - 1)
From IDI	DRAM
From IOSF	DRAM
Security	IMR ranges are SAI protected.

2.1.5.1 Protected Memory Range (PMR-H: Programmable)

VT-d defines a high (greater than 4 GiB) protected memory range. This range is re-locatable. This range must be protected by IMRs to ensure only the IA core has access to this range before VT-d translation is enabled.

There is one range per VT-d engine. So the SoC has two PMR-H ranges.

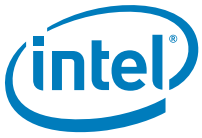
In addition to PMR-H (above 4 GiB) there is a PMR-L below 4 GiB with the same access restrictions.

Table 2-31. PMR-H

Name	PMR-H
Range	0.0.0.DefVTdBAR.PMRHBASE to 0.0.0DefVTdBAR.PMRHLIMIT and 0.0.0.GfxVTdBAR.PMRHBASE to 0.0.0GfxVTdBAR.PMRHLIMIT
From IDI	DRAM
From IOSF	DRAM
Security	GT has a copy of GfxVTd PMR. It will make sure that only VT-d walks are allowed to touch PMR and hence get onto IDI. Other tnx that hit PMR are killed before they get onto IDI. Display will add GfxVTd PMR. It will make sure that only VTd walks are allowed to go to PMR range and all other tnx will be killed before they get onto IOSF primary. DefVTd PMR will be implemented in Bunit. https://hsdes-stable.intel.com/home/default.html#article?id=101147810

2.1.6 High MMIO Address Range (TOUUD to 0x7F_FFFF_FFFF)

The range from TOUUD to 512 GiB (7F_FFFF_FFFFh) is used for devices in MMIO space. There are no legacy fixed or programmable MMIO address ranges in High MMIO space.



Root complex integrated PCI devices have memory space BARs that can be configured to claim memory within this region. Root Ports (PCIe or Mobile Express) have Base and limit range registers that can be configured to claim memory within this region.

Table 2-32. High MMIO Address Range

Name	High MMIO
Range	0.0.0.MCHBAR.TOUUD to 0x7F_FFFF_FFFF
From IDI	PSF1, unless a specific rule supersedes this rule.
From IOSF	PSF1, unless a specific rule supersedes this rule.
Security	No restrictions.

2.1.6.1 Other Ranges in High MMIO Address Ranges

Many of the programmable ranges defined in the Low MMIO Address Range can be configured to be in either Low or High MMIO Address space. The following list of ranges in Low MMIO space may be configured into High MMIO space:

- MCHBAR
- Default VTd BAR
- Graphics VTd BAR
- GTTMMADR
- GTMADR
- IBAR

2.2 System DRAM Address Space

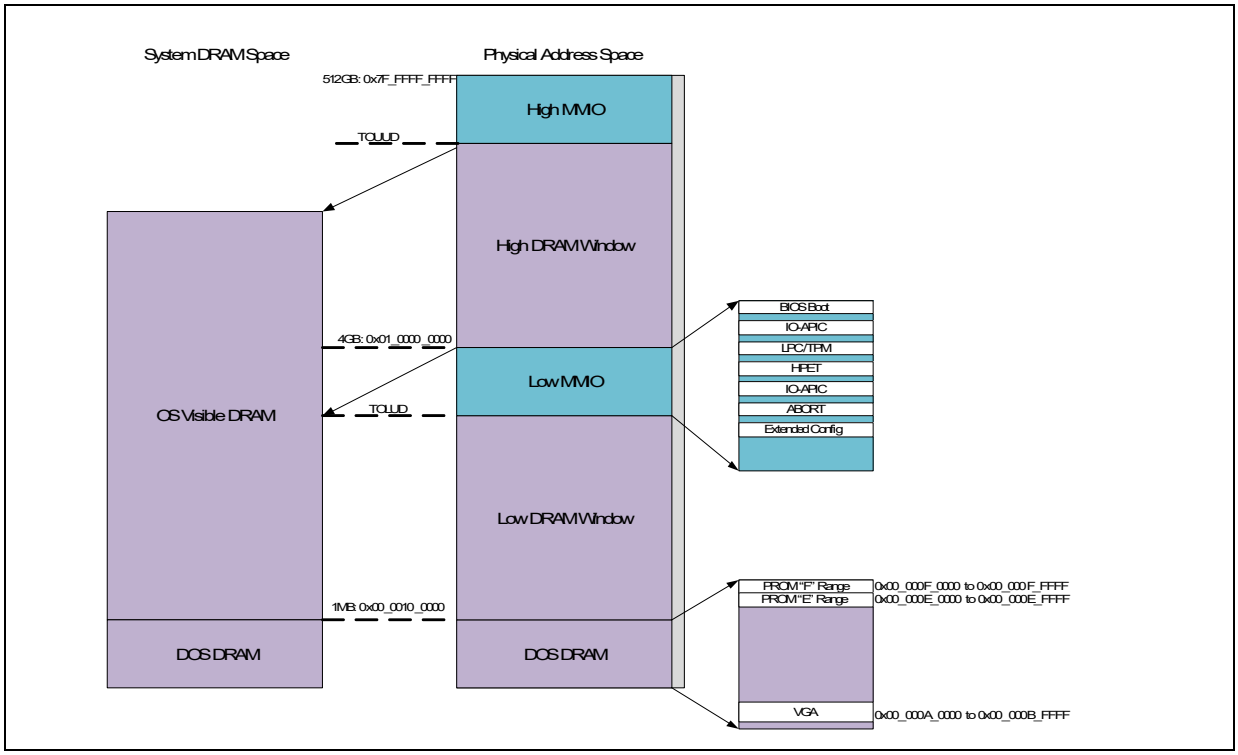
This is the range of addresses presented to the memory controller after all security checks and reclaiming has been done. The memory controller is aware of the total amount of populated DRAM and addresses above this range are considered invalid – writes will be dropped and reads will return all '1's.

In truth, memory controllers have options to swizzle which System DRAM Address Space address bits map to banks, rows, columns to increase performance. For purposes of this discussion, this mapping is assumed to 1-to-1.

2.2.1 Physical to System DRAM Address Mapping

Inside the system agent the Physical Address is converted to a System DRAM Address. This is done to "reclaim" all addressable DRAM that would otherwise be lost because the addresses conflict with the Low MMIO range.

Figure 2-2. Physical to System DRAM Address Map



2.2.2 Case 1: 2 GiB DRAM. Minimum 1 GiB PCI MMIO

BUNIT.TOLUD needs to be no greater than 3 GiB to make room for 1 GiB of Low MMIO between TOLUD and 4 GiB.

TOLUD could be set to 3 GiB, but any Physical Address Space request from 2 GiB to 3 GiB will exceed available DRAM and this range will need to be marked as unavailable by the IAFW to the OS ("bad"). Instead, it is better to leave the 2 GiB to 3 GiB Physical Address Space range available for MMIO devices. Setting TOLUD to 2 GiB makes all 2 GiB of DRAM available and provides 2 GiB of Low MMIO space.

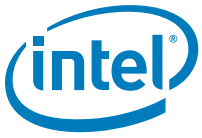
Because available DRAM is less than 4 GiB, BUNIT.TOUUD should be set to 4 GiB, allowing all of the 4 GiB to 64 GiB address space to be used for 64 b PCI MMIO.

2.2.3 Case 2: 8 GiB DRAM. Minimum 1 GiB PCI MMIO

BUNIT.TOLUD needs to be no greater than 3 GiB to make room for 1 GiB of Low MMIO between TOLUD and 4 GiB.

Setting TOLUD to 3 GiB gives the required range for Low MMIO and makes the maximum amount of Physical Address Range below 4 GiB available to access DRAM.

To make use of the remaining DRAM Address Space (3 GiB to 8 GiB), the Physical Address Space range 4 GiB to 9 GiB will automatically be mapped downwards by 1 GiB (subtract 4 GiB and add TOLUD) to 3 GiB to 8 GiB in DRAM Address Space before the request make it to the memory controller. This mapping happens for all DRAM request from CPUs or devices.



TOUUD would be set to 9 GiB and the full remaining Physical Address Space range from 9 GiB to 512 GiB is available for HIGH MMIO.

2.3 System Management Mode (SMM)

System Management Mode uses main memory for System Management RAM (SMM RAM). System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM.

2.3.1 IAFW Programming Restrictions

If any of the following conditions are violated the results of SMM accesses are unpredictable and may cause the system to hang:

- The upper bound of the SMM region is controlled by BGSM. The lower bound is controlled by TSEGMB.
- IAFW should program the upper and lower bounds with the upper > lower and ensuring that the address space must not overlap address space assigned to system DRAM, or to any MMIO range. This is an IAFW responsibility.
- The SMM region must not be reported to the OS as available DRAM. This is an IAFW responsibility.
- Any address translated through the GMADR TLB must not target the SMM Range.
- IAFW should initially leave the SMM region open to allow writing of SMM code in DRAM.
- Must setup the SMMR register in each CPU to prevent cache based attacks.
- The System Management Mode Range Register (SMRR) is an enhancement to the IA-32 Intel architecture that constrains SMM cache-ability controls to SMM code.
- After the microcode update has been loaded and during the SMM relocation phase of the POST, IAFW must detect if the processor supports SMRR by examining the SMRR_CAP bit (IA32_MTRR_CAP[11]). If the SMRR_CAP bit is set (‘1’) the processor supports the SMRR feature. If the SMRR_CAP bit is clear (‘0’) the processor does not support the SMRR feature. If the SMRR is supported, it must be enabled by setting bit 3 in the IA32_FEATURE_CONTROL MSR[3] (MSR 3Ah) together with the lock bit(bit 0) of the same MSR. In addition, It must set the SMRR_PHYS_BASE and SMRR_PHYS_MASK to match the BUNIT.BSMMRRL/ BUNIT.BSMMRRH defined region.
- South Cluster devices are **never** allowed to access SMM space. ABIMR must be used for this.

2.3.2 SoC Internal Enforcement of SMM Protection

Notes:

1. SoC will automatically filter CPU request from threads that are not in SMM mode that hit the SMM range. Writes will be dropped and reads will return all ‘1’s.
2. Access to the SMM area of physical address space from agents other than the CPU should be prevented. It is the responsibility of IAFW to use a SMM policy registers for this functionality.

2.3.2.1 CPU WB Transaction to an Enabled SMM Address Space

CPU Writeback transactions to enabled SMM Address Space must be written to the associated SMM DRAM even though BUNIT.BSMMRRL/BUNIT.BSMMRRH *[ALLOW_NON_SMM_WRITES_TO_SMM_SPACE_SMMWRITESOPEN]* = 0 and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cache able extended SMM space is used. It is the responsibility of IAFW to ensure that the SMM physical address range is not exposed to the operating system or used for any other function.

IAFW must also program the SMRR register in the CPU(s) to prevent a cache based security risk.

2.4 I/O Space

The SoC implements a 64 KiB + 3 B I/O address space. The I/O Space is accessed by the CPU using the IN/OUT instructions. This address space is separate from both the Host Memory Address Space described in Section 2.1, "Host Memory Address Space" and the PCI config space described in Section 2.1, "Host Memory Address Space". These requests never map to system DRAM. These requests are always NP and the CPU waits for a completion before proceeding to the next instruction.

The CPU micro-code is responsible for ensuring that I/O transactions issued on IDI do not cross a 4 B boundary. When an instruction would results in an un-aligned I/O transaction micro-code will issue two I/O transactions. When an instruction targets the upper three bytes of the 64 KiB I/O space (FFFDh-FFFFh) and the transaction is split, the second half of the transaction will access some or all of the "+ 3" bytes of I/O space (1_0000h to 1_00002h). For example a 4 B read to FFFEh results in a 2 B transaction to FFFEh, and a 2 B transaction to 1_0000h.

Notes:

1. There are no actual resources located at 1_0000 to 1_0003.
2. Funny I/O is treated as a separate address space (see Section 2.6, "Funny I/O Space"). Eight byte Funny I/O transactions are allowed but micro-code will ensure they are always naturally aligned.

Some root complex integrated PCI devices have I/O space BARs that can be configured to claim memory within this region. Root Ports (PCIe or Mobile Express) have Base and limit range registers that can be configured to claim I/O addresses within this region. IAFW and the OS ensure that the PCI BARs are not programmed to overlap with any of the legacy address ranges.

2.4.1 Fixed I/O Ranges: Decode and Routing

These Fixed address ranges are either positively decoded in the System Agent or subtractively routed to the Primary to Sideband Bridge (P2SB).

The following table defines the Fixed I/O address ranges that are positively decoded in the system agent. If any of these ranges are not enabled, a transaction to that range will subtractively decode to the P2SB.

The System Agent must shadow a copy of several LPC registers (IOE and IOD). Only one of LPC registers will be enabled at a time and they always have the same device and function number (specifically device 31, function 0).

The B-Unit implements the GCS register.

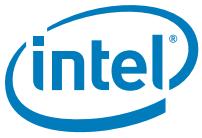


Table 2-33. Fixed I/O Address Map Positive Decode

I/O Address	IOSF Primary Target	Register control
080h	LPC or PCIe	GCS.RPR = 1
084h–086h	LPC or PCIe	GCS.RPR = 1
088h	LPC or PCIe	GCS.RPR = 1
08Ch–08Eh	LPC or PCIe	GCS.RPR = 1
200h–207h	LPC	IOE.LGE = 1
208h–20Fh	LPC	IOE.HGE = 1
220h–227h	LPC	((IOE.CAE & IOD.CA) = 3'b010) OR ((IOE.CBE & IOD.CB) = 03'b10)
228h–22Fh	LPC	((IOE.CAE & IOD.CA) = 3'b011) OR ((IOE.CBE & IOD.CB) = 3'b011)
238h–23Fh	LPC	(9IOE.CAE & IOD.CA) = 3'b100) OR (IOE.CBE & IOD.CB = 3'b100)
278h–27Fh	LPC	(IOE.PPE & IOD.LPT) = 2'b01
2E8h–2EFh	LPC	((IOE.CAE & IOD.CA) = 3'b101) OR ((IOE.CBE & IOD.CB) = 3'b101)
2F8h–2FFh	LPC	((IOE.CAE & IOD.CA) = 3'b001) OR ((IOE.CBE & IOD.CB) = 3'b001)
338h–33Fh	LPC	((IOE.CAE & IOD.CA) = 3'b110) OR ((IOE.CBE & IOD.CB) = 3'b110)
370h–375h	LPC	(IOE.FDE & IOD.FDD) = 1
377h	LPC	(IOE.FDE & IOD.FDD) = 1
378h–37Fh	LPC	(IOE.PPE & IOD.LPT) = 2'b00
3BCh–3BEh	LPC	(IOE.PPE & IOD.LPT) = 2'b10
3E8h–3EFh	LPC	((IOE.CAE & IOD.CA) = 3'b111) OR ((IOE.CBE & IOD.CB) = 3'b111)
3F0h–3F5h	LPC	(IOE.FDE & IOD.FDD) = 0
3F7h–3F7h	LPC	(IOE.FDE & IOD.FDD) = 0
3F8h–3FFh	LPC	((IOE.CAE & IOD.CA) = 3'b000) OR ((IOE.CBE & IOD.CB) = 3'b000)
4D0h–4D1h	LPC	N/A
678h–67Fh	LPC	(IOE.PPE & IOD.LPT) = 2'b01
778h–77Fh	LPC	(IOE.PPE & IOD.LPT) = 2'b00
7BCh–7BEh	LPC	(IOE.PPE & IOD.LPT) = 2'b10

The following table defines the Fixed I/O address ranges that are subtractively routed to the P2SB. Transactions that reach the P2SB are either terminated or forwarded on IOSF SB to the final destination. A hard strap informs the P2SB if LPC is enabled.

Table 2-34. Fixed I/O Address Map Subtractive Decode (Sheet 1 of 3)

I/O Address	IOSF Primary Target	IOSF SB Target
000h–01Fh	P2SB	Terminate
020h–021h	P2SB	ITSS (interrupt)
024h–025h	P2SB	ITSS (interrupt)
028h–029h	P2SB	ITSS (interrupt)
02Ch–02Dh	P2SB	ITSS (interrupt)

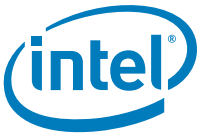


Table 2-34. Fixed I/O Address Map Subtractive Decode (Sheet 2 of 3)

I/O Address	IOSF Primary Target	IOSF SB Target
02Eh–02Fh	P2SB	LPC
030h–031h	P2SB	ITSS (interrupt)
034h–035h	P2SB	ITSS (interrupt)
038h–039h	P2SB	ITSS (interrupt)
03Ch–03Dh	P2SB	ITSS (interrupt)
040h	P2SB	ITSS (Timer 0 Register)
041h	P2SB	Terminate
042h	P2SB	ITSS (Timer 2 Register)
043h	P2SB	ITSS (Timer Control Word Register)
04Eh–04Fh	LPC	LPC
050h	P2SB	ITSS (alias of 040h)
051h	P2SB	Terminate
052h	P2SB	ITSS (alias of 042h)
053h	P2SB	ITSS (alias of 043h)
060h	P2SB	LPC
061h	P2SB	ITSS (CPU I/F)
062h	P2SB	LPC
063h	P2SB	ITSS (CPU I/F)
064h	P2SB	LPC
065h	P2SB	ITSS (CPU I/F)
066h	P2SB	LPC
067h	P2SB	ITSS (CPU I/F)
070h	P2SB	ITSS (CPU I/F), RTC, PMC
071h	P2SB	RTC, PMC
072h–073h	P2SB	RTC, PMC
073h	P2SB	RTC, PMC
074h	P2SB	RTC, PMC
075h	P2SB	RTC, PMC
076h–077h	P2SB	RTC, PMC
080h	P2SB	LPC or PMC
081h–083h	P2SB	Terminate
084h–086h	P2SB	LPC or PMC
087h	P2SB	Terminate
088h	P2SB	LPC or PMC
089h–08Bh	P2SB	Terminate
08Ch–08Eh	P2SB	LPC or PMC
08Fh	P2SB	Terminate
090h	P2SB	LPC
091h	P2SB	Terminate

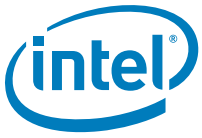


Table 2-34. Fixed I/O Address Map Subtractive Decode (Sheet 3 of 3)

I/O Address	IOSF Primary Target	IOSF SB Target
092h	P2SB	ITSS (CPU I/F)
093h	P2SB	Terminate
094h–096h	P2SB	LPC or PMC
097h	P2SB	Terminate
098h	P2SB	LPC or PMC
099h–09Bh	P2SB	Terminate
09Ch–09Eh	P2SB	LPC or PMC
09Fh	P2SB	Terminate
0A0h–0A1h	P2SB	ITSS (interrupt)
0A4h–0A5h	P2SB	ITSS (interrupt)
0A8h–0A9h	P2SB	ITSS (interrupt)
0ACh–0ADh	P2SB	ITSS (interrupt)
0B0h–0B1h	P2SB	ITSS (interrupt)
0B2h–0B3h	P2SB	PMC
0B4h–0B5h	P2SB	ITSS (interrupt)
0B8h–0B9h	P2SB	ITSS (interrupt)
0BCh–0BDh	P2SB	ITSS (interrupt)
0C0h–0DFh	P2SB	Terminate
0F0h	P2SB	Terminate
170h–177h	P2SB	Terminate
1F0h–1F7h	P2SB	Terminate
376h	P2SB	Terminate
3F6h	P2SB	Terminate
4D0h–4D1h	P2SB	ITSS (interrupt)
CF9h	P2SB	ITSS (CPU I/F)

2.4.2 Variable I/O Ranges: Decode and Routing

Several PCI functions have I/O BARs (See Table 2-39, Funny I/O Address Ranges and Routing). The PCIe root ports have I/O Base and Limit ranges. Address decode for the standard PCI bars and bridge Base/Limit registers occurs in the IOSF fabric, except for VC0a agents on PSF0.

The Following table lists all of the non-standard legacy variable I/O address ranges along with the agent they target. These ranges are source decoded in the System Agent.

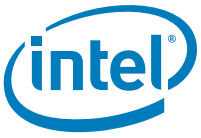


Table 2-35. Legacy Variable I/O Address Map

Range Name	Size (Bytes)	Target	Enable	Bar
LPC Generic 1	4 to 256	LPC	LGIR1[0]	LGIR1
LPC Generic 2	4 to 256	LPC	LGIR2[0]	LGIR2
LPC Generic 3	4 to 256	LPC	LGIR3[0]	LGIR3
LPC Generic 4	4 to 256	LPC	LGIR4[0]	LGIR4

2.4.2.1 Integrated Graphics Device (IGD)

Note: the IGD BARs are not restricted to Low MMIO space and could be programmed in High MMIO space.

Note: The Integrated graphics device has two Host Memory Space BARs. These are standard PCI BARs.

- Address decode to the IGD I/O BARs are valid if the Integrated Graphics device is enabled and system software has enabled the I/O Access to the device:
- IGDEnabled:
  (0.0.0.PCI.DEVEN.D2F0EN = 1)
  AND (0.2.0.PCI.PMCSR.PSRSTAT = 2'b00)
  AND (0.2.0.PCI.PCICMD2.IOE = 1)

Table 2-36. Display IOBAR

Name	GTTMMADR
Range	BAR: 0.2.0.PCI.IOBAR (8 B)

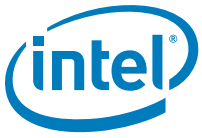
From IDI	IF (IGDEnabled)
	  Display
	ELSE
	  PSF1

From IOSF	I/OA-Unit
Security	No Restrictions.

2.5 PCI Config Space

PCI Config space is used to access both PCI devices inside the SoC and PCI/PCIe devices outside the SoC connected to the PCIe hierarchy. This space is only accessible from the CPU. Software has two mechanisms for accessing this space: (1) standard CF8/CFC "I/O" ports; (2) PCI Enhanced Configuration. The CPU traps CF8/CFC accesses in uCode and converts them to Funny I/O transactions. PCI Enhanced Configuration accesses appear within the Extended Configuration range as defined by the PCIEXBAR register. The system agent converts both of these types of transactions into IOSF transactions that target the PCI config space.

All SoC internal devices are on PCI bus #0. The list of all integrated PCI functions is in Section 2.8, "PCI Devices". For more information on the PCI configuration space refer to the PCI 3.0 specification and the PCIe 3.0 specification.



2.5.1 Configuration Mechanisms

The CPU is the originator of configuration cycles. The configuration cycles will be translated to PCI Config cycles before being sent on PSF fabric to configure different PCI devices or a transaction on IOSF-SB fabric to update the register.

Note: All configuration registers are expected to be mapped on IOSF-SB fabric.

2.5.1.1 Standard PCI Configuration Mechanism

The following is the mechanism for software to generate configuration cycles using a Address/Data pair in I/O space: CF8h (CONFIG_ADDRESS) and CFCh (CONFIG_DATA).

A 4 B (DW) I/O write cycle places a value into CONFIG_ADDRESS that specifies the PCI bus, the Device on that bus, the Function within the Device, and a offset to the configuration register of the Function being accessed. CONFIG_ADDRESS[31] must be '1' to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in a Funny I/O transaction that is converted by the system agent into a PCI configuration transaction.

Note: This mechanism is limited to accessing the first 256 B of configuration space.

The format of the address is as follows:

Table 2-37. PCI Config PORT CF8 Mapping

Field	I/O CF8h CONFIG_ADDRESS Bits	IDI Funny I/O bit location	IOSF CMD Header Bits
Bus Number	23:16	27:20	Byte 8 [7:0]
Device Number	15:11	19:15	Byte 9 [7:3]
Function Number	10:08	14:12	Byte 9 [2:0]
Register Number	07:02	07:02	Byte 11 [7:2]

Bit 31 of offset CF8h must be set for a configuration cycle to be generated.

2.5.1.2 PCI Express Enhanced Configuration Mechanism

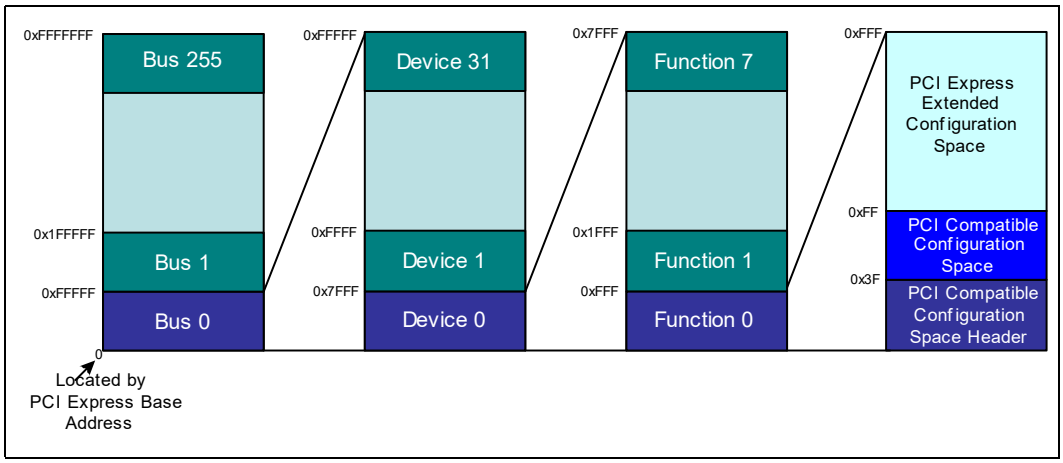
PCI Express extends the configuration space to 4096 B per device/function as compared to 256 B allowed by PCI Specification Revision 3.0. PCI Express configuration space is divided into a PCI 3.0 compatible region, which consists of the first 256 B of a logical device's configuration space and a PCI Express extended region which consists of the remaining configuration space.

The PCI-compatible region can be accessed using either the Standard PCI Configuration Mechanism or using the PCI Express Enhanced Configuration Mechanism described in this section. The extended configuration registers may only be accessed using the PCI Express Enhanced Configuration Mechanism. To maintain compatibility with PCI configuration addressing mechanisms, system software must access the extended configuration space using 32 b data operations (32 b aligned) only. These 32 b operations include byte enables allowing only appropriate bytes within the DWORD to be accessed. Locked transactions to the PCI Express memory mapped configuration address space are not supported. All changes made using either access mechanism are equivalent.

The PCI Express Enhanced Configuration Mechanism utilizes a flat memory-mapped address space to access device configuration registers. This address space is reported by the system firmware to the operating system.

The PCI Express Configuration Transaction Header includes an additional 4 b (ExtendedRegisterAddress[3:0]) between the Function Number and Register Address fields to provide indexing into the 4 KiB of configuration space allocated to each potential device. For PCI Compatible Configuration Requests, the Extended Register Address field must be all '0's.

Figure 2-3. Memory Map to PCI Express Device Configuration Space



Just the same as with PCI devices, each device is selected based on decoded address information that is provided as a part of the address portion of Configuration Request packets. A PCI Express device will decode all address information fields (bus, device, function and extended address numbers) to provide access to the correct register.

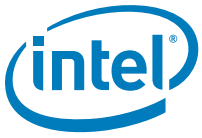
A flat 256 MiB Host Memory Address Space window into Enhanced Configuration Space is defined using the BUNIT.PCIEXBAR. This registers contains a 12 b base address which is compared against bits 39:28 of the incoming memory address. If these 12 b match the cycle is turned into a configuration cycle with the following fields:

Table 2-38. PCI Config Memory Bar Mapping

Field	Host Memory Space address	IDI Memory Cycle Bit location	IOSF CMD Header Bits
Bus Number [7:0]	27:20	27:20	Byte 8 [7:0]
Device Number [4:0]	19:15	19:15	Byte 9 [7:3]
Function Number [2:0]	14:12	14:12	Byte 9 [2:0]
Register Number [9:0]	11:2	11:2	Reg[9:6] ⇒ Byte 10 [3:0] Reg[5:0] ⇒ Byte 11 [7:2]

To access this space (steps 1, 2, and 3 are done only once by IAFW),

1. Use the PCI compatible configuration mechanism to enable the PCI Express enhanced configuration mechanism by writing '1' to bit 0 of BUNIT.PCIEXBAR registers.



2. Use the PCI compatible configuration mechanism to write an appropriate PCI Express base address into BUNIT.PCIEXBAR registers
3. Calculate the host address of the register you wish to set using

host address=(PCI Express base
+ (1 MiB× bus number)
+ (32 KiB× device number)
+ (4 KiB× function number)
+ (1 B× offset within the function))

4. Use a memory write or memory read cycle to the calculated host address to write or read that register.

2.5.1.3 Type 0/Type 1 Configuration

If the Bus Number is zero, the SoC will generate a Type 0 Configuration Cycle on IOSF. If the Bus Number is non-zero, the SoC will generate a Type 1 Configuration Cycle on IOSF.

2.5.2 ACPI Mode

Some devices/functions are not intended to be enumerated/configurable by the OS—they consume memory space, but this is not under the control of the OS. This may be for security reasons, if there is no driver for the function, or if the function is specifically for IAFW. For normal PCI functions, the PSF implements a PCI Configuration Object, which is the set of PCI Config registers that it shadows so that it can perform fabric decode and routing of transactions. For ACPI functions, the PSF implements either a Hybrid or Fixed ACPI Configuration Object. A summary is given below.

2.5.2.1 Hybrid ACPI Configuration Object

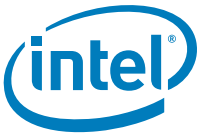
Each Hybrid ACPI configuration object has a config header disable bit associated with it. When this bit is set the PCI configuration object becomes a hybrid ACPI configuration object. The PSF fabric stops routing PCI configuration cycles to the associated function, and stops updating the shadow registers of the configuration object. The hybrid ACPI shadow registers will be compared to for Fabric decode. The configuration object remains accessible and update able via IOSF SB.

To use a device as an ACPI device, IAFW would first configure the device and then set the cfgDis bit. IAFW then informs the OS via the ACPI tables about the system resources (e.g. memory range) that have been assigned to the function.

Functions that are switchable between host and CSE root spaces use hybrid ACPI objects to allow their configuration space to be hidden while set to CSE root space, for security.

2.5.2.2 Fixed ACPI Configuration Object

A Fixed (or Native) ACPI configuration object has the same structure as a PCI configuration object, except almost all the values are set as compile-time constants. The funDis, barDis, and ROMbarDis bits are the only control fields implemented, to disable the function or BARs. The BAR and other PCI configuration settings are immutable.



Native ACPI objects are used for security (no configuration cycles accepted) and for completion routing-by-ID without BARs (also known as a ghost BDF).

2.5.2.3 IOSF2OCP Bridge ACPI Mode

The IOSF2OCP Bridge allows the PCI functions that it implements to be put into an ACPI mode. In this mode of operation, PCI config accesses to the function return a UR completion. A control bit in the private configuration space (PCICFGCTRL[{1 to 32}].PCI_CFG_DIS) disables PCI configuration accesses in the Bridge. The values programmed in the PCI Configuration registers are still valid. The Bridge uses these registers (for example BAR, MSE, D3, and BME) to determine how to handle memory accesses.

An additional BAR1 register is present in the PCI configuration space of the Bridge, for each function, specifically to provide access to the PCI Config registers when the function is in ACPI mode. Memory accesses to BAR1 access the PCI configuration space of the corresponding function; that is BAR1 is an alias to the PCI configuration space. The address decode for BAR1 ignores the MSE and D3 device states in the PCI configuration space.

Note: MMIO transaction are posted and PCI configuration accesses are non-posted. A read must always be performed following BAR1 access to ensure the Bridge observes the BAR1 write access. Only 4 B (1 DW) BAR1 downstream accesses are supported. BAR1 memory accesses, which fall outside the standard PCI configuration registers, are treated as accesses to reserved registers.

Refer to the latest version of the IOSF2OCP Bridge EAD for further details.

2.6 Funny I/O Space

Both uCode and the IGD can issue transactions on IDI targeting the Funny I/O space. Any I/O transaction with an address beyond 64 KiB + 3 is a Funny I/O transaction. There are three targets for Funny I/O transactions in the SoC: the IGD, the C-unit, and the SoC cores.

The IGD uses Funny I/O to communicate internally between the GT logic on IDI and the Display logic on IOSF. In addition there is a 32 KiB window within the GT Funny I/O range that aliases to MCHBAR providing read only access for GT to MCHBAR registers. (Read only access is enforced by SAI checks in the B-Unit).

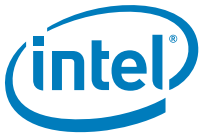
The SoC cores use Funny I/O to access PCI configuration registers (see Section 2.5, "PCI Config Space" for more details on funny I/O access to PCI config space.) In addition there is a set of uncore Configuration Registers (CRs) that are accessed by funny I/O. Uncore CRs can be accessed by uCode. In addition some of the CRs are exposed to software as MSRs.

The SoC cores can send LT doorbell transactions to other cores using Funny I/O. These Funny I/O transactions route between cores on IDI through the system agent.

2.6.1 RAVDMs

GT to CSE VDM flow is as follows:

1. GT issues Funny I/O transaction
2. B-Unit routes to A-Unit



3. A-Unit converts to RAVDM and sends to PSF1 for decode
4. PSF1 routes by ID to CSE
5. VDM "Target ID" should use the HECI1 B/D/F

GT will target the PAVP VDM range of the GTTMMADR. GT will only send posted RAVDM writes with RSP = 0 for the PAVP flow. GT RAVDMs that are writes are forwarded to CSE. Reads to the PAVP region get routed normally to display.

There are no display → CSE RAVDMs.

2.6.2 Funny IO Address Ranges

Table 2-39, Funny I/O Address Ranges and Routing below provides the address ranges and how they are routed in the system.

Table 2-39. Funny I/O Address Ranges and Routing

Range	Usage	Routing
0x2000_0000 to 0x2013_FFFF	GT Funny I/O	Route to Display: NOTE writes to 0x2012_8000 to 0x2012_FFFFh are routed to display as RAVDMs.
0x2014_0000 to 0x2014_7FFF	GT Funny I/O: MCH BAR alias (Read only)	Route to C-unit
0x2014_8000 to 0x201F_FFFF	GT Funny I/O	Route to Display
0x4000_0000 to 0x40FF_FFFF	CR access	Route to C-unit
0x8000_0000 to 0x8FFF_FFFF	PCI Config Space access	Convert to IOSF CFG transaction in SA and route by B/D/F
0xFED0_0000 to 0xFEDF_FFFF	LT Doorbells	IDI to SA to IDI—doesn't travel to A-Unit

2.7 IOSF-SB Private CR Space

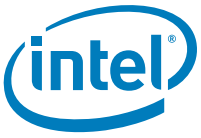
IOSF-SB message space is used to access registers mapped on IOSF-SB. These registers include uncore CRs, and chipset specific registers. The Private CR space is accessed on IOSF SB using the CRRd and CRWr opcodes. Each Destination ID can have up to 48 b of Byte addressable private register space.

An uncore CR is a configuration register that is accessible either by uCode or by IA code through the MSR read/write instruction. Uncore CRs are accessed through Funny I/O and mapped onto IOSF SB in the C-unit.

Chipset specific registers are accessed through a memory BAR in the P2S Bridge function. Many I/O controllers and most of the Analog PHYs contain Chipset specific registers for IAFW configuration. Historically these were mapped behind the SoC "RCBA" or Root Complex Base Address register.

Access to IOSF-SB by the Host or System Agent is possible over PSF via the Primary to Sideband Bridge (P2SB). P2SB will forward properly formatted register access requests as CRRd and CRWr requests via IOSF-SB. The P2SB also provides a mask that can be used to restrict access to certain endpoints.

P2SB offers two access methods for Primary to Sideband message generation:



- Sideband register access via MMIO (SBREG_BAR interface); limited to 16-bit addressing
- Sideband Message Interface (required for 48 b addressing beyond 64 KiB)

PSF CR space can be accessed using the simpler MMIO BAR interface. A single MRd64/MWr64 to the P2SB BAR causes a CRRd/Wr message to be sent via IOSF-SB.

Table 2-40. P2SB MMIO Register Interface

Addr[63:24]	Addr[23:16]	Addr[15:2]	Addr[1:0]
BAR	Target Port ID	Register offset	2'b00

As seen in Table 2-40, P2SB MMIO Register Interface, the memory address contains the BAR, destination port ID, and register offset. Using MMIO, all Sideband messages sent are non-posted and will back pressure on PSF. Writes are pipelined; whereas reads are serialized.

The Funny I/O access mechanism and the MMIO access mechanism both provide paths to the same registers on IOSF SB. However, Uncore CRs and MSRs must be protected from access by un-privileged code. SAI enforcement at the target is used for this.

2.8 PCI Devices

The PCI Configuration Matrix tables (linked) provide the Device and Function number assignment for all internal devices. In addition it specifies the number and size of the BARs for each Function. Address decoding for devices 0 (function 0 only), 2, and 3 are performed by B-Unit. All other device functions are address decoded by PSF.

Note: Functions that are implemented in an IOSF2OCP Bridge have a 4 KiB 64 b BAR1 that aliases to PCI Config space for the corresponding function. This is to provide access to the PCI Config registers when the function is in ACPI mode. Refer to the latest version of the IOSF2OCP Bridge EAD for details.

2.9 System Memory Protection

The SoC security mechanism is designed to provide access control for data stored in DRAM. Security checks happen in the Host Memory Address Space, but only for request on the way to DRAM rather than devices/MMIO.

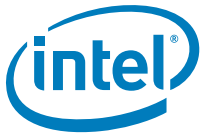
It is important for both security and coherency checking that there are no aliasing cases in either Host Memory Address Space or System DRAM Address Space for request targeting DRAM. This means that SoC must not allow accesses to two different addresses to retrieve data from the same location in DRAM.

To ensure no aliasing, certain rules must be followed.

2.9.1 PMR-L and PMR-H

Bunit will implement PMR protection for the default VTd engine.

Display (and GT) will implement PMR protection for the Gfx VTd engine:



- GT has a copy of GfxVTd PMR. It will make sure that only VT-d walks are allowed to touch PMR and hence get onto IDI. Other transactions that hit PMR are killed before they get onto IDI.
- Display will add GfxVTd PMR. It will make sure that only VTd walks are allowed to go to PMR range and all other transactions will be killed before they get onto IOSF primary.

Software is required to program PMR_def and PMR_gfx as the same but they may be different during the initial setup period.

2.9.2 B-Unit Isolated Memory Regions (IMRs)

Isolated memory regions provide a mechanism to add SAI checks to certain regions of memory.

2.9.3 Summary of SoC Lock Bits

The preferred mechanism of locking registers is to use SAI policy registers. However there are many IP which do have lock bits in the SoC. The recommendation is to not add any new lock bits, but instead use SAI policy registers.

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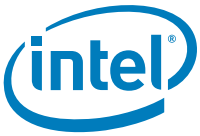


3 CSE Root Space

3.1 CSE Memory Address Space

The SoC implements a 64 b CSE Memory Address space. Internal to the CSE the minute IA subsystem uses a 32 b physical address. At the CSE Gasket a set of programmable Address Translation Tables (ATT) allow the CSE minute IA and internal DMA engines to access the full 64 b CSE Memory space of the SoC. This section describes the address space and routing outside of the CSE.

Some portion of the CSE Memory Address Space references System DRAM. IMR regions are used to divide the DRAM between the Host Memory Space and the CSE Memory Space.

VT-d does not apply in the CSE Memory Address space.

CSE Memory Address Space Decode and Routing

Transactions that originate inside the CSE are positively decoded against several possible ranges in the IOSF fabric. The downstream subtractive decode path from the CSE leads to System DRAM.

Transactions that originate outside of the CSE in the CSE root space are positively decoded against several possible ranges in the IOSF fabric. The upstream subtractive decode path from agents outside the CSE leads to the CSE. Transactions from devices outside the CSE that access System DRAM in the CSE Memory Address Space are considered Peer to Peer transactions and must be positively decoded.

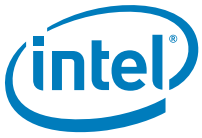
3.1.1 SoC System Agent Decode and Routing

Any transaction in the CSE root space that arrives at the A-Unit and does not positively decode to a Peer target will be forwarded to the B-Unit. Within the B-Unit the Address is checked against the IMRs and stolen memory ranges (TSEG SMM and Graphics Stolen Memory). If the IMRs allow access the transaction is converted to a System DRAM Address Space and sent to DRAM. Otherwise the transaction is aborted.

IMRs in the system agent are applied to both Host Memory address space and CSE Memory Address space. Depending on how the IMRs are programmed the Host Memory Space and the CSE Memory Space may be completely non-overlapping, or there may be IMR regions that create an alias where both Host Memory Space and CSE Memory Space reference the same System DRAM Address.

3.1.2 Abort Handling

The term abort is used in this document to handle a few different error handling mechanisms.



3.1.2.1 B-Unit Abort Handling

Non-posted Transactions that are aborted in the B-Unit will have a completion returned to the originator with bogus data. Posted transactions that are aborted in the B-Unit are dropped without altering the contents of system memory. Depending on the reason for the abort, the B-Unit will follow different error logging behaviors.

3.1.2.2 IOSF Abort Handling

Transactions routed to IOSF will either positively decode or be routed to the B-Unit. There are no cases where the IOSF fabric will abort a CSE memory space transaction.

The IOSF fabric will perform error handling for CSE space configuration cycles see Section 2.5, "PCI Config Space".

3.1.3 Fixed Positive Decode Ranges

The following table defines the fixed address ranges in the CSE Memory Address Space. The IOSF fabric is configured to route these ranges to the correct destination.

IOSF target	Range	Notes
PMC (Shared SRAM)	0x8000_0000_FF06_C000 to 0x8000_0000_FF06_FFFF	Writes and reads to this range.
LPSS (secure I/O)	0x8000_0000_FF00_6000 to 0x8000_0000_FF00_6FFF	Writes and reads to this range.
LPSS (secure I/O)	0x8000_0000_FF00_7000 to 0x8000_0000_FF00_7FFF	Writes and reads to this range.

3.1.4 Programmable Positive Decode Ranges

3.1.4.1 Dedicated PCI Functions

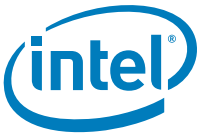
A PCI function that is always present in the CSE root space is a dedicated function. There are two dedicated functions in the SoC: Audio and the SPI controller. The CSE Programs the BARs of the dedicated function using PCI configuration cycles.

3.1.4.2 Switchable PCI Functions

Several of the PCI functions in the SoC are configurable to be in either the Host Root Space or the CSE Root Space. These functions are never in both spaces at the same time. These functions include the USB-Device controller, the PMC, the 15 functions in the LPSS, and the four functions in the SCS.

When the device is switched into the CSE Root Space, the CSE programs the BARs of the device to set the address range the device will respond to in the CSE Memory Address Space.

Switchable functions will have the same Device and Function number in both CSE Root Space and the Host Root Space. See Section 2.8, "PCI Devices" for the Device and Function number assignments.



3.1.4.3 DRAM as Peer Address Ranges

To enable routing of transactions from outside the CSE to System DRAM the IOSF fabric implements a hybrid ACPI configuration object. This is a set of registers inside the IOSF fabric that match the definition of a standard PCI type0 header. They are programmed over IOSF SB by the CSE. The BARs must be programmed by the system to route transactions to the IMR regions that are accessed in the CSE root space by peer agents.

To simplify IMR region sizing in the fabric, two large 256 MiB sized BARs are created in one hybrid ACPI object associated with ISH in PSF3. The actual IMRs will be assigned by CSE within the 256 MiB BAR region (or 512 MiB if combined). Upstream requests to the IMRs will be within the region covered by the BARs.

The following is the list of peer agents that require access to System DRAM in the CSE root space. The decode mode, either address (italicized to differentiate) or source, is listed for requests and completions. Address decoding is provided by the IOSF fabric and indicated by italics, whereas source decoding is provided by either B-Unit or the IP.

- I-Unit — Requests: source decode, Completions: source decode
- Audio — Requests: source decode, *Completions: address decode*
- ISH — *Requests: address decode, Completions: address decode*
- PMC — *Requests: address decode, Completions: address decode*

The IMR completions are routed back downstream to the requester by ID (BDF). A hybrid ACPI object in the IOSF fabric is associated with Audio, PMC, and ISH to route completions. Note that the ISH hybrid ACPI object serves dual purpose by providing the IMR region BARs and the ISH BDF for ISH IMR completions.

3.2 System DRAM Address Space

The physical CSE Memory Address is converted to a System DRAM address in the exact same way as a Host Memory Address. See Section 2.2, "System DRAM Address Space".

3.3 I/O Space

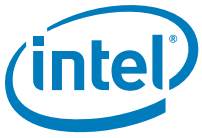
There are no resources mapped into I/O Space in the CSE root space outside of the CSE.

3.4 PCI Config Space

The CSE only accesses root complex integrated functions. By convention devices 0 to 8 will be inside the CSE itself, and devices 9 to 31 are available for use outside of the CSE. All CSE functions are on PCI bus #0.

It is possible for the CSE subsystem to generate type1 configuration transactions onto the IOSF fabric. There is no use case for this in the SoC, but it could occur. These will subtractively decode to the A-Unit and should be properly aborted.

It is possible for the CSE subsystem to generate Type 0 configuration transactions onto the IOSF fabric that will not positively decode. There is no use case for this in the SoC, bit it could occur. These will subtractively decode to the A-Unit and should be properly aborted.



3.5 IOSF-SB Private CR Space

The CSE can access IOSF-SB Private CR space from an SB ATT window in the Gasket. The IOSF-SB Private CR space is the same in CSE root space and Host root space. SAI protections are used where necessary to restrict access.

3.6 PCI Devices

The following PCI Devices are always available in the CSE root space.

Please note that some unnecessary device address resources exist in the PSF configuration because removal was not possible with schedule constraints. Specifically, PSF SPI defines an extra 16 MiB BAR for Huffman decompression, which will not be used and doesn't affect the address map.

PCI Configuration Matrix:

Table 3-1. PCI Configuration Matrix (Sheet 1 of 2)

Logical Function	PSF Agent	Type	DID	Device	Function
SoC Base device ID			5A80		
Host Bridge	C-unit	PCI	0x5AF0	0	0
DPTF (Camarillo)	C-unit	PCI	0x5A8C	0	1
Gen	Display	PCI	0x5A84	2	0
Iunit	Iunit	PCIe	0x5A88	3	0
Reserved (CSE)	CSE			7	0
P2SB	P2SB	PCI	0x5A92	13	0
PMC	PMC	ACPI	0x5A94	13	1
SPI	SPI	ACPI	0x5A96	13	2
Shared SRAM	PMC	ACPI	0x5AEC	13	3
Audio	Audio	PCIe	0x5A98	14	0
CSE-HECI1	CSE	PCI	0x5A9A	15	0
CSE-HECI2	CSE	PCI	0x5A9C	15	1
CSE-HECI3	CSE	PCI	0x5A9E	15	2
CSE-fTPM (PSF ghost)	CSE	ACPI		15	7
CSE-HOFFL	HOFFL	PCI	0x5AA0	16	0
ISH	ISH	PCI	0x5AA2	17	0
SATA	SATA	SATA	0x5AE0	18	0
PCIe-A 0	PCIe-A	PCIe	0x5AD8	19	0
PCIe-A 1	PCIe-A	PCIe	0x5AD9	19	1
PCIe-A 2	PCIe-A	PCIe	0x5ADA	19	2
PCIe-A 3	PCIe-A	PCIe	0x5ADB	19	3
PCIe-B 0	PCIe-B	PCIe	0x5AD6	20	0
PCIe-B 1	PCIe-B	PCIe	0x5AD7	20	1
USB-Host (xHCI)	USB-H	PCI	0x5AA8	21	0
USB-Device (xDCI)	USB-D	PCI	0x5AAA	21	1
I2C 0	LPSS	PCI	0x5AAC	22	0

Table 3-1. PCI Configuration Matrix (Sheet 2 of 2)

Logical Function	PSF Agent	Type	DID	Device	Function
I2C 1	LPSS	PCI	0x5AAE	22	1
I2C 2	LPSS	PCI	0x5AB0	22	2
I2C 3	LPSS	PCI	0x5AB2	22	3
I2C 6	LPSS	PCI	0x5AB8	23	2
I2C 7	LPSS	PCI	0x5ABA	23	3
UART 0	LPSS	PCI	0x5ABC	24	0
UART 1	LPSS	PCI	0x5ABE	24	1
UART 2	LPSS	PCI	0x5AC0	24	2
UART 3	LPSS	PCI	0x5AEE	24	3
SPI 0	LPSS	PCI	0x5AC2	25	0
SPI 1	LPSS	PCI	0x5AC4	25	1
SPI 2	LPSS	PCI	0x5AC6	25	2
PWM	PMC	PCI	0x5AC8	26	0
SD Card	SCS	PCI	0x5ACA	27	0
eMMC	SCS	PCI	0x5ACC	28	0
LPC	LPC	PCI	0x5AE8	31	0
SMBUS	SMBUS	PCI	0x5AD4	31	1

For the switchable PCI devices see Section 2.8, "PCI Devices" for device/function assignments and BAR information. The following PCI devices are switchable: USB-Device, I2C0 to I2C7, UART0 to UART2, SPI0 to SPI2, SD Card, eMMC.

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4 Register Access Methods

There are five common register access methods:

- I/O-Space Register Access Methods

1. Fixed I/O Register Access (both Regular I/O and Funny I/O accesses)
2. Variable I/O (I/O-Referenced) Register Access
3. PCI Configuration Register Access (Indirect—via Memory or I/O Registers)

- Memory-Space (Memory Mapped I/O, MMIO) Register Access Methods

4. Fixed Memory-Mapped Register Access
5. Variable Memory (Memory-Referenced) Register Access

For details on the address ranges supported by these register access methods, see the Address Map chapter.

Note: MCHBAR MMIO space has been adopted to replace the Message Bus Register Access functionality provided in previous devices. This change has been made to improve convergence between client and SoC devices as well as to resolve outstanding issues relating to interrupts, security, and VT-d support.

4.1 I/O-Space Register Access Methods

4.1.1 Fixed I/O Register Access

Fixed I/O registers are accessed by specifying their address in a PORT IN or PORT OUT transaction from the CPU core. This allows direct manipulation of the registers. Fixed I/O registers are unmovable register in I/O space. There are two categories of Fixed I/O registers:

Regular I/O registers—registers whose addresses fit within 16 b (0x0000 to 0xFFFF)

Funny I/O registers—registers whose addresses are above 2^16 + 3 (0x10004 and up)

Regular I/O registers are visible to all agents capable of making I/O accesses; Funny I/O registers are limited to SoC IA core uCode and the GEN9 Display (IGD) for internal communications within the SoC.

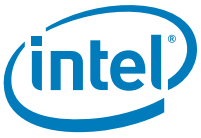
Table 4-1. Fixed I/O Register Access Method Example (P80 Register)

Type: I/O Register (Size: 32 b)	P80: 80h

Note: Funny I/O register accesses may be 64 b.

4.1.2 Variable I/O (I/O-Referenced) Register Access

Variable I/O (I/O-referenced) registers use programmable base address registers (BARs) to select the base I/O address for a range of I/O addresses. The I/O BARs act as pointers to blocks of actual I/O registers; other than the variable starting address for Variable I/O registers, accessing these registers is the same as for Fixed I/O registers.



To access an I/O-referenced register for a specific I/O base address, start with that base address and add the register's offset. Example pseudo code for an I/O-referenced register read is as follows:

```
Register_Snapshot= IOREAD([IO_BAR] + Register_Offset)
```

Base-address registers are often located in the PCI configuration space and are programmable by the BIOS/OS. Other base-address register types may include fixed memory registers, fixed I/O registers or message-bus registers.

Table 4-2. Referenced I/O Register Access Method Example (HSTS Register)

Type: I/O Register (Size: 8 b)	HSTS: [_IOBAR] + 0h _IOBAR Type: PCI Configuration Register (Size: 32 b) _IOBAR Reference: [B:0, D:31, F:3] + 20h

4.1.3 PCI Configuration Register Access

Access to PCI configuration space registers is performed through one of two different configuration access methods (CAMs):

- I/O-indexed—PCI CAM
- Memory-mapped—PCI Enhanced CAM (ECAM)

Each PCI function has a standard PCI header consisting of 256 B for the I/O-access scheme (CAM), or 4096 B for the enhanced memory-access method (ECAM). Invalid read accesses return binary strings with all bits set to '1'.

Table 4-3. PCI Register Access Method Example (VID Register)

Type: PCI Configuration Register (Size: 16 b)	VID: [B:0, D:31, F:3] + 0h

4.1.3.1 PCI Configuration Access—CAM: I/O Indexed Scheme

Accesses to configuration space using the I/O method relies on two 32 b I/O registers:

- CONFIG_ADDRESS—I/O Port CF8h
- CONFIG_DATA—I/O Port CFCh

These two registers are both 32 b registers in I/O space. Using this indirect access mode, software uses CONFIG_ADDRESS (CF8h) as an index register, indicating which configuration-space register to access, and CONFIG_DATA (CFCh) acts as a window to the register pointed to in CONFIG_ADDRESS. Accesses to CONFIG_ADDRESS (CF8h) are internally captured. Upon a read or write access to CONFIG_DATA (CFCh), configuration cycles will be generated to the PCI function specified by the address captured in CONFIG_ADDRESS. The format of the address is shown in Table 4-1, Fixed I/O Register Access Method Example (P80 Register).

Table 4-4. PCI CONFIG_ADDRESS Register (I/O PORT CF8h) Mapping

Field	CONFIG_ADDRESS Bits
Enable PCI Configuration Space Mapping	31
Reserved	30:24
Bus Number	23:16
Device Number	15:11

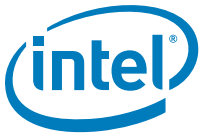


Table 4-4. PCI CONFIG_ADDRESS Register (I/O PORT CF8h) Mapping

Field	CONFIG_ADDRESS Bits
Function Number	10:08
Register/Offset Number	07:02
Note: Bit 31 of CONFIG_ADDRESS must be set for a configuration cycle to be generated.	

Pseudo code for a PCI register read is as follows:

```
Register_Snapshot= MEMREAD([Mem_BAR] + Register_Offset)

MyCfgAddr[23:16]= bus

MyCfgAddr[15:11]= device

MyCfgAddr[10:8]= funct

MyCfgAddr[7:2]= dWordMask(offset)

MyCfgAddr[31]= 1

IOWRITE(0xCF8, MyCfgAddr)

Register_Snapshot= IOREAD(0xCFC)
```

4.1.3.2 PCI Configuration Access—ECAM: Memory Mapped Scheme

A flat, 256 MiB memory space may also be allocated to perform configuration transactions. This is enabled through the BUNIT.BECREG message bus register (Port: 3h, Register: 27h) found in the SoC. BUNIT.BECREG allows remapping this 256 MiB region anywhere in physical memory space. Memory accesses within the programmed MMIO range result in configuration cycles to the appropriate PCI devices specified by the memory address as shown in Table 4-4, PCI CONFIG_ADDRESS Register (I/O PORT CF8h) Mapping.

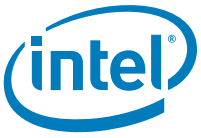
ECAM Memory Address Field	ECAM Memory Address Bits
Use from BAR: BUNIT.BECREG[31:28]	31:28
Bus Number	27:20
Device Number	19:15
Function Number	14:12
Register Number	11:02

ECAM Memory Address Field	ECAM Memory Address Bits
Use from BAR: BUNIT.BECREG[31:28]	31:28
Bus Number	27:20
Device Number	19:15
Function Number	14:12
Register Number	11:02

Note: ECAM accesses are only possible when BUNIT.BECREG.ECENABLE (bit 0) is set.

Pseudo code for an enhanced PCI configuration register read is as follows:

```
MyCfgAddr[27:20]= bus
```



```
MyCfgAddr[19:15]= device

MyCfgAddr[14:12]= funct

MyCfgAddr[11:2]= dw_offset

MyCfgAddr[31:28]= BECREG[31:28]

Register_Snapshot= MEMREAD(MyCfgAddr)
```

4.2 Memory-Space Register Access Methods

4.2.1 Fixed Memory-Mapped Register Access

Fixed Memory-Mapped I/O (MMIO) registers are accessed by specifying their 32 b/39 b address in a memory transaction from the CPU core. This allows direct manipulation of the registers. Fixed MMIO registers are unmovable registers in memory space.

Table 4-5. Fixed Memory-Mapped Register Access Method Example (IDX Register)

Type: Memory-Mapped I/O Register (Size: 32 b)	IDX: FEC00000h

4.2.2 Variable Memory (Memory-Referenced) Register Access

The SoC uses programmable base address registers (BARs) to set a range of physical address (memory) locations that it will use to decode memory reads and writes from the CPU to directly access a register. These BARs act as pointers to blocks of actual memory-mapped I/O (MMIO) registers. To access a memory-referenced register for a specific base address, start with that base address and add the register's offset. Example pseudo code for a read is shown below:

```
Register_Snapshot= MEMREAD([Mem_BAR] + Register_Offset)
```

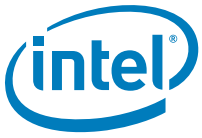
Base-address registers are often located in the PCI configuration space and are programmable by the BIOS/OS. Other common base address register types include fixed memory registers and I/O registers that point to MMIO register blocks.

Table 4-6. Memory-Mapped Register Access Method Example (_MBAR Register)

Type: Memory-Mapped I/O Register (Size: 8 b)	_MBAR Type: PCI Configuration Register (Size: 32 b) _MBAR Reference: [B:0, D:31, F:3] + 10h

4.3 Register Field Access Types

Access Type	Comments
RO	**Read-Only**
RO/C	Read-Only Clear on Read, loaded by HW
RO/Strap	Read-Only Strap
RO/V	**Read-Only Variable**
RO/V/P	**Read-Only Variable Sticky**



Access Type	Comments
RW	**Read-Write**
RW/L	**Read-Write Lock**
RW/1C	**Read-Write 1 to Clear (set by hardware, cleared by FW)**
RW/1C/HC	Read-Write 1 to Clear with Hardware Clear (set by hardware, cleared by FW or HW)
RW/1C/HC/L	Read-Write 1 to Clear with Hardware clear Lock
RW/1C/L	Read-Write 1 to Clear Lock
RW/1C/P	**Read-Write 1 to Clear Sticky (set by hardware, cleared by FW)**
RW/1C/P/L	Read-Write 1 to Clear Sticky Lock
RW/1S	**Read-Write 1 to Set, cannot be cleared**
RW/1S/HC	Read-Write 1 to Set with Hardware clear (set by FW, cleared by HW)
RW/1S/HC/L	Read-Write 1 to Set with Hardware Clear, Lock
RW/1S/1C/HC	Read-Write 1 to Set, write 1 to clear with hardware clear
RW/1S/1C/HC/L	Read-Write 1 to Set, write 1 to clear with hardware clear, Lock
RW/HC	Read-Write with Hardware Clear
RW/O	**Read-Write Once**
RW/O/L	Read-Write Once Lock
RW/O/P	Read-Write Once Sticky
RW/P	**Read-Write Sticky**
RW/P/L	Read-Write Sticky Lock
RW/P/Strap	Read-Write Sticky Strap
RW/Strap	Read-Write Strap
RW/V	**Read-Write Variable**
RW/V/L	**Read-Write Variable Lock**
WO	**Write-Only**
WO/L	Write-Only Lock

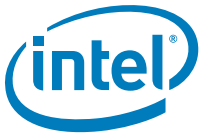
Table 4-7. Access Type Explanations

Base Access Type	Description
RO	Read Only: Writes to this register do not affect the register value. Reads return either a constant or variable device state.
RW	Read Write: Writes to this register setting alter the register value with the value written. Reads return the value of the register.
WO	Write Only: Writes to this register alters the register value. Original—Reads always return 0; revised—RTL will read reset, Saola mask read value, later Saola may change to check

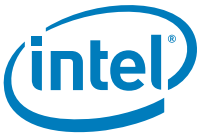
Table 4-8. Attributes/Modifiers are Applied to Base Access Types to Describe HW Interaction or Other Details

Attribute	Applicable Base Access Type	Description
/C	RO	Clear on Read: A read to the register will clear on a read to the register. Implies that HW modifies the register value.
/V	RO, RW	Variable: The read status is variable (not constant), and if the register is writable, reads do not return the write value, but return values that are dependant on other device or component state or other registers.
/P	RO, RW	PWROK: Reset only by loss of power (!PWROK). Also referred to as Sticky. The actual PWROK signal that is used as a reset depends on the power well the register is implemented in.
/L	RW, WO	Lock: Prior to the Lock bit being set (in a separate register), writes to the register load the register with the value written. Reads return the value of the register. This register is not writable once the lock bit is set. Reads to a locked register return the contents of the register. The Lock Bit itself typically has a /L attribute modifier and in some (rare) cases the Lock Bit could also have a /P modifier.
/1C	RW	Read Write 1 to Clear: Register that is set to '1' by hardware, and cleared to '0' by software writing a '1' to the register. Software writes of 0 have no effect.
/1S	RW	Read Write 1 to Set: Register that is set to '1' by software writing a '1' to the register. Software writes to 0 have no effect.
/HC	RW	Hardware Clear: Register that is cleared to '0' by hardware.
/O	RW	Write Once: This register may be written to any value once. After that, the register is Read Only.

Base Access	Attribute	HW Access	SW Access	Other
Type				
RO		none	readable, constant value	
RO	/C	loadable	readable, cleared on a read	
RO	/V	loadable	readable	
RO	/V/P	loadable	readable	reset by PWROK
RW		none	readable	
			writeable	
RW	/1C	settable	readable writeable (1 to clear, 0 has no effect)	intended to be single-bit field
RW	/1C/HC	settable clearable	readable writeable (1 to clear, 0 has no effect)	intended to be single-bit field
RW	/1C/HC/L	settable clearable	readable writeable when not locked (1 to clear, 0 has no effect)	intended to be single-bit field
RW	/1C/L	settable	readable writeable when not locked (1 to clear, 0 has no effect)	intended to be single-bit field



Base Access	Attribute	HW Access	SW Access	Other
RW	/1C/P	settable	readable writeable (1 to clear, 0 has no effect)	intended to be single-bit field reset by PWROK
RW	/1C/P/L	settable	readable writeable when not locked (1 to clear, 0 has no effect)	intended to be single-bit field reset by PWROK
RW	/1S	none	readable writeable (1 to set, 0 has no effect)	intended to be single-bit field
RW	/1S/1C/HC	settable clearable	readable writeable (1 to toggle, 0 has no effect)	intended to be single-bit field
RW	/1S/1C/HC/L	settable clearable	readable writeable when not locked (1 to toggle, 0 has no effect)	intended to be single-bit field
RW	/1S/HC	clearable	readable writeable (1 to set, 0 has no effect)	intended to be single-bit field
RW	/1S/HC/L	clearable	readable writeable when not locked (1 to set, 0 has no effect)	intended to be single-bit field
RW	/L	none	readable writeable when not locked	
RW	/O	none	readable writeable once (any value)	
RW	/O/L	none	readable writeable once when not locked (any value)	
RW	/O/P	none	readable writeable once when not locked (any value)	reset by PWROK
RW	/P	none	readable writeable	reset by PWROK
RW	/V	loadable	readable writeable	
RW	/V/L	loadable	readable writeable when not locked	For /V/L, Saola will have to behave the same as /V and will not lock since we cannot predicting the value
WO		none	reads return 0	

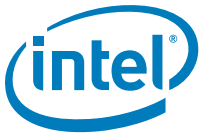


Base Access	Attribute	HW Access	SW Access	Other
			writeable	
WO	/L	none	reads return 0 writeable when not locked	

4.4 Alternate Access Mode

Although not a specific I/O register access mode, the ITSS implements a special Alternate Access mode to enable saving write-only (WO) registers during the state-save process. In this mode, subsequent reads to a fixed I/O register returns all of the ITSS WO-register values in sequence during state save; these values can then be written back to the appropriate registers during state restore.

§ §



5 MCHBAR

5.1 Registers Summary

Table 5-1. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6000h	6007h	Security Control Policy (C_CR_SECURITY_CP_0_0_0_MCHBAR)—Offset 6000h	0h
6008h	600Fh	Security Read Access Control Policy (C_CR_SECURITY_RAC_0_0_0_MCHBAR)—Offset 6008h	C0061210202h
6010h	6017h	Security Write Access Control Policy (C_CR_SECURITY_WAC_0_0_0_MCHBAR)—Offset 6010h	C0061210202h
6018h	601Fh	BIOSWR Control Policy (C_CR_BIOSWR_CP_0_0_0_MCHBAR)—Offset 6018h	C0061010202h
6020h	6027h	BIOSWR Read Access Control (C_CR_BIOSWR_RAC_0_0_0_MCHBAR)—Offset 6020h	80000C0063210217h
6028h	602Fh	BIOSWR Write Access Control (C_CR_BIOSWR_WAC_0_0_0_MCHBAR)—Offset 6028h	C00610C0212h
6030h	6037h	P_U_CODEWR_ALLRD Control Policy (C_CR_P_U_CODEWR_ALLRD_CP_0_0_0_MCHBAR)—Offset 6030h	40001000202h
6038h	603Fh	P_U_CODEWR_ALLRD Read Access Control Policy (C_CR_P_U_CODEWR_ALLRD_RAC_0_0_0_MCHBAR)—Offset 6038h	FFFFFFFFFFFFFFFFh
6040h	6047h	P_U_CODEWR_ALLRD Write Access Control Policy (C_CR_P_U_CODEWR_ALLRD_WAC_0_0_0_MCHBAR)—Offset 6040h	40001000202h
6050h	6057h	BIOS/PMC WR Control Policy (C_CR_BIOS_PMC_WR_CP_0_0_0_MCHBAR)—Offset 6050h	C0061210202h
6058h	605Fh	BIOS/PMC WR Read Access Control (C_CR_BIOS_PMC_WR_RAC_0_0_0_MCHBAR)—Offset 6058h	80000C0063210217h
6060h	6067h	BIOS/PMC WR Write Access Control (C_CR_BIOS_PMC_WR_WAC_0_0_0_MCHBAR)—Offset 6060h	C00612C0212h
6070h	6077h	P_U_PMC_CODEWR_ALLRD Control Policy (C_CR_P_U_PMC_CODEWR_ALLRD_CP_0_0_0_MCHBAR)—Offset 6070h	40001200202h
6078h	607Fh	P_U_PMC_CODEWR_ALLRD Read Access Control Policy (C_CR_P_U_PMC_CODEWR_ALLRD_RAC_0_0_0_MCHBAR)—Offset 6078h	FFFFFFFFFFFFFFFFh
6080h	6087h	P_U_PMC_CODEWR_ALLRD Write Access Control Policy (C_CR_P_U_PMC_CODEWR_ALLRD_WAC_0_0_0_MCHBAR)—Offset 6080h	40001200202h
6C80h	6C87h	Default VTd Base Address Register (DEFVTDBAR_0_0_0_MCHBAR_C)—Offset 6C80h	0h
6C88h	6C8Fh	Graphics VTd Base Address Register (GFXVTDBAR_0_0_0_MCHBAR_C)—Offset 6C88h	0h
6B60h		Noncached Region Control (B_CR_BNOCACHECTL_0_0_0_MCHBAR)—Offset 6B60h	0h

5.1.1 Security Control Policy (C_CR_SECURITY_CP_0_0_0_MCHBAR)—Offset 6000h

Control policy register for the Security Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RO	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to update the CP, RAC, and WAC registers of the policy group.

5.1.2 Security Read Access Control Policy (C_CR_SECURITY_RAC_0_0_0_MCHBAR)—Offset 6008h

Read access control policy register for the Security Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061210202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061210202h RO	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to read the registers contained in the policy group.

5.1.3 Security Write Access Control Policy (C_CR_SECURITY_WAC_0_0_0_MCHBAR)—Offset 6010h

Write access control policy register for the Security Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061210202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061210202h RO	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to write the registers contained in the policy group.

5.1.4 BIOSWR Control Policy (C_CR_BIOSWR_CP_0_0_0_MCHBAR)—Offset 6018h

Control policy register for the BIOS Write Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to update the CP, RAC, and WAC registers of the policy group.

5.1.5 BIOSWR Read Access Control (C_CR_BIOSWR_RAC_0_0_0_MCHBAR)—Offset 6020h

Read access control policy register for the BIOS Write Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 80000C0063210217h

Bit Range	Default & Access	Field Name (ID): Description
63:0	80000C0063210217h RW	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to read the registers contained in the policy group.

5.1.6 BIOSWR Write Access Control (C_CR_BIOSWR_WAC_0_0_0_MCHBAR)—Offset 6028h

Write access control policy register for the BIOS Write Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C00610C0212h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C00610C0212h RW	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to write the registers contained in the policy group.

5.1.7 P_U_CODEWR_ALLRD Control Policy (C_CR_P_U_CODEWR_ALLRD_CP_0_0_0_MCHBAR)—Offset 6030h

Control policy register for the P-Code/U-Code Write, All Read Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001000202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001000202h RW	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to update the CP, RAC, and WAC registers of the policy group.

5.1.8 P_U_CODEWR_ALLRD Read Access Control Policy (C_CR_P_U_CODEWR_ALLRD_RAC_0_0_0_MCHBAR)—Offset 6038h

Read access control policy register for the P-Code/U-Code Write, All Read Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: FFFFFFFFFFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:0	FFFFFFFFF FFFFFFFh RO	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to read the registers contained in the policy group.

5.1.9 P_U_CODEWR_ALLRD Write Access Control Policy (C_CR_P_U_CODEWR_ALLRD_WAC_0_0_0_MCHBAR)—Offset 6040h

Write access control policy register for the P-Code/U-Code Write, All Read Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001000202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001000 202h RW	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to write the registers contained in the policy group.

5.1.10 BIOS/PMC WR Control Policy (C_CR_BIOS_PMC_WR_CP_0_0_0_MCHBAR)—Offset 6050h

Control policy register for the BIOS/PMC Write Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061210202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061210 202h RW	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to update the CP, RAC, and WAC registers of the policy group.

5.1.11 BIOS/PMC WR Read Access Control (C_CR_BIOS_PMC_WR_RAC_0_0_0_MCHBAR)—Offset 6058h

Read access control policy register for the BIOS/PMC Write Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 80000C0063210217h

Bit Range	Default & Access	Field Name (ID): Description
63:0	80000C0063210217h RW	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to read the registers contained in the policy group.

5.1.12 BIOS/PMC WR Write Access Control (C_CR_BIOS_PMC_WR_WAC_0_0_0_MCHBAR)—Offset 6060h

Write access control policy register for the BIOS/PMC Write Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C00612C0212h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C00612C0212h RW	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to write the registers contained in the policy group.

5.1.13 P_U_PMC_CODEWR_ALLRD Control Policy (C_CR_P_U_PMC_CODEWR_ALLRD_CP_0_0_0_MCHBAR)—Offset 6070h

Control policy register for the P-Code/U-Code/PMC Write, All Read Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001200202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001200202h RW	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to update the CP, RAC, and WAC registers of the policy group.

5.1.14 P_U_PMC_CODEWR_ALLRD Read Access Control Policy (C_CR_P_U_PMC_CODEWR_ALLRD_RAC_0_0_0_MCHBAR)—Offset 6078h

Read access control policy register for the P-Code/U-Code/PMC Write, All Read Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: FFFFFFFFFFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:0	FFFFFFFFFFFFFFFFh RO	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to read the registers contained in the policy group.

5.1.15 P_U_PMC_CODEWR_ALLRD Write Access Control Policy (C_CR_P_U_PMC_CODEWR_ALLRD_WAC_0_0_0_MCHBAR)—Offset 6080h

Write access control policy register for the P-Code/U-Code/PMC Write, All Read Policy Group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001200202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001200202h RW	**Security Attribute of Initiator Permission Enable (sai):** Each bit is associated with the SAI of an agent. When set to 1'b1, the associated agent is granted permission to write the registers contained in the policy group.

5.1.16 Default VTd Base Address Register (DEFVTDBAR_0_0_0_MCHBAR_C)—Offset 6C80h

This is the base address for the Default VT configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset the DEFVTd configuration space is disabled and must be enabled by writing a 1'b1 to DEFVTBAREN. BIOS programs this register after which the register cannot be altered. BIOS must write DEFVTDBAR and then immediately follow it up with a read to DEFVTDBAR to ensure that all copies of DEFVTDBAR in the system are updated.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:40	0h RO	**Reserved (RESERVED_1):** Reserved.
39	0h RO	**Default VTd Base Address Bit 40 (DEFVTDBAR_40_BIT):** Reserved for future growth to 40bit addressing in uServer. Will always be 1'b0 in the SoC.
38:12	0h RW	**Default VTd Base Address Register (DEFVTDBAR):** If DEFVTDBAR is enabled this field corresponds to bits 38:12 of the base address default IOMMU VTd configuration space. BIOS will program this register, resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the default VTd IOMMU register set. If DEFVTDBAR is enabled and incoming Request Address[38:12] matches DEFVTDBAR[38:12], the request targets the Default VTd BAR.
11:2	0h RO	**Reserved (RESERVED_0):** Reserved.
1	0h RW	**DEFVTDBAR Register Lock (LOCK):** This lock bit only impacts the Display copy of this register. In the C-Unit all register protection is implemented with SAI policy groups. This bit is maintained in the C-Unit for software observability. Display description: Locks the contents of the register, including itself.
0	0h RW/L	**Default VTd Base Address Range Enable (DEFVTDBAREN):** 0: DEFVTDBAR is disabled and does not claim any memory 1: DEFVTDBAR memory mapped accesses are claimed and decoded appropriately. This bit will remain 1'b0 if VTd capability is disabled.

5.1.17 Graphics VTd Base Address Register (GFXVTDBAR_0_0_0_MCHBAR_C)—Offset 6C88h

This is the base address for the Graphics VT configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset the GFXVT configuration space is disabled and must be enabled by writing a 1 to GFXVTBAREN. BIOS programs this register, after which the register cannot be altered. BIOS must write GFXVTDBAR, immediately follow it up with read of DEVEN_0_0_0_PCI, and then write (with value from read operation) to DEVEN_0_0_0_PCI, to ensure that all copies of GFXVTDBAR in the system are updated.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_1):** Reserved.
38:12	0h RW	**Graphics VT Base Address Register (GFXVTBAR):** This field corresponds to bits 39 to 12 of the base address GFXVT configuration space. BIOS will program this register, resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the GFXVT register set. All the Bits in this register are locked in LT mode.
11:2	0h RO	**Reserved (RESERVED_0):** Reserved.
1	0h RW	**GFXVTDBAR Register Lock (LOCK):** This lock bit only impacts the Display copy of this register. In the C-Unit all register protection is implemented with SAI policy groups. This bit is maintained in the C-Unit for software observability. Display description: Locks the contents of the register, including itself.
0	0h RW/L	**Graphics VT Base Address Range Enable (GFXVTBAREN):** 0: GFXVTBAR is disabled and does not claim any memory. 1: GFXVTBAR memory mapped accesses are claimed and decoded appropriately. This bit will remain 0 if VTd capability is disabled.

5.1.18 Noncached Region Control (B_CR_BNOCACHECTL_0_0_0_MCHBAR)—Offset 6B60h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**RESERVED_0 (Reserved):** Reserved.
0:0	0h RW	**ENABLE_NO_SNOOP (Enable No Snoop)**: When set, B-Unit compares bits 35:20 incoming addresses to Upper and Lower NoSnoop Bounds to see if the transaction should be prevented from issuing a processor snoop operation.

5.2 Registers Summary

Table 5-2. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1000h	1003h	DRAM Rank Population 0 (D_CR_DRP0)—Offset 1000h	10000000h

Table 5-2. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1008h	100Bh	DRAM Timing Register 0A (D_CR_DTR0A)—Offset 1008h	210702CBh
100Ch	100Fh	DRAM Timing Register 1A (D_CR_DTR1A)—Offset 100Ch	30481218h
1010h	1013h	DRAM Timing Register 2A (D_CR_DTR2A)—Offset 1010h	8C080C30h
1014h	1017h	DRAM Timing Register 3A (D_CR_DTR3A)—Offset 1014h	3002EA28h
1018h	101Bh	DRAM Timing Register 4A (D_CR_DTR4A)—Offset 1018h	30209149h
101Ch	101Fh	DRAM Timing Register 5A (D_CR_DTR5A)—Offset 101Ch	304200C2h
1020h	1023h	DRAM Timing Register 6A (D_CR_DTR6A)—Offset 1020h	20100000h
1024h	1027h	DRAM Timing Register 7A (D_CR_DTR7A)—Offset 1024h	D060C06h
1028h	102Bh	DRAM Timing Register 8A (D_CR_DTR8A)—Offset 1028h	CC50A18h
102Ch	102Fh	D-Unit ODT Control Register A (D_CR_DOCRA)—Offset 102Ch	0h
1030h	1033h	D-Unit Power Management Control 0 (D_CR_DPMC0)—Offset 1030h	0h
1034h	1037h	D-Unit Power Management Control 1 (D_CR_DPMC1)—Offset 1034h	10000028h
1038h	103Bh	DRAM Refresh Control (D_CR_DRFC)—Offset 1038h	1750h
103Ch	103Fh	D-Unit Scheduler (D_CR_DSCH)—Offset 103Ch	3901C08h
1040h	1043h	DRAM Calibration Control (D_CR_DCAL)—Offset 1040h	1057h
1044h	1047h	VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 104Ch	20000h
104Ch	104Fh	VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 104Ch	0h
1050h	1053h	Periodic DRAM Temperature Polling Control (TQ) (D_CR_TQCTL)—Offset 1050h	6C000008h
1054h	1057h	TQ Temperature Offset Control (D_CR_TQOFFSET)—Offset 1054h	0h
1058h	105Bh	D-Unit Control Operations (D_CR_DCO)—Offset 1058h	0h
10A4h	10A7h	Data Scrambler (D_CR_SCRAMCTRL)—Offset 10A4h	0h
10ACh	10AFh	Error Injection Address Register (D_CR_ERR_INJ)—Offset 10ACh	0h
10B0h	10B3h	Error Injection Control Register (D_CR_ERR_INJ_CTL)—Offset 10B0h	0h
10B4h	10B7h	Error Log Register (D_CR_ERR_ECC_LOG)—Offset 10B4h	0h
10BCh	10BFh	D-Unit Fuse Status (D_CR_DFUSESTAT)—Offset 10BCh	0h
1124h	1127h	Major Mode Control (D_CR_MMC)—Offset 1124h	2B01E518h
1128h	112Bh	Major Mode RD/WR Counter (Set A and B) (D_CR_MMRDWR_AB)—Offset 1128h	1F207C8h
112Ch	112Fh	Major Mode RD/WR Counter (Set C and D) (D_CR_MMRDWR_CD)—Offset 112Ch	1F207C8h
1130h	1133h	Access Class Initial Priority (D_CR_ACCIP)—Offset 1130h	17C2h
1134h	1137h	Access Class 0 Priority Promotion Control (D_CR_RD_PROM0)—Offset 1134h	1F52940h
1138h	113Bh	Access Class 1 Priority Promotion Control (D_CR_RD_PROM1)—Offset 1138h	14000000h
113Ch	113Fh	Access Class 2 Priority Promotion Control (D_CR_RD_PROM2)—Offset 113Ch	0h
1140h	1143h	Access Class 3 Priority Promotion Control (D_CR_RD_PROM3)—Offset 1140h	1F29400h
1144h	1147h	Access Class 4 Priority Promotion Control (D_CR_RD_PROM4)—Offset 1144h	1F5294Ah
1148h	114Bh	Deadline Threshold (D_CR_DL_THRS)—Offset 1148h	6h

Table 5-2. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
114Ch	114Fh	Major Mode Blocking Rules Control (D_CR_MM_BLK)—Offset 114Ch	1800h
1154h	1157h	DRAM Self-Refresh Command (D_CR_DRAM_SR_CMD)—Offset 1154h	0h
1180h	1183h	DQS Retraining Control (D_CR_DQS_RETRAINING_CTL)—Offset 1180h	0h
1184h	1187h	MR4 De-Swizzle Control (D_CR_MR4_DESWIZZLE)—Offset 1184h	0h

5.2.1 DRAM Rank Population 0 (D_CR_DRP0)—Offset 1000h

Rank configuration register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**DRAM Device Per Rank (DRAMDEVICE_PR):** Specifies the number of DRAM devices that are ganged together to form a single rank. • 00: 1 DRAM device in each rank. • 01: 2 DRAM devices in each rank. • 10: 4 DRAM devices in each rank. • 11: 8 DRAM devices in each rank. Note: The actual number of devices is one more than the value programmed when ECC is enabled.
29:28	1h RW	**Address Decode (ADDRDEC):** Specifies the address mapping to be used: • 00: 1KB (A). • 01: 2KB (B). • 10: 4KB (C). • 11: Reserved.
27:25	0h RW	**Burst Length Mode (BLMODE):** • 000: Fixed BL8. • 001: Onthefly BL8. • 010: Fixed BL16. • 011: Onthefly BL16. • 100: Fixed BL32. • 101: Onthefly BL32. • 110-111: Reserved.

Bit Range	Default & Access	Field Name (ID): Description
24:22	0h RW	**DRAM Type (DRAMTYPE):** • 000: DDR3L. • 001: LPDDR3. • 010: LPDDR4. • 011: Reserved. • 100: Reserved. • 101-111: Reserved. Note: The D-Unit should only use this field if allowed by fuse.
21	0h RW	**ECC Enable (ECCEN):** • 0: ECC is disabled. • 1: ECC is enabled. This bit determines if the D-Unit treats the PMI BE_ECC bits as ECC bits or Byte Enables. The D-Unit should not allow this bit to be set if ECC is disabled by fuse. This should only be used in configurations that support ECC (DDR3L).
20:19	0h RW	**CA Swizzle Type (CASWIZZLE):** • 00: uniDIMM/SODIMM. • 01: BGA. • 10: BGA mirrored (LPDDR3 Only). • 11: UDIMM (DDR3L Only).
18:16	0h RO	**Reserved (RSVD18_16):** Reserved.
15	0h RW	**Bank Address Hashing Enable (BAHEN):** See Address Mapping section for full description. • 0: Bank Address Hashing disabled. • 1: Bank Address Hashing enabled.
14	0h RW	**Rank Select Interleave Enable (RSIEN):** See Address Mapping section for full description. • 0: Rank Select Interleaving disabled. • 1: Rank Select Interleaving enabled.
13:9	0h RO	**Reserved (RSVD13_9):** Reserved.
8:6	0h RW	**DRAM Device Density (DDEN):** Density of the DRAM devices populated on Ranks 0 and 1. • 000: 4 Gb. • 001: 6 Gb. • 010: 8 Gb. • 011: 12 Gb. • 100: 16 Gb. • 101-111: Reserved. Note: For LPDDR4 this value is the die density.

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**DRAM Device Data Width (DWID):** Data width of the DRAM device populated on Ranks 0 and 1. • 00: x8. • 01: x16. • 10: x32. • 11: x64.
3	0h RO	**Reserved (RSVD3):** Reserved.
2	0h RW	**Dual Data Mode Enable (DDMEN):** • 0: PMI Dual Data Mode is disabled in D-Unit, full cacheline read and writes go through a single D-Unit. • 1: PMI Dual Data Mode is enabled, only half cacheline read/ writes go through a single D-Unit.
1	0h RW	**Rank Enable 1 (RKEN1):** Enable Rank 1: Must be set to 1 to enable use of this rank.
0	0h RW	**Rank Enable 0 (RKEN0):** Enable Rank 0: Must be set to 1 to enable use of this rank. Note: Setting this bit to 0 is not a functional mode.

5.2.2 DRAM Timing Register 0A (D_CR_DTR0A)—Offset 1008h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 210702CBh

Bit Range	Default & Access	Field Name (ID): Description
31:25	10h RW	**Valid Clocks Before CKE High [tCKCKEH/tCSCKEH/tCKSRX] (TCKCKEH):** Number of valid clocks before CKE high (in DRAM clocks). • LPDDR4: The value in this register covers both tCKCKEH and tCSCKEH. • DDR3L/LPDDR3: The value covers tCKSRX which is defined as the number of valid DRAM clocks that have to toggle before the issuing of the Self Refresh Exit SRX. This value is also used if the clock frequency is changed or the clock is stopped or tristated during Power Down i.e. the number valid DRAM clocks that have to toggle before the issuing of the Power Down Exit PDX command. tCKCKEH can be used to compensate for clock stabilization delays in the motherboard. Note: D-unit hardware enforces minimum of two SPID clock before CKEH, any value in this register is the additional time.

Bit Range	Default & Access	Field Name (ID): Description
24:21	8h RW	**Exit Self-Refresh to Valid Commands Requiring a Locked DLL Delay [tXSDLL] (TXSDLL):** D-Unit waits max(tXSR+tZQCL/ tZQCS, tXSDLL) before allowing traffic to DRAM (in 64 x DRAM Clocks). LPDDR3/LPDDR4: tXSDLL = 0. DDR3L: tXSDLL = tDLLK = 512 Clocks = 8 x 64 DRAM Clocks. Note: In the equation above, tZQCL/tZQCS = 0 if no ZQ is performed on SR exit.
20:12	70h RW	**Exit Self-Refresh to Valid Command Delay [tXS/tXSR] (TXSR):** DDR3L: tXS - Delay between Self Refresh Exit SRX to any DRAM Command not requiring DLL Lock. LPDDR/: tXSR - Delay between Self Refresh Exit SRX to any DRAM Command. (in DRAM clocks).
11:6	Bh RW	**Activate RAS to CAS Command Delay [tRCD] (TRCD):** Specifies the delay between a DRAM Activate command and a DRAM Read or Write command to the same bank (in DRAM clocks). Note: Derating adds 1.875ns to this timing.
5:0	Bh RW	**Precharge to Activate Command Delay of a Single Bank [tRPpb] (TRPPB):** Specifies the delay between a DRAM Precharge command and a DRAM Activate command to the same bank (in DRAM Clocks). Note : this CR should be constrained to a minimum of 4 in LPDDR3 and minimum of 8 in LPDDR4. Note: Derating adds 1.875ns to this timing.

5.2.3 DRAM Timing Register 1A (D_CR_DTR1A)—Offset 100Ch

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 30481218h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Exit Power Down to Next Command Delay [tXP] (TXP):** Specifies the delay from the DRAM Power Down Exit (PDX) command to any valid command (in DRAM clocks). Note: The value in this field must be programmed to tXPDLL when Slow Exit Mode Power-down is enabled for DDR3L.
26	0h RO	**Reserved (RSVD26):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
25:14	120h RW	**ZQ (long) Calibration Time [tZQCL/tZQCAL] (TZQCL):** • LPDDR3/DDR3L: tZQCL/tZQoper: Specifies the delay between the DRAM ZQ Calibration Long (ZQCL) command and any DRAM command during normal operation. • LPDDR4: tZQCAL: ZQ Calibration time (in DRAM clocks). Note: This field defines the ZQ Calibration Long delay during normal operation. It is not the same as tZQinit which uses the same ZQCL command but the delay is longer. tZQinit applies only during poweron initialization of the DRAM devices and tZQoper applies during normal operation. BIOS executes the DRAM initialization sequence so it has to ensure tZQinit is met and not the D-Unit.
13:6	48h RW	**ZQ Short Calibration Time [tZQCS] (TZQCS):** ZQCS to any DRAM Command Delay: Specifies the delay between the DRAM ZQ Calibration Short (ZQCS) command and any DRAM command (in DRAM clocks). DDR3L and LPDDR3 only. LPDDR4 does not support ZQCS command
5:0	18h RW	**ZQ Latch Time [tZQLAT] (TZQLAT):** Specifies the delay between the DRAM ZQ Calibration Latch command and any DRAM command (in DRAM clocks). LPDDR4 only.Not used in DDR3L/LPDDR3/.

5.2.4 DRAM Timing Register 2A (D_CR_DTR2A)—Offset 1010h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8C080C30h

Bit Range	Default & Access	Field Name (ID): Description
31:23	118h RW	**All Bank Refresh Cycle Time [tRFCab] (NRFCAB):** Specifies the delay between the REFab command to the next valid command. (in DRAM clocks)
22:21	0h RO	**Reserved (RSVD22_21):** Reserved.
20:17	4h RW	**CKE Minimum Pulse Width [tCKE] (TCKE):** Specifies the minimum time from CKEL to CKEH (in DRAM clocks).
16	0h RO	**Reserved (RSVD16):** Reserved.
15:0	C30h RW	**Refresh Interval Time [tREFI] (NREFI):** Specifies the average time between refresh commands. JEDEC Base Refresh Interval time (in DRAM clocks). Note: D-Unit will ignore the 2 LSBs of this field.

5.2.5 DRAM Timing Register 3A (D_CR_DTR3A)—Offset 1014h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3002EA28h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Read to Precharge Delay [tRDPRE] (TRTP):** Specifies the minimum delay between the DRAM Read and Precharge commands to the same bank (in DRAM clocks). • LPDDR3 Equation: = BL/2 + tRTP - 4. • LPDDR4 Equation: = BL/2 + Max (8, tRTP) - 8. • DDR3L Equation: = tRTP.
26:20	0h RW	**CAS to CAS Command Delay Adder (TCCD_INC):** Specifies the number of clocks to be added to turnaround times (for Stretch Mode). It increases delay between Read to Read or Read to Write commands (in 4 x DRAM clocks).
19:13	17h RW	**Write to Precharge Command Delay [tWRPRE] (TWTP):** Specifies the minimum delay between the DRAM Write command and the Precharge command to the same bank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tWTP = BL/2 + WL + tWR + 1. • DDR3L Equation: tWTP = BL/2 + CWL + tWR.
12:11	1h RW	**DRAM Command Valid Duration (TCMD):** Specifies the number of DRAM clocks a command is held valid on the DRAM Address and Control buses. 1N is the DDR3 basic requirement. 2N is the extended mode for board signal integrity. • 0h: Reserved. • 1h: 1 DRAM Clock (1N). • 2h: 2 DRAM Clocks (2N). • 3h: Reserved. Note: DDR3L only. tCMD must be set to 1N for LPDDR3/LPDDR4.
10:6	8h RW	**Write Latency [WL/CWL] (TCWL):** The delay between the internal write command and the availability of the first word of DRAM input data (in DRAM clocks).
5:0	28h RW	**Write CAS to Masked Write CAS Delay Same Bank (TWMWSB):** Specifies the minimum delay between DRAM Write command to Masked Write command to same bank (in DRAM clocks). • LPDDR4 Equation: tWMWSB = tCCDMW (BL16) or tCCDMW + 8 (BL32). Note: Masked Write operation in LPDDR4 is always BL16. D-Unit applies this timing for same rank as well as same bank.

5.2.6 DRAM Timing Register 4A (D_CR_DTR4A)—Offset 1018h

Specifies DRAM timings parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 30209149h

Bit Range	Default & Access	Field Name (ID): Description
31:24	30h RW	**Four Bank Activate Window [tFAW] (TFAW):** A rolling timeframe in which a maximum of four Activate commands can be issued to the same rank. This is to limit the peak current draw from the DRAM devices (in DRAM clocks).
23:18	8h RW	**Write to Read DQ Delay Different Ranks (TWRDR):** Specifies the delay from the start of a Write data burst of one rank to the start of a Read data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tWRDR = WL + tDQSSmax + BL/2 + tWPST - (RL + tDQSCKmin - tRPRE). • LPDDR4 Equation: tWRDR = WL - RL + BL/2 + 4 - tDQSCKmin. • DDR3L Equation: tWRDR = CWL + tDQSSmax + BL/2 + tWPST - (CL + tDQSCKmin - tRPRE). Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj.
17:12	9h RW	**Read to Write DQ Delay Different Ranks (TRWDR):** Specifies the delay from the start of a Read data burst of one rank to the Start of a Write data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tRWDR = RL + tDQSCKmax + BL/2 + tRPST - (WL + tDQSSmin - tWPRE). • LPDDR4 Equation: tRWDR = RL + tDQSCKmax + BL/2 - (WL - 2). • DDR3L Equation: tRWDR = CL + tDQSCKmax + BL/2 + tRPST - (CWL + tDQSSmin - tWPRE). Note: For LPDDR3/4 using ODT, this latency may need to be adjusted by tODTon. Note: For DDR3L using ODT, this latency may need to be increased by one clock.
11:6	5h RW	**Write to Write DQ Delay Different Ranks (TWWDR):** Specifies the delay from the start of a Write data burst of one rank to the start of a Write data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tWWDR = BL/2 + tDQSSmax - tDQSSmin + tWPRE. • LPDDR4 Equation: tWWDR = BL/2 + 4 - tDQSSmin. • DDR3L Equation: tWWDR = BL/2 + tDQSSmax - tDQSSmin + tWPRE. Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj.
5:0	9h RW	**Read to Read DQ Delay Different Ranks (TRRDR):** Specifies the delay from the start of a Read data burst of one rank to the Start of a Read data burst of a different rank (in DRAM clocks). • LPDDR3/4 Equation: tRRDR = BL/2 + tDQSCKmax - tDQSCKmin + tRPRE. • DDR3L Equation: tRRDR = BL/2 + tRPST + tDQSCKmax - tDQSCKmin + tRPRE + 1.

5.2.7 DRAM Timing Register 5A (D_CR_DTR5A)—Offset 101Ch

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

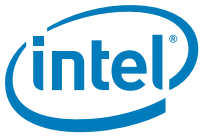
Default: 304200C2h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Row Activation to Row Activation Delay [tRRD] (TRRD):** Specifies the minimum delay in DRAM clocks between two DRAM Activate commands to the same rank but different banks (tRC is the minimum delay between activations of the same bank). Note: Derating adds 1.875ns to this timing.
26	0h RO	**Reserved (RSVD26):** Reserved.
25:23	0h RW	**Derate Increment (TDERATE_INC):** Specifies the additional delay that is added to DRAM timing when indicated by MR4 status. (in DRAM clocks) LPDDR3/LPDDR4: Value is 1.875ns. Note: The value in this register is only added to these timing parameters: tRCD, tRAS, tRP and tRRD.
22:18	10h RW	**Write to Write DQ Delay Same Rank (TWWSR):** Specifies the delay from a DRAM Write to another Write command of the same rank (in DRAM clocks). LPDDR3/LPDDR4/DDR3L Equation: tRRSR = tCCD.
17:13	10h RW	**Read to Read DQ Delay Same Rank (TRRSR):** Specifies the delay from a DRAM Read to another Read command of the same rank (in DRAM clocks). LPDDR3/LPDDR4/DDR3L Equation: tRRSR = tCCD.
12:6	3h RW	**Write to Read DQ Delay Same Rank (TWRSR):** Specifies the delay from a DRAM Read to Write command of the same rank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tWRSR = WL + tDQSSmax + BL/2 + tWTR. • DDR3L Equation: tWRSR = CWL + tDQSSmax + BL/2 + tWPST + tWTR.
5:0	2h RW	**Read to Write DQ Delay Same Rank (TRWSR):** Specifies the delay from a DRAM Read to a Write command of the same rank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tRWSR = RL + tDQSCKmax + BL/2 - WL + tWPRE. • DDR3L Equation: tRWSR = CL + tDQSCKmax + BL/2 + tRPST - (CWL +tDQSSmin - tWPRE). Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj. Note: For DDR3L using ODT, this latency may need to be increased by one clock.

5.2.8 DRAM Timing Register 6A (D_CR_DTR6A)—Offset 1020h

Specifies DRAM timing parameters.

Access Method



Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 20100000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	20h RW	**Opportunistic Refresh Idle Timer (OREFDLY):** Rank idle period that defines an opportunity for refresh (in DRAM clocks).
23:19	2h RW	**Valid Clocks After CKE Low [tCKELCK/tCKELCS/tCPDED/tCKSRE] (TCKCKEL):** Specifies the amount of time that DRAM clocks need to toggle after CKE goes low (in DRAM Clocks). • For /LPDDR3, this covers tCPDED. • For LPDDR4, this covers both tCKELCK and tCKELCS. • For DDR3L, this is tCKSRE. Note: D-Unit hardware enforces minimum of one SPID clocks after CKEL, any value in this register is the additional time.
18:15	0h RW	**Maintenance Operation Delay (MNTDLY):** When a critical read request is pending in RPQ and a maintenance operation (MRR, ZQCal, Ref, etc, panic refresh is an exception to this delay.) needs to be performed, D-Unit waits this amount of time before performing the maintenance operation to allow for some high priority requests to be issued (in 4x SPID clocks).
14:8	0h RW	**Mode Register Read to Any Command Delay (TPSTMRRBLK):** Specifies the quiet time after issuing MRR command (in DRAM Clocks). Note: D-Unit treats MRR as a read and always applies relevant turnaround times, any value programmed in this CR must be greater than those turnaround times for D-Unit to enforce any additional time from MRR to the next read/write.
7	0h RO	**Reserved (RSVD7):** Reserved.
6:0	0h RW	**Any Command to Mode Register Read/Write Delay (TPREMRBLK):** Specifies the quiet time before issuing MRR/MRW command. (in DRAM clocks). Note: D-Unit treats MRR as a read and always applies relevant turnaround times, any value programmed in this CR must be greater than those turnaround times for D-Unit to enforce any additional time from previous read/writes.

5.2.9 DRAM Timing Register 7A (D_CR_DTR7A)—Offset 1024h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: D060C06h

Bit Range	Default & Access	Field Name (ID): Description
31:26	3h RW	**All Bank Precharge to Activate Command Delay [tRPab] (TRPAB):** Specifies the delay between a DRAM Precharge All Bank command and a DRAM Activate command (in DRAM Clocks). Note: This CR should be constrained to a minimum of 4 in LP3 and minimum of 8 in LP4. Note: Derating adds 1.875ns to this timing. • For LPDDR, tRPpb = tRP, tRPab = tRP + 3ns. • For DDR3L 8ch tRPpb = tRPab = tRP.
25:23	2h RW	**Mode Register Write to any Command Delay [tMRD/tMRW] (TPSTMRWBLK):** Specifies the quiet time after issuing MRW command (in 8 x DRAM clocks). Note: This time covers for both tMRD and tMRW.
22:16	6h RW	**Write Command to Power Down Delay [tWRPDEN] (TWRPDEN):** Specifies the minimum time between a write command to PowerDown command (in DRAM clocks). Must be at least equal to tWR + tCCD + tWL + 2.
15:9	6h RW	**Read Command to Power Down Delay [tRDPDEN] (TRDPDEN):** Specifies the minimum time between a read command to PowerDown command (in DRAM clocks). Must be at least equal to CL/RL + tDQSCKmax + tCCD + tRPST.
8:7	0h RO	**Reserved (RSVD8_7):** Reserved.
6:0	6h RW	**Row Activation Period [tRAS] (TRAS):** Specifies the minimum delay between the DRAM Activate and Precharge commands to the same bank (in DRAM clocks). Note: Derating adds 1.875ns to this timing.

5.2.10 DRAM Timing Register 8A (D_CR_DTR8A)—Offset 1028h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: CC50A18h

Bit Range	Default & Access	Field Name (ID): Description
31:26	3h RW	**Minimum Self-Refresh Time [tSR/tCKESR] (TCKESR):** Specifies the minimum time that DRAM should remain in SR (in DRAM clocks).
25:21	6h RW	**Minimum Low Power Mode Residency (LPMDRES):** Specifies the minimum time that PHY should remain in LPMode (in DRAM clocks).

Bit Range	Default & Access	Field Name (ID): Description
20:15	Ah RW	**Low Power Mode Exit to Clock Enable Delay (LPMDTOCKEDLY):** Specifies the minimum time between the LP Mode exit to the CK stop/tristate deassertion and powerdown exit (in DRAM clocks). Note: Must be equal to t_idle_latency and less than 0x3C.
14:8	Ah RW	**Clock Stop to Low Power Mode Delay (CKETOLPMDDLY):** Specifies the time between CK stop/tristate to the Low Power Mode entry. This timing parameter is used to delay Low Power Mode entry (in DRAM clocks). Note: Must be at least equal to t_idle_length parameter and less than 0x7C.
7:0	18h RW	**Power Down Idle Timer (PWDDLY):** This is a non-JEDEC timing parameter used to delay powerdown entry (in DRAM clocks).

5.2.11 D-Unit ODT Control Register A (D_CR_DOCRA)—Offset 102Ch

Specifies the parameters to control DRAM ODT.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29	0h RW	**Rank 1 Read ODT Control (R1RDODTCTL):** Specifies the behavior of ODT signals when a Read command is issued to Rank 1. 0 - Read ODT is disabled for Rank 1 1 - Assert ODT to for Rank 0 (non-targeted Rank) Note: This register should be set to 0 for LPDDR3 devices
28	0h RW	**Rank 0 Read ODT Control (R0RDODTCTL):** Specifies the behavior of ODT signals when a Read command is issued to Rank 0. 0 - Read ODT is disabled for Rank 0 1 - Assert ODT to for Rank 1 (non-targeted Rank) Note: This register is reserved for LPDDR3 devices

Bit Range	Default & Access	Field Name (ID): Description
27:26	0h RW	**Rank 1 Write ODT Control (R1WRODTCTL):** Specifies the behavior of ODT signals when a Write command is issued to Rank 1. 00 - Write ODT is disabled 01 - Assert ODT to Rank 0 (non-targeted Rank) 10 - Assert ODT to Rank 1 (targeted Rank) 11 - Assert ODT to Rank 0 and Rank 1 Note: 10 and 11 are reserved values for LPDDR3
25:24	0h RW	**Rank 0 Write ODT Control (R0WRODTCTL):** Specifies the behavior of ODT signals when a Write command is issued to Rank 0. 00 - Write ODT is disabled 01 - Assert ODT to Rank 0 (targeted Rank) 10 - Assert ODT to Rank 1 (non-targeted Rank) 11 - Assert ODT to Rank 0 and Rank 1 Note: 10 and 11 are reserved values for LPDDR3
23:18	0h RO	**Reserved (RSVD23_18):** Reserved.
17:14	0h RW	**Read ODT assertion to de-assertion delay (DDR3L Only) (RDODTSTOP):** Specifies Read ODT assertion to ODT de-assert delay (in DRAM clocks). DDR3L Equation: RDODTSTOP = DOCRx.WRODTSTOP (subtract 1 if DOCRx.WRODTSTART = 1 in 2N mode).
13	0h RO	**Reserved (RSVD13):** Reserved.
12:9	0h RW	**Read command to ODT assertion delay (DDR3L Only) (RDODTSTART):** Specifies Read ODT assertion delay after Read Command (in DRAM clocks). DDR3L Equation: RDODTSTART = CL CWL (add 1 if DOCRx.WRODTSTART = 0 in 2N mode). The max value for this CR is 0xE
8:5	0h RW	**Write ODT Assertion to De-assertion Delay (WRODTSTOP):** Specifies number of clocks after ODT assertion that D-Unit deasserts ODT signal (in DRAM clocks). LPDDR3 Equation: WRODTSTOP = RU(tODTon(max)/tCK) + RU((tDQSSmax+tWPST)/tCK) + BL/2 - RD(tODToffmin/tCK) DDR3L Equation: WRODTSTOP >= 6
4	0h RO	**Reserved (RSVD4):** Reserved.
3:0	0h RW	**Write command to ODT assertion delay (WRODTSTART):** Specifies number of clocks after Write command that D-Unit asserts ODT signal (in DRAM clocks). LPDDR3 Equation: WRODTSTART = WL - RU(tODTon(max)/tCK) DDR3L Equation: WRODTSTART = 0 Note: DDR3 spec requires ODT to be asserted high when the DRAM Write command is issued. In DDR3L 2N mode the value can be set to 0 to assert ODT one DRAM clock earlier than the Write Command (WR) or set to 1 to assert at the same clock as command (CS assertion). The max value for this CR is 0xE

5.2.12 D-Unit Power Management Control 0 (D_CR_DPMC0)—Offset 1030h

Specifies the parameters to control D-Unit power management features.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD31_29):** Reserved.
28:24	0h RW	**SUSPEND/SUSPENDP Power Management Message Opcode (SUSPMOP):** DDRIO PHY Power Mode Opcode: After the D-Unit has placed the DRAM devices in Self Refresh/PASR mode as the result of a SUSPEND/SUSPENDP message, it sends this 5-bit value to the DDRIO PHY to tell it which power saving mode it should enter. Changing this register value while in SUSPEND will have no effect. Note: This opcode cannot be a PM state where it disables PHY PLLs i.e PM7 in LPDDR PHY.
23	0h RO	**Reserved (RSVD23):** Reserved.
22	0h RW	**PM Message Wait for Clock Gate Enable (SRPMCLKW):** Specifies when it is safe to send PM message to the PHY. When enabled, D-Unit waits for SPID Clock to deassert before sending a PM message on SR entry. • 0: D-Unit will not wait for SPID_clk to deassert before sending the PM message to PHY. • 1: D-Unit will wait for SPID_clk to deassert before sending PM message to the PHY. Note: The value must be 1 when DYNPMOP = 7h.
21:17	0h RW	**Dynamic Self-Refresh Power Management Message Opcode (DYNPMOP):** DDRIO PHY Power Mode Opcode: After the D-Unit has placed the DRAM devices in Self Refresh mode as the result of a Dynamic Self-Refresh, it sends this 5bit value to the DDRIO PHY to tell it which power saving mode it should enter. Changing this register value while in self-refresh will only change the PM state for the next entry in DynSR.
16	0h RW	**Dynamic Self-Refresh Enable (DYNSREN):** When set to 1, the D-Unit will automatically control DRAM Self Refresh entry and exit based on interface state and requests in pending queues. When there is no pending request in the queues and PMI is idle, then the D-Unit will place the DRAM devices in Self Refresh mode. The DRAM devices will be brought out of Self-Refresh when idle conditions don't hold.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Self-Refresh Entry Delay (SREDLY):** Specifies the minimum time the D-Unit will wait before it enters Dynamic Self-Refresh mode when idle (in 16x DRAM Clocks). Note: The value in this field needs to be minimum of 4 in functional mode and minimum of 50 in PSMI mode.

5.2.13 D-Unit Power Management Control 1 (D_CR_DPMC1)—Offset 1034h

Specifies the parameters to control D-Unit power management features.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10000028h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29	0h RW	**D-Unit Repeaters Clock Gate Disable (RPTCLKGTDIS):** Setting this bit to 0 allows majority of the repeaters between D-Unit and PHY to clock gate when there is no activity in order to save power. 0 - Enable Repeaters clock gating, 1 - Disable Repeaters clock gating. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.
28	1h RW	**IOSF-SB End Point Clock Gate Disable (SBEPCLKGTDIS):** Setting this bit to 0 enables the clock gating of IOSF-SB End Points in D-Unit and CPGC when there is no IOSF-SB activity in order to save power. 0 - Enable IOSF-SB EP clock gating, 1 - Disable IOSF-SB clock gating. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.
27	0h RW	**Local Clock Gate Disable (CLKGTDIS):** Setting this bit to 0 allows the majority of the D-Unit clocks to be gated off when there is no activity in order to save power. When set to 1, D-Unit clockgating is disabled. • 0: Enable. • 1: Disable. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.

Bit Range	Default & Access	Field Name (ID): Description
26	0h RW	**Chip Select Tristate Enable (CSTRIST):** • 0: The DRAM CS pins associated with the enabled ranks are never tristated. • 1: The DRAM CS pins are tristated when DRAM clock is stopped or tristated. Note: CS is not tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1).
25:24	0h RW	**Command/Address Tristate (CMDTRIST):** • 00: The DRAM CA pins are never tristated. • 01: The DRAM CA pins are only tristated when all enabled CKE pins are low. • 10: The DRAM CA pins are tristated when not driving a valid command. • 11: Reserved
23:16	0h RW	**Partial Array Self-Refresh Segment Mask (PASR):** This is the Segment Mask used for the MRW to enable PASR during SUSPENDP (Partial Array Self Refresh entry).
15:8	0h RW	**Page Close Timeout Period (PCLSTO):** Specifies the time from the last access of a DRAM page until that page is scheduled to close by sending a Precharge command to DRAM (in 16 x DRAM clocks).
7	0h RW	**Page Close Timeout Disable (PCLSTODIS):** When disabled, D-Unit will not close the DRAM page when idle. • 0: Enable page close timer. • 1: Disable page close timer (Used during DRAM init and DDRIO training).
6	0h RO	**Reserved (RSVD6):** Reserved.
5	1h RW	**ODT Tristate Enable (ODTTRIST):** • 0: The DRAM ODT pins associated with the enabled ranks are never tristated. • 1: DRAMs ODT pins are tristated when DRAM clock is stopped or tristated. Note: ODT is not tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1)
4:3	1h RW	**Clock Stop/Tristate Enable (ENCKSTP):** Enable/Disable CK Stop/Tristate During Power down. • 00: Disable CK Stop/Tristate During Power down. • 01: Enable CK Stop During Power down. • 10: Enable CK Tristate During Power down. • 11: Reserved Note: CK is not stopped or tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1).

Bit Range	Default & Access	Field Name (ID): Description
2:1	0h RW	**Low Power Mode Opcode (LPMODEOP):** D-Unit will send the value in this register after it has entered Powerdown Mode and has stopped/tristated the clock. 00: Disable LPMode. Note: LPMODE entry is not possible when global tristate flow is disabled (DCBR.TRISTDIS = 1).
0	0h RW	**Disable Power Down (DISPWRDN):** Setting this bit to 1 disables dynamic control of DRAM Power-Down entry and exit by keeping the CKE pins driven high. BIOS may set it to 1 during DRAM initialization and DDRIO training. This bit should be set to 0 for normal operation. • 0: The D-Unit dynamically controls the CKE pins to place the DRAM devices in Power Down mode and bring them out of Power Down mode. • 1: The D-Unit constantly drives the CKE pins high to keep the DRAM devices from entering Power Down mode when ranks are idle. Note: This bit is overridden if CKEMODE = 1. This bit does not control CKE behavior on SR entry/exit.

5.2.14 DRAM Refresh Control (D_CR_DRFC)—Offset 1038h

Specifies the parameters to control scheduling of refresh commands.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1750h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD31_22):** Reserved.
21	0h RW	**Disable Refresh Debt Clear (DISREFDBTCLR):** When set, D-Unit will not clear refresh debt before Self Refresh SR Entry: • 0: D-Unit sends all postponed REF commands to DRAM before it enters Self Refresh. • 1: D-Unit enters SR without clearing the Refresh Debt (for Debug only).
20	0h RW	**Refresh Skew Disable (REFSKWDIS):** Disables Skewing of Refresh Counting between Ranks. Each rank has its own refresh counter. By default incrementing these refresh counters are skewed by 1/2 the tREFI period. Setting this bit to a 1 disables this feature and all refresh counters will increment at the same time per tREFI period. Skewing the tREFI counters can improve performance since traffic to all ranks does not have to be blocked to perform refresh. • 0: Incrementing the refresh counters are skewed by 1/2 tREFI period. • 1: All refresh counters will increment at the same time per tREFI period.

Bit Range	Default & Access	Field Name (ID): Description
19:18	0h RO	**Reserved (RSVD19_18):** Reserved.
17:16	0h RO	**Reserved (RSVD17_16):** Reserved.
15	0h RW	**Extra Refresh Debit (EXTRAREFDBT):** When set to 1, D-Unit adds one extra refresh debit (for a total of two) on Self-refresh exit.
14:12	1h RW	**Minimum Refresh Rate (MINREFRATE):** Ensures that refresh rate never drops below a certain limit regardless of TQ polling. • 000: Disable tREFI counter and stop issuing refresh commands. • 001: 0.25x refresh rate (i.e. 4x tREFI same as no limit). • 010: 0.5x refresh rate (i.e. 2x tREFI). • 011: 1x refresh rate (i.e. 1x tREFI). • 100: 2x refresh rate (i.e. 0.5x tREFI). • 101: 4x refresh rate (i.e. 0.25x tREFI). • 110: 4x refresh rate with derating forced on i.e. 0.25x tREFI. • 111: Reserved.
11:8	7h RW	**Refresh Panic Watermark (REFWMPNC):** When the Refresh counter per rank is greater than this value, the D-Unit will send a REF command to the rank regardless of pending requests. Note: REFWMPNC must be greater than or equal to REFWMHI and greater than 2, Max Value must be less than 8 to not violate 9xtREFI JEDEC requirement.
7:4	5h RW	**Refresh High Watermark (REFWMHI):** When the Refresh counter per rank is greater than this value, the D-Unit will send a REF command to the rank if there is no critical priority requests in the pending queues. Note: Value must be greater or equal to 1 and less than or equal to REFWMPNC.
3:1	0h RO	**Reserved (RSVD3_1):** Reserved.
0	0h RW	**Opportunistic Refresh Disable (OREFDIS):** Disable opportunistic scheduling of refresh. • 0: D-Unit will send a REF command only if there is no pending request to that rank. • 1: D-Unit will not send any opportunistic refreshes. Refresh commands are only sent when the refresh counter is greater than REFWMHI. Note: When set, DISREFDBTCLR must also be set to be able to enter SR.

5.2.15 D-Unit Scheduler (D_CR_DSCH)—Offset 103Ch

Specifies parameters to control scheduling of commands to DRAM.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3901C08h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:29	0h RW	**BGF Early Read Data Valid (BGF_EARLY_RDDATA_VALID):** Specifies the number of clocks the D-Unit sends the read data valid through the BGF earlier as compared to the data. • 00: Always write read valid in same SPID clock as data. • 01: Always write read valid one SPID clock before data. • 10: Write read valid up to 2 SPID clocks before data. • 11: Reserved
28:27	0h RW	**SPID Early Read Data Valid (SPID_EARLY_RDDATA_VALID):** Specifies the delay in SPID clocks from RDDATA_VALID assertion to actual data on SPID. The value should match what is programmed in DDRIO (PHY).
26:21	1Ch RW	**Write Pending Queue Count (WPQCOUNT):** Used to limit the number of available slots in Write Pending Queue/ Write Data Buffer. WPQCOUNT will only recognize changes when PMI ISM is not active.
20:16	10h RW	**Read Pending Queue Count (RPQCOUNT):** Used to limit the number of entries in Read Pending Queue. RPQCOUNT will only recognize changes when PMI ISM is not active.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:10	7h RW	**Read Return Data Additional Credits (BLKRDBF_ADD_RDDATA_CR):** Number of additional full cacheline (64B) read data return credits exposed to D-Unit when BLKRDBF is set. Note: The value in this field has no effect on Read return credits when BLKRDBF is not set.
9:8	0h RW	**In-Order Mode (INORDERMODE):** • 0h: In order mode disabled: Commands are sent out of order. • 1h: Partial in order mode: Read and Write CAS commands are sent in the order they were recieved. ACT and PRE can go out of order. • 2h: Full in order mode serialized test: All DRAM commands CAS ACT PRE associated with a PMI request are issued to DDR before any DRAM commands for a subsequent PMI request. • 3h: Reserved. In order modes should be enabled during init/training/CPGC testing. Should never be changed while the D-Unit queues are nonempty.
7	0h RW	**Idle Bypass Mode Enable (BYPASSEN):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Block When RDB Full (BLKRDBF):** When set D-Unit stops scheduling new read commands to DRAM when the read data buffer (RDB) is full.
5:4	0h RW	**Stretch Mode (STRETCHMODE):** When stretch mode is enabled, commands are initiated only on Phase 0 of SPIDClk. • 00: Stretch mode is disabled. • 01: Commands are initiated on Phase 0 of every SPID clocks. • 10: Commands are initiated on Phase 0 of even SPID clocks. • 11: Commands are initiated on Phase 0 of odd SPID clocks.
3:0	8h RW	**Masked Write Turnaround Delta (TMWR_TA_DELTA):** The value in this register is subtracted from Masked Write to Read, Masked Write to Write and Masked Write to Masked Write turnaround times to account for half BL MWr commands in LPDDR4. • LPDDR4: = MWr tCCD = MWr BL/2 = 8.

5.2.16 DRAM Calibration Control (D_CR_DCAL)—Offset 1040h

Specifies parameters to control ZQ Calibration.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1057h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ZQ Calibration Type (ZQCALTYPE):** Determines whether the ZQ Calibration is a long or short calibration command (due to ZQCALSTRT). 0: Short calibration (ZQCS). 1: Long calibration (ZQCL).
30	0h RW/V	**ZQ Calibration Start Rank 1 (ZQCALSTRTR1):** Set this bit to 1 to start the ZQ calibration sequence on Rank 1. This bit will remain a 1 until the ZQ calibration is complete for rank 1, then it will return to 0. 0: ZQ calibration is done. 1: ZQ calibration has started and is in progress.
29	0h RW/V	**ZQ Calibration Start Rank 0 (ZQCALSTRTR0):** Set this bit to 1 to start the ZQ calibration sequence on Rank 0. This bit will remain a 1 until the ZQ calibration is complete for rank 0, then it will return to 0. 0: ZQ calibration is done. 1: ZQ calibration has started and is in progress.
28:23	0h RO	**Reserved (RSVD28_23):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RW	**Self-Refresh Exit ZQ Calibration Control (SRXZQC):** • 00: On DynSR exit ZQ timer determines the ZQ type. When the state is lost (i.e due to AutoPG/S0ix) ZQCL is always performed. • 01: Always perform ZQCL after self refresh exit, in LPDDR4, ZQ with traffic blocked. • 10: Always perform ZQCS on SR exit. For LPDDR4, ZQ while traffic is allowed. • 11: No ZQCL commands are sent (it disables ZQCAL commands on SR exit).
20:18	0h RO	**Reserved (RSVD20_18):** Reserved.
17	0h RW	**ZQ Calibration Mode (ZQCLMODE):** Specifies how ZQCal commands are sent to different ranks. • 0: ZQCal commands are sent in parallel to all ranks. • 1: ZQCal commands are sent serially to each rank.
16	0h RW	**Periodic ZQ Calibration Disable (ZQCDIS):** • 0: Periodic ZQ Calibration is Enabled. • 1: Disable periodic ZQ Calibration.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:0	1057h RW	**ZQ Calibration Interval (ZQINT):** Specifies the time interval between two ZQCS (LPDDR3) or ZQ Start (LPDDR4) commands to a DRAM device. (in RTC 32.8KHz clocks)

5.2.17 VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 104Ch

Specifies parameters for VNN Scaling Timer in D-Unit. The values in this register will be set by P-code during VNN scaling period.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VNN Scaling Timer Enable (VNN_TIMER_EN):** • 0: The D-Unit VNN Scaling Timer is disabled. • 1: The D-Unit VNN Scaling Timer is enabled.
30:12	0h RO	**Reserved (RSVD30_12):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11:0	0h RW	**VNN Timer Time (VNN_TIMER_TIME):** The final timer value (in 16 x DRAM clocks).

5.2.18 Periodic DRAM Temperature Polling Control (TQ) (D_CR_TQCTL)—Offset 1050h

Specifies the control for periodic temperature monitoring and control of DRAM device.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6C000008h

Bit Range	Default & Access	Field Name (ID): Description
31:29	3h RW/V	**TQ Data Rank 1 (TQDATAR1):** If Rank 1 is disabled, this value will remain zero. This field contains the data of the last DRAM Mode Register Read to MR4 MRR issued. It is overwritten with each command.
28:26	3h RW/V	**TQ Data Rank 0 (TQDATAR0):** This field contains the data of the last DRAM Mode Register Read to MR4 MRR issued. It is overwritten with each command.
25:22	0h RO	**Reserved (RSVD25_22):** Reserved.
21:8	0h RW	**TQ Poll Period (TQPOLLPER):** This sets the frequency by which the D-Unit polls the DRAM mode register MR4 to determine required refresh rate (in 4x tREFI units).
7:5	0h RO	**Reserved (RSVD7_5):** Reserved.
4	0h RW	**Self Refresh Temperature Range Enable (DDR3 Only) (SRTEN):** When set, before every Self refresh entry, D-Unit writes a 1 to bit 7 of TQOFFSET.MR_VALUE when TQDATA for that rank indicates a value higher then 0x3, and writes a 0 to that bit otherwise. The new MR_VALUE is then written into MR2 of DDR3 for each enabled rank.
3	1h RW	**Enable Dynamic Timing Derating (ENDERATE):** When set to 1, the Dynamic Timing Derating is enabled. When the D-Unit determines (via TQ polling) that the DRAM requires timing derating in addition to refresh interval adjustment, the D-Unit will automatically adjust the relevant timing parameters.
2	0h RW	**Enable TQ Data Push (TQDATAPUSHEN):** When set to 1, D-Unit pushes the data form the last MR4 read to a punit register.
1	0h RW	**Enable TQ Poll on Self-Refresh Exit (TQPOLLSREN):** This bit enables MR4 read on Self Refresh Exit. If disabled, D-Unit will not read MR4 value on Self-Refresh exit.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Enable Periodic TQ Poll (TQPOLLEN):** This bit enables periodic TQ Poll. If disabled, D-Unit will not read MR4 value periodically. Note: Will be enabled only if refreshes are enabled.

5.2.19 TQ Temperature Offset Control (D_CR_TQOFFSET)—Offset 1054h

Specifies temperature offset and refresh rate adjustments requested by software.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:16	0h RW	**MR Value (MR_VALUE):** MR2 Shadow Register (DDR3L Only): BIOS writes the correct value of MR2 register in DDR3L into this field at boot time. D-Unit modifies one bit and rewrites the MR2 into DDR3L DRAM before SR entry.
15:11	0h RO	**Reserved (RSVD15_11):** Reserved
10:8	0h RW	**MR4 Adder (MR4_ADDER):** D-Unit adds the value of this field to TQDATA read from MR4 the resulting value is used to control refresh rate and AC timing derating.
7:3	0h RO	**Reserved (RSVD7_3):** Reserved.
2	0h RW/V	**MR3 Offset Update (MR3_OFFSET_UPDATE):** When set, D-Unit writes the merged value of MR3_VALUE and MR3_THERM_OFFSET into MR3 of DRAM. D-Unit clears this bit once the value is written.
1:0	0h RW	**MR3 Thermal Offset (MR3_THERM_OFFSET):** Reserved

5.2.20 D-Unit Control Operations (D_CR_DCO)—Offset 1058h

Specifies D-Unit initialization and control operation.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Initialization Complete (IC):** Indicates that initialization of the D-Unit has been completed. Memory accesses are permitted and maintenance operation begins. Until this bit is set to a 1, the memory controller will not accept DRAM requests from the Bunit/ GSA/2LM (PMI ISMs will not leave idle). Note: Set this bit to 1 only when all other D-Unit registers have been configured. Usually set at the last configuration step by BIOS on cold/warm reset. D-Unit hardware sets this bit on SR exit.
30	0h RO/V	**DDRIO PHY Initialization Complete (DIOIC):** Status indication that the DDRIO PHY initialization is complete reflects the status spid_init_complete signal.
29	0h RO	**Reserved (RSVD29):** Reserved.
28	0h RW	**PMI Control Select (PMICTL):** • 0: D-Unit PMI is connected to Bunit/GSA/2LM. • 1: D-Unit PMI is connected to CPGC. Note: D_CR_DSCH_BYPASSEN must be set to 0 in CPGC mode. Note: PMI must be idle and D-Unit BGF_RUN = 0 before changing the value in this register.
27:8	0h RO	**Reserved (RSVD27_8):** Reserved.
7:4	0h RO	**Reserved (RSVD7_4):** Reserved.
3	0h RW	**Enable PSMI Mode (PSMIEN):** When enabled, D-Unit will synchronize clock crossing signals. • 0: PSMI Mode is disabled. • 1: PSMI Mode is enabled. Note: Change only allowed when D-Unit is idle.
2	0h RW	**Maintenance Reset (MNTRST):** Writing a 1 to this field resets all maintenance timers. Clears all states and also clears refresh debt queues. This bit needs to be cleared by software after at least 3 SPID clocks.
1	0h RW	**Enable Maintenance Operations (MNTEN):** Setting this field to 1 enables all maintenance operations. When DCO.IC is set, the maintenance operations are enabled irrespective of the value of this field.
0	0h RO	**Reserved (RSVD0):** Reserved.

5.2.21 Data Scrambler (D_CR_SCRAMCTRL)—Offset 10A4h

Specifies parameters to control data scrambling in D-Unit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Data Scrambler (SCRM_EN):** When set to 1, data scrambling is enabled. When set to 0, data scrambling is disabled. Should be set before D_CR_BGF_CTL_BGF_RUN is set to 1.
30	0h RO	**Reserved (RSVD30):** Reserved.
29:28	0h RW	**Scrambler Clock Gate Select (CLOCKGATE):** This field controls how the scrambler output code is clock gated to reduce power. • 00: Clock gate disabled. • 01: Clock Gate every 2 cycle. • 10: Clock Gate every 3 cycle. • 11: Clock Gate every 4 cycle.
27:16	0h RO	**Reserved (RSVD27_16):** Reserved.
15:0	0h RW	**Scrambling Key (KEY):** Sets the key for the scrambler. The key should be a random value that is set following each cold boot.

5.2.22 Error Injection Address Register (D_CR_ERR_INJ)—Offset 10ACh

Contains the target address for ECC error injection.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:1	0h RW	**Error Injection Target Address (ADDRESS):** Specifies the PMI address of the write transaction to be injected with the error. Only applicable to Write transactions. Read/under-fill read of the partial write operation is not affected.
0	0h RO	**Reserved (RSVD0):** Reserved.

5.2.23 Error Injection Control Register (D_CR_ERR_INJ_CTL)—Offset 10B0h

Controls injecting correctable or uncorrectable errors into the write requests specified by target address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD31_4):** Reserved
3	0h RW	**Error Injection Type Higher 32B (SEL_HI):** If enabled, the error injection is continuously armed for ERR_INJ.ADDR 32B write address matching until it is cleared. • 00: No error injection. • 01: Uncorrectable Error (UE) is armed for write address matching to inject UE by using the same poisoning scheme, i.e. inverting corresponding write ECC[6:0] on QW0 of the 32B data. • 10: Correctable Error (CE) is armed for write address matching to inject CE by inverting corresponding write ECC[0] on QW0 of the 32B data. • 11: Reserved.
2	0h RW	**Error Injection Enable Higher 32B (EN_HI):** When set the error injection is continuously armed for higher 32B of D_CR_ERR_INJ_ADDR write address matching until it is cleared.
1	0h RW	**Error Injection Type Lower 32B (SEL_LO):** 0 - Uncorrectable Error (UE) is armed for write address matching to inject UE by using the same poisoning scheme, i.e. inverting corresponding write ECC[6:0] on every QW of the 32B data. 1 - Correctable Error (CE) is armed for write address matching to inject CE by inverting corresponding write ECC[0] on every QW of the 32B data.
0	0h RW	**Error Injection Enable Lower 32B (EN_LO):** When set, the error injection is continuously armed for lower 32B of D_CR_ERR_INJ_ADDR write address matching until it is cleared.

5.2.24 Error Log Register (D_CR_ERR_ECC_LOG)—Offset 10B4h

Detected ECC errors are captured in this register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Clear (CLEAR):** Setting this bit to one clears all fields in this register, including itself.

Bit Range	Default & Access	Field Name (ID): Description
30:29	0h RW	**PMI VISA Byte Select (ECC_VISA):** Select ECC or PMI byte on VISA : • 00: ECC byte, • 01: PMI Data Byte [7:0], • 10: PMI Data Byte [63:56], • 11: PMI Data Byte [255:248]
28	0h RW/V	**Correctable Single-bit Error (CERR):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. A multiple bit error that occurs after this bit is set will override the address/error syndrome information.
27	0h RW/V	**Uncorrectable Multiple-bit Error (MERR):** This bit is set when an uncorrectable multiple-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked until this bit is cleared.
26:25	0h RW/V	**Error Burst Number (ERR_BURST):** Burst number (in BL8) of the error within a chunk.
24	0h RW/V	**Error Chunk Number (ERR_CHUNK):** Chunk number of the error. 0 - lower 32B chunk has error if MERR/CERR is set 1 - higher 32B chunk has the error if MERR/CERR is set
23:16	0h RW/V	**Quad Word ECC Syndrome (SYNDROME_QW):** ECC Syndrome for a QW (64 bit) within 32B Address
15:0	0h RW/V	**Request Tag (TAG):** Read Return Tag matches with the PMI Request Tag which triggered the error log.

5.2.25 D-Unit Fuse Status (D_CR_DFUSESTAT)—Offset 10BCh

Contains the values read from D-Unit fuses.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD31_16):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**D-Unit Fuse Status (FUSESTAT):** D-Unit fuse bits are captured into this register and are available to be read. • [0]: fus_dun_ecc_dis. • [3:1]: fus_dun_max_supported_device_size[2:0]. • [4:4]: fus_dun_lpddr3_dis. • [5:5]: fus_dun_lpddr4_dis. • [6:6]: reserved. • [7:7]: fus_dun_ddr3l_dis. • [15:8]: reserved.

5.2.26 Major Mode Control (D_CR_MMC)—Offset 1124h

Specifies parameters to control read/write major mode operation and transitions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2B01E518h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:27	5h RW	**RAW Conflict Read Priority for WMM Transition (RAW_WMM):** If a conflict read reaches this priority (or greater depending on access class occupancy), WMM will be triggered to unblock the corresponding write. D-Unit will stay in WMM until corresponding write is issued. Note: The value in this bit must not be higher than lowest terminal priority level of each access class.
26	0h RO	**Reserved (RSVD26):** Reserved.
25:23	6h RW	**Read Isoch Trigger Priority (RIMPRIO):** If any read in the RPQ is at this programmable priority, RIM is triggered.
22:18	0h RO	**Reserved (RSVD22_18):** Reserved.
17:12	1Eh RW	**Write Isoch Threshold (WIMTHRS):** When the number of entries in WPQ is greater than or equal to this value (higher than WMM entry watermark, less than WPQ size), it triggers write isoch mode (WIM).
11:6	14h RW	**Write Major Mode Exit Watermark (WMMEXIT):** When the number of entries in WPQ is less than this value, the D-Unit will switch back to read major mode.

Bit Range	Default & Access	Field Name (ID): Description
5:0	18h RW	**Write Major Mode Entry Watermark (WMMENTRY):** When the number of entries in WPQ is greater than or equal to this value, the D-Unit will switch to write major mode (WMM). Note: the value must not be set to 0.

5.2.27 Major Mode RD/WR Counter (Set A and B) (D_CR_MMRDWR_AB)—Offset 1128h

Minimum read and maximum write counter control. This register defines the minimum number of reads in RMM and maximum number of writes in WMM before a mode transition happens.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F207C8h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:20	1Fh RW	**Max Writes B (MAXWRB):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set B).
19:14	8h RW	**Min Reads B (MINRDB):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set B).
13:12	0h RO	**Reserved (RSVD13_12):** Reserved.
11:6	1Fh RW	**Max Writes A (MAXWRA):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set A).
5:0	8h RW	**Min Reads A (MINRDA):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set A).

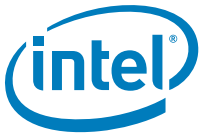
5.2.28 Major Mode RD/WR Counter (Set C and D) (D_CR_MMRDWR_CD)—Offset 112Ch

Minimum read and maximum write counter control. This register defines the minumum number of reads in RMM and maximum number of writes in WMM before a mode transition happens (sets C and D).

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F207C8h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:20	1Fh RW	**Max Writes D (MAXWRD):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set D).
19:14	8h RW	**Min Reads D (MINRDD):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set D).
13:12	0h RO	**Reserved (RSVD13_12):** Reserved.
11:6	1Fh RW	**Max Writes C (MAXWRC):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set C).
5:0	8h RW	**Min Reads C (MINRDC):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set C).

5.2.29 Access Class Initial Priority (D_CR_ACCIP)—Offset 1130h

Each field of this register defines the initial priority of one access class.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 17C2h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved (RSVD31_15):** Reserved.
14:12	1h RW	**Access Class 4 Initial Priority (AC4IP):** Initial priority level of read requests coming with access class 4.
11:9	3h RW	**Access Class 3 Initial Priority (AC3IP):** Initial priority level of read requests coming with access class 3.
8:6	7h RW	**Access Class 2 Initial Priority (AC2IP):** Initial priority level of read requests coming with access class 2.
5:3	0h RW	**Access Class 1 Initial Priority (AC1IP):** Initial priority level of read requests coming with access class 1.
2:0	2h RW	**Access Class 0 Initial Priority (AC0IP):** Initial priority level of read requests coming with access class 0.

5.2.30 Access Class 0 Priority Promotion Control (D_CR_RD_PROM0)—Offset 1134h

This register defines the priority promotion policy for access class 0. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F52940h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	Ah RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	Ah RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	Ah RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.2.31 Access Class 1 Priority Promotion Control (D_CR_RD_PROM1)—Offset 1138h

This register defines the priority promotion policy for access class 1. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the associated level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 14000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	Ah RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	0h RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

Bit Range	Default & Access	Field Name (ID): Description
19:15	0h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	0h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.2.32 Access Class 2 Priority Promotion Control (D_CR_RD_PROM2)—Offset 113Ch

This register defines the priority promotion policy for access class 2. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	0h RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	0h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	0h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.2.33 Access Class 3 Priority Promotion Control (D_CR_RD_PROM3)—Offset 1140h

This register defines the aging policy for access class 3. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F29400h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	5h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	5h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.2.34 Access Class 4 Priority Promotion Control (D_CR_RD_PROM4)—Offset 1144h

This register defines the aging policy for access class 3. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F5294Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	Ah RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	Ah RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	Ah RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	Ah RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.2.35 Deadline Threshold (D_CR_DL_THRS)—Offset 1148h

Specifies when the request with initial priority 0 get promoted to a higher priority level.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD31_11):** Reserved.
10:0	6h RW	**Deadline Threshold (DEADLINE_THRS):** A requests with initial priority of 0 will exit priority 0 when its deadline is equal or less than this value plus current time. This field does not affect the priority of any requests in access classes with initial priority bigger than 0.

5.2.36 Major Mode Blocking Rules Control (D_CR_MM_BLK)—Offset 114Ch

This register controls blocking rules enforced in RMM and WMM.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1800h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved (RSVD31_25):** Reserved.
24	0h RW	**WMM Regular Rule 1 (WMM_REG_R1):** Disable WMM unsafe write page hits block safe write page misses same bank.
23:20	0h RO	**Reserved (RSVD23_20):** Reserved.
19	0h RW	**WMM Priority Rule 4 (WMM_PRIO_R4):** Disable WMM unsafe priority 1 read miss block write hit to same bank. Note: This rule does not block the bank that is being blocked by WMM_PRIO_R3. Priority rules 1, 3 and 4 should be enabled/disabled together.
18	0h RW	**WMM Priority Rule 3 (WMM_PRIO_R3):** Disable WMM unsafe priority 1 write hit block write miss to same bank. Note: This rule does not block the bank that is being blocked by WMM_PRIO_R1. Priority rules 1,3 and 4 should be enabled/disabled together.
17	0h RW	**WMM Priority Rule 2 (WMM_PRIO_R2):** Disable WMM CAS block rule.
16	0h RW	**WMM Priority Rule 1 (WMM_PRIO_R1):** Disable WMM unsafe top priority 1 write miss block write hit same bank. Priority rules 1, 3 and 4 should be enabled/disabled together.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13	0h RW	**RMM Regular Rule 6 (RMM_REG_R6):** Disable RMM unsafe write page hits block safe write page misses same bank.
12	1h RW	**RMM Regular Rule 5 (RMM_REG_R5):** Disable RMM unsafe read page miss block all safe and unsafe write page hit to the same bank. Note: This field must not be set to 0 (enabled) if RMM_REG_R4 is also 0.
11	1h RW	**RMM Regular Rule 4 (RMM_REG_R4):** Disable RMM unsafe write page hit block safe read page miss same bank. Note: This field must not be set to 0 (enabled) if RMM_REG_R5 is also 0.
10	0h RW	**RMM Regular Rule 3 (RMM_REG_R3):** Disable RMM unsafe read page hit block safe read and write page miss same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R3 and RMM_PRIO_R1.
9	0h RW	**RMM Regular Rule 2 (RMM_REG_R2):** Disable RMM unsafe read page empty block safe write page empty same rank.
8	0h RW	**RMM Regular Rule 1 (RMM_REG_R1):** Disable RMM unsafe read page hit block safe write page hit same rank.
7:4	0h RO	**Reserved (RSVD7_4):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**RMM Priority Rule 4 (RMM_PRIO_R4):** Disable RMM unsafe critical read miss block read and write hit to same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R3. Priority rules 1, 3 and 4 should be enabled/disabled together.
2	0h RW	**RMM Priority Rule 3 (RMM_PRIO_R3):** Disable RMM unsafe critical read hit block read and write miss to same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R1. Priority rules 1, 3 and 4 should be enabled/disabled together.
1	0h RW	**RMM Priority Rule 2 (RMM_PRIO_R2):** Disable RMM CAS block rule.
0	0h RW	**RMM Priority Rule 1 (RMM_PRIO_R1):** Disable RMM unsafe top critical read miss block read and write hit same bank. Note: Priority rules 1, 3 and 4 should be enabled/disabled together.

5.2.37 DRAM Self-Refresh Command (D_CR_DRAM_SR_CMD)—Offset 1154h

Self refresh command register to allow sending WAKE and SUSPEND messages to D-Unit. (Only one bit can be set at a time). Posted writes to this register are not completed until hardware clears the field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD31_4):** Reserved.
3	0h RW/V	**SUSPENDP (SUSPENDP):** A SUSPENDP message will put the DRAM into self-refresh mode. The D-Unit will complete servicing outstanding memory requests and flush all queued Refresh commands to DRAM before putting the DRAM in self refresh mode. Finally, a PM message will be sent to the PHY. The bit is cleared by hardware after the PHY indicates the transition requested in the PM message has been completed. D-Unit will perform an MRW to MR17 with an opcode as defined by DPMC0.PASR before it places the DRAM into Self-Refresh.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/V	**SUSPEND (SUSPEND):** A SUSPEND message will put the DRAM into self-refresh mode. The D-Unit will complete servicing outstanding memory requests and flush all queued Refresh commands to DRAM before putting the DRAM in Self Refresh mode. Finally, a PM message will be sent to the PHY. The bit is cleared by hardware only after the PHY indicates the transition requested in the PM message has been completed. Note: When COLDWAKE is set prior of setting this bit the DRAM will not be placed in SR.
1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RW/V	**WAKE (WAKE):** Take PHY out of PM states and wakes the DRAM out of self refresh mode. The bit is cleared by hardware only when the DRAM has exited out of self refresh mode and is accessible. Note: When COLDWAKE is set prior of setting this bit the D-Unit will not send SR exit command and will not set the DCO.IC bit.

5.2.38 DQS Retraining Control (D_CR_DQS_RETRAINING_CTL)—Offset 1180h

LPDDR4 DQS Retraining control register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DQS Periodic Retraining Interval (DQS_RETRAIN_INT):** This sets the frequency by which the D-Unit initiates periodic retraining (in 1x NREFI).
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:4	0h RW	**DQS Oscillator Runtime (DQS_OSC_RT):** After D-Unit starts DQS oscillator, it must wait this amount of time before being able to read the value in MR18 and MR19 (in 16x DRAM clocks). Value in this register must be at least equal to DRAM's MR23 value. + tOSCO.
3:2	0h RO	**Reserved (RSVD3_2):** Reserved.
1	0h RW	**DQS Retrain SRX Exit (DQS_RETRAIN_SRX_EN):** Enable retraining on SR exit. This bit enables LPDDR4 DQS retraining on Self Refresh Exit. If disabled, D-Unit will not perform retraining on SR exit.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**DQS Retrain Enable (DQS_RETRAIN_EN):** Periodic retraining enable: This bit enables periodic DQS retraining. If disabled, D-Unit will not perform retraining periodically. Note: Will be enabled only if DCO.IC is set and refreshes are enabled in DRF.MINREFRATE.

5.2.39 MR4 De-Swizzle Control (D_CR_MR4_DESWIZZLE)—Offset 1184h

Controls the data bits swizzling crossbar for MR4.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:28	0h RW	**MR4 Bit 2 Select 2nd Byte (MR4_BIT2_SEL2):** Selects bit 2 of MR4 data.
27	0h RO	**Reserved (RSVD27):** Reserved
26:24	0h RW	**MR4 Bit 1 Select 2nd Byte (MR4_BIT1_SEL2):** Selects bit 1 of MR4 data
23	0h RO	**Reserved (RSVD23):** Reserved
22:20	0h RW	**MR4 Bit 0 Select 2nd Byte (MR4_BIT0_SEL2):** Selects bit 0 of MR4 data.
19:18	0h RO	**Reserved (RSVD19_18):** Reserved
17:16	0h RW	**MR4 Byte 2 Select (MR4_BYTE_SEL2):** Selects byte position of the MR4 data for second device.
15	0h RO	**Reserved (RSVD15):** Reserved
14:12	0h RW	**MR4 Bit 2 Select (MR4_BIT2_SEL):** Selects bit 2 of MR4 data.
11	0h RO	**Reserved (RSVD11):** Reserved.
10:8	0h RW	**MR4 Bit 1 Select (MR4_BIT1_SEL):** Selects bit 1 of MR4 data.
7	0h RO	**Reserved (RSVD7):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**MR4 Bit 0 Select (MR4_BIT0_SEL):** Selects bit 0 of MR4 data.
3:2	0h RO	**Reserved (RSVD3_2):** Reserved.
1:0	0h RW	**MR4 Byte Select (MR4_BYTE_SEL):** Selects byte position of the MR4 data first device.

5.3 Registers Summary

Table 5-3. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1200h	1203h	DRAM Rank Population 0 (D_CR_DRP0)—Offset 1200h	10000000h
1208h	120Bh	DRAM Timing Register 0A (D_CR_DTR0A)—Offset 1208h	210702CBh
120Ch	120Fh	DRAM Timing Register 1A (D_CR_DTR1A)—Offset 120Ch	30481218h
1210h	1213h	DRAM Timing Register 2A (D_CR_DTR2A)—Offset 1210h	8C080C30h
1214h	1217h	DRAM Timing Register 3A (D_CR_DTR3A)—Offset 1214h	3002EA28h
1218h	121Bh	DRAM Timing Register 4A (D_CR_DTR4A)—Offset 1218h	30209149h
121Ch	121Fh	DRAM Timing Register 5A (D_CR_DTR5A)—Offset 121Ch	304200C2h
1220h	1223h	DRAM Timing Register 6A (D_CR_DTR6A)—Offset 1220h	20100000h
1224h	1227h	DRAM Timing Register 7A (D_CR_DTR7A)—Offset 1224h	D060C06h
1228h	122Bh	DRAM Timing Register 8A (D_CR_DTR8A)—Offset 1228h	CC50A18h
122Ch	122Fh	D-Unit ODT Control Register A (D_CR_DOCRA)—Offset 122Ch	0h
1230h	1233h	D-Unit Power Management Control 0 (D_CR_DPMC0)—Offset 1230h	0h
1234h	1237h	D-Unit Power Management Control 1 (D_CR_DPMC1)—Offset 1234h	10000028h
1238h	123Bh	DRAM Refresh Control (D_CR_DRFC)—Offset 1238h	1750h
123Ch	123Fh	D-Unit Scheduler (D_CR_DSCH)—Offset 123Ch	3901C08h
1240h	1243h	DRAM Calibration Control (D_CR_DCAL)—Offset 1240h	1057h
1244h	1247h	VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 124Ch	20000h
124Ch	124Fh	VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 124Ch	0h
1250h	1253h	Periodic DRAM Temperature Polling Control (TQ) (D_CR_TQCTL)—Offset 1250h	6C000008h
1254h	1257h	TQ Temperature Offset Control (D_CR_TQOFFSET)—Offset 1254h	0h
1258h	125Bh	D-Unit Control Operations (D_CR_DCO)—Offset 1258h	0h
12A4h	12A7h	Data Scrambler (D_CR_SCRAMCTRL)—Offset 12A4h	0h
12ACh	12AFh	Error Injection Address Register (D_CR_ERR_INJ)—Offset 12ACh	0h
12B0h	12B3h	Error Injection Control Register (D_CR_ERR_INJ_CTL)—Offset 12B0h	0h
12B4h	12B7h	Error Log Register (D_CR_ERR_ECC_LOG)—Offset 12B4h	0h
12BCh	12BFh	D-Unit Fuse Status (D_CR_DFUSESTAT)—Offset 12BCh	0h
1324h	1327h	Major Mode Control (D_CR_MMC)—Offset 1324h	2B01E518h
1328h	132Bh	Major Mode RD/WR Counter (Set A and B) (D_CR_MMRDWR_AB)—Offset 1328h	1F207C8h

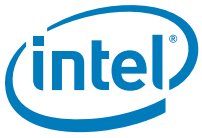


Table 5-3. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
132Ch	132Fh	Major Mode RD/WR Counter (Set C and D) (D_CR_MMRDWR_CD)—Offset 132Ch	1F207C8h
1330h	1333h	Access Class Initial Priority (D_CR_ACCIP)—Offset 1330h	17C2h
1334h	1337h	Access Class 0 Priority Promotion Control (D_CR_RD_PROM0)—Offset 1334h	1F52940h
1338h	133Bh	Access Class 1 Priority Promotion Control (D_CR_RD_PROM1)—Offset 1338h	14000000h
133Ch	133Fh	Access Class 2 Priority Promotion Control (D_CR_RD_PROM2)—Offset 133Ch	0h
1340h	1343h	Access Class 3 Priority Promotion Control (D_CR_RD_PROM3)—Offset 1340h	1F29400h
1344h	1347h	Access Class 4 Priority Promotion Control (D_CR_RD_PROM4)—Offset 1344h	1F5294Ah
1348h	134Bh	Deadline Threshold (D_CR_DL_THRS)—Offset 1348h	6h
134Ch	134Fh	Major Mode Blocking Rules Control (D_CR_MM_BLK)—Offset 134Ch	1800h
1354h	1357h	DRAM Self-Refresh Command (D_CR_DRAM_SR_CMD)—Offset 1354h	0h
1380h	1383h	DQS Retraining Control (D_CR_DQS_RETRAINING_CTL)—Offset 1380h	0h
1384h	1387h	MR4 De-Swizzle Control (D_CR_MR4_DESWIZZLE)—Offset 1384h	0h

5.3.1 DRAM Rank Population 0 (D_CR_DRP0)—Offset 1200h

Rank configuration register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**DRAM Device Per Rank (DRAMDEVICE_PR):** Specifies the number of DRAM devices that are ganged together to form a single rank. • 00: 1 DRAM device in each rank. • 01: 2 DRAM devices in each rank. • 10: 4 DRAM devices in each rank. • 11: 8 DRAM devices in each rank. Note: The actual number of devices is one more than the value programmed when ECC is enabled.
29:28	1h RW	**Address Decode (ADDRDEC):** Specifies the address mapping to be used: • 00: 1KB (A). • 01: 2KB (B). • 10: 4KB (C). • 11: Reserved.

Bit Range	Default & Access	Field Name (ID): Description
27:25	0h RW	**Burst Length Mode (BLMODE):** • 000: Fixed BL8. • 001: Onthefly BL8. • 010: Fixed BL16. • 011: Onthefly BL16. • 100: Fixed BL32. • 101: Onthefly BL32. • 110-111: Reserved.
24:22	0h RW	**DRAM Type (DRAMTYPE):** • 000: DDR3L. • 001: LPDDR3. • 010: LPDDR4. • 011: Reserved. • 100: Reserved. • 101-111: Reserved. Note: The D-Unit should only use this field if allowed by fuse.
21	0h RW	**ECC Enable (ECCEN):** • 0: ECC is disabled. • 1: ECC is enabled. This bit determines if the D-Unit treats the PMI BE_ECC bits as ECC bits or Byte Enables. The D-Unit should not allow this bit to be set if ECC is disabled by fuse. This should only be used in configurations that support ECC (DDR3L).
20:19	0h RW	**CA Swizzle Type (CASWIZZLE):** • 00: uniDIMM/SODIMM. • 01: BGA. • 10: BGA mirrored (LPDDR3 Only). • 11: UDIMM (DDR3L Only).
18:16	0h RO	**Reserved (RSVD18_16):** Reserved.
15	0h RW	**Bank Address Hashing Enable (BAHEN):** See Address Mapping section for full description. • 0: Bank Address Hashing disabled. • 1: Bank Address Hashing enabled.
14	0h RW	**Rank Select Interleave Enable (RSIEN):** See Address Mapping section for full description. • 0: Rank Select Interleaving disabled. • 1: Rank Select Interleaving enabled.
13:9	0h RO	**Reserved (RSVD13_9):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:6	0h RW	**DRAM Device Density (DDEN):** Density of the DRAM devices populated on Ranks 0 and 1. • 000: 4 Gb. • 001: 6 Gb. • 010: 8 Gb. • 011: 12 Gb. • 100: 16 Gb. • 101-111: Reserved. Note: For LPDDR4 this value is the die density.
5:4	0h RW	**DRAM Device Data Width (DWID):** Data width of the DRAM device populated on Ranks 0 and 1. • 00: x8. • 01: x16. • 10: x32. • 11: x64.
3	0h RO	**Reserved (RSVD3):** Reserved.
2	0h RW	**Dual Data Mode Enable (DDMEN):** • 0: PMI Dual Data Mode is disabled in D-Unit, full cacheline read and writes go through a single D-Unit. • 1: PMI Dual Data Mode is enabled, only half cacheline read/ writes go through a single D-Unit.
1	0h RW	**Rank Enable 1 (RKEN1):** Enable Rank 1: Must be set to 1 to enable use of this rank.
0	0h RW	**Rank Enable 0 (RKEN0):** Enable Rank 0: Must be set to 1 to enable use of this rank. Note: Setting this bit to 0 is not a functional mode.

5.3.2 DRAM Timing Register 0A (D_CR_DTR0A)—Offset 1208h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 210702CBh

Bit Range	Default & Access	Field Name (ID): Description
31:25	10h RW	**Valid Clocks Before CKE High [tCKCKEH/tCSCKEH/tCKSRX] (TCKCKEH):** Number of valid clocks before CKE high (in DRAM clocks). • LPDDR4: The value in this register covers both tCKCKEH and tCSCKEH. • DDR3L/LPDDR3/: The value covers tCKSRX which is defined as the number of valid DRAM clocks that have to toggle before the issuing of the Self Refresh Exit SRX. This value is also used if the clock frequency is changed or the clock is stopped or tristated during Power Down i.e. the number valid DRAM clocks that have to toggle before the issuing of the Power Down Exit PDX command. tCKCKEH can be used to compensate for clock stabilization delays in the motherboard. Note: D-unit hardware enforces minimum of two SPID clock before CKEH, any value in this register is the additional time.
24:21	8h RW	**Exit Self-Refresh to Valid Commands Requiring a Locked DLL Delay [tXSDLL] (TXSDLL):** D-Unit waits max(tXSR+tZQCL/ tZQCS, tXSDLL) before allowing traffic to DRAM (in 64 x DRAM Clocks). LPDDR3/LPDDR4: tXSDLL = 0. DDR3L: tXSDLL = tDLLK = 512 Clocks = 8 x 64 DRAM Clocks. Note: In the equation above, tZQCL/tZQCS = 0 if no ZQ is performed on SR exit.
20:12	70h RW	**Exit Self-Refresh to Valid Command Delay [tXS/tXSR] (TXSR):** DDR3L: tXS - Delay between Self Refresh Exit SRX to any DRAM Command not requiring DLL Lock. LPDDR/: tXSR - Delay between Self Refresh Exit SRX to any DRAM Command. (in DRAM clocks).
11:6	Bh RW	**Activate RAS to CAS Command Delay [tRCD] (TRCD):** Specifies the delay between a DRAM Activate command and a DRAM Read or Write command to the same bank (in DRAM clocks). Note: Derating adds 1.875ns to this timing.
5:0	Bh RW	**Precharge to Activate Command Delay of a Single Bank [tRPpb] (TRPPB):** Specifies the delay between a DRAM Precharge command and a DRAM Activate command to the same bank (in DRAM Clocks). Note : this CR should be constrained to a minimum of 4 in LPDDR3 and minimum of 8 in LPDDR4. Note: Derating adds 1.875ns to this timing.

5.3.3 DRAM Timing Register 1A (D_CR_DTR1A)—Offset 120Ch

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 30481218h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Exit Power Down to Next Command Delay [tXP] (TXP):** Specifies the delay from the DRAM Power Down Exit (PDX) command to any valid command (in DRAM clocks). Note: The value in this field must be programmed to tXPDLL when Slow Exit Mode Power-down is enabled for DDR3L.
26	0h RO	**Reserved (RSVD26):** Reserved.
25:14	120h RW	**ZQ (long) Calibration Time [tZQCL/tZQCAL] (TZQCL):** • LPDDR3/DDR3L: tZQCL/tZQoper: Specifies the delay between the DRAM ZQ Calibration Long (ZQCL) command and any DRAM command during normal operation. • LPDDR4: tZQCAL: ZQ Calibration time (in DRAM clocks). Note: This field defines the ZQ Calibration Long delay during normal operation. It is not the same as tZQinit which uses the same ZQCL command but the delay is longer. tZQinit applies only during poweron initialization of the DRAM devices and tZQoper applies during normal operation. BIOS executes the DRAM initialization sequence so it has to ensure tZQinit is met and not the D-Unit.
13:6	48h RW	**ZQ Short Calibration Time [tZQCS] (TZQCS):** ZQCS to any DRAM Command Delay: Specifies the delay between the DRAM ZQ Calibration Short (ZQCS) command and any DRAM command (in DRAM clocks). DDR3L and LPDDR3 only. LPDDR4 does not support ZQCS command
5:0	18h RW	**ZQ Latch Time [tZQLAT] (TZQLAT):** Specifies the delay between the DRAM ZQ Calibration Latch command and any DRAM command (in DRAM clocks). LPDDR4 only.Not used in DDR3L/LPDDR3/.

5.3.4 DRAM Timing Register 2A (D_CR_DTR2A)—Offset 1210h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8C080C30h

Bit Range	Default & Access	Field Name (ID): Description
31:23	118h RW	**All Bank Refresh Cycle Time [tRFCab] (NRFCAB):** Specifies the delay between the REFab command to the next valid command. (in DRAM clocks)
22:21	0h RO	**Reserved (RSVD22_21):** Reserved.
20:17	4h RW	**CKE Minimum Pulse Width [tCKE] (TCKE):** Specifies the minimum time from CKEL to CKEH (in DRAM clocks).

Bit Range	Default & Access	Field Name (ID): Description
16	0h RO	**Reserved (RSVD16):** Reserved.
15:0	C30h RW	**Refresh Interval Time [tREFI] (NREFI):** Specifies the average time between refresh commands. JEDEC Base Refresh Interval time (in DRAM clocks). Note: D-Unit will ignore the 2 LSBs of this field.

5.3.5 DRAM Timing Register 3A (D_CR_DTR3A)—Offset 1214h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3002EA28h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Read to Precharge Delay [tRDPRE] (TRTP):** Specifies the minimum delay between the DRAM Read and Precharge commands to the same bank (in DRAM clocks). • LPDDR3 Equation: = BL/2 + tRTP - 4. • LPDDR4 Equation: = BL/2 + Max (8, tRTP) - 8. • DDR3L Equation: = tRTP.
26:20	0h RW	**CAS to CAS Command Delay Adder (TCCD_INC):** Specifies the number of clocks to be added to turnaround times (for Stretch Mode). It increases delay between Read to Read or Read to Write commands (in 4 x DRAM clocks).
19:13	17h RW	**Write to Precharge Command Delay [tWRPRE] (TWTP):** Specifies the minimum delay between the DRAM Write command and the Precharge command to the same bank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tWTP = BL/2 + WL + tWR + 1. • DDR3L Equation: tWTP = BL/2 + CWL + tWR.
12:11	1h RW	**DRAM Command Valid Duration (TCMD):** Specifies the number of DRAM clocks a command is held valid on the DRAM Address and Control buses. 1N is the DDR3 basic requirement. 2N is the extended mode for board signal integrity. • 0h: Reserved. • 1h: 1 DRAM Clock (1N). • 2h: 2 DRAM Clocks (2N). • 3h: Reserved. Note: DDR3L only. tCMD must be set to 1N for LPDDR3/LPDDR4.
10:6	8h RW	**Write Latency [WL/CWL] (TCWL):** The delay between the internal write command and the availability of the first word of DRAM input data (in DRAM clocks).

Bit Range	Default & Access	Field Name (ID): Description
5:0	28h RW	**Write CAS to Masked Write CAS Delay Same Bank (TWMWSB):** Specifies the minimum delay between DRAM Write command to Masked Write command to same bank (in DRAM clocks). • LPDDR4 Equation: tWMWSB = tCCDMW (BL16) or tCCDMW + 8 (BL32). Note: Masked Write operation in LPDDR4 is always BL16. D-Unit applies this timing for same rank as well as same bank.

5.3.6 DRAM Timing Register 4A (D_CR_DTR4A)—Offset 1218h

Specifies DRAM timings parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 30209149h

Bit Range	Default & Access	Field Name (ID): Description
31:24	30h RW	**Four Bank Activate Window [tFAW] (TFAW):** A rolling timeframe in which a maximum of four Activate commands can be issued to the same rank. This is to limit the peak current draw from the DRAM devices (in DRAM clocks).
23:18	8h RW	**Write to Read DQ Delay Different Ranks (TWRDR):** Specifies the delay from the start of a Write data burst of one rank to the start of a Read data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tWRDR = WL + tDQSSmax + BL/2 + tWPST - (RL + tDQSCKmin - tRPRE). • LPDDR4 Equation: tWRDR = WL - RL + BL/2 + 4 - tDQSCKmin. • DDR3L Equation: tWRDR = CWL + tDQSSmax + BL/2 + tWPST - (CL + tDQSCKmin - tRPRE). Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj.
17:12	9h RW	**Read to Write DQ Delay Different Ranks (TRWDR):** Specifies the delay from the start of a Read data burst of one rank to the Start of a Write data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tRWDR = RL + tDQSCKmax + BL/2 + tRPST - (WL + tDQSSmin - tWPRE). • LPDDR4 Equation: tRWDR = RL + tDQSCKmax + BL/2 - (WL - 2). • DDR3L Equation: tRWDR = CL + tDQSCKmax + BL/2 + tRPST - (CWL + tDQSSmin - tWPRE). Note: For LPDDR3/4 using ODT, this latency may need to be adjusted by tODTon. Note: For DDR3L using ODT, this latency may need to be increased by one clock.

Bit Range	Default & Access	Field Name (ID): Description
11:6	5h RW	**Write to Write DQ Delay Different Ranks (TWWDR):** Specifies the delay from the start of a Write data burst of one rank to the start of a Write data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tWWDR = BL/2 + tDQSSmax - tDQSSmin + tWPRE. • LPDDR4 Equation: tWWDR = BL/2 + 4 - tDQSSmin. • DDR3L Equation: tWWDR = BL/2 + tDQSSmax - tDQSSmin + tWPRE. Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj.
5:0	9h RW	**Read to Read DQ Delay Different Ranks (TRRDR):** Specifies the delay from the start of a Read data burst of one rank to the Start of a Read data burst of a different rank (in DRAM clocks). • LPDDR3/4 Equation: tRRDR = BL/2 + tDQSCKmax - tDQSCKmin + tRPRE. • DDR3L Equation: tRRDR = BL/2 + tRPST + tDQSCKmax - tDQSCKmin + tRPRE + 1.

5.3.7 DRAM Timing Register 5A (D_CR_DTR5A)—Offset 121Ch

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 304200C2h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Row Activation to Row Activation Delay [tRRD] (TRRD):** Specifies the minimum delay in DRAM clocks between two DRAM Activate commands to the same rank but different banks (tRC is the minimum delay between activations of the same bank). Note: Derating adds 1.875ns to this timing.
26	0h RO	**Reserved (RSVD26):** Reserved.
25:23	0h RW	**Derate Increment (TDERATE_INC):** Specifies the additional delay that is added to DRAM timing when indicated by MR4 status. (in DRAM clocks) LPDDR3/LPDDR4: Value is 1.875ns. Note: The value in this register is only added to these timing parameters: tRCD, tRAS, tRP and tRRD.
22:18	10h RW	**Write to Write DQ Delay Same Rank (TWWSR):** Specifies the delay from a DRAM Write to another Write command of the same rank (in DRAM clocks). LPDDR3/LPDDR4/DDR3L Equation: tRRSR = tCCD.

Bit Range	Default & Access	Field Name (ID): Description
17:13	10h RW	**Read to Read DQ Delay Same Rank (TRRSR):** Specifies the delay from a DRAM Read to another Read command of the same rank (in DRAM clocks). LPDDR3/LPDDR4/DDR3L Equation: tRRSR = tCCD.
12:6	3h RW	**Write to Read DQ Delay Same Rank (TWRSR):** Specifies the delay from a DRAM Read to Write command of the same rank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tWRSR = WL + tDQSSmax + BL/2 + tWTR. • DDR3L Equation: tWRSR = CWL + tDQSSmax + BL/2 + tWPST + tWTR.
5:0	2h RW	**Read to Write DQ Delay Same Rank (TRWSR):** Specifies the delay from a DRAM Read to a Write command of the same rank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tRWSR = RL + tDQSCKmax + BL/2 - WL + tWPRE. • DDR3L Equation: tRWSR = CL + tDQSCKmax + BL/2 + tRPST - (CWL +tDQSSmin - tWPRE). Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj. Note: For DDR3L using ODT, this latency may need to be increased by one clock.

5.3.8 DRAM Timing Register 6A (D_CR_DTR6A)—Offset 1220h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 20100000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	20h RW	**Opportunistic Refresh Idle Timer (OREFDLY):** Rank idle period that defines an opportunity for refresh (in DRAM clocks).
23:19	2h RW	**Valid Clocks After CKE Low [tCKELCK/tCKELCS/tCPDED/tCKSRE] (TCKCKEL):** Specifies the amount of time that DRAM clocks need to toggle after CKE goes low (in DRAM Clocks). • For LPDDR3, this covers tCPDED. • For LPDDR4, this covers both tCKELCK and tCKELCS. • For DDR3L, this is tCKSRE. Note: D-Unit hardware enforces minimum of one SPID clocks after CKEL, any value in this register is the additional time.
18:15	0h RW	**Maintenance Operation Delay (MNTDLY):** When a critical read request is pending in RPQ and a maintenance operation (MRR, ZQCal, Ref, etc, panic refresh is an exception to this delay.) needs to be performed, D-Unit waits this amount of time before performing the maintenance operation to allow for some high priority requests to be issued (in 4x SPID clocks).

Bit Range	Default & Access	Field Name (ID): Description
14:8	0h RW	**Mode Register Read to Any Command Delay (TPSTMRRBLK):** Specifies the quiet time after issuing MRR command (in DRAM Clocks). Note: D-Unit treats MRR as a read and always applies relevant turnaround times, any value programmed in this CR must be greater than those turnaround times for D-Unit to enforce any additional time from MRR to the next read/write.
7	0h RO	**Reserved (RSVD7):** Reserved.
6:0	0h RW	**Any Command to Mode Register Read/Write Delay (TPREMRBLK):** Specifies the quiet time before issuing MRR/MRW command. (in DRAM clocks). Note: D-Unit treats MRR as a read and always applies relevant turnaround times, any value programmed in this CR must be greater than those turnaround times for D-Unit to enforce any additional time from previous read/writes.

5.3.9 DRAM Timing Register 7A (D_CR_DTR7A)—Offset 1224h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: D060C06h

Bit Range	Default & Access	Field Name (ID): Description
31:26	3h RW	**All Bank Precharge to Activate Command Delay [tRPab] (TRPAB):** Specifies the delay between a DRAM Precharge All Bank command and a DRAM Activate command (in DRAM Clocks). Note: This CR should be constrained to a minimum of 4 in LP3 and minimum of 8 in LP4. Note: Derating adds 1.875ns to this timing. • For LPDDR, tRPpb = tRP, tRPab = tRP + 3ns. • For DDR3L 8ch tRPpb = tRPab = tRP.
25:23	2h RW	**Mode Register Write to any Command Delay [tMRD/tMRW] (TPSTMRWBLK):** Specifies the quiet time after issuing MRW command (in 8 x DRAM clocks). Note: This time covers for both tMRD and tMRW.
22:16	6h RW	**Write Command to Power Down Delay [tWRPDEN] (TWRPDEN):** Specifies the minimum time between a write command to PowerDown command (in DRAM clocks). Must be at least equal to tWR + tCCD + tWL + 2.
15:9	6h RW	**Read Command to Power Down Delay [tRDPDEN] (TRDPDEN):** Specifies the minimum time between a read command to PowerDown command (in DRAM clocks). Must be at least equal to CL/RL + tDQSCKmax + tCCD + tRPST.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RO	**Reserved (RSVD8_7):** Reserved.
6:0	6h RW	**Row Activation Period [tRAS] (TRAS):** Specifies the minimum delay between the DRAM Activate and Precharge commands to the same bank (in DRAM clocks). Note: Derating adds 1.875ns to this timing.

5.3.10 DRAM Timing Register 8A (D_CR_DTR8A)—Offset 1228h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: CC50A18h

Bit Range	Default & Access	Field Name (ID): Description
31:26	3h RW	**Minimum Self-Refresh Time [tSR/tCKESR] (TCKESR):** Specifies the minimum time that DRAM should remain in SR (in DRAM clocks).
25:21	6h RW	**Minimum Low Power Mode Residency (LPMDRES):** Specifies the minimum time that PHY should remain in LPMode (in DRAM clocks).
20:15	Ah RW	**Low Power Mode Exit to Clock Enable Delay (LPMDTOCKEDLY):** Specifies the minimum time between the LP Mode exit to the CK stop/tristate deassertion and powerdown exit (in DRAM clocks). Note: Must be equal to t_idle_latency and less than 0x3C.
14:8	Ah RW	**Clock Stop to Low Power Mode Delay (CKETOLPMDDLY):** Specifies the time between CK stop/tristate to the Low Power Mode entry. This timing parameter is used to delay Low Power Mode entry (in DRAM clocks). Note: Must be at least equal to t_idle_length parameter and less than 0x7C.
7:0	18h RW	**Power Down Idle Timer (PWDDLY):** This is a non-JEDEC timing parameter used to delay powerdown entry (in DRAM clocks).

5.3.11 D-Unit ODT Control Register A (D_CR_DOCRA)—Offset 122Ch

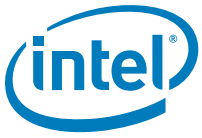
Specifies the parameters to control DRAM ODT.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29	0h RW	**Rank 1 Read ODT Control (R1RDODTCTL):** Specifies the behavior of ODT signals when a Read command is issued to Rank 1. 0 - Read ODT is disabled for Rank 1 1 - Assert ODT to for Rank 0 (non-targeted Rank) Note: This register should be set to 0 for LPDDR3 devices
28	0h RW	**Rank 0 Read ODT Control (R0RDODTCTL):** Specifies the behavior of ODT signals when a Read command is issued to Rank 0. 0 - Read ODT is disabled for Rank 0 1 - Assert ODT to for Rank 1 (non-targeted Rank) Note: This register is reserved for LPDDR3 devices
27:26	0h RW	**Rank 1 Write ODT Control (R1WRODTCTL):** Specifies the behavior of ODT signals when a Write command is issued to Rank 1. 00 - Write ODT is disabled 01 - Assert ODT to Rank 0 (non-targeted Rank) 10 - Assert ODT to Rank 1 (targeted Rank) 11 - Assert ODT to Rank 0 and Rank 1 Note: 10 and 11 are reserved values for LPDDR3
25:24	0h RW	**Rank 0 Write ODT Control (R0WRODTCTL):** Specifies the behavior of ODT signals when a Write command is issued to Rank 0. 00 - Write ODT is disabled 01 - Assert ODT to Rank 0 (targeted Rank) 10 - Assert ODT to Rank 1 (non-targeted Rank) 11 - Assert ODT to Rank 0 and Rank 1 Note: 10 and 11 are reserved values for LPDDR3
23:18	0h RO	**Reserved (RSVD23_18):** Reserved.
17:14	0h RW	**Read ODT assertion to de-assertion delay (DDR3L Only) (RDODTSTOP):** Specifies Read ODT assertion to ODT de-assert delay (in DRAM clocks). DDR3L Equation: RDODTSTOP = DOCRx.WRODTSTOP (subtract 1 if DOCRx.WRODTSTART = 1 in 2N mode).
13	0h RO	**Reserved (RSVD13):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
12:9	0h RW	**Read command to ODT assertion delay (DDR3L Only) (RDODTSTART):** Specifies Read ODT assertion delay after Read Command (in DRAM clocks). DDR3L Equation: RDODTSTART = CL CWL (add 1 if DOCRx.WRODTSTART = 0 in 2N mode). The max value for this CR is 0xE
8:5	0h RW	**Write ODT Assertion to De-assertion Delay (WRODTSTOP):** Specifies number of clocks after ODT assertion that D-Unit deasserts ODT signal (in DRAM clocks). LPDDR3 Equation: WRODTSTOP = RU(tODTon(max)/tCK) + RU((tDQSSmax+tWPST)/tCK) + BL/2 - RD(tODToffmin/tCK) DDR3L Equation: WRODTSTOP >= 6
4	0h RO	**Reserved (RSVD4):** Reserved.
3:0	0h RW	**Write command to ODT assertion delay (WRODTSTART):** Specifies number of clocks after Write command that D-Unit asserts ODT signal (in DRAM clocks). LPDDR3 Equation: WRODTSTART = WL - RU(tODTon(max)/tCK) DDR3L Equation: WRODTSTART = 0 Note: DDR3 spec requires ODT to be asserted high when the DRAM Write command is issued. In DDR3L 2N mode the value can be set to 0 to assert ODT one DRAM clock earlier than the Write Command (WR) or set to 1 to assert at the same clock as command (CS assertion). The max value for this CR is 0xE

5.3.12 D-Unit Power Management Control 0 (D_CR_DPMC0)—Offset 1230h

Specifies the parameters to control D-Unit power management features.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD31_29):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28:24	0h RW	**SUSPEND/SUSPENDP Power Management Message Opcode (SUSPMOP):** DDRIO PHY Power Mode Opcode: After the D-Unit has placed the DRAM devices in Self Refresh/PASR mode as the result of a SUSPEND/SUSPENDP message, it sends this 5-bit value to the DDRIO PHY to tell it which power saving mode it should enter. Changing this register value while in SUSPEND will have no effect. Note: This opcode cannot be a PM state where it disables PHY PLLs i.e PM7 in LPDDR PHY.
23	0h RO	**Reserved (RSVD23):** Reserved.
22	0h RW	**PM Message Wait for Clock Gate Enable (SRPMCLKW):** Specifies when it is safe to send PM message to the PHY. When enabled, D-Unit waits for SPID Clock to deassert before sending a PM message on SR entry. • 0: D-Unit will not wait for SPID_clk to deassert before sending the PM message to PHY. • 1: D-Unit will wait for SPID_clk to deassert before sending PM message to the PHY. Note: The value must be 1 when DYNPMOP = 7h.
21:17	0h RW	**Dynamic Self-Refresh Power Management Message Opcode (DYNPMOP):** DDRIO PHY Power Mode Opcode: After the D-Unit has placed the DRAM devices in Self Refresh mode as the result of a Dynamic Self-Refresh, it sends this 5bit value to the DDRIO PHY to tell it which power saving mode it should enter. Changing this register value while in self-refresh will only change the PM state for the next entry in DynSR.
16	0h RW	**Dynamic Self-Refresh Enable (DYNSREN):** When set to 1, the D-Unit will automatically control DRAM Self Refresh entry and exit based on interface state and requests in pending queues. When there is no pending request in the queues and PMI is idle, then the D-Unit will place the DRAM devices in Self Refresh mode. The DRAM devices will be brought out of Self-Refresh when idle conditions don't hold.
15:0	0h RW	**Self-Refresh Entry Delay (SREDLY):** Specifies the minimum time the D-Unit will wait before it enters Dynamic Self-Refresh mode when idle (in 16x DRAM Clocks). Note: The value in this field needs to be minimum of 4 in functional mode and minimum of 50 in PSMI mode.

5.3.13 D-Unit Power Management Control 1 (D_CR_DPMC1)—Offset 1234h

Specifies the parameters to control D-Unit power management features.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10000028h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29	0h RW	**D-Unit Repeaters Clock Gate Disable (RPTCLKGTDIS):** Setting this bit to 0 allows majority of the repeaters between D-Unit and PHY to clock gate when there is no activity in order to save power. 0 - Enable Repeaters clock gating, 1 - Disable Repeaters clock gating. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.
28	1h RW	**IOSF-SB End Point Clock Gate Disable (SBEPCLKGTDIS):** Setting this bit to 0 enables the clock gating of IOSF-SB End Points in D-Unit and CPGC when there is no IOSF-SB activity in order to save power. 0 - Enable IOSF-SB EP clock gating, 1 - Disable IOSF-SB clock gating. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.
27	0h RW	**Local Clock Gate Disable (CLKGTDIS):** Setting this bit to 0 allows the majority of the D-Unit clocks to be gated off when there is no activity in order to save power. When set to 1, D-Unit clockgating is disabled. • 0: Enable. • 1: Disable. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.
26	0h RW	**Chip Select Tristate Enable (CSTRIST):** • 0: The DRAM CS pins associated with the enabled ranks are never tristated. • 1: The DRAM CS pins are tristated when DRAM clock is stopped or tristated. Note: CS is not tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1).
25:24	0h RW	**Command/Address Tristate (CMDTRIST):** • 00: The DRAM CA pins are never tristated. • 01: The DRAM CA pins are only tristated when all enabled CKE pins are low. • 10: The DRAM CA pins are tristated when not driving a valid command. • 11: Reserved
23:16	0h RW	**Partial Array Self-Refresh Segment Mask (PASR):** This is the Segment Mask used for the MRW to enable PASR during SUSPENDP (Partial Array Self Refresh entry).

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Page Close Timeout Period (PCLSTO):** Specifies the time from the last access of a DRAM page until that page is scheduled to close by sending a Precharge command to DRAM (in 16 x DRAM clocks).
7	0h RW	**Page Close Timeout Disable (PCLSTODIS):** When disabled, D-Unit will not close the DRAM page when idle. • 0: Enable page close timer. • 1: Disable page close timer (Used during DRAM init and DDRIO training).
6	0h RO	**Reserved (RSVD6):** Reserved.
5	1h RW	**ODT Tristate Enable (ODTTRIST):** • 0: The DRAM ODT pins associated with the enabled ranks are never tristated. • 1: DRAMs ODT pins are tristated when DRAM clock is stopped or tristated. Note: ODT is not tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1)
4:3	1h RW	**Clock Stop/Tristate Enable (ENCKSTP):** Enable/Disable CK Stop/Tristate During Power down. • 00: Disable CK Stop/Tristate During Power down. • 01: Enable CK Stop During Power down. • 10: Enable CK Tristate During Power down. • 11: Reserved Note: CK is not stopped or tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1).
2:1	0h RW	**Low Power Mode Opcode (LPMODEOP):** D-Unit will send the value in this register after it has entered Powerdown Mode and has stopped/tristated the clock. 00: Disable LPMode. Note: LPMODE entry is not possible when global tristate flow is disabled (DCBR.TRISTDIS = 1).
0	0h RW	**Disable Power Down (DISPWRDN):** Setting this bit to 1 disables dynamic control of DRAM Power-Down entry and exit by keeping the CKE pins driven high. BIOS may set it to 1 during DRAM initialization and DDRIO training. This bit should be set to 0 for normal operation. • 0: The D-Unit dynamically controls the CKE pins to place the DRAM devices in Power Down mode and bring them out of Power Down mode. • 1: The D-Unit constantly drives the CKE pins high to keep the DRAM devices from entering Power Down mode when ranks are idle. Note: This bit is overridden if CKEMODE = 1. This bit does not control CKE behavior on SR entry/exit.

5.3.14 DRAM Refresh Control (D_CR_DRFC)—Offset 1238h

Specifies the parameters to control scheduling of refresh commands.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1750h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD31_22):** Reserved.
21	0h RW	**Disable Refresh Debt Clear (DISREFDBTCLR):** When set, D-Unit will not clear refresh debt before Self Refresh SR Entry: • 0: D-Unit sends all postponed REF commands to DRAM before it enters Self Refresh. • 1: D-Unit enters SR without clearing the Refresh Debt (for Debug only).
20	0h RW	**Refresh Skew Disable (REFSKWDIS):** Disables Skewing of Refresh Counting between Ranks. Each rank has its own refresh counter. By default incrementing these refresh counters are skewed by 1/2 the tREFI period. Setting this bit to a 1 disables this feature and all refresh counters will increment at the same time per tREFI period. Skewing the tREFI counters can improve performance since traffic to all ranks does not have to be blocked to perform refresh. • 0: Incrementing the refresh counters are skewed by 1/2 tREFI period. • 1: All refresh counters will increment at the same time per tREFI period.
19:18	0h RO	**Reserved (RSVD19_18):** Reserved.
17:16	0h RO	**Reserved (RSVD17_16):** Reserved.
15	0h RW	**Extra Refresh Debit (EXTRAREFDBT):** When set to 1, D-Unit adds one extra refresh debit (for a total of two) on Self-refresh exit.
14:12	1h RW	**Minimum Refresh Rate (MINREFRATE):** Ensures that refresh rate never drops below a certain limit regardless of TQ polling. • 000: Disable tREFI counter and stop issuing refresh commands. • 001: 0.25x refresh rate (i.e. 4x tREFI same as no limit). • 010: 0.5x refresh rate (i.e. 2x tREFI). • 011: 1x refresh rate (i.e. 1x tREFI). • 100: 2x refresh rate (i.e. 0.5x tREFI). • 101: 4x refresh rate (i.e. 0.25x tREFI). • 110: 4x refresh rate with derating forced on i.e. 0.25x tREFI. • 111: Reserved.
11:8	7h RW	**Refresh Panic Watermark (REFWMPNC):** When the Refresh counter per rank is greater than this value, the D-Unit will send a REF command to the rank regardless of pending requests. Note: REFWMPNC must be greater than or equal to REFWMHI and greater than 2, Max Value must be less than 8 to not violate 9xtREFI JEDEC requirement.

Bit Range	Default & Access	Field Name (ID): Description
7:4	5h RW	**Refresh High Watermark (REFWMHI):** When the Refresh counter per rank is greater than this value, the D-Unit will send a REF command to the rank if there is no critical priority requests in the pending queues. Note: Value must be greater or equal to 1 and less than or equal to REFWMPNC.
3:1	0h RO	**Reserved (RSVD3_1):** Reserved.
0	0h RW	**Opportunistic Refresh Disable (OREFDIS):** Disable opportunistic scheduling of refresh. • 0: D-Unit will send a REF command only if there is no pending request to that rank. • 1: D-Unit will not send any opportunistic refreshes. Refresh commands are only sent when the refresh counter is greater than REFWMHI. Note: When set, DISREFDBTCLR must also be set to be able to enter SR.

5.3.15 D-Unit Scheduler (D_CR_DSCH)—Offset 123Ch

Specifies parameters to control scheduling of commands to DRAM.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3901C08h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:29	0h RW	**BGF Early Read Data Valid (BGF_EARLY_RDDATA_VALID):** Specifies the number of clocks the D-Unit sends the read data valid through the BGF earlier as compared to the data. • 00: Always write read valid in same SPID clock as data. • 01: Always write read valid one SPID clock before data. • 10: Write read valid up to 2 SPID clocks before data. • 11: Reserved
28:27	0h RW	**SPID Early Read Data Valid (SPID_EARLY_RDDATA_VALID):** Specifies the delay in SPID clocks from RDDATA_VALID assertion to actual data on SPID. The value should match what is programmed in DDRIO (PHY).
26:21	1Ch RW	**Write Pending Queue Count (WPQCOUNT):** Used to limit the number of available slots in Write Pending Queue/ Write Data Buffer. WPQCOUNT will only recognize changes when PMI ISM is not active.

Bit Range	Default & Access	Field Name (ID): Description
20:16	10h RW	**Read Pending Queue Count (RPQCOUNT):** Used to limit the number of entries in Read Pending Queue. RPQCOUNT will only recognize changes when PMI ISM is not active.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:10	7h RW	**Read Return Data Additional Credits (BLKRDBF_ADD_RDDATA_CR):** Number of additional full cacheline (64B) read data return credits exposed to D-Unit when BLKRDBF is set. Note: The value in this field has no effect on Read return credits when BLKRDBF is not set.
9:8	0h RW	**In-Order Mode (INORDERMODE):** • 0h: In order mode disabled: Commands are sent out of order. • 1h: Partial in order mode: Read and Write CAS commands are sent in the order they were recieved. ACT and PRE can go out of order. • 2h: Full in order mode serialized test: All DRAM commands CAS ACT PRE associated with a PMI request are issued to DDR before any DRAM commands for a subsequent PMI request. • 3h: Reserved. In order modes should be enabled during init/training/CPGC testing. Should never be changed while the D-Unit queues are nonempty.
7	0h RW	**Idle Bypass Mode Enable (BYPASSEN):** Reserved.
6	0h RW	**Block When RDB Full (BLKRDBF):** When set D-Unit stops scheduling new read commands to DRAM when the read data buffer (RDB) is full.
5:4	0h RW	**Stretch Mode (STRETCHMODE):** When stretch mode is enabled, commands are initiated only on Phase 0 of SPIDClk. • 00: Stretch mode is disabled. • 01: Commands are initiated on Phase 0 of every SPID clocks. • 10: Commands are initiated on Phase 0 of even SPID clocks. • 11: Commands are initiated on Phase 0 of odd SPID clocks.
3:0	8h RW	**Masked Write Turnaround Delta (TMWR_TA_DELTA):** The value in this register is subtracted from Masked Write to Read, Masked Write to Write and Masked Write to Masked Write turnaround times to account for half BL MWr commands in LPDDR4. • LPDDR4: = MWr tCCD = MWr BL/2 = 8.

5.3.16 DRAM Calibration Control (D_CR_DCAL)—Offset 1240h

Specifies parameters to control ZQ Calibration.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1057h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ZQ Calibration Type (ZQCALTYPE):** Determines whether the ZQ Calibration is a long or short calibration command (due to ZQCALSTRT). 0: Short calibration (ZQCS). 1: Long calibration (ZQCL).
30	0h RW/V	**ZQ Calibration Start Rank 1 (ZQCALSTRTR1):** Set this bit to 1 to start the ZQ calibration sequence on Rank 1. This bit will remain a 1 until the ZQ calibration is complete for rank 1, then it will return to 0. 0: ZQ calibration is done. 1: ZQ calibration has started and is in progress.
29	0h RW/V	**ZQ Calibration Start Rank 0 (ZQCALSTRTR0):** Set this bit to 1 to start the ZQ calibration sequence on Rank 0. This bit will remain a 1 until the ZQ calibration is complete for rank 0, then it will return to 0. 0: ZQ calibration is done. 1: ZQ calibration has started and is in progress.
28:23	0h RO	**Reserved (RSVD28_23):** Reserved.
22:21	0h RW	**Self-Refresh Exit ZQ Calibration Control (SRXZQC):** • 00: On DynSR exit ZQ timer determines the ZQ type. When the state is lost (i.e due to AutoPG/S0ix) ZQCL is always performed. • 01: Always perform ZQCL after self refresh exit, in LPDDR4, ZQ with traffic blocked. • 10: Always perform ZQCS on SR exit. For LPDDR4, ZQ while traffic is allowed. • 11: No ZQCL commands are sent (it disables ZQCAL commands on SR exit).
20:18	0h RO	**Reserved (RSVD20_18):** Reserved.
17	0h RW	**ZQ Calibration Mode (ZQCLMODE):** Specifies how ZQCal commands are sent to different ranks. • 0: ZQCal commands are sent in parallel to all ranks. • 1: ZQCal commands are sent serially to each rank.
16	0h RW	**Periodic ZQ Calibration Disable (ZQCDIS):** • 0: Periodic ZQ Calibration is Enabled. • 1: Disable periodic ZQ Calibration.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:0	1057h RW	**ZQ Calibration Interval (ZQINT):** Specifies the time interval between two ZQCS (LPDDR3) or ZQ Start (LPDDR4) commands to a DRAM device. (in RTC 32.8KHz clocks)

5.3.17 VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 124Ch

Specifies parameters for VNN Scaling Timer in D-Unit. The values in this register will be set by P-code during VNN scaling period.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VNN Scaling Timer Enable (VNN_TIMER_EN):** • 0: The D-Unit VNN Scaling Timer is disabled. • 1: The D-Unit VNN Scaling Timer is enabled.
30:12	0h RO	**Reserved (RSVD30_12):** Reserved.
11:0	0h RW	**VNN Timer Time (VNN_TIMER_TIME):** The final timer value (in 16 x DRAM clocks).

5.3.18 Periodic DRAM Temperature Polling Control (TQ) (D_CR_TQCTL)—Offset 1250h

Specifies the control for periodic temperature monitoring and control of DRAM device.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6C000008h

Bit Range	Default & Access	Field Name (ID): Description
31:29	3h RW/V	**TQ Data Rank 1 (TQDATAR1):** If Rank 1 is disabled, this value will remain zero. This field contains the data of the last DRAM Mode Register Read to MR4 MRR issued. It is overwritten with each command.
28:26	3h RW/V	**TQ Data Rank 0 (TQDATAR0):** This field contains the data of the last DRAM Mode Register Read to MR4 MRR issued. It is overwritten with each command.
25:22	0h RO	**Reserved (RSVD25_22):** Reserved.
21:8	0h RW	**TQ Poll Period (TQPOLLPER):** This sets the frequency by which the D-Unit polls the DRAM mode register MR4 to determine required refresh rate (in 4x tREFI units).

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved (RSVD7_5):** Reserved.
4	0h RW	**Self Refresh Temperature Range Enable (DDR3 Only) (SRTEN):** When set, before every Self refresh entry, D-Unit writes a 1 to bit 7 of TQOFFSET.MR_VALUE when TQDATA for that rank indicates a value higher then 0x3, and writes a 0 to that bit otherwise. The new MR_VALUE is then written into MR2 of DDR3 for each enabled rank.
3	1h RW	**Enable Dynamic Timing Derating (ENDERATE):** When set to 1, the Dynamic Timing Derating is enabled. When the D-Unit determines (via TQ polling) that the DRAM requires timing derating in addition to refresh interval adjustment, the D-Unit will automatically adjust the relevant timing parameters.
2	0h RW	**Enable TQ Data Push (TQDATAPUSHEN):** When set to 1, D-Unit pushes the data form the last MR4 read to a punit register.
1	0h RW	**Enable TQ Poll on Self-Refresh Exit (TQPOLLSREN):** This bit enables MR4 read on Self Refresh Exit. If disabled, D-Unit will not read MR4 value on Self-Refresh exit.
0	0h RW	**Enable Periodic TQ Poll (TQPOLLEN):** This bit enables periodic TQ Poll. If disabled, D-Unit will not read MR4 value periodically. Note: Will be enabled only if refreshes are enabled.

5.3.19 TQ Temperature Offset Control (D_CR_TQOFFSET)—Offset 1254h

Specifies temperature offset and refresh rate adjustments requested by software.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:16	0h RW	**MR Value (MR_VALUE):** MR2 Shadow Register (DDR3L Only): BIOS writes the correct value of MR2 register in DDR3L into this field at boot time. D-Unit modifies one bit and rewrites the MR2 into DDR3L DRAM before SR entry.
15:11	0h RO	**Reserved (RSVD15_11):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**MR4 Adder (MR4_ADDER):** D-Unit adds the value of this field to TQDATA read from MR4 the resulting value is used to control refresh rate and AC timing derating.
7:3	0h RO	**Reserved (RSVD7_3):** Reserved.
2	0h RW/V	**MR3 Offset Update (MR3_OFFSET_UPDATE):** When set, D-Unit writes the merged value of MR3_VALUE and MR3_THERM_OFFSET into MR3 of DRAM. D-Unit clears this bit once the value is written.
1:0	0h RW	**MR3 Thermal Offset (MR3_THERM_OFFSET):** Reserved

5.3.20 D-Unit Control Operations (D_CR_DCO)—Offset 1258h

Specifies D-Unit initialization and control operation.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Initialization Complete (IC):** Indicates that initialization of the D-Unit has been completed. Memory accesses are permitted and maintenance operation begins. Until this bit is set to a 1, the memory controller will not accept DRAM requests from the Bunit/ GSA/2LM (PMI ISMs will not leave idle). Note: Set this bit to 1 only when all other D-Unit registers have been configured. Usually set at the last configuration step by BIOS on cold/warm reset. D-Unit hardware sets this bit on SR exit.
30	0h RO/V	**DDRIO PHY Initialization Complete (DIOIC):** Status indication that the DDRIO PHY initialization is complete reflects the status spid_init_complete signal.
29	0h RO	**Reserved (RSVD29):** Reserved.
28	0h RW	**PMI Control Select (PMICTL):** • 0: D-Unit PMI is connected to Bunit/GSA/2LM. • 1: D-Unit PMI is connected to CPGC. Note: D_CR_DSCH_BYPASSEN must be set to 0 in CPGC mode. Note: PMI must be idle and D-Unit BGF_RUN = 0 before changing the value in this register.
27:8	0h RO	**Reserved (RSVD27_8):** Reserved.
7:4	0h RO	**Reserved (RSVD7_4):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Enable PSMI Mode (PSMIEN):** When enabled, D-Unit will synchronize clock crossing signals. • 0: PSMI Mode is disabled. • 1: PSMI Mode is enabled. Note: Change only allowed when D-Unit is idle.
2	0h RW	**Maintenance Reset (MNTRST):** Writing a 1 to this field resets all maintenance timers. Clears all states and also clears refresh debt queues. This bit needs to be cleared by software after at least 3 SPID clocks.
1	0h RW	**Enable Maintenance Operations (MNTEN):** Setting this field to 1 enables all maintenance operations. When DCO.IC is set, the maintenance operations are enabled irrespective of the value of this field.
0	0h RO	**Reserved (RSVD0):** Reserved.

5.3.21 Data Scrambler (D_CR_SCRAMCTRL)—Offset 12A4h

Specifies parameters to control data scrambling in D-Unit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Data Scrambler (SCRM_EN):** When set to 1, data scrambling is enabled. When set to 0, data scrambling is disabled. Should be set before D_CR_BGF_CTL_BGF_RUN is set to 1.
30	0h RO	**Reserved (RSVD30):** Reserved.
29:28	0h RW	**Scrambler Clock Gate Select (CLOCKGATE):** This field controls how the scrambler output code is clock gated to reduce power. • 00: Clock gate disabled. • 01: Clock Gate every 2 cycle. • 10: Clock Gate every 3 cycle. • 11: Clock Gate every 4 cycle.
27:16	0h RO	**Reserved (RSVD27_16):** Reserved.
15:0	0h RW	**Scrambling Key (KEY):** Sets the key for the scrambler. The key should be a random value that is set following each cold boot.

5.3.22 Error Injection Address Register (D_CR_ERR_INJ)—Offset 12ACh

Contains the target address for ECC error injection.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:1	0h RW	**Error Injection Target Address (ADDRESS):** Specifies the PMI address of the write transaction to be injected with the error. Only applicable to Write transactions. Read/under-fill read of the partial write operation is not affected.
0	0h RO	**Reserved (RSVD0):** Reserved.

5.3.23 Error Injection Control Register (D_CR_ERR_INJ_CTL)—Offset 12B0h

Controls injecting correctable or uncorrectable errors into the write requests specified by target address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD31_4):** Reserved
3	0h RW	**Error Injection Type Higher 32B (SEL_HI):** If enabled, the error injection is continuously armed for ERR_INJ.ADDR 32B write address matching until it is cleared. • 00: No error injection. • 01: Uncorrectable Error (UE) is armed for write address matching to inject UE by using the same poisoning scheme, i.e. inverting corresponding write ECC[6:0] on QW0 of the 32B data. • 10: Correctable Error (CE) is armed for write address matching to inject CE by inverting corresponding write ECC[0] on QW0 of the 32B data. • 11: Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Error Injection Enable Higher 32B (EN_HI):** When set the error injection is continuously armed for higher 32B of D_CR_ERR_INJ_ADDR write address matching until it is cleared.
1	0h RW	**Error Injection Type Lower 32B (SEL_LO):** 0 - Uncorrectable Error (UE) is armed for write address matching to inject UE by using the same poisoning scheme, i.e. inverting corresponding write ECC[6:0] on every QW of the 32B data. 1 - Correctable Error (CE) is armed for write address matching to inject CE by inverting corresponding write ECC[0] on every QW of the 32B data.
0	0h RW	**Error Injection Enable Lower 32B (EN_LO):** When set, the error injection is continuously armed for lower 32B of D_CR_ERR_INJ_ADDR write address matching until it is cleared.

5.3.24 Error Log Register (D_CR_ERR_ECC_LOG)—Offset 12B4h

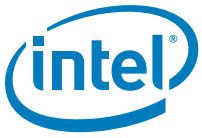
Detected ECC errors are captured in this register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Clear (CLEAR):** Setting this bit to one clears all fields in this register, including itself.
30:29	0h RW	**PMI VISA Byte Select (ECC_VISA):** Select ECC or PMI byte on VISA : • 00: ECC byte, • 01: PMI Data Byte [7:0], • 10: PMI Data Byte [63:56], • 11: PMI Data Byte [255:248]
28	0h RW/V	**Correctable Single-bit Error (CERR):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. A multiple bit error that occurs after this bit is set will override the address/error syndrome information.
27	0h RW/V	**Uncorrectable Multiple-bit Error (MERR):** This bit is set when an uncorrectable multiple-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked until this bit is cleared.



Bit Range	Default & Access	Field Name (ID): Description
26:25	0h RW/V	**Error Burst Number (ERR_BURST):** Burst number (in BL8) of the error within a chunk.
24	0h RW/V	**Error Chunk Number (ERR_CHUNK):** Chunk number of the error. 0 - lower 32B chunk has error if MERR/CERR is set 1 - higher 32B chunk has the error if MERR/CERR is set
23:16	0h RW/V	**Quad Word ECC Syndrome (SYNDROME_QW):** ECC Syndrome for a QW (64 bit) within 32B Address
15:0	0h RW/V	**Request Tag (TAG):** Read Return Tag matches with the PMI Request Tag which triggered the error log.

5.3.25 D-Unit Fuse Status (D_CR_DFUSESTAT)—Offset 12BCh

Contains the values read from D-Unit fuses.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD31_16):** Reserved.
15:0	0h RO/V	**D-Unit Fuse Status (FUSESTAT):** D-Unit fuse bits are captured into this register and are available to be read. • [0]: fus_dun_ecc_dis. • [3:1]: fus_dun_max_supported_device_size[2:0]. • [4:4]: fus_dun_lpddr3_dis. • [5:5]: fus_dun_lpddr4_dis. • [6:6]: reserved. • [7:7]: fus_dun_ddr3l_dis. • [15:8]: reserved.

5.3.26 Major Mode Control (D_CR_MMC)—Offset 1324h

Specifies parameters to control read/write major mode operation and transitions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2B01E518h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:27	5h RW	**RAW Conflict Read Priority for WMM Transition (RAW_WMM):** If a conflict read reaches this priority (or greater depending on access class occupancy), WMM will be triggered to unblock the corresponding write. D-Unit will stay in WMM until corresponding write is issued. Note: The value in this bit must not be higher than lowest terminal priority level of each access class.
26	0h RO	**Reserved (RSVD26):** Reserved.
25:23	6h RW	**Read Isoch Trigger Priority (RIMPRIO):** If any read in the RPQ is at this programmable priority, RIM is triggered.
22:18	0h RO	**Reserved (RSVD22_18):** Reserved.
17:12	1Eh RW	**Write Isoch Threshold (WIMTHRS):** When the number of entries in WPQ is greater than or equal to this value (higher than WMM entry watermark, less than WPQ size), it triggers write isoch mode (WIM).
11:6	14h RW	**Write Major Mode Exit Watermark (WMMEXIT):** When the number of entries in WPQ is less than this value, the D-Unit will switch back to read major mode.
5:0	18h RW	**Write Major Mode Entry Watermark (WMMENTRY):** When the number of entries in WPQ is greater than or equal to this value, the D-Unit will switch to write major mode (WMM). Note: the value must not be set to 0.

5.3.27 Major Mode RD/WR Counter (Set A and B) (D_CR_MMRDWR_AB)—Offset 1328h

Minimum read and maximum write counter control. This register defines the minimum number of reads in RMM and maximum number of writes in WMM before a mode transition happens.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F207C8h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:20	1Fh RW	**Max Writes B (MAXWRB):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set B).

Bit Range	Default & Access	Field Name (ID): Description
19:14	8h RW	**Min Reads B (MINRDB):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set B).
13:12	0h RO	**Reserved (RSVD13_12):** Reserved.
11:6	1Fh RW	**Max Writes A (MAXWRA):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set A).
5:0	8h RW	**Min Reads A (MINRDA):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set A).

5.3.28 Major Mode RD/WR Counter (Set C and D) (D_CR_MMRDWR_CD)—Offset 132Ch

Minimum read and maximum write counter control. This register defines the minimum number of reads in RMM and maximum number of writes in WMM before a mode transition happens (sets C and D).

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F207C8h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:20	1Fh RW	**Max Writes D (MAXWRD):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set D).
19:14	8h RW	**Min Reads D (MINRDD):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set D).
13:12	0h RO	**Reserved (RSVD13_12):** Reserved.
11:6	1Fh RW	**Max Writes C (MAXWRC):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set C).
5:0	8h RW	**Min Reads C (MINRDC):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set C).

5.3.29 Access Class Initial Priority (D_CR_ACCIP)—Offset 1330h

Each field of this register defines the initial priority of one access class.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 17C2h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved (RSVD31_15):** Reserved.
14:12	1h RW	**Access Class 4 Initial Priority (AC4IP):** Initial priority level of read requests coming with access class 4.
11:9	3h RW	**Access Class 3 Initial Priority (AC3IP):** Initial priority level of read requests coming with access class 3.
8:6	7h RW	**Access Class 2 Initial Priority (AC2IP):** Initial priority level of read requests coming with access class 2.
5:3	0h RW	**Access Class 1 Initial Priority (AC1IP):** Initial priority level of read requests coming with access class 1.
2:0	2h RW	**Access Class 0 Initial Priority (AC0IP):** Initial priority level of read requests coming with access class 0.

5.3.30 Access Class 0 Priority Promotion Control (D_CR_RD_PROM0)—Offset 1334h

This register defines the priority promotion policy for access class 0. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F52940h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	Ah RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	Ah RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	Ah RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.3.31 Access Class 1 Priority Promotion Control (D_CR_RD_PROM1)—Offset 1338h

This register defines the priority promotion policy for access class 1. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the associated level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 14000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	Ah RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	0h RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	0h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	0h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.3.32 Access Class 2 Priority Promotion Control (D_CR_RD_PROM2)—Offset 133Ch

This register defines the priority promotion policy for access class 2. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	0h RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	0h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	0h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.3.33 Access Class 3 Priority Promotion Control (D_CR_RD_PROM3)—Offset 1340h

This register defines the aging policy for access class 3. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F29400h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	5h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	5h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

Bit Range	Default & Access	Field Name (ID): Description
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.3.34 Access Class 4 Priority Promotion Control (D_CR_RD_PROM4)—Offset 1344h

This register defines the aging policy for access class 3. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F5294Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	Ah RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	Ah RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	Ah RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	Ah RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.3.35 Deadline Threshold (D_CR_DL_THRS)—Offset 1348h

Specifies when the request with initial priority 0 get promoted to a higher priority level.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD31_11):** Reserved.
10:0	6h RW	**Deadline Threshold (DEADLINE_THRS):** A requests with initial priority of 0 will exit priority 0 when its deadline is equal or less than this value plus current time. This field does not affect the priority of any requests in access classes with initial priority bigger than 0.

5.3.36 Major Mode Blocking Rules Control (D_CR_MM_BLK)—Offset 134Ch

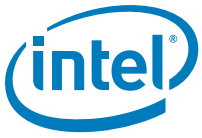
This register controls blocking rules enforced in RMM and WMM.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1800h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved (RSVD31_25):** Reserved.
24	0h RW	**WMM Regular Rule 1 (WMM_REG_R1):** Disable WMM unsafe write page hits block safe write page misses same bank.
23:20	0h RO	**Reserved (RSVD23_20):** Reserved.
19	0h RW	**WMM Priority Rule 4 (WMM_PRIO_R4):** Disable WMM unsafe priority 1 read miss block write hit to same bank. Note: This rule does not block the bank that is being blocked by WMM_PRIO_R3. Priority rules 1, 3 and 4 should be enabled/disabled together.
18	0h RW	**WMM Priority Rule 3 (WMM_PRIO_R3):** Disable WMM unsafe priority 1 write hit block write miss to same bank. Note: This rule does not block the bank that is being blocked by WMM_PRIO_R1. Priority rules 1,3 and 4 should be enabled/disabled together.
17	0h RW	**WMM Priority Rule 2 (WMM_PRIO_R2):** Disable WMM CAS block rule.
16	0h RW	**WMM Priority Rule 1 (WMM_PRIO_R1):** Disable WMM unsafe top priority 1 write miss block write hit same bank. Priority rules 1, 3 and 4 should be enabled/disabled together.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13	0h RW	**RMM Regular Rule 6 (RMM_REG_R6):** Disable RMM unsafe write page hits block safe write page misses same bank.



Bit Range	Default & Access	Field Name (ID): Description
12	1h RW	**RMM Regular Rule 5 (RMM_REG_R5):** Disable RMM unsafe read page miss block all safe and unsafe write page hit to the same bank. Note: This field must not be set to 0 (enabled) if RMM_REG_R4 is also 0.
11	1h RW	**RMM Regular Rule 4 (RMM_REG_R4):** Disable RMM unsafe write page hit block safe read page miss same bank. Note: This field must not be set to 0 (enabled) if RMM_REG_R5 is also 0.
10	0h RW	**RMM Regular Rule 3 (RMM_REG_R3):** Disable RMM unsafe read page hit block safe read and write page miss same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R3 and RMM_PRIO_R1.
9	0h RW	**RMM Regular Rule 2 (RMM_REG_R2):** Disable RMM unsafe read page empty block safe write page empty same rank.
8	0h RW	**RMM Regular Rule 1 (RMM_REG_R1):** Disable RMM unsafe read page hit block safe write page hit same rank.
7:4	0h RO	**Reserved (RSVD7_4):** Reserved.
3	0h RW	**RMM Priority Rule 4 (RMM_PRIO_R4):** Disable RMM unsafe critical read miss block read and write hit to same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R3. Priority rules 1, 3 and 4 should be enabled/disabled together.
2	0h RW	**RMM Priority Rule 3 (RMM_PRIO_R3):** Disable RMM unsafe critical read hit block read and write miss to same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R1. Priority rules 1, 3 and 4 should be enabled/disabled together.
1	0h RW	**RMM Priority Rule 2 (RMM_PRIO_R2):** Disable RMM CAS block rule.
0	0h RW	**RMM Priority Rule 1 (RMM_PRIO_R1):** Disable RMM unsafe top critical read miss block read and write hit same bank. Note: Priority rules 1, 3 and 4 should be enabled/disabled together.

5.3.37 DRAM Self-Refresh Command (D_CR_DRAM_SR_CMD)—Offset 1354h

Self refresh command register to allow sending WAKE and SUSPEND messages to D-Unit. (Only one bit can be set at a time). Posted writes to this register are not completed until hardware clears the field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD31_4):** Reserved.
3	0h RW/V	**SUSPENDP (SUSPENDP):** A SUSPENDP message will put the DRAM into self-refresh mode. The D-Unit will complete servicing outstanding memory requests and flush all queued Refresh commands to DRAM before putting the DRAM in self refresh mode. Finally, a PM message will be sent to the PHY. The bit is cleared by hardware after the PHY indicates the transition requested in the PM message has been completed. D-Unit will perform an MRW to MR17 with an opcode as defined by DPMC0.PASR before it places the DRAM into Self-Refresh.
2	0h RW/V	**SUSPEND (SUSPEND):** A SUSPEND message will put the DRAM into self-refresh mode. The D-Unit will complete servicing outstanding memory requests and flush all queued Refresh commands to DRAM before putting the DRAM in Self Refresh mode. Finally, a PM message will be sent to the PHY. The bit is cleared by hardware only after the PHY indicates the transition requested in the PM message has been completed. Note: When COLDWAKE is set prior of setting this bit the DRAM will not be placed in SR.
1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RW/V	**WAKE (WAKE):** Take PHY out of PM states and wakes the DRAM out of self refresh mode. The bit is cleared by hardware only when the DRAM has exited out of self refresh mode and is accessible. Note: When COLDWAKE is set prior of setting this bit the D-Unit will not send SR exit command and will not set the DCO.IC bit.

5.3.38 DQS Retraining Control (D_CR_DQS_RETRAINING_CTL)—Offset 1380h

LPDDR4 DQS Retraining control register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DQS Periodic Retraining Interval (DQS_RETRAIN_INT):** This sets the frequency by which the D-Unit initiates periodic retraining (in 1x NREFI).

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:4	0h RW	**DQS Oscillator Runtime (DQS_OSC_RT):** After D-Unit starts DQS oscillator, it must wait this amount of time before being able to read the value in MR18 and MR19 (in 16x DRAM clocks). Value in this register must be at least equal to DRAM's MR23 value. + tOSCO.
3:2	0h RO	**Reserved (RSVD3_2):** Reserved.
1	0h RW	**DQS Retrain SRX Exit (DQS_RETRAIN_SRX_EN):** Enable retraining on SR exit. This bit enables LPDDR4 DQS retraining on Self Refresh Exit. If disabled, D-Unit will not perform retraining on SR exit.
0	0h RW	**DQS Retrain Enable (DQS_RETRAIN_EN):** Periodic retraining enable: This bit enables periodic DQS retraining. If disabled, D-Unit will not perform retraining periodically. Note: Will be enabled only if DCO.IC is set and refreshes are enabled in DRF.MINREFRATE.

5.3.39 MR4 De-Swizzle Control (D_CR_MR4_DESWIZZLE)—Offset 1384h

Controls the data bits swizzling crossbar for MR4.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:28	0h RW	**MR4 Bit 2 Select 2nd Byte (MR4_BIT2_SEL2):** Selects bit 2 of MR4 data.
27	0h RO	**Reserved (RSVD27):** Reserved
26:24	0h RW	**MR4 Bit 1 Select 2nd Byte (MR4_BIT1_SEL2):** Selects bit 1 of MR4 data
23	0h RO	**Reserved (RSVD23):** Reserved
22:20	0h RW	**MR4 Bit 0 Select 2nd Byte (MR4_BIT0_SEL2):** Selects bit 0 of MR4 data.

Bit Range	Default & Access	Field Name (ID): Description
19:18	0h RO	**Reserved (RSVD19_18):** Reserved
17:16	0h RW	**MR4 Byte 2 Select (MR4_BYTE_SEL2):** Selects byte position of the MR4 data for second device.
15	0h RO	**Reserved (RSVD15):** Reserved
14:12	0h RW	**MR4 Bit 2 Select (MR4_BIT2_SEL):** Selects bit 2 of MR4 data.
11	0h RO	**Reserved (RSVD11):** Reserved.
10:8	0h RW	**MR4 Bit 1 Select (MR4_BIT1_SEL):** Selects bit 1 of MR4 data.
7	0h RO	**Reserved (RSVD7):** Reserved.
6:4	0h RW	**MR4 Bit 0 Select (MR4_BIT0_SEL):** Selects bit 0 of MR4 data.
3:2	0h RO	**Reserved (RSVD3_2):** Reserved.
1:0	0h RW	**MR4 Byte Select (MR4_BYTE_SEL):** Selects byte position of the MR4 data first device.

5.4 Registers Summary

Table 5-4. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1400h	1403h	DRAM Rank Population 0 (D_CR_DRP0)—Offset 1400h	10000000h
1408h	140Bh	DRAM Timing Register 0A (D_CR_DTR0A)—Offset 1408h	210702CBh
140Ch	140Fh	DRAM Timing Register 1A (D_CR_DTR1A)—Offset 140Ch	30481218h
1410h	1413h	DRAM Timing Register 2A (D_CR_DTR2A)—Offset 1410h	8C080C30h
1414h	1417h	DRAM Timing Register 3A (D_CR_DTR3A)—Offset 1414h	3002EA28h
1418h	141Bh	DRAM Timing Register 4A (D_CR_DTR4A)—Offset 1418h	30209149h
141Ch	141Fh	DRAM Timing Register 5A (D_CR_DTR5A)—Offset 141Ch	304200C2h
1420h	1423h	DRAM Timing Register 6A (D_CR_DTR6A)—Offset 1420h	20100000h
1424h	1427h	DRAM Timing Register 7A (D_CR_DTR7A)—Offset 1424h	D060C06h
1428h	142Bh	DRAM Timing Register 8A (D_CR_DTR8A)—Offset 1428h	CC50A18h
142Ch	142Fh	D-Unit ODT Control Register A (D_CR_DOCRA)—Offset 142Ch	0h
1430h	1433h	D-Unit Power Management Control 0 (D_CR_DPMC0)—Offset 1430h	0h
1434h	1437h	D-Unit Power Management Control 1 (D_CR_DPMC1)—Offset 1434h	10000028h
1438h	143Bh	DRAM Refresh Control (D_CR_DRFC)—Offset 1438h	1750h
143Ch	143Fh	D-Unit Scheduler (D_CR_DSCH)—Offset 143Ch	3901C08h
1440h	1443h	DRAM Calibration Control (D_CR_DCAL)—Offset 1440h	1057h
1444h	1447h	VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 144Ch	20000h

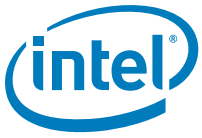


Table 5-4. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
144Ch	144Fh	VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 144Ch	0h
1450h	1453h	Periodic DRAM Temperature Polling Control (TQ) (D_CR_TQCTL)—Offset 1450h	6C000008h
1454h	1457h	TQ Temperature Offset Control (D_CR_TQOFFSET)—Offset 1454h	0h
1458h	145Bh	D-Unit Control Operations (D_CR_DCO)—Offset 1458h	0h
14A4h	14A7h	Data Scrambler (D_CR_SCRAMCTRL)—Offset 14A4h	0h
14ACh	14AFh	Error Injection Address Register (D_CR_ERR_INJ)—Offset 14ACh	0h
14B0h	14B3h	Error Injection Control Register (D_CR_ERR_INJ_CTL)—Offset 14B0h	0h
14B4h	14B7h	Error Log Register (D_CR_ERR_ECC_LOG)—Offset 14B4h	0h
14BCh	14BFh	D-Unit Fuse Status (D_CR_DFUSESTAT)—Offset 14BCh	0h
1524h	1527h	Major Mode Control (D_CR_MMC)—Offset 1524h	2B01E518h
1528h	152Bh	Major Mode RD/WR Counter (Set A and B) (D_CR_MMRDWR_AB)—Offset 1528h	1F207C8h
152Ch	152Fh	Major Mode RD/WR Counter (Set C and D) (D_CR_MMRDWR_CD)—Offset 152Ch	1F207C8h
1530h	1533h	Access Class Initial Priority (D_CR_ACCIP)—Offset 1530h	17C2h
1534h	1537h	Access Class 0 Priority Promotion Control (D_CR_RD_PROM0)—Offset 1534h	1F52940h
1538h	153Bh	Access Class 1 Priority Promotion Control (D_CR_RD_PROM1)—Offset 1538h	14000000h
153Ch	153Fh	Access Class 2 Priority Promotion Control (D_CR_RD_PROM2)—Offset 153Ch	0h
1540h	1543h	Access Class 3 Priority Promotion Control (D_CR_RD_PROM3)—Offset 1540h	1F29400h
1544h	1547h	Access Class 4 Priority Promotion Control (D_CR_RD_PROM4)—Offset 1544h	1F5294Ah
1548h	154Bh	Deadline Threshold (D_CR_DL_THRS)—Offset 1548h	6h
154Ch	154Fh	Major Mode Blocking Rules Control (D_CR_MM_BLK)—Offset 154Ch	1800h
1554h	1557h	DRAM Self-Refresh Command (D_CR_DRAM_SR_CMD)—Offset 1554h	0h
1580h	1583h	DQS Retraining Control (D_CR_DQS_RETRAINING_CTL)—Offset 1580h	0h
1584h	1587h	MR4 De-Swizzle Control (D_CR_MR4_DESWIZZLE)—Offset 1584h	0h

5.4.1 DRAM Rank Population 0 (D_CR_DRP0)—Offset 1400h

Rank configuration register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**DRAM Device Per Rank (DRAMDEVICE_PR):** Specifies the number of DRAM devices that are ganged together to form a single rank. • 00: 1 DRAM device in each rank. • 01: 2 DRAM devices in each rank. • 10: 4 DRAM devices in each rank. • 11: 8 DRAM devices in each rank. Note: The actual number of devices is one more than the value programmed when ECC is enabled.
29:28	1h RW	**Address Decode (ADDRDEC):** Specifies the address mapping to be used: • 00: 1KB (A). • 01: 2KB (B). • 10: 4KB (C). • 11: Reserved.
27:25	0h RW	**Burst Length Mode (BLMODE):** • 000: Fixed BL8. • 001: Onthefly BL8. • 010: Fixed BL16. • 011: Onthefly BL16. • 100: Fixed BL32. • 101: Onthefly BL32. • 110-111: Reserved.
24:22	0h RW	**DRAM Type (DRAMTYPE):** • 000: DDR3L. • 001: LPDDR3. • 010: LPDDR4. • 011: Reserved. • 100: Reserved. • 101-111: Reserved. Note: The D-Unit should only use this field if allowed by fuse.
21	0h RW	**ECC Enable (ECCEN):** • 0: ECC is disabled. • 1: ECC is enabled. This bit determines if the D-Unit treats the PMI BE_ECC bits as ECC bits or Byte Enables. The D-Unit should not allow this bit to be set if ECC is disabled by fuse. This should only be used in configurations that support ECC (DDR3L).
20:19	0h RW	**CA Swizzle Type (CASWIZZLE):** • 00: uniDIMM/SODIMM. • 01: BGA. • 10: BGA mirrored (LPDDR3 Only). • 11: UDIMM (DDR3L Only).
18:16	0h RO	**Reserved (RSVD18_16):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Bank Address Hashing Enable (BAHEN):** See Address Mapping section for full description. • 0: Bank Address Hashing disabled. • 1: Bank Address Hashing enabled.
14	0h RW	**Rank Select Interleave Enable (RSIEN):** See Address Mapping section for full description. • 0: Rank Select Interleaving disabled. • 1: Rank Select Interleaving enabled.
13:9	0h RO	**Reserved (RSVD13_9):** Reserved.
8:6	0h RW	**DRAM Device Density (DDEN):** Density of the DRAM devices populated on Ranks 0 and 1. • 000: 4 Gb. • 001: 6 Gb. • 010: 8 Gb. • 011: 12 Gb. • 100: 16 Gb. • 101-111: Reserved. Note: For LPDDR4 this value is the die density.
5:4	0h RW	**DRAM Device Data Width (DWID):** Data width of the DRAM device populated on Ranks 0 and 1. • 00: x8. • 01: x16. • 10: x32. • 11: x64.
3	0h RO	**Reserved (RSVD3):** Reserved.
2	0h RW	**Dual Data Mode Enable (DDMEN):** • 0: PMI Dual Data Mode is disabled in D-Unit, full cacheline read and writes go through a single D-Unit. • 1: PMI Dual Data Mode is enabled, only half cacheline read/ writes go through a single D-Unit.
1	0h RW	**Rank Enable 1 (RKEN1):** Enable Rank 1: Must be set to 1 to enable use of this rank.
0	0h RW	**Rank Enable 0 (RKEN0):** Enable Rank 0: Must be set to 1 to enable use of this rank. Note: Setting this bit to 0 is not a functional mode.

5.4.2 DRAM Timing Register 0A (D_CR_DTR0A)—Offset 1408h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 210702CBh

Bit Range	Default & Access	Field Name (ID): Description
31:25	10h RW	**Valid Clocks Before CKE High [tCKCKEH/tCSCKEH/tCKSRX] (TCKCKEH):** Number of valid clocks before CKE high (in DRAM clocks). • LPDDR4: The value in this register covers both tCKCKEH and tCSCKEH. • DDR3L/LPDDR3: The value covers tCKSRX which is defined as the number of valid DRAM clocks that have to toggle before the issuing of the Self Refresh Exit SRX. This value is also used if the clock frequency is changed or the clock is stopped or tristated during Power Down i.e. the number valid DRAM clocks that have to toggle before the issuing of the Power Down Exit PDX command. tCKCKEH can be used to compensate for clock stabilization delays in the motherboard. Note: D-unit hardware enforces minimum of two SPID clock before CKEH, any value in this register is the additional time.
24:21	8h RW	**Exit Self-Refresh to Valid Commands Requiring a Locked DLL Delay [tXSDLL] (TXSDLL):** D-Unit waits max(tXSR+tZQCL/tZQCS, tXSDLL) before allowing traffic to DRAM (in 64 x DRAM Clocks). LPDDR3/LPDDR4: tXSDLL = 0. DDR3L: tXSDLL = tDLLK = 512 Clocks = 8 x 64 DRAM Clocks. Note: In the equation above, tZQCL/tZQCS = 0 if no ZQ is performed on SR exit.
20:12	70h RW	**Exit Self-Refresh to Valid Command Delay [tXS/tXSR] (TXSR):** DDR3L: tXS - Delay between Self Refresh Exit SRX to any DRAM Command not requiring DLL Lock. LPDDR/: tXSR - Delay between Self Refresh Exit SRX to any DRAM Command. (in DRAM clocks).
11:6	Bh RW	**Activate RAS to CAS Command Delay [tRCD] (TRCD):** Specifies the delay between a DRAM Activate command and a DRAM Read or Write command to the same bank (in DRAM clocks). Note: Derating adds 1.875ns to this timing.
5:0	Bh RW	**Precharge to Activate Command Delay of a Single Bank [tRPpb] (TRPPB):** Specifies the delay between a DRAM Precharge command and a DRAM Activate command to the same bank (in DRAM Clocks). Note : this CR should be constrained to a minimum of 4 in LPDDR3 and minimum of 8 in LPDDR4. Note: Derating adds 1.875ns to this timing.

5.4.3 DRAM Timing Register 1A (D_CR_DTR1A)—Offset 140Ch

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 30481218h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Exit Power Down to Next Command Delay [tXP] (TXP):** Specifies the delay from the DRAM Power Down Exit (PDX) command to any valid command (in DRAM clocks). Note: The value in this field must be programmed to tXPDLL when Slow Exit Mode Power-down is enabled for DDR3L.
26	0h RO	**Reserved (RSVD26):** Reserved.
25:14	120h RW	**ZQ (long) Calibration Time [tZQCL/tZQCAL] (TZQCL):** • LPDDR3/DDR3L: tZQCL/tZQoper: Specifies the delay between the DRAM ZQ Calibration Long (ZQCL) command and any DRAM command during normal operation. • LPDDR4: tZQCAL: ZQ Calibration time (in DRAM clocks). Note: This field defines the ZQ Calibration Long delay during normal operation. It is not the same as tZQinit which uses the same ZQCL command but the delay is longer. tZQinit applies only during poweron initialization of the DRAM devices and tZQoper applies during normal operation. BIOS executes the DRAM initialization sequence so it has to ensure tZQinit is met and not the D-Unit.
13:6	48h RW	**ZQ Short Calibration Time [tZQCS] (TZQCS):** ZQCS to any DRAM Command Delay: Specifies the delay between the DRAM ZQ Calibration Short (ZQCS) command and any DRAM command (in DRAM clocks). DDR3L and LPDDR3 only. LPDDR4 does not support ZQCS command
5:0	18h RW	**ZQ Latch Time [tZQLAT] (TZQLAT):** Specifies the delay between the DRAM ZQ Calibration Latch command and any DRAM command (in DRAM clocks). LPDDR4 only.Not used in DDR3L/LPDDR3.

5.4.4 DRAM Timing Register 2A (D_CR_DTR2A)—Offset 1410h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8C080C30h

Bit Range	Default & Access	Field Name (ID): Description
31:23	118h RW	**All Bank Refresh Cycle Time [tRFCab] (NRFCAB):** Specifies the delay between the REFab command to the next valid command. (in DRAM clocks)

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD22_21):** Reserved.
20:17	4h RW	**CKE Minimum Pulse Width [tCKE] (TCKE):** Specifies the minimum time from CKEL to CKEH (in DRAM clocks).
16	0h RO	**Reserved (RSVD16):** Reserved.
15:0	C30h RW	**Refresh Interval Time [tREFI] (NREFI):** Specifies the average time between refresh commands. JEDEC Base Refresh Interval time (in DRAM clocks). Note: D-Unit will ignore the 2 LSBs of this field.

5.4.5 DRAM Timing Register 3A (D_CR_DTR3A)—Offset 1414h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3002EA28h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Read to Precharge Delay [tRDPRE] (TRTP):** Specifies the minimum delay between the DRAM Read and Precharge commands to the same bank (in DRAM clocks). • LPDDR3 Equation: = BL/2 + tRTP - 4. • LPDDR4 Equation: = BL/2 + Max (8, tRTP) - 8. • DDR3L Equation: = tRTP.
26:20	0h RW	**CAS to CAS Command Delay Adder (TCCD_INC):** Specifies the number of clocks to be added to turnaround times (for Stretch Mode). It increases delay between Read to Read or Read to Write commands (in 4 x DRAM clocks).
19:13	17h RW	**Write to Precharge Command Delay [tWRPRE] (TWTP):** Specifies the minimum delay between the DRAM Write command and the Precharge command to the same bank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tWTP = BL/2 + WL + tWR + 1. • DDR3L Equation: tWTP = BL/2 + CWL + tWR.
12:11	1h RW	**DRAM Command Valid Duration (TCMD):** Specifies the number of DRAM clocks a command is held valid on the DRAM Address and Control buses. 1N is the DDR3 basic requirement. 2N is the extended mode for board signal integrity. • 0h: Reserved. • 1h: 1 DRAM Clock (1N). • 2h: 2 DRAM Clocks (2N). • 3h: Reserved. Note: DDR3L only. tCMD must be set to 1N for LPDDR3/LPDDR4.

Bit Range	Default & Access	Field Name (ID): Description
10:6	8h RW	**Write Latency [WL/CWL] (TCWL):** The delay between the internal write command and the availability of the first word of DRAM input data (in DRAM clocks).
5:0	28h RW	**Write CAS to Masked Write CAS Delay Same Bank (TWMWSB):** Specifies the minimum delay between DRAM Write command to Masked Write command to same bank (in DRAM clocks). • LPDDR4 Equation: tWMWSB = tCCDMW (BL16) or tCCDMW + 8 (BL32). Note: Masked Write operation in LPDDR4 is always BL16. D-Unit applies this timing for same rank as well as same bank.

5.4.6 DRAM Timing Register 4A (D_CR_DTR4A)—Offset 1418h

Specifies DRAM timings parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 30209149h

Bit Range	Default & Access	Field Name (ID): Description
31:24	30h RW	**Four Bank Activate Window [tFAW] (TFAW):** A rolling timeframe in which a maximum of four Activate commands can be issued to the same rank. This is to limit the peak current draw from the DRAM devices (in DRAM clocks).
23:18	8h RW	**Write to Read DQ Delay Different Ranks (TWRDR):** Specifies the delay from the start of a Write data burst of one rank to the start of a Read data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tWRDR = WL + tDQSSmax + BL/2 + tWPST - (RL + tDQSCKmin - tRPRE). • LPDDR4 Equation: tWRDR = WL - RL + BL/2 + 4 - tDQSCKmin. • DDR3L Equation: tWRDR = CWL + tDQSSmax + BL/2 + tWPST - (CL + tDQSCKmin - tRPRE). Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj.
17:12	9h RW	**Read to Write DQ Delay Different Ranks (TRWDR):** Specifies the delay from the start of a Read data burst of one rank to the Start of a Write data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tRWDR = RL + tDQSCKmax + BL/2 + tRPST - (WL + tDQSSmin - tWPRE). • LPDDR4 Equation: tRWDR = RL + tDQSCKmax + BL/2 - (WL - 2). • DDR3L Equation: tRWDR = CL + tDQSCKmax + BL/2 + tRPST - (CWL + tDQSSmin - tWPRE). Note: For LPDDR3/4 using ODT, this latency may need to be adjusted by tODTon. Note: For DDR3L using ODT, this latency may need to be increased by one clock.

Bit Range	Default & Access	Field Name (ID): Description
11:6	5h RW	**Write to Write DQ Delay Different Ranks (TWWDR):** Specifies the delay from the start of a Write data burst of one rank to the start of a Write data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tWWDR = BL/2 + tDQSSmax - tDQSSmin + tWPRE. • LPDDR4 Equation: tWWDR = BL/2 + 4 - tDQSSmin. • DDR3L Equation: tWWDR = BL/2 + tDQSSmax - tDQSSmin + tWPRE. Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj.
5:0	9h RW	**Read to Read DQ Delay Different Ranks (TRRDR):** Specifies the delay from the start of a Read data burst of one rank to the Start of a Read data burst of a different rank (in DRAM clocks). • LPDDR3/4 Equation: tRRDR = BL/2 + tDQSCKmax - tDQSCKmin + tRPRE. • DDR3L Equation: tRRDR = BL/2 + tRPST + tDQSCKmax - tDQSCKmin + tRPRE + 1.

5.4.7 DRAM Timing Register 5A (D_CR_DTR5A)—Offset 141Ch

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 304200C2h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Row Activation to Row Activation Delay [tRRD] (TRRD):** Specifies the minimum delay in DRAM clocks between two DRAM Activate commands to the same rank but different banks (tRC is the minimum delay between activations of the same bank). Note: Derating adds 1.875ns to this timing.
26	0h RO	**Reserved (RSVD26):** Reserved.
25:23	0h RW	**Derate Increment (TDERATE_INC):** Specifies the additional delay that is added to DRAM timing when indicated by MR4 status. (in DRAM clocks) LPDDR3/LPDDR4: Value is 1.875ns. Note: The value in this register is only added to these timing parameters: tRCD, tRAS, tRP and tRRD.
22:18	10h RW	**Write to Write DQ Delay Same Rank (TWWSR):** Specifies the delay from a DRAM Write to another Write command of the same rank (in DRAM clocks). LPDDR3/LPDDR4/DDR3L Equation: tRRSR = tCCD.

Bit Range	Default & Access	Field Name (ID): Description
17:13	10h RW	**Read to Read DQ Delay Same Rank (TRRSR):** Specifies the delay from a DRAM Read to another Read command of the same rank (in DRAM clocks). LPDDR3/LPDDR4/DDR3L Equation: tRRSR = tCCD.
12:6	3h RW	**Write to Read DQ Delay Same Rank (TWRSR):** Specifies the delay from a DRAM Read to Write command of the same rank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tWRSR = WL + tDQSSmax + BL/2 + tWTR. • DDR3L Equation: tWRSR = CWL + tDQSSmax + BL/2 + tWPST + tWTR.
5:0	2h RW	**Read to Write DQ Delay Same Rank (TRWSR):** Specifies the delay from a DRAM Read to a Write command of the same rank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tRWSR = RL + tDQSCKmax + BL/2 - WL + tWPRE. • DDR3L Equation: tRWSR = CL + tDQSCKmax + BL/2 + tRPST - (CWL +tDQSSmin - tWPRE). Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj. Note: For DDR3L using ODT, this latency may need to be increased by one clock.

5.4.8 DRAM Timing Register 6A (D_CR_DTR6A)—Offset 1420h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 20100000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	20h RW	**Opportunistic Refresh Idle Timer (OREFDLY):** Rank idle period that defines an opportunity for refresh (in DRAM clocks).
23:19	2h RW	**Valid Clocks After CKE Low [tCKELCK/tCKELCS/tCPDED/tCKSRE] (TCKCKEL):** Specifies the amount of time that DRAM clocks need to toggle after CKE goes low (in DRAM Clocks). • For LPDDR3, this covers tCPDED. • For LPDDR4, this covers both tCKELCK and tCKELCS. • For DDR3L, this is tCKSRE. Note: D-Unit hardware enforces minimum of one SPID clocks after CKEL, any value in this register is the additional time.
18:15	0h RW	**Maintenance Operation Delay (MNTDLY):** When a critical read request is pending in RPQ and a maintenance operation (MRR, ZQCal, Ref, etc, panic refresh is an exception to this delay.) needs to be performed, D-Unit waits this amount of time before performing the maintenance operation to allow for some high priority requests to be issued (in 4x SPID clocks).

Bit Range	Default & Access	Field Name (ID): Description
14:8	0h RW	**Mode Register Read to Any Command Delay (TPSTMRRBLK):** Specifies the quiet time after issuing MRR command (in DRAM Clocks). Note: D-Unit treats MRR as a read and always applies relevant turnaround times, any value programmed in this CR must be greater than those turnaround times for D-Unit to enforce any additional time from MRR to the next read/write.
7	0h RO	**Reserved (RSVD7):** Reserved.
6:0	0h RW	**Any Command to Mode Register Read/Write Delay (TPREMRBLK):** Specifies the quiet time before issuing MRR/MRW command. (in DRAM clocks). Note: D-Unit treats MRR as a read and always applies relevant turnaround times, any value programmed in this CR must be greater than those turnaround times for D-Unit to enforce any additional time from previous read/writes.

5.4.9 DRAM Timing Register 7A (D_CR_DTR7A)—Offset 1424h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: D060C06h

Bit Range	Default & Access	Field Name (ID): Description
31:26	3h RW	**All Bank Precharge to Activate Command Delay [tRPab] (TRPAB):** Specifies the delay between a DRAM Precharge All Bank command and a DRAM Activate command (in DRAM Clocks). Note: This CR should be constrained to a minimum of 4 in LP3 and minimum of 8 in LP4. Note: Derating adds 1.875ns to this timing. • For LPDDR, tRPpb = tRP, tRPab = tRP + 3ns. • For DDR3L 8ch tRPpb = tRPab = tRP.
25:23	2h RW	**Mode Register Write to any Command Delay [tMRD/tMRW] (TPSTMRWBLK):** Specifies the quiet time after issuing MRW command (in 8 x DRAM clocks). Note: This time covers for both tMRD and tMRW.
22:16	6h RW	**Write Command to Power Down Delay [tWRPDEN] (TWRPDEN):** Specifies the minimum time between a write command to PowerDown command (in DRAM clocks). Must be at least equal to tWR + tCCD + tWL + 2.
15:9	6h RW	**Read Command to Power Down Delay [tRDPDEN] (TRDPDEN):** Specifies the minimum time between a read command to PowerDown command (in DRAM clocks). Must be at least equal to CL/RL + tDQSCKmax + tCCD + tRPST.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RO	**Reserved (RSVD8_7):** Reserved.
6:0	6h RW	**Row Activation Period [tRAS] (TRAS):** Specifies the minimum delay between the DRAM Activate and Precharge commands to the same bank (in DRAM clocks). Note: Derating adds 1.875ns to this timing.

5.4.10 DRAM Timing Register 8A (D_CR_DTR8A)—Offset 1428h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: CC50A18h

Bit Range	Default & Access	Field Name (ID): Description
31:26	3h RW	**Minimum Self-Refresh Time [tSR/tCKESR] (TCKESR):** Specifies the minimum time that DRAM should remain in SR (in DRAM clocks).
25:21	6h RW	**Minimum Low Power Mode Residency (LPMDRES):** Specifies the minimum time that PHY should remain in LPMode (in DRAM clocks).
20:15	Ah RW	**Low Power Mode Exit to Clock Enable Delay (LPMDTOCKEDLY):** Specifies the minimum time between the LP Mode exit to the CK stop/tristate deassertion and powerdown exit (in DRAM clocks). Note: Must be equal to t_idle_latency and less than 0x3C.
14:8	Ah RW	**Clock Stop to Low Power Mode Delay (CKETOLPMDDLY):** Specifies the time between CK stop/tristate to the Low Power Mode entry. This timing parameter is used to delay Low Power Mode entry (in DRAM clocks). Note: Must be at least equal to t_idle_length parameter and less than 0x7C.
7:0	18h RW	**Power Down Idle Timer (PWDDLY):** This is a non-JEDEC timing parameter used to delay powerdown entry (in DRAM clocks).

5.4.11 D-Unit ODT Control Register A (D_CR_DOCRA)—Offset 142Ch

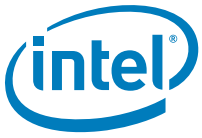
Specifies the parameters to control DRAM ODT.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29	0h RW	**Rank 1 Read ODT Control (R1RDODTCTL):** Specifies the behavior of ODT signals when a Read command is issued to Rank 1. 0 - Read ODT is disabled for Rank 1 1 - Assert ODT to for Rank 0 (non-targeted Rank) Note: This register should be set to 0 for LPDDR3 devices
28	0h RW	**Rank 0 Read ODT Control (R0RDODTCTL):** Specifies the behavior of ODT signals when a Read command is issued to Rank 0. 0 - Read ODT is disabled for Rank 0 1 - Assert ODT to for Rank 1 (non-targeted Rank) Note: This register is reserved for LPDDR3 devices
27:26	0h RW	**Rank 1 Write ODT Control (R1WRODTCTL):** Specifies the behavior of ODT signals when a Write command is issued to Rank 1. 00 - Write ODT is disabled 01 - Assert ODT to Rank 0 (non-targeted Rank) 10 - Assert ODT to Rank 1 (targeted Rank) 11 - Assert ODT to Rank 0 and Rank 1 Note: 10 and 11 are reserved values for LPDDR3
25:24	0h RW	**Rank 0 Write ODT Control (R0WRODTCTL):** Specifies the behavior of ODT signals when a Write command is issued to Rank 0. 00 - Write ODT is disabled 01 - Assert ODT to Rank 0 (targeted Rank) 10 - Assert ODT to Rank 1 (non-targeted Rank) 11 - Assert ODT to Rank 0 and Rank 1 Note: 10 and 11 are reserved values for LPDDR3
23:18	0h RO	**Reserved (RSVD23_18):** Reserved.
17:14	0h RW	**Read ODT assertion to de-assertion delay (DDR3L Only) (RDODTSTOP):** Specifies Read ODT assertion to ODT de-assert delay (in DRAM clocks). DDR3L Equation: RDODTSTOP = DOCRx.WRODTSTOP (subtract 1 if DOCRx.WRODTSTART = 1 in 2N mode).
13	0h RO	**Reserved (RSVD13):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
12:9	0h RW	**Read command to ODT assertion delay (DDR3L Only) (RDODTSTART):** Specifies Read ODT assertion delay after Read Command (in DRAM clocks). DDR3L Equation: RDODTSTART = CL CWL (add 1 if DOCRx.WRODTSTART = 0 in 2N mode). The max value for this CR is 0xE
8:5	0h RW	**Write ODT Assertion to De-assertion Delay (WRODTSTOP):** Specifies number of clocks after ODT assertion that D-Unit deasserts ODT signal (in DRAM clocks). LPDDR3 Equation: WRODTSTOP = RU(tODTon(max)/tCK) + RU((tDQSSmax+tWPST)/tCK) + BL/2 - RD(tODToffmin/tCK) DDR3L Equation: WRODTSTOP >= 6
4	0h RO	**Reserved (RSVD4):** Reserved.
3:0	0h RW	**Write command to ODT assertion delay (WRODTSTART):** Specifies number of clocks after Write command that D-Unit asserts ODT signal (in DRAM clocks). LPDDR3 Equation: WRODTSTART = WL - RU(tODTon(max)/tCK) DDR3L Equation: WRODTSTART = 0 Note: DDR3 spec requires ODT to be asserted high when the DRAM Write command is issued. In DDR3L 2N mode the value can be set to 0 to assert ODT one DRAM clock earlier than the Write Command (WR) or set to 1 to assert at the same clock as command (CS assertion). The max value for this CR is 0xE

5.4.12 D-Unit Power Management Control 0 (D_CR_DPMC0)—Offset 1430h

Specifies the parameters to control D-Unit power management features.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD31_29):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28:24	0h RW	**SUSPEND/SUSPENDP Power Management Message Opcode (SUSPMOP):** DDRIO PHY Power Mode Opcode: After the D-Unit has placed the DRAM devices in Self Refresh/PASR mode as the result of a SUSPEND/SUSPENDP message, it sends this 5-bit value to the DDRIO PHY to tell it which power saving mode it should enter. Changing this register value while in SUSPEND will have no effect. Note: This opcode cannot be a PM state where it disables PHY PLLs i.e PM7 in LPDDR PHY.
23	0h RO	**Reserved (RSVD23):** Reserved.
22	0h RW	**PM Message Wait for Clock Gate Enable (SRPMCLKW):** Specifies when it is safe to send PM message to the PHY. When enabled, D-Unit waits for SPID Clock to deassert before sending a PM message on SR entry. • 0: D-Unit will not wait for SPID_clk to deassert before sending the PM message to PHY. • 1: D-Unit will wait for SPID_clk to deassert before sending PM message to the PHY. Note: The value must be 1 when DYNPMOP = 7h.
21:17	0h RW	**Dynamic Self-Refresh Power Management Message Opcode (DYNPMOP):** DDRIO PHY Power Mode Opcode: After the D-Unit has placed the DRAM devices in Self Refresh mode as the result of a Dynamic Self-Refresh, it sends this 5bit value to the DDRIO PHY to tell it which power saving mode it should enter. Changing this register value while in self-refresh will only change the PM state for the next entry in DynSR.
16	0h RW	**Dynamic Self-Refresh Enable (DYNSREN):** When set to 1, the D-Unit will automatically control DRAM Self Refresh entry and exit based on interface state and requests in pending queues. When there is no pending request in the queues and PMI is idle, then the D-Unit will place the DRAM devices in Self Refresh mode. The DRAM devices will be brought out of Self-Refresh when idle conditions don't hold.
15:0	0h RW	**Self-Refresh Entry Delay (SREDLY):** Specifies the minimum time the D-Unit will wait before it enters Dynamic Self-Refresh mode when idle (in 16x DRAM Clocks). Note: The value in this field needs to be minimum of 4 in functional mode and minimum of 50 in PSMI mode.

5.4.13 D-Unit Power Management Control 1 (D_CR_DPMC1)—Offset 1434h

Specifies the parameters to control D-Unit power management features.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10000028h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29	0h RW	**D-Unit Repeaters Clock Gate Disable (RPTCLKGTDIS):** Setting this bit to 0 allows majority of the repeaters between D-Unit and PHY to clock gate when there is no activity in order to save power. 0 - Enable Repeaters clock gating, 1 - Disable Repeaters clock gating. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.
28	1h RW	**IOSF-SB End Point Clock Gate Disable (SBEPCLKGTDIS):** Setting this bit to 0 enables the clock gating of IOSF-SB End Points in D-Unit and CPGC when there is no IOSF-SB activity in order to save power. 0 - Enable IOSF-SB EP clock gating, 1 - Disable IOSF-SB clock gating. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.
27	0h RW	**Local Clock Gate Disable (CLKGTDIS):** Setting this bit to 0 allows the majority of the D-Unit clocks to be gated off when there is no activity in order to save power. When set to 1, D-Unit clockgating is disabled. • 0: Enable. • 1: Disable. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.
26	0h RW	**Chip Select Tristate Enable (CSTRIST):** • 0: The DRAM CS pins associated with the enabled ranks are never tristated. • 1: The DRAM CS pins are tristated when DRAM clock is stopped or tristated. Note: CS is not tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1).
25:24	0h RW	**Command/Address Tristate (CMDTRIST):** • 00: The DRAM CA pins are never tristated. • 01: The DRAM CA pins are only tristated when all enabled CKE pins are low. • 10: The DRAM CA pins are tristated when not driving a valid command. • 11: Reserved
23:16	0h RW	**Partial Array Self-Refresh Segment Mask (PASR):** This is the Segment Mask used for the MRW to enable PASR during SUSPENDP (Partial Array Self Refresh entry).

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Page Close Timeout Period (PCLSTO):** Specifies the time from the last access of a DRAM page until that page is scheduled to close by sending a Precharge command to DRAM (in 16 x DRAM clocks).
7	0h RW	**Page Close Timeout Disable (PCLSTODIS):** When disabled, D-Unit will not close the DRAM page when idle. • 0: Enable page close timer. • 1: Disable page close timer (Used during DRAM init and DDRIO training).
6	0h RO	**Reserved (RSVD6):** Reserved.
5	1h RW	**ODT Tristate Enable (ODTTRIST):** • 0: The DRAM ODT pins associated with the enabled ranks are never tristated. • 1: DRAMs ODT pins are tristated when DRAM clock is stopped or tristated. Note: ODT is not tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1)
4:3	1h RW	**Clock Stop/Tristate Enable (ENCKSTP):** Enable/Disable CK Stop/Tristate During Power down. • 00: Disable CK Stop/Tristate During Power down. • 01: Enable CK Stop During Power down. • 10: Enable CK Tristate During Power down. • 11: Reserved Note: CK is not stopped or tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1).
2:1	0h RW	**Low Power Mode Opcode (LPMODEOP):** D-Unit will send the value in this register after it has entered Powerdown Mode and has stopped/tristated the clock. 00: Disable LPMode. Note: LPMODE entry is not possible when global tristate flow is disabled (DCBR.TRISTDIS = 1).
0	0h RW	**Disable Power Down (DISPWRDN):** Setting this bit to 1 disables dynamic control of DRAM Power-Down entry and exit by keeping the CKE pins driven high. BIOS may set it to 1 during DRAM initialization and DDRIO training. This bit should be set to 0 for normal operation. • 0: The D-Unit dynamically controls the CKE pins to place the DRAM devices in Power Down mode and bring them out of Power Down mode. • 1: The D-Unit constantly drives the CKE pins high to keep the DRAM devices from entering Power Down mode when ranks are idle. Note: This bit is overridden if CKEMODE = 1. This bit does not control CKE behavior on SR entry/exit.

5.4.14 DRAM Refresh Control (D_CR_DRFC)—Offset 1438h

Specifies the parameters to control scheduling of refresh commands.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1750h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD31_22):** Reserved.
21	0h RW	**Disable Refresh Debt Clear (DISREFDBTCLR):** When set, D-Unit will not clear refresh debt before Self Refresh SR Entry: • 0: D-Unit sends all postponed REF commands to DRAM before it enters Self Refresh. • 1: D-Unit enters SR without clearing the Refresh Debt (for Debug only).
20	0h RW	**Refresh Skew Disable (REFSKWDIS):** Disables Skewing of Refresh Counting between Ranks. Each rank has its own refresh counter. By default incrementing these refresh counters are skewed by 1/2 the tREFI period. Setting this bit to a 1 disables this feature and all refresh counters will increment at the same time per tREFI period. Skewing the tREFI counters can improve performance since traffic to all ranks does not have to be blocked to perform refresh. • 0: Incrementing the refresh counters are skewed by 1/2 tREFI period. • 1: All refresh counters will increment at the same time per tREFI period.
19:18	0h RO	**Reserved (RSVD19_18):** Reserved.
17:16	0h RO	**Reserved (RSVD17_16):** Reserved.
15	0h RW	**Extra Refresh Debit (EXTRAREFDBT):** When set to 1, D-Unit adds one extra refresh debit (for a total of two) on Self-refresh exit.
14:12	1h RW	**Minimum Refresh Rate (MINREFRATE):** Ensures that refresh rate never drops below a certain limit regardless of TQ polling. • 000: Disable tREFI counter and stop issuing refresh commands. • 001: 0.25x refresh rate (i.e. 4x tREFI same as no limit). • 010: 0.5x refresh rate (i.e. 2x tREFI). • 011: 1x refresh rate (i.e. 1x tREFI). • 100: 2x refresh rate (i.e. 0.5x tREFI). • 101: 4x refresh rate (i.e. 0.25x tREFI). • 110: 4x refresh rate with derating forced on i.e. 0.25x tREFI. • 111: Reserved.
11:8	7h RW	**Refresh Panic Watermark (REFWMPNC):** When the Refresh counter per rank is greater than this value, the D-Unit will send a REF command to the rank regardless of pending requests. Note: REFWMPNC must be greater than or equal to REFWMHI and greater than 2, Max Value must be less than 8 to not violate 9xtREFI JEDEC requirement.

Bit Range	Default & Access	Field Name (ID): Description
7:4	5h RW	**Refresh High Watermark (REFWMHI):** When the Refresh counter per rank is greater than this value, the D-Unit will send a REF command to the rank if there is no critical priority requests in the pending queues. Note: Value must be greater or equal to 1 and less than or equal to REFWMPNC.
3:1	0h RO	**Reserved (RSVD3_1):** Reserved.
0	0h RW	**Opportunistic Refresh Disable (OREFDIS):** Disable opportunistic scheduling of refresh. • 0: D-Unit will send a REF command only if there is no pending request to that rank. • 1: D-Unit will not send any opportunistic refreshes. Refresh commands are only sent when the refresh counter is greater than REFWMHI. Note: When set, DISREFDBTCLR must also be set to be able to enter SR.

5.4.15 D-Unit Scheduler (D_CR_DSCH)—Offset 143Ch

Specifies parameters to control scheduling of commands to DRAM.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3901C08h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:29	0h RW	**BGF Early Read Data Valid (BGF_EARLY_RDDATA_VALID):** Specifies the number of clocks the D-Unit sends the read data valid through the BGF earlier as compared to the data. • 00: Always write read valid in same SPID clock as data. • 01: Always write read valid one SPID clock before data. • 10: Write read valid up to 2 SPID clocks before data. • 11: Reserved
28:27	0h RW	**SPID Early Read Data Valid (SPID_EARLY_RDDATA_VALID):** Specifies the delay in SPID clocks from RDDATA_VALID assertion to actual data on SPID. The value should match what is programmed in DDRIO (PHY).
26:21	1Ch RW	**Write Pending Queue Count (WPQCOUNT):** Used to limit the number of available slots in Write Pending Queue/ Write Data Buffer. WPQCOUNT will only recognize changes when PMI ISM is not active.

Bit Range	Default & Access	Field Name (ID): Description
20:16	10h RW	**Read Pending Queue Count (RPQCOUNT):** Used to limit the number of entries in Read Pending Queue. RPQCOUNT will only recognize changes when PMI ISM is not active.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:10	7h RW	**Read Return Data Additional Credits (BLKRDBF_ADD_RDDATA_CR):** Number of additional full cacheline (64B) read data return credits exposed to D-Unit when BLKRDBF is set. Note: The value in this field has no effect on Read return credits when BLKRDBF is not set.
9:8	0h RW	**In-Order Mode (INORDERMODE):** • 0h: In order mode disabled: Commands are sent out of order. • 1h: Partial in order mode: Read and Write CAS commands are sent in the order they were received. ACT and PRE can go out of order. • 2h: Full in order mode serialized test: All DRAM commands CAS ACT PRE associated with a PMI request are issued to DDR before any DRAM commands for a subsequent PMI request. • 3h: Reserved. In order modes should be enabled during init/training/CPGC testing. Should never be changed while the D-Unit queues are nonempty.
7	0h RW	**Idle Bypass Mode Enable (BYPASSEN):** Reserved.
6	0h RW	**Block When RDB Full (BLKRDBF):** When set D-Unit stops scheduling new read commands to DRAM when the read data buffer (RDB) is full.
5:4	0h RW	**Stretch Mode (STRETCHMODE):** When stretch mode is enabled, commands are initiated only on Phase 0 of SPIDClk. • 00: Stretch mode is disabled. • 01: Commands are initiated on Phase 0 of every SPID clocks. • 10: Commands are initiated on Phase 0 of even SPID clocks. • 11: Commands are initiated on Phase 0 of odd SPID clocks.
3:0	8h RW	**Masked Write Turnaround Delta (TMWR_TA_DELTA):** The value in this register is subtracted from Masked Write to Read, Masked Write to Write and Masked Write to Masked Write turnaround times to account for half BL MWr commands in LPDDR4. • LPDDR4: = MWr tCCD = MWr BL/2 = 8.

5.4.16 DRAM Calibration Control (D_CR_DCAL)—Offset 1440h

Specifies parameters to control ZQ Calibration.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1057h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ZQ Calibration Type (ZQCALTYPE):** Determines whether the ZQ Calibration is a long or short calibration command (due to ZQCALSTRT). 0: Short calibration (ZQCS). 1: Long calibration (ZQCL).
30	0h RW/V	**ZQ Calibration Start Rank 1 (ZQCALSTRTR1):** Set this bit to 1 to start the ZQ calibration sequence on Rank 1. This bit will remain a 1 until the ZQ calibration is complete for rank 1, then it will return to 0. 0: ZQ calibration is done. 1: ZQ calibration has started and is in progress.
29	0h RW/V	**ZQ Calibration Start Rank 0 (ZQCALSTRTR0):** Set this bit to 1 to start the ZQ calibration sequence on Rank 0. This bit will remain a 1 until the ZQ calibration is complete for rank 0, then it will return to 0. 0: ZQ calibration is done. 1: ZQ calibration has started and is in progress.
28:23	0h RO	**Reserved (RSVD28_23):** Reserved.
22:21	0h RW	**Self-Refresh Exit ZQ Calibration Control (SRXZQC):** • 00: On DynSR exit ZQ timer determines the ZQ type. When the state is lost (i.e due to AutoPG/S0ix) ZQCL is always performed. • 01: Always perform ZQCL after self refresh exit, in LPDDR4, ZQ with traffic blocked. • 10: Always perform ZQCS on SR exit. For LPDDR4, ZQ while traffic is allowed. • 11: No ZQCL commands are sent (it disables ZQCAL commands on SR exit).
20:18	0h RO	**Reserved (RSVD20_18):** Reserved.
17	0h RW	**ZQ Calibration Mode (ZQCLMODE):** Specifies how ZQCal commands are sent to different ranks. • 0: ZQCal commands are sent in parallel to all ranks. • 1: ZQCal commands are sent serially to each rank.
16	0h RW	**Periodic ZQ Calibration Disable (ZQCDIS):** • 0: Periodic ZQ Calibration is Enabled. • 1: Disable periodic ZQ Calibration.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:0	1057h RW	**ZQ Calibration Interval (ZQINT):** Specifies the time interval between two ZQCS (LPDDR3) or ZQ Start (LPDDR4) commands to a DRAM device. (in RTC 32.8KHz clocks)

5.4.17 VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 144Ch

Specifies parameters for VNN Scaling Timer in D-Unit. The values in this register will be set by P-code during VNN scaling period.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VNN Scaling Timer Enable (VNN_TIMER_EN):** • 0: The D-Unit VNN Scaling Timer is disabled. • 1: The D-Unit VNN Scaling Timer is enabled.
30:12	0h RO	**Reserved (RSVD30_12):** Reserved.
11:0	0h RW	**VNN Timer Time (VNN_TIMER_TIME):** The final timer value (in 16 x DRAM clocks).

5.4.18 Periodic DRAM Temperature Polling Control (TQ) (D_CR_TQCTL)—Offset 1450h

Specifies the control for periodic temperature monitoring and control of DRAM device.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6C000008h

Bit Range	Default & Access	Field Name (ID): Description
31:29	3h RW/V	**TQ Data Rank 1 (TQDATAR1):** If Rank 1 is disabled, this value will remain zero. This field contains the data of the last DRAM Mode Register Read to MR4 MRR issued. It is overwritten with each command.
28:26	3h RW/V	**TQ Data Rank 0 (TQDATAR0):** This field contains the data of the last DRAM Mode Register Read to MR4 MRR issued. It is overwritten with each command.
25:22	0h RO	**Reserved (RSVD25_22):** Reserved.
21:8	0h RW	**TQ Poll Period (TQPOLLPER):** This sets the frequency by which the D-Unit polls the DRAM mode register MR4 to determine required refresh rate (in 4x tREFI units).

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved (RSVD7_5):** Reserved.
4	0h RW	**Self Refresh Temperature Range Enable (DDR3 Only) (SRTEN):** When set, before every Self refresh entry, D-Unit writes a 1 to bit 7 of TQOFFSET.MR_VALUE when TQDATA for that rank indicates a value higher then 0x3, and writes a 0 to that bit otherwise. The new MR_VALUE is then written into MR2 of DDR3 for each enabled rank.
3	1h RW	**Enable Dynamic Timing Derating (ENDERATE):** When set to 1, the Dynamic Timing Derating is enabled. When the D-Unit determines (via TQ polling) that the DRAM requires timing derating in addition to refresh interval adjustment, the D-Unit will automatically adjust the relevant timing parameters.
2	0h RW	**Enable TQ Data Push (TQDATAPUSHEN):** When set to 1, D-Unit pushes the data form the last MR4 read to a punit register.
1	0h RW	**Enable TQ Poll on Self-Refresh Exit (TQPOLLSREN):** This bit enables MR4 read on Self Refresh Exit. If disabled, D-Unit will not read MR4 value on Self-Refresh exit.
0	0h RW	**Enable Periodic TQ Poll (TQPOLLEN):** This bit enables periodic TQ Poll. If disabled, D-Unit will not read MR4 value periodically. Note: Will be enabled only if refreshes are enabled.

5.4.19 TQ Temperature Offset Control (D_CR_TQOFFSET)—Offset 1454h

Specifies temperature offset and refresh rate adjustments requested by software.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:16	0h RW	**MR Value (MR_VALUE):** MR2 Shadow Register (DDR3L Only): BIOS writes the correct value of MR2 register in DDR3L into this field at boot time. D-Unit modifies one bit and rewrites the MR2 into DDR3L DRAM before SR entry.
15:11	0h RO	**Reserved (RSVD15_11):** Reserved
10:8	0h RW	**MR4 Adder (MR4_ADDER):** D-Unit adds the value of this field to TQDATA read from MR4 the resulting value is used to control refresh rate and AC timing derating.

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved (RSVD7_3):** Reserved.
2	0h RW/V	**MR3 Offset Update (MR3_OFFSET_UPDATE):** When set, D-Unit writes the merged value of MR3_VALUE and MR3_THERM_OFFSET into MR3 of DRAM. D-Unit clears this bit once the value is written.
1:0	0h RW	**MR3 Thermal Offset (MR3_THERM_OFFSET):** Reserved.

5.4.20 D-Unit Control Operations (D_CR_DCO)—Offset 1458h

Specifies D-Unit initialization and control operation.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Initialization Complete (IC):** Indicates that initialization of the D-Unit has been completed. Memory accesses are permitted and maintenance operation begins. Until this bit is set to a 1, the memory controller will not accept DRAM requests from the Bunit/ GSA/2LM (PMI ISMs will not leave idle). Note: Set this bit to 1 only when all other D-Unit registers have been configured. Usually set at the last configuration step by BIOS on cold/warm reset. D-Unit hardware sets this bit on SR exit.
30	0h RO/V	**DDRIO PHY Initialization Complete (DIOIC):** Status indication that the DDRIO PHY initialization is complete reflects the status spid_init_complete signal.
29	0h RO	**Reserved (RSVD29):** Reserved.
28	0h RW	**PMI Control Select (PMICTL):** • 0: D-Unit PMI is connected to Bunit/GSA/2LM. • 1: D-Unit PMI is connected to CPGC. Note: D_CR_DSCH_BYPASSEN must be set to 0 in CPGC mode. Note: PMI must be idle and D-Unit BGF_RUN = 0 before changing the value in this register.
27:8	0h RO	**Reserved (RSVD27_8):** Reserved.
7:4	0h RO	**Reserved (RSVD7_4):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Enable PSMI Mode (PSMIEN):** When enabled, D-Unit will synchronize clock crossing signals. • 0: PSMI Mode is disabled. • 1: PSMI Mode is enabled. Note: Change only allowed when D-Unit is idle.
2	0h RW	**Maintenance Reset (MNTRST):** Writing a 1 to this field resets all maintenance timers. Clears all states and also clears refresh debt queues. This bit needs to be cleared by software after at least 3 SPID clocks.
1	0h RW	**Enable Maintenance Operations (MNTEN):** Setting this field to 1 enables all maintenance operations. When DCO.IC is set, the maintenance operations are enabled irrespective of the value of this field.
0	0h RO	**Reserved (RSVD0):** Reserved.

5.4.21 Data Scrambler (D_CR_SCRAMCTRL)—Offset 14A4h

Specifies parameters to control data scrambling in D-Unit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Data Scrambler (SCRM_EN):** When set to 1, data scrambling is enabled. When set to 0, data scrambling is disabled. Should be set before D_CR_BGF_CTL_BGF_RUN is set to 1.
30	0h RO	**Reserved (RSVD30):** Reserved.
29:28	0h RW	**Scrambler Clock Gate Select (CLOCKGATE):** This field controls how the scrambler output code is clock gated to reduce power. • 00: Clock gate disabled. • 01: Clock Gate every 2 cycle. • 10: Clock Gate every 3 cycle. • 11: Clock Gate every 4 cycle.
27:16	0h RO	**Reserved (RSVD27_16):** Reserved.
15:0	0h RW	**Scrambling Key (KEY):** Sets the key for the scrambler. The key should be a random value that is set following each cold boot.

5.4.22 Error Injection Address Register (D_CR_ERR_INJ)—Offset 14ACh

Contains the target address for ECC error injection.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:1	0h RW	**Error Injection Target Address (ADDRESS):** Specifies the PMI address of the write transaction to be injected with the error. Only applicable to Write transactions. Read/under-fill read of the partial write operation is not affected.
0	0h RO	**Reserved (RSVD0):** Reserved.

5.4.23 Error Injection Control Register (D_CR_ERR_INJ_CTL)—Offset 14B0h

Controls injecting correctable or uncorrectable errors into the write requests specified by target address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD31_4):** Reserved
3	0h RW	**Error Injection Type Higher 32B (SEL_HI):** If enabled, the error injection is continuously armed for ERR_INJ.ADDR 32B write address matching until it is cleared. • 00: No error injection. • 01: Uncorrectable Error (UE) is armed for write address matching to inject UE by using the same poisoning scheme, i.e. inverting corresponding write ECC[6:0] on QW0 of the 32B data. • 10: Correctable Error (CE) is armed for write address matching to inject CE by inverting corresponding write ECC[0] on QW0 of the 32B data. • 11: Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Error Injection Enable Higher 32B (EN_HI):** When set the error injection is continuously armed for higher 32B of D_CR_ERR_INJ_ADDR write address matching until it is cleared.
1	0h RW	**Error Injection Type Lower 32B (SEL_LO):** 0 - Uncorrectable Error (UE) is armed for write address matching to inject UE by using the same poisoning scheme, i.e. inverting corresponding write ECC[6:0] on every QW of the 32B data. 1 - Correctable Error (CE) is armed for write address matching to inject CE by inverting corresponding write ECC[0] on every QW of the 32B data.
0	0h RW	**Error Injection Enable Lower 32B (EN_LO):** When set, the error injection is continuously armed for lower 32B of D_CR_ERR_INJ_ADDR write address matching until it is cleared.

5.4.24 Error Log Register (D_CR_ERR_ECC_LOG)—Offset 14B4h

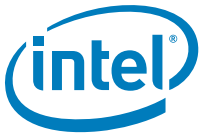
Detected ECC errors are captured in this register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Clear (CLEAR):** Setting this bit to one clears all fields in this register, including itself.
30:29	0h RW	**PMI VISA Byte Select (ECC_VISA):** Select ECC or PMI byte on VISA : • 00: ECC byte, • 01: PMI Data Byte [7:0], • 10: PMI Data Byte [63:56], • 11: PMI Data Byte [255:248]
28	0h RW/V	**Correctable Single-bit Error (CERR):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. A multiple bit error that occurs after this bit is set will override the address/error syndrome information.
27	0h RW/V	**Uncorrectable Multiple-bit Error (MERR):** This bit is set when an uncorrectable multiple-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked until this bit is cleared.



Bit Range	Default & Access	Field Name (ID): Description
26:25	0h RW/V	**Error Burst Number (ERR_BURST):** Burst number (in BL8) of the error within a chunk.
24	0h RW/V	**Error Chunk Number (ERR_CHUNK):** Chunk number of the error. 0 - lower 32B chunk has error if MERR/CERR is set 1 - higher 32B chunk has the error if MERR/CERR is set
23:16	0h RW/V	**Quad Word ECC Syndrome (SYNDROME_QW):** ECC Syndrome for a QW (64 bit) within 32B Address
15:0	0h RW/V	**Request Tag (TAG):** Read Return Tag matches with the PMI Request Tag which triggered the error log.

5.4.25 D-Unit Fuse Status (D_CR_DFUSESTAT)—Offset 14BCh

Contains the values read from D-Unit fuses.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD31_16):** Reserved.
15:0	0h RO/V	**D-Unit Fuse Status (FUSESTAT):** D-Unit fuse bits are captured into this register and are available to be read. • [0]: fus_dun_ecc_dis. • [3:1]: fus_dun_max_supported_device_size[2:0]. • [4:4]: fus_dun_lpddr3_dis. • [5:5]: fus_dun_lpddr4_dis. • [6:6]: reserved. • [7:7]: fus_dun_ddr3l_dis. • [15:8]: reserved.

5.4.26 Major Mode Control (D_CR_MMC)—Offset 1524h

Specifies parameters to control read/write major mode operation and transitions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2B01E518h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:27	5h RW	**RAW Conflict Read Priority for WMM Transition (RAW_WMM):** If a conflict read reaches this priority (or greater depending on access class occupancy), WMM will be triggered to unblock the corresponding write. D-Unit will stay in WMM until corresponding write is issued. Note: The value in this bit must not be higher than lowest terminal priority level of each access class.
26	0h RO	**Reserved (RSVD26):** Reserved.
25:23	6h RW	**Read Isoch Trigger Priority (RIMPRIO):** If any read in the RPQ is at this programmable priority, RIM is triggered.
22:18	0h RO	**Reserved (RSVD22_18):** Reserved.
17:12	1Eh RW	**Write Isoch Threshold (WIMTHRS):** When the number of entries in WPQ is greater than or equal to this value (higher than WMM entry watermark, less than WPQ size), it triggers write isoch mode (WIM).
11:6	14h RW	**Write Major Mode Exit Watermark (WMMEXIT):** When the number of entries in WPQ is less than this value, the D-Unit will switch back to read major mode.
5:0	18h RW	**Write Major Mode Entry Watermark (WMMENTRY):** When the number of entries in WPQ is greater than or equal to this value, the D-Unit will switch to write major mode (WMM). Note: the value must not be set to 0.

5.4.27 Major Mode RD/WR Counter (Set A and B) (D_CR_MMRDWR_AB)—Offset 1528h

Minimum read and maximum write counter control. This register defines the minimum number of reads in RMM and maximum number of writes in WMM before a mode transition happens.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F207C8h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:20	1Fh RW	**Max Writes B (MAXWRB):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set B).

Bit Range	Default & Access	Field Name (ID): Description
19:14	8h RW	**Min Reads B (MINRDB):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set B).
13:12	0h RO	**Reserved (RSVD13_12):** Reserved.
11:6	1Fh RW	**Max Writes A (MAXWRA):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set A).
5:0	8h RW	**Min Reads A (MINRDA):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set A).

5.4.28 Major Mode RD/WR Counter (Set C and D) (D_CR_MMRDWR_CD)—Offset 152Ch

Minimum read and maximum write counter control. This register defines the minimum number of reads in RMM and maximum number of writes in WMM before a mode transition happens (sets C and D).

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F207C8h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:20	1Fh RW	**Max Writes D (MAXWRD):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set D).
19:14	8h RW	**Min Reads D (MINRDD):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set D).
13:12	0h RO	**Reserved (RSVD13_12):** Reserved.
11:6	1Fh RW	**Max Writes C (MAXWRC):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set C).
5:0	8h RW	**Min Reads C (MINRDC):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set C).

5.4.29 Access Class Initial Priority (D_CR_ACCIP)—Offset 1530h

Each field of this register defines the initial priority of one access class.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 17C2h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved (RSVD31_15):** Reserved.
14:12	1h RW	**Access Class 4 Initial Priority (AC4IP):** Initial priority level of read requests coming with access class 4.
11:9	3h RW	**Access Class 3 Initial Priority (AC3IP):** Initial priority level of read requests coming with access class 3.
8:6	7h RW	**Access Class 2 Initial Priority (AC2IP):** Initial priority level of read requests coming with access class 2.
5:3	0h RW	**Access Class 1 Initial Priority (AC1IP):** Initial priority level of read requests coming with access class 1.
2:0	2h RW	**Access Class 0 Initial Priority (AC0IP):** Initial priority level of read requests coming with access class 0.

5.4.30 Access Class 0 Priority Promotion Control (D_CR_RD_PROM0)—Offset 1534h

This register defines the priority promotion policy for access class 0. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F52940h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	Ah RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	Ah RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	Ah RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.4.31 Access Class 1 Priority Promotion Control (D_CR_RD_PROM1)—Offset 1538h

This register defines the priority promotion policy for access class 1. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the associated level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 14000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	Ah RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	0h RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	0h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	0h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.4.32 Access Class 2 Priority Promotion Control (D_CR_RD_PROM2)—Offset 153Ch

This register defines the priority promotion policy for access class 2. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	0h RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	0h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	0h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.4.33 Access Class 3 Priority Promotion Control (D_CR_RD_PROM3)—Offset 1540h

This register defines the aging policy for access class 3. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F29400h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	5h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	5h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

Bit Range	Default & Access	Field Name (ID): Description
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.4.34 Access Class 4 Priority Promotion Control (D_CR_RD_PROM4)—Offset 1544h

This register defines the aging policy for access class 3. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F5294Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	Ah RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	Ah RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	Ah RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	Ah RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.4.35 Deadline Threshold (D_CR_DL_THRS)—Offset 1548h

Specifies when the request with initial priority 0 get promoted to a higher priority level.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD31_11):** Reserved.
10:0	6h RW	**Deadline Threshold (DEADLINE_THRS):** A requests with initial priority of 0 will exit priority 0 when its deadline is equal or less than this value plus current time. This field does not affect the priority of any requests in access classes with initial priority bigger than 0.

5.4.36 Major Mode Blocking Rules Control (D_CR_MM_BLK)—Offset 154Ch

This register controls blocking rules enforced in RMM and WMM.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1800h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved (RSVD31_25):** Reserved.
24	0h RW	**WMM Regular Rule 1 (WMM_REG_R1):** Disable WMM unsafe write page hits block safe write page misses same bank.
23:20	0h RO	**Reserved (RSVD23_20):** Reserved.
19	0h RW	**WMM Priority Rule 4 (WMM_PRIO_R4):** Disable WMM unsafe priority 1 read miss block write hit to same bank. Note: This rule does not block the bank that is being blocked by WMM_PRIO_R3. Priority rules 1, 3 and 4 should be enabled/disabled together.
18	0h RW	**WMM Priority Rule 3 (WMM_PRIO_R3):** Disable WMM unsafe priority 1 write hit block write miss to same bank. Note: This rule does not block the bank that is being blocked by WMM_PRIO_R1. Priority rules 1,3 and 4 should be enabled/disabled together.
17	0h RW	**WMM Priority Rule 2 (WMM_PRIO_R2):** Disable WMM CAS block rule.
16	0h RW	**WMM Priority Rule 1 (WMM_PRIO_R1):** Disable WMM unsafe top priority 1 write miss block write hit same bank. Priority rules 1, 3 and 4 should be enabled/disabled together.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13	0h RW	**RMM Regular Rule 6 (RMM_REG_R6):** Disable RMM unsafe write page hits block safe write page misses same bank.

Bit Range	Default & Access	Field Name (ID): Description
12	1h RW	**RMM Regular Rule 5 (RMM_REG_R5):** Disable RMM unsafe read page miss block all safe and unsafe write page hit to the same bank. Note: This field must not be set to 0 (enabled) if RMM_REG_R4 is also 0.
11	1h RW	**RMM Regular Rule 4 (RMM_REG_R4):** Disable RMM unsafe write page hit block safe read page miss same bank. Note: This field must not be set to 0 (enabled) if RMM_REG_R5 is also 0.
10	0h RW	**RMM Regular Rule 3 (RMM_REG_R3):** Disable RMM unsafe read page hit block safe read and write page miss same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R3 and RMM_PRIO_R1.
9	0h RW	**RMM Regular Rule 2 (RMM_REG_R2):** Disable RMM unsafe read page empty block safe write page empty same rank.
8	0h RW	**RMM Regular Rule 1 (RMM_REG_R1):** Disable RMM unsafe read page hit block safe write page hit same rank.
7:4	0h RO	**Reserved (RSVD7_4):** Reserved.
3	0h RW	**RMM Priority Rule 4 (RMM_PRIO_R4):** Disable RMM unsafe critical read miss block read and write hit to same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R3. Priority rules 1, 3 and 4 should be enabled/disabled together.
2	0h RW	**RMM Priority Rule 3 (RMM_PRIO_R3):** Disable RMM unsafe critical read hit block read and write miss to same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R1. Priority rules 1, 3 and 4 should be enabled/disabled together.
1	0h RW	**RMM Priority Rule 2 (RMM_PRIO_R2):** Disable RMM CAS block rule.
0	0h RW	**RMM Priority Rule 1 (RMM_PRIO_R1):** Disable RMM unsafe top critical read miss block read and write hit same bank. Note: Priority rules 1, 3 and 4 should be enabled/disabled together.

5.4.37 DRAM Self-Refresh Command (D_CR_DRAM_SR_CMD)—Offset 1554h

Self refresh command register to allow sending WAKE and SUSPEND messages to D-Unit. (Only one bit can be set at a time). Posted writes to this register are not completed until hardware clears the field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD31_4):** Reserved.
3	0h RW/V	**SUSPENDP (SUSPENDP):** A SUSPENDP message will put the DRAM into self-refresh mode. The D-Unit will complete servicing outstanding memory requests and flush all queued Refresh commands to DRAM before putting the DRAM in self refresh mode. Finally, a PM message will be sent to the PHY. The bit is cleared by hardware after the PHY indicates the transition requested in the PM message has been completed. D-Unit will perform an MRW to MR17 with an opcode as defined by DPMC0.PASR before it places the DRAM into Self-Refresh.
2	0h RW/V	**SUSPEND (SUSPEND):** A SUSPEND message will put the DRAM into self-refresh mode. The D-Unit will complete servicing outstanding memory requests and flush all queued Refresh commands to DRAM before putting the DRAM in Self Refresh mode. Finally, a PM message will be sent to the PHY. The bit is cleared by hardware only after the PHY indicates the transition requested in the PM message has been completed. Note: When COLDWAKE is set prior of setting this bit the DRAM will not be placed in SR.
1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RW/V	**WAKE (WAKE):** Take PHY out of PM states and wakes the DRAM out of self refresh mode. The bit is cleared by hardware only when the DRAM has exited out of self refresh mode and is accessible. Note: When COLDWAKE is set prior of setting this bit the D-Unit will not send SR exit command and will not set the DCO.IC bit.

5.4.38 DQS Retraining Control (D_CR_DQS_RETRAINING_CTL)—Offset 1580h

LPDDR4 DQS Retraining control register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DQS Periodic Retraining Interval (DQS_RETRAIN_INT):** This sets the frequency by which the D-Unit initiates periodic retraining (in 1x NREFI).

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:4	0h RW	**DQS Oscillator Runtime (DQS_OSC_RT):** After D-Unit starts DQS oscillator, it must wait this amount of time before being able to read the value in MR18 and MR19 (in 16x DRAM clocks). Value in this register must be at least equal to DRAM's MR23 value. + tOSCO.
3:2	0h RO	**Reserved (RSVD3_2):** Reserved.
1	0h RW	**DQS Retrain SRX Exit (DQS_RETRAIN_SRX_EN):** Enable retraining on SR exit. This bit enables LPDDR4 DQS retraining on Self Refresh Exit. If disabled, D-Unit will not perform retraining on SR exit.
0	0h RW	**DQS Retrain Enable (DQS_RETRAIN_EN):** Periodic retraining enable: This bit enables periodic DQS retraining. If disabled, D-Unit will not perform retraining periodically. Note: Will be enabled only if DCO.IC is set and refreshes are enabled in DRF.MINREFRATE.

5.4.39 MR4 De-Swizzle Control (D_CR_MR4_DESWIZZLE)—Offset 1584h

Controls the data bits swizzling crossbar for MR4.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:28	0h RW	**MR4 Bit 2 Select 2nd Byte (MR4_BIT2_SEL2):** Selects bit 2 of MR4 data.
27	0h RO	**Reserved (RSVD27):** Reserved
26:24	0h RW	**MR4 Bit 1 Select 2nd Byte (MR4_BIT1_SEL2):** Selects bit 1 of MR4 data
23	0h RO	**Reserved (RSVD23):** Reserved
22:20	0h RW	**MR4 Bit 0 Select 2nd Byte (MR4_BIT0_SEL2):** Selects bit 0 of MR4 data.

Bit Range	Default & Access	Field Name (ID): Description
19:18	0h RO	**Reserved (RSVD19_18):** Reserved
17:16	0h RW	**MR4 Byte 2 Select (MR4_BYTE_SEL2):** Selects byte position of the MR4 data for second device.
15	0h RO	**Reserved (RSVD15):** Reserved
14:12	0h RW	**MR4 Bit 2 Select (MR4_BIT2_SEL):** Selects bit 2 of MR4 data.
11	0h RO	**Reserved (RSVD11):** Reserved.
10:8	0h RW	**MR4 Bit 1 Select (MR4_BIT1_SEL):** Selects bit 1 of MR4 data.
7	0h RO	**Reserved (RSVD7):** Reserved.
6:4	0h RW	**MR4 Bit 0 Select (MR4_BIT0_SEL):** Selects bit 0 of MR4 data.
3:2	0h RO	**Reserved (RSVD3_2):** Reserved.
1:0	0h RW	**MR4 Byte Select (MR4_BYTE_SEL):** Selects byte position of the MR4 data first device.

5.5 Registers Summary

Table 5-5. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1600h	1603h	DRAM Rank Population 0 (D_CR_DRP0)—Offset 1600h	10000000h
1608h	160Bh	DRAM Timing Register 0A (D_CR_DTR0A)—Offset 1608h	210702CBh
160Ch	160Fh	DRAM Timing Register 1A (D_CR_DTR1A)—Offset 160Ch	30481218h
1610h	1613h	DRAM Timing Register 2A (D_CR_DTR2A)—Offset 1610h	8C080C30h
1614h	1617h	DRAM Timing Register 3A (D_CR_DTR3A)—Offset 1614h	3002EA28h
1618h	161Bh	DRAM Timing Register 4A (D_CR_DTR4A)—Offset 1618h	30209149h
161Ch	161Fh	DRAM Timing Register 5A (D_CR_DTR5A)—Offset 161Ch	304200C2h
1620h	1623h	DRAM Timing Register 6A (D_CR_DTR6A)—Offset 1620h	20100000h
1624h	1627h	DRAM Timing Register 7A (D_CR_DTR7A)—Offset 1624h	D060C06h
1628h	162Bh	DRAM Timing Register 8A (D_CR_DTR8A)—Offset 1628h	CC50A18h
162Ch	162Fh	D-Unit ODT Control Register A (D_CR_DOCRA)—Offset 162Ch	0h
1630h	1633h	D-Unit Power Management Control 0 (D_CR_DPMC0)—Offset 1630h	0h
1634h	1637h	D-Unit Power Management Control 1 (D_CR_DPMC1)—Offset 1634h	10000028h
1638h	163Bh	DRAM Refresh Control (D_CR_DRFC)—Offset 1638h	1750h
163Ch	163Fh	D-Unit Scheduler (D_CR_DSCH)—Offset 163Ch	3901C08h
1640h	1643h	DRAM Calibration Control (D_CR_DCAL)—Offset 1640h	1057h
1644h	1647h	VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 164Ch	20000h

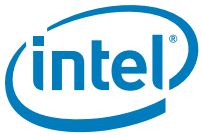


Table 5-5. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
164Ch	164Fh	VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 164Ch	0h
1650h	1653h	Periodic DRAM Temperature Polling Control (TQ) (D_CR_TQCTL)—Offset 1650h	6C000008h
1654h	1657h	TQ Temperature Offset Control (D_CR_TQOFFSET)—Offset 1654h	0h
1658h	165Bh	D-Unit Control Operations (D_CR_DCO)—Offset 1658h	0h
16A4h	16A7h	Data Scrambler (D_CR_SCRAMCTRL)—Offset 16A4h	0h
16ACh	16AFh	Error Injection Address Register (D_CR_ERR_INJ)—Offset 16ACh	0h
16B0h	16B3h	Error Injection Control Register (D_CR_ERR_INJ_CTL)—Offset 16B0h	0h
16B4h	16B7h	Error Log Register (D_CR_ERR_ECC_LOG)—Offset 16B4h	0h
16BCh	16BFh	D-Unit Fuse Status (D_CR_DFUSESTAT)—Offset 16BCh	0h
1724h	1727h	Major Mode Control (D_CR_MMC)—Offset 1724h	2B01E518h
1728h	172Bh	Major Mode RD/WR Counter (Set A and B) (D_CR_MMRDWR_AB)—Offset 1728h	1F207C8h
172Ch	172Fh	Major Mode RD/WR Counter (Set C and D) (D_CR_MMRDWR_CD)—Offset 172Ch	1F207C8h
1730h	1733h	Access Class Initial Priority (D_CR_ACCIP)—Offset 1730h	17C2h
1734h	1737h	Access Class 0 Priority Promotion Control (D_CR_RD_PROM0)—Offset 1734h	1F52940h
1738h	173Bh	Access Class 1 Priority Promotion Control (D_CR_RD_PROM1)—Offset 1738h	14000000h
173Ch	173Fh	Access Class 2 Priority Promotion Control (D_CR_RD_PROM2)—Offset 173Ch	0h
1740h	1743h	Access Class 3 Priority Promotion Control (D_CR_RD_PROM3)—Offset 1740h	1F29400h
1744h	1747h	Access Class 4 Priority Promotion Control (D_CR_RD_PROM4)—Offset 1744h	1F5294Ah
1748h	174Bh	Deadline Threshold (D_CR_DL_THRS)—Offset 1748h	6h
174Ch	174Fh	Major Mode Blocking Rules Control (D_CR_MM_BLK)—Offset 174Ch	1800h
1754h	1757h	DRAM Self-Refresh Command (D_CR_DRAM_SR_CMD)—Offset 1754h	0h
1780h	1783h	DQS Retraining Control (D_CR_DQS_RETRAINING_CTL)—Offset 1780h	0h
1784h	1787h	MR4 De-Swizzle Control (D_CR_MR4_DESWIZZLE)—Offset 1784h	0h

5.5.1 DRAM Rank Population 0 (D_CR_DRP0)—Offset 1600h

Rank configuration register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**DRAM Device Per Rank (DRAMDEVICE_PR):** Specifies the number of DRAM devices that are ganged together to form a single rank. • 00: 1 DRAM device in each rank. • 01: 2 DRAM devices in each rank. • 10: 4 DRAM devices in each rank. • 11: 8 DRAM devices in each rank. Note: The actual number of devices is one more than the value programmed when ECC is enabled.
29:28	1h RW	**Address Decode (ADDRDEC):** Specifies the address mapping to be used: • 00: 1KB (A). • 01: 2KB (B). • 10: 4KB (C). • 11: Reserved.
27:25	0h RW	**Burst Length Mode (BLMODE):** • 000: Fixed BL8. • 001: Onthefly BL8. • 010: Fixed BL16. • 011: Onthefly BL16. • 100: Fixed BL32. • 101: Onthefly BL32. • 110-111: Reserved.
24:22	0h RW	**DRAM Type (DRAMTYPE):** • 000: DDR3L. • 001: LPDDR3. • 010: LPDDR4. • 011: Reserved. • 100: Reserved. • 101-111: Reserved. Note: The D-Unit should only use this field if allowed by fuse.
21	0h RW	**ECC Enable (ECCEN):** • 0: ECC is disabled. • 1: ECC is enabled. This bit determines if the D-Unit treats the PMI BE_ECC bits as ECC bits or Byte Enables. The D-Unit should not allow this bit to be set if ECC is disabled by fuse. This should only be used in configurations that support ECC (DDR3L).
20:19	0h RW	**CA Swizzle Type (CASWIZZLE):** • 00: uniDIMM/SODIMM. • 01: BGA. • 10: BGA mirrored (LPDDR3 Only). • 11: UDIMM (DDR3L Only).
18:16	0h RO	**Reserved (RSVD18_16):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Bank Address Hashing Enable (BAHEN):** See Address Mapping section for full description. • 0: Bank Address Hashing disabled. • 1: Bank Address Hashing enabled.
14	0h RW	**Rank Select Interleave Enable (RSIEN):** See Address Mapping section for full description. • 0: Rank Select Interleaving disabled. • 1: Rank Select Interleaving enabled.
13:9	0h RO	**Reserved (RSVD13_9):** Reserved.
8:6	0h RW	**DRAM Device Density (DDEN):** Density of the DRAM devices populated on Ranks 0 and 1. • 000: 4 Gb. • 001: 6 Gb. • 010: 8 Gb. • 011: 12 Gb. • 100: 16 Gb. • 101-111: Reserved. Note: For LPDDR4 this value is the die density.
5:4	0h RW	**DRAM Device Data Width (DWID):** Data width of the DRAM device populated on Ranks 0 and 1. • 00: x8. • 01: x16. • 10: x32. • 11: x64.
3	0h RO	**Reserved (RSVD3):** Reserved.
2	0h RW	**Dual Data Mode Enable (DDMEN):** • 0: PMI Dual Data Mode is disabled in D-Unit, full cacheline read and writes go through a single D-Unit. • 1: PMI Dual Data Mode is enabled, only half cacheline read/ writes go through a single D-Unit.
1	0h RW	**Rank Enable 1 (RKEN1):** Enable Rank 1: Must be set to 1 to enable use of this rank.
0	0h RW	**Rank Enable 0 (RKEN0):** Enable Rank 0: Must be set to 1 to enable use of this rank. Note: Setting this bit to 0 is not a functional mode.

5.5.2 DRAM Timing Register 0A (D_CR_DTR0A)—Offset 1608h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 210702CBh

Bit Range	Default & Access	Field Name (ID): Description
31:25	10h RW	**Valid Clocks Before CKE High [tCKCKEH/tCSCKEH/tCKSRX] (TCKCKEH):** Number of valid clocks before CKE high (in DRAM clocks). • LPDDR4: The value in this register covers both tCKCKEH and tCSCKEH. • DDR3L/LPDDR3: The value covers tCKSRX which is defined as the number of valid DRAM clocks that have to toggle before the issuing of the Self Refresh Exit SRX. This value is also used if the clock frequency is changed or the clock is stopped or tristated during Power Down i.e. the number valid DRAM clocks that have to toggle before the issuing of the Power Down Exit PDX command. tCKCKEH can be used to compensate for clock stabilization delays in the motherboard. Note: D-unit hardware enforces minimum of two SPID clock before CKEH, any value in this register is the additional time.
24:21	8h RW	**Exit Self-Refresh to Valid Commands Requiring a Locked DLL Delay [tXSDLL] (TXSDLL):** D-Unit waits max(tXSR+tZQCL/tZQCS, tXSDLL) before allowing traffic to DRAM (in 64 x DRAM Clocks). LPDDR3/LPDDR4: tXSDLL = 0. DDR3L: tXSDLL = tDLLK = 512 Clocks = 8 x 64 DRAM Clocks. Note: In the equation above, tZQCL/tZQCS = 0 if no ZQ is performed on SR exit.
20:12	70h RW	**Exit Self-Refresh to Valid Command Delay [tXS/tXSR] (TXSR):** DDR3L: tXS - Delay between Self Refresh Exit SRX to any DRAM Command not requiring DLL Lock. LPDDR: tXSR - Delay between Self Refresh Exit SRX to any DRAM Command. (in DRAM clocks).
11:6	Bh RW	**Activate RAS to CAS Command Delay [tRCD] (TRCD):** Specifies the delay between a DRAM Activate command and a DRAM Read or Write command to the same bank (in DRAM clocks). Note: Derating adds 1.875ns to this timing.
5:0	Bh RW	**Precharge to Activate Command Delay of a Single Bank [tRPpb] (TRPPB):** Specifies the delay between a DRAM Precharge command and a DRAM Activate command to the same bank (in DRAM Clocks). Note : this CR should be constrained to a minimum of 4 in LPDDR3 and minimum of 8 in LPDDR4. Note: Derating adds 1.875ns to this timing.

5.5.3 DRAM Timing Register 1A (D_CR_DTR1A)—Offset 160Ch

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 30481218h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Exit Power Down to Next Command Delay [tXP] (TXP):** Specifies the delay from the DRAM Power Down Exit (PDX) command to any valid command (in DRAM clocks). Note: The value in this field must be programmed to tXPDLL when Slow Exit Mode Power-down is enabled for DDR3L.
26	0h RO	**Reserved (RSVD26):** Reserved.
25:14	120h RW	**ZQ (long) Calibration Time [tZQCL/tZQCAL] (TZQCL):** • LPDDR3/DDR3L: tZQCL/tZQoper: Specifies the delay between the DRAM ZQ Calibration Long (ZQCL) command and any DRAM command during normal operation. • LPDDR4: tZQCAL: ZQ Calibration time (in DRAM clocks). Note: This field defines the ZQ Calibration Long delay during normal operation. It is not the same as tZQinit which uses the same ZQCL command but the delay is longer. tZQinit applies only during poweron initialization of the DRAM devices and tZQoper applies during normal operation. BIOS executes the DRAM initialization sequence so it has to ensure tZQinit is met and not the D-Unit.
13:6	48h RW	**ZQ Short Calibration Time [tZQCS] (TZQCS):** ZQCS to any DRAM Command Delay: Specifies the delay between the DRAM ZQ Calibration Short (ZQCS) command and any DRAM command (in DRAM clocks). DDR3L and LPDDR3 only. LPDDR4 does not support ZQCS command
5:0	18h RW	**ZQ Latch Time [tZQLAT] (TZQLAT):** Specifies the delay between the DRAM ZQ Calibration Latch command and any DRAM command (in DRAM clocks). LPDDR4 only.Not used in DDR3L/LPDDR3.

5.5.4 DRAM Timing Register 2A (D_CR_DTR2A)—Offset 1610h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8C080C30h

Bit Range	Default & Access	Field Name (ID): Description
31:23	118h RW	**All Bank Refresh Cycle Time [tRFCab] (NRFCAB):** Specifies the delay between the REFab command to the next valid command. (in DRAM clocks)

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD22_21):** Reserved.
20:17	4h RW	**CKE Minimum Pulse Width [tCKE] (TCKE):** Specifies the minimum time from CKEL to CKEH (in DRAM clocks).
16	0h RO	**Reserved (RSVD16):** Reserved.
15:0	C30h RW	**Refresh Interval Time [tREFI] (NREFI):** Specifies the average time between refresh commands. JEDEC Base Refresh Interval time (in DRAM clocks). Note: D-Unit will ignore the 2 LSBs of this field.

5.5.5 DRAM Timing Register 3A (D_CR_DTR3A)—Offset 1614h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3002EA28h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Read to Precharge Delay [tRDPRE] (TRTP):** Specifies the minimum delay between the DRAM Read and Precharge commands to the same bank (in DRAM clocks). • LPDDR3 Equation: = BL/2 + tRTP - 4. • LPDDR4 Equation: = BL/2 + Max (8, tRTP) - 8. • DDR3L Equation: = tRTP.
26:20	0h RW	**CAS to CAS Command Delay Adder (TCCD_INC):** Specifies the number of clocks to be added to turnaround times (for Stretch Mode). It increases delay between Read to Read or Read to Write commands (in 4 x DRAM clocks).
19:13	17h RW	**Write to Precharge Command Delay [tWRPRE] (TWTP):** Specifies the minimum delay between the DRAM Write command and the Precharge command to the same bank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tWTP = BL/2 + WL + tWR + 1. • DDR3L Equation: tWTP = BL/2 + CWL + tWR.
12:11	1h RW	**DRAM Command Valid Duration (TCMD):** Specifies the number of DRAM clocks a command is held valid on the DRAM Address and Control buses. 1N is the DDR3 basic requirement. 2N is the extended mode for board signal integrity. • 0h: Reserved. • 1h: 1 DRAM Clock (1N). • 2h: 2 DRAM Clocks (2N). • 3h: Reserved. Note: DDR3L only. tCMD must be set to 1N for LPDDR3/LPDDR4.

Bit Range	Default & Access	Field Name (ID): Description
10:6	8h RW	**Write Latency [WL/CWL] (TCWL):** The delay between the internal write command and the availability of the first word of DRAM input data (in DRAM clocks).
5:0	28h RW	**Write CAS to Masked Write CAS Delay Same Bank (TWMWSB):** Specifies the minimum delay between DRAM Write command to Masked Write command to same bank (in DRAM clocks). • LPDDR4 Equation: tWMWSB = tCCDMW (BL16) or tCCDMW + 8 (BL32). Note: Masked Write operation in LPDDR4 is always BL16. D-Unit applies this timing for same rank as well as same bank.

5.5.6 DRAM Timing Register 4A (D_CR_DTR4A)—Offset 1618h

Specifies DRAM timings parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 30209149h

Bit Range	Default & Access	Field Name (ID): Description
31:24	30h RW	**Four Bank Activate Window [tFAW] (TFAW):** A rolling timeframe in which a maximum of four Activate commands can be issued to the same rank. This is to limit the peak current draw from the DRAM devices (in DRAM clocks).
23:18	8h RW	**Write to Read DQ Delay Different Ranks (TWRDR):** Specifies the delay from the start of a Write data burst of one rank to the start of a Read data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tWRDR = WL + tDQSSmax + BL/2 + tWPST - (RL + tDQSCKmin - tRPRE). • LPDDR4 Equation: tWRDR = WL - RL + BL/2 + 4 - tDQSCKmin. • DDR3L Equation: tWRDR = CWL + tDQSSmax + BL/2 + tWPST - (CL + tDQSCKmin - tRPRE). Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj.
17:12	9h RW	**Read to Write DQ Delay Different Ranks (TRWDR):** Specifies the delay from the start of a Read data burst of one rank to the Start of a Write data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tRWDR = RL + tDQSCKmax + BL/2 + tRPST - (WL + tDQSSmin - tWPRE). • LPDDR4 Equation: tRWDR = RL + tDQSCKmax + BL/2 - (WL - 2). • DDR3L Equation: tRWDR = CL + tDQSCKmax + BL/2 + tRPST - (CWL + tDQSSmin - tWPRE). Note: For LPDDR3/4 using ODT, this latency may need to be adjusted by tODTon. Note: For DDR3L using ODT, this latency may need to be increased by one clock.

Bit Range	Default & Access	Field Name (ID): Description
11:6	5h RW	**Write to Write DQ Delay Different Ranks (TWWDR):** Specifies the delay from the start of a Write data burst of one rank to the start of a Write data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tWWDR = BL/2 + tDQSSmax - tDQSSmin + tWPRE. • LPDDR4 Equation: tWWDR = BL/2 + 4 - tDQSSmin. • DDR3L Equation: tWWDR = BL/2 + tDQSSmax - tDQSSmin + tWPRE. Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj.
5:0	9h RW	**Read to Read DQ Delay Different Ranks (TRRDR):** Specifies the delay from the start of a Read data burst of one rank to the Start of a Read data burst of a different rank (in DRAM clocks). • LPDDR3/4 Equation: tRRDR = BL/2 + tDQSCKmax - tDQSCKmin + tRPRE. • DDR3L Equation: tRRDR = BL/2 + tRPST + tDQSCKmax - tDQSCKmin + tRPRE + 1.

5.5.7 DRAM Timing Register 5A (D_CR_DTR5A)—Offset 161Ch

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 304200C2h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Row Activation to Row Activation Delay [tRRD] (TRRD):** Specifies the minimum delay in DRAM clocks between two DRAM Activate commands to the same rank but different banks (tRC is the minimum delay between activations of the same bank). Note: Derating adds 1.875ns to this timing.
26	0h RO	**Reserved (RSVD26):** Reserved.
25:23	0h RW	**Derate Increment (TDERATE_INC):** Specifies the additional delay that is added to DRAM timing when indicated by MR4 status. (in DRAM clocks) LPDDR3/LPDDR4: Value is 1.875ns. Note: The value in this register is only added to these timing parameters: tRCD, tRAS, tRP and tRRD.
22:18	10h RW	**Write to Write DQ Delay Same Rank (TWWSR):** Specifies the delay from a DRAM Write to another Write command of the same rank (in DRAM clocks). LPDDR3/LPDDR4/DDR3L Equation: tRRSR = tCCD.

Bit Range	Default & Access	Field Name (ID): Description
17:13	10h RW	**Read to Read DQ Delay Same Rank (TRRSR):** Specifies the delay from a DRAM Read to another Read command of the same rank (in DRAM clocks). LPDDR3/LPDDR4/DDR3L Equation: tRRSR = tCCD.
12:6	3h RW	**Write to Read DQ Delay Same Rank (TWRSR):** Specifies the delay from a DRAM Read to Write command of the same rank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tWRSR = WL + tDQSSmax + BL/2 + tWTR. • DDR3L Equation: tWRSR = CWL + tDQSSmax + BL/2 + tWPST + tWTR.
5:0	2h RW	**Read to Write DQ Delay Same Rank (TRWSR):** Specifies the delay from a DRAM Read to a Write command of the same rank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tRWSR = RL + tDQSCKmax + BL/2 - WL + tWPRE. • DDR3L Equation: tRWSR = CL + tDQSCKmax + BL/2 + tRPST - (CWL +tDQSSmin - tWPRE). Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj. Note: For DDR3L using ODT, this latency may need to be increased by one clock.

5.5.8 DRAM Timing Register 6A (D_CR_DTR6A)—Offset 1620h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 20100000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	20h RW	**Opportunistic Refresh Idle Timer (OREFDLY):** Rank idle period that defines an opportunity for refresh (in DRAM clocks).
23:19	2h RW	**Valid Clocks After CKE Low [tCKELCK/tCKELCS/tCPDED/tCKSRE] (TCKCKEL):** Specifies the amount of time that DRAM clocks need to toggle after CKE goes low (in DRAM Clocks). • For LPDDR3, this covers tCPDED. • For LPDDR4, this covers both tCKELCK and tCKELCS. • For DDR3L, this is tCKSRE. Note: D-Unit hardware enforces minimum of one SPID clocks after CKEL, any value in this register is the additional time.
18:15	0h RW	**Maintenance Operation Delay (MNTDLY):** When a critical read request is pending in RPQ and a maintenance operation (MRR, ZQCal, Ref, etc, panic refresh is an exception to this delay.) needs to be performed, D-Unit waits this amount of time before performing the maintenance operation to allow for some high priority requests to be issued (in 4x SPID clocks).

Bit Range	Default & Access	Field Name (ID): Description
14:8	0h RW	**Mode Register Read to Any Command Delay (TPSTMRRBLK):** Specifies the quiet time after issuing MRR command (in DRAM Clocks). Note: D-Unit treats MRR as a read and always applies relevant turnaround times, any value programmed in this CR must be greater than those turnaround times for D-Unit to enforce any additional time from MRR to the next read/write.
7	0h RO	**Reserved (RSVD7):** Reserved.
6:0	0h RW	**Any Command to Mode Register Read/Write Delay (TPREMRBLK):** Specifies the quiet time before issuing MRR/MRW command. (in DRAM clocks). Note: D-Unit treats MRR as a read and always applies relevant turnaround times, any value programmed in this CR must be greater than those turnaround times for D-Unit to enforce any additional time from previous read/writes.

5.5.9 DRAM Timing Register 7A (D_CR_DTR7A)—Offset 1624h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: D060C06h

Bit Range	Default & Access	Field Name (ID): Description
31:26	3h RW	**All Bank Precharge to Activate Command Delay [tRPab] (TRPAB):** Specifies the delay between a DRAM Precharge All Bank command and a DRAM Activate command (in DRAM Clocks). Note: This CR should be constrained to a minimum of 4 in LP3 and minimum of 8 in LP4. Note: Derating adds 1.875ns to this timing. • For LPDDR, tRPpb = tRP, tRPab = tRP + 3ns. • For DDR3L 8ch tRPpb = tRPab = tRP.
25:23	2h RW	**Mode Register Write to any Command Delay [tMRD/tMRW] (TPSTMRWBLK):** Specifies the quiet time after issuing MRW command (in 8 x DRAM clocks). Note: This time covers for both tMRD and tMRW.
22:16	6h RW	**Write Command to Power Down Delay [tWRPDEN] (TWRPDEN):** Specifies the minimum time between a write command to PowerDown command (in DRAM clocks). Must be at least equal to tWR + tCCD + tWL + 2.
15:9	6h RW	**Read Command to Power Down Delay [tRDPDEN] (TRDPDEN):** Specifies the minimum time between a read command to PowerDown command (in DRAM clocks). Must be at least equal to CL/RL + tDQSCKmax + tCCD + tRPST.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RO	**Reserved (RSVD8_7):** Reserved.
6:0	6h RW	**Row Activation Period [tRAS] (TRAS):** Specifies the minimum delay between the DRAM Activate and Precharge commands to the same bank (in DRAM clocks). Note: Derating adds 1.875ns to this timing.

5.5.10 DRAM Timing Register 8A (D_CR_DTR8A)—Offset 1628h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: CC50A18h

Bit Range	Default & Access	Field Name (ID): Description
31:26	3h RW	**Minimum Self-Refresh Time [tSR/tCKESR] (TCKESR):** Specifies the minimum time that DRAM should remain in SR (in DRAM clocks).
25:21	6h RW	**Minimum Low Power Mode Residency (LPMDRES):** Specifies the minimum time that PHY should remain in LPMode (in DRAM clocks).
20:15	Ah RW	**Low Power Mode Exit to Clock Enable Delay (LPMDTOCKEDLY):** Specifies the minimum time between the LP Mode exit to the CK stop/tristate deassertion and powerdown exit (in DRAM clocks). Note: Must be equal to t_idle_latency and less than 0x3C.
14:8	Ah RW	**Clock Stop to Low Power Mode Delay (CKETOLPMDDLY):** Specifies the time between CK stop/tristate to the Low Power Mode entry. This timing parameter is used to delay Low Power Mode entry (in DRAM clocks). Note: Must be at least equal to t_idle_length parameter and less than 0x7C.
7:0	18h RW	**Power Down Idle Timer (PWDDLY):** This is a non-JEDEC timing parameter used to delay powerdown entry (in DRAM clocks).

5.5.11 D-Unit ODT Control Register A (D_CR_DOCRA)—Offset 162Ch

Specifies the parameters to control DRAM ODT.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29	0h RW	**Rank 1 Read ODT Control (R1RDODTCTL):** Specifies the behavior of ODT signals when a Read command is issued to Rank 1. 0 - Read ODT is disabled for Rank 1 1 - Assert ODT to for Rank 0 (non-targeted Rank) Note: This register should be set to 0 for LPDDR3 devices
28	0h RW	**Rank 0 Read ODT Control (R0RDODTCTL):** Specifies the behavior of ODT signals when a Read command is issued to Rank 0. 0 - Read ODT is disabled for Rank 0 1 - Assert ODT to for Rank 1 (non-targeted Rank) Note: This register is reserved for LPDDR3 devices
27:26	0h RW	**Rank 1 Write ODT Control (R1WRODTCTL):** Specifies the behavior of ODT signals when a Write command is issued to Rank 1. 00 - Write ODT is disabled 01 - Assert ODT to Rank 0 (non-targeted Rank) 10 - Assert ODT to Rank 1 (targeted Rank) 11 - Assert ODT to Rank 0 and Rank 1 Note: 10 and 11 are reserved values for LPDDR3
25:24	0h RW	**Rank 0 Write ODT Control (R0WRODTCTL):** Specifies the behavior of ODT signals when a Write command is issued to Rank 0. 00 - Write ODT is disabled 01 - Assert ODT to Rank 0 (targeted Rank) 10 - Assert ODT to Rank 1 (non-targeted Rank) 11 - Assert ODT to Rank 0 and Rank 1 Note: 10 and 11 are reserved values for LPDDR3
23:18	0h RO	**Reserved (RSVD23_18):** Reserved.
17:14	0h RW	**Read ODT assertion to de-assertion delay (DDR3L Only) (RDODTSTOP):** Specifies Read ODT assertion to ODT de-assert delay (in DRAM clocks). DDR3L Equation: RDODTSTOP = DOCRx.WRODTSTOP (subtract 1 if DOCRx.WRODTSTART = 1 in 2N mode).
13	0h RO	**Reserved (RSVD13):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
12:9	0h RW	**Read command to ODT assertion delay (DDR3L Only) (RDODTSTART):** Specifies Read ODT assertion delay after Read Command (in DRAM clocks). DDR3L Equation: RDODTSTART = CL CWL (add 1 if DOCRx.WRODTSTART = 0 in 2N mode). The max value for this CR is 0xE
8:5	0h RW	**Write ODT Assertion to De-assertion Delay (WRODTSTOP):** Specifies number of clocks after ODT assertion that D-Unit deasserts ODT signal (in DRAM clocks). LPDDR3 Equation: WRODTSTOP = RU(tODTon(max)/tCK) + RU((tDQSSmax+tWPST)/tCK) + BL/2 - RD(tODToffmin/tCK) DDR3L Equation: WRODTSTOP >= 6
4	0h RO	**Reserved (RSVD4):** Reserved.
3:0	0h RW	**Write command to ODT assertion delay (WRODTSTART):** Specifies number of clocks after Write command that D-Unit asserts ODT signal (in DRAM clocks). LPDDR3 Equation: WRODTSTART = WL - RU(tODTon(max)/tCK) DDR3L Equation: WRODTSTART = 0 Note: DDR3 spec requires ODT to be asserted high when the DRAM Write command is issued. In DDR3L 2N mode the value can be set to 0 to assert ODT one DRAM clock earlier than the Write Command (WR) or set to 1 to assert at the same clock as command (CS assertion). The max value for this CR is 0xE

5.5.12 D-Unit Power Management Control 0 (D_CR_DPMC0)—Offset 1630h

Specifies the parameters to control D-Unit power management features.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD31_29):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28:24	0h RW	**SUSPEND/SUSPENDP Power Management Message Opcode (SUSPMOP):** DDRIO PHY Power Mode Opcode: After the D-Unit has placed the DRAM devices in Self Refresh/PASR mode as the result of a SUSPEND/SUSPENDP message, it sends this 5-bit value to the DDRIO PHY to tell it which power saving mode it should enter. Changing this register value while in SUSPEND will have no effect. Note: This opcode cannot be a PM state where it disables PHY PLLs i.e PM7 in LPDDR PHY.
23	0h RO	**Reserved (RSVD23):** Reserved.
22	0h RW	**PM Message Wait for Clock Gate Enable (SRPMCLKW):** Specifies when it is safe to send PM message to the PHY. When enabled, D-Unit waits for SPID Clock to deassert before sending a PM message on SR entry. • 0: D-Unit will not wait for SPID_clk to deassert before sending the PM message to PHY. • 1: D-Unit will wait for SPID_clk to deassert before sending PM message to the PHY. Note: The value must be 1 when DYNPMOP = 7h.
21:17	0h RW	**Dynamic Self-Refresh Power Management Message Opcode (DYNPMOP):** DDRIO PHY Power Mode Opcode: After the D-Unit has placed the DRAM devices in Self Refresh mode as the result of a Dynamic Self-Refresh, it sends this 5bit value to the DDRIO PHY to tell it which power saving mode it should enter. Changing this register value while in self-refresh will only change the PM state for the next entry in DynSR.
16	0h RW	**Dynamic Self-Refresh Enable (DYNSREN):** When set to 1, the D-Unit will automatically control DRAM Self Refresh entry and exit based on interface state and requests in pending queues. When there is no pending request in the queues and PMI is idle, then the D-Unit will place the DRAM devices in Self Refresh mode. The DRAM devices will be brought out of Self-Refresh when idle conditions don't hold.
15:0	0h RW	**Self-Refresh Entry Delay (SREDLY):** Specifies the minimum time the D-Unit will wait before it enters Dynamic Self-Refresh mode when idle (in 16x DRAM Clocks). Note: The value in this field needs to be minimum of 4 in functional mode and minimum of 50 in PSMI mode.

5.5.13 D-Unit Power Management Control 1 (D_CR_DPMC1)—Offset 1634h

Specifies the parameters to control D-Unit power management features.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10000028h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29	0h RW	**D-Unit Repeaters Clock Gate Disable (RPTCLKGTDIS):** Setting this bit to 0 allows majority of the repeaters between D-Unit and PHY to clock gate when there is no activity in order to save power. 0 - Enable Repeaters clock gating, 1 - Disable Repeaters clock gating. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.
28	1h RW	**IOSF-SB End Point Clock Gate Disable (SBEPCLKGTDIS):** Setting this bit to 0 enables the clock gating of IOSF-SB End Points in D-Unit and CPGC when there is no IOSF-SB activity in order to save power. 0 - Enable IOSF-SB EP clock gating, 1 - Disable IOSF-SB clock gating. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.
27	0h RW	**Local Clock Gate Disable (CLKGTDIS):** Setting this bit to 0 allows the majority of the D-Unit clocks to be gated off when there is no activity in order to save power. When set to 1, D-Unit clockgating is disabled. • 0: Enable. • 1: Disable. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.
26	0h RW	**Chip Select Tristate Enable (CSTRIST):** • 0: The DRAM CS pins associated with the enabled ranks are never tristated. • 1: The DRAM CS pins are tristated when DRAM clock is stopped or tristated. Note: CS is not tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1).
25:24	0h RW	**Command/Address Tristate (CMDTRIST):** • 00: The DRAM CA pins are never tristated. • 01: The DRAM CA pins are only tristated when all enabled CKE pins are low. • 10: The DRAM CA pins are tristated when not driving a valid command. • 11: Reserved
23:16	0h RW	**Partial Array Self-Refresh Segment Mask (PASR):** This is the Segment Mask used for the MRW to enable PASR during SUSPENDP (Partial Array Self Refresh entry).

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Page Close Timeout Period (PCLSTO):** Specifies the time from the last access of a DRAM page until that page is scheduled to close by sending a Precharge command to DRAM (in 16 x DRAM clocks).
7	0h RW	**Page Close Timeout Disable (PCLSTODIS):** When disabled, D-Unit will not close the DRAM page when idle. • 0: Enable page close timer. • 1: Disable page close timer (Used during DRAM init and DDRIO training).
6	0h RO	**Reserved (RSVD6):** Reserved.
5	1h RW	**ODT Tristate Enable (ODTTRIST):** • 0: The DRAM ODT pins associated with the enabled ranks are never tristated. • 1: DRAMs ODT pins are tristated when DRAM clock is stopped or tristated. Note: ODT is not tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1)
4:3	1h RW	**Clock Stop/Tristate Enable (ENCKSTP):** Enable/Disable CK Stop/Tristate During Power down. • 00: Disable CK Stop/Tristate During Power down. • 01: Enable CK Stop During Power down. • 10: Enable CK Tristate During Power down. • 11: Reserved Note: CK is not stopped or tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1).
2:1	0h RW	**Low Power Mode Opcode (LPMODEOP):** D-Unit will send the value in this register after it has entered Powerdown Mode and has stopped/tristated the clock. 00: Disable LPMode. Note: LPMODE entry is not possible when global tristate flow is disabled (DCBR.TRISTDIS = 1).
0	0h RW	**Disable Power Down (DISPWRDN):** Setting this bit to 1 disables dynamic control of DRAM Power-Down entry and exit by keeping the CKE pins driven high. BIOS may set it to 1 during DRAM initialization and DDRIO training. This bit should be set to 0 for normal operation. • 0: The D-Unit dynamically controls the CKE pins to place the DRAM devices in Power Down mode and bring them out of Power Down mode. • 1: The D-Unit constantly drives the CKE pins high to keep the DRAM devices from entering Power Down mode when ranks are idle. Note: This bit is overridden if CKEMODE = 1. This bit does not control CKE behavior on SR entry/exit.

5.5.14 DRAM Refresh Control (D_CR_DRFC)—Offset 1638h

Specifies the parameters to control scheduling of refresh commands.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1750h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD31_22):** Reserved.
21	0h RW	**Disable Refresh Debt Clear (DISREFDBTCLR):** When set, D-Unit will not clear refresh debt before Self Refresh SR Entry: • 0: D-Unit sends all postponed REF commands to DRAM before it enters Self Refresh. • 1: D-Unit enters SR without clearing the Refresh Debt (for Debug only).
20	0h RW	**Refresh Skew Disable (REFSKWDIS):** Disables Skewing of Refresh Counting between Ranks. Each rank has its own refresh counter. By default incrementing these refresh counters are skewed by 1/2 the tREFI period. Setting this bit to a 1 disables this feature and all refresh counters will increment at the same time per tREFI period. Skewing the tREFI counters can improve performance since traffic to all ranks does not have to be blocked to perform refresh. • 0: Incrementing the refresh counters are skewed by 1/2 tREFI period. • 1: All refresh counters will increment at the same time per tREFI period.
19:18	0h RO	**Reserved (RSVD19_18):** Reserved.
17:16	0h RO	**Reserved (RSVD17_16):** Reserved.
15	0h RW	**Extra Refresh Debit (EXTRAREFDBT):** When set to 1, D-Unit adds one extra refresh debit (for a total of two) on Self-refresh exit.
14:12	1h RW	**Minimum Refresh Rate (MINREFRATE):** Ensures that refresh rate never drops below a certain limit regardless of TQ polling. • 000: Disable tREFI counter and stop issuing refresh commands. • 001: 0.25x refresh rate (i.e. 4x tREFI same as no limit). • 010: 0.5x refresh rate (i.e. 2x tREFI). • 011: 1x refresh rate (i.e. 1x tREFI). • 100: 2x refresh rate (i.e. 0.5x tREFI). • 101: 4x refresh rate (i.e. 0.25x tREFI). • 110: 4x refresh rate with derating forced on i.e. 0.25x tREFI. • 111: Reserved.
11:8	7h RW	**Refresh Panic Watermark (REFWMPNC):** When the Refresh counter per rank is greater than this value, the D-Unit will send a REF command to the rank regardless of pending requests. Note: REFWMPNC must be greater than or equal to REFWMHI and greater than 2, Max Value must be less than 8 to not violate 9xtREFI JEDEC requirement.

Bit Range	Default & Access	Field Name (ID): Description
7:4	5h RW	**Refresh High Watermark (REFWMHI):** When the Refresh counter per rank is greater than this value, the D-Unit will send a REF command to the rank if there is no critical priority requests in the pending queues. Note: Value must be greater or equal to 1 and less than or equal to REFWMPNC.
3:1	0h RO	**Reserved (RSVD3_1):** Reserved.
0	0h RW	**Opportunistic Refresh Disable (OREFDIS):** Disable opportunistic scheduling of refresh. • 0: D-Unit will send a REF command only if there is no pending request to that rank. • 1: D-Unit will not send any opportunistic refreshes. Refresh commands are only sent when the refresh counter is greater than REFWMHI. Note: When set, DISREFDBTCLR must also be set to be able to enter SR.

5.5.15 D-Unit Scheduler (D_CR_DSCH)—Offset 163Ch

Specifies parameters to control scheduling of commands to DRAM.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3901C08h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:29	0h RW	**BGF Early Read Data Valid (BGF_EARLY_RDDATA_VALID):** Specifies the number of clocks the D-Unit sends the read data valid through the BGF earlier as compared to the data. • 00: Always write read valid in same SPID clock as data. • 01: Always write read valid one SPID clock before data. • 10: Write read valid up to 2 SPID clocks before data. • 11: Reserved
28:27	0h RW	**SPID Early Read Data Valid (SPID_EARLY_RDDATA_VALID):** Specifies the delay in SPID clocks from RDDATA_VALID assertion to actual data on SPID. The value should match what is programmed in DDRIO (PHY).
26:21	1Ch RW	**Write Pending Queue Count (WPQCOUNT):** Used to limit the number of available slots in Write Pending Queue/ Write Data Buffer. WPQCOUNT will only recognize changes when PMI ISM is not active.

Bit Range	Default & Access	Field Name (ID): Description
20:16	10h RW	**Read Pending Queue Count (RPQCOUNT):** Used to limit the number of entries in Read Pending Queue. RPQCOUNT will only recognize changes when PMI ISM is not active.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:10	7h RW	**Read Return Data Additional Credits (BLKRDBF_ADD_RDDATA_CR):** Number of additional full cacheline (64B) read data return credits exposed to D-Unit when BLKRDBF is set. Note: The value in this field has no effect on Read return credits when BLKRDBF is not set.
9:8	0h RW	**In-Order Mode (INORDERMODE):** • 0h: In order mode disabled: Commands are sent out of order. • 1h: Partial in order mode: Read and Write CAS commands are sent in the order they were recieved. ACT and PRE can go out of order. • 2h: Full in order mode serialized test: All DRAM commands CAS ACT PRE associated with a PMI request are issued to DDR before any DRAM commands for a subsequent PMI request. • 3h: Reserved. In order modes should be enabled during init/training/CPGC testing. Should never be changed while the D-Unit queues are nonempty.
7	0h RW	**Idle Bypass Mode Enable (BYPASSEN):** Reserved.
6	0h RW	**Block When RDB Full (BLKRDBF):** When set D-Unit stops scheduling new read commands to DRAM when the read data buffer (RDB) is full.
5:4	0h RW	**Stretch Mode (STRETCHMODE):** When stretch mode is enabled, commands are initiated only on Phase 0 of SPIDClk. • 00: Stretch mode is disabled. • 01: Commands are initiated on Phase 0 of every SPID clocks. • 10: Commands are initiated on Phase 0 of even SPID clocks. • 11: Commands are initiated on Phase 0 of odd SPID clocks.
3:0	8h RW	**Masked Write Turnaround Delta (TMWR_TA_DELTA):** The value in this register is subtracted from Masked Write to Read, Masked Write to Write and Masked Write to Masked Write turnaround times to account for half BL MWr commands in LPDDR4. • LPDDR4: = MWr tCCD = MWr BL/2 = 8.

5.5.16 DRAM Calibration Control (D_CR_DCAL)—Offset 1640h

Specifies parameters to control ZQ Calibration.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1057h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ZQ Calibration Type (ZQCALTYPE):** Determines whether the ZQ Calibration is a long or short calibration command (due to ZQCALSTRT). 0: Short calibration (ZQCS). 1: Long calibration (ZQCL).
30	0h RW/V	**ZQ Calibration Start Rank 1 (ZQCALSTRTR1):** Set this bit to 1 to start the ZQ calibration sequence on Rank 1. This bit will remain a 1 until the ZQ calibration is complete for rank 1, then it will return to 0. 0: ZQ calibration is done. 1: ZQ calibration has started and is in progress.
29	0h RW/V	**ZQ Calibration Start Rank 0 (ZQCALSTRTR0):** Set this bit to 1 to start the ZQ calibration sequence on Rank 0. This bit will remain a 1 until the ZQ calibration is complete for rank 0, then it will return to 0. 0: ZQ calibration is done. 1: ZQ calibration has started and is in progress.
28:23	0h RO	**Reserved (RSVD28_23):** Reserved.
22:21	0h RW	**Self-Refresh Exit ZQ Calibration Control (SRXZQC):** • 00: On DynSR exit ZQ timer determines the ZQ type. When the state is lost (i.e due to AutoPG/S0ix) ZQCL is always performed. • 01: Always perform ZQCL after self refresh exit, in LPDDR4, ZQ with traffic blocked. • 10: Always perform ZQCS on SR exit. For LPDDR4, ZQ while traffic is allowed. • 11: No ZQCL commands are sent (it disables ZQCAL commands on SR exit).
20:18	0h RO	**Reserved (RSVD20_18):** Reserved.
17	0h RW	**ZQ Calibration Mode (ZQCLMODE):** Specifies how ZQCal commands are sent to different ranks. • 0: ZQCal commands are sent in parallel to all ranks. • 1: ZQCal commands are sent serially to each rank.
16	0h RW	**Periodic ZQ Calibration Disable (ZQCDIS):** • 0: Periodic ZQ Calibration is Enabled. • 1: Disable periodic ZQ Calibration.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:0	1057h RW	**ZQ Calibration Interval (ZQINT):** Specifies the time interval between two ZQCS (LPDDR3) or ZQ Start (LPDDR4) commands to a DRAM device. (in RTC 32.8KHz clocks)

5.5.17 VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 164Ch

Specifies parameters for VNN Scaling Timer in D-Unit. The values in this register will be set by P-code during VNN scaling period.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VNN Scaling Timer Enable (VNN_TIMER_EN):** • 0: The D-Unit VNN Scaling Timer is disabled. • 1: The D-Unit VNN Scaling Timer is enabled.
30:12	0h RO	**Reserved (RSVD30_12):** Reserved.
11:0	0h RW	**VNN Timer Time (VNN_TIMER_TIME):** The final timer value (in 16 x DRAM clocks).

5.5.18 Periodic DRAM Temperature Polling Control (TQ) (D_CR_TQCTL)—Offset 1650h

Specifies the control for periodic temperature monitoring and control of DRAM device.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6C000008h

Bit Range	Default & Access	Field Name (ID): Description
31:29	3h RW/V	**TQ Data Rank 1 (TQDATAR1):** If Rank 1 is disabled, this value will remain zero. This field contains the data of the last DRAM Mode Register Read to MR4 MRR issued. It is overwritten with each command.
28:26	3h RW/V	**TQ Data Rank 0 (TQDATAR0):** This field contains the data of the last DRAM Mode Register Read to MR4 MRR issued. It is overwritten with each command.
25:22	0h RO	**Reserved (RSVD25_22):** Reserved.
21:8	0h RW	**TQ Poll Period (TQPOLLPER):** This sets the frequency by which the D-Unit polls the DRAM mode register MR4 to determine required refresh rate (in 4x tREFI units).

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved (RSVD7_5):** Reserved.
4	0h RW	**Self Refresh Temperature Range Enable (DDR3 Only) (SRTEN):** When set, before every Self refresh entry, D-Unit writes a 1 to bit 7 of TQOFFSET.MR_VALUE when TQDATA for that rank indicates a value higher then 0x3, and writes a 0 to that bit otherwise. The new MR_VALUE is then written into MR2 of DDR3 for each enabled rank.
3	1h RW	**Enable Dynamic Timing Derating (ENDERATE):** When set to 1, the Dynamic Timing Derating is enabled. When the D-Unit determines (via TQ polling) that the DRAM requires timing derating in addition to refresh interval adjustment, the D-Unit will automatically adjust the relevant timing parameters.
2	0h RW	**Enable TQ Data Push (TQDATAPUSHEN):** When set to 1, D-Unit pushes the data form the last MR4 read to a punit register.
1	0h RW	**Enable TQ Poll on Self-Refresh Exit (TQPOLLSREN):** This bit enables MR4 read on Self Refresh Exit. If disabled, D-Unit will not read MR4 value on Self-Refresh exit.
0	0h RW	**Enable Periodic TQ Poll (TQPOLLEN):** This bit enables periodic TQ Poll. If disabled, D-Unit will not read MR4 value periodically. Note: Will be enabled only if refreshes are enabled.

5.5.19 TQ Temperature Offset Control (D_CR_TQOFFSET)—Offset 1654h

Specifies temperature offset and refresh rate adjustments requested by software.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:16	0h RW	**MR Value (MR_VALUE):** MR2 Shadow Register (DDR3L Only): BIOS writes the correct value of MR2 register in DDR3L into this field at boot time. D-Unit modifies one bit and rewrites the MR2 into DDR3L DRAM before SR entry.
15:11	0h RO	**Reserved (RSVD15_11):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**MR4 Adder (MR4_ADDER):** D-Unit adds the value of this field to TQDATA read from MR4 the resulting value is used to control refresh rate and AC timing derating.
7:3	0h RO	**Reserved (RSVD7_3):** Reserved.
2	0h RW/V	**MR3 Offset Update (MR3_OFFSET_UPDATE):** When set, D-Unit writes the merged value of MR3_VALUE and MR3_THERM_OFFSET into MR3 of DRAM. D-Unit clears this bit once the value is written.
1:0	0h RW	**MR3 Thermal Offset (MR3_THERM_OFFSET):** Reserved.

5.5.20 D-Unit Control Operations (D_CR_DCO)—Offset 1658h

Specifies D-Unit initialization and control operation.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Initialization Complete (IC):** Indicates that initialization of the D-Unit has been completed. Memory accesses are permitted and maintenance operation begins. Until this bit is set to a 1, the memory controller will not accept DRAM requests from the Bunit/ GSA/2LM (PMI ISMs will not leave idle). Note: Set this bit to 1 only when all other D-Unit registers have been configured. Usually set at the last configuration step by BIOS on cold/warm reset. D-Unit hardware sets this bit on SR exit.
30	0h RO/V	**DDRIO PHY Initialization Complete (DIOIC):** Status indication that the DDRIO PHY initialization is complete reflects the status spid_init_complete signal.
29	0h RO	**Reserved (RSVD29):** Reserved.
28	0h RW	**PMI Control Select (PMICTL):** • 0: D-Unit PMI is connected to Bunit/GSA/2LM. • 1: D-Unit PMI is connected to CPGC. Note: D_CR_DSCH_BYPASSEN must be set to 0 in CPGC mode. Note: PMI must be idle and D-Unit BGF_RUN = 0 before changing the value in this register.
27:8	0h RO	**Reserved (RSVD27_8):** Reserved.
7:4	0h RO	**Reserved (RSVD7_4):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Enable PSMI Mode (PSMIEN):** When enabled, D-Unit will synchronize clock crossing signals. • 0: PSMI Mode is disabled. • 1: PSMI Mode is enabled. Note: Change only allowed when D-Unit is idle.
2	0h RW	**Maintenance Reset (MNTRST):** Writing a 1 to this field resets all maintenance timers. Clears all states and also clears refresh debt queues. This bit needs to be cleared by software after at least 3 SPID clocks.
1	0h RW	**Enable Maintenance Operations (MNTEN):** Setting this field to 1 enables all maintenance operations. When DCO.IC is set, the maintenance operations are enabled irrespective of the value of this field.
0	0h RO	**Reserved (RSVD0):** Reserved.

5.5.21 Data Scrambler (D_CR_SCRAMCTRL)—Offset 16A4h

Specifies parameters to control data scrambling in D-Unit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Data Scrambler (SCRM_EN):** When set to 1, data scrambling is enabled. When set to 0, data scrambling is disabled. Should be set before D_CR_BGF_CTL_BGF_RUN is set to 1.
30	0h RO	**Reserved (RSVD30):** Reserved.
29:28	0h RW	**Scrambler Clock Gate Select (CLOCKGATE):** This field controls how the scrambler output code is clock gated to reduce power. • 00: Clock gate disabled. • 01: Clock Gate every 2 cycle. • 10: Clock Gate every 3 cycle. • 11: Clock Gate every 4 cycle.
27:16	0h RO	**Reserved (RSVD27_16):** Reserved.
15:0	0h RW	**Scrambling Key (KEY):** Sets the key for the scrambler. The key should be a random value that is set following each cold boot.

5.5.22 Error Injection Address Register (D_CR_ERR_INJ)—Offset 16ACh

Contains the target address for ECC error injection.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:1	0h RW	**Error Injection Target Address (ADDRESS):** Specifies the PMI address of the write transaction to be injected with the error. Only applicable to Write transactions. Read/under-fill read of the partial write operation is not affected.
0	0h RO	**Reserved (RSVD0):** Reserved.

5.5.23 Error Injection Control Register (D_CR_ERR_INJ_CTL)—Offset 16B0h

Controls injecting correctable or uncorrectable errors into the write requests specified by target address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD31_4):** Reserved
3	0h RW	**Error Injection Type Higher 32B (SEL_HI):** If enabled, the error injection is continuously armed for ERR_INJ.ADDR 32B write address matching until it is cleared. • 00: No error injection. • 01: Uncorrectable Error (UE) is armed for write address matching to inject UE by using the same poisoning scheme, i.e. inverting corresponding write ECC[6:0] on QW0 of the 32B data. • 10: Correctable Error (CE) is armed for write address matching to inject CE by inverting corresponding write ECC[0] on QW0 of the 32B data. • 11: Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Error Injection Enable Higher 32B (EN_HI):** When set the error injection is continuously armed for higher 32B of D_CR_ERR_INJ_ADDR write address matching until it is cleared.
1	0h RW	**Error Injection Type Lower 32B (SEL_LO):** 0 - Uncorrectable Error (UE) is armed for write address matching to inject UE by using the same poisoning scheme, i.e. inverting corresponding write ECC[6:0] on every QW of the 32B data. 1 - Correctable Error (CE) is armed for write address matching to inject CE by inverting corresponding write ECC[0] on every QW of the 32B data.
0	0h RW	**Error Injection Enable Lower 32B (EN_LO):** When set, the error injection is continuously armed for lower 32B of D_CR_ERR_INJ_ADDR write address matching until it is cleared.

5.5.24 Error Log Register (D_CR_ERR_ECC_LOG)—Offset 16B4h

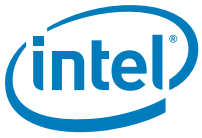
Detected ECC errors are captured in this register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Clear (CLEAR):** Setting this bit to one clears all fields in this register, including itself.
30:29	0h RW	**PMI VISA Byte Select (ECC_VISA):** Select ECC or PMI byte on VISA : • 00: ECC byte, • 01: PMI Data Byte [7:0], • 10: PMI Data Byte [63:56], • 11: PMI Data Byte [255:248]
28	0h RW/V	**Correctable Single-bit Error (CERR):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. A multiple bit error that occurs after this bit is set will override the address/error syndrome information.
27	0h RW/V	**Uncorrectable Multiple-bit Error (MERR):** This bit is set when an uncorrectable multiple-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked until this bit is cleared.



Bit Range	Default & Access	Field Name (ID): Description
26:25	0h RW/V	**Error Burst Number (ERR_BURST):** Burst number (in BL8) of the error within a chunk.
24	0h RW/V	**Error Chunk Number (ERR_CHUNK):** Chunk number of the error. 0 - lower 32B chunk has error if MERR/CERR is set 1 - higher 32B chunk has the error if MERR/CERR is set
23:16	0h RW/V	**Quad Word ECC Syndrome (SYNDROME_QW):** ECC Syndrome for a QW (64 bit) within 32B Address
15:0	0h RW/V	**Request Tag (TAG):** Read Return Tag matches with the PMI Request Tag which triggered the error log.

5.5.25 D-Unit Fuse Status (D_CR_DFUSESTAT)—Offset 16BCh

Contains the values read from D-Unit fuses.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD31_16):** Reserved.
15:0	0h RO/V	**D-Unit Fuse Status (FUSESTAT):** D-Unit fuse bits are captured into this register and are available to be read. • [0]: fus_dun_ecc_dis. • [3:1]: fus_dun_max_supported_device_size[2:0]. • [4:4]: fus_dun_lpddr3_dis. • [5:5]: fus_dun_lpddr4_dis. • [6:6]: reserved. • [7:7]: fus_dun_ddr3l_dis. • [15:8]: reserved.

5.5.26 Major Mode Control (D_CR_MMC)—Offset 1724h

Specifies parameters to control read/write major mode operation and transitions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2B01E518h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:27	5h RW	**RAW Conflict Read Priority for WMM Transition (RAW_WMM):** If a conflict read reaches this priority (or greater depending on access class occupancy), WMM will be triggered to unblock the corresponding write. D-Unit will stay in WMM until corresponding write is issued. Note: The value in this bit must not be higher than lowest terminal priority level of each access class.
26	0h RO	**Reserved (RSVD26):** Reserved.
25:23	6h RW	**Read Isoch Trigger Priority (RIMPRIO):** If any read in the RPQ is at this programmable priority, RIM is triggered.
22:18	0h RO	**Reserved (RSVD22_18):** Reserved.
17:12	1Eh RW	**Write Isoch Threshold (WIMTHRS):** When the number of entries in WPQ is greater than or equal to this value (higher than WMM entry watermark, less than WPQ size), it triggers write isoch mode (WIM).
11:6	14h RW	**Write Major Mode Exit Watermark (WMMEXIT):** When the number of entries in WPQ is less than this value, the D-Unit will switch back to read major mode.
5:0	18h RW	**Write Major Mode Entry Watermark (WMMENTRY):** When the number of entries in WPQ is greater than or equal to this value, the D-Unit will switch to write major mode (WMM). Note: the value must not be set to 0.

5.5.27 Major Mode RD/WR Counter (Set A and B) (D_CR_MMRDWR_AB)—Offset 1728h

Minimum read and maximum write counter control. This register defines the minimum number of reads in RMM and maximum number of writes in WMM before a mode transition happens.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F207C8h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:20	1Fh RW	**Max Writes B (MAXWRB):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set B).

Bit Range	Default & Access	Field Name (ID): Description
19:14	8h RW	**Min Reads B (MINRDB):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set B).
13:12	0h RO	**Reserved (RSVD13_12):** Reserved.
11:6	1Fh RW	**Max Writes A (MAXWRA):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set A).
5:0	8h RW	**Min Reads A (MINRDA):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set A).

5.5.28 Major Mode RD/WR Counter (Set C and D) (D_CR_MMRDWR_CD)—Offset 172Ch

Minimum read and maximum write counter control. This register defines the minumum number of reads in RMM and maximum number of writes in WMM before a mode transition happens (sets C and D).

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F207C8h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:20	1Fh RW	**Max Writes D (MAXWRD):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set D).
19:14	8h RW	**Min Reads D (MINRDD):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set D).
13:12	0h RO	**Reserved (RSVD13_12):** Reserved.
11:6	1Fh RW	**Max Writes C (MAXWRC):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set C).
5:0	8h RW	**Min Reads C (MINRDC):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set C).

5.5.29 Access Class Initial Priority (D_CR_ACCIP)—Offset 1730h

Each field of this register defines the initial priority of one access class.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 17C2h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved (RSVD31_15):** Reserved.
14:12	1h RW	**Access Class 4 Initial Priority (AC4IP):** Initial priority level of read requests coming with access class 4.
11:9	3h RW	**Access Class 3 Initial Priority (AC3IP):** Initial priority level of read requests coming with access class 3.
8:6	7h RW	**Access Class 2 Initial Priority (AC2IP):** Initial priority level of read requests coming with access class 2.
5:3	0h RW	**Access Class 1 Initial Priority (AC1IP):** Initial priority level of read requests coming with access class 1.
2:0	2h RW	**Access Class 0 Initial Priority (AC0IP):** Initial priority level of read requests coming with access class 0.

5.5.30 Access Class 0 Priority Promotion Control (D_CR_RD_PROM0)—Offset 1734h

This register defines the priority promotion policy for access class 0. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F52940h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	Ah RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	Ah RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	Ah RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.5.31 Access Class 1 Priority Promotion Control (D_CR_RD_PROM1)—Offset 1738h

This register defines the priority promotion policy for access class 1. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the associated level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 14000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	Ah RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	0h RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	0h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	0h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.5.32 Access Class 2 Priority Promotion Control (D_CR_RD_PROM2)—Offset 173Ch

This register defines the priority promotion policy for access class 2. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	0h RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	0h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	0h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.5.33 Access Class 3 Priority Promotion Control (D_CR_RD_PROM3)—Offset 1740h

This register defines the aging policy for access class 3. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F29400h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	5h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	5h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

Bit Range	Default & Access	Field Name (ID): Description
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.5.34 Access Class 4 Priority Promotion Control (D_CR_RD_PROM4)—Offset 1744h

This register defines the aging policy for access class 3. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F5294Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	Ah RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	Ah RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	Ah RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	Ah RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.5.35 Deadline Threshold (D_CR_DL_THRS)—Offset 1748h

Specifies when the request with initial priority 0 get promoted to a higher priority level.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD31_11):** Reserved.
10:0	6h RW	**Deadline Threshold (DEADLINE_THRS):** A requests with initial priority of 0 will exit priority 0 when its deadline is equal or less than this value plus current time. This field does not affect the priority of any requests in access classes with initial priority bigger than 0.

5.5.36 Major Mode Blocking Rules Control (D_CR_MM_BLK)—Offset 174Ch

This register controls blocking rules enforced in RMM and WMM.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1800h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved (RSVD31_25):** Reserved.
24	0h RW	**WMM Regular Rule 1 (WMM_REG_R1):** Disable WMM unsafe write page hits block safe write page misses same bank.
23:20	0h RO	**Reserved (RSVD23_20):** Reserved.
19	0h RW	**WMM Priority Rule 4 (WMM_PRIO_R4):** Disable WMM unsafe priority 1 read miss block write hit to same bank. Note: This rule does not block the bank that is being blocked by WMM_PRIO_R3. Priority rules 1, 3 and 4 should be enabled/disabled together.
18	0h RW	**WMM Priority Rule 3 (WMM_PRIO_R3):** Disable WMM unsafe priority 1 write hit block write miss to same bank. Note: This rule does not block the bank that is being blocked by WMM_PRIO_R1. Priority rules 1,3 and 4 should be enabled/disabled together.
17	0h RW	**WMM Priority Rule 2 (WMM_PRIO_R2):** Disable WMM CAS block rule.
16	0h RW	**WMM Priority Rule 1 (WMM_PRIO_R1):** Disable WMM unsafe top priority 1 write miss block write hit same bank. Priority rules 1, 3 and 4 should be enabled/disabled together.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13	0h RW	**RMM Regular Rule 6 (RMM_REG_R6):** Disable RMM unsafe write page hits block safe write page misses same bank.

Bit Range	Default & Access	Field Name (ID): Description
12	1h RW	**RMM Regular Rule 5 (RMM_REG_R5):** Disable RMM unsafe read page miss block all safe and unsafe write page hit to the same bank. Note: This field must not be set to 0 (enabled) if RMM_REG_R4 is also 0.
11	1h RW	**RMM Regular Rule 4 (RMM_REG_R4):** Disable RMM unsafe write page hit block safe read page miss same bank. Note: This field must not be set to 0 (enabled) if RMM_REG_R5 is also 0.
10	0h RW	**RMM Regular Rule 3 (RMM_REG_R3):** Disable RMM unsafe read page hit block safe read and write page miss same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R3 and RMM_PRIO_R1.
9	0h RW	**RMM Regular Rule 2 (RMM_REG_R2):** Disable RMM unsafe read page empty block safe write page empty same rank.
8	0h RW	**RMM Regular Rule 1 (RMM_REG_R1):** Disable RMM unsafe read page hit block safe write page hit same rank.
7:4	0h RO	**Reserved (RSVD7_4):** Reserved.
3	0h RW	**RMM Priority Rule 4 (RMM_PRIO_R4):** Disable RMM unsafe critical read miss block read and write hit to same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R3. Priority rules 1, 3 and 4 should be enabled/disabled together.
2	0h RW	**RMM Priority Rule 3 (RMM_PRIO_R3):** Disable RMM unsafe critical read hit block read and write miss to same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R1. Priority rules 1, 3 and 4 should be enabled/disabled together.
1	0h RW	**RMM Priority Rule 2 (RMM_PRIO_R2):** Disable RMM CAS block rule.
0	0h RW	**RMM Priority Rule 1 (RMM_PRIO_R1):** Disable RMM unsafe top critical read miss block read and write hit same bank. Note: Priority rules 1, 3 and 4 should be enabled/disabled together.

5.5.37 DRAM Self-Refresh Command (D_CR_DRAM_SR_CMD)—Offset 1754h

Self refresh command register to allow sending WAKE and SUSPEND messages to D-Unit. (Only one bit can be set at a time). Posted writes to this register are not completed until hardware clears the field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD31_4):** Reserved.
3	0h RW/V	**SUSPENDP (SUSPENDP):** A SUSPENDP message will put the DRAM into self-refresh mode. The D-Unit will complete servicing outstanding memory requests and flush all queued Refresh commands to DRAM before putting the DRAM in self refresh mode. Finally, a PM message will be sent to the PHY. The bit is cleared by hardware after the PHY indicates the transition requested in the PM message has been completed. D-Unit will perform an MRW to MR17 with an opcode as defined by DPMC0.PASR before it places the DRAM into Self-Refresh.
2	0h RW/V	**SUSPEND (SUSPEND):** A SUSPEND message will put the DRAM into self-refresh mode. The D-Unit will complete servicing outstanding memory requests and flush all queued Refresh commands to DRAM before putting the DRAM in Self Refresh mode. Finally, a PM message will be sent to the PHY. The bit is cleared by hardware only after the PHY indicates the transition requested in the PM message has been completed. Note: When COLDWAKE is set prior of setting this bit the DRAM will not be placed in SR.
1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RW/V	**WAKE (WAKE):** Take PHY out of PM states and wakes the DRAM out of self refresh mode. The bit is cleared by hardware only when the DRAM has exited out of self refresh mode and is accessible. Note: When COLDWAKE is set prior of setting this bit the D-Unit will not send SR exit command and will not set the DCO.IC bit.

5.5.38 DQS Retraining Control (D_CR_DQS_RETRAINING_CTL)—Offset 1780h

LPDDR4 DQS Retraining control register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DQS Periodic Retraining Interval (DQS_RETRAIN_INT):** This sets the frequency by which the D-Unit initiates periodic retraining (in 1x NREFI).

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:4	0h RW	**DQS Oscillator Runtime (DQS_OSC_RT):** After D-Unit starts DQS oscillator, it must wait this amount of time before being able to read the value in MR18 and MR19 (in 16x DRAM clocks). Value in this register must be at least equal to DRAM's MR23 value. + tOSCO.
3:2	0h RO	**Reserved (RSVD3_2):** Reserved.
1	0h RW	**DQS Retrain SRX Exit (DQS_RETRAIN_SRX_EN):** Enable retraining on SR exit. This bit enables LPDDR4 DQS retraining on Self Refresh Exit. If disabled, D-Unit will not perform retraining on SR exit.
0	0h RW	**DQS Retrain Enable (DQS_RETRAIN_EN):** Periodic retraining enable: This bit enables periodic DQS retraining. If disabled, D-Unit will not perform retraining periodically. Note: Will be enabled only if DCO.IC is set and refreshes are enabled in DRF.MINREFRATE.

5.5.39 MR4 De-Swizzle Control (D_CR_MR4_DESWIZZLE)—Offset 1784h

Controls the data bits swizzling crossbar for MR4.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:28	0h RW	**MR4 Bit 2 Select 2nd Byte (MR4_BIT2_SEL2):** Selects bit 2 of MR4 data.
27	0h RO	**Reserved (RSVD27):** Reserved
26:24	0h RW	**MR4 Bit 1 Select 2nd Byte (MR4_BIT1_SEL2):** Selects bit 1 of MR4 data
23	0h RO	**Reserved (RSVD23):** Reserved
22:20	0h RW	**MR4 Bit 0 Select 2nd Byte (MR4_BIT0_SEL2):** Selects bit 0 of MR4 data.

Bit Range	Default & Access	Field Name (ID): Description
19:18	0h RO	**Reserved (RSVD19_18):** Reserved
17:16	0h RW	**MR4 Byte 2 Select (MR4_BYTE_SEL2):** Selects byte position of the MR4 data for second device.
15	0h RO	**Reserved (RSVD15):** Reserved
14:12	0h RW	**MR4 Bit 2 Select (MR4_BIT2_SEL):** Selects bit 2 of MR4 data.
11	0h RO	**Reserved (RSVD11):** Reserved.
10:8	0h RW	**MR4 Bit 1 Select (MR4_BIT1_SEL):** Selects bit 1 of MR4 data.
7	0h RO	**Reserved (RSVD7):** Reserved.
6:4	0h RW	**MR4 Bit 0 Select (MR4_BIT0_SEL):** Selects bit 0 of MR4 data.
3:2	0h RO	**Reserved (RSVD3_2):** Reserved.
1:0	0h RW	**MR4 Byte Select (MR4_BYTE_SEL):** Selects byte position of the MR4 data first device.

5.6 Registers Summary

Table 5-6. Summary of memss_regs Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1A00h	1A03h	DRAM Rank Population 0 (D_CR_DRP0)—Offset 1A00h	10000000h
1A08h	1A0Bh	DRAM Timing Register 0A (D_CR_DTR0A)—Offset 1A08h	210702CBh
1A0Ch	1A0Fh	DRAM Timing Register 1A (D_CR_DTR1A)—Offset 1A0Ch	30481218h
1A10h	1A13h	DRAM Timing Register 2A (D_CR_DTR2A)—Offset 1A10h	8C080C30h
1A14h	1A17h	DRAM Timing Register 3A (D_CR_DTR3A)—Offset 1A14h	3002EA28h
1A18h	1A1Bh	DRAM Timing Register 4A (D_CR_DTR4A)—Offset 1A18h	30209149h
1A1Ch	1A1Fh	DRAM Timing Register 5A (D_CR_DTR5A)—Offset 1A1Ch	304200C2h
1A20h	1A23h	DRAM Timing Register 6A (D_CR_DTR6A)—Offset 1A20h	20100000h
1A24h	1A27h	DRAM Timing Register 7A (D_CR_DTR7A)—Offset 1A24h	D060C06h
1A28h	1A2Bh	DRAM Timing Register 8A (D_CR_DTR8A)—Offset 1A28h	CC50A18h
1A2Ch	1A2Fh	D-Unit ODT Control Register A (D_CR_DOCRA)—Offset 1A2Ch	0h
1A30h	1A33h	D-Unit Power Management Control 0 (D_CR_DPMC0)—Offset 1A30h	0h
1A34h	1A37h	D-Unit Power Management Control 1 (D_CR_DPMC1)—Offset 1A34h	10000028h
1A38h	1A3Bh	DRAM Refresh Control (D_CR_DRFC)—Offset 1A38h	1750h
1A3Ch	1A3Fh	D-Unit Scheduler (D_CR_DSCH)—Offset 1A3Ch	3901C08h
1A40h	1A43h	DRAM Calibration Control (D_CR_DCAL)—Offset 1A40h	1057h
1A44h	1A47h	VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 1A4Ch	20000h

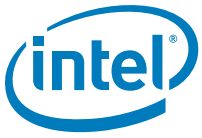


Table 5-6. Summary of memss_regs Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1A4Ch	1A4Fh	VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 1A4Ch	0h
1A50h	1A53h	Periodic DRAM Temperature Polling Control (TQ) (D_CR_TQCTL)—Offset 1A50h	6C000008h
1A54h	1A57h	TQ Temperature Offset Control (D_CR_TQOFFSET)—Offset 1A54h	0h
1A58h	1A5Bh	D-Unit Control Operations (D_CR_DCO)—Offset 1A58h	0h
1AA4h	1AA7h	Data Scrambler (D_CR_SCRAMCTRL)—Offset 1AA4h	0h
1AACh	1AAFh	Error Injection Address Register (D_CR_ERR_INJ)—Offset 1AACh	0h
1AB0h	1AB3h	Error Injection Control Register (D_CR_ERR_INJ_CTL)—Offset 1AB0h	0h
1AB4h	1AB7h	Error Log Register (D_CR_ERR_ECC_LOG)—Offset 1AB4h	0h
1ABCh	1ABFh	D-Unit Fuse Status (D_CR_DFUSESTAT)—Offset 1ABCh	0h
1B24h	1B27h	Major Mode Control (D_CR_MMC)—Offset 1B24h	2B01E518h
1B28h	1B2Bh	Major Mode RD/WR Counter (Set A and B) (D_CR_MMRDWR_AB)—Offset 1B28h	1F207C8h
1B2Ch	1B2Fh	Major Mode RD/WR Counter (Set C and D) (D_CR_MMRDWR_CD)—Offset 1B2Ch	1F207C8h
1B30h	1B33h	Access Class Initial Priority (D_CR_ACCIP)—Offset 1B30h	17C2h
1B34h	1B37h	Access Class 0 Priority Promotion Control (D_CR_RD_PROM0)—Offset 1B34h	1F52940h
1B38h	1B3Bh	Access Class 1 Priority Promotion Control (D_CR_RD_PROM1)—Offset 1B38h	14000000h
1B3Ch	1B3Fh	Access Class 2 Priority Promotion Control (D_CR_RD_PROM2)—Offset 1B3Ch	0h
1B40h	1B43h	Access Class 3 Priority Promotion Control (D_CR_RD_PROM3)—Offset 1B40h	1F29400h
1B44h	1B47h	Access Class 4 Priority Promotion Control (D_CR_RD_PROM4)—Offset 1B44h	1F5294Ah
1B48h	1B4Bh	Deadline Threshold (D_CR_DL_THRS)—Offset 1B48h	6h
1B4Ch	1B4Fh	Major Mode Blocking Rules Control (D_CR_MM_BLK)—Offset 1B4Ch	1800h
1B54h	1B57h	DRAM Self-Refresh Command (D_CR_DRAM_SR_CMD)—Offset 1B54h	0h
1B80h	1B83h	DQS Retraining Control (D_CR_DQS_RETRAINING_CTL)—Offset 1B80h	0h
1B84h	1B87h	MR4 De-Swizzle Control (D_CR_MR4_DESWIZZLE)—Offset 1B84h	0h

5.6.1 DRAM Rank Population 0 (D_CR_DRP0)—Offset 1A00h

Rank configuration register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**DRAM Device Per Rank (DRAMDEVICE_PR):** Specifies the number of DRAM devices that are ganged together to form a single rank. • 00: 1 DRAM device in each rank. • 01: 2 DRAM devices in each rank. • 10: 4 DRAM devices in each rank. • 11: 8 DRAM devices in each rank. Note: The actual number of devices is one more than the value programmed when ECC is enabled.
29:28	1h RW	**Address Decode (ADDRDEC):** Specifies the address mapping to be used: • 00: 1KB (A). • 01: 2KB (B). • 10: 4KB (C). • 11: Reserved.
27:25	0h RW	**Burst Length Mode (BLMODE):** • 000: Fixed BL8. • 001: Onthefly BL8. • 010: Fixed BL16. • 011: Onthefly BL16. • 100: Fixed BL32. • 101: Onthefly BL32. • 110-111: Reserved.
24:22	0h RW	**DRAM Type (DRAMTYPE):** • 000: DDR3L. • 001: LPDDR3. • 010: LPDDR4. • 011: Reserved. • 100: Reserved. • 101-111: Reserved. Note: The D-Unit should only use this field if allowed by fuse.
21	0h RW	**ECC Enable (ECCEN):** • 0: ECC is disabled. • 1: ECC is enabled. This bit determines if the D-Unit treats the PMI BE_ECC bits as ECC bits or Byte Enables. The D-Unit should not allow this bit to be set if ECC is disabled by fuse. This should only be used in configurations that support ECC (DDR3L).
20:19	0h RW	**CA Swizzle Type (CASWIZZLE):** • 00: uniDIMM/SODIMM. • 01: BGA. • 10: BGA mirrored (LPDDR3 Only). • 11: UDIMM (DDR3L Only).
18:16	0h RO	**Reserved (RSVD18_16):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Bank Address Hashing Enable (BAHEN):** See Address Mapping section for full description. • 0: Bank Address Hashing disabled. • 1: Bank Address Hashing enabled.
14	0h RW	**Rank Select Interleave Enable (RSIEN):** See Address Mapping section for full description. • 0: Rank Select Interleaving disabled. • 1: Rank Select Interleaving enabled.
13:9	0h RO	**Reserved (RSVD13_9):** Reserved.
8:6	0h RW	**DRAM Device Density (DDEN):** Density of the DRAM devices populated on Ranks 0 and 1. • 000: 4 Gb. • 001: 6 Gb. • 010: 8 Gb. • 011: 12 Gb. • 100: 16 Gb. • 101-111: Reserved. Note: For LPDDR4 this value is the die density.
5:4	0h RW	**DRAM Device Data Width (DWID):** Data width of the DRAM device populated on Ranks 0 and 1. • 00: x8. • 01: x16. • 10: x32. • 11: x64.
3	0h RO	**Reserved (RSVD3):** Reserved.
2	0h RW	**Dual Data Mode Enable (DDMEN):** • 0: PMI Dual Data Mode is disabled in D-Unit, full cacheline read and writes go through a single D-Unit. • 1: PMI Dual Data Mode is enabled, only half cacheline read/ writes go through a single D-Unit.
1	0h RW	**Rank Enable 1 (RKEN1):** Enable Rank 1: Must be set to 1 to enable use of this rank.
0	0h RW	**Rank Enable 0 (RKEN0):** Enable Rank 0: Must be set to 1 to enable use of this rank. Note: Setting this bit to 0 is not a functional mode.

5.6.2 DRAM Timing Register 0A (D_CR_DTR0A)—Offset 1A08h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 210702CBh

Bit Range	Default & Access	Field Name (ID): Description
31:25	10h RW	**Valid Clocks Before CKE High [tCKCKEH/tCSCKEH/tCKSRX] (TCKCKEH):** Number of valid clocks before CKE high (in DRAM clocks). • LPDDR4: The value in this register covers both tCKCKEH and tCSCKEH. • DDR3L/LPDDR3: The value covers tCKSRX which is defined as the number of valid DRAM clocks that have to toggle before the issuing of the Self Refresh Exit SRX. This value is also used if the clock frequency is changed or the clock is stopped or tristated during Power Down i.e. the number valid DRAM clocks that have to toggle before the issuing of the Power Down Exit PDX command. tCKCKEH can be used to compensate for clock stabilization delays in the motherboard. Note: D-unit hardware enforces minimum of two SPID clock before CKEH, any value in this register is the additional time.
24:21	8h RW	**Exit Self-Refresh to Valid Commands Requiring a Locked DLL Delay [tXSDLL] (TXSDLL):** D-Unit waits max(tXSR+tZQCL/tZQCS, tXSDLL) before allowing traffic to DRAM (in 64 x DRAM Clocks). LPDDR3/LPDDR4: tXSDLL = 0. DDR3L: tXSDLL = tDLLK = 512 Clocks = 8 x 64 DRAM Clocks. Note: In the equation above, tZQCL/tZQCS = 0 if no ZQ is performed on SR exit.
20:12	70h RW	**Exit Self-Refresh to Valid Command Delay [tXS/tXSR] (TXSR):** DDR3L: tXS - Delay between Self Refresh Exit SRX to any DRAM Command not requiring DLL Lock. LPDDR: tXSR - Delay between Self Refresh Exit SRX to any DRAM Command. (in DRAM clocks).
11:6	Bh RW	**Activate RAS to CAS Command Delay [tRCD] (TRCD):** Specifies the delay between a DRAM Activate command and a DRAM Read or Write command to the same bank (in DRAM clocks). Note: Derating adds 1.875ns to this timing.
5:0	Bh RW	**Precharge to Activate Command Delay of a Single Bank [tRPpb] (TRPPB):** Specifies the delay between a DRAM Precharge command and a DRAM Activate command to the same bank (in DRAM Clocks). Note : this CR should be constrained to a minimum of 4 in LPDDR3 and minimum of 8 in LPDDR4. Note: Derating adds 1.875ns to this timing.

5.6.3 DRAM Timing Register 1A (D_CR_DTR1A)—Offset 1A0Ch

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 30481218h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Exit Power Down to Next Command Delay [tXP] (TXP):** Specifies the delay from the DRAM Power Down Exit (PDX) command to any valid command (in DRAM clocks). Note: The value in this field must be programmed to tXPDLL when Slow Exit Mode Power-down is enabled for DDR3L.
26	0h RO	**Reserved (RSVD26):** Reserved.
25:14	120h RW	**ZQ (long) Calibration Time [tZQCL/tZQCAL] (TZQCL):** • LPDDR3/DDR3L: tZQCL/tZQoper: Specifies the delay between the DRAM ZQ Calibration Long (ZQCL) command and any DRAM command during normal operation. • LPDDR4: tZQCAL: ZQ Calibration time (in DRAM clocks). Note: This field defines the ZQ Calibration Long delay during normal operation. It is not the same as tZQinit which uses the same ZQCL command but the delay is longer. tZQinit applies only during poweron initialization of the DRAM devices and tZQoper applies during normal operation. BIOS executes the DRAM initialization sequence so it has to ensure tZQinit is met and not the D-Unit.
13:6	48h RW	**ZQ Short Calibration Time [tZQCS] (TZQCS):** ZQCS to any DRAM Command Delay: Specifies the delay between the DRAM ZQ Calibration Short (ZQCS) command and any DRAM command (in DRAM clocks). DDR3L and LPDDR3 only. LPDDR4 does not support ZQCS command
5:0	18h RW	**ZQ Latch Time [tZQLAT] (TZQLAT):** Specifies the delay between the DRAM ZQ Calibration Latch command and any DRAM command (in DRAM clocks). LPDDR4 only.Not used in DDR3L/LPDDR3.

5.6.4 DRAM Timing Register 2A (D_CR_DTR2A)—Offset 1A10h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8C080C30h

Bit Range	Default & Access	Field Name (ID): Description
31:23	118h RW	**All Bank Refresh Cycle Time [tRFCab] (NRFCAB):** Specifies the delay between the REFab command to the next valid command. (in DRAM clocks)

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	**Reserved (RSVD22_21):** Reserved.
20:17	4h RW	**CKE Minimum Pulse Width [tCKE] (TCKE):** Specifies the minimum time from CKEL to CKEH (in DRAM clocks).
16	0h RO	**Reserved (RSVD16):** Reserved.
15:0	C30h RW	**Refresh Interval Time [tREFI] (NREFI):** Specifies the average time between refresh commands. JEDEC Base Refresh Interval time (in DRAM clocks). Note: D-Unit will ignore the 2 LSBs of this field.

5.6.5 DRAM Timing Register 3A (D_CR_DTR3A)—Offset 1A14h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3002EA28h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Read to Precharge Delay [tRDPRE] (TRTP):** Specifies the minimum delay between the DRAM Read and Precharge commands to the same bank (in DRAM clocks). • LPDDR3 Equation: = BL/2 + tRTP - 4. • LPDDR4 Equation: = BL/2 + Max (8, tRTP) - 8. • DDR3L Equation: = tRTP.
26:20	0h RW	**CAS to CAS Command Delay Adder (TCCD_INC):** Specifies the number of clocks to be added to turnaround times (for Stretch Mode). It increases delay between Read to Read or Read to Write commands (in 4 x DRAM clocks).
19:13	17h RW	**Write to Precharge Command Delay [tWRPRE] (TWTP):** Specifies the minimum delay between the DRAM Write command and the Precharge command to the same bank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tWTP = BL/2 + WL + tWR + 1. • DDR3L Equation: tWTP = BL/2 + CWL + tWR.
12:11	1h RW	**DRAM Command Valid Duration (TCMD):** Specifies the number of DRAM clocks a command is held valid on the DRAM Address and Control buses. 1N is the DDR3 basic requirement. 2N is the extended mode for board signal integrity. • 0h: Reserved. • 1h: 1 DRAM Clock (1N). • 2h: 2 DRAM Clocks (2N). • 3h: Reserved. Note: DDR3L only. tCMD must be set to 1N for LPDDR3/LPDDR4.

Bit Range	Default & Access	Field Name (ID): Description
10:6	8h RW	**Write Latency [WL/CWL] (TCWL):** The delay between the internal write command and the availability of the first word of DRAM input data (in DRAM clocks).
5:0	28h RW	**Write CAS to Masked Write CAS Delay Same Bank (TWMWSB):** Specifies the minimum delay between DRAM Write command to Masked Write command to same bank (in DRAM clocks). • LPDDR4 Equation: tWMWSB = tCCDMW (BL16) or tCCDMW + 8 (BL32). Note: Masked Write operation in LPDDR4 is always BL16. D-Unit applies this timing for same rank as well as same bank.

5.6.6 DRAM Timing Register 4A (D_CR_DTR4A)—Offset 1A18h

Specifies DRAM timings parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 30209149h

Bit Range	Default & Access	Field Name (ID): Description
31:24	30h RW	**Four Bank Activate Window [tFAW] (TFAW):** A rolling timeframe in which a maximum of four Activate commands can be issued to the same rank. This is to limit the peak current draw from the DRAM devices (in DRAM clocks).
23:18	8h RW	**Write to Read DQ Delay Different Ranks (TWRDR):** Specifies the delay from the start of a Write data burst of one rank to the start of a Read data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tWRDR = WL + tDQSSmax + BL/2 + tWPST - (RL + tDQSCKmin - tRPRE). • LPDDR4 Equation: tWRDR = WL - RL + BL/2 + 4 - tDQSCKmin. • DDR3L Equation: tWRDR = CWL + tDQSSmax + BL/2 + tWPST - (CL + tDQSCKmin - tRPRE). Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj.
17:12	9h RW	**Read to Write DQ Delay Different Ranks (TRWDR):** Specifies the delay from the start of a Read data burst of one rank to the Start of a Write data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tRWDR = RL + tDQSCKmax + BL/2 + tRPST - (WL + tDQSSmin - tWPRE). • LPDDR4 Equation: tRWDR = RL + tDQSCKmax + BL/2 - (WL - 2). • DDR3L Equation: tRWDR = CL + tDQSCKmax + BL/2 + tRPST - (CWL + tDQSSmin - tWPRE). Note: For LPDDR3/4 using ODT, this latency may need to be adjusted by tODTon. Note: For DDR3L using ODT, this latency may need to be increased by one clock.

Bit Range	Default & Access	Field Name (ID): Description
11:6	5h RW	**Write to Write DQ Delay Different Ranks (TWWDR):** Specifies the delay from the start of a Write data burst of one rank to the start of a Write data burst of a different rank (in DRAM clocks). • LPDDR3 Equation: tWWDR = BL/2 + tDQSSmax - tDQSSmin + tWPRE. • LPDDR4 Equation: tWWDR = BL/2 + 4 - tDQSSmin. • DDR3L Equation: tWWDR = BL/2 + tDQSSmax - tDQSSmin + tWPRE. Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj.
5:0	9h RW	**Read to Read DQ Delay Different Ranks (TRRDR):** Specifies the delay from the start of a Read data burst of one rank to the Start of a Read data burst of a different rank (in DRAM clocks). • LPDDR3/4 Equation: tRRDR = BL/2 + tDQSCKmax - tDQSCKmin + tRPRE. • DDR3L Equation: tRRDR = BL/2 + tRPST + tDQSCKmax - tDQSCKmin + tRPRE + 1.

5.6.7 DRAM Timing Register 5A (D_CR_DTR5A)—Offset 1A1Ch

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 304200C2h

Bit Range	Default & Access	Field Name (ID): Description
31:27	6h RW	**Row Activation to Row Activation Delay [tRRD] (TRRD):** Specifies the minimum delay in DRAM clocks between two DRAM Activate commands to the same rank but different banks (tRC is the minimum delay between activations of the same bank). Note: Derating adds 1.875ns to this timing.
26	0h RO	**Reserved (RSVD26):** Reserved.
25:23	0h RW	**Derate Increment (TDERATE_INC):** Specifies the additional delay that is added to DRAM timing when indicated by MR4 status. (in DRAM clocks) LPDDR3/LPDDR4: Value is 1.875ns. Note: The value in this register is only added to these timing parameters: tRCD, tRAS, tRP and tRRD.
22:18	10h RW	**Write to Write DQ Delay Same Rank (TWWSR):** Specifies the delay from a DRAM Write to another Write command of the same rank (in DRAM clocks). LPDDR3/LPDDR4/DDR3L Equation: tRRSR = tCCD.

Bit Range	Default & Access	Field Name (ID): Description
17:13	10h RW	**Read to Read DQ Delay Same Rank (TRRSR):** Specifies the delay from a DRAM Read to another Read command of the same rank (in DRAM clocks). LPDDR3/LPDDR4/DDR3L Equation: tRRSR = tCCD.
12:6	3h RW	**Write to Read DQ Delay Same Rank (TWRSR):** Specifies the delay from a DRAM Read to Write command of the same rank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tWRSR = WL + tDQSSmax + BL/2 + tWTR. • DDR3L Equation: tWRSR = CWL + tDQSSmax + BL/2 + tWPST + tWTR.
5:0	2h RW	**Read to Write DQ Delay Same Rank (TRWSR):** Specifies the delay from a DRAM Read to a Write command of the same rank (in DRAM clocks). • LPDDR3/LPDDR4 Equation: tRWSR = RL + tDQSCKmax + BL/2 - WL + tWPRE. • DDR3L Equation: tRWSR = CL + tDQSCKmax + BL/2 + tRPST - (CWL +tDQSSmin - tWPRE). Note: For LPDDR3/4 using ODT, this latency may need to be increased by tODToffadj. Note: For DDR3L using ODT, this latency may need to be increased by one clock.

5.6.8 DRAM Timing Register 6A (D_CR_DTR6A)—Offset 1A20h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 20100000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	20h RW	**Opportunistic Refresh Idle Timer (OREFDLY):** Rank idle period that defines an opportunity for refresh (in DRAM clocks).
23:19	2h RW	**Valid Clocks After CKE Low [tCKELCK/tCKELCS/tCPDED/tCKSRE] (TCKCKEL):** Specifies the amount of time that DRAM clocks need to toggle after CKE goes low (in DRAM Clocks). • For LPDDR3, this covers tCPDED. • For LPDDR4, this covers both tCKELCK and tCKELCS. • For DDR3L, this is tCKSRE. Note: D-Unit hardware enforces minimum of one SPID clocks after CKEL, any value in this register is the additional time.
18:15	0h RW	**Maintenance Operation Delay (MNTDLY):** When a critical read request is pending in RPQ and a maintenance operation (MRR, ZQCal, Ref, etc, panic refresh is an exception to this delay.) needs to be performed, D-Unit waits this amount of time before performing the maintenance operation to allow for some high priority requests to be issued (in 4x SPID clocks).

Bit Range	Default & Access	Field Name (ID): Description
14:8	0h RW	**Mode Register Read to Any Command Delay (TPSTMRRBLK):** Specifies the quiet time after issuing MRR command (in DRAM Clocks). Note: D-Unit treats MRR as a read and always applies relevant turnaround times, any value programmed in this CR must be greater than those turnaround times for D-Unit to enforce any additional time from MRR to the next read/write.
7	0h RO	**Reserved (RSVD7):** Reserved.
6:0	0h RW	**Any Command to Mode Register Read/Write Delay (TPREMRBLK):** Specifies the quiet time before issuing MRR/MRW command. (in DRAM clocks). Note: D-Unit treats MRR as a read and always applies relevant turnaround times, any value programmed in this CR must be greater than those turnaround times for D-Unit to enforce any additional time from previous read/writes.

5.6.9 DRAM Timing Register 7A (D_CR_DTR7A)—Offset 1A24h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: D060C06h

Bit Range	Default & Access	Field Name (ID): Description
31:26	3h RW	**All Bank Precharge to Activate Command Delay [tRPab] (TRPAB):** Specifies the delay between a DRAM Precharge All Bank command and a DRAM Activate command (in DRAM Clocks). Note: This CR should be constrained to a minimum of 4 in LP3 and minimum of 8 in LP4. Note: Derating adds 1.875ns to this timing. • For LPDDR, tRPpb = tRP, tRPab = tRP + 3ns. • For DDR3L 8ch tRPpb = tRPab = tRP.
25:23	2h RW	**Mode Register Write to any Command Delay [tMRD/tMRW] (TPSTMRWBLK):** Specifies the quiet time after issuing MRW command (in 8 x DRAM clocks). Note: This time covers for both tMRD and tMRW.
22:16	6h RW	**Write Command to Power Down Delay [tWRPDEN] (TWRPDEN):** Specifies the minimum time between a write command to PowerDown command (in DRAM clocks). Must be at least equal to tWR + tCCD + tWL + 2.
15:9	6h RW	**Read Command to Power Down Delay [tRDPDEN] (TRDPDEN):** Specifies the minimum time between a read command to PowerDown command (in DRAM clocks). Must be at least equal to CL/RL + tDQSCKmax + tCCD + tRPST.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RO	**Reserved (RSVD8_7):** Reserved.
6:0	6h RW	**Row Activation Period [tRAS] (TRAS):** Specifies the minimum delay between the DRAM Activate and Precharge commands to the same bank (in DRAM clocks). Note: Derating adds 1.875ns to this timing.

5.6.10 DRAM Timing Register 8A (D_CR_DTR8A)—Offset 1A28h

Specifies DRAM timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: CC50A18h

Bit Range	Default & Access	Field Name (ID): Description
31:26	3h RW	**Minimum Self-Refresh Time [tSR/tCKESR] (TCKESR):** Specifies the minimum time that DRAM should remain in SR (in DRAM clocks).
25:21	6h RW	**Minimum Low Power Mode Residency (LPMDRES):** Specifies the minimum time that PHY should remain in LPMode (in DRAM clocks).
20:15	Ah RW	**Low Power Mode Exit to Clock Enable Delay (LPMDTOCKEDLY):** Specifies the minimum time between the LP Mode exit to the CK stop/tristate deassertion and powerdown exit (in DRAM clocks). Note: Must be equal to t_idle_latency and less than 0x3C.
14:8	Ah RW	**Clock Stop to Low Power Mode Delay (CKETOLPMDDLY):** Specifies the time between CK stop/tristate to the Low Power Mode entry. This timing parameter is used to delay Low Power Mode entry (in DRAM clocks). Note: Must be at least equal to t_idle_length parameter and less than 0x7C.
7:0	18h RW	**Power Down Idle Timer (PWDDLY):** This is a non-JEDEC timing parameter used to delay powerdown entry (in DRAM clocks).

5.6.11 D-Unit ODT Control Register A (D_CR_DOCRA)—Offset 1A2Ch

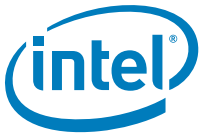
Specifies the parameters to control DRAM ODT.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29	0h RW	**Rank 1 Read ODT Control (R1RDODTCTL):** Specifies the behavior of ODT signals when a Read command is issued to Rank 1. 0 - Read ODT is disabled for Rank 1 1 - Assert ODT to for Rank 0 (non-targeted Rank) Note: This register should be set to 0 for LPDDR3 devices
28	0h RW	**Rank 0 Read ODT Control (R0RDODTCTL):** Specifies the behavior of ODT signals when a Read command is issued to Rank 0. 0 - Read ODT is disabled for Rank 0 1 - Assert ODT to for Rank 1 (non-targeted Rank) Note: This register is reserved for LPDDR3 devices
27:26	0h RW	**Rank 1 Write ODT Control (R1WRODTCTL):** Specifies the behavior of ODT signals when a Write command is issued to Rank 1. 00 - Write ODT is disabled 01 - Assert ODT to Rank 0 (non-targeted Rank) 10 - Assert ODT to Rank 1 (targeted Rank) 11 - Assert ODT to Rank 0 and Rank 1 Note: 10 and 11 are reserved values for LPDDR3
25:24	0h RW	**Rank 0 Write ODT Control (R0WRODTCTL):** Specifies the behavior of ODT signals when a Write command is issued to Rank 0. 00 - Write ODT is disabled 01 - Assert ODT to Rank 0 (targeted Rank) 10 - Assert ODT to Rank 1 (non-targeted Rank) 11 - Assert ODT to Rank 0 and Rank 1 Note: 10 and 11 are reserved values for LPDDR3
23:18	0h RO	**Reserved (RSVD23_18):** Reserved.
17:14	0h RW	**Read ODT assertion to de-assertion delay (DDR3L Only) (RDODTSTOP):** Specifies Read ODT assertion to ODT de-assert delay (in DRAM clocks). DDR3L Equation: RDODTSTOP = DOCRx.WRODTSTOP (subtract 1 if DOCRx.WRODTSTART = 1 in 2N mode).
13	0h RO	**Reserved (RSVD13):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
12:9	0h RW	**Read command to ODT assertion delay (DDR3L Only) (RDODTSTART):** Specifies Read ODT assertion delay after Read Command (in DRAM clocks). DDR3L Equation: RDODTSTART = CL CWL (add 1 if DOCRx.WRODTSTART = 0 in 2N mode). The max value for this CR is 0xE
8:5	0h RW	**Write ODT Assertion to De-assertion Delay (WRODTSTOP):** Specifies number of clocks after ODT assertion that D-Unit deasserts ODT signal (in DRAM clocks). LPDDR3 Equation: WRODTSTOP = RU(tODTon(max)/tCK) + RU((tDQSSmax+tWPST)/tCK) + BL/2 - RD(tODToffmin/tCK) DDR3L Equation: WRODTSTOP >= 6
4	0h RO	**Reserved (RSVD4):** Reserved.
3:0	0h RW	**Write command to ODT assertion delay (WRODTSTART):** Specifies number of clocks after Write command that D-Unit asserts ODT signal (in DRAM clocks). LPDDR3 Equation: WRODTSTART = WL - RU(tODTon(max)/tCK) DDR3L Equation: WRODTSTART = 0 Note: DDR3 spec requires ODT to be asserted high when the DRAM Write command is issued. In DDR3L 2N mode the value can be set to 0 to assert ODT one DRAM clock earlier than the Write Command (WR) or set to 1 to assert at the same clock as command (CS assertion). The max value for this CR is 0xE

5.6.12 D-Unit Power Management Control 0 (D_CR_DPMC0)—Offset 1A30h

Specifies the parameters to control D-Unit power management features.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD31_29):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28:24	0h RW	**SUSPEND/SUSPENDP Power Management Message Opcode (SUSPMOP):** DDRIO PHY Power Mode Opcode: After the D-Unit has placed the DRAM devices in Self Refresh/PASR mode as the result of a SUSPEND/SUSPENDP message, it sends this 5-bit value to the DDRIO PHY to tell it which power saving mode it should enter. Changing this register value while in SUSPEND will have no effect. Note: This opcode cannot be a PM state where it disables PHY PLLs i.e PM7 in LPDDR PHY.
23	0h RO	**Reserved (RSVD23):** Reserved.
22	0h RW	**PM Message Wait for Clock Gate Enable (SRPMCLKW):** Specifies when it is safe to send PM message to the PHY. When enabled, D-Unit waits for SPID Clock to deassert before sending a PM message on SR entry. • 0: D-Unit will not wait for SPID_clk to deassert before sending the PM message to PHY. • 1: D-Unit will wait for SPID_clk to deassert before sending PM message to the PHY. Note: The value must be 1 when DYNPMOP = 7h.
21:17	0h RW	**Dynamic Self-Refresh Power Management Message Opcode (DYNPMOP):** DDRIO PHY Power Mode Opcode: After the D-Unit has placed the DRAM devices in Self Refresh mode as the result of a Dynamic Self-Refresh, it sends this 5bit value to the DDRIO PHY to tell it which power saving mode it should enter. Changing this register value while in self-refresh will only change the PM state for the next entry in DynSR.
16	0h RW	**Dynamic Self-Refresh Enable (DYNSREN):** When set to 1, the D-Unit will automatically control DRAM Self Refresh entry and exit based on interface state and requests in pending queues. When there is no pending request in the queues and PMI is idle, then the D-Unit will place the DRAM devices in Self Refresh mode. The DRAM devices will be brought out of Self-Refresh when idle conditions don't hold.
15:0	0h RW	**Self-Refresh Entry Delay (SREDLY):** Specifies the minimum time the D-Unit will wait before it enters Dynamic Self-Refresh mode when idle (in 16x DRAM Clocks). Note: The value in this field needs to be minimum of 4 in functional mode and minimum of 50 in PSMI mode.

5.6.13 D-Unit Power Management Control 1 (D_CR_DPMC1)—Offset 1A34h

Specifies the parameters to control D-Unit power management features.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10000028h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29	0h RW	**D-Unit Repeaters Clock Gate Disable (RPTCLKGTDIS):** Setting this bit to 0 allows majority of the repeaters between D-Unit and PHY to clock gate when there is no activity in order to save power. 0 - Enable Repeaters clock gating, 1 - Disable Repeaters clock gating. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.
28	1h RW	**IOSF-SB End Point Clock Gate Disable (SBEPCLKGTDIS):** Setting this bit to 0 enables the clock gating of IOSF-SB End Points in D-Unit and CPGC when there is no IOSF-SB activity in order to save power. 0 - Enable IOSF-SB EP clock gating, 1 - Disable IOSF-SB clock gating. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.
27	0h RW	**Local Clock Gate Disable (CLKGTDIS):** Setting this bit to 0 allows the majority of the D-Unit clocks to be gated off when there is no activity in order to save power. When set to 1, D-Unit clockgating is disabled. • 0: Enable. • 1: Disable. Note: This is a de-feature bit and should be set to 0 for normal operation. Note: The value should only change after DRAM Timing Registers (DTR) are programmed.
26	0h RW	**Chip Select Tristate Enable (CSTRIST):** • 0: The DRAM CS pins associated with the enabled ranks are never tristated. • 1: The DRAM CS pins are tristated when DRAM clock is stopped or tristated. Note: CS is not tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1).
25:24	0h RW	**Command/Address Tristate (CMDTRIST):** • 00: The DRAM CA pins are never tristated. • 01: The DRAM CA pins are only tristated when all enabled CKE pins are low. • 10: The DRAM CA pins are tristated when not driving a valid command. • 11: Reserved
23:16	0h RW	**Partial Array Self-Refresh Segment Mask (PASR):** This is the Segment Mask used for the MRW to enable PASR during SUSPENDP (Partial Array Self Refresh entry).

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Page Close Timeout Period (PCLSTO):** Specifies the time from the last access of a DRAM page until that page is scheduled to close by sending a Precharge command to DRAM (in 16 x DRAM clocks).
7	0h RW	**Page Close Timeout Disable (PCLSTODIS):** When disabled, D-Unit will not close the DRAM page when idle. • 0: Enable page close timer. • 1: Disable page close timer (Used during DRAM init and DDRIO training).
6	0h RO	**Reserved (RSVD6):** Reserved.
5	1h RW	**ODT Tristate Enable (ODTTRIST):** • 0: The DRAM ODT pins associated with the enabled ranks are never tristated. • 1: DRAMs ODT pins are tristated when DRAM clock is stopped or tristated. Note: ODT is not tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1)
4:3	1h RW	**Clock Stop/Tristate Enable (ENCKSTP):** Enable/Disable CK Stop/Tristate During Power down. • 00: Disable CK Stop/Tristate During Power down. • 01: Enable CK Stop During Power down. • 10: Enable CK Tristate During Power down. • 11: Reserved Note: CK is not stopped or tristated when global tristate flow is disabled (DCBR.TRISTDIS = 1).
2:1	0h RW	**Low Power Mode Opcode (LPMODEOP):** D-Unit will send the value in this register after it has entered Powerdown Mode and has stopped/tristated the clock. 00: Disable LPMode. Note: LPMODE entry is not possible when global tristate flow is disabled (DCBR.TRISTDIS = 1).
0	0h RW	**Disable Power Down (DISPWRDN):** Setting this bit to 1 disables dynamic control of DRAM Power-Down entry and exit by keeping the CKE pins driven high. BIOS may set it to 1 during DRAM initialization and DDRIO training. This bit should be set to 0 for normal operation. • 0: The D-Unit dynamically controls the CKE pins to place the DRAM devices in Power Down mode and bring them out of Power Down mode. • 1: The D-Unit constantly drives the CKE pins high to keep the DRAM devices from entering Power Down mode when ranks are idle. Note: This bit is overridden if CKEMODE = 1. This bit does not control CKE behavior on SR entry/exit.

5.6.14 DRAM Refresh Control (D_CR_DRFC)—Offset 1A38h

Specifies the parameters to control scheduling of refresh commands.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1750h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD31_22):** Reserved.
21	0h RW	**Disable Refresh Debt Clear (DISREFDBTCLR):** When set, D-Unit will not clear refresh debt before Self Refresh SR Entry: • 0: D-Unit sends all postponed REF commands to DRAM before it enters Self Refresh. • 1: D-Unit enters SR without clearing the Refresh Debt (for Debug only).
20	0h RW	**Refresh Skew Disable (REFSKWDIS):** Disables Skewing of Refresh Counting between Ranks. Each rank has its own refresh counter. By default incrementing these refresh counters are skewed by 1/2 the tREFI period. Setting this bit to a 1 disables this feature and all refresh counters will increment at the same time per tREFI period. Skewing the tREFI counters can improve performance since traffic to all ranks does not have to be blocked to perform refresh. • 0: Incrementing the refresh counters are skewed by 1/2 tREFI period. • 1: All refresh counters will increment at the same time per tREFI period.
19:18	0h RO	**Reserved (RSVD19_18):** Reserved.
17:16	0h RO	**Reserved (RSVD17_16):** Reserved.
15	0h RW	**Extra Refresh Debit (EXTRAREFDBT):** When set to 1, D-Unit adds one extra refresh debit (for a total of two) on Self-refresh exit.
14:12	1h RW	**Minimum Refresh Rate (MINREFRATE):** Ensures that refresh rate never drops below a certain limit regardless of TQ polling. • 000: Disable tREFI counter and stop issuing refresh commands. • 001: 0.25x refresh rate (i.e. 4x tREFI same as no limit). • 010: 0.5x refresh rate (i.e. 2x tREFI). • 011: 1x refresh rate (i.e. 1x tREFI). • 100: 2x refresh rate (i.e. 0.5x tREFI). • 101: 4x refresh rate (i.e. 0.25x tREFI). • 110: 4x refresh rate with derating forced on i.e. 0.25x tREFI. • 111: Reserved.
11:8	7h RW	**Refresh Panic Watermark (REFWMPNC):** When the Refresh counter per rank is greater than this value, the D-Unit will send a REF command to the rank regardless of pending requests. Note: REFWMPNC must be greater than or equal to REFWMHI and greater than 2, Max Value must be less than 8 to not violate 9xtREFI JEDEC requirement.

Bit Range	Default & Access	Field Name (ID): Description
7:4	5h RW	**Refresh High Watermark (REFWMHI):** When the Refresh counter per rank is greater than this value, the D-Unit will send a REF command to the rank if there is no critical priority requests in the pending queues. Note: Value must be greater or equal to 1 and less than or equal to REFWMPNC.
3:1	0h RO	**Reserved (RSVD3_1):** Reserved.
0	0h RW	**Opportunistic Refresh Disable (OREFDIS):** Disable opportunistic scheduling of refresh. • 0: D-Unit will send a REF command only if there is no pending request to that rank. • 1: D-Unit will not send any opportunistic refreshes. Refresh commands are only sent when the refresh counter is greater than REFWMHI. Note: When set, DISREFDBTCLR must also be set to be able to enter SR.

5.6.15 D-Unit Scheduler (D_CR_DSCH)—Offset 1A3Ch

Specifies parameters to control scheduling of commands to DRAM.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3901C08h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:29	0h RW	**BGF Early Read Data Valid (BGF_EARLY_RDDATA_VALID):** Specifies the number of clocks the D-Unit sends the read data valid through the BGF earlier as compared to the data. • 00: Always write read valid in same SPID clock as data. • 01: Always write read valid one SPID clock before data. • 10: Write read valid up to 2 SPID clocks before data. • 11: Reserved
28:27	0h RW	**SPID Early Read Data Valid (SPID_EARLY_RDDATA_VALID):** Specifies the delay in SPID clocks from RDDATA_VALID assertion to actual data on SPID. The value should match what is programmed in DDRIO (PHY).
26:21	1Ch RW	**Write Pending Queue Count (WPQCOUNT):** Used to limit the number of available slots in Write Pending Queue/ Write Data Buffer. WPQCOUNT will only recognize changes when PMI ISM is not active.

Bit Range	Default & Access	Field Name (ID): Description
20:16	10h RW	**Read Pending Queue Count (RPQCOUNT):** Used to limit the number of entries in Read Pending Queue. RPQCOUNT will only recognize changes when PMI ISM is not active.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:10	7h RW	**Read Return Data Additional Credits (BLKRDBF_ADD_RDDATA_CR):** Number of additional full cacheline (64B) read data return credits exposed to D-Unit when BLKRDBF is set. Note: The value in this field has no effect on Read return credits when BLKRDBF is not set.
9:8	0h RW	**In-Order Mode (INORDERMODE):** • 0h: In order mode disabled: Commands are sent out of order. • 1h: Partial in order mode: Read and Write CAS commands are sent in the order they were recieved. ACT and PRE can go out of order. • 2h: Full in order mode serialized test: All DRAM commands CAS ACT PRE associated with a PMI request are issued to DDR before any DRAM commands for a subsequent PMI request. • 3h: Reserved. In order modes should be enabled during init/training/CPGC testing. Should never be changed while the D-Unit queues are nonempty.
7	0h RW	**Idle Bypass Mode Enable (BYPASSEN):** Reserved.
6	0h RW	**Block When RDB Full (BLKRDBF):** When set D-Unit stops scheduling new read commands to DRAM when the read data buffer (RDB) is full.
5:4	0h RW	**Stretch Mode (STRETCHMODE):** When stretch mode is enabled, commands are initiated only on Phase 0 of SPIDClk. • 00: Stretch mode is disabled. • 01: Commands are initiated on Phase 0 of every SPID clocks. • 10: Commands are initiated on Phase 0 of even SPID clocks. • 11: Commands are initiated on Phase 0 of odd SPID clocks.
3:0	8h RW	**Masked Write Turnaround Delta (TMWR_TA_DELTA):** The value in this register is subtracted from Masked Write to Read, Masked Write to Write and Masked Write to Masked Write turnaround times to account for half BL MWr commands in LPDDR4. • LPDDR4: = MWr tCCD = MWr BL/2 = 8.

5.6.16 DRAM Calibration Control (D_CR_DCAL)—Offset 1A40h

Specifies parameters to control ZQ Calibration.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1057h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ZQ Calibration Type (ZQCALTYPE):** Determines whether the ZQ Calibration is a long or short calibration command (due to ZQCALSTRT). 0: Short calibration (ZQCS). 1: Long calibration (ZQCL).
30	0h RW/V	**ZQ Calibration Start Rank 1 (ZQCALSTRTR1):** Set this bit to 1 to start the ZQ calibration sequence on Rank 1. This bit will remain a 1 until the ZQ calibration is complete for rank 1, then it will return to 0. 0: ZQ calibration is done. 1: ZQ calibration has started and is in progress.
29	0h RW/V	**ZQ Calibration Start Rank 0 (ZQCALSTRTR0):** Set this bit to 1 to start the ZQ calibration sequence on Rank 0. This bit will remain a 1 until the ZQ calibration is complete for rank 0, then it will return to 0. 0: ZQ calibration is done. 1: ZQ calibration has started and is in progress.
28:23	0h RO	**Reserved (RSVD28_23):** Reserved.
22:21	0h RW	**Self-Refresh Exit ZQ Calibration Control (SRXZQC):** • 00: On DynSR exit ZQ timer determines the ZQ type. When the state is lost (i.e due to AutoPG/S0ix) ZQCL is always performed. • 01: Always perform ZQCL after self refresh exit, in LPDDR4, ZQ with traffic blocked. • 10: Always perform ZQCS on SR exit. For LPDDR4, ZQ while traffic is allowed. • 11: No ZQCL commands are sent (it disables ZQCAL commands on SR exit).
20:18	0h RO	**Reserved (RSVD20_18):** Reserved.
17	0h RW	**ZQ Calibration Mode (ZQCLMODE):** Specifies how ZQCal commands are sent to different ranks. • 0: ZQCal commands are sent in parallel to all ranks. • 1: ZQCal commands are sent serially to each rank.
16	0h RW	**Periodic ZQ Calibration Disable (ZQCDIS):** • 0: Periodic ZQ Calibration is Enabled. • 1: Disable periodic ZQ Calibration.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:0	1057h RW	**ZQ Calibration Interval (ZQINT):** Specifies the time interval between two ZQCS (LPDDR3) or ZQ Start (LPDDR4) commands to a DRAM device. (in RTC 32.8KHz clocks)

5.6.17 VNN Scaling Timer Control (D_CR_VNNTIMER)—Offset 1A4Ch

Specifies parameters for VNN Scaling Timer in D-Unit. The values in this register will be set by P-code during VNN scaling period.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VNN Scaling Timer Enable (VNN_TIMER_EN):** • 0: The D-Unit VNN Scaling Timer is disabled. • 1: The D-Unit VNN Scaling Timer is enabled.
30:12	0h RO	**Reserved (RSVD30_12):** Reserved.
11:0	0h RW	**VNN Timer Time (VNN_TIMER_TIME):** The final timer value (in 16 x DRAM clocks).

5.6.18 Periodic DRAM Temperature Polling Control (TQ) (D_CR_TQCTL)—Offset 1A50h

Specifies the control for periodic temperature monitoring and control of DRAM device.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6C000008h

Bit Range	Default & Access	Field Name (ID): Description
31:29	3h RW/V	**TQ Data Rank 1 (TQDATAR1):** If Rank 1 is disabled, this value will remain zero. This field contains the data of the last DRAM Mode Register Read to MR4 MRR issued. It is overwritten with each command.
28:26	3h RW/V	**TQ Data Rank 0 (TQDATAR0):** This field contains the data of the last DRAM Mode Register Read to MR4 MRR issued. It is overwritten with each command.
25:22	0h RO	**Reserved (RSVD25_22):** Reserved.
21:8	0h RW	**TQ Poll Period (TQPOLLPER):** This sets the frequency by which the D-Unit polls the DRAM mode register MR4 to determine required refresh rate (in 4x tREFI units).

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved (RSVD7_5):** Reserved.
4	0h RW	**Self Refresh Temperature Range Enable (DDR3 Only) (SRTEN):** When set, before every Self refresh entry, D-Unit writes a 1 to bit 7 of TQOFFSET.MR_VALUE when TQDATA for that rank indicates a value higher then 0x3, and writes a 0 to that bit otherwise. The new MR_VALUE is then written into MR2 of DDR3 for each enabled rank.
3	1h RW	**Enable Dynamic Timing Derating (ENDERATE):** When set to 1, the Dynamic Timing Derating is enabled. When the D-Unit determines (via TQ polling) that the DRAM requires timing derating in addition to refresh interval adjustment, the D-Unit will automatically adjust the relevant timing parameters.
2	0h RW	**Enable TQ Data Push (TQDATAPUSHEN):** When set to 1, D-Unit pushes the data form the last MR4 read to a punit register.
1	0h RW	**Enable TQ Poll on Self-Refresh Exit (TQPOLLSREN):** This bit enables MR4 read on Self Refresh Exit. If disabled, D-Unit will not read MR4 value on Self-Refresh exit.
0	0h RW	**Enable Periodic TQ Poll (TQPOLLEN):** This bit enables periodic TQ Poll. If disabled, D-Unit will not read MR4 value periodically. Note: Will be enabled only if refreshes are enabled.

5.6.19 TQ Temperature Offset Control (D_CR_TQOFFSET)—Offset 1A54h

Specifies temperature offset and refresh rate adjustments requested by software.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:16	0h RW	**MR Value (MR_VALUE):** MR2 Shadow Register (DDR3L Only): BIOS writes the correct value of MR2 register in DDR3L into this field at boot time. D-Unit modifies one bit and rewrites the MR2 into DDR3L DRAM before SR entry.
15:11	0h RO	**Reserved (RSVD15_11):** Reserved
10:8	0h RW	**MR4 Adder (MR4_ADDER):** D-Unit adds the value of this field to TQDATA read from MR4 the resulting value is used to control refresh rate and AC timing derating.

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved (RSVD7_3):** Reserved.
2	0h RW/V	**MR3 Offset Update (MR3_OFFSET_UPDATE):** When set, D-Unit writes the merged value of MR3_VALUE and MR3_THERM_OFFSET into MR3 of DRAM. D-Unit clears this bit once the value is written.
1:0	0h RW	**MR3 Thermal Offset (MR3_THERM_OFFSET):** Reserved.

5.6.20 D-Unit Control Operations (D_CR_DCO)—Offset 1A58h

Specifies D-Unit initialization and control operation.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Initialization Complete (IC):** Indicates that initialization of the D-Unit has been completed. Memory accesses are permitted and maintenance operation begins. Until this bit is set to a 1, the memory controller will not accept DRAM requests from the Bunit/ GSA/2LM (PMI ISMs will not leave idle). Note: Set this bit to 1 only when all other D-Unit registers have been configured. Usually set at the last configuration step by BIOS on cold/warm reset. D-Unit hardware sets this bit on SR exit.
30	0h RO/V	**DDRIO PHY Initialization Complete (DIOIC):** Status indication that the DDRIO PHY initialization is complete reflects the status spid_init_complete signal.
29	0h RO	**Reserved (RSVD29):** Reserved.
28	0h RW	**PMI Control Select (PMICTL):** • 0: D-Unit PMI is connected to Bunit/GSA/2LM. • 1: D-Unit PMI is connected to CPGC. Note: D_CR_DSCH_BYPASSEN must be set to 0 in CPGC mode. Note: PMI must be idle and D-Unit BGF_RUN = 0 before changing the value in this register.
27:8	0h RO	**Reserved (RSVD27_8):** Reserved.
7:4	0h RO	**Reserved (RSVD7_4):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Enable PSMI Mode (PSMIEN):** When enabled, D-Unit will synchronize clock crossing signals. • 0: PSMI Mode is disabled. • 1: PSMI Mode is enabled. Note: Change only allowed when D-Unit is idle.
2	0h RW	**Maintenance Reset (MNTRST):** Writing a 1 to this field resets all maintenance timers. Clears all states and also clears refresh debt queues. This bit needs to be cleared by software after at least 3 SPID clocks.
1	0h RW	**Enable Maintenance Operations (MNTEN):** Setting this field to 1 enables all maintenance operations. When DCO.IC is set, the maintenance operations are enabled irrespective of the value of this field.
0	0h RO	**Reserved (RSVD0):** Reserved.

5.6.21 Data Scrambler (D_CR_SCRAMCTRL)—Offset 1AA4h

Specifies parameters to control data scrambling in D-Unit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Data Scrambler (SCRM_EN):** When set to 1, data scrambling is enabled. When set to 0, data scrambling is disabled. Should be set before D_CR_BGF_CTL_BGF_RUN is set to 1.
30	0h RO	**Reserved (RSVD30):** Reserved.
29:28	0h RW	**Scrambler Clock Gate Select (CLOCKGATE):** This field controls how the scrambler output code is clock gated to reduce power. • 00: Clock gate disabled. • 01: Clock Gate every 2 cycle. • 10: Clock Gate every 3 cycle. • 11: Clock Gate every 4 cycle.
27:16	0h RO	**Reserved (RSVD27_16):** Reserved.
15:0	0h RW	**Scrambling Key (KEY):** Sets the key for the scrambler. The key should be a random value that is set following each cold boot.

5.6.22 Error Injection Address Register (D_CR_ERR_INJ)—Offset 1AACh

Contains the target address for ECC error injection.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:1	0h RW	**Error Injection Target Address (ADDRESS):** Specifies the PMI address of the write transaction to be injected with the error. Only applicable to Write transactions. Read/under-fill read of the partial write operation is not affected.
0	0h RO	**Reserved (RSVD0):** Reserved.

5.6.23 Error Injection Control Register (D_CR_ERR_INJ_CTL)—Offset 1AB0h

Controls injecting correctable or uncorrectable errors into the write requests specified by target address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD31_4):** Reserved
3	0h RW	**Error Injection Type Higher 32B (SEL_HI):** If enabled, the error injection is continuously armed for ERR_INJ.ADDR 32B write address matching until it is cleared. • 00: No error injection. • 01: Uncorrectable Error (UE) is armed for write address matching to inject UE by using the same poisoning scheme, i.e. inverting corresponding write ECC[6:0] on QW0 of the 32B data. • 10: Correctable Error (CE) is armed for write address matching to inject CE by inverting corresponding write ECC[0] on QW0 of the 32B data. • 11: Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Error Injection Enable Higher 32B (EN_HI):** When set the error injection is continuously armed for higher 32B of D_CR_ERR_INJ_ADDR write address matching until it is cleared.
1	0h RW	**Error Injection Type Lower 32B (SEL_LO):** 0 - Uncorrectable Error (UE) is armed for write address matching to inject UE by using the same poisoning scheme, i.e. inverting corresponding write ECC[6:0] on every QW of the 32B data. 1 - Correctable Error (CE) is armed for write address matching to inject CE by inverting corresponding write ECC[0] on every QW of the 32B data.
0	0h RW	**Error Injection Enable Lower 32B (EN_LO):** When set, the error injection is continuously armed for lower 32B of D_CR_ERR_INJ_ADDR write address matching until it is cleared.

5.6.24 Error Log Register (D_CR_ERR_ECC_LOG)—Offset 1AB4h

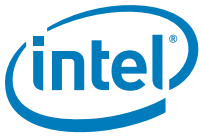
Detected ECC errors are captured in this register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Clear (CLEAR):** Setting this bit to one clears all fields in this register, including itself.
30:29	0h RW	**PMI VISA Byte Select (ECC_VISA):** Select ECC or PMI byte on VISA : • 00: ECC byte, • 01: PMI Data Byte [7:0], • 10: PMI Data Byte [63:56], • 11: PMI Data Byte [255:248]
28	0h RW/V	**Correctable Single-bit Error (CERR):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. A multiple bit error that occurs after this bit is set will override the address/error syndrome information.
27	0h RW/V	**Uncorrectable Multiple-bit Error (MERR):** This bit is set when an uncorrectable multiple-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked until this bit is cleared.



Bit Range	Default & Access	Field Name (ID): Description
26:25	0h RW/V	**Error Burst Number (ERR_BURST):** Burst number (in BL8) of the error within a chunk.
24	0h RW/V	**Error Chunk Number (ERR_CHUNK):** Chunk number of the error. 0 - lower 32B chunk has error if MERR/CERR is set 1 - higher 32B chunk has the error if MERR/CERR is set
23:16	0h RW/V	**Quad Word ECC Syndrome (SYNDROME_QW):** ECC Syndrome for a QW (64 bit) within 32B Address
15:0	0h RW/V	**Request Tag (TAG):** Read Return Tag matches with the PMI Request Tag which triggered the error log.

5.6.25 D-Unit Fuse Status (D_CR_DFUSESTAT)—Offset 1ABCh

Contains the values read from D-Unit fuses.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD31_16):** Reserved.
15:0	0h RO/V	**D-Unit Fuse Status (FUSESTAT):** D-Unit fuse bits are captured into this register and are available to be read. • [0]: fus_dun_ecc_dis. • [3:1]: fus_dun_max_supported_device_size[2:0]. • [4:4]: fus_dun_lpddr3_dis. • [5:5]: fus_dun_lpddr4_dis. • [6:6]: reserved. • [7:7]: fus_dun_ddr3l_dis. • [15:8]: reserved.

5.6.26 Major Mode Control (D_CR_MMC)—Offset 1B24h

Specifies parameters to control read/write major mode operation and transitions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2B01E518h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:27	5h RW	**RAW Conflict Read Priority for WMM Transition (RAW_WMM):** If a conflict read reaches this priority (or greater depending on access class occupancy), WMM will be triggered to unblock the corresponding write. D-Unit will stay in WMM until corresponding write is issued. Note: The value in this bit must not be higher than lowest terminal priority level of each access class.
26	0h RO	**Reserved (RSVD26):** Reserved.
25:23	6h RW	**Read Isoch Trigger Priority (RIMPRIO):** If any read in the RPQ is at this programmable priority, RIM is triggered.
22:18	0h RO	**Reserved (RSVD22_18):** Reserved.
17:12	1Eh RW	**Write Isoch Threshold (WIMTHRS):** When the number of entries in WPQ is greater than or equal to this value (higher than WMM entry watermark, less than WPQ size), it triggers write isoch mode (WIM).
11:6	14h RW	**Write Major Mode Exit Watermark (WMMEXIT):** When the number of entries in WPQ is less than this value, the D-Unit will switch back to read major mode.
5:0	18h RW	**Write Major Mode Entry Watermark (WMMENTRY):** When the number of entries in WPQ is greater than or equal to this value, the D-Unit will switch to write major mode (WMM). Note: the value must not be set to 0.

5.6.27 Major Mode RD/WR Counter (Set A and B) (D_CR_MMRDWR_AB)—Offset 1B28h

Minimum read and maximum write counter control. This register defines the minimum number of reads in RMM and maximum number of writes in WMM before a mode transition happens.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F207C8h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:20	1Fh RW	**Max Writes B (MAXWRB):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set B).

Bit Range	Default & Access	Field Name (ID): Description
19:14	8h RW	**Min Reads B (MINRDB):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set B).
13:12	0h RO	**Reserved (RSVD13_12):** Reserved.
11:6	1Fh RW	**Max Writes A (MAXWRA):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set A).
5:0	8h RW	**Min Reads A (MINRDA):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set A).

5.6.28 Major Mode RD/WR Counter (Set C and D) (D_CR_MMRDWR_CD)—Offset 1B2Ch

Minimum read and maximum write counter control. This register defines the minimum number of reads in RMM and maximum number of writes in WMM before a mode transition happens (sets C and D).

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F207C8h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD31_26):** Reserved.
25:20	1Fh RW	**Max Writes D (MAXWRD):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set D).
19:14	8h RW	**Min Reads D (MINRDD):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set D).
13:12	0h RO	**Reserved (RSVD13_12):** Reserved.
11:6	1Fh RW	**Max Writes C (MAXWRC):** Maximum number of writes D-Unit can send in WMM mode before returning to RMM (set C).
5:0	8h RW	**Min Reads C (MINRDC):** Minimum number of reads that has to be serviced before a switch to WMM is allowed (set C).

5.6.29 Access Class Initial Priority (D_CR_ACCIP)—Offset 1B30h

Each field of this register defines the initial priority of one access class.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 17C2h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved (RSVD31_15):** Reserved.
14:12	1h RW	**Access Class 4 Initial Priority (AC4IP):** Initial priority level of read requests coming with access class 4.
11:9	3h RW	**Access Class 3 Initial Priority (AC3IP):** Initial priority level of read requests coming with access class 3.
8:6	7h RW	**Access Class 2 Initial Priority (AC2IP):** Initial priority level of read requests coming with access class 2.
5:3	0h RW	**Access Class 1 Initial Priority (AC1IP):** Initial priority level of read requests coming with access class 1.
2:0	2h RW	**Access Class 0 Initial Priority (AC0IP):** Initial priority level of read requests coming with access class 0.

5.6.30 Access Class 0 Priority Promotion Control (D_CR_RD_PROM0)—Offset 1B34h

This register defines the priority promotion policy for access class 0. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F52940h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	Ah RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	Ah RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	Ah RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.6.31 Access Class 1 Priority Promotion Control (D_CR_RD_PROM1)—Offset 1B38h

This register defines the priority promotion policy for access class 1. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the associated level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 14000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	Ah RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	0h RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	0h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	0h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.6.32 Access Class 2 Priority Promotion Control (D_CR_RD_PROM2)—Offset 1B3Ch

This register defines the priority promotion policy for access class 2. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	0h RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	0h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	0h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.6.33 Access Class 3 Priority Promotion Control (D_CR_RD_PROM3)—Offset 1B40h

This register defines the aging policy for access class 3. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F29400h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	5h RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	5h RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	0h RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

Bit Range	Default & Access	Field Name (ID): Description
4:0	0h RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.6.34 Access Class 4 Priority Promotion Control (D_CR_RD_PROM4)—Offset 1B44h

This register defines the aging policy for access class 3. Each field of this register defines the number of CASes that pass before the request is promoted to the next priority level. A value of 31 indicates the request should never be promoted to the next level and the request has reached its maximum priority.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F5294Ah

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD31_30):** Reserved.
29:25	0h RW	**Priority 6 Residency (P6RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
24:20	1Fh RW	**Priority 5 Residency (P5RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
19:15	Ah RW	**Priority 4 Residency (P4RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
14:10	Ah RW	**Priority 3 Residency (P3RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
9:5	Ah RW	**Priority 2 Residency (P2RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.
4:0	Ah RW	**Priority 1 Residency (P1RES):** Number of CASes that pass before a request in this priority promotes to the next priority level.

5.6.35 Deadline Threshold (D_CR_DL_THRS)—Offset 1B48h

Specifies when the request with initial priority 0 get promoted to a higher priority level.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved (RSVD31_11):** Reserved.
10:0	6h RW	**Deadline Threshold (DEADLINE_THRS):** A requests with initial priority of 0 will exit priority 0 when its deadline is equal or less than this value plus current time. This field does not affect the priority of any requests in access classes with initial priority bigger than 0.

5.6.36 Major Mode Blocking Rules Control (D_CR_MM_BLK)—Offset 1B4Ch

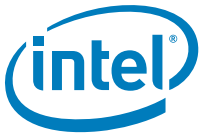
This register controls blocking rules enforced in RMM and WMM.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1800h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved (RSVD31_25):** Reserved.
24	0h RW	**WMM Regular Rule 1 (WMM_REG_R1):** Disable WMM unsafe write page hits block safe write page misses same bank.
23:20	0h RO	**Reserved (RSVD23_20):** Reserved.
19	0h RW	**WMM Priority Rule 4 (WMM_PRIO_R4):** Disable WMM unsafe priority 1 read miss block write hit to same bank. Note: This rule does not block the bank that is being blocked by WMM_PRIO_R3. Priority rules 1, 3 and 4 should be enabled/disabled together.
18	0h RW	**WMM Priority Rule 3 (WMM_PRIO_R3):** Disable WMM unsafe priority 1 write hit block write miss to same bank. Note: This rule does not block the bank that is being blocked by WMM_PRIO_R1. Priority rules 1,3 and 4 should be enabled/disabled together.
17	0h RW	**WMM Priority Rule 2 (WMM_PRIO_R2):** Disable WMM CAS block rule.
16	0h RW	**WMM Priority Rule 1 (WMM_PRIO_R1):** Disable WMM unsafe top priority 1 write miss block write hit same bank. Priority rules 1, 3 and 4 should be enabled/disabled together.
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13	0h RW	**RMM Regular Rule 6 (RMM_REG_R6):** Disable RMM unsafe write page hits block safe write page misses same bank.



Bit Range	Default & Access	Field Name (ID): Description
12	1h RW	**RMM Regular Rule 5 (RMM_REG_R5):** Disable RMM unsafe read page miss block all safe and unsafe write page hit to the same bank. Note: This field must not be set to 0 (enabled) if RMM_REG_R4 is also 0.
11	1h RW	**RMM Regular Rule 4 (RMM_REG_R4):** Disable RMM unsafe write page hit block safe read page miss same bank. Note: This field must not be set to 0 (enabled) if RMM_REG_R5 is also 0.
10	0h RW	**RMM Regular Rule 3 (RMM_REG_R3):** Disable RMM unsafe read page hit block safe read and write page miss same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R3 and RMM_PRIO_R1.
9	0h RW	**RMM Regular Rule 2 (RMM_REG_R2):** Disable RMM unsafe read page empty block safe write page empty same rank.
8	0h RW	**RMM Regular Rule 1 (RMM_REG_R1):** Disable RMM unsafe read page hit block safe write page hit same rank.
7:4	0h RO	**Reserved (RSVD7_4):** Reserved.
3	0h RW	**RMM Priority Rule 4 (RMM_PRIO_R4):** Disable RMM unsafe critical read miss block read and write hit to same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R3. Priority rules 1, 3 and 4 should be enabled/disabled together.
2	0h RW	**RMM Priority Rule 3 (RMM_PRIO_R3):** Disable RMM unsafe critical read hit block read and write miss to same bank. Note: This rule does not block the bank that is being blocked by RMM_PRIO_R1. Priority rules 1, 3 and 4 should be enabled/disabled together.
1	0h RW	**RMM Priority Rule 2 (RMM_PRIO_R2):** Disable RMM CAS block rule.
0	0h RW	**RMM Priority Rule 1 (RMM_PRIO_R1):** Disable RMM unsafe top critical read miss block read and write hit same bank. Note: Priority rules 1, 3 and 4 should be enabled/disabled together.

5.6.37 DRAM Self-Refresh Command (D_CR_DRAM_SR_CMD)—Offset 1B54h

Self refresh command register to allow sending WAKE and SUSPEND messages to D-Unit. (Only one bit can be set at a time). Posted writes to this register are not completed until hardware clears the field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD31_4):** Reserved.
3	0h RW/V	**SUSPENDP (SUSPENDP):** A SUSPENDP message will put the DRAM into self-refresh mode. The D-Unit will complete servicing outstanding memory requests and flush all queued Refresh commands to DRAM before putting the DRAM in self refresh mode. Finally, a PM message will be sent to the PHY. The bit is cleared by hardware after the PHY indicates the transition requested in the PM message has been completed. D-Unit will perform an MRW to MR17 with an opcode as defined by DPMC0.PASR before it places the DRAM into Self-Refresh.
2	0h RW/V	**SUSPEND (SUSPEND):** A SUSPEND message will put the DRAM into self-refresh mode. The D-Unit will complete servicing outstanding memory requests and flush all queued Refresh commands to DRAM before putting the DRAM in Self Refresh mode. Finally, a PM message will be sent to the PHY. The bit is cleared by hardware only after the PHY indicates the transition requested in the PM message has been completed. Note: When COLDWAKE is set prior of setting this bit the DRAM will not be placed in SR.
1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RW/V	**WAKE (WAKE):** Take PHY out of PM states and wakes the DRAM out of self refresh mode. The bit is cleared by hardware only when the DRAM has exited out of self refresh mode and is accessible. Note: When COLDWAKE is set prior of setting this bit the D-Unit will not send SR exit command and will not set the DCO.IC bit.

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**Clear Mask (CLEAR_MASK):** Mask ANDed with pseudo-random data. Resets to all 1s. Setting bit n to 0 in this register will force every nth bit in the data to be set to 0

5.6.38 DQS Retraining Control (D_CR_DQS_RETRAINING_CTL)—Offset 1B80h

LPDDR4 DQS Retraining control register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DQS Periodic Retraining Interval (DQS_RETRAIN_INT):** This sets the frequency by which the D-Unit initiates periodic retraining (in 1x NREFI).
15:14	0h RO	**Reserved (RSVD15_14):** Reserved.
13:4	0h RW	**DQS Oscillator Runtime (DQS_OSC_RT):** After D-Unit starts DQS oscillator, it must wait this amount of time before being able to read the value in MR18 and MR19 (in 16x DRAM clocks). Value in this register must be at least equal to DRAM's MR23 value. + tOSCO.
3:2	0h RO	**Reserved (RSVD3_2):** Reserved.
1	0h RW	**DQS Retrain SRX Exit (DQS_RETRAIN_SRX_EN):** Enable retraining on SR exit. This bit enables LPDDR4 DQS retraining on Self Refresh Exit. If disabled, D-Unit will not perform retraining on SR exit.
0	0h RW	**DQS Retrain Enable (DQS_RETRAIN_EN):** Periodic retraining enable: This bit enables periodic DQS retraining. If disabled, D-Unit will not perform retraining periodically. Note: Will be enabled only if DCO.IC is set and refreshes are enabled in DRF.MINREFRATE.

5.6.39 MR4 De-Swizzle Control (D_CR_MR4_DESWIZZLE)—Offset 1B84h

Controls the data bits swizzling crossbar for MR4.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD31):** Reserved.
30:28	0h RW	**MR4 Bit 2 Select 2nd Byte (MR4_BIT2_SEL2):** Selects bit 2 of MR4 data.
27	0h RO	**Reserved (RSVD27):** Reserved
26:24	0h RW	**MR4 Bit 1 Select 2nd Byte (MR4_BIT1_SEL2):** Selects bit 1 of MR4 data
23	0h RO	**Reserved (RSVD23):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
22:20	0h RW	**MR4 Bit 0 Select 2nd Byte (MR4_BIT0_SEL2):** Selects bit 0 of MR4 data.
19:18	0h RO	**Reserved (RSVD19_18):** Reserved
17:16	0h RW	**MR4 Byte 2 Select (MR4_BYTE_SEL2):** Selects byte position of the MR4 data for second device.
15	0h RO	**Reserved (RSVD15):** Reserved
14:12	0h RW	**MR4 Bit 2 Select (MR4_BIT2_SEL):** Selects bit 2 of MR4 data.
11	0h RO	**Reserved (RSVD11):** Reserved.
10:8	0h RW	**MR4 Bit 1 Select (MR4_BIT1_SEL):** Selects bit 1 of MR4 data.
7	0h RO	**Reserved (RSVD7):** Reserved.
6:4	0h RW	**MR4 Bit 0 Select (MR4_BIT0_SEL):** Selects bit 0 of MR4 data.
3:2	0h RO	**Reserved (RSVD3_2):** Reserved.
1:0	0h RW	**MR4 Byte Select (MR4_BYTE_SEL):** Selects byte position of the MR4 data first device.

5.7 Registers Summary

Table 5-7. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
7000h	7003h	Thermal Device Mailbox Data0 (P_CR_THERMAL_MAILBOX_DATA0_0_0_0_MCHBAR)—Offset 7000h	0h
7004h	7007h	Thermal Device Mailbox Data1 (P_CR_THERMAL_MAILBOX_DATA1_0_0_0_MCHBAR)—Offset 7004h	0h
7008h	700Bh	Thermal Device Mailbox Interface (P_CR_THERMAL_MAILBOX_INTERFACE_0_0_0_MCHBAR)—Offset 7008h	0h
700Ch	700Fh	Thermal Device IRQ and Lock Configuration (P_CR_THERMAL_DEVICE_IRQ_0_0_0_MCHBAR)—Offset 700Ch	0h
7010h	7013h	Package Thermal Interrupt Control (P_CR_PKG_THERM_INTERRUPT_0_0_0_MCHBAR)—Offset 7010h	0h
7014h	7017h	ISPDRIVER_PROCESSING_SYSTEM_FREQ_CAPABILITIES_0_0_0_MCHBAR (P_CR_PROCESSING_SYSTEM_FREQ_CAPABILITIES_0_0_0_MCHBAR)—Offset 7014h	0h
701Ch	701Fh	Package Thermal Status (P_CR_PKG_THERM_STATUS_0_0_0_MCHBAR)—Offset 701Ch	0h

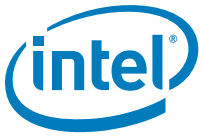


Table 5-7. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
7024h	7027h	LPDDR DRAM Thermal (MR4) Status of Channel 01 (P_CR_MEM_MR4_TEMPERATURE_DEV1_0_0_0_MCHBAR)—Offset 7024h	0h
7028h	702Bh	LPDDR DRAM Thermal (MR4) Status of Channel 10 (P_CR_MEM_MR4_TEMPERATURE_DEV2_0_0_0_MCHBAR)—Offset 7028h	0h
702Ch	702Fh	Machine Check Error Source Log (P_CR_MCA_ERROR_SRC_0_0_0_MCHBAR)—Offset 702Ch	0h
7030h	7033h	DDR Thermal Throttling Control (P_CR_DDR_THERM_THRT_CTRL_0_0_0_MCHBAR)—Offset 7030h	0h
7034h	7037h	DDR Thermal Interrupt Control (P_CR_DDR_THERM_INTERRUPT_0_0_0_MCHBAR)—Offset 7034h	0h
7038h	703Bh	DDR Thermal Status (P_CR_DDR_THERM_STATUS_0_0_0_MCHBAR)—Offset 7038h	0h
7048h	704Bh	Dram Energy Counter (P_CR_DDR_ENERGY_STATUS_0_0_0_MCHBAR)—Offset 7048h	0h
704Ch	704Fh	DDR RAPL Performance Status (P_CR_DDR_RAPL_PERF_STATUS_0_0_0_MCHBAR)—Offset 704Ch	58F0h
7050h	7053h	Package RAPL Performance Status (P_CR_PACKAGE_RAPL_PERF_STATUS_0_0_0_MCHBAR)—Offset 7050h	0h
7054h	7057h	IA Core Performance / Power Priority Control (P_CR_PRIMARY_PLANE_TURBO_PLCY_0_0_0_MCHBAR)—Offset 7054h	0h
7058h	705Bh	Graphics Performance / Power Priority Control (P_CR_SECONDARY_PLANE_TURBO_PLCY_0_0_0_MCHBAR)—Offset 7058h	10h
705Ch	705Fh	IA Energy Counter (P_CR_PRIMARY_PLANE_ENERGY_STATUS_0_0_0_MCHBAR)—Offset 705Ch	0h
7060h	7063h	Graphics Energy Counter (P_CR_SECONDARY_PLANE_ENERGY_STATUS_0_0_0_MCHBAR)—Offset 7060h	0h
7068h	706Bh	PACKAGE_POWER_SKU_UNIT (P_CR_PACKAGE_POWER_SKU_UNIT_0_0_0_MCHBAR)—Offset 7068h	330A0E08h
706Ch	706Fh	SOC Energy Counter (P_CR_PACKAGE_ENERGY_STATUS_0_0_0_MCHBAR)—Offset 706Ch	0h
7070h	7073h	GT_PERF_STATUS (P_CR_GT_PERF_STATUS_0_0_0_MCHBAR)—Offset 7070h	0h
7074h	7077h	Temperature Reference and Control (P_CR_TEMPERATURE_TARGET_0_0_0_MCHBAR)—Offset 7074h	5A0000h
7078h	707Bh	BIOS Reset Completion (P_CR_BIOS_RESET_CPL_0_0_0_MCHBAR)—Offset 7078h	0h
7080h	7083h	BIOS_MAILBOX_DATA (P_CR_BIOS_MAILBOX_DATA_0_0_0_MCHBAR)—Offset 7080h	0h
7084h	7087h	BIOS_MAILBOX_INTERFACE (P_CR_BIOS_MAILBOX_INTERFACE_0_0_0_MCHBAR)—Offset 7084h	0h

Table 5-7. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
7088h	708Bh	CORE_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_CORE_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 7088h	0h
708Ch	708Fh	GRAPHICS_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_GRAPHICS_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 708Ch	0h
7090h	7093h	SYSTEM_AGENT_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_SYSTEM_AGENT_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 7090h	0h
7094h	7097h	Memory Frequency Status (P_CR_FAR_MEMORY_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 7094h	0h
70A0h	70A7h	Package Power SKU and RAPL Power Control Capabilities (P_CR_PACKAGE_POWER_SKU_0_0_0_MCHBAR)—Offset 70A0h	12024000600118h
70A8h	70AFh	Package RAPL Power Limit (P_CR_PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR)—Offset 70A8h	0h
70B0h	70B3h	IA_PERF_LIMIT_REASONS (P_CR_IA_PERF_LIMIT_REASONS_0_0_0_MCHBAR)—Offset 70B0h	0h
70C0h	70C3h	IA Core C0 Residency Counter (P_CR_TELEM_IA_C0_RESIDENCY_0_0_0_MCHBAR)—Offset 70C0h	0h
70C4h	70C7h	Graphics C0 Residency Counter (P_CR_TELEM_GT_C0_RESIDENCY_0_0_0_MCHBAR)—Offset 70C4h	0h
70C8h	70CBh	I-unit Processing System C0 Residency Counter (P_CR_TELEM_IUNIT_C0_RESIDENCY_0_0_0_MCHBAR)—Offset 70C8h	0h
70CCh	70CFh	TELEM_IA_FREQ_ACCUMULATOR (P_CR_TELEM_IA_FREQ_ACCUMULATOR_0_0_0_MCHBAR)—Offset 70CCh	0h
70D0h	70D3h	Graphics C0 Residency Counter (P_CR_TELEM_GT_FREQ_ACCUMULATOR_0_0_0_MCHBAR)—Offset 70D0h	0h
70D4h	70D7h	I-unit Processing System C0 Residency Counter (P_CR_TELEM_IUNIT_FREQ_ACCUMULATOR_0_0_0_MCHBAR)—Offset 70D4h	0h
70E8h	70EFh	Memory Active Residency (P_CR_TELEM_FAR_MEMORY_ACTIVE_0_0_0_MCHBAR)—Offset 70E8h	0h
70F4h	70F7h	Package Temperatures (P_CR_PACKAGE_TEMPERATURES_0_0_0_MCHBAR)—Offset 70F4h	0h
7104h	7107h	Package Thermal Limit Control (P_CR_THERMAL_LIMIT_CONTROL_0_0_0_MCHBAR)—Offset 7104h	0h
7108h	710Bh	Memory Subsystem Frequency Capabilities (P_CR_MEMSS_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 7108h	0h
7114h	7117h	Memory Controller (MC) BIOS Reset Request and Status (P_CR_MC_BIOS_REQ_0_0_0_MCHBAR)—Offset 7114h	0h
7118h	711Bh	MEMSS_FREQUENCY_CAPABILITIES1 (P_CR_MEMSS_FREQUENCY_CAPABILITIES1_0_0_0_MCHBAR)—Offset 7118h	0h

Table 5-7. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
7160h	7163h	PP1_C0_CORE_CLOCK_0_0_0_MCHBAR (P_CR_PP1_C0_CORE_CLOCK_0_0_0_MCHBAR)—Offset 7160h	0h
7164h	7167h	Core Exists Vector (P_CR_CORE_EXISTS_VECTOR_0_0_0_MCHBAR)—Offset 7164h	0h
7168h	716Bh	Software Core Disable Mask (P_CR_CORE_DISABLE_MASK_0_0_0_MCHBAR)—Offset 7168h	0h
71F0h	71F7h	PL3 and PL4 Control (P_CR_PL3_CONTROL_0_0_0_MCHBAR)—Offset 71F0h	0h
7244h	7247h	Graphics Superqueue Active Clocks (P_CR_PP1_ANY_THREAD_ACTIVITY_0_0_0_MCHBAR)—Offset 7244h	0h
7248h	724Bh	LPDDR DRAM Thermal (MR4) Status of Channel 00 (P_CR_MEM_MR4_TEMPERATURE_DEV3_0_0_0_MCHBAR)—Offset 7248h	0h
724Ch	724Fh	LPDDR DRAM Thermal (MR4) Status of Channel 11 (P_CR_MEM_MR4_TEMPERATURE_DEV4_0_0_0_MCHBAR)—Offset 724Ch	0h

5.7.1 Thermal Device Mailbox Data0 (P_CR_THERMAL_MAILBOX_DATA0_0_0_0_MCHBAR)—Offset 7000h

This register represents the lower 32b of the thermal mailbox data. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**DATA[31:0] (DATA):** This field contains the low 32 bits of data associated with specific commands.

5.7.2 Thermal Device Mailbox Data1 (P_CR_THERMAL_MAILBOX_DATA1_0_0_0_MCHBAR)—Offset 7004h

This register represents the upper 32b of the thermal mailbox data. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**DATA[63:32] (DATA):** This field contains the low 32 bits of data associated with specific commands.

5.7.3 Thermal Device Mailbox Interface (P_CR_THERMAL_MAILBOX_INTERFACE_0_0_0_MCHBAR)—Offset 7008h

This register implements the control and response of the Thermal Device Mailbox. Software may use this mailbox to configure and query various parameters into SOC thermal / power control. This particular register is responsible for initiating requests to the thermal device and reading responses. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Run/Busy (RUN_BUSY):** The run/busy control is used for managing the semaphore on the mailbox interface. Typical usage involves the following flow: • Software waits for the interface run/busy bit to clear. • Software writes the mailbox data registers as appropriate for this command. • Software writes a command encoding and sets the run/busy bit in the interface register. • Software waits for the interface run/busy bit to clear to indicate the command has been handled. • Software queries the completion code in the command field of the interface register to ensure it passed (0b indicates pass) Bit encoding for the run/busy: • 0 = The thermal mailbox is idle or the last request has been completed. Software may initiate new requests. • 1 = The thermal mailbox is busy. The thermal device is still handling a request. Writes to thermal mailbox are not allowed at this time.
30:29	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28:8	0h RW/V	**Additional Parameters (ADDR_CNTL):** This field is used as an additional modifier to the command encoding for incoming mailbox requests. In thermal device mailbox responses, this field is always zero. The applicability of this additional parameter field is handled on a case by case basis for the services supplied by this mailbox
7:0	0h RW/V	**Command / Completion Code (COMMAND):** For incoming requests (where run/busy=1), this field represents the command opcode. For responses (where run/busy=0), this field represents the response completion code. A completion code of 0b indicates passing, all other completion codes indicate failure.

5.7.4 Thermal Device IRQ and Lock Configuration (P_CR_THERMAL_DEVICE_IRQ_0_0_0_MCHBAR)—Offset 700Ch

IRQ vector number for thermal/power device that is sent to the IOAPIC and Lock field for INTR_LAT_0_0_1_PCI.INTRPIN

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**LOCK (LOCK):** Used to lock P_CR_INTR_LAT_0_0_1_PCI.INTPIN. BIOS should set this lock bit before passing control to the OS
30:8	0h RO	**RESERVED (RESERVED):** Reserved
7:0	0h RW	**IRQ (IRQ):** IRQ vector number for the thermal / power device. This field controls the event vector issues to the IOAPIC. It must be configured by BIOS for INTA support.

5.7.5 Package Thermal Interrupt Control (P_CR_PKG_THERM_INTERRUPT_0_0_0_MCHBAR)—Offset 7010h

This register is used to manage processor thermal interrupts, including management of filtering on the virtual thermal sensor control signal. These features are designed to allow software to implement smooth control of thermally significant events for platform thermal management. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:24	0h RW	**Time Window (TIME_WINDOW):** Virtual Temperature thermal filter RC time constant. Virtual temperature readings are run through an RC filter before they are fed into status and interrupt generation. This filtering allows software smooth control of thermal responses to thermally significant events. The bits of this field describe parameters for a mathematical equation for time window configuration. This field is split into two sub-fields: • x = bits[6:5] • y = bits[4:0] Time window equation: **time_window = PACKAGE_POWER_SKU_UNIT.TIME_UNIT * ((1+x/4)^y)**
23:16	0h RW	**Thermal Threshold 2 Temperature (THRESHOLD2_TEMP):** Thermal interrupt threshold temperature in degrees Celsius. Described in a signed, 2's complement format with the LSB representing 1'C resolution (S8.7.0). E.g., a reading of 0x28 == 40'C. This threshold is managed relative to the filtered temperature.
15:8	0h RW	**Thermal Threshold 1 Temperature (THRESHOLD1_TEMP):** Thermal interrupt threshold temperature in degrees Celsius. Described in a signed, 2's complement format with the LSB representing 1'C resolution (S8.7.0). E.g., a reading of 0x28 == 40'C. This threshold is managed relative to the filtered temperature.
7:3	0h RO	Reserved.
2	0h RW	**Critical Thermal Event Interrupt Enable (CRITICAL_THERMAL_INT_ENABLE):** Enable thermal interrupt generation when the processor has detected a critical thermal event that requires immediate servicing. This event is intended to be an alert indicating thermal control failure and is an early warning of thermal runaway.
1	0h RW	**THRESHOLD2_INT_ENABLE (THRESHOLD2_INT_ENABLE):** When set, enables the generation of a thermal interrupt whenever the Thermal Threshold 2 Temperature is crossed. Interrupts are generated when the threshold is crossed in either direction. Interrupt destination is programmed in the TMBAR configuration space.
0	0h RW	**Threshold 1 Interrupt Enable (THRESHOLD1_INT_ENABLE):** When set, enables the generation of a thermal interrupt whenever the Thermal Threshold 1 Temperature is crossed. Interrupts are generated when the threshold is crossed in either direction. Interrupt destination is programmed in the TMBAR configuration space.

5.7.6 ISPDRIVER_PROCESSING_SYSTEM_FREQ_CAPABILITIES_0_0_0_MCHBAR (P_CR_PROCESSING_SYSTEM_FREQ_CAPABILITIES_0_0_0_MCHBAR)—Offset 7014h

PUNIT_MMIO: Image Processing System Frequency Capabilities
This register describes the frequency capabilities of the image processing system. Units are 25MHz multiplied by the ratio.
Minimum and maximum ratio fields are initialized by pCode at reset. Last resolved ratio is updated upon changes to the processing system frequency. The efficient ratio is determined by firmware and may be updated dynamically depending on firmware support.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LAST_RESOLVED_RATIO (LAST_RESOLVED_RATIO):** Last resolved ratio for the image processing system. Units are 25MHz multiplied by the ratio. This value is updated dynamically whenever the processing system frequency changes.
23:16	0h RO/V	**MAX_RATIO (MAX_RATIO):** Maximum ratio for the image processing system. Units are 25MHz multiplied by the ratio.
15:8	0h RO/V	**EFFICIENT_RATIO (EFFICIENT_RATIO):** Firmware-calculated efficient ratio for the image processing system. Units are 25MHz multiplied by the ratio.
7:0	0h RO/V	**MIN_RATIO (MIN_RATIO):** Minimum ratio for the image processing system. Units are 25MHz multiplied by the ratio.

5.7.7 Package Thermal Status (P_CR_PKG_THERM_STATUS_0_0_0_MCHBAR)—Offset 701Ch

This register is used to monitor the status of the package level virtual thermal sensor and details on the source of package level thermal events. The package level virtual thermal sensor is a filtered version of the maximum temperature observed at any domain within the package. That temperature is applied to the Package Thermal Interrupt configuration for event delivery to software for run-time thermal management. When an event is observed, this register describe the source(s) of that event.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	0h RO/V	**Temperature (TEMPERATURE):** Virtual maximum SOC temperature in degrees Celsius. Calculated as a maximum of all on-die thermal sensor readings and filtered according to the time constant described in the PKG_THERM_INTERRUPT register. Data format is signed, 2's complement with the LSB representing 1'C resolution (S8.7.0).
15:6	0h RO	Reserved.
5	0h RW/0C/V	**Critical Thermal Event Log (CRITICAL_THERMAL_EVENT_LOG):** Sticky log bit indicating that the processor has operated out of its thermal specification since the last time software cleared this bit. Set by hardware on a 0 to 1 transition of Critical Thermal Event Status.
4	0h RO/V	**Critical Thermal Event Status (CRITICAL_THERMAL_EVENT_STATUS):** Status bit indicating that the processor is operating outside of its thermal specification. It is intended as an early warning of thermal runaway in the silicon and shutdown is recommended.
3	0h RW/0C/V	**Thermal Threshold 2 Log (THRESHOLD2_LOG):** Sticky log bit that indicates temperature has crossed the software programmable thermal threshold2 in either falling or rising directions.
2	0h RO/V	**Thermal Threshold 2 Status (THRESHOLD2_STATUS):** Indicates that the current filtered temperature (bits 23:16 of this register) is greater than or equal to the Threshold2 defined in the PKG_THERM_INTERRUPT configuration register.
1	0h RW/0C/V	**Thermal Threshold 1 Log (THRESHOLD1_LOG):** Sticky log bit that indicates temperature has crossed the software programmable thermal threshold1 in either falling or rising directions.
0	0h RO/V	**Thermal Threshold 1 Status (THRESHOLD1_STATUS):** Indicates that the current filtered temperature (bits 23:16 of this register) is greater than or equal to the Threshold1 defined in the PKG_THERM_INTERRUPT configuration register.

5.7.8 LPDDR DRAM Thermal (MR4) Status of Channel 01 (P_CR_MEM_MR4_TEMPERATURE_DEV1_0_0_0_MCHBAR)—Offset 7024h

LPDDR DRAM Thermal (MR4) Status of Channel 01, when there are multiple DRAMs in a rank, the maximum MR4 is reported

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
5:3	0h RW	**MR4 DRAM thermal status of Channel 01 Rank 1 (MR4_RANK_1):** This field is updated each read of LPDDR DRAM MR4 Device Temperature Status per rank. Update rate is configured by BIOS.
2:0	0h RW	**MR4 DRAM thermal status of Channel 01 Rank 0 (MR4_RANK_0):** This field is updated each read of LPDDR DRAM MR4 Device Temperature Status per rank. Update rate is configured by BIOS.

5.7.9 LPDDR DRAM Thermal (MR4) Status of Channel 10 (P_CR_MEM_MR4_TEMPERATURE_DEV2_0_0_0_MCHBAR)—Offset 7028h

LPDDR DRAM Thermal (MR4) Status of Channel 10, when there are multiple DRAMs in a rank, the maximum MR4 is reported

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
5:3	0h RW	**MR4 DRAM thermal status of Channel 10 Rank 1 (MR4_RANK_1):** This field is updated each read of LPDDR DRAM MR4 Device Temperature Status per rank. Update rate is configured by BIOS.
2:0	0h RW	**MR4 DRAM thermal status of Channel 10 Rank 0 (MR4_RANK_0):** This field is updated each read of LPDDR DRAM MR4 Device Temperature Status per rank. Update rate is configured by BIOS.

5.7.10 Machine Check Error Source Log (P_CR_MCA_ERROR_SRC_0_0_0_MCHBAR)—Offset 702Ch

This register logs error source information i.e IERR or MCERR information for Pcode. The error fields are cleared by HW or BIOS. This register is also shadowed in the I/O space.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**CATERR (CATERR):** Asserted by HW on IERR or MCERR assertion.
30	0h RW/V	**IERR (IERR):** Asserted by HW on IERR assertion.
29	0h RW/V	**MCERR (MCERR):** Asserted by HW on MCERR assertion.
28:8	0h RO	Reserved.
7:0	0h RW	**RESERVED (RESERVED):** Undefined - reserved for future use.

5.7.11 DDR Thermal Throttling Control (P_CR_DDR_THERM_THRT_CTRL_0_0_0_MCHBAR)—Offset 7030h

This register is used to configure thermal throttling policies for memory.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**RESERVED_1 (RESERVED_1):** RESERVED
25	0h RW/V	**DDR3L Refresh Rate (DDR3L_REFRESH_RATE):** This field is to allow platform software to request refresh rate for DDR3L
24	0h RW/V	**DDR3L Throttle Enable (THROTTLE_LEVEL_ENABLE):** When set and DRAM_Type is DDR3L, SOC throttles memory traffic to level specified in THRT_LVL NOTE: This field is ignored if DRAM_Type is not DDR3L

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RW/V	**DDR3L Throttle Level (THROTTLE_LEVEL):** Throttle level in %BW, in units of 1%. Default = 0%. Input of 100 or higher is clipped to 100%, NOTE: this field is ignored if DRAM_type is not DDR3L
15:10	0h RO	**RESERVED_0 (RESERVED_0):** RESERVED
9	0h RW/V	**Memory Thermal Throttle Enable (MEM_THRT_ENABLE):** When set, memory traffic is throttled if memory MR4 value >= THERM_THRT_THRESHOLD, respectively. Thermal throttling is achieved by applying memory bandwidth clips in the memory subsystem.
8	0h RW/V	**Memory Thermal Throttling Configuration (MEM_THRT_CFG):** Configure memory throttling behavior. Policies are defined as follows: • 0 = Thermal throttling policy uses instantaneous MR4 status for THERM_THRT_THRESHOLD • 1 = Thermal throttling policy uses time filtered MR4 status for THERM_THRT_THRESHOLD. Filtering time constant is configured in the DDR_THERM_INTERRUPT register.
7	0h RW/V	**Reserved (NM_THERM_THRT_ENABLE):** Reserved
6:4	0h RW/V	**Reserved (NM_THERM_THRT_THRESHOLD):** Reserved
3	0h RW/V	**LPDDR Memory Thermal Throttling Enable (FM_THERM_THRT_ENABLE):** When set, throttling is activated if LPDDR memory MR4 value is greater than or equal to THERM_THRT_THRESHOLD. For the standard LPDDR DRAM that is only capable up to Tcasemax of 85C this bit should be set to enable LPDDR throttling to keep DRAM within its Tcasemax spec.
2:0	0h RW/V	**LPDDR Memory Thermal Throttling Threshold (FM_THERM_THRT_THRESHOLD):** Configurable threshold of LPDDR memory MR4 value greater than or equal to which thermal throttling is activated. For the standard LPDDR DRAM that is only capable up to Tcasemax of 85C this field should be configured to avoid DRAM to exceed its Tcasemax spec. • Memory MR4 >= Threshold = Enable thermal throttling • Memory MR4 < Threshold = Disable thermal throttling

5.7.12 DDR Thermal Interrupt Control (P_CR_DDR_THERM_INTERRUPT_0_0_0_MCHBAR)—Offset 7034h

This register is used to manage DDR thermal interrupts, including management of filtering on the virtual DRAM thermal sensor control signal. These features are designed to allow software to implement smooth control of thermally significant events for platform thermal management.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:24	0h RW	**Time Window (TIME_WINDOW):** Virtual Temperature thermal filter RC time constant. Virtual temperature readings are run through an RC filter before they are fed into status and interrupt generation. This filtering allows software smooth control of thermal responses to thermally significant events. The bits of this field describe parameters for a mathematical equation for time window configuration. This field is split into two sub-fields: • x = bits[6:5] • y = bits[4:0] Time window equation: **time_window = PACKAGE_POWER_SKU_UNIT.TIME_UNIT * ((1+x/4)^y)**
23:16	0h RO	Reserved.
15	0h RW	**Reserved (NEAR_MEM_MR4_THRESHOLD2_INT_ENABLE):** Reserved
14:12	0h RW	**Reserved (NEAR_MEM_MR4_THRESHOLD2):** Reserved
11	0h RW	**Reserved (NEAR_MEM_MR4_THRESHOLD1_INT_ENABLE):** Reserved
10:8	0h RW	**Reserved (NEAR_MEM_MR4_THRESHOLD1):** Reserved
7	0h RW	**Memory MR4 Threshold 2 Interrupt Enable (FAR_MEM_MR4_THRESHOLD2_INT_ENABLE):** Enable thermal interrupt generation whenever the virtual maximum memory MR4 has crossed THRESHOLD2. Interrupts are triggered when the filtered MR4 temperature crosses in both rising and falling directions.
6:4	0h RW	**Memory MR4 Threshold 2 (FAR_MEM_MR4_THRESHOLD2):** Configurable memory threshold2 value for memory thermal interrupt generation
3	0h RW	**Memory MR4 Threshold 1 Interrupt Enable (FAR_MEM_MR4_THRESHOLD1_INT_ENABLE):** Enable thermal interrupt generation whenever the virtual maximum memory MR4 has crossed THRESHOLD1. Interrupts are triggered when the filtered MR4 temperature crosses in both rising and falling directions.
2:0	0h RW	**Memory MR4 Threshold 1 (FAR_MEM_MR4_THRESHOLD1):** Configurable memory threshold1 value for memory thermal interrupt generation

5.7.13 DDR Thermal Status (P_CR_DDR_THERM_STATUS_0_0_0_MCHBAR)—Offset 7038h

Status register for monitoring DDR thermal status. Data reported here is aggregated by memory type, and values reported represent the maximum MR4 readings observed in those respective domains. Temperatures are additionally filtered by the MR4 thermal filtering time constant described in the DDR Thermal Interrupt configuration register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:19	0h RO/V	**Reserved (NEAR_MEM_MR4):** Reserved
18:16	0h RO/V	**LPDDR Memory MR4 (FAR_MEM_MR4):** Virtual maximum memory MR4 reading. Calculated as a maximum of all LPDDR memory MR4 readings and filtered according to the time constant described in DDR_THERM_INTERRUPT register.
15:8	0h RO	Reserved.
7	0h RW/0C/V	**Reserved (NEAR_MEM_MR4_THRESHOLD2_LOG):** Reserved
6	0h RO/V	**Reserved (NEAR_MEM_MR4_THRESHOLD2_STATUS):** Reserved
5	0h RW/0C/V	**Reserved (NEAR_MEM_MR4_THRESHOLD1_LOG):** Reserved
4	0h RO/V	**Reserved (NEAR_MEM_MR4_THRESHOLD1_STATUS):** Reserved
3	0h RW/0C/V	**Memory MR4 Threshold2 Log (FAR_MEM_MR4_THRESHOLD2_LOG):** Indicates that the virtual maximum memory MR4 has crossed THRESHOLD2 since the last time this register was cleared. The bit is set when the threshold is crossed in either direction. Software may clear this bit.
2	0h RO/V	**Memory MR4 Threshold2 Status (FAR_MEM_MR4_THRESHOLD2_STATUS):** Status bit is set when the virtual maximum memory MR4 reading is greater than or equal to THRESHOLD2. It is cleared when temperature is less than THRESHOLD2

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW/0C/V	**Memory MR4 Threshold1 Log (FAR_MEM_MR4_THRESHOLD1_LOG):** Indicates that the virtual maximum memory MR4 has crossed THRESHOLD1 since the last time this register was cleared. The bit is set when the threshold is crossed in either direction. Software may clear this bit.
0	0h RO/V	**Memory MR4 Threshold1 Status (FAR_MEM_MR4_THRESHOLD1_STATUS):** Status bit is set when the virtual maximum memory MR4 reading is greater than or equal to THRESHOLD1. It is cleared when temperature is less than THRESHOLD1

5.7.14 Dram Energy Counter (P_CR_DDR_ENERGY_STATUS_0_0_0_MCHBAR)—Offset 7048h

Reports total energy consumed in DRAM. The energy status is reported in units which are defined by PACKAGE_POWER_SKU_UNIT_MSR.ENERGY_UNIT. The counter will wrap around and continue counting from zero when it reaches its limit and therefore should be polled sufficiently frequently to avoid aliasing. Typically, software will calculate delta energy and delta time and divide the two to estimate Watts consumed over a time window. The value of this register is updated at approximately every 1ms. This energy status is what is used by DDR RAPL or OLTM control algorithms if the product supports those features.
To calculate Watts: **Watts = delta(energy) / delta(time) / 2^PACKAGE_POWER_SKU_UNIT_MSR.ENERGY_UNIT** THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**JOULES (JOULES):** Total Joules of energy consumed by all DIMMs. Units are proportional to Joules and are defined by PACKAGE_POWER_SKU_UNIT_MSR.ENERGY_UNIT.

5.7.15 DDR RAPL Performance Status (P_CR_DDR_RAPL_PERF_STATUS_0_0_0_MCHBAR)—Offset 704Ch

Memory RAPL performance throttling counter. This counter accumulates time that any channel in the memory controller is bandwidth throttled due to memory RAPL constraints. This counter counts total time (in PACKAGE_POWER_SKU_UNIT_MSR.TIME_UNIT units) that any channel is throttled. If

two channels are throttled, this counter increments at a 2x rate, so that for 1ms in wall clock time the counter counts 2ms. This counter does not include throttling as a result of thermal management or MEMHOT. This register is updated at approximately 1ms intervals. This counter is normalized to 'seconds' and is not subject to variation of actual DRAM clock speeds. This register is read only for software via MMIO MSR and PECI/PCS. This register starts counting at zero from reset and continues counting forever and wraparounds may occur, so software should ensure the sample rate is sufficient to avoid aliasing. This is an unsigned value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 58F0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	58F0h RW	**DDR Bandwidth Throttle Duration (DURATION):** Bandwidth throttle duration counter due to Memory RAPL. Sum across all channels in PACKAGE_POWER_SKU_UNIT_MSR.TIME_UNIT units. This data can serve as a proxy for the potential performance impacts of RAPL on memory accesses.

5.7.16 Package RAPL Performance Status (P_CR_PACKAGE_RAPL_PERF_STATUS_0_0_0_MCHBAR) —Offset 7050h

Counts time that any core in the IA domain is performance throttled below OS request and below the base frequency (P1) because of power limits (PL1 or PL2). Counts in time units defined by PACKAGE_POWER_SKU_UNIT_MSR.TIME_UNIT. If software uses the TURBO_ACTIVATION_RATIO or PECI ACPI P-NOTIFY, the turbo activation ratios described by those features will may elevate the effective OS request (as calculated by this counter) to max turbo. This register starts counting at zero from reset and continues counting forever and wraparounds may occur, so software should ensure the sample rate is sufficient to avoid aliasing. This is an unsigned value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Performance Throttle Duration (COUNTS):** Time that any core in the IA domain is performance throttled below OS request and below the base frequency (P1) because of power limits (PL1 or PL2). Counts in time units defined by PACKAGE_POWER_SKU_UNIT_MSR.TIME_UNIT

5.7.17 IA Core Performance / Power Priority Control (P_CR_PRIMARY_PLANE_TURBO_PLCY_0_0_0_MCHBAR)—Offset 7054h

The PRIMARY_PLANE_TURBO_POWER_POLICY and SECONDARY_PLANE_TURBO_POWER_POLICY are used together as hints to balance the power budget between the primary (IA core) and secondary (Graphics) power planes. This biasing is effectively a performance biasing, and it helps Punit firmware assess where software needs performance the most

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
4:0	0h RW	**IA Core Priority Level (PRIPTP):** Performance priority Level for the IA Core (primary) power plane. A higher number implies a higher priority.

5.7.18 Graphics Performance / Power Priority Control (P_CR_SECONDARY_PLANE_TURBO_PLCY_0_0_0_MCHBAR)—Offset 7058h

The PRIMARY_PLANE_TURBO_POWER_POLICY and SECONDARY_PLANE_TURBO_POWER_POLICY are used together as hints to balance the power budget between the primary (IA core) and secondary (Graphics) power planes. This biasing is effectively a performance biasing, and it helps Punit firmware assess where software needs performance the most

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
4:0	10h RW	**Graphics Priority Level (SECPTP):** Performance priority Level for the Graphics (secondary) power plane. A higher number implies a higher priority.

5.7.19 IA Energy Counter (P_CR_PRIMARY_PLANE_ENERGY_STATUS_0_0_0_MCHBAR)—Offset 705Ch

Reports total energy consumed across all IA cores. The energy status is reported in units which are defined by PACKAGE_POWER_SKU_UNIT_MSR.ENERGY_UNIT. The counter will wrap around and continue counting from zero when it reaches its limit and therefore should be polled sufficiently frequently to avoid aliasing. Typically, software will calculate delta energy and delta time and divide the two to estimate Watts consumed over a time window. The value of this register is updated at approximately every 1ms.
To calculate Watts: **Watts = delta(energy) / delta(time) / 2^PACKAGE_POWER_SKU_UNIT_MSR.ENERGY_UNIT** THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**IA Energy Counter (DATA):** Contains an accumulated value of the energy consumed in the primary power plane. To find the energy consumed in a given time window, software should subtract the two energy readings. Software will have to take care of counter wrapping around when it overflows. Units are proportional to Joules exact precision is defined by PACKAGE_POWER_SKU_UNIT_MSR.ENERGY_UNIT

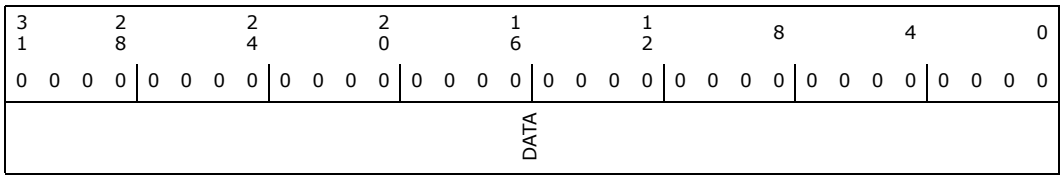
5.7.20 Graphics Energy Counter (P_CR_SECONDARY_PLANE_ENERGY_STATUS_0_0_0_MCHBAR)—Offset 7060h

Reports total energy consumed across all IA cores. The energy status is reported in units which are defined by PACKAGE_POWER_SKU_UNIT_MSR.ENERGY_UNIT. The counter will wrap around and continue counting from zero when it reaches its limit and therefore should be polled sufficiently frequently to avoid aliasing. Typically, software will calculate delta energy and delta time and divide the two to estimate Watts consumed over a time window. The value of this register is updated at approximately every 1ms.
To calculate Watts: **Watts = delta(energy) / delta(time) / 2^PACKAGE_POWER_SKU_UNIT_MSR.ENERGY_UNIT** THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Graphics Energy Counter (DATA):** Contains an accumulated value of the energy consumed in the secondary power plane. To find the energy consumed in a given time window, sofwtare should subtract the two energy readings. Software will have to take care of counter wrapping around when it overflows. Units are proportional to Joules exact precsion is defined by PACKAGE_POWER_SKU_UNIT_MSR.ENERGY_UNIT

5.7.21 PACKAGE_POWER_SKU_UNIT (P_CR_PACKAGE_POWER_SKU_UNIT_0_0_0_MCHBAR)—Offset 7068h

Defines units for calculating SKU power, current, energy, resistance and timing parameters.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 330A0E08h

Bit Range	Default & Access	Field Name (ID): Description
31:28	3h RW	**RESISTANCE_UNIT (RESISTANCE_UNIT):** Used to define the units of resistance for control registers that describe parameters in ohms such as VR_CURRENT_CONFIG. The actual unit value is calculated by 1mohm / 2^RESISTANCE_UNIT. The default value of 3 corresponds to 0.125mohm.
27:24	3h RW	**CURRENT_UNIT (CURRENT_UNIT):** Used to define the units of amps in control registers such as VR_CURRENT_CONFIG. The actual unit value is calculated by 1A / 2^CURRENT_UNIT. The default value of 3 corresponds to 0.125A.
23:20	0h RSV	**RESERVED_2 (RESERVED_2):** Reserved
19:16	Ah RW	**TIME_UNIT (TIME_UNIT):** Used for to define the time units in registers such as PL1, PL2, PL3 and PL4. The actual unit value is calculated by 1s / 2^TIME_UNIT. The default value of 10 corresponds to 0.977ms.
15:13	0h RSV	**RESERVED_1 (RESERVED_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
12:8	Eh RW	**ENERGY_UNIT (ENERGY_UNIT):** Used to define the units of energy reporting registers such as PACKAGE_ENERGY_STATUS. The actual unit value is calculated by 1 J / 2^ENERGY_UNIT. The default value of 14 corresponds to ~61uJ per bit.
7:4	0h RSV	**RESERVED_0 (RESERVED_0):** Reserved
3:0	8h RW	**PWR_UNIT (PWR_UNIT):** Used to define the units of power control registers such as PL1, PL2, PL3 and PL4. The actual unit value is calculated by 1 W / 2^PWR_UNIT. The default value of 8 corresponds to 3.9mW per bit.

5.7.22 SOC Energy Counter (P_CR_PACKAGE_ENERGY_STATUS_0_0_0_MCHBAR)—Offset 706Ch

Reports total energy consumed across the entire SOC / Package. The energy status is reported in units which are defined by PACKAGE_POWER_SKU_UNIT_MSR.ENERGY_UNIT. The counter will wrap around and continue counting from zero when it reaches its limit and therefore should be polled sufficiently frequently to avoid aliasing. Typically, software will calculate delta energy and delta time and divide the two to estimate Watts consumed over a time window. The value of this register is updated at approximately every 1ms. This energy status is what is used by RAPL PL1, PL2 and PL3 control algorithms.
To calculate Watts: **Watts = delta(energy) / delta(time) / 2^PACKAGE_POWER_SKU_UNIT_MSR.ENERGY_UNIT** THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**SOC Energy Counter (DATA):** Contains accumulated energy consumed by the entire CPU. This counter will wrap around and keep counting when the counter overflows. Units are proportional to Joules exact precision is defined by PACKAGE_POWER_SKU_UNIT_MSR.ENERGY_UNIT

5.7.23 GT_PERF_STATUS (P_CR_GT_PERF_STATUS_0_0_0_MCHBAR)—Offset 7070h

Contains the voltage and ratio status for GT. This register is mapped to GT_PERF_STATUS_0_0_0_MCHBAR.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25:17	0h RO/V	**RP_STATE_RATIO_SLICE (RP_STATE_RATIO_SLICE):** Ratio of the current RP-state, in 16.6Mhz 1xclks. When the graphics engine is in RC6, this field is zeroed out.
16:8	0h RO/V	**RP_STATE_RATIO_UNSLICE (RP_STATE_RATIO_UNSLICE):** Ratio of the current RP-state, in 16.6Mhz 1xclks. When the graphics engine is in RC6, this field is zeroed out.
7:0	0h RO/V	**RP_STATE_VOLTAGE (RP_STATE_VOLTAGE):** RP-State Voltage GT Target Voltage in U1.7 Volts

5.7.24 Temperature Reference and Control (P_CR_TEMPERATURE_TARGET_0_0_0_MCHBAR)—Offset 7074h

This register contains information about the fan speed control target temperature as well as details on the reference temperature for IA core DTS relative temperature reading. **MSR_Name**: TEMPERATURE_TARGET **MSR_Addr**: 0x1A2

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 5A0000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RSV	**RESERVED_1 (RESERVED_1):** Reserved
30:24	0h RW	**Thermal Monitor Activation Offset Control (TJ_MAX_TCC_OFFSET):** This field allows platform software to configure the temperature at which thermal monitor engages to be lower than the manufacturing configured maximum constraint. This field is programmed in 1'C units. E.g., if the default silicon configured maximum temperature is 100'C and this field is configured to 10, then the silicon will engage thermal throttling algorithms at 90'C

Bit Range	Default & Access	Field Name (ID): Description
23:16	5Ah RO/V	**Reference Temperature (REF_TEMP):** Tjmax a.k.a. Thermal Monitor activation temperature or Prochot Temperature. This is the maximum junction temperature at which thermal throttling aka thermal monitor is activated. This temperature is the maximum temperature at which the silicon is capable of operating at. All IA core digital thermal sensor readings are reported as a relative negative offset from this reference temperature, such that a read on of zero implies the cores are running at this temperature.
15:8	0h RO/V	**Fan Temperature Target Offset (FAN_TEMP_TARGET_OFFSET):** Fan Temperature Target Offset a.k.a. TControl indicates the relative offset from the the Thermal Monitor Trip Temperature at which fans should be engaged.
7:0	0h RSV	**RESERVED_0 (RESERVED_0):** Reserved

5.7.25 BIOS Reset Completion (P_CR_BIOS_RESET_CPL_0_0_0_MCHBAR)—Offset 7078h

This register is used as a means for BIOS to communicate staging to the Punit / Pcode. The exact definition and utility of each bit may differ across products. The general philosophy is that when BIOS is done with stage0, it writes the RST_CPL0 bit and then waits for the PCODE_INIT_DONE0 bit to be set before proceeding to the next step.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**RESERVED0 (RESERVED0):** reserved
15	0h RO/V	**Stage7 Pcode Reset Complete (PCODE_INIT_DONE7):** Pcode sets this bit when it has completed this stage, BIOS must wait for this bit to be set before proceeding to the next stage. Stage validity is product-specific and this stage may not be applicable to this product.
14	0h RO/V	**Stage6 Pcode Reset Complete (PCODE_INIT_DONE6):** Pcode sets this bit when it has completed this stage, BIOS must wait for this bit to be set before proceeding to the next stage. Stage validity is product-specific and this stage may not be applicable to this product.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO/V	**Stage5 Pcode Reset Complete (PCODE_INIT_DONE5):** Pcode sets this bit when it has completed this stage, BIOS must wait for this bit to be set before proceeding to the next stage. Stage validity is product-specific and this stage may not be applicable to this product.
12	0h RO/V	**Stage4 Pcode Reset Complete (PCODE_INIT_DONE4):** Pcode sets this bit when it has completed this stage, BIOS must wait for this bit to be set before proceeding to the next stage. Stage validity is product-specific and this stage may not be applicable to this product.
11	0h RO/V	**Stage3 Pcode Reset Complete (PCODE_INIT_DONE3):** Pcode sets this bit when it has completed this stage, BIOS must wait for this bit to be set before proceeding to the next stage. Stage validity is product-specific and this stage may not be applicable to this product.
10	0h RO/V	**Stage2 Pcode Reset Complete (PCODE_INIT_DONE2):** Pcode sets this bit when it has completed this stage, BIOS must wait for this bit to be set before proceeding to the next stage. Stage validity is product-specific and this stage may not be applicable to this product.
9	0h RO/V	**Stage1 Pcode Reset Complete (PCODE_INIT_DONE1):** Pcode sets this bit when it has completed this stage, BIOS must wait for this bit to be set before proceeding to the next stage. Stage validity is product-specific and this stage may not be applicable to this product.
8	0h RO/V	**Stage0 Pcode Reset Complete (PCODE_INIT_DONE):** Pcode has completed its actions in response to Stage0 BIOS Reset complete. Between BIOS Stage0 complete and pcode Stage0 complete, pcode will apply all power savings configurations to PCS and will set up C_STATE_LATENCY control MSR settings for IRTL management.
7	0h RW	**Stage7 BIOS Reset Complete (RST_CPL7):** reset complete
6	0h RW	**Stage6 BIOS Reset Complete (RST_CPL6):** BIOS sets this bit when it has completed this stage, Pcode must wait for this bit to be set before proceeding to the next stage. Stage validity is product-specific and this stage may not be applicable to this product.
5	0h RW	**Stage5 BIOS Reset Complete (RST_CPL5):** BIOS sets this bit when it has completed this stage, Pcode must wait for this bit to be set before proceeding to the next stage. Stage validity is product-specific and this stage may not be applicable to this product.
4	0h RW	**Stage4 BIOS Reset Complete (RST_CPL4):** BIOS sets this bit when it has completed this stage, Pcode must wait for this bit to be set before proceeding to the next stage. Stage validity is product-specific and this stage may not be applicable to this product.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Stage3 BIOS Reset Complete (RST_CPL3):** BIOS sets this bit when it has completed this stage, Pcode must wait for this bit to be set before proceeding to the next stage. Stage validity is product-specific and this stage may not be applicable to this product.
2	0h RW	**Stage2 BIOS Reset Complete (RST_CPL2):** BIOS sets this bit when it has completed this stage, Pcode must wait for this bit to be set before proceeding to the next stage. Stage validity is product-specific and this stage may not be applicable to this product.
1	0h RW	**Stage1 BIOS Reset Complete (RST_CPL1):** BIOS sets this bit when it has completed this stage, Pcode must wait for this bit to be set before proceeding to the next stage. Stage validity is product-specific and this stage may not be applicable to this product.
0	0h RW	**Stage0 BIOS Reset Complete (RST_CPL):** Set by BIOS to indicate that all power management configurations as part of reset are complete. This must include Punit patch load done as well as all relevant Punit power management register and mailbox configurations done. Once this bit is set, Punit will allow normal power management to start. Before setting this bit, P-states and C-states support is disabled. BIOS should wait before receiving the Pcode Stage0 reset complete before proceeding with any further steps.

5.7.26 BIOS_MAILBOX_DATA (P_CR_BIOS_MAILBOX_DATA_0_0_0_MCHBAR)—Offset 7080h

Data register for the BIOStoPCODE mailbox. This mailbox is implemented as a means for accessing statistics and implementing BIOS-Pcode handshakes. This register is used in conjunction with BIOS_MAILBOX_INTERFACE. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**DATA (DATA):** This field contains the data associated with specific commands.

5.7.27 BIOS_MAILBOX_INTERFACE (P_CR_BIOS_MAILBOX_INTERFACE_0_0_0_MCHBAR)—Offset 7084h

Control and Status register for the BIOStoPCODE mailbox. This mailbox is implemented as a means for accessing statistics and implementing BIOS-Pcode handshakes. This register is used in conjunction with BIOS_MAILBOX_DATA. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**RUN_BUSY (RUN_BUSY):** SW may write to the two mailbox registers only when RUN_BUSY is clear(0). Setting RUN_BUSY to 1 will pend a Fast Path event to Pcode. After setting this bit SW will poll this bit until it is cleared. PCODE will clear RUN_BUSY after updating the mailbox registers with the result and error code.
30:29	0h RO	Reserved.
28:8	0h RW/V	**ADDRESS (ADDRESS):** This field is used to specify an additional parameter to extend the command when needed.
7:0	0h RW/V	**COMMAND (COMMAND):** This field contains the SW request command or the PCODE response code depending on the setting of RUN_BUSY.

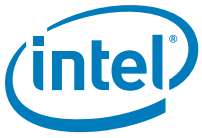
5.7.28 CORE_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_CORE_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 7088h

PUNIT_MMIO: Core Frequency Capabilities
This register describes the frequency capabilities of the IA cores. Units are 100MHz multiplied by the ratio.
Minimum and maximum ratio fields are initialized by pCode at reset. Last resolved ratio is updated upon changes to the processing system frequency. The efficient ratio is determined by firmware and may be updated dynamically depending on firmware support.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LAST_RESOLVED_FREQ (LAST_RESOLVED_FREQ):** Last resolved ratio for the IA cores. Units are 100MHz multiplied by the ratio. This value is updated dynamically whenever the IA core frequency changes.
23:16	0h RO/V	**MAX_SUPPORTED_FREQ (MAX_SUPPORTED_FREQ):** Maximum ratio for the IA cores. Units are 100MHz multiplied by the ratio.
15:8	0h RO/V	**EFFICIENT_FREQ (EFFICIENT_FREQ):** Firmware-calculated efficient ratio for the IA cores. Units are 100MHz multiplied by the ratio.
7:0	0h RO/V	**MIN_SUPPORTED_FREQ (MIN_SUPPORTED_FREQ):** Minimum supported ratio for the IA cores. Units are 100MHz multiplied by the ratio.

5.7.29 GRAPHICS_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_GRAPHICS_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 708Ch

PUNIT_MMIO: Graphics Engine Frequency Capabilities
This register describes the frequency capabilities of the integrated graphics engine. Units are 50MHz multiplied by the ratio.
Minimum and maximum ratio fields are initialized by pCode at reset. Last resolved ratio is updated upon changes to the integrated graphics engine frequency. The efficient ratio is determined by firmware and may be updated dynamically depending on firmware support.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LAST_RESOLVED_FREQ (LAST_RESOLVED_FREQ):** Last resolved ratio for the integrated graphics engine. Units are 50MHz multiplied by the ratio. This value is updated dynamically whenever the graphics engine frequency changes.
23:16	0h RO/V	**MAX_SUPPORTED_FREQ (MAX_SUPPORTED_FREQ):** Maximum supported ratio for the integrated graphics engine. Units are 50MHz multiplied by the ratio.
15:8	0h RO/V	**EFFICIENT_FREQ (EFFICIENT_FREQ):** Firmware-calculated efficient ratio for the integrated graphics engine. Units are 50MHz multiplied by the ratio.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO/V	**MIN_SUPPORTED_FREQ (MIN_SUPPORTED_FREQ):** Minimum supported ratio for the integrated graphics engine. Units are 50MHz multiplied by the ratio.

5.7.30 SYSTEM_AGENT_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_SYSTEM_AGENT_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 7090h

PUNIT_MMIO: System Agent Frequency Capabilities
This register describes the frequency capabilities of the System Agent. Units are 16.666MHz multiplied by the ratio.
Last resolved ratio is updated upon changes to the System Agent frequency.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LAST_RESOLVED_RATIO (LAST_RESOLVED_RATIO):** Last resolved System Agent ratio, in units of 16.666MHz.
23:16	0h RO/V	**RESERVED_2 (RESERVED_2):** Reserved
15:8	0h RO/V	**RESERVED_1 (RESERVED_1):** Reserved
7:0	0h RO/V	**RESERVED_0 (RESERVED_0):** Reserved

5.7.31 Memory Frequency Status (P_CR_FAR_MEMORY_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 7094h

This register reports out the LPDDR memory frequency. The actual capabilities of the SOC with respect to LPDDR frequency is described in the MEMSS_FREQUENCY_CAPABILITIES register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Last Resolved Memory Frequency (LAST_RESOLVED_RATIO):** This field reports out the LPDDR memory frequency in integer multiple of 133.33MHz. This register reflects what BIOS has programmed as the default LPDDR frequency in products that do not support run-time memory frequency control. For products supporting run-time memory frequency control, this field describes the last resolved frequency.
23:16	0h RO/V	**RESERVED_2 (RESERVED_2):** Reserved
15:8	0h RO/V	**RESERVED_1 (RESERVED_1):** Reserved
7:0	0h RO/V	**RESERVED_0 (RESERVED_0):** Reserved

5.7.32 Package Power SKU and RAPL Power Control Capabilities (P_CR_PACKAGE_POWER_SKU_0_0_0_MCHBAR)—Offset 70A0h

This register describes the the power SKU of the part and limits on time window and power limit configuration allowed in the RAPL PL1 and PL2 configuration registers.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 12024000600118h

Bit Range	Default & Access	Field Name (ID): Description
63:55	0h RO	**RESERVED_3 (RESERVED_3):** Reserved
54:48	12h RW	**RAPL Maximum Allowed Time Window (PKG_MAX_WIN):** The maximal time window allowed to be programmed for RAPL PL1 and PL2 controls for the SKU. Higher values will be clamped to this value. The bits of this field describe parameters for a mathematical equation for time window configuration. This field is split into two sub-fields: • x = bits[6:5] • y = bits[4:0] Time window equation: **time_window = PACKAGE_POWER_SKU_UNIT.TIME_UNIT * ((1+x/4)^y)**
47	0h RO	**RESERVED_2 (RESERVED_2):** Reserved
46:32	240h RW	**RAPL Maximum Power Limit (PKG_MAX_PWR):** The maximal package power setting allowed for the SKU. Higher values will be clamped to this value. The maximum setting is typical not guaranteed. The default value for this field is determined by fuses. The units for this value are defined in PACKAGE_POWER_SKU_MSR[PWR_UNIT].

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**RESERVED_1 (RESERVED_1):** Reserved
30:16	60h RW	**Package Minimum Power (PKG_MIN_PWR):** The minimal package power setting allowed for the SKU. Lower values may not be achievable by run-time RAPL PL1 and PL2 control algorithms.
15	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
14:0	118h RW	**PKG_TDP (PKG_TDP):** The TDP package power setting allowed for the SKU. The TDP setting is typical not guaranteed. The default value for this field is determined by fuses. The units for this value are defined in PACKAGE_POWER_SKU_MSR[PWR_UNIT].

5.7.33 Package RAPL Power Limit (P_CR_PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR)—Offset 70A8h

Package RAPL Power Limit allows a software agent to define power limitation for the package domain. Power limitation is defined in terms of average power usage (Watts) over a time window specified. Two power limits and associated time windows can be specified. These power limits are commonly referred to as PL1 (long time window) and PL2 (short time window). Each power limit provides independent clamping control that would permit the processor cores to go below OS-requested state to meet the power limits. A lock mechanism allow the software agent to enforce power limit settings. Once the lock bit is set, the power limit settings are static and un-modifiable until next RESET.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/L	**Package RAPL Lock (PKG_PWR_LIM_LOCK):** When set all settings in this register are locked and are treated as Read Only. This lock control is persistent until the next reset. This bit will typically set by BIOS during boot time or resume from Sx.
62:56	0h RSV	**RESERVED_1 (RESERVED_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
55:49	0h RW/L	**Power Limit 2 (PL2) Time Window (PKG_PWR_LIM_2_TIME):** Time window for Power Limit 1 (PL2). This describes the control window of the power limit. This time window is described in an RC time constant format, which means that if 1s is programmed, the power limit constraint really applies at more like 5s. The maximal time window is bounded by PACKAGE_POWER_SKU_MSR.PKG_MAX_WIN. Thre is no constraint on the minimum programmable time window, however at very short time windows the control algorithms may not be effective. The bits of this field describe parameters for a mathematical equation for time window configuration. This field is split into two sub-fields: • x = bits[6:5] • y = bits[4:0] Time window equation: **time_window = PACKAGE_POWER_SKU_UNIT.TIME_UNIT * ((1+x/4)^y)**
48	0h RW/L	**Power Limit 2 (PL2) Clamp (PKG_CLMP_LIM_2):** Clamp mode control for PL2. • 0 = PL2 power control is prevented from forcing P-states below the base frequency / P1 for any domain in the SOC. • 1 = PL2 power control will take all actions necessary to meet the power target, even if that involves running at clock frequencies below the base frequency / P1 level. In order to ensure proper SOC cooling, it is generally recommended that the clamp mode is always enabled.
47	0h RW/L	**Power Limit 2 (PL2) Enable (PKG_PWR_LIM_2_EN):** Enable for Power Limit 2 (PL2). Setting this bit activates the power limit and time window defined for PL2.
46:32	0h RW/L	**Power Limit 2 (PL2) (PKG_PWR_LIM_2):** Sets the average power usage limit of the package domain corresponding to the PL2 time window. The power units of this field are specified by the PACKAGE_POWER_SKU_UNIT_MSR.PWR_UNIT. This power limit must be configured by software before it will engage. The PL2 limit is most commonly associated with long time windows (1s and longer), although there are no explicit constraints on what software configures.
31:24	0h RSV	**RESERVED_0 (RESERVED_0):** Reserved
23:17	0h RW/L	**Power Limit 1 (PL1) Time Window (PKG_PWR_LIM_1_TIME):** Time window for Power Limit 1 (PL1). This describes the control window of the power limit. This time window is described in an RC time constant format, which means that if 1s is programmed, the power limit constraint really applies at more like 5s. The maximal time window is bounded by PACKAGE_POWER_SKU_MSR.PKG_MAX_WIN. Thre is no constraint on the minimum programmable time window, however at very short time windows the control algorithms may not be effective. The bits of this field describe parameters for a mathematical equation for time window configuration. This field is split into two sub-fields: • x = bits[6:5] • y = bits[4:0] Time window equation: **time_window = PACKAGE_POWER_SKU_UNIT.TIME_UNIT * ((1+x/4)^y)**

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/L	**Power Limit 1 (PL1) Clamp (PKG_CLMP_LIM_1):** Clamp mode control for PL1. • 0 = PL1 power control is prevented from forcing P-states below the base frequency / P1 for any domain in the SOC. • 1 = PL1 power control will take all actions necessary to meet the power target, even if that involves running at clock frequencies below the base frequency / P1 level. In order to ensure proper SOC cooling, it is generally recommended that the clamp mode is always enabled.
15	0h RW/L	**Power Limit 1 (PL1) Enable (PKG_PWR_LIM_1_EN):** Enable for Power Limit 1 (PL1). Setting this bit activates the power limit and time window defined for PL1.
14:0	0h RW/L	**Power Limit 1 (PL1) (PKG_PWR_LIM_1):** Sets the average power usage limit of the package domain corresponding to the PL1 time window. The power units of this field are specified by the PACKAGE_POWER_SKU_UNIT_MSR.PWR_UNIT. This power limit must be configured by software before it will engage. The PL1 limit is most commonly associated with long time windows (1s and longer), although there are no explicit constraints on what software configures.

5.7.34 IA_PERF_LIMIT_REASONS (P_CR_IA_PERF_LIMIT_REASONS_0_0_0_MCHBAR)—Offset 70B0h

This register reports reasons for performance limitations on the IA cores. Status bits are an instantaneous indication of an active constraint. Log bits indicate that a constraint was enforced since the log bit was last cleared.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/0C/V	**QOS_LOG (QOS_LOG):** Logged indication that frequency was clamped below the software-defined quality-of-service floor. This bit is set by firmware, and is clearable by software.
30	0h RW/0C/V	**MAX_EFFICIENCY_FREQ_LOG (MAX_EFFICIENCY_FREQ_LOG):** Logged indication that frequency was clamped below the firmware-calculated maximum efficiency frequency. This bit is set by firmware, and is clearable by software.
29	0h RW/0C/V	**MCT_LOG (MCT_LOG):** Logged indication that frequency was clamped due to ratio change transition attenuation. This bit is set by firmware, and is clearable by software.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RW/0C/V	**EDP_LOG (EDP_LOG):** Logged indication that frequency was clamped due to the package-level Electrical Design Point constraint. This bit is set by firmware, and is clearable by software.
27	0h RW/0C/V	**MULTI_CORE_TURBO_LOG (MULTI_CORE_TURBO_LOG):** Logged indication that frequency was clamped due to effective multi-core turbo constraints. This bit is set by firmware, and is clearable by software.
26	0h RW/0C/V	**VR_THERMALERT_LOG (VR_THERMALERT_LOG):** Logged indication that frequency was clamped due to a voltage regulator thermal excursion. This bit is set by firmware, and is clearable by software.
25	0h RW/0C/V	**IA_UTILIZATION_LOG (IA_UTILIZATION_LOG):** Logged indication that frequency was clamped due to the autonomous utilization-based P-state control algorithm. This bit is set by firmware, and is clearable by software.
24	0h RW/0C/V	**DEV3_LOG (DEV3_LOG):** Logged indication that frequency was clamped due to a Device 3 driver override. This bit is set by firmware, and is clearable by software.
23	0h RW/0C/V	**DEV2_LOG (DEV2_LOG):** Logged indication that frequency was clamped due to a Device 2 driver override. This bit is set by firmware, and is clearable by software.
22	0h RW/0C/V	**SPARE6_LOG (SPARE6_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
21	0h RW/0C/V	**SPARE5_LOG (SPARE5_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
20	0h RW/0C/V	**SPARE4_LOG (SPARE4_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
19	0h RW/0C/V	**PL2_LOG (PL2_LOG):** Logged indication that frequency was clamped due to a package-level PL2 excursion. This bit is set by firmware, and is clearable by software.
18	0h RW/0C/V	**PL1_LOG (PL1_LOG):** Logged indication that frequency was clamped due to a package-level PL1 excursion. This bit is set by firmware, and is clearable by software.
17	0h RW/0C/V	**THERMAL_LOG (THERMAL_LOG):** Logged indication that frequency was clamped due to a thermal excursion. This bit is set by firmware, and is clearable by software.
16	0h RW/0C/V	**PROCHOT_LOG (PROCHOT_LOG):** Logged indication that frequency was clamped due to PROCHOT assertion. This bit is set by firmware, and is clearable by software.
15	0h RO/V	**QOS_STATUS (QOS_STATUS):** Frequency is limited below the operating system or driver Quality-of-Service floor.
14	0h RO/V	**MAX_EFFICIENCY_FREQ_STATUS (MAX_EFFICIENCY_FREQ_STATUS):** Frequency is limited below the maximum efficiency frequency.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO/V	**MCT_STATUS (MCT_STATUS):** Frequency is limited due to ratio change transition attenuation (MCT, prevents frequent ratio changes due to core C-state entry/exit).
12	0h RO/V	**EDP_STATUS (EDP_STATUS):** Frequency is limited due to a package-level EDP constraint.
11	0h RO/V	**MULTI_CORE_TURBO_STATUS (MULTI_CORE_TURBO_STATUS):** Frequency is limited due to effective multi-core turbo constraints.
10	0h RO/V	**VR_THERMALERT_STATUS (VR_THERMALERT_STATUS):** Frequency is limited due to a VR thermal excursion.
9	0h RO/V	**IA_UTILIZATION_STATUS (IA_UTILIZATION_STATUS):** Frequency is limited due to autonomous utilization-based P-state control.
8	0h RO/V	**DEV3_STATUS (DEV3_STATUS):** Frequency is limited due to Dev3 driver override.
7	0h RO/V	**DEV2_STATUS (DEV2_STATUS):** Frequency is limited due to Dev2 driver override.
6	0h RO/V	**SPARE6_STATUS (SPARE6_STATUS):** Spare status bit.
5	0h RO/V	**SPARE5_STATUS (SPARE5_STATUS):** Spare status bit.
4	0h RO/V	**SPARE4_STATUS (SPARE4_STATUS):** Spare status bit.
3	0h RO/V	**PL2_STATUS (PL2_STATUS):** Frequency is limited due to a package-level PL2 excursion.
2	0h RO/V	**PL1_STATUS (PL1_STATUS):** Frequency is limited due to a package-level PL1 excursion.
1	0h RO/V	**THERMAL_STATUS (THERMAL_STATUS):** Frequency is limited due to thermal excursion.
0	0h RO/V	**PROCHOT_STATUS (PROCHOT_STATUS):** Frequency is limited due to external PROCHOT assertion.

5.7.35 IA Core C0 Residency Counter (P_CR_TELEM_IA_C0_RESIDENCY_0_0_0_MCHBAR)—Offset 70C0h

This counter measures time that any core is active in the C0 state. This counter counts at the crystal clock frequency divided by 16. This counter may be used along with the IA Frequency Accumulator to calculate the average active clock ratio multiplier on the IA domain. **Average Active Frequency = Frequency Accumulator / C0 Residency**

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**C0 Residency (DATA):** This counter measures time that any core is active in the C0 state. This counter counts at the crystal clock frequency divided by 16.

5.7.36 Graphics C0 Residency Counter (P_CR_TELEM_GT_C0_RESIDENCY_0_0_0_MCHBAR)—Offset 70C4h

This counter measures time that graphics is active in the C0 state. This counter counts at the crystal clock frequency divided by 16. This counter may be used along with the Graphics Frequency Accumulator to calculate the average active clock ratio multiplier on the GT domain. **Average Active Frequency = Frequency Accumulator / C0 Residency**

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**C0 Residency (DATA):** This counter measures time that graphics is active in the C0 state. This counter counts at the crystal clock frequency divided by 16.

5.7.37 I-unit Processing System C0 Residency Counter (P_CR_TELEM_IUNIT_C0_RESIDENCY_0_0_0_MCHBAR)—Offset 70C8h

This counter measures time that I-unit processing system is active in the C0 state. This counter counts at the crystal clock frequency divided by 16. This counter may be used along with the I-unit Frequency Accumulator to calculate the average active clock ratio multiplier on the I-unit domain. **Average Active Frequency = Frequency Accumulator / C0 Residency**

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**C0 Residency (DATA):** This counter measures time that I-unit processing system is active in the C0 state. This counter counts at the crystal clock frequency divided by 16.

5.7.38 TELEM_IA_FREQ_ACCUMULATOR (P_CR_TELEM_IA_FREQ_ACCUMULATOR_0_0_0_MCHBAR)—Offset 70CCh

Frequency accumulation data counted at ART >> 4

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**DATA (DATA):** Residency data

5.7.39 Graphics C0 Residency Counter (P_CR_TELEM_GT_FREQ_ACCUMULATOR_0_0_0_MCHBAR)—Offset 70D0h

This counter integrates the current clock ratio multiplier for the Graphics domain at the same rate as the corresponding C0 residency counter. Its primary utility is in assessing the average active frequency of the domain **Average Active Frequency = Frequency Accumulator / C0 Residency**

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Clock Ratio Multiplier Accumulator (DATA):** This counter integrates the current clock ratio of the domain at the same rate as the corresponding C0 residency counter

5.7.40 I-unit Processing System C0 Residency Counter (P_CR_TELEM_IUNIT_FREQ_ACCUMULATOR_0_0_0_MCHBAR)—Offset 70D4h

This counter integrates the current clock ratio multiplier for the I-unit processing system domain at the same rate as the corresponding C0 residency counter. Its primary utility is in assessing the average active frequency of the domain
Average Active Frequency = Frequency Accumulator / C0 Residency

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Clock Ratio Multiplier Accumulator (DATA):** This counter integrates the current clock ratio of the domain at the same rate as the corresponding C0 residency counter

5.7.41 Memory Active Residency (P_CR_TELEM_FAR_MEMORY_ACTIVE_0_0_0_MCHBAR)—Offset 70E8h

This counter measures the total time spent with memory active, as measured by any rank being in the active or active idle state. The inverse of this counter indicates the total time spent with all memory in the self-refresh state. This counter counts at the crystal clock frequency divided by 16.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RO/V	**DATA (DATA):** This counter measures the total time spent with memory active, as measured by any rank being in the active or active idle state. The inverse of this counter indicates the total time spent with all memory in the self-refresh state. This counter counts at the crystal clock frequency divided by 16.

5.7.42 Package Temperatures (P_CR_PACKAGE_TEMPERATURES_0_0_0_MCHBAR)—Offset 70F4h

Read-only register used for monitoring thermal status from all domains in the package.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**System Agent Temperature (SA_Temperature):** System agent domain max temperature in degrees C. Reported in a signed, 2's complement format with the LSB representing 1'C resolution (S8.7.0). Raw, unfiltered
23:16	0h RO/V	**I-unit Temperature (ISP_Temperature):** Camera domain max temperature in degrees C. Reported in a signed, 2's complement format with the LSB representing 1'C resolution (S8.7.0). Raw, unfiltered
15:8	0h RO/V	**Graphics Temperature (GT_Temperature):** Graphics domain max temperature in degrees C. Reported in a signed, 2's complement format with the LSB representing 1'C resolution (S8.7.0). Raw, unfiltered
7:0	0h RO/V	**IA Core Temperature (IA_Temperature):** Virtual max temperature of all IA cores in degrees C. Reported in a signed, 2's complement format with the LSB representing 1'C resolution (S8.7.0). Raw, unfiltered

5.7.43 Package Thermal Limit Control (P_CR_THERMAL_LIMIT_CONTROL_0_0_0_MCHBAR)—Offset 7104h

This register is used for run-time control of the package level virtual thermal sensor. This interrupt and threshold is most commonly utilized by drivers wishing to control maximum silicon temperature in order to manage local or system level thermals due to various physical constraints. This temperature configuration applies only to in-die thermal sensors and not to any DRAM related thermal control.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Enable (ENABLE):** When set, it enables run-time thermal limit control to the THERMAL_LIMIT_TEMP described in this register.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Package Thermal Limit Temperature (THERMAL_LIMIT_TEMP):** Maximum SOC temperature allowed. Described in a signed, 2's complement format with the least significant bit representing 1'C resolution (S8.7.0). If the setting is higher than the processor's factory configured maximum temperature as described in the TEMPERATURE_TARGET MSR, this field is ignored. This field may be updated at any time.

5.7.44 Memory Subsystem Frequency Capabilities (P_CR_MEMSS_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 7108h

Describes the maximum frequency capabilities of DDR supported on this particular SOC. If the maximum supported frequency reports a zero, it indicates that the respective DRAM technology is not supported on this product.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Reserved (NUM_NM_CH):** Reserved
29:24	0h RW	**Reserved (WIO_FREQ):** Reserved
23:18	0h RW	**LPDDR4 Max Frequency (LP4_FREQ_HIGH):** This field indicates maximum LPDDR4 frequency that SOC supports, in integer multiple of 133.33MHz. A value of zero indicates LPDDR4 is not supported.
17:12	0h RW	**LPDDR4 Max Frequency at Min Voltage (LP4_FREQ_LOW):** This field indicates maximum LPDDR4 frequency supported at the minimum voltage level, in integer multiple of 133.33MHz. If this frequency is the same as 'Max' frequency, it indicates there is no voltage scaling. A value of zero indicates LPDDR4 is not supported.
11:6	0h RW	**LPDDR3 Max Frequency (LP3_FREQ_HIGH):** This field indicates maximum LPDDR3 frequency that SOC supports, in integer multiple of 133.33MHz. A value of zero indicates LPDDR3 is not supported.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**LPDDR3 Max Frequency at Min Voltage (LP3_FREQ_LOW):** This field indicates maximum LPDDR3 frequency supported at the minimum voltage level, in integer multiple of 133.33MHz. If this frequency is the same as 'Max' frequency, it indicates there is no voltage scaling. A value of zero indicates LPDDR3 is not supported.

5.7.45 Memory Controller (MC) BIOS Reset Request and Status (P_CR_MC_BIOS_REQ_0_0_0_MCHBAR)—Offset 7114h

This register is used as the primary interface between BIOS and P-unit with respect to the Memory sub-system reset flow. This register provides both details about the current memory configuration as well as memory power-up sequencing controls. The typical memory subsystem reset and configuration flow is as follows. Each bullet describes the strict sequential ordering of the flow.

- BIOS reads MEMSS_FREQUENCY_CAPABILITIES to discover silicon capabilities.
- BIOS detects LPDDR DRAM frequency and the number of LPDDR channels that have DRAM devices attached. These results are then configured into the LPDDR channel active and frequency configuration fields.
- BIOS discovers if DRAM is currently in self-refresh, and if so, it configures Request Type (REQ_TYPE) to 100b to indicate this state. The SOC then uses this information as a way to ensure proper self-refresh exit flows as part of power-up sequencing.
- Once the lower 16 bits of the MC_BIOS_REQ register are configured based on platform discovery, BIOS sets Run/Busy to initiate firmware to start the memory subsystem reset sequence.
- P-unit firmware executes the initial configuration of PHY settings, and when complete it clears Run/Busy bit
- BIOS executes DDR PHY static configuration flow and initializes PHY PLL, and ensures that both steps are complete
- BIOS sets MC_BIOS_REQ.PHY_CONFIG_COMPLETE and MC_BIOS_REQ.RUN_BUSY to start the next phase
- P-unit firmware initiates the power-up sequence for D-units and Wide I/O collateral logic.
- P-unit firmware sets MC_BIOS_REQ.DUNIT_RESET_COMPLETE and clears the Run/Busy when it is done.
- BIOS observes Run/Busy deassertion and continues with MRC flow to initialize, train, configure memory subsystem settings.
- BIOS sets MC_BIOS_REQ.CPGC_MODE_COMPLETE and MC_BIOS_REQ.RUN_BUSY to start the next phase
- P-unit firmware configures D-unit, PHY to support normal operation of memory subsystem, and when completed, clears the Run/Busy bit
- BIOS waits for MC_BIOS_REQ.RUN_BUSY to clear, and then complete remaining configuration of Dunit and MLMC.
- BIOS executes memory configuration validation and lock sequence with the CSE.
- BIOS sets MC_BIOS_REQ.MEM_INIT_DONE and MC_BIOS_REQ.RUN_BUSY to indicate to Punit that all memory configuration is complete and memory configuration is locked.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Run/Busy (RUN_BUSY):** This bit indicates that the BIOS request is pending for P-unit firmware processing. BIOS sets this bit together with command details defined in the lower bits of this register. Firmware may only clear this bit after the BIOS request has been observed and completed. • 0 = The MC BIOS reset mailbox is idle or the last request has been completed. Software may initiate new requests. • 1 = The MC BIOS reset mailbox is busy. It is still handling a request. Writes to the mailbox are not allowed at this time.
30:27	0h RW	**RESERVED_2 (RESERVED_2):** reserved
26:24	0h RW	**DRAM_TYPE (DRAM_TYPE):** BIOS programs DRAM type filed: • 001b = LPDDR3 • 010b = LPDDR4 • 100b = DDR3L • else = reserved
23:20	0h RW	**RESERVED_1 (RESERVED_1):** reserved
19	0h RW	**Memory Init Done (MEM_INIT_DONE):** BIOS programs this bit after memory subsystem is fully configured, including security locking configuration completed
18	0h RW	**CPGC Mode Complete (CPGC_MODE_COMPLETE):** BIOS programs this bit after the memory train/init flow is complete. This initiates P-unit firmware execution of memory and D-unit clock configuration settings for normal operation
17	0h RW	**D-unit Reset Complete (DUNIT_RESET_COMPLETE):** Punit programs this bit after memory subsystem IPs are powered and corresponding reset flows are complete. At this point, those blocks are ready for executing the memory training flow, including intialization to support CPGC mode. BIOS can talk to Dunit after this.
16	0h RW	**Memory PHY Configuration Complete (PHY_CONFIG_COMPLETE):** BIOS programs this bit indicating PHY initial configuration is complete and all DDR PHY PLLs are locked. Upon observation of this flag, P-unit firmware will initiate the power-up sequence of memory subsystem related IPs

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**DDR Channel 11 Active (FM_CH3_ACTIVE):** BIOS writes this value to indicate a DDR memory channel has DRAM devices active to allow the channel to have active memory traffic. Note, by default, a channel is not active and BIOS needs to explicitly program a value of 1 to indicate that the channel is active. If a channel is fused off on a particular SOC, BIOS input is ignored: • 0 = channel not active • 1 = channel active
14	0h RW	**DDR Channel 00 Active (FM_CH2_ACTIVE):** BIOS writes this value to indicate a DDR memory channel has DRAM devices active to allow the channel to have active memory traffic. Note, by default, a channel is not active and BIOS needs to explicitly program a value of 1 to indicate that the channel is active. If a channel is fused off on a particular SOC, BIOS input is ignored: • 0 = channel not active • 1 = channel active
13	0h RW	**DDR Channel 10 Active (FM_CH1_ACTIVE):** BIOS writes this value to indicate a DDR memory channel has DRAM devices active to allow the channel to have active memory traffic. Note, by default, a channel is not active and BIOS needs to explicitly program a value of 1 to indicate that the channel is active. If a channel is fused off on a particular SOC, BIOS input is ignored: • 0 = channel not active • 1 = channel active
12	0h RW	**DDR Channel 01 Active (FM_CH0_ACTIVE):** BIOS writes this value to indicate a DDR memory channel has DRAM devices active to allow the channel to have active memory traffic. Note, by default, a channel is not active and BIOS needs to explicitly program a value of 1 to indicate that the channel is active. If a channel is fused off on a particular SOC, BIOS input is ignored: • 0 = channel not active • 1 = channel active
11	0h RW	**RESERVED_2 (WIO_ONLY):** Reserved
10	0h RW	**RESERVED_0 (RESERVED_0):** reserved
9	0h RW	**RESERVED_3 (REQ_TYPE_SPECIAL):** reserved
8:6	0h RW	**Request Type (REQ_TYPE):** This field is used to configure reset hints to the P-unit firmware. Encodings include: • 1xxb = Memory is in self-refresh, manual self-refresh exit is required • 0xxb = Memory is not in self-refresh or DRAM contents do not need to be preserved.
5:0	0h RW	**DDR Frequency Configuration (REQ_DATA):** BIOS programs this field to request DDR frequency in integer multiple of 133.33MHz. BIOS reads MEMSS_FREQUENCY_CAPABILITIES register(s) to discover maximum SOC supported capabilities. And BIOS is expected to request only legal DDR frequencies that are equal or lower than the maximum SOC supported capabilities.

5.7.46 MEMSS_FREQUENCY_CAPABILITIES1 (P_CR_MEMSS_FREQUENCY_CAPABILITIES1_0_0_0_MCHBAR)—Offset 7118h

Describes the maximum frequency capabilities of DDR supported and DDR configuration on this particular SOC. If the maximum supported frequency reports a zero, it indicates that the respective DRAM technology is not supported on this product.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RW	**RESERVED_2 (RESERVED_2):** reserved
24	0h RW	**DDR_CONFIG_LIMITATION (DDR_CONFIG_LIMITATION):** Describe the DDR configuration limitation of this particular SOC: • 0 = no DDR configuration limitation • 1 = DDR configuration is limited to1ch x 64-bit DDR3L, or 2ch x32 LPDDR3 or LPDDR4
23:12	0h RW	**RESERVED_1 (RESERVED_1):** reserved
11:6	0h RW	**DDR3L Max Frequency (DDR3L_FREQ_HIGH):** This field indicates maximum DDR3L frequency that SOC supports, in integer multiple of 133.33MHz. A value of zero indicates DDR3L is not supported.
5:0	0h RW	**DDR3L Max Frequency at Min Voltage (DDR3L_FREQ_LOW):** This field indicates maximum DDR3L frequency supported at the minimum voltage level, in integer multiple of 133.33MHz. If this frequency is the same as 'Max' frequency, it indicates there is no voltage scaling. A value of zero indicates LPDDR4 is not supported.

5.7.47 PP1_C0_CORE_CLOCK_0_0_0_MCHBAR (P_CR_PP1_C0_CORE_CLOCK_0_0_0_MCHBAR)—Offset 7160h

GT RC0 residency counter. Holds the accumulated number of CS clks that GT has been in RC0.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**DATA (DATA):** Accumulated cycles GT has been in RC0.

5.7.48 Core Exists Vector (P_CR_CORE_EXISTS_VECTOR_0_0_0_MCHBAR)—Offset 7164h

Indication of the physical presence of IA cores in this silicon. IA core modules are defined as containing pairs of cores and an associated L2 cache. Module existence can therefore be inferred by OR'ing pairs of COREx_EXISTS in this register. This register does not reflect the impact of any software-based core disabling. It always reflects the capabilities of the silicon.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RW	**CORE3_EXISTS (CORE3_EXISTS):** Indication of core physical presence
2	0h RW	**CORE2_EXISTS (CORE2_EXISTS):** Indication of core physical presence
1	0h RW	**CORE1_EXISTS (CORE1_EXISTS):** Indication of core physical presence
0	0h RW	**CORE0_EXISTS (CORE0_EXISTS):** Indication of core physical presence

5.7.49 Software Core Disable Mask (P_CR_CORE_DISABLE_MASK_0_0_0_MCHBAR)—Offset 7168h

Software may disable cores using this interface. The bit definition of this register exactly matches that defined in the CORE_EXISTS_VECTOR register. Punit firmware will apply the mask programmed into this register against the CORE_EXISTS_VECTOR to establish the resolved cores and modules to power up after a cold reset. The flow is as follows:

- Cold boot
- BIOS reads CORE_EXISTS_VECTOR to establish which modules and cores are present
- BIOS writes 1b to the corresponding core that it wishes to **disable**.
- BIOS may disable entire modules by writing 1b to a pair of cores.

- The results of the configuration are maintained in the sustain power well.
- BIOS initiates a cold reset flow at the platform. In a cold reset, the sustain power well maintains power most other rails are power cycled.
- On cold reset exit, Punit firmware inspects the core configuration and launches only the cores requested by BIOS. To software, it will appear as if these cores do not exist.

Software may discover the resolved core exists vector: resolved_core_exists_vector = (!CORE_DISABLE_MASK) & CORE_EXISTS_VECTOR

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RW	**CORE3_DISABLE_MASK (CORE3_DISABLE_MASK):** core3 disable mask
2	0h RW	**CORE2_DISABLE_MASK (CORE2_DISABLE_MASK):** core2 disable mask
1	0h RW	**CORE1_DISABLE_MASK (CORE1_DISABLE_MASK):** core1 disable mask
0	0h RW	**CORE0_DISABLE_MASK (CORE0_DISABLE_MASK):** core0 disable mask

5.7.50 PL3 and PL4 Control (P_CR_PL3_CONTROL_0_0_0_MCHBAR)—Offset 71F0h

Control Power Limit 3 (PL3) and Power Limit 4 (PL4) using this register. This limit control is physically different from the same control in the IA core MSR space.

- PL3 is designed to clamp peak sustained power to levels supported by the battery or input power supply and as such manage lifetime degradation of that power delivery element. With PL3, peak power excursions above the limit are allowed so long as they do not exceed the configured duty cycle constraint in this register.
- PL4 is designed to clamp peak instantaneous power to levels below the max supported by the battery or input power supply. These clamps are implemented a priori and the SOC is guaranteed to constrain itself below the PL4 limit always.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/L	**Lock (LOCK):** Write a 1b to lock this register until next reset. Once locked, no further updates may be written to any bits in the register.
62:48	0h RO	Reserved.
47	0h RW/L	**PL4 Enable (PL4_ENABLE):** • 0 = disabled • 1 = enabled
46:32	0h RW/L	**PL4 Max Power (PMAX):** Power Limit 'PL4' or Pmax power limit in the units as described PACAKGE_POWER_SKU_UNIT MSR. The SOC guarantees it will never exceed this power limit even for very short time windows.
31	0h RO	Reserved.
30:24	0h RW/L	**PL3 Duty Cycle (DUTY_CYCLE):** Power limit excursion duty cycle control for PL3, describing what percentage of time it is allowed for the SOC to exceed the programmed PL3 power limit. 0% implies excursions are not supported ever and 100% implies excursions are always allowed (effectively disabling the feature). Units are in percentage(%). E.g., to allow for 20% excursion time and 80% PL3 power limit clamp time, program a value of 14h. Values greater than 100 (64h) are clipped to 100%.
23:17	0h RW/L	**PL3 Time Window (TIME_WINDOW):** Duration over which duty cycle control will be maintained. The bits of this field describe parameters for a mathematical equation for time window configuration. This time window is strictly adhered to, if the window described is 40ms, then silicon guarantees no excursions to the programmed duty cycle within a rolling 40ms window. This field is split into two sub-fields: • x = bits[6:5] • y = bits[4:0] Time window equation: **time_window = PACKAGE_POWER_SKU_UNIT.TIME_UNIT * ((1+x/4)^y)**
16	0h RO	Reserved.
15	0h RW/L	**PL3 Enable (PL3_ENABLE):** • 0 = disabled • 1 = enabled
14:0	0h RW/L	**PL3 Power Limit (POWER_LIMIT):** Power Limit 3 (PL3) or PAppMax power level. Any SOC power measurement observed above this level is considered as an excursion against the PL3 power limit and duty cycle / time window budget. Units of this power limit are defined by PACKAGE_POWER_SKU_UNIT_MSR.PWR_UNIT.

5.7.51 Graphics Superqueue Active Clocks (P_CR_PP1_ANY_THREAD_ACTIVITY_0_0_0_MCHBAR)—Offset 7244h

Graphics Superqueue active residency counter. Counts at the crystal clock frequency divided by 16.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Superqueue Active Residency (SUPERQUEUE_ACTIVE_RESIDENCY):** Graphics Superqueue active residency counter. Counts in crystal reference clocks divided by 16.

5.7.52 LPDDR DRAM Thermal (MR4) Status of Channel 00 (P_CR_MEM_MR4_TEMPERATURE_DEV3_0_0_0_MCHBAR)—Offset 7248h

LPDDR DRAM Thermal (MR4) Status of Channel 00, when there are multiple DRAMs in a rank, the maximum MR4 is reported

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
5:3	0h RW	**MR4 DRAM thermal status of Channel 00 Rank 1 (MR4_RANK_1):** This field is updated each read of LPDDR DRAM MR4 Device Temperature Status per rank. Update rate is configured by BIOS.
2:0	0h RW	**MR4 DRAM thermal status of Channel 00 Rank 0 (MR4_RANK_0):** This field is updated each read of LPDDR DRAM MR4 Device Temperature Status per rank. Update rate is configured by BIOS.

5.7.53 LPDDR DRAM Thermal (MR4) Status of Channel 11 (P_CR_MEM_MR4_TEMPERATURE_DEV4_0_0_0_MCHBAR)—Offset 724Ch

LPDDR DRAM Thermal (MR4) Status of Channel 11, when there are multiple DRAMs in a rank, the maximum MR4 is reported

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
5:3	0h RW	**MR4 DRAM thermal status of Channel 11 Rank 1 (MR4_RANK_1):** This field is updated each read of LPDDR DRAM MR4 Device Temperature Status per rank. Update rate is configured by BIOS.
2:0	0h RW	**MR4 DRAM thermal status of Channel 11 Rank 0 (MR4_RANK_0):** This field is updated each read of LPDDR DRAM MR4 Device Temperature Status per rank. Update rate is configured by BIOS.

5.8 Registers Summary

Table 5-8. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6400h	6403h	Upstream Device Arbiter Grant Count A2T (A_CR_UPARB_GCNT_DEV_A2T_MCHBAR)—Offset 6400h	1010101h
6404h	6407h	Upstream A2B Arbiter Channel 0 Grant Count (A_CR_UPARB_GCNT_A2B_0_MCHBAR)—Offset 6404h	1010101h
6408h	640Bh	Upstream A2B Arbiter Channel 1 Grant Count (A_CR_UPARB_GCNT_A2B_1_MCHBAR)—Offset 6408h	1010101h
640Ch	640Fh	Upstream A2B Arbiter Channel 2 Grant Count (A_CR_UPARB_GCNT_A2B_2_MCHBAR)—Offset 640Ch	1000100h
6410h	6413h	Upstream A2B Arbiter Channel 3 Grant Count (A_CR_UPARB_GCNT_A2B_3_MCHBAR)—Offset 6410h	1010101h
6414h	6417h	Upstream A2B Arbiter Channel 4 Grant Count (A_CR_UPARB_GCNT_A2B_4_MCHBAR)—Offset 6414h	1000100h
6418h	641Bh	Upstream A2B Arbiter Channel 5 Grant Count (A_CR_UPARB_GCNT_A2B_5_MCHBAR)—Offset 6418h	1000101h
641Ch	641Fh	Upstream A2B Arbiter Channel 6 Grant Count (A_CR_UPARB_GCNT_A2B_6_MCHBAR)—Offset 641Ch	1000101h
6420h	6423h	Upstream A2B Arbiter Channel 7 Grant Count (A_CR_UPARB_GCNT_A2B_7_MCHBAR)—Offset 6420h	1000101h

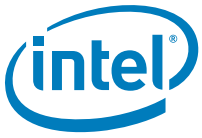


Table 5-8. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6424h	6427h	Upstream A2T Arbiter Channel 0 Grant Count (A_CR_UPARB_GCNT_A2T_0_MCHBAR)—Offset 6424h	1000101h
6428h	642Bh	Upstream P2P Arbiter Channel 0 Grant Count (A_CR_UPARB_GCNT_P2P_0_MCHBAR)—Offset 6428h	1010101h
642Ch	642Fh	Upstream P2P Arbiter Channel 1 Grant Count (A_CR_UPARB_GCNT_P2P_1_MCHBAR)—Offset 642Ch	1010101h
6430h	6433h	Upstream Private Credit Return Grant Count Posted 0 (A_CR_CRDARB_PRIV_GCNT_DEV_P_0_MCHBAR)—Offset 6430h	1000101h
6434h	6437h	Upstream Private Credit Return Grant Count Posted 1 (A_CR_CRDARB_PRIV_GCNT_DEV_P_1_MCHBAR)—Offset 6434h	1010100h
6438h	643Bh	Upstream Private Credit Return Grant Count Non-posted 0 (A_CR_CRDARB_PRIV_GCNT_DEV_N_0_MCHBAR)—Offset 6438h	1010101h
643Ch	643Fh	Upstream Private Credit Return Grant Count Posted 1 (A_CR_CRDARB_PRIV_GCNT_DEV_N_1_MCHBAR)—Offset 643Ch	1040104h
6440h	6443h	Upstream Private Credit Return Grant Count Completion (A_CR_CRDARB_PRIV_GCNT_DEV_C_0_MCHBAR)—Offset 6440h	101h
6444h	6447h	Upstream Shared Credit Return Grant Count Posted 0 (A_CR_CRDARB_SHRD_GCNT_DEV_P_0_MCHBAR)—Offset 6444h	1000101h
6448h	644Bh	Upstream Shared Credit Return Grant Count Posted 1 (A_CR_CRDARB_SHRD_GCNT_DEV_P_1_MCHBAR)—Offset 6448h	1010100h
644Ch	644Fh	Upstream Shared Credit Return Grant Count Non-posted 0 (A_CR_CRDARB_SHRD_GCNT_DEV_N_0_MCHBAR)—Offset 644Ch	1010101h
6450h	6453h	Upstream Shared Credit Return Grant Count Posted 1 (A_CR_CRDARB_SHRD_GCNT_DEV_N_1_MCHBAR)—Offset 6450h	1040104h
6454h	6457h	Upstream Shared Credit Return Grant Count Completion (A_CR_CRDARB_SHRD_GCNT_DEV_C_0_MCHBAR)—Offset 6454h	101h
6458h	645Bh	Upstream Credit Arbiter Private Credit Return Class Arbiter Grant Count (A_CR_CRDARB_PRIV_GCNT_CLS_MCHBAR)—Offset 6458h	10101h
645Ch	645Fh	Upstream Credit Arbiter Shared Cedit Return Class Arbiter Grant Count (A_CR_CRDARB_SHRD_GCNT_CLS_MCHBAR)—Offset 645Ch	10101h
6460h	6463h	Gazelle Queue Limit Channel 0-3 (A_CR_GZLQ_LIMIT_CH0_3_MCHBAR)—Offset 6460h	FFFFFFFFh
6464h	6467h	Gazelle Queue Limit Channels 4-7 (A_CR_GZLQ_LIMIT_CH4_7_MCHBAR)—Offset 6464h	FFFFFFFFh
6468h	646Bh	IOMMU Arbiter Grant Count VC0a Register (A_CR_IOMMUARB_GCNT_VC0a_0_0_0_MCHBAR)—Offset 6468h	10101h
646Ch	646Fh	IOMMU Arbiter Grant Count VC0b Register (A_CR_IOMMUARB_GCNT_VC0b_0_0_0_MCHBAR)—Offset 646Ch	10101h
6470h	6473h	IOMMU Arbiter Grant Count VC1b Register (A_CR_IOMMUARB_GCNT_VC1b_0_0_0_MCHBAR)—Offset 6470h	10101h

Table 5-8. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6474h	6477h	Gazelle Queue Reserved Entries Channels 0-3 (A_CR_GZLQ_RSVD_CH0_3_MCHBAR)—Offset 6474h	4040101h
6478h	647Bh	Gazelle Queue Reserved Entries Channels 4-7 (A_CR_GZLQ_RSVD_CH4_7_MCHBAR)—Offset 6478h	1010101h
647Ch	647Fh	Spare BIOS (A_CR_SPARE_BIOS_MCHBAR)—Offset 647Ch	0h
6490h	6493h	Upcmd Credit Maximum Channel 0 (A_CR_UPCMD_CRDTMAX_CH0_0_0_0_MCHBAR)—Offset 6490h	4040Ch
6494h	6497h	Upcmd Credit Maximum Channel 1 (A_CR_UPCMD_CRDTMAX_CH1_0_0_0_MCHBAR)—Offset 6494h	40404h
6498h	649Bh	Upcmd Credit Maximum Channel 2 (A_CR_UPCMD_CRDTMAX_CH2_0_0_0_MCHBAR)—Offset 6498h	7F00h
649Ch	649Fh	Upcmd Credit Maximum Channel 3 (A_CR_UPCMD_CRDTMAX_CH3_0_0_0_MCHBAR)—Offset 649Ch	7F7Fh
64A0h	64A3h	Upcmd Credit Maximum Channel 4 (A_CR_UPCMD_CRDTMAX_CH4_0_0_0_MCHBAR)—Offset 64A0h	400h
64A4h	64A7h	Upcmd Credit Maximum Channel 5 (A_CR_UPCMD_CRDTMAX_CH5_0_0_0_MCHBAR)—Offset 64A4h	404h
64A8h	64ABh	Upcmd Credit Maximum Channel 6 (A_CR_UPCMD_CRDTMAX_CH6_0_0_0_MCHBAR)—Offset 64A8h	404h
64ACh	64AFh	Upcmd Credit Maximum Channel 7 (A_CR_UPCMD_CRDTMAX_CH7_0_0_0_MCHBAR)—Offset 64ACh	40Ch
64C0h	64C3h	MOT OUT Base Register (A_CR_MOT_OUT_BASE_0_0_0_MCHBAR)—Offset 64C0h	0h
64C4h	64C7h	MOT OUT Mask Register (A_CR_MOT_OUT_MASK_0_0_0_MCHBAR)—Offset 64C4h	0h
64C8h	64CFh	A-Unit BIOSWR Control Policy (A_CR_BIOSWR_CP_0_0_0_MCHBAR)—Offset 64C8h	40061010202h
64D0h	64D7h	A-Unit BIOSWR Ready Access Control (A_CR_BIOSWR_RAC_0_0_0_MCHBAR)—Offset 64D0h	80000C0063010217h
64D8h	64DFh	BIOSWR Write Access Control (A_CR_BIOSWR_WAC_0_0_0_MCHBAR)—Offset 64D8h	C0061000212h
64E0h	64E7h	AUnit Pcode/Ucode Write, All Read Control Policy Register (A_CR_P_U_CODEWR_ALLRD_CP_0_0_0_MCHBAR)—Offset 64E0h	40001000202h
64E8h	64EFh	AUnit Pcode/Ucode Write, All Read Read Access Control Policy Register (A_CR_P_U_CODEWR_ALLRD_RAC_0_0_0_MCHBAR)—Offset 64E8h	FFFFFFFFFFFFFFFFh
64F0h	64F7h	AUnit Pcode/Ucode Write, All Read Write Access Control Policy Register (A_CR_P_U_CODEWR_ALLRD_WAC_0_0_0_MCHBAR)—Offset 64F0h	40001000202h
6500h	6503h	CHAP Select 1 (A_CR_CHAP_SLCT1_MCHBAR)—Offset 6500h	0h
6504h	6507h	CHAP Select 2 (A_CR_CHAP_SLCT2_MCHBAR)—Offset 6504h	0h
6508h	650Bh	CHAP Select 3 (A_CR_CHAP_SLCT3_MCHBAR)—Offset 6508h	4h

Table 5-8. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6510h	6517h	A_IMRGLOBAL_BM Control Policy (A_CR_IMRGLOBAL_BM_CP_0_0_0_MCHBAR)—Offset 6510h	C0061010202h
6518h	651Fh	A_IMRGLOBAL_BM Read Access Control (A_CR_IMRGLOBAL_BM_RAC_0_0_0_MCHBAR)—Offset 6518h	F0FFFF0FFFF0FFFFh
6520h	6527h	A_IMRGLOBAL_BM Write Access Control (A_CR_IMRGLOBAL_BM_WAC_0_0_0_MCHBAR)—Offset 6520h	C0061010202h
6588h	658Bh	Uncorrectable Error Status Register (A_CR_UNCERRSTS_0_0_0_MCHBAR)—Offset 6588h	0h
658Ch	658Fh	Uncorrectable Error Mask Register (A_CR_UNCERRMSK_0_0_0_MCHBAR)—Offset 658Ch	FFFFFFFFh
65C0h	65C7h	Slice and Channel Hash (A_CR_SLICE_CHANNEL_HASH_0_0_0_MCHBAR)—Offset 65C0h	3C00000000h
65C8h	65CFh	Mirror Range Register (A_CR_MIRROR_RANGE_0_0_0_MCHBAR)—Offset 65C8h	0h
65D0h	65D3h	ASYM MEM REGION 0 CONFIGURATION WITH NO INTERLEAVING (A_CR_ASYM_MEM_REGION0_0_0_0_MCHBAR)—Offset 65D0h	0h
65D4h	65D7h	ASYM MEM REGION 1 CONFIGURATION WITH NO INTERLEAVING (A_CR_ASYM_MEM_REGION1_0_0_0_MCHBAR)—Offset 65D4h	0h
65D8h	65DBh	Two-Way Asymmetric Memory Region Configuration (A_CR_ASYM_2WAY_MEM_REGION_0_0_0_MCHBAR)—Offset 65D8h	0h

5.8.1 Upstream Device Arbiter Grant Count A2T (A_CR_UPARB_GCNT_DEV_A2T_MCHBAR)—Offset 6400h

Upstream Device arbiter grant count for A-Unit to T-Unit transactions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**VC0B Completion Grant Count (VC0B_C):** VC0B completion grant count to T-Unit.
23:22	0h RO	Reserved.
21:16	1h RW	**VC0B Posted Grant Count (VC0B_P):** VC0B posted transaction grant count to T-Unit. This is only for MSIs.

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:8	1h RW	**VC0A Completion Grant Count (VC0A_C):** VC0A completion grant count to T-Unit.
7:6	0h RO	Reserved.
5:0	1h RW	**VC0A Posted Grant Count (VC0A_P):** VC0A posted to T-Unit MSIs.

5.8.2 Upstream A2B Arbiter Channel 0 Grant Count (A_CR_UPARB_GCNT_A2B_0_MCHBAR)—Offset 6404h

Upstream Class/Target arbiter grant count.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 0 Target Arbiter Grant Count (CHID0_TGT):** Target arbiter grant count for the channel ID 0 class arbiter.
23:22	0h RO	Reserved.
21:16	1h RW	**Channel ID 0 Non-posted IOMMU Grant Count (CHID0_MMU_NP):** Grant count for IOMMU non-posted transactions on channel ID 0.
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 0 Non-posted Grant Count (CHID0_NP):** Grant count for non-posted transactions on channel ID 0.
7:6	0h RO	Reserved.
5:0	1h RW	**Channel ID 0 P Grant Count (CHID0_P):** Grant count for posted transactions on channel ID 0.

5.8.3 Upstream A2B Arbiter Channel 1 Grant Count (A_CR_UPARB_GCNT_A2B_1_MCHBAR)—Offset 6408h

Upstream Class/Target arbiter grant count.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 1 Target Arbiter Grant Count (CHID1_TGT):** Target arbiter grant count for the channel ID 1 class arbiter.
23:22	0h RO	Reserved.
21:16	1h RW	**Channel ID 1 Non-posted IOMMU Grant Count (CHID1_MMU_NP):** Grant count for IOMMU non-posted transactions on channel ID 1.
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 1 Non-posted Grant Count (CHID1_NP):** Grant count for non-posted transactions on channel ID 1.
7:6	0h RO	Reserved.
5:0	1h RW	**Channel ID 1 P Grant Count (CHID1_P):** Grant count for posted transactions on channel ID 1.

5.8.4 Upstream A2B Arbiter Channel 2 Grant Count (A_CR_UPARB_GCNT_A2B_2_MCHBAR)—Offset 640Ch

Upstream Class/Target arbiter grant count.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1000100h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 2 Target Arbiter Grant Count (CHID2_TGT):** Target arbiter grant count for the channel ID 2 class arbiter.
23:22	0h RO	Reserved.
21:16	0h RO	**Channel ID 2 Non-posted IOMMU Grant Count (CHID2_MMU_NP):** Grant count for IOMMU non-posted transactions on channel ID 2.

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 2 Non-posted Grant Count (CHID2_NP):** Grant count for non-posted transactions on channel ID 2.
7:6	0h RO	Reserved.
5:0	0h RO	**Channel ID 2 P Grant Count (CHID2_P):** Grant count for posted transactions on channel ID 2.

5.8.5 Upstream A2B Arbiter Channel 3 Grant Count (A_CR_UPARB_GCNT_A2B_3_MCHBAR)—Offset 6410h

Upstream Class/Target arbiter grant count.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 3 Target Arbiter Grant Count (CHID3_TGT):** Target arbiter grant count for the channel ID 3 class arbiter.
23:22	0h RO	Reserved.
21:16	1h RW	**Channel ID 3 Non-posted IOMMU Grant Count (CHID3_MMU_NP):** Grant count for IOMMU non-posted transactions on channel ID 3.
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 3 Non-posted Grant Count (CHID3_NP):** Grant count for non-posted transactions on channel ID 3.
7:6	0h RO	Reserved.
5:0	1h RW	**Channel ID 3 P Grant Count (CHID3_P):** Grant count for posted transactions on channel ID 3.

5.8.6 Upstream A2B Arbiter Channel 4 Grant Count (A_CR_UPARB_GCNT_A2B_4_MCHBAR)—Offset 6414h

Upstream Class/Target arbiter grant count.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1000100h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 4 Target Arbiter Grant Count (CHID4_TGT):** Target arbiter grant count for the channel ID 4 class arbiter.
23:22	0h RO	Reserved.
21:16	0h RO	**Channel ID 4 Non-posted IOMMU Grant Count (CHID4_MMU_NP):** Grant count for IOMMU non-posted transactions on channel ID 4.
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 4 Non-posted Grant Count (CHID4_NP):** Grant count for non-posted transactions on channel ID 4.
7:6	0h RO	Reserved.
5:0	0h RO	**Channel ID 4 P Grant Count (CHID4_P):** Grant count for posted transactions on channel ID 4.

5.8.7 Upstream A2B Arbiter Channel 5 Grant Count (A_CR_UPARB_GCNT_A2B_5_MCHBAR)—Offset 6418h

Upstream Class/Target arbiter grant count.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1000101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 5 Target Arbiter Grant Count (CHID5_TGT):** Target arbiter grant count for the channel ID 5 class arbiter.
23:22	0h RO	Reserved.
21:16	0h RO	**Channel ID 5 Non-posted IOMMU Grant Count (CHID5_MMU_NP):** Grant count for IOMMU non-posted transactions on channel ID 5.

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 5 Non-posted Grant Count (CHID5_NP):** Grant count for non-posted transactions on channel ID 5.
7:6	0h RO	Reserved.
5:0	1h RW	**Channel ID 5 P Grant Count (CHID5_P):** Grant count for posted transactions on channel ID 5.

5.8.8 Upstream A2B Arbiter Channel 6 Grant Count (A_CR_UPARB_GCNT_A2B_6_MCHBAR)—Offset 641Ch

Upstream Class/Target arbiter grant count for A-Unit to B-Unit transactions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1000101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 6 Target Arbiter Grant Count (CHID6_TGT):** Target arbiter grant count for the channel ID 6 class arbiter.
23:22	0h RO	Reserved.
21:16	0h RO	**Channel ID 6 Non-posted IOMMU Grant Count (CHID6_MMU_NP):** Grant count for IOMMU non-posted transactions on channel ID 6.
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 6 Non-posted Grant Count (CHID6_NP):** Grant count for non-posted transactions on channel ID 6.
7:6	0h RO	Reserved.
5:0	1h RW	**Channel ID 6 P Grant Count (CHID6_P):** Grant count for posted transactions on channel ID 6.

5.8.9 Upstream A2B Arbiter Channel 7 Grant Count (A_CR_UPARB_GCNT_A2B_7_MCHBAR)—Offset 6420h

Upstream Class/Target arbiter grant count for A-Unit to B-Unit transactions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1000101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 7 Target Arbiter Grant Count (CHID7_TGT):** Target arbiter grant count for the channel ID 7 class arbiter.
23:22	0h RO	Reserved.
21:16	0h RO	**Channel ID 7 Non-posted IOMMU Grant Count (CHID7_MMU_NP):** Grant count for IOMMU non-posted transactions on channel ID 7.
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 7 Non-posted Grant Count (CHID7_NP):** Grant count for non-posted transactions on channel ID 7.
7:6	0h RO	Reserved.
5:0	1h RW	**Channel ID 7 P Grant Count (CHID7_P):** Grant count for posted transactions on channel ID 7.

5.8.10 Upstream A2T Arbiter Channel 0 Grant Count (A_CR_UPARB_GCNT_A2T_0_MCHBAR)—Offset 6424h

Upstream Class/Target arbiter grant count for A-Unit to T-Unit transactions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1000101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 0 Target Arbiter Grant Count (CHID0_TGT):** Target arbiter grant count for the channel ID 0 a2t class arbiter.
23:22	0h RO	Reserved.
21:16	0h RO	**Channel ID 0 Non-posted IOMMU Grant Count (CHID0_MMU_NP):** Grant count for IOMMU non-posted transactions on channel ID 0.

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 0 Non-posted Grant Count (CHID0_NP):** Grant count for non-posted transactions on channel ID 0.
7:6	0h RO	Reserved.
5:0	1h RW	**Channel ID 0 P Grant Count (CHID0_P):** Grant count for posted transactions on channel ID 0.

5.8.11 Upstream P2P Arbiter Channel 0 Grant Count (A_CR_UPARB_GCNT_P2P_0_MCHBAR)—Offset 6428h

Upstream Class/Target arbiter grant count.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RO	**Channel ID 0 Target Arbiter Grant Count (CHID0_TGT):** Target arbiter grant count for the channel ID 0 p2p class arbiter.
23:22	0h RO	Reserved.
21:16	1h RO	**Channel ID 0 C Grant Count (CHID0_C):** Grant count for completions on channel ID 0.
15:14	0h RO	Reserved.
13:8	1h RO	**Channel ID 0 Non-posted Grant Count (CHID0_N):** Grant count for non-posted transactions on channel ID 0.
7:6	0h RO	Reserved.
5:0	1h RO	**Channel ID 0 P Grant Count (CHID0_P):** Grant count for posted transactions on channel ID 0.

5.8.12 Upstream P2P Arbiter Channel 1 Grant Count (A_CR_UPARB_GCNT_P2P_1_MCHBAR)—Offset 642Ch

Upstream Class/Target arbiter grant count.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RO	**Channel ID 1 Target Arbiter Grant Count (CHID1_TGT):** Target arbiter grant count for the channel ID 1 p2p class arbiter.
23:22	0h RO	Reserved.
21:16	1h RO	**Channel ID 1 C Grant Count (CHID1_C):** Grant count for completions on channel ID 1.
15:14	0h RO	Reserved.
13:8	1h RO	**Channel ID 1 Non-posted Grant Count (CHID1_N):** Grant count for non-posted transactions on channel ID 1.
7:6	0h RO	Reserved.
5:0	1h RO	**Channel ID 1 P Grant Count (CHID1_P):** Grant count for posted transactions on channel ID 1

5.8.13 Upstream Private Credit Return Grant Count Posted 0 (A_CR_CRDARB_PRIV_GCNT_DEV_P_0_MCHBAR)—Offset 6430h

PSF credit return device arb grant count posted.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1000101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 3 P Grant Count (CHID3):** Grant count for posted transactions on channel ID 3.
23:22	0h RO	Reserved.
21:16	0h RO	**Channel ID 2 P Grant Count (CHID2):** Grant count for posted transactions on channel ID 2.
15:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:8	1h RW	**Channel ID 1 P Grant Count (CHID1):** Grant count for posted transactions on channel ID 1.
7:6	0h RO	Reserved.
5:0	1h RW	**Channel ID 0 P Grant Count (CHID0):** Grant count for posted transactions on channel ID 0.

5.8.14 Upstream Private Credit Return Grant Count Posted 1 (A_CR_CRDARB_PRIV_GCNT_DEV_P_1_MCHBAR)—Offset 6434h

PSF credit return device arb grant count posted.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010100h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 7 P Grant Count (CHID7):** Grant count for posted transactions on channel ID 7.
23:22	0h RO	Reserved.
21:16	1h RW	**Channel ID 6 P Grant Count (CHID6):** Grant count for posted transactions on channel ID 6.
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 5 P Grant Count (CHID5):** Grant count for posted transactions on channel ID 5.
7:6	0h RO	Reserved.
5:0	0h RO	**Channel ID 4 P Grant Count (CHID4):** Grant count for posted transactions on channel ID 4.

5.8.15 Upstream Private Credit Return Grant Count Non-posted 0 (A_CR_CRDARB_PRIV_GCNT_DEV_N_0_MCHBAR)—Offset 6438h

PSF credit return device arb grant count non-posted.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 3 Non-posted Grant Count (CHID3):** Grant count for non-posted transactions on channel ID 3.
23:22	0h RO	Reserved.
21:16	1h RW	**Channel ID 2 Non-posted Grant Count (CHID2):** Grant count for non-posted transactions on channel ID 2.
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 1 Non-posted Grant Count (CHID1):** Grant count for non-posted transactions on channel ID 1.
7:6	0h RO	Reserved.
5:0	1h RW	**Channel ID 0 Non-posted Grant Count (CHID0):** Grant count for non-posted transactions on channel ID 0.

5.8.16 Upstream Private Credit Return Grant Count Posted 1 (A_CR_CRDARB_PRIV_GCNT_DEV_N_1_MCHBAR)—Offset 643Ch

PSF credit return device arb grant count non-posted.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1040104h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 7 Non-posted Grant Count (CHID7):** Grant count for non-posted transactions on channel ID 7.
23:22	0h RO	Reserved.
21:16	4h RW	**Channel ID 6 Non-posted Grant Count (CHID6):** Grant count for non-posted transactions on channel ID 6.
15:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:8	1h RW	**Channel ID 5 Non-posted Grant Count (CHID5):** Grant count for non-posted transactions on channel ID 5.
7:6	0h RO	Reserved.
5:0	4h RW	**Channel ID 4 Non-posted Grant Count (CHID4):** Grant count for non-posted transactions on channel ID 4.

5.8.17 Upstream Private Credit Return Grant Count Completion (A_CR_CRDARB_PRIV_GCNT_DEV_C_0_MCHBAR)—Offset 6440h

PSF credit return device arb grant count completion.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	0h RO	**Channel ID 3 C Grant Count (CHID3):** Grant count for completions on channel ID 3.
23:22	0h RO	Reserved.
21:16	0h RO	**Channel ID 2 C Grant Count (CHID2):** Grant count for completions on channel ID 2.
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 1 C Grant Count (CHID1):** Grant count for completions on channel ID 1.
7:6	0h RO	Reserved.
5:0	1h RW	**Channel ID 0 C Grant Count (CHID0):** Grant count for completions on channel ID 0.

5.8.18 Upstream Shared Credit Return Grant Count Posted 0 (A_CR_CRDARB_SHRD_GCNT_DEV_P_0_MCHBAR)—Offset 6444h

PSF credit return device arb grant count Posteds

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1000101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 3 P Grant Count (CHID3):** Grant count for posted transactions on channel ID 3.
23:22	0h RO	Reserved.
21:16	0h RO	**Channel ID 2 P Grant Count (CHID2):** Grant count for posted transactions on channel ID 2.
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 1 P Grant Count (CHID1):** Grant count for posted transactions on channel ID 1.
7:6	0h RO	Reserved.
5:0	1h RW	**Channel ID 0 P Grant Count (CHID0):** Grant count for posted transactions on channel ID 0.

5.8.19 Upstream Shared Credit Return Grant Count Posted 1 (A_CR_CRDARB_SHRD_GCNT_DEV_P_1_MCHBAR)—Offset 6448h

PSF credit return device arb grant count posted.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010100h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 7 P Grant Count (CHID7):** Grant count for posted transactions on channel ID 7.
23:22	0h RO	Reserved.
21:16	1h RW	**Channel ID 6 P Grant Count (CHID6):** Grant count for posted transactions on channel ID 6.
15:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:8	1h RW	**Channel ID 5 P Grant Count (CHID5):** Grant count for posted transactions on channel ID 5.
7:6	0h RO	Reserved.
5:0	0h RO	**Channel ID 4 P Grant Count (CHID4):** Grant count for posted transactions on channel ID 4.

5.8.20 Upstream Shared Credit Return Grant Count Non-posted 0 (A_CR_CRDARB_SHRD_GCNT_DEV_N_0_MCHBAR)—Offset 644Ch

PSF credit return device arb grant count non-posted.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 3 Non-posted Grant Count (CHID3):** Grant count for non-posted transactions on channel ID 3.
23:22	0h RO	Reserved.
21:16	1h RW	**Channel ID 2 Non-posted Grant Count (CHID2):** Grant count for non-posted transactions on channel ID 2.
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 1 Non-posted Grant Count (CHID1):** Grant count for non-posted transactions on channel ID 1.
7:6	0h RO	Reserved.
5:0	1h RW	**Channel ID 0 Non-posted Grant Count (CHID0):** Grant count for non-posted transactions on channel ID 0.

5.8.21 Upstream Shared Credit Return Grant Count Posted 1 (A_CR_CRDARB_SHRD_GCNT_DEV_N_1_MCHBAR)—Offset 6450h

PSF credit return device arb grant count non-posted.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1040104h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	1h RW	**Channel ID 7 Non-posted Grant Count (CHID7):** Grant count for non-posted transactions on channel ID 7.
23:22	0h RO	Reserved.
21:16	4h RW	**Channel ID 6 Non-posted Grant Count (CHID6):** Grant count for non-posted transactions on channel ID 6.
15:14	0h RO	Reserved.
13:8	1h RW	**Channel ID 5 Non-posted Grant Count (CHID5):** Grant count for non-posted transactions on channel ID 5.
7:6	0h RO	Reserved.
5:0	4h RW	**Channel ID 4 Non-posted Grant Count (CHID4):** Grant count for non-posted transactions on channel ID 4.

5.8.22 Upstream Shared Credit Return Grant Count Completion (A_CR_CRDARB_SHRD_GCNT_DEV_C_0_MCHBAR)—Offset 6454h

PSF credit return device arb grant count completion.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 101h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	0h RO	**Channel ID 3 C Grant Count (CHID3):** Grant count for completions on channel ID 3.
23:22	0h RO	Reserved.
21:16	0h RO	**Channel ID 2 C Grant Count (CHID2):** Grant count for completions on channel ID 2.
15:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:8	1h RW	**Channel ID 1 C Grant Count (CHID1):** Grant count for completions on channel ID 1.
7:6	0h RO	Reserved.
5:0	1h RW	**Channel ID 0 C Grant Count (CHID0):** Grant count for completions on channel ID 0.

5.8.23 Upstream Credit Arbiter Private Credit Return Class Arbiter Grant Count (A_CR_CRDARB_PRIV_GCNT_CLS_MCHBAR)—Offset 6458h

PSF credit return class arb grant count

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10101h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:16	1h RW	**Completion (C):** All Completions.
15:14	0h RO	Reserved.
13:8	1h RW	**Non-posted (NP):** All non-posted.
7:6	0h RO	Reserved.
5:0	1h RW	**Posted (P):** All posted.

5.8.24 Upstream Credit Arbiter Shared Cedit Return Class Arbiter Grant Count (A_CR_CRDARB_SHRD_GCNT_CLS_MCHBAR)—Offset 645Ch

PSF credit return class arb grant count

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10101h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:16	1h RW	**C (C):** All Completions
15:14	0h RO	Reserved.
13:8	1h RW	**NP (NP):** All Non Posteds
7:6	0h RO	Reserved.
5:0	1h RW	**P (P):** All Posteds

5.8.25 Gazelle Queue Limit Channel 0-3 (A_CR_GZLQ_LIMIT_CH0_3_MCHBAR)—Offset 6460h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:24	FFh RW	**Channel ID 3 (CHID3):** Gazelle queue limit for Upstream NP on channel ID 3.
23:16	FFh RW	**Channel ID 2 (CHID2):** Gazelle queue limit for Upstream NP on channel ID 2.
15:8	FFh RW	**Channel ID 1 (CHID1):** Gazelle queue limit for Upstream NP on channel ID 1.
7:0	FFh RW	**Channel ID 0 (CHID0):** Gazelle queue limit for Upstream NP on channel ID 0.

5.8.26 Gazelle Queue Limit Channels 4-7 (A_CR_GZLQ_LIMIT_CH4_7_MCHBAR)—Offset 6464h

Gazelle queue limit for channel ID 4 to 7.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:24	FFh RW	**Channel ID 7 (CHID7):** Gazelle queue limit for Upstream NP on channel ID 7.
23:16	FFh RW	**Channel ID 6 (CHID6):** Gazelle queue limit for Upstream NP on channel ID 6.
15:8	FFh RW	**Channel ID 5 (CHID5):** Gazelle queue limit for Upstream NP on channel ID 5.
7:0	FFh RW	**Channel ID 4 (CHID4):** Gazelle queue limit for Upstream NP on channel ID 4.

5.8.27 IOMMU Arbiter Grant Count VC0a Register (A_CR_IOMMUARB_GCNT_VC0a_0_0_0_MCHBAR)—Offset 6468h

IOMMU arbiter grant count.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10101h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:16	1h RW	**Class Count (CLASS_CNT):** IOMMU arbiter class grant count.
15:14	0h RO	Reserved.
13:8	1h RW	**Device Non-posted (DEV_NP):** IOMMU arbiter device grant count for NP.
7:6	0h RO	Reserved.
5:0	1h RW	**Device Posted (DEV_P):** IOMMU arbiter device grant count for p.

5.8.28 IOMMU Arbiter Grant Count VC0b Register (A_CR_IOMMUARB_GCNT_VC0b_0_0_0_MCHBAR)—Offset 646Ch

IOMMU arbiter grant count.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10101h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:16	1h RW	**Class Count (CLASS_CNT):** IOMMU arbiter class grant count.
15:14	0h RO	Reserved.
13:8	1h RW	**Device Non-posted (DEV_NP):** IOMMU arbiter device grant count for NP.
7:6	0h RO	Reserved.
5:0	1h RW	**Device Posted (DEV_P):** IOMMU arbiter device grant count for p.

5.8.29 IOMMU Arbiter Grant Count VC1b Register (A_CR_IOMMUARB_GCNT_VC1b_0_0_0_MCHBAR)—Offset 6470h

IOMMU arbiter grant count.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10101h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:16	1h RW	**Class Count (CLASS_CNT):** IOMMU arbiter class grant count.
15:14	0h RO	Reserved.
13:8	1h RW	**Device Non-posted (DEV_NP):** IOMMU arbiter device grant count for NP.
7:6	0h RO	Reserved.
5:0	1h RW	**Device Posted (DEV_P):** IOMMU arbiter device grant count for p.

5.8.30 Gazelle Queue Reserved Entries Channels 0-3 (A_CR_GZLQ_RSVD_CH0_3_MCHBAR)—Offset 6474h

Gazelle queue limit for channel ID 0 to 3.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4040101h

Bit Range	Default & Access	Field Name (ID): Description
31:24	4h RW	**Channel ID 3 (CHID3):** Gazelle queue limit for Upstream NP on channel ID 3.
23:16	4h RW	**Channel ID 2 (CHID2):** Gazelle queue limit for Upstream NP on channel ID 2.
15:8	1h RW	**Channel ID 1 (CHID1):** Gazelle queue limit for Upstream NP on Channel ID 1.
7:0	1h RW	**Channel ID 0 (CHID0):** Gazelle queue limit for Upstream NP on Channel ID 0.

5.8.31 Gazelle Queue Reserved Entries Channels 4-7 (A_CR_GZLQ_RSVD_CH4_7_MCHBAR)—Offset 6478h

GazelleQ limit for CHID 0 to 3

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010101h

Bit Range	Default & Access	Field Name (ID): Description
31:24	1h RW	**Channel ID 7 (CHID7):** Gazelle queue limit for Upstream NP on channel ID 7.
23:16	1h RW	**Channel ID 6 (CHID6):** Gazellequeue limit for Upstream NP on channel ID 6.
15:8	1h RW	**Channel ID 5 (CHID5):** Gazelle queue limit for Upstream NP on channel ID 5.
7:0	1h RW	**Channel ID 4 (CHID4):** Gazelle queue limit for Upstream NP on channel ID 4.

5.8.32 Spare BIOS (A_CR_SPARE_BIOS_MCHBAR)—Offset 647Ch

Spare CR in MCHBAR.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SPARE RW Bits (SPARE_RW):** Spare RW 32 bits in BIOSWR policy group.

5.8.33 Upcmd Credit Maximum Channel 0 (A_CR_UPCMD_CRDTMAX_CH0_0_0_0_MCHBAR)—Offset 6490h

Upcmd Credit Max for PSF0 on Ch0 : Maximum number of credits exposed to PSF0.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4040Ch

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	4h RW	**Completion Max (CMP_MAX):** Max Cmp credits sent to PSF0 for Chid.
15	0h RO	Reserved.
14:8	4h RW	**Non-Posted Max (NP_MAX):** Max non-posted credits sent to PSF0 for Chid.
7	0h RO	Reserved.
6:0	Ch RW	**Posted Max (P_MAX):** Max posted credits sent to PSF0 for Chid.

5.8.34 Upcmd Credit Maximum Channel 1 (A_CR_UPCMD_CRDTMAX_CH1_0_0_0_MCHBAR)—Offset 6494h

Upcmd Credit Max for PSF0 on Ch1 : Maximum number of credits exposed to PSF0.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40404h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	4h RW	**Completion Max (CMP_MAX):** Max Cmp credits sent to PSF0 for Chid.
15	0h RO	Reserved.
14:8	4h RW	**Non-Posted Max (NP_MAX):** Max non-posted credits sent to PSF0 for Chid.
7	0h RO	Reserved.
6:0	4h RW	**Posted Max (P_MAX):** Max posted credits sent to PSF0 for Chid.

5.8.35 Upcmd Credit Maximum Channel 2 (A_CR_UPCMD_CRDTMAX_CH2_0_0_0_MCHBAR)—Offset 6498h

Upcmd Credit Max for PSF0 on Ch2 : Maximum number of credits exposed to PSF0.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 7F00h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	0h RW	**Completion Max (CMP_MAX):** Max Cmp credits sent to PSF0 for Chid.
15	0h RO	Reserved.
14:8	7Fh RW	**Non-Posted Max (NP_MAX):** Max non-posted credits sent to PSF0 for Chid.
7	0h RO	Reserved.
6:0	0h RW	**Posted Max (P_MAX):** Max posted credits sent to PSF0 for Chid.

5.8.36 Upcmd Credit Maximum Channel 3 (A_CR_UPCMD_CRDTMAX_CH3_0_0_0_MCHBAR)—Offset 649Ch

Upcmd Credit Max for PSF0 on Ch3 : Maximum number of credits exposed to PSF0.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	0h RW	**Completion Max (CMP_MAX):** Max Cmp credits sent to PSF0 for Chid.
15	0h RO	Reserved.
14:8	7Fh RW	**Non-Posted Max (NP_MAX):** Max non-posted credits sent to PSF0 for Chid.
7	0h RO	Reserved.
6:0	7Fh RW	**Posted Max (P_MAX):** Max posted credits sent to PSF0 for Chid.

5.8.37 Upcmd Credit Maximum Channel 4 (A_CR_UPCMD_CRDTMAX_CH4_0_0_0_MCHBAR)—Offset 64A0h

Upcmd Credit Max for PSF0 on Ch4 : Maximum number of credits exposed to PSF0.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 400h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	0h RW	**Completion Max (CMP_MAX):** Max Cmp credits sent to PSF0 for Chid.
15	0h RO	Reserved.
14:8	4h RW	**Non-Posted Max (NP_MAX):** Max non-posted credits sent to PSF0 for Chid.
7	0h RO	Reserved.
6:0	0h RW	**Posted Max (P_MAX):** Max posted credits sent to PSF0 for Chid.

5.8.38 Upcmd Credit Maximum Channel 5 (A_CR_UPCMD_CRDTMAX_CH5_0_0_0_MCHBAR)—Offset 64A4h

Upcmd Credit Max for PSF0 on Ch5 : Maximum number of credits exposed to PSF0.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 404h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	0h RW	**Completion Max (CMP_MAX):** Max Cmp credits sent to PSF0 for Chid.
15	0h RO	Reserved.
14:8	4h RW	**Non-Posted Max (NP_MAX):** Max non-posted credits sent to PSF0 for Chid.
7	0h RO	Reserved.
6:0	4h RW	**Posted Max (P_MAX):** Max posted credits sent to PSF0 for Chid.

5.8.39 Upcmd Credit Maximum Channel 6 (A_CR_UPCMD_CRDTMAX_CH6_0_0_0_MCHBAR)—Offset 64A8h

Upcmd Credit Max for PSF0 on Ch6 : Maximum number of credits exposed to PSF0.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 404h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	0h RW	**Completion Max (CMP_MAX):** Max Cmp credits sent to PSF0 for Chid.
15	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:8	4h RW	**Non-Posted Max (NP_MAX):** Max non-posted credits sent to PSF0 for Chid.
7	0h RO	Reserved.
6:0	4h RW	**Posted Max (P_MAX):** Max posted credits sent to PSF0 for Chid.

5.8.40 Upcmd Credit Maximum Channel 7 (A_CR_UPCMD_CRDTMAX_CH7_0_0_0_MCHBAR)—Offset 64ACh

Upcmd Credit Max for PSF0 on Ch7 : Maximum number of credits exposed to PSF0.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40Ch

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	0h RW	**Completion Max (CMP_MAX):** Max Cmp credits sent to PSF0 for Chid.
15	0h RO	Reserved.
14:8	4h RW	**Non-Posted Max (NP_MAX):** Max non-posted credits sent to PSF0 for Chid.
7	0h RO	Reserved.
6:0	Ch RW	**Posted Max (P_MAX):** Max posted credits sent to PSF0 for Chid.

5.8.41 MOT OUT Base Register (A_CR_MOT_OUT_BASE_0_0_0_MCHBAR)—Offset 64C0h

This register contains the value of the start address of the MOT debug data region. The smallest reserved region for MOT debug data (if enabled) is 16MB. MOT region must be power-of-two sized and naturally

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR enable (IMR_EN):** IMR Enable: Enables access checking for the MOT region. Note: this does not enable MOT itself merely enables access control checks for transactions that attempt to access the MOT buffer.
30	0h RO	**Trace Enable (TR_EN):** Asset Classification (AC)[0]: Trace Enable: Enables snooping of transactions to the IMR region by tracing agents such as MOT. Reserved and set to 0 for the MOT region, since otherwise this would enable recursive
29	0h RO	Reserved.
28:14	0h RW	**MOT_OUT_BASE address (MOT_OUT_BASE):** Specifies bits 38:24 of the start address of the MOT memory region. Region size must be a strict poweroftwo at least 16MB and naturally aligned to the size. These bits are compared with the result of the MOT_OUT_MASK[28:14] applied to bits 38:24 of the incoming address to determine if an access falls within the MOT region.
13:0	0h RO	Reserved.

5.8.42 MOT OUT Mask Register (A_CR_MOT_OUT_MASK_0_0_0_MCHBAR)—Offset 64C4h

This register specifies the size of the MOT region. If a request address [39:24] AND-ed with MOT_OUT_MASK[15:0] matches the MOT_OUT_BASE[15:0], then the request falls within the MOT_OUT region

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**GT Implicit Writeback Enable (GT_IWB_EN):** Asset Classification AC[2]: GT Implicit WB Enable: Enables implicit writebacks to protected region from GT caching agent. When set to 1 enables implicit writeback data HITM data from GT to be returned to the requester. When set to 0 inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester depending on the setting of the IA_IWB_EN bit.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW	**IA Implicit Writeback Enable (IA_IWB_EN):** Asset Classification AC[1]: IA Implicit WB Enable: Enables implicit writebacks to protected region from IA caching agent. When set to 1 enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0 inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester depending on the setting of the GT_IWB_EN bit.
29	0h RO	Reserved.
28:14	0h RW	**MOT OUT Mask (MOT_OUT_MASK):** Specifies the size of the MOT region. If Request Address [38:24] ANDed with MOT_OUT_MASK[28:14] matches the MOT_OUT_BASE[28:14] then the request falls within the MOT_OUT region
13:0	0h RO	Reserved.

5.8.43 A-Unit BIOSWR Control Policy (A_CR_BIOSWR_CP_0_0_0_MCHBAR)—Offset 64C8h

This register controls the access policy to the A-Unit BIOS_RAC BIOS_AC BIOS_CP.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40061010202h RW	**BIOS Control Policy (BIOSWR_CP):** Bit vector used to determine which agents are allowed access to the A-Unit BIOSWR Registers based on the value from the agents 6 bit SAI field. This register is selfreferential the access policy provided applies to access to the control register itself.

5.8.44 A-Unit BIOSWR Ready Access Control (A_CR_BIOSWR_RAC_0_0_0_MCHBAR)—Offset 64D0h

This register configures the Read Access Policy for the A-Unit BIOS policy configuration registers. It is programmed with a SAI Policy that indicates which agents in the system are allowed to perform read operations to A-Unit BIOS policy group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 80000C0063010217h

Bit Range	Default & Access	Field Name (ID): Description
63:0	80000C0063010217h RW	**BIOS Read Access Control (BIOSWR_RAC):** Bit vector used to determine which agents are allowed Rd access to the A-Unit BIOSWR Register based on the value from the agents 6 bit SAI field.

5.8.45 BIOSWR Write Access Control (A_CR_BIOSWR_WAC_0_0_0_MCHBAR)—Offset 64D8h

This register configures the Write Access Policy for the A-Unit BIOSWR registers. It is programmed with a SAI Policy that indicates which agents in the system are allowed to perform read operations to A-Unit BIOS policy group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061000212h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061000212h RW	**BIOS Write Access Control (BIOSWR_WAC):** Bit vector used to determine which agents are allowed Wr access to the A-Unit BIOSWR registers based on the value from the agents 6 bit SAI field.

5.8.46 AUnit Pcode/Ucode Write, All Read Control Policy Register (A_CR_P_U_CODEWR_ALLRD_CP_0_0_0_MCHBAR)—Offset 64E0h

AUnit Pcode/Ucode Write, All Read Control Policy: This register controls the access policy to the Aunit P_U_CODEWR_ALLRD_RAC P_U_CODEWR_ALLRD_WAC

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001000202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001000202h RW	**P_U_CODEWR_ALLRD Control Policy (P_U_CODEWR_ALLRD_CP):** Bit vector used to determine which agents are allowed access to the Aunit P_U_CODEWR_ALLRD based on the value from the agents 6 bit SAI field. This register is selfreferential the access policy provided applies to access to the control register itself.

5.8.47 AUnit Pcode/Ucode Write, All Read Read Access Control Policy Register (A_CR_P_U_CODEWR_ALLRD_RAC_0_0_0_MCHBAR)—Offset 64E8h

AUnit Pcode/Ucode Write, All Read Read Access Control Policy: This register controls the read access policy to the Aunit P_U_CODEWR_ALLRD

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: FFFFFFFFFFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:0	FFFFFFFFFFFFFFFFh RO	**P_U_CODEWR_ALLRD Read Access Control (P_U_CODEWR_ALLRD_RAC):** Bit vector used to determine which agents are allowed Rd access to the Aunit P_U_CODEWR_ALLRD based on the value from the agents 6 bit SAI field.

5.8.48 AUnit Pcode/Ucode Write, All Read Write Access Control Policy Register (A_CR_P_U_CODEWR_ALLRD_WAC_0_0_0_MCHBAR)—Offset 64F0h

AUnit Pcode/Ucode Write, All Read Write Access Control Policy: This register controls the write access policy to the Aunit P_U_CODEWR_ALLRD

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001000202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001000202h RW	**P_U_CODEWR_ALLRD Write Access Control (P_U_CODEWR_ALLRD_WAC):** Bit vector used to determine which agents are allowed Wr access to the Aunit P_U_CODEWR_ALLRD based on the value from the agents 6 bit SAI field.

5.8.49 CHAP Select 1 (A_CR_CHAP_SLCT1_MCHBAR)—Offset 6500h

Chap event select register 1.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	0h RW	**Channel ID Y Count Upstream txn (CHID_Y_CNT_UPTXN):** Count upstream txn on all VCs where CHID_Y[i]=1.
15:8	0h RO	Reserved.
7:0	0h RW	**Channel ID X Count Upstream txn (CHID_X_CNT_UPTXN):** Count upstream txn on all VCs where CHID_X[i]=1.

5.8.50 CHAP Select 2 (A_CR_CHAP_SLCT2_MCHBAR)—Offset 6504h

Chap event select register 2.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	0h RW	**Channel ID Y Count Downstream txn (CHID_Y_CNT_DNTXN):** Count downstream txn on all VCs where CHID_Y[i]=1.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h RW	**Channel ID X Count Downstream txn (CHID_X_CNT_DNTXN):** Count downstream txn on all VCs where CHID_X[i]=1.

5.8.51 CHAP Select 3 (A_CR_CHAP_SLCT3_MCHBAR)—Offset 6508h

Chap event select register 3.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:2	1h RW	**Q Occupancy Y (Q_OCCUPANCY_Y):** Count occupancy/residency of certain Q in A-Unit • 00: UpCmd • 01: UpData • 10: GzlQ • 11: DnCmd/Data
1:0	0h RW	**Q Occupancy X (Q_OCCUPANCY_X):** Count occupancy/residency of certain Q in A-Unit • 00: UpCmd • 01: UpData • 10: GzlQ • 11: DnCmd/Data

5.8.52 A_IMRGLOBAL_BM Control Policy (A_CR_IMRGLOBAL_BM_CP_0_0_0_MCHBAR)—Offset 6510h

This register controls the access policy to the A-Unit IMRGLOBAL_BM_RAC IMRGLOBAL_BM_AC IMRGLOBAL_BM_CP.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMRGLOBAL_BM Control Policy (IMRGLOBAL_BM_CP):** Bit vector used to determine which agents are allowed access to the A-Unit IMRGLOBAL_BM Registers based on the value from the agents 6 bit SAI field. This register is selfreferential the access policy provided applies to access to the control register itself.

5.8.53 A_IMRGLOBAL_BM Read Access Control (A_CR_IMRGLOBAL_BM_RAC_0_0_0_MCHBAR)—Offset 6518h

This register configures the Read Access Policy for the A-Unit IMRGLOBAL_BM policy configuration registers. It is programmed with a SAI Policy that indicates which agents in the system are allowed to perform read operations to A-Unit IMRGLOBAL_BM policy group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: F0FFFF0FFFF0FFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:0	F0FFFF0FFFF0FFFFh RO	**IMRGLOBAL_BM Read Access Control (IMRGLOBAL_BM_RAC):** Bit vector used to determine which agents are allowed Rd access to the A-Unit IMRGLOBAL_BM Register based on the value from the agents 6 bit SAI field.

5.8.54 A_IMRGLOBAL_BM Write Access Control (A_CR_IMRGLOBAL_BM_WAC_0_0_0_MCHBAR)—Offset 6520h

This register configures the Write Access Policy for the A-Unit IMRGLOBAL_BM registers. It is programmed with a SAI Policy that indicates which agents in the system are allowed to perform read operations to A-Unit IMRGLOBAL_BM policy group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010 202h RW	**IMRGLOBAL_BM Write Access Control (IMRGLOBAL_BM_WAC):** Bit vector used to determine which agents are allowed Wr access to the A-Unit IMRGLOBAL_BM registers based on the value from the agents 6 bit SAI field.

5.8.55 Uncorrectable Error Status Register (A_CR_UNCERRSTS_0_0_0_MCHBAR)—Offset 6588h

Errors that have been seen in aunit. The error is only logged if the respective bit in UNCERRMSK is 0.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**reserved (undefined31):** reserved for future use
30	0h RO	**reserved (undefined30):** reserved for future use
29	0h RO	**reserved (undefined29):** reserved for future use
28	0h RO	**reserved (undefined28):** reserved for future use
27	0h RO	**reserved (undefined27):** reserved for future use
26	0h RO	**reserved (undefined26):** reserved for future use
25	0h RO	**reserved (undefined25):** reserved for future use
24	0h RO	**reserved (undefined24):** reserved for future use
23	0h RO	**reserved (undefined23):** reserved for future use
22	0h RO	**reserved (undefined22):** reserved for future use
21	0h RO	**reserved (undefined21):** reserved for future use
20	0h RO	**reserved (undefined20):** reserved for future use
19	0h RO	**reserved (undefined19):** reserved for future use
18	0h RO	**reserved (undefined18):** reserved for future use

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**reserved (undefined17):** reserved for future use
16	0h RO	**reserved (undefined16):** reserved for future use
15	0h RO	**reserved (undefined15):** reserved for future use
14	0h RO	**reserved (undefined14):** reserved for future use
13	0h RO	**reserved (undefined13):** reserved for future use
12	0h RO	**reserved (undefined12):** reserved for future use
11	0h RO	**reserved (undefined11):** reserved for future use
10	0h RW/1C	**msi rsvd set (msi_rsvd_set):** An MSI was received with reserved bits set
9	0h RW/1C	**gpa overflow (gpa_overflow):** A transaction was received with a guest physical address that was too large
8	0h RW/1C	**illegal msi (illegal_msi):** A malformed/illegal MSI was received in the upstream direction
7	0h RW/1C	**at translated illegal device (at_translated_illegal_device):** A device that is not support to set the AT bit set it to an illegal value
6	0h RO	**reserved (undefined5):** reserved for future use
5	0h RW/1C	**bad sai cmpl (bad_sai_cmpl):** An incorrect/illegal sai was received with an upstream completion transaction.
4	0h RW/1C	**received lk cmpl (received_lk_cmpl):** Received a CmplLck completion from iosf.
3	0h RW/1C	**bad sai nonposted (bad_sai_nonposted):** An incorrect/illegal sai was received with an upstream non-posted transaction.
2	0h RW/1C	**illegal nonposted opcode (illegal_nonposted_opcode):** Illegal/Unsupported non-posted opcode received from iosf.
1	0h RW/1C	**bad sai posted (bad_sai_posted):** An incorrect/illegal sai was received with an upstream posted transaction.
0	0h RW/1C	**illegal posted opcode (illegal_posted_opcode):** Illegal/ Unsupported posted opcode received from iosf.

5.8.56 Uncorrectable Error Mask Register (A_CR_UNCERRMSK_0_0_0_MCHBAR)—Offset 658Ch

Masks whether a reported error is logged and signaled to the IEH. 1- do not log/signal. 0 - log/signal.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**reserved (undefined31):** reserved for future use
30	1h RO	**reserved (undefined30):** reserved for future use
29	1h RO	**reserved (undefined29):** reserved for future use
28	1h RO	**reserved (undefined28):** reserved for future use
27	1h RO	**reserved (undefined27):** reserved for future use
26	1h RO	**reserved (undefined26):** reserved for future use
25	1h RO	**reserved (undefined25):** reserved for future use
24	1h RO	**reserved (undefined24):** reserved for future use
23	1h RO	**reserved (undefined23):** reserved for future use
22	1h RO	**reserved (undefined22):** reserved for future use
21	1h RO	**reserved (undefined21):** reserved for future use
20	1h RO	**reserved (undefined20):** reserved for future use
19	1h RO	**reserved (undefined19):** reserved for future use
18	1h RO	**reserved (undefined18):** reserved for future use
17	1h RO	**reserved (undefined17):** reserved for future use
16	1h RO	**reserved (undefined16):** reserved for future use
15	1h RO	**reserved (undefined15):** reserved for future use
14	1h RO	**reserved (undefined14):** reserved for future use
13	1h RO	**reserved (undefined13):** reserved for future use
12	1h RO	**reserved (undefined12):** reserved for future use
11	1h RO	**reserved (undefined11):** reserved for future use

Bit Range	Default & Access	Field Name (ID): Description
10	1h RW	**msi rsvd set (msi_rsvd_set):** An MSI was received with reserved bits set
9	1h RW	**gpa overflow (gpa_overflow):** A transaction was received with a guest physical address that was too large
8	1h RW	**illegal msi (illegal_msi):** A malformed/illegal MSI was received in the upstream direction
7	1h RW	**at translated illegal device (at_translated_illegal_device):** A device that is not support to set the AT bit set it to an illegal value
6	1h RO	**reserved (undefined5):** reserved for future use
5	1h RW	**bad sai cmpl (bad_sai_cmpl):** An incorrect/illegal sai was received with an upstream completion transaction.
4	1h RW	**received lk cmpl (received_lk_cmpl):** Received a CmplLck completion from iosf.
3	1h RW	**bad sai nonposted (bad_sai_nonposted):** An incorrect/illegal sai was received with an upstream non-posted transaction.
2	1h RW	**illegal nonposted opcode (illegal_nonposted_opcode):** Illegal/Unsupported non-posted opcode received from iosf.
1	1h RW	**bad sai posted (bad_sai_posted):** An incorrect/illegal sai was received with an upstream posted transaction.
0	1h RW	**illegal posted opcode (illegal_posted_opcode):** Illegal/ Unsupported posted opcode received from iosf.

5.8.57 Slice and Channel Hash (A_CR_SLICE_CHANNEL_HASH_0_0_0_MCHBAR)—Offset 65C0h

A-Unit slice and channel hash function.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 3C00000000h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**Lock (LOCK):** Intended usage is for BIOS to set the LOCK when it updates the CR. A-Unit implements only storage for this bit. No hardware exists to implement hardware locking.
62:52	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
51:38	0h RW	**Channel Hash Mask (CH_HASH_MASK):** When both PMI channels in a slice are enabled, this field specifies the Channel Hash Mask to be applied on Addr[19:6] postremap DRAM address of the request to compute which PMI channel a request must be routed to. Relevant only when HVM mode is disabled and only for requests that do not fall under the MOT region. B-Unit will override the programmed value to include the Channel Selector bit See SLICEHASH.INTERLEAVE_MODE field. Note that HVM mode and MOT regions have special hash requirements and hence they do not use the CH_HASH_MASK.
37:36	3h RW	**Channel Enabled for Slice 1 (SYM_SLICE1_CHANNEL_ENABLED):** Specifies which channel is enabled for Slice 1, This is for those cases where Channel 0 or 1 could be disabled for Slice 1 If both bits are set then channel select will be based on the Channel Select logic
35:34	3h RW	**Channel Enabled for Slice 0 (SYM_SLICE0_CHANNEL_ENABLED):** Specifies which channel is enabled for Slice 0, This is for those cases where Channel 0 or 1 could be disabled for Slice 0 If both bits are set then channel select will be based on the Channel Select logic
33	0h RO	Reserved.
32	0h RW	**Channel 1 Disabled (CH_1_DISABLED):** Channel 1 in both slices are disabled no memory address mapped to ch 1. All requests sent to channel 0.
31	0h RW	**Enable PMI Dual Data Mode (ENABLE_PMI_DUAL_DATA_MODE):** When set to 1, Single Command Interface and Dual Data Interface for Reads and Writes
30:20	0h RO	Reserved.
19:6	0h RW	**Slice Hash Mask (SLICE_HASH_MASK):** When both slices are enabled this field specifies the Slice Hash Mask to be applied on Addr[19:6] physical address of the request to compute which slice a request must be routed to. Relevant only when HVM mode is disabled and only for physical addresses that do not fall under the Asymmetric Memory Region and the MOT region. B-Unit will override the programmed value to include the Slice Selector bit See INTERLEAVE_MODE field. Note that HVM mode nonaddress IDI requests asymmetric memory region and MOT regions have special hash requirements and hence they do not use the SLICE_HASH_MASK.
5	0h RO	Reserved.
4	0h RW	**Slice 0 Mem Disabled (SLICE_0_MEM_DISABLED):** Slice 0 is disabled for memory accesses; no memory address mapped to Slice 0 and all memory requests sent to Slice 1.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RW	**Interleave Mode (INTERLEAVE_MODE):** Default interleave mode that specifies how the Slice Selector and Channel Selector bits are to be determined. Relevant only when HVM mode is disabled and only for system memory addresses that do not fall under the MOT region or the Asymmetric memory region in the System Address Map. Legal encodings are 0x0 0x1 and 0x2. An encoding of 0x3 is treated as if it was 0x2. When both slices and all four PMI channels are enabled: • 0h: Default Slice Selector is Addr[10] and Default Channel Selector is Addr[11] • 1h: Default Slice Selector is Addr[11] and Default Channel Selector is Addr[12] • 2h: Default Slice Selector is Addr[12] and Default Channel Selector is Addr[13] When both slices are enabled but only one channel in each slice enabled: • 0h: Default Slice Selector is Addr[10] • 1h: Default Slice Selector is Addr[11] • 2h: Default Slice Selector is Addr[12] When only SLICE0 is enabled and both channels on that slice are enabled: • 0h: Default Channel Selector is Addr[10] • 1h: Default Channel Selector is Addr[11] • 2h: Default Channel Selector is Addr[12] When SLICE0 and only one channel in that slice is enabled this field is not relevant. B-Unit overrides the setting of the SLICE_HASH_MASK to always include the Slice Selector bit. Similarly, B-Unit overrides the setting of the CH_HASH_MASK to always include the Channel Selector bit.
1	0h RW	**HVM Mode (HVM_MODE):** • 0: HVM mode is disabled. • 1: HVM mode is enabled. When HVM mode is enabled, Slice Hash and Channel Hash is done as follows: Both slices and all four PMI channels enabled: • Slice Hash is Request Physical Addr[29] • Channel Hash is PostRemap Addr[30] Both slices enabled but only one PMI channel in each slice enabled: • Slice Hash is Request Physical Addr[29] Only one SLICE0 enabled but both PMI channels in SLICE0 enabled: • Channel Hash is PostRemap Addr[29] When HVM_MODE is enabled TOLUD must be set at 2GB.
0	0h RW	**Slice 1 Disabled (SLICE_1_DISABLED):** Slice 1 is disabled; no memory address mapped to Slice 1. All request sent to Slice 0.

5.8.58 Mirror Range Register (A_CR_MIRROR_RANGE_0_0_0_MCHBAR)—Offset 65C8h

Mirror Range: This register defines base and limit of the 8M aligned region in memory that captures the mirror writes. Since b[22:0] are assumed to be 0's the smallest size of the region is 8M

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:48	0h RO	Reserved.
47:32	0h RW	**Mirror Limit Address (MIRROR_LIMIT):** Mirror Limit: specifies b38:b23 of HPA indicating the end of mirror packet buffer region
31:16	0h RO	Reserved.
15:0	0h RW	**Mirror_Base Address (MIRROR_BASE):** Mirror Base: specifies b38:b23 of HPA indicating the start of mirror packet buffer region

5.8.59 ASYM MEM REGION 0 CONFIGURATION WITH NO INTERLEAVING (A_CR_ASYM_MEM_REGION0_0_0_0_MCHBAR)—Offset 65D0h

Specification of asymmetric memory region 0 (in slice 0) for the configuration with 2 asymmetric memory regions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Asymmetric Region in Slice 0, With No Interleaving (SLICE0_ASYM_ENABLE):** Setting this bit to 0 disables asymmetric memory region 0; setting it to 1 enables the region.
30	0h RW	**Channel Select for ASYM Region Slice 0 (SLICE0_ASYM_CHANNEL_SELECT):** Specifies which Channel in ASYM Slice 0 request is sent
29:19	0h RW	**Limit Address for Asymmetric Memory Region, Slice 0, With No Interleaving (SLICE0_ASYM_LIMIT):** Specifies bits [38:31] of the highest address of asymmetric memory region 0 (in slice 0); all the lower bits of the region's highest address are equal to 1.
18:15	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:4	0h RW	**Base Address for Asymmetric Memory Region, Slice 0, With No Interleaving (SLICE0_ASYM_BASE):** Specifies bits [38:31] of the base address of asymmetric memory region 0 (in slice 0); all the lower bits of the region's base address are equal to 0.
3:0	0h RO	Reserved.

5.8.60 ASYM MEM REGION 1 CONFIGURATION WITH NO INTERLEAVING (A_CR_ASYM_MEM_REGION1_0_0_0_MCHBAR)—Offset 65D4h

Specification of asymmetric memory region 1 (in slice 1) for the configuration with 2 asymmetric memory regions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Asymmetric Region in Slice 1, With No Interleaving (SLICE1_ASYM_ENABLE):** Setting this bit to 0 disables asymmetric memory region 1; setting it to 1 enables the region.
30	0h RW	**Channel Select for ASYM SLICE 1 (SLICE1_ASYM_CHANNEL_SELECT):** Specifies Channel for ASYM Region Slice 1
29:19	0h RW	**Limit Address for Asymmetric Memory Region, Slice 1, With No Interleaving (SLICE1_ASYM_LIMIT):** Specifies bits [38:31] of the highest address of asymmetric memory region 1 (in slice 1); all the lower bits of the region's highest address are equal to 1.
18:15	0h RO	Reserved.
14:4	0h RW	**Limit Address for Asymmetric Memory Region, Slice 1, With No Interleaving (SLICE1_ASYM_BASE):** Specifies bits [38:31] of the base address of asymmetric memory region 1 (in slice 1); all the lower bits of the region's base address are equal to 0.
3:0	0h RO	Reserved.

5.8.61 Two-Way Asymmetric Memory Region Configuration (A_CR_ASYM_2WAY_MEM_REGION_0_0_0_MCHBAR)—Offset 65D8h

Specification of asymmetric memory region 1 (in slice 1) for the configuration with 2 asymmetric memory regions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Two-Way Asymmetric Memory Configuration (ASYM_2WAY_INTERLEAVE_ENABLE):** Setting this bit to 0 disables Interleave Asymmetric memory region 1, setting it to 1 enables the region.
30:28	0h RO	Reserved.
27:17	0h RW	**Limit Address for Two-Way Asymmetric Memory Region (ASYM_2WAY_LIMIT):** Specifies bits [38:28] of the highest address of Interleave Asymmetric Region, all the lower bits of the region's highest address are equal to 1.
16:15	0h RO	Reserved.
14:4	0h RW	**Base Address for Two-Way Asymmetric Memory Region (ASYM_2WAY_BASE):** Specifies bits [38:28] of the base address of Interleave Asymmetric Region; all the lower bits of the region's base address are equal to 0.
3:2	0h RO	Reserved.
1:0	0h RW	**Two-Way Asymmetric Interleave Mode (ASYM_2WAY_INTLV_MODE):** Going with 2 bits here. 2'b00 : Asymmetric memory Split between Channel 0 of Slice 0 and Slice 1 2'b01 : Asymmetric memory split between Channel 1 of Slice 0 and Slice 1 2'b10 : Asymmetric memory split between Channel 0 and Channel 1 of Slice 0 2'b11 : Asymmetric memory split between Channel 0 and Channel 1 of Slice 1

5.9 Registers Summary

Table 5-9. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6800h	6803h	B-Unit Miscellaneous Configuration (B_CR_BMISC_0_0_0_MCHBAR)—Offset 6800h	7h

Table 5-9. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6808h	680Fh	Security Control Policy (B_CR_SECURITY_CP_0_0_0_MCHBAR)—Offset 6808h	0h
6810h	6817h	Security Group Read Access Policy (B_CR_SECURITY_RAC_0_0_0_MCHBAR)—Offset 6810h	C0061010202h
6818h	681Fh	Security Group Write Access Policy (B_CR_SECURITY_WAC_0_0_0_MCHBAR)—Offset 6818h	C0061010202h
6868h	686Bh	Slice 0 Memory Access Count (B_CR_MEM_ACCESS_COUNT_SLICE0)—Offset 6868h	0h
686Ch	686Fh	Slice 1 Memory Access Count (B_CR_MEM_ACCESS_COUNT_SLICE1)—Offset 686Ch	0h
6870h	6873h	IMR0 Base (B_CR_BIMR0BASE_0_0_0_MCHBAR)—Offset 6870h	0h
6874h	6877h	IMR0 Mask (B_CR_BIMR0MASK_0_0_0_MCHBAR)—Offset 6874h	0h
6878h	687Fh	IMR0 Control Policy (B_CR_BIMR0CP_0_0_0_MCHBAR)—Offset 6878h	C0061010202h
6880h	6887h	IMR0 Read Access Policy (B_CR_BIMR0RAC_0_0_0_MCHBAR)—Offset 6880h	0h
6888h	688Fh	IMR0 Write Access Policy (B_CR_BIMR0WAC_0_0_0_MCHBAR)—Offset 6888h	0h
6890h	6893h	IMR1 Base (B_CR_BIMR1BASE_0_0_0_MCHBAR)—Offset 6890h	0h
6894h	6897h	IMR1 Mask (B_CR_BIMR1MASK_0_0_0_MCHBAR)—Offset 6894h	0h
6898h	689Fh	IMR1 Control Policy (B_CR_BIMR1CP_0_0_0_MCHBAR)—Offset 6898h	C0061010202h
68A0h	68A7h	IMR1 Read Access Policy (B_CR_BIMR1RAC_0_0_0_MCHBAR)—Offset 68A0h	0h
68A8h	68AFh	IMR1 Write Access Policy (B_CR_BIMR1WAC_0_0_0_MCHBAR)—Offset 68A8h	0h
68B0h	68B3h	Base 0 IMR2 Base (B_CR_BIMR2BASE_0_0_0_MCHBAR)—Offset 68B0h	0h
68B4h	68B7h	IMR2 Mask (B_CR_BIMR2MASK_0_0_0_MCHBAR)—Offset 68B4h	0h
68B8h	68BFh	IMR2 Control Policy (B_CR_BIMR2CP_0_0_0_MCHBAR)—Offset 68B8h	C0061010202h
68C0h	68C7h	IMR2 Read Access Policy (B_CR_BIMR2RAC_0_0_0_MCHBAR)—Offset 68C0h	0h
68C8h	68CFh	IMR2 Write Access Policy (B_CR_BIMR2WAC_0_0_0_MCHBAR)—Offset 68C8h	0h
68D0h	68D3h	IMR3 Base (B_CR_BIMR3BASE_0_0_0_MCHBAR)—Offset 68D0h	0h
68D4h	68D7h	IMR3 Mask (B_CR_BIMR3MASK_0_0_0_MCHBAR)—Offset 68D4h	0h
68D8h	68DFh	IMR3 Control Policy (B_CR_BIMR3CP_0_0_0_MCHBAR)—Offset 68D8h	C0061010202h
68E0h	68E7h	IMR3 Read Access Policy (B_CR_BIMR3RAC_0_0_0_MCHBAR)—Offset 68E0h	0h
68E8h	68EFh	IMR3 Write Access Policy (B_CR_BIMR3WAC_0_0_0_MCHBAR)—Offset 68E8h	0h

Table 5-9. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
68F0h	68F3h	IMR4 Base (B_CR_BIMR4BASE_0_0_0_MCHBAR)—Offset 68F0h	0h
68F4h	68F7h	IMR4 Mask (B_CR_BIMR4MASK_0_0_0_MCHBAR)—Offset 68F4h	0h
68F8h	68FFh	B-Unit IMR4 Control Policy (B_CR_BIMR4CP_0_0_0_MCHBAR)—Offset 68F8h	C0061010202h
6900h	6907h	IMR4 Read Access Policy (B_CR_BIMR4RAC_0_0_0_MCHBAR)—Offset 6900h	0h
6908h	690Fh	IMR4 Write Access Policy (B_CR_BIMR4WAC_0_0_0_MCHBAR)—Offset 6908h	0h
6910h	6913h	IMR5 Base (B_CR_BIMR5BASE_0_0_0_MCHBAR)—Offset 6910h	0h
6914h	6917h	IMR5 Mask (B_CR_BIMR5MASK_0_0_0_MCHBAR)—Offset 6914h	0h
6918h	691Fh	IMR5 Control Policy (B_CR_BIMR5CP_0_0_0_MCHBAR)—Offset 6918h	C0061010202h
6920h	6927h	IMR5 Read Access Policy (B_CR_BIMR5RAC_0_0_0_MCHBAR)—Offset 6920h	0h
6928h	692Fh	IMR5 Write Access Policy (B_CR_BIMR5WAC_0_0_0_MCHBAR)—Offset 6928h	0h
6930h	6933h	IMR6 Base (B_CR_BIMR6BASE_0_0_0_MCHBAR)—Offset 6930h	0h
6934h	6937h	IMR6 Mask (B_CR_BIMR6MASK_0_0_0_MCHBAR)—Offset 6934h	0h
6938h	693Fh	IMR6 Control Policy (B_CR_BIMR6CP_0_0_0_MCHBAR)—Offset 6938h	C0061010202h
6940h	6947h	IMR6 Read Access Policy (B_CR_BIMR6RAC_0_0_0_MCHBAR)—Offset 6940h	0h
6948h	694Fh	IMR6 Write Access Policy (B_CR_BIMR6WAC_0_0_0_MCHBAR)—Offset 6948h	0h
6950h	6953h	IMR7 Base (B_CR_BIMR7BASE_0_0_0_MCHBAR)—Offset 6950h	0h
6954h	6957h	IMR7 Mask (B_CR_BIMR7MASK_0_0_0_MCHBAR)—Offset 6954h	0h
6958h	695Fh	IMR7 Control Policy (B_CR_BIMR7CP_0_0_0_MCHBAR)—Offset 6958h	C0061010202h
6960h	6967h	IMR7 Read Access Policy (B_CR_BIMR7RAC_0_0_0_MCHBAR)—Offset 6960h	0h
6968h	696Fh	IMR7 Write Access Policy (B_CR_BIMR7WAC_0_0_0_MCHBAR)—Offset 6968h	0h
6970h	6973h	IMR8 Base (B_CR_BIMR8BASE_0_0_0_MCHBAR)—Offset 6970h	0h
6974h	6977h	IMR8 Mask (B_CR_BIMR8MASK_0_0_0_MCHBAR)—Offset 6974h	0h
6978h	697Fh	IMR8 Control Policy (B_CR_BIMR8CP_0_0_0_MCHBAR)—Offset 6978h	C0061010202h
6980h	6987h	IMR8 Read Access Policy (B_CR_BIMR8RAC_0_0_0_MCHBAR)—Offset 6980h	0h
6988h	698Fh	IMR8 Write Access Policy (B_CR_BIMR8WAC_0_0_0_MCHBAR)—Offset 6988h	0h

Table 5-9. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6990h	6993h	IMR9 Base (B_CR_BIMR9BASE_0_0_0_MCHBAR)—Offset 6990h	0h
6994h	6997h	IMR9 Mask (B_CR_BIMR9MASK_0_0_0_MCHBAR)—Offset 6994h	0h
6998h	699Fh	IMR9 Control Policy (B_CR_BIMR9CP_0_0_0_MCHBAR)—Offset 6998h	C0061010202h
69A0h	69A7h	IMR9 Read Access Policy (B_CR_BIMR9RAC_0_0_0_MCHBAR)—Offset 69A0h	0h
69A8h	69AFh	IMR9 Write Access Policy (B_CR_BIMR9WAC_0_0_0_MCHBAR)—Offset 69A8h	0h
69B0h	69B3h	IMR10 Base (B_CR_BIMR10BASE_0_0_0_MCHBAR)—Offset 69B0h	0h
69B4h	69B7h	IMR10 Mask (B_CR_BIMR10MASK_0_0_0_MCHBAR)—Offset 69B4h	0h
69B8h	69BFh	IMR10 Control Policy (B_CR_BIMR10CP_0_0_0_MCHBAR)—Offset 69B8h	C0061010202h
69C0h	69C7h	IMR10 Read Access Policy (B_CR_BIMR10RAC_0_0_0_MCHBAR)—Offset 69C0h	0h
69C8h	69CFh	IMR10 Write Access Policy (B_CR_BIMR10WAC_0_0_0_MCHBAR)—Offset 69C8h	0h
69D0h	69D3h	IMR11 Base (B_CR_BIMR11BASE_0_0_0_MCHBAR)—Offset 69D0h	0h
69D4h	69D7h	IMR11 Mask (B_CR_BIMR11MASK_0_0_0_MCHBAR)—Offset 69D4h	0h
69D8h	69DFh	IMR11 Control Policy (B_CR_BIMR11CP_0_0_0_MCHBAR)—Offset 69D8h	C0061010202h
69E0h	69E7h	IMR11 Read Access Policy (B_CR_BIMR11RAC_0_0_0_MCHBAR)—Offset 69E0h	0h
69E8h	69EFh	IMR11 Write Access Policy (B_CR_BIMR11WAC_0_0_0_MCHBAR)—Offset 69E8h	0h
69F0h	69F3h	IMR12 Base (B_CR_BIMR12BASE_0_0_0_MCHBAR)—Offset 69F0h	0h
69F4h	69F7h	IMR12 Mask (B_CR_BIMR12MASK_0_0_0_MCHBAR)—Offset 69F4h	0h
69F8h	69FFh	IMR12 Control Policy (B_CR_BIMR12CP_0_0_0_MCHBAR)—Offset 69F8h	C0061010202h
6A00h	6A07h	IMR12 Read Access Policy (B_CR_BIMR12RAC_0_0_0_MCHBAR)—Offset 6A00h	0h
6A08h	6A0Fh	IMR12 Write Access Policy (B_CR_BIMR12WAC_0_0_0_MCHBAR)—Offset 6A08h	0h
6A10h	6A13h	IMR13 Base (B_CR_BIMR13BASE_0_0_0_MCHBAR)—Offset 6A10h	0h
6A14h	6A17h	IMR13 Mask (B_CR_BIMR13MASK_0_0_0_MCHBAR)—Offset 6A14h	0h
6A18h	6A1Fh	IMR13 Control Policy (B_CR_BIMR13CP_0_0_0_MCHBAR)—Offset 6A18h	C0061010202h
6A20h	6A27h	IMR13 Read Access Policy (B_CR_BIMR13RAC_0_0_0_MCHBAR)—Offset 6A20h	0h
6A28h	6A2Fh	IMR13 Write Access Policy (B_CR_BIMR13WAC_0_0_0_MCHBAR)—Offset 6A28h	0h

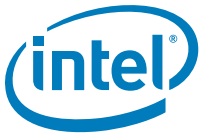


Table 5-9. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6A30h	6A33h	IMR14 Base (B_CR_BIMR14BASE_0_0_0_MCHBAR)—Offset 6A30h	0h
6A34h	6A37h	IMR14 Mask (B_CR_BIMR14MASK_0_0_0_MCHBAR)—Offset 6A34h	0h
6A38h	6A3Fh	IMR14 Control Policy (B_CR_BIMR14CP_0_0_0_MCHBAR)—Offset 6A38h	C0061010202h
6A40h	6A47h	IMR14 Read Access Policy (B_CR_BIMR14RAC_0_0_0_MCHBAR)—Offset 6A40h	0h
6A48h	6A4Fh	IMR14 Write Access Policy (B_CR_BIMR14WAC_0_0_0_MCHBAR)—Offset 6A48h	0h
6A50h	6A53h	IMR15 Base (B_CR_BIMR15BASE_0_0_0_MCHBAR)—Offset 6A50h	0h
6A54h	6A57h	IMR15 Mask (B_CR_BIMR15MASK_0_0_0_MCHBAR)—Offset 6A54h	0h
6A58h	6A5Fh	IMR15 Control Policy (B_CR_BIMR15CP_0_0_0_MCHBAR)—Offset 6A58h	C0061010202h
6A60h	6A67h	IMR15 Read Access Policy (B_CR_BIMR15RAC_0_0_0_MCHBAR)—Offset 6A60h	0h
6A68h	6A6Fh	IMR15 Write Access Policy (B_CR_BIMR15WAC_0_0_0_MCHBAR)—Offset 6A68h	0h
6A70h	6A73h	IMR16 Base (B_CR_BIMR16BASE_0_0_0_MCHBAR)—Offset 6A70h	0h
6A74h	6A77h	IMR16 Mask (B_CR_BIMR16MASK_0_0_0_MCHBAR)—Offset 6A74h	0h
6A78h	6A7Fh	IMR16 Control Policy (B_CR_BIMR16CP_0_0_0_MCHBAR)—Offset 6A78h	C0061010202h
6A80h	6A87h	IMR16 Read Access Policy (B_CR_BIMR16RAC_0_0_0_MCHBAR)—Offset 6A80h	0h
6A88h	6A8Fh	IMR16 Write Access Policy (B_CR_BIMR16WAC_0_0_0_MCHBAR)—Offset 6A88h	0h
6A90h	6A93h	IMR17 Base (B_CR_BIMR17BASE_0_0_0_MCHBAR)—Offset 6A90h	0h
6A94h	6A97h	IMR17 Mask (B_CR_BIMR17MASK_0_0_0_MCHBAR)—Offset 6A94h	0h
6A98h	6A9Fh	IMR17 Control Policy (B_CR_BIMR17CP_0_0_0_MCHBAR)—Offset 6A98h	C0061010202h
6AA0h	6AA7h	IMR17 Read Access Policy (B_CR_BIMR17RAC_0_0_0_MCHBAR)—Offset 6AA0h	0h
6AA8h	6AAFh	IMR17 Write Access Policy (B_CR_BIMR17WAC_0_0_0_MCHBAR)—Offset 6AA8h	0h
6AB0h	6AB3h	IMR18 Base (B_CR_BIMR18BASE_0_0_0_MCHBAR)—Offset 6AB0h	0h
6AB4h	6AB7h	IMR18 Mask (B_CR_BIMR18MASK_0_0_0_MCHBAR)—Offset 6AB4h	0h
6AB8h	6ABFh	IMR18 Control Policy (B_CR_BIMR18CP_0_0_0_MCHBAR)—Offset 6AB8h	C0061010202h
6AC0h	6AC7h	IMR18 Read Access Policy (B_CR_BIMR18RAC_0_0_0_MCHBAR)—Offset 6AC0h	0h
6AC8h	6ACFh	IMR18 Write Access Policy (B_CR_BIMR18WAC_0_0_0_MCHBAR)—Offset 6AC8h	0h

Table 5-9. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6AD0h	6AD3h	IMR19 Base (B_CR_BIMR19BASE_0_0_0_MCHBAR)—Offset 6AD0h	0h
6AD4h	6AD7h	IMR19 Mask (B_CR_BIMR19MASK_0_0_0_MCHBAR)—Offset 6AD4h	0h
6AD8h	6ADFh	IMR19 Control Policy (B_CR_BIMR19CP_0_0_0_MCHBAR)—Offset 6AD8h	C0061010202h
6AE0h	6AE7h	IMR19 Read Access Policy (B_CR_BIMR19RAC_0_0_0_MCHBAR)—Offset 6AE0h	0h
6AE8h	6AEFh	IMR19 Write Access Policy (B_CR_BIMR19WAC_0_0_0_MCHBAR)—Offset 6AE8h	0h
6AF0h	6AF3h	MOT Out Base (B_CR_MOT_OUT_BASE_0_0_0_MCHBAR)—Offset 6AF0h	0h
6AF4h	6AF7h	MOT Out Mask (B_CR_MOT_OUT_MASK_0_0_0_MCHBAR)—Offset 6AF4h	0h
6AF8h	6AFFh	MOT Buffer Control Policy (B_CR_BMOT_BUF_CP_0_0_0_MCHBAR)—Offset 6AF8h	C0061010202h
6B00h	6B07h	MOT Buffer Read Access Policy (B_CR_BMOT_BUF_RAC_0_0_0_MCHBAR)—Offset 6B00h	60010017h
6B08h	6B0Fh	MOT Buffer Write Access Policy (B_CR_BMOT_BUF_WAC_0_0_0_MCHBAR)—Offset 6B08h	60010000h
6B10h	6B17h	IMR Global BM Control Policy (B_CR_BIMRGLOBAL_BM_CP_0_0_0_MCHBAR)—Offset 6B10h	C0061010202h
6B18h	6B1Fh	IMR Global BM Read Access Control (B_CR_BIMRGLOBAL_BM_RAC_0_0_0_MCHBAR)—Offset 6B18h	FFFFFFFFFFFFFFFFh
6B20h	6B27h	IMR Global BM Write Access Policy (B_CR_BIMRGLOBAL_BM_WAC_0_0_0_MCHBAR)—Offset 6B20h	C0061010202h
6B28h	6B2Fh	Graphics Stolen Memory Control Policy (B_CR_BGSMCP_0_0_0_MCHBAR)—Offset 6B28h	C0061010202h
6B30h	6B37h	GSM Read Access Policy (B_CR_BGSMRAC_0_0_0_MCHBAR)—Offset 6B30h	100060010100h
6B38h	6B3Fh	GSM Write Access Policy (B_CR_BGSMWAC_0_0_0_MCHBAR)—Offset 6B38h	100060010100h
6B40h	6B47h	TPM Control Policy (B_CR_TPM_CP_0_0_0_MCHBAR)—Offset 6B40h	C0061010202h
6B48h	6B4Fh	TPM Access Control (B_CR_TPM_AC_0_0_0_MCHBAR)—Offset 6B48h	C0061010202h
6B50h	6B53h	BGSM Control Register (B_CR_BGSM_CTRL_0_0_0_MCHBAR)—Offset 6B50h	19h
6B54h	6B57h	SMM Control Register (B_CR_BSMR_CTRL_0_0_0_MCHBAR)—Offset 6B54h	7h
6B58h	6B5Bh	Default VTd Control Register (B_CR_BDEFVTDPMR_CTRL_0_0_0_MCHBAR)—Offset 6B58h	1Ch
6B7Ch	6B7Fh	MOT Trigger Trace Control (B_CR_MOT_TRIG_TRACE_CTRL_0_0_0_MCHBAR)—Offset 6B7Ch	E0000000h
6B80h	6B87h	MOT Slice 0 Memory Pointer (B_CR_MOT_SLICE_0_MEM_PTR_0_0_0_MCHBAR)—Offset 6B80h	2h

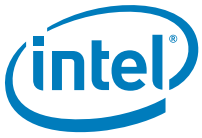


Table 5-9. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6B88h	6B8Fh	MOT Slice 1 Memory Pointer (B_CR_MOT_SLICE_1_MEM_PTR_0_0_0_MCHBAR)—Offset 6B88h	2h
6B90h	6B93h	MOT Slice 0 Record ID (B_CR_MOT_SLICE_0_RECORD_ID_0_0_0_MCHBAR)—Offset 6B90h	0h
6B94h	6B97h	MOT Slice 1 Record ID (B_CR_MOT_SLICE_1_RECORD_ID_0_0_0_MCHBAR)—Offset 6B94h	0h
6BA0h	6BA7h	MOT Filter Match 0 (B_CR_MOT_FILTER_MATCH0_0_0_0_MCHBAR)—Offset 6BA0h	0h
6BA8h	6BAFh	MOT Filter Mask (B_CR_MOT_FILTER_MASK0_0_0_0_MCHBAR)—Offset 6BA8h	7FFFFFFFE0h
6BB0h	6BB7h	MOT Filter Match 1 (B_CR_MOT_FILTER_MATCH1_0_0_0_MCHBAR)—Offset 6BB0h	0h
6BB8h	6BBFh	MOT Filter Mask 1 (B_CR_MOT_FILTER_MASK1_0_0_0_MCHBAR)—Offset 6BB8h	7FFFFFFFE0h
6BC0h	6BC7h	MOT Filter Misc 0 (B_CR_MOT_FILTER_MISC0_0_0_0_MCHBAR)—Offset 6BC0h	0h
6BC8h	6BCFh	MOT Filter Misc 1 (B_CR_MOT_FILTER_MISC1_0_0_0_MCHBAR)—Offset 6BC8h	0h
6BD0h	6BD7h	MOT Trigger Match 0 (B_CR_MOT_TRIGGER_MATCH0_0_0_0_MCHBAR)—Offset 6BD0h	0h
6BD8h	6BDFh	MOT Trigger Mask 0 (B_CR_MOT_TRIGGER_MASK0_0_0_0_MCHBAR)—Offset 6BD8h	7FFFFFFFE0h
6BE0h	6BE7h	MOT Trigger Match 1 (B_CR_MOT_TRIGGER_MATCH1_0_0_0_MCHBAR)—Offset 6BE0h	0h
6BE8h	6BEFh	MOT Trigger Mask 1 (B_CR_MOT_TRIGGER_MASK1_0_0_0_MCHBAR)—Offset 6BE8h	7FFFFFFFE0h
6BF0h	6BF7h	MOT Trigger Misc 0 (B_CR_MOT_TRIGGER_MISC0_0_0_0_MCHBAR)—Offset 6BF0h	0h
6BF8h	6BFFh	MOT Trigger Misc 1 (B_CR_MOT_TRIGGER_MISC1_0_0_0_MCHBAR)—Offset 6BF8h	0h
6C00h	6C03h	MOT PSMI Sync (B_CR_MOT_PSMI_SYNC_0_0_0_MCHBAR)—Offset 6C00h	0h
6C08h	6C0Fh	BIOSWR Control Policy (B_CR_BIOSWR_CP_0_0_0_MCHBAR)—Offset 6C08h	C0061010202h
6C10h	6C17h	BIOSWR Read Access Policy (B_CR_BIOSWR_RAC_0_0_0_MCHBAR)—Offset 6C10h	80000C00630D0217h
6C18h	6C1Fh	BIOSWR Write Access Policy (B_CR_BIOSWR_WAC_0_0_0_MCHBAR)—Offset 6C18h	C00610C0212h
6C24h	6C27h	TPM Selector (B_CR_TPM_SELECTOR_0_0_0_MCHBAR)—Offset 6C24h	0h
6C28h	6C2Fh	B-Unit Pcode/Ucode Write, All Read Control Policy Register (B_CR_P_U_CODEWR_ALLRD_CP_0_0_0_MCHBAR)—Offset 6C28h	40001000202h

Table 5-9. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6C30h	6C37h	B-Unit Pcode/Ucode Read Access Policy (B_CR_P_U_CODEWR_ALLRD_RAC_0_0_0_MCHBAR)—Offset 6C30h	FFFFFFFFFFFFFFFFh
6C38h	6C3Fh	B-Unit Pcode/Ucode Write Access Policy (B_CR_P_U_CODEWR_ALLRD_WAC_0_0_0_MCHBAR)—Offset 6C38h	40001000202h
6C80h	6C87h	Default VTd BAR (B_CR_DEFVTDBAR_0_0_0_MCHBAR)—Offset 6C80h	0h
6C88h	6C8Fh	Gfx VTd BAR (B_CR_GFXVTDBAR_0_0_0_MCHBAR)—Offset 6C88h	0h
6C90h	6C93h	B-Unit Lites Group 0 Control (B_CR_LITES0_CTL_0_0_0_MCHBAR)—Offset 6C90h	0h
6C94h	6C97h	B-Unit Lites Group 0 Opcode Match Filter (B_CR_LITES0_OPCODE_MATCH_0_0_0_MCHBAR)—Offset 6C94h	0h
6C98h	6C9Bh	B-Unit Lites Group 0 Agent Match Filter (B_CR_LITES0_AGENT_MATCH_0_0_0_MCHBAR)—Offset 6C98h	0h
6C9Ch	6C9Fh	B-Unit Lites Group 0 U2C IntData Match Filter (B_CR_LITES0_U2CINTDATA_MATCH_0_0_0_MCHBAR)—Offset 6C9Ch	0h
6CA0h	6CA7h	B-Unit Lites Group 0 Address Match Filter LITES0_ADDR_MATCH (B_CR_LITES0_ADDR_MATCH_0_0_0_MCHBAR)—Offset 6CA0h	0h
6CA8h	6CAFh	B-Unit Lites Group 0 Address Mask Filter LITES0_ADDR_MASK (B_CR_LITES0_ADDR_MASK_0_0_0_MCHBAR)—Offset 6CA8h	0h
6CB0h	6CB3h	B-Unit Lites Group 0 Data Match Filter LITES0_DATA_MATCH (B_CR_LITES0_DATA_MATCH_0_0_0_MCHBAR)—Offset 6CB0h	0h
6CB4h	6CB7h	B-Unit Lites Group 0 Data Mask Filter LITES0_DATA_MASK (B_CR_LITES0_DATA_MASK_0_0_0_MCHBAR)—Offset 6CB4h	0h
6CC0h	6CC3h	B-Unit Lites Group 1 Control (B_CR_LITES1_CTL_0_0_0_MCHBAR)—Offset 6CC0h	0h
6CC4h	6CC7h	B-Unit Lites Group 1 Opcode Match Filter (B_CR_LITES1_OPCODE_MATCH_0_0_0_MCHBAR)—Offset 6CC4h	0h
6CC8h	6CCBh	B-Unit Lites Group 1 Agent Match Filter (B_CR_LITES1_AGENT_MATCH_0_0_0_MCHBAR)—Offset 6CC8h	0h
6CCCh	6CCFh	B-Unit Lites Group 1 U2C IntData Match Filter (B_CR_LITES1_U2CINTDATA_MATCH_0_0_0_MCHBAR)—Offset 6CCCh	0h
6CD0h	6CD7h	B-Unit Lites Group 1 Address Match Filter LITES1_ADDR_MATCH (B_CR_LITES1_ADDR_MATCH_0_0_0_MCHBAR)—Offset 6CD0h	0h
6CD8h	6CDFh	B-Unit Lites Group 1 Address Mask Filter LITES1_ADDR_MASK (B_CR_LITES1_ADDR_MASK_0_0_0_MCHBAR)—Offset 6CD8h	0h
6CE0h	6CE3h	B-Unit Lites Group 1 Data Match Filter LITES1_DATA_MATCH (B_CR_LITES1_DATA_MATCH_0_0_0_MCHBAR)—Offset 6CE0h	0h
6CE4h	6CE7h	B-Unit Lites Group 1 Data Mask Filter LITES1_DATA_MASK (B_CR_LITES1_DATA_MASK_0_0_0_MCHBAR)—Offset 6CE4h	0h

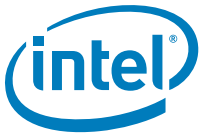


Table 5-9. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6CF0h	6CF3h	B-Unit Lites Group 2 Control (B_CR_LITES2_CTL_0_0_0_MCHBAR)—Offset 6CF0h	0h
6CF4h	6CF7h	B-Unit Lites Group 2 Opcode Match Filter (B_CR_LITES2_OPCODE_MATCH_0_0_0_MCHBAR)—Offset 6CF4h	0h
6CF8h	6CFBh	B-Unit Lites Group 2 Agent Match Filter (B_CR_LITES2_AGENT_MATCH_0_0_0_MCHBAR)—Offset 6CF8h	0h
6CFCh	6CFFh	B-Unit Lites Group 2 U2C IntData Match Filter (B_CR_LITES2_U2CINTDATA_MATCH_0_0_0_MCHBAR)—Offset 6CFCh	0h
6D00h	6D07h	B-Unit Lites Group 2 Address Match Filter LITES2_ADDR_MATCH (B_CR_LITES2_ADDR_MATCH_0_0_0_MCHBAR)—Offset 6D00h	0h
6D08h	6D0Fh	B-Unit Lites Group 2 Address Mask Filter LITES2_ADDR_MASK (B_CR_LITES2_ADDR_MASK_0_0_0_MCHBAR)—Offset 6D08h	0h
6D10h	6D13h	B-Unit Lites Group 2 Data Match Filter LITES2_DATA_MATCH (B_CR_LITES2_DATA_MATCH_0_0_0_MCHBAR)—Offset 6D10h	0h
6D14h	6D17h	B-Unit Lites Group 2 Data Mask Filter LITES2_DATA_MASK (B_CR_LITES2_DATA_MASK_0_0_0_MCHBAR)—Offset 6D14h	0h
6D20h	6D23h	B-Unit Lites Group 3 Control (B_CR_LITES3_CTL_0_0_0_MCHBAR)—Offset 6D20h	0h
6D24h	6D27h	B-Unit Lites Group 3 Opcode Match Filter (B_CR_LITES3_OPCODE_MATCH_0_0_0_MCHBAR)—Offset 6D24h	0h
6D28h	6D2Bh	B-Unit Lites Group 3 Agent Match Filter (B_CR_LITES3_AGENT_MATCH_0_0_0_MCHBAR)—Offset 6D28h	0h
6D2Ch	6D2Fh	B-Unit Lites Group 3 U2C IntData Match Filter (B_CR_LITES3_U2CINTDATA_MATCH_0_0_0_MCHBAR)—Offset 6D2Ch	0h
6D30h	6D37h	B-Unit Lites Group 3 Address Match Filter LITES3_ADDR_MATCH (B_CR_LITES3_ADDR_MATCH_0_0_0_MCHBAR)—Offset 6D30h	0h
6D38h	6D3Fh	B-Unit Lites Group 3 Address Mask Filter LITES3_ADDR_MASK (B_CR_LITES3_ADDR_MASK_0_0_0_MCHBAR)—Offset 6D38h	0h
6D40h	6D43h	B-Unit Lites Group 3 Data Match Filter LITES3_DATA_MATCH (B_CR_LITES3_DATA_MATCH_0_0_0_MCHBAR)—Offset 6D40h	0h
6D44h	6D47h	B-Unit Lites Group 3 Data Mask Filter LITES3_DATA_MASK (B_CR_LITES3_DATA_MASK_0_0_0_MCHBAR)—Offset 6D44h	0h
6D48h	6D4Bh	B-Unit Lites and Emon Master Control LITESEMONCTL (B_CR_LITESEMON_CTL_0_0_0_MCHBAR)—Offset 6D48h	0h
6D4Ch	6D4Fh	B-Unit Arbiter Control BARBCTRL0 (B_CR_BARBCTRL0)—Offset 6D4Ch	4040404h
6D50h	6D53h	B-Unit Arbiter Control BARBCTRL1 (B_CR_BARBCTRL1)—Offset 6D50h	4040404h
6D54h	6D57h	B-Unit Scheduler Control (B_CR_BSCHWT0)—Offset 6D54h	4040404h
6D58h	6D5Bh	B-Unit Scheduler Control (B_CR_BSCHWT1)—Offset 6D58h	4040404h
6D5Ch	6D5Fh	B-Unit Scheduler Control (B_CR_BSCHWT2)—Offset 6D5Ch	4040404h

Table 5-9. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6D60h	6D63h	B-Unit Scheduler Control (B_CR_BSCHWT3)—Offset 6D60h	4040404h
6D64h	6D67h	B-Unit Flush Control (B_CR_BWFLUSH)—Offset 6D64h	FF010000h
6D68h	6D6Bh	B-Unit Flush Weights (B_CR_BFLWT)—Offset 6D68h	404h
6D6Ch	6D6Fh	Weighted Scheduling Control of High Priority ISOC and Other Requests (B_CR_BISOCWT)—Offset 6D6Ch	80003F0Fh
6D70h	6D73h	B-Unit Control (B_CR_BCTRL2)—Offset 6D70h	F0034h
6D74h	6D77h	Asset Classification Bits (B_CR_AC_RS0_0_0_0_MCHBAR)—Offset 6D74h	100000h
6D78h	6D7Bh	IDI Real-Time Feature Configuration Bits (B_CR_RT_EN_0_0_0_MCHBAR)—Offset 6D78h	0h
6D7Ch	6D7Fh	B-Unit Control Register 3 (B_CR_BCTRL3)—Offset 6D7Ch	140h
6E40h	6E43h	Asymmetric Memory Region 0 With No Interleaving Configuration (B_CR_ASYM_MEM_REGION0_0_0_0_MCHBAR)—Offset 6E40h	0h
6E44h	6E47h	Asymmetric Memory Region 1 With No Interleaving Configuration (B_CR_ASYM_MEM_REGION1_0_0_0_MCHBAR)—Offset 6E44h	0h
6E48h	6E4Bh	B-Unit Machine Check Mode Low (B_CR_BMCMODE_LOW)—Offset 6E48h	1h
6E4Ch	6E4Fh	B-Unit Machine Check Mode High (B_CR_BMCMODE_HIGH)—Offset 6E4Ch	0h
6E50h	6E53h	Two-Way Asymmetric Memory Region Configuration (B_CR_ASYM_2WAY_MEM_REGION_0_0_0_MCHBAR)—Offset 6E50h	0h

5.9.1 B-Unit Miscellaneous Configuration (B_CR_BMISC_0_0_0_MCHBAR)—Offset 6800h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 7h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RESERVED_0):** Reserved.
3	0h RW	**Send Boot Vector to DRAM (SEND_BOOT_VECTOR_TO_DRAM):** When set,IA accesses to 0xFFFF_0000 to 0XFFFF_FFFF will be sent to memory, regardless of the Host IO Boundary setting in TOLUD.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW	**ABSeginDRAM Legacy Video Area (ABSEGINDRAM):** When this bit is set, reads and writes targeting A or Bsegments are routed to DRAM. Asegment corresponds to the memory range 0xA_0000 to 0xA_FFFF. Bsegment corresponds to the memory ranges 0xB_0000 to 0xB_7FFF and 0xB_8000 to 0xB_FFFF.
1	1h RW	**Read FSeg from DRAM (READ_FSEG_FROM_DRAM):** When this bit is set, reads targeting Fsegment are routed to DRAM. Fsegment corresponds to the memory range 0xF_0000 to 0xF_FFFF.
0	1h RW	**Read ESeg from DRAM (READ_ESEG_FROM_DRAM):** When this bit is set, reads targeting Esegment are routed to DRAM. Esegment corresponds to the memory range 0xE_0000 to 0xE_FFFF.

5.9.2 Security Control Policy (B_CR_SECURITY_CP_0_0_0_MCHBAR)—Offset 6808h

This register controls the access policy to the B-Unit SEC Read Access Control Policy SECURITY_RAC, Write Access Control policy registers SECURITY_WAC, and self-referentially to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RO	**Security Control Policy (SEC_SAI_POL):** Bit vector used to determine which agents are allowed access to the SECURITY_RAC, SECURITY_WAC and SECURITY_CP registers, based on the value from each agent's 6bit SAI field.

5.9.3 Security Group Read Access Policy (B_CR_SECURITY_RAC_0_0_0_MCHBAR)—Offset 6810h

This register configures the Read Access Policy for the B-Unit Security Group registers. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RO	**Security SAI Read Access Policy (SEC_SAI_POL):** Bit vector used to determine which agents are allowed read access to the B-Unit Security Group Configuration registers based on each agent's 6bit encoded SAI value.

5.9.4 Security Group Write Access Policy (B_CR_SECURITY_WAC_0_0_0_MCHBAR)—Offset 6818h

This register configures the Write Access Policy for the B-Unit Security Group registers. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RO	**Security SAI Write Access Policy (SEC_SAI_POL):** Bit vector used to determine which agents are allowed write access to the B-Unit Security Group Configuration registers, based on each agent's 6bit encoded SAI value.

5.9.5 Slice 0 Memory Access Count (B_CR_MEM_ACCESS_COUNT_SLICE0)—Offset 6868h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Memory Access Count (MEM_ACCESS_COUNT):** Counts the number of PMI transactions that the B-Unit has sent to any PMI channel. Counts both reads and writes. Counter is not saturating and will roll over to zero. It is up to the consumer of the counter to handle roll over cases.

5.9.6 Slice 1 Memory Access Count (B_CR_MEM_ACCESS_COUNT_SLICE1)—Offset 686Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Memory Access Count (MEM_ACCESS_COUNT):** Counts the number of PMI transactions that the B-Unit has sent to any PMI channel. Counts both reads and writes. Counter is not saturating and will roll over to zero. It is up to the consumer of the counter to handle roll over cases.

5.9.7 IMR0 Base (B_CR_BIMR0BASE_0_0_0_MCHBAR)—Offset 6870h

This register, along with IMR0MASK, IMR0RAC, and IMR0WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR0RAC and IMR0WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR0 Base (IMR0_BASE):** Specifies bits 38:10 of the start address of IMR0 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR0MASK[28:0] applied to bits 38:10 of the incoming address, to determine if an access falls within the IMR0 defined region.

5.9.8 IMR0 Mask (B_CR_BIMR0MASK_0_0_0_MCHBAR)—Offset 6874h

This register, along with IMR0BASE, IMR0RAC, and IMR0WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR0RAC and IMR0WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit WB Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables return to the requester of implicit writeback HITM data from GT. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit WB Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester, depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR0 Mask (IMR0_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR0BASE[28:0] value. A match indicates that the incoming address falls within the IMR0 region.

5.9.9 IMR0 Control Policy (B_CR_BIMR0CP_0_0_0_MCHBAR)—Offset 6878h

This register controls the access policy to the Read Access Policy BIMR0RAC, Write Access Policy BIMR0WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR0 Control Policy (IMR0_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR0RAC, BIMR0WAC and BIMR0CP registers based on the value from each agent's 6bit SAI field.

5.9.10 IMR0 Read Access Policy (B_CR_BIMR0RAC_0_0_0_MCHBAR)—Offset 6880h

This register, along with IMR0BASE, IMR0MASK and IMR0WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR0. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR0 Read Access Policy 63 (IMR0_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR0 Read Access Policy 62 (IMR0_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR0 Read Access Policy 61 (IMR0_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR0 Read Access Policy 60 (IMR0_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR0 Read Access Policy 59 (IMR0_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR0 Read Access Policy 58 (IMR0_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
57	0h RO	**IMR0 Read Access Policy 57 (IMR0_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR0 Read Access Policy 56 (IMR0_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR0 Read Access Policy 55 (IMR0_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR0 Read Access Policy 54 (IMR0_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR0 Read Access Policy 53 (IMR0_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR0 Read Access Policy 52 (IMR0_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR0 Read Access Policy 51 (IMR0_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR0 Read Access Policy 50 (IMR0_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR0 Read Access Policy 49 (IMR0_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR0 Read Access Policy 48 (IMR0_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR0 Read Access Policy 47 (IMR0_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR0 Read Access Policy 46 (IMR0_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR0 Read Access Policy 45 (IMR0_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR0 Read Access Policy 44 (IMR0_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR0 Read Access Policy 43 (IMR0_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
42	0h RW	**IMR0 Read Access Policy 42 (IMR0_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR0 Read Access Policy 41 (IMR0_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR0 Read Access Policy 40 (IMR0_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR0 Read Access Policy 39 (IMR0_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR0 Read Access Policy 38 (IMR0_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR0 Read Access Policy 37 (IMR0_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR0 Read Access Policy 36 (IMR0_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR0 Read Access Policy 35 (IMR0_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR0 Read Access Policy 34 (IMR0_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR0 Read Access Policy 33 (IMR0_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR0 Read Access Policy 32 (IMR0_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR0 Read Access Policy 31 (IMR0_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR0 Read Access Policy 30 (IMR0_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR0 Read Access Policy 29 (IMR0_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR0 Read Access Policy 28 (IMR0_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW	**IMR0 Read Access Policy 27 (IMR0_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR0 Read Access Policy 26 (IMR0_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR0 Read Access Policy 25 (IMR0_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR0 Read Access Policy 24 (IMR0_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR0 Read Access Policy 23 (IMR0_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR0 Read Access Policy 22 (IMR0_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR0 Read Access Policy 21 (IMR0_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR0 Read Access Policy 20 (IMR0_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR0 Read Access Policy 19 (IMR0_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR0 Read Access Policy 18 (IMR0_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR0 Read Access Policy 17 (IMR0_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR0 Read Access Policy 16 (IMR0_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR0 Read Access Policy 15 (IMR0_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR0 Read Access Policy 14 (IMR0_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR0 Read Access Policy 13 (IMR0_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**IMR0 Read Access Policy 12 (IMR0_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR0 Read Access Policy 11 (IMR0_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR0 Read Access Policy 10 (IMR0_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR0 Read Access Policy 9 (IMR0_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR0 Read Access Policy 8 (IMR0_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR0 Read Access Policy 7 (IMR0_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR0 Read Access Policy 6 (IMR0_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR0 Read Access Policy 5 (IMR0_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR0 Read Access Policy 4 (IMR0_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR0 Read Access Policy 3 (IMR0_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR0 Read Access Policy 2 (IMR0_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR0 Read Access Policy 1 (IMR0_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR0 Read Access Policy 0 (IMR0_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR0 region, based on each agent's 6bit encoded SAI value.

5.9.11 IMR0 Write Access Policy (B_CR_BIMR0WAC_0_0_0_MCHBAR)—Offset 6888h

This register, along with IMR0BASE, IMR0MASK and IMR0RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR0. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR0 Write Access Policy 63 (IMR0_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR0 Write Access Policy 62 (IMR0_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR0 Write Access Policy 61 (IMR0_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR0 Write Access Policy 60 (IMR0_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR0 Write Access Policy 59 (IMR0_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR0 Write Access Policy 58 (IMR0_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR0 Write Access Policy 57 (IMR0_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR0 Write Access Policy 56 (IMR0_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR0 Write Access Policy 55 (IMR0_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR0 Write Access Policy 54 (IMR0_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
53	0h RO	**IMR0 Write Access Policy 53 (IMR0_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR0 Write Access Policy 52 (IMR0_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR0 Write Access Policy 51 (IMR0_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR0 Write Access Policy 50 (IMR0_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR0 Write Access Policy 49 (IMR0_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR0 Write Access Policy 48 (IMR0_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR0 Write Access Policy 47 (IMR0_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR0 Write Access Policy 46 (IMR0_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR0 Write Access Policy 45 (IMR0_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR0 Write Access Policy 44 (IMR0_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR0 Write Access Policy 43 (IMR0_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR0 Write Access Policy 42 (IMR0_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR0 Write Access Policy 41 (IMR0_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR0 Write Access Policy 40 (IMR0_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR0 Write Access Policy 39 (IMR0_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
38	0h RW	**IMR0 Write Access Policy 38 (IMR0_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR0 Write Access Policy 37 (IMR0_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR0 Write Access Policy 36 (IMR0_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR0 Write Access Policy 35 (IMR0_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR0 Write Access Policy 34 (IMR0_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR0 Write Access Policy 33 (IMR0_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR0 Write Access Policy 32 (IMR0_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR0 Write Access Policy 31 (IMR0_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR0 Write Access Policy 30 (IMR0_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR0 Write Access Policy 29 (IMR0_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR0 Write Access Policy 28 (IMR0_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR0 Write Access Policy 27 (IMR0_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR0 Write Access Policy 26 (IMR0_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR0 Write Access Policy 25 (IMR0_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR0 Write Access Policy 24 (IMR0_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**IMR0 Write Access Policy 23 (IMR0_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR0 Write Access Policy 22 (IMR0_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR0 Write Access Policy 21 (IMR0_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR0 Write Access Policy 20 (IMR0_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR0 Write Access Policy 19 (IMR0_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR0 Write Access Policy 18 (IMR0_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR0 Write Access Policy 17 (IMR0_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR0 Write Access Policy 16 (IMR0_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR0 Write Access Policy 15 (IMR0_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR0 Write Access Policy 14 (IMR0_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR0 Write Access Policy 13 (IMR0_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR0 Write Access Policy 12 (IMR0_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR0 Write Access Policy 11 (IMR0_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR0 Write Access Policy 10 (IMR0_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR0 Write Access Policy 9 (IMR0_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**IMR0 Write Access Policy 8 (IMR0_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR0 Write Access Policy 7 (IMR0_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR0 Write Access Policy 6 (IMR0_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR0 Write Access Policy 5 (IMR0_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR0 Write Access Policy 4 (IMR0_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR0 Write Access Policy 3 (IMR0_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR0 Write Access Policy 2 (IMR0_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR0 Write Access Policy 1 (IMR0_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR0 Write Access Policy 0 (IMR0_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR0 region, based on each agent's 6bit encoded SAI value.

5.9.12 IMR1 Base (B_CR_BIMR1BASE_0_0_0_MCHBAR)—Offset 6890h

This register, along with IMR1MASK, IMR1RAC and IMR1WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR1RAC and IMR1WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Trace Enable (TR_EN):** Asset Classification AC[0]: Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 1 IMR1 Base (IMR1_BASE):** Specifies bits 38:10 of the start address of IMR1 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR1MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR1 defined region.

5.9.13 IMR1 Mask (B_CR_BIMR1MASK_0_0_0_MCHBAR)—Offset 6894h

This register, along with IMR1BASE, IMR1RAC and IMR1WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR1RAC and IMR1WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**GT Implicit Writeback Enable (GT_IWB_EN):** Asset Classification AC[2]: Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables return to the requester of implicit writeback HITM data from GT. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester depending on the setting of the GT_IWB_EN bit.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 1 IMR1 Mask (IMR1_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR1BASE[28:0] value. A match indicates that the incoming address falls within the IMR1 region.

5.9.14 IMR1 Control Policy (B_CR_BIMR1CP_0_0_0_MCHBAR)—Offset 6898h

This register controls the access policy to the Read Access Policy BIMR1RAC, the Write Access Policy BIMR1WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR1 Control Policy (IMR1_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR1RAC, BIMR1WAC and BIMR1CP registers, based on the value from each agent's 6bit SAI field.

5.9.15 IMR1 Read Access Policy (B_CR_BIMR1RAC_0_0_0_MCHBAR)—Offset 68A0h

This register, along with IMR1BASE, IMR1MASK and IMR1WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR1. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR1 Read Access Policy 63 (IMR1_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR1 Read Access Policy 62 (IMR1_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR1 Read Access Policy 61 (IMR1_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR1 Read Access Policy 60 (IMR1_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR1 Read Access Policy 59 (IMR1_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR1 Read Access Policy 58 (IMR1_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR1 Read Access Policy 57 (IMR1_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR1 Read Access Policy 56 (IMR1_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR1 Read Access Policy 55 (IMR1_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR1 Read Access Policy 54 (IMR1_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR1 Read Access Policy 53 (IMR1_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR1 Read Access Policy 52 (IMR1_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR1 Read Access Policy 51 (IMR1_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR1 Read Access Policy 50 (IMR1_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR1 Read Access Policy 49 (IMR1_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**IMR1 Read Access Policy 48 (IMR1_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR1 Read Access Policy 47 (IMR1_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR1 Read Access Policy 46 (IMR1_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR1 Read Access Policy 45 (IMR1_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR1 Read Access Policy 44 (IMR1_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR1 Read Access Policy 43 (IMR1_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR1 Read Access Policy 42 (IMR1_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR1 Read Access Policy 41 (IMR1_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR1 Read Access Policy 40 (IMR1_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR1 Read Access Policy 39 (IMR1_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR1 Read Access Policy 38 (IMR1_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR1 Read Access Policy 37 (IMR1_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR1 Read Access Policy 36 (IMR1_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR1 Read Access Policy 35 (IMR1_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR1 Read Access Policy 34 (IMR1_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
33	0h RW	**IMR1 Read Access Policy 33 (IMR1_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR1 Read Access Policy 32 (IMR1_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR1 Read Access Policy 31 (IMR1_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR1 Read Access Policy 30 (IMR1_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR1 Read Access Policy 29 (IMR1_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR1 Read Access Policy 28 (IMR1_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR1 Read Access Policy 27 (IMR1_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR1 Read Access Policy 26 (IMR1_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR1 Read Access Policy 25 (IMR1_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR1 Read Access Policy 24 (IMR1_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR1 Read Access Policy 23 (IMR1_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR1 Read Access Policy 22 (IMR1_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR1 Read Access Policy 21 (IMR1_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR1 Read Access Policy 20 (IMR1_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR1 Read Access Policy 19 (IMR1_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**IMR1 Read Access Policy 18 (IMR1_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR1 Read Access Policy 17 (IMR1_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR1 Read Access Policy 16 (IMR1_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR1 Read Access Policy 15 (IMR1_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR1 Read Access Policy 14 (IMR1_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR1 Read Access Policy 13 (IMR1_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR1 Read Access Policy 12 (IMR1_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR1 Read Access Policy 11 (IMR1_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR1 Read Access Policy 10 (IMR1_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR1 Read Access Policy 9 (IMR1_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR1 Read Access Policy 8 (IMR1_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR1 Read Access Policy 7 (IMR1_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR1 Read Access Policy 6 (IMR1_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR1 Read Access Policy 5 (IMR1_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR1 Read Access Policy 4 (IMR1_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**IMR1 Read Access Policy 3 (IMR1_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR1 Read Access Policy 2 (IMR1_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR1 Read Access Policy 1 (IMR1_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR1 Read Access Policy 0 (IMR1_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR1 region, based on each agent's 6bit encoded SAI value.

5.9.16 IMR1 Write Access Policy (B_CR_BIMR1WAC_0_0_0_MCHBAR)—Offset 68A8h

This register, along with IMR1BASE, IMR1MASK and IMR1RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR1. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR1 Write Access Policy 63 (IMR1_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR1 Write Access Policy 62 (IMR1_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR1 Write Access Policy 61 (IMR1_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR1 Write Access Policy 60 (IMR1_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR1 Write Access Policy 59 (IMR1_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
58	0h RO	**IMR1 Write Access Policy 58 (IMR1_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR1 Write Access Policy 57 (IMR1_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR1 Write Access Policy 56 (IMR1_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR1 Write Access Policy 55 (IMR1_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR1 Write Access Policy 54 (IMR1_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR1 Write Access Policy 53 (IMR1_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR1 Write Access Policy 52 (IMR1_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR1 Write Access Policy 51 (IMR1_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR1 Write Access Policy 50 (IMR1_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR1 Write Access Policy 49 (IMR1_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR1 Write Access Policy 48 (IMR1_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR1 Write Access Policy 47 (IMR1_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR1 Write Access Policy 46 (IMR1_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR1 Write Access Policy 45 (IMR1_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR1 Write Access Policy 44 (IMR1_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
43	0h RW	**IMR1 Write Access Policy 43 (IMR1_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR1 Write Access Policy 42 (IMR1_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR1 Write Access Policy 41 (IMR1_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR1 Write Access Policy 40 (IMR1_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR1 Write Access Policy 39 (IMR1_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR1 Write Access Policy 38 (IMR1_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR1 Write Access Policy 37 (IMR1_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR1 Write Access Policy 36 (IMR1_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR1 Write Access Policy 35 (IMR1_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR1 Write Access Policy 34 (IMR1_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR1 Write Access Policy 33 (IMR1_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR1 Write Access Policy 32 (IMR1_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR1 Write Access Policy 31 (IMR1_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR1 Write Access Policy 30 (IMR1_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR1 Write Access Policy 29 (IMR1_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RW	**IMR1 Write Access Policy 28 (IMR1_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR1 Write Access Policy 27 (IMR1_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR1 Write Access Policy 26 (IMR1_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR1 Write Access Policy 25 (IMR1_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR1 Write Access Policy 24 (IMR1_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR1 Write Access Policy 23 (IMR1_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR1 Write Access Policy 22 (IMR1_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR1 Write Access Policy 21 (IMR1_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR1 Write Access Policy 20 (IMR1_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR1 Write Access Policy 19 (IMR1_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR1 Write Access Policy 18 (IMR1_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR1 Write Access Policy 17 (IMR1_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR1 Write Access Policy 16 (IMR1_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR1 Write Access Policy 15 (IMR1_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR1 Write Access Policy 14 (IMR1_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**IMR1 Write Access Policy 13 (IMR1_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR1 Write Access Policy 12 (IMR1_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR1 Write Access Policy 11 (IMR1_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR1 Write Access Policy 10 (IMR1_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR1 Write Access Policy 9 (IMR1_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR1 Write Access Policy 8 (IMR1_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR1 Write Access Policy 7 (IMR1_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR1 Write Access Policy 6 (IMR1_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR1 Write Access Policy 5 (IMR1_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR1 Write Access Policy 4 (IMR1_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR1 Write Access Policy 3 (IMR1_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR1 Write Access Policy 2 (IMR1_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR1 Write Access Policy 1 (IMR1_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR1 Write Access Policy 0 (IMR1_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR1 region, based on each agent's 6bit encoded SAI value.

5.9.17 Base 0 IMR2 Base (B_CR_BIMR2BASE_0_0_0_MCHBAR)—Offset 68B0h

This register, along with IMR2MASK, IMR2RAC and IMR2WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR2RAC and IMR2WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR2 Base (IMR2_BASE):** Specifies bits 38:10 of the start address of IMR2 region. IMR region size must be a strict power of two, at least 1KB and naturally aligned to the size. These bits are compared with the result of the IMR2MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR2 defined region.

5.9.18 IMR2 Mask (B_CR_BIMR2MASK_0_0_0_MCHBAR)—Offset 68B4h

This register, along with IMR2BASE, IMR2RAC, and IMR2WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR2RAC and IMR2WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR2 Mask (IMR2_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR2BASE[28:0] value. A match indicates that the incoming address falls within the IMR2 region.

5.9.19 IMR2 Control Policy (B_CR_BIMR2CP_0_0_0_MCHBAR)—Offset 68B8h

This register controls the access policy to the Read Access Policy BIMR2RAC, Write Access Policy BIMR2WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR2 Control Policy (IMR2_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR2RAC, BIMR2WAC and BIMR2CP registers, based on the value from each agent's 6bit SAI field.

5.9.20 IMR2 Read Access Policy (B_CR_BIMR2RAC_0_0_0_MCHBAR)—Offset 68C0h

This register, along with IMR2BASE, IMR2MASK and IMR2WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR2. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR2 Read Access Policy 63 (IMR2_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR2 Read Access Policy 62 (IMR2_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR2 Read Access Policy 61 (IMR2_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR2 Read Access Policy 60 (IMR2_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR2 Read Access Policy 59 (IMR2_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR2 Read Access Policy 58 (IMR2_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR2 Read Access Policy 57 (IMR2_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR2 Read Access Policy 56 (IMR2_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR2 Read Access Policy 55 (IMR2_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR2 Read Access Policy 54 (IMR2_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
53	0h RO	**IMR2 Read Access Policy 53 (IMR2_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR2 Read Access Policy 52 (IMR2_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR2 Read Access Policy 51 (IMR2_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR2 Read Access Policy 50 (IMR2_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR2 Read Access Policy 49 (IMR2_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR2 Read Access Policy 48 (IMR2_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR2 Read Access Policy 47 (IMR2_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR2 Read Access Policy 46 (IMR2_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR2 Read Access Policy 45 (IMR2_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR2 Read Access Policy 44 (IMR2_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR2 Read Access Policy 43 (IMR2_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR2 Read Access Policy 42 (IMR2_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR2 Read Access Policy 41 (IMR2_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR2 Read Access Policy 40 (IMR2_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR2 Read Access Policy 39 (IMR2_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
38	0h RW	**IMR2 Read Access Policy 38 (IMR2_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR2 Read Access Policy 37 (IMR2_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR2 Read Access Policy 36 (IMR2_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR2 Read Access Policy 35 (IMR2_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR2 Read Access Policy 34 (IMR2_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR2 Read Access Policy 33 (IMR2_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR2 Read Access Policy 32 (IMR2_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR2 Read Access Policy 31 (IMR2_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR2 Read Access Policy 30 (IMR2_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR2 Read Access Policy 29 (IMR2_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR2 Read Access Policy 28 (IMR2_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR2 Read Access Policy 27 (IMR2_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR2 Read Access Policy 26 (IMR2_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR2 Read Access Policy 25 (IMR2_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR2 Read Access Policy 24 (IMR2_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**IMR2 Read Access Policy 23 (IMR2_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR2 Read Access Policy 22 (IMR2_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR2 Read Access Policy 21 (IMR2_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR2 Read Access Policy 20 (IMR2_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR2 Read Access Policy 19 (IMR2_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR2 Read Access Policy 18 (IMR2_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR2 Read Access Policy 17 (IMR2_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR2 Read Access Policy 16 (IMR2_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR2 Read Access Policy 15 (IMR2_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR2 Read Access Policy 14 (IMR2_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR2 Read Access Policy 13 (IMR2_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR2 Read Access Policy 12 (IMR2_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR2 Read Access Policy 11 (IMR2_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR2 Read Access Policy 10 (IMR2_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR2 Read Access Policy 9 (IMR2_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**IMR2 Read Access Policy 8 (IMR2_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR2 Read Access Policy 7 (IMR2_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR2 Read Access Policy 6 (IMR2_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR2 Read Access Policy 5 (IMR2_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR2 Read Access Policy 4 (IMR2_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR2 Read Access Policy 3 (IMR2_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR2 Read Access Policy 2 (IMR2_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR2 Read Access Policy 1 (IMR2_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR2 Read Access Policy 0 (IMR2_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR2 region, based on each agent's 6bit encoded SAI value.

5.9.21 IMR2 Write Access Policy (B_CR_BIMR2WAC_0_0_0_MCHBAR)—Offset 68C8h

This register, along with IMR2BASE, IMR2MASK and IMR2RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR2. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR2 Write Access Policy 63 (IMR2_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR2 Write Access Policy 62 (IMR2_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR2 Write Access Policy 61 (IMR2_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR2 Write Access Policy 60 (IMR2_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR2 Write Access Policy 59 (IMR2_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR2 Write Access Policy 58 (IMR2_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR2 Write Access Policy 57 (IMR2_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR2 Write Access Policy 56 (IMR2_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR2 Write Access Policy 55 (IMR2_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR2 Write Access Policy 54 (IMR2_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR2 Write Access Policy 53 (IMR2_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR2 Write Access Policy 52 (IMR2_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR2 Write Access Policy 51 (IMR2_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR2 Write Access Policy 50 (IMR2_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR2 Write Access Policy 49 (IMR2_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**IMR2 Write Access Policy 48 (IMR2_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR2 Write Access Policy 47 (IMR2_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR2 Write Access Policy 46 (IMR2_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR2 Write Access Policy 45 (IMR2_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR2 Write Access Policy 44 (IMR2_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR2 Write Access Policy 43 (IMR2_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR2 Write Access Policy 42 (IMR2_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR2 Write Access Policy 41 (IMR2_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR2 Write Access Policy 40 (IMR2_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR2 Write Access Policy 39 (IMR2_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR2 Write Access Policy 38 (IMR2_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR2 Write Access Policy 37 (IMR2_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR2 Write Access Policy 36 (IMR2_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR2 Write Access Policy 35 (IMR2_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR2 Write Access Policy 34 (IMR2_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
33	0h RW	**IMR2 Write Access Policy 33 (IMR2_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR2 Write Access Policy 32 (IMR2_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR2 Write Access Policy 31 (IMR2_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR2 Write Access Policy 30 (IMR2_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR2 Write Access Policy 29 (IMR2_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR2 Write Access Policy 28 (IMR2_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR2 Write Access Policy 27 (IMR2_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR2 Write Access Policy 26 (IMR2_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR2 Write Access Policy 25 (IMR2_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR2 Write Access Policy 24 (IMR2_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR2 Write Access Policy 23 (IMR2_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR2 Write Access Policy 22 (IMR2_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR2 Write Access Policy 21 (IMR2_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR2 Write Access Policy 20 (IMR2_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR2 Write Access Policy 19 (IMR2_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**IMR2 Write Access Policy 18 (IMR2_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR2 Write Access Policy 17 (IMR2_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR2 Write Access Policy 16 (IMR2_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR2 Write Access Policy 15 (IMR2_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR2 Write Access Policy 14 (IMR2_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR2 Write Access Policy 13 (IMR2_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR2 Write Access Policy 12 (IMR2_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR2 Write Access Policy 11 (IMR2_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR2 Write Access Policy 10 (IMR2_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR2 Write Access Policy 9 (IMR2_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR2 Write Access Policy 8 (IMR2_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR2 Write Access Policy 7 (IMR2_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR2 Write Access Policy 6 (IMR2_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR2 Write Access Policy 5 (IMR2_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR2 Write Access Policy 4 (IMR2_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**IMR2 Write Access Policy 3 (IMR2_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR2 Write Access Policy 2 (IMR2_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR2 Write Access Policy 1 (IMR2_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR2 Write Access Policy 0 (IMR2_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR2 region, based on each agent's 6bit encoded SAI value.

5.9.22 IMR3 Base (B_CR_BIMR3BASE_0_0_0_MCHBAR)—Offset 68D0h

This register, along with IMR3MASK, IMR3RAC and IMR3WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR3RAC and IMR3WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR3 Base (IMR3_BASE):** Specifies bits 38:10 of the start address of IMR3 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR3MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR3 defined region.

5.9.23 IMR3 Mask (B_CR_BIMR3MASK_0_0_0_MCHBAR)—Offset 68D4h

This register, along with IMR3BASE, IMR3RAC and IMR3WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR3RAC and IMR3WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR3 Mask (IMR3_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR3BASE[28:0] value. A match indicates that the incoming address falls within the IMR3 region.

5.9.24 IMR3 Control Policy (B_CR_BIMR3CP_0_0_0_MCHBAR)—Offset 68D8h

This register controls the access policy to the Read Access Policy BIMR3RAC, the Write Access Policy BIMR3WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR3 Control Policy (IMR3_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR3RAC, BIMR3WAC and BIMR3CP registers, based on the value from each agent's 6bit SAI field.

5.9.25 IMR3 Read Access Policy (B_CR_BIMR3RAC_0_0_0_MCHBAR)—Offset 68E0h

This register, along with IMR3BASE, IMR3MASK and IMR3WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR3. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR3 Read Access Policy 63 (IMR3_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR3 Read Access Policy 62 (IMR3_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR3 Read Access Policy 61 (IMR3_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR3 Read Access Policy 60 (IMR3_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR3 Read Access Policy 59 (IMR3_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR3 Read Access Policy 58 (IMR3_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
57	0h RO	**IMR3 Read Access Policy 57 (IMR3_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR3 Read Access Policy 56 (IMR3_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR3 Read Access Policy 55 (IMR3_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR3 Read Access Policy 54 (IMR3_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR3 Read Access Policy 53 (IMR3_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR3 Read Access Policy 52 (IMR3_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR3 Read Access Policy 51 (IMR3_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR3 Read Access Policy 50 (IMR3_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR3 Read Access Policy 49 (IMR3_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR3 Read Access Policy 48 (IMR3_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR3 Read Access Policy 47 (IMR3_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR3 Read Access Policy 46 (IMR3_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR3 Read Access Policy 45 (IMR3_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR3 Read Access Policy 44 (IMR3_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR3 Read Access Policy 43 (IMR3_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
42	0h RW	**IMR3 Read Access Policy 42 (IMR3_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR3 Read Access Policy 41 (IMR3_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR3 Read Access Policy 40 (IMR3_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR3 Read Access Policy 39 (IMR3_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR3 Read Access Policy 38 (IMR3_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR3 Read Access Policy 37 (IMR3_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR3 Read Access Policy 36 (IMR3_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR3 Read Access Policy 35 (IMR3_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR3 Read Access Policy 34 (IMR3_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR3 Read Access Policy 33 (IMR3_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR3 Read Access Policy 32 (IMR3_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR3 Read Access Policy 31 (IMR3_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR3 Read Access Policy 30 (IMR3_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR3 Read Access Policy 29 (IMR3_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR3 Read Access Policy 28 (IMR3_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW	**IMR3 Read Access Policy 27 (IMR3_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR3 Read Access Policy 26 (IMR3_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR3 Read Access Policy 25 (IMR3_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR3 Read Access Policy 24 (IMR3_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR3 Read Access Policy 23 (IMR3_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR3 Read Access Policy 22 (IMR3_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR3 Read Access Policy 21 (IMR3_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR3 Read Access Policy 20 (IMR3_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR3 Read Access Policy 19 (IMR3_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR3 Read Access Policy 18 (IMR3_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR3 Read Access Policy 17 (IMR3_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR3 Read Access Policy 16 (IMR3_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR3 Read Access Policy 15 (IMR3_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR3 Read Access Policy 14 (IMR3_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR3 Read Access Policy 13 (IMR3_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**IMR3 Read Access Policy 12 (IMR3_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR3 Read Access Policy 11 (IMR3_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR3 Read Access Policy 10 (IMR3_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR3 Read Access Policy 9 (IMR3_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR3 Read Access Policy 8 (IMR3_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR3 Read Access Policy 7 (IMR3_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR3 Read Access Policy 6 (IMR3_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR3 Read Access Policy 5 (IMR3_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR3 Read Access Policy 4 (IMR3_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR3 Read Access Policy 3 (IMR3_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR3 Read Access Policy 2 (IMR3_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR3 Read Access Policy 1 (IMR3_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR3 Read Access Policy 0 (IMR3_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR3 region, based on each agent's 6bit encoded SAI value.

5.9.26 IMR3 Write Access Policy (B_CR_BIMR3WAC_0_0_0_MCHBAR)—Offset 68E8h

This register, along with IMR3BASE, IMR3MASK and IMR3RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR3. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR3 Write Access Policy 63 (IMR3_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR3 Write Access Policy 62 (IMR3_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR3 Write Access Policy 61 (IMR3_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR3 Write Access Policy 60 (IMR3_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR3 Write Access Policy 59 (IMR3_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR3 Write Access Policy 58 (IMR3_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR3 Write Access Policy 57 (IMR3_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR3 Write Access Policy 56 (IMR3_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR3 Write Access Policy 55 (IMR3_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR3 Write Access Policy 54 (IMR3_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
53	0h RO	**IMR3 Write Access Policy 53 (IMR3_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR3 Write Access Policy 52 (IMR3_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR3 Write Access Policy 51 (IMR3_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR3 Write Access Policy 50 (IMR3_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR3 Write Access Policy 49 (IMR3_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR3 Write Access Policy 48 (IMR3_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR3 Write Access Policy 47 (IMR3_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR3 Write Access Policy 46 (IMR3_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR3 Write Access Policy 45 (IMR3_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR3 Write Access Policy 44 (IMR3_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR3 Write Access Policy 43 (IMR3_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR3 Write Access Policy 42 (IMR3_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR3 Write Access Policy 41 (IMR3_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR3 Write Access Policy 40 (IMR3_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR3 Write Access Policy 39 (IMR3_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
38	0h RW	**IMR3 Write Access Policy 38 (IMR3_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR3 Write Access Policy 37 (IMR3_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR3 Write Access Policy 36 (IMR3_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR3 Write Access Policy 35 (IMR3_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR3 Write Access Policy 34 (IMR3_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR3 Write Access Policy 33 (IMR3_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR3 Write Access Policy 32 (IMR3_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR3 Write Access Policy 31 (IMR3_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR3 Write Access Policy 30 (IMR3_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR3 Write Access Policy 29 (IMR3_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR3 Write Access Policy 28 (IMR3_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR3 Write Access Policy 27 (IMR3_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR3 Write Access Policy 26 (IMR3_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR3 Write Access Policy 25 (IMR3_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR3 Write Access Policy 24 (IMR3_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**IMR3 Write Access Policy 23 (IMR3_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR3 Write Access Policy 22 (IMR3_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR3 Write Access Policy 21 (IMR3_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR3 Write Access Policy 20 (IMR3_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR3 Write Access Policy 19 (IMR3_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR3 Write Access Policy 18 (IMR3_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR3 Write Access Policy 17 (IMR3_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR3 Write Access Policy 16 (IMR3_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR3 Write Access Policy 15 (IMR3_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR3 Write Access Policy 14 (IMR3_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR3 Write Access Policy 13 (IMR3_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR3 Write Access Policy 12 (IMR3_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR3 Write Access Policy 11 (IMR3_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR3 Write Access Policy 10 (IMR3_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR3 Write Access Policy 9 (IMR3_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**IMR3 Write Access Policy 8 (IMR3_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR3 Write Access Policy 7 (IMR3_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR3 Write Access Policy 6 (IMR3_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR3 Write Access Policy 5 (IMR3_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR3 Write Access Policy 4 (IMR3_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR3 Write Access Policy 3 (IMR3_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR3 Write Access Policy 2 (IMR3_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR3 Write Access Policy 1 (IMR3_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR3 Write Access Policy 0 (IMR3_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR3 region, based on each agent's 6bit encoded SAI value.

5.9.27 IMR4 Base (B_CR_BIMR4BASE_0_0_0_MCHBAR)—Offset 68F0h

This register, along with IMR4MASK, IMR4RAC and IMR4WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR4RAC and IMR4WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR4 Base (IMR4_BASE):** Specifies bits 38:10 of the start address of IMR4 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR4MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR4 defined region.

5.9.28 IMR4 Mask (B_CR_BIMR4MASK_0_0_0_MCHBAR)—Offset 68F4h

This register, along with IMR4BASE, IMR4RAC and IMR4WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR4RAC and IMR4WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester, depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester, depending on the setting of the GT_IWB_EN bit.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR4 Mask (IMR4_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR4BASE[28:0] value. A match indicates that the incoming address falls within the IMR4 region.

5.9.29 B-Unit IMR4 Control Policy (B_CR_BIMR4CP_0_0_0_MCHBAR)—Offset 68F8h

This register controls the access policy to the Read Access Policy BIMR4RAC, the Write Access Policy BIMR4WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**B-Unit IMR4 Control Policy (IMR4_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR4RAC, BIMR4WAC and BIMR4CP registers, based on the value from each agent's 6bit SAI field.

5.9.30 IMR4 Read Access Policy (B_CR_BIMR4RAC_0_0_0_MCHBAR)—Offset 6900h

This register, along with IMR4BASE, IMR4MASK and IMR4WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR4. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR4 Read Access Policy 63 (IMR4_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR4 Read Access Policy 62 (IMR4_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR4 Read Access Policy 61 (IMR4_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR4 Read Access Policy 60 (IMR4_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR4 Read Access Policy 59 (IMR4_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR4 Read Access Policy 58 (IMR4_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR4 Read Access Policy 57 (IMR4_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR4 Read Access Policy 56 (IMR4_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR4 Read Access Policy 55 (IMR4_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR4 Read Access Policy 54 (IMR4_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR4 Read Access Policy 53 (IMR4_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR4 Read Access Policy 52 (IMR4_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR4 Read Access Policy 51 (IMR4_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR4 Read Access Policy 50 (IMR4_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR4 Read Access Policy 49 (IMR4_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**IMR4 Read Access Policy 48 (IMR4_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR4 Read Access Policy 47 (IMR4_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR4 Read Access Policy 46 (IMR4_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR4 Read Access Policy 45 (IMR4_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR4 Read Access Policy 44 (IMR4_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR4 Read Access Policy 43 (IMR4_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR4 Read Access Policy 42 (IMR4_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR4 Read Access Policy 41 (IMR4_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR4 Read Access Policy 40 (IMR4_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR4 Read Access Policy 39 (IMR4_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR4 Read Access Policy 38 (IMR4_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR4 Read Access Policy 37 (IMR4_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR4 Read Access Policy 36 (IMR4_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR4 Read Access Policy 35 (IMR4_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR4 Read Access Policy 34 (IMR4_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
33	0h RW	**IMR4 Read Access Policy 33 (IMR4_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR4 Read Access Policy 32 (IMR4_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR4 Read Access Policy 31 (IMR4_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR4 Read Access Policy 30 (IMR4_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR4 Read Access Policy 29 (IMR4_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR4 Read Access Policy 28 (IMR4_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR4 Read Access Policy 27 (IMR4_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR4 Read Access Policy 26 (IMR4_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR4 Read Access Policy 25 (IMR4_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR4 Read Access Policy 24 (IMR4_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR4 Read Access Policy 23 (IMR4_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR4 Read Access Policy 22 (IMR4_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR4 Read Access Policy 21 (IMR4_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR4 Read Access Policy 20 (IMR4_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR4 Read Access Policy 19 (IMR4_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**IMR4 Read Access Policy 18 (IMR4_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR4 Read Access Policy 17 (IMR4_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR4 Read Access Policy 16 (IMR4_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR4 Read Access Policy 15 (IMR4_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR4 Read Access Policy 14 (IMR4_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR4 Read Access Policy 13 (IMR4_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR4 Read Access Policy 12 (IMR4_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR4 Read Access Policy 11 (IMR4_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR4 Read Access Policy 10 (IMR4_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR4 Read Access Policy 9 (IMR4_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR4 Read Access Policy 8 (IMR4_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR4 Read Access Policy 7 (IMR4_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR4 Read Access Policy 6 (IMR4_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR4 Read Access Policy 5 (IMR4_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR4 Read Access Policy 4 (IMR4_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**IMR4 Read Access Policy 3 (IMR4_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR4 Read Access Policy 2 (IMR4_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR4 Read Access Policy 1 (IMR4_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR4 Read Access Policy 0 (IMR4_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR4 region, based on each agent's 6bit encoded SAI value.

5.9.31 IMR4 Write Access Policy (B_CR_BIMR4WAC_0_0_0_MCHBAR)—Offset 6908h

This register, along with IMR4BASE, IMR4MASK and IMR4RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with a SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR4. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR4_WRITE_POL_63 (IMR4_WRITE_POL_63):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR4_WRITE_POL_62 (IMR4_WRITE_POL_62):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR4_WRITE_POL_61 (IMR4_WRITE_POL_61):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR4_WRITE_POL_60 (IMR4_WRITE_POL_60):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
59	0h RO	**IMR4_WRITE_POL_59 (IMR4_WRITE_POL_59):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR4_WRITE_POL_58 (IMR4_WRITE_POL_58):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR4_WRITE_POL_57 (IMR4_WRITE_POL_57):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR4_WRITE_POL_56 (IMR4_WRITE_POL_56):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR4_WRITE_POL_55 (IMR4_WRITE_POL_55):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR4_WRITE_POL_54 (IMR4_WRITE_POL_54):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR4_WRITE_POL_53 (IMR4_WRITE_POL_53):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR4_WRITE_POL_52 (IMR4_WRITE_POL_52):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR4_WRITE_POL_51 (IMR4_WRITE_POL_51):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR4_WRITE_POL_50 (IMR4_WRITE_POL_50):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR4_WRITE_POL_49 (IMR4_WRITE_POL_49):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**IMR4_WRITE_POL_48 (IMR4_WRITE_POL_48):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR4_WRITE_POL_47 (IMR4_WRITE_POL_47):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR4_WRITE_POL_46 (IMR4_WRITE_POL_46):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR4_WRITE_POL_45 (IMR4_WRITE_POL_45):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR4_WRITE_POL_44 (IMR4_WRITE_POL_44):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR4_WRITE_POL_43 (IMR4_WRITE_POL_43):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR4_WRITE_POL_42 (IMR4_WRITE_POL_42):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR4_WRITE_POL_41 (IMR4_WRITE_POL_41):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR4_WRITE_POL_40 (IMR4_WRITE_POL_40):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR4_WRITE_POL_39 (IMR4_WRITE_POL_39):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR4_WRITE_POL_38 (IMR4_WRITE_POL_38):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
37	0h RO	**IMR4_WRITE_POL_37 (IMR4_WRITE_POL_37):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR4_WRITE_POL_36 (IMR4_WRITE_POL_36):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR4_WRITE_POL_35 (IMR4_WRITE_POL_35):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR4_WRITE_POL_34 (IMR4_WRITE_POL_34):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR4_WRITE_POL_33 (IMR4_WRITE_POL_33):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR4_WRITE_POL_32 (IMR4_WRITE_POL_32):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR4_WRITE_POL_31 (IMR4_WRITE_POL_31):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR4_WRITE_POL_30 (IMR4_WRITE_POL_30):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR4_WRITE_POL_29 (IMR4_WRITE_POL_29):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR4_WRITE_POL_28 (IMR4_WRITE_POL_28):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR4_WRITE_POL_27 (IMR4_WRITE_POL_27):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
26	0h RW	**IMR4_WRITE_POL_26 (IMR4_WRITE_POL_26):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR4_WRITE_POL_25 (IMR4_WRITE_POL_25):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR4_WRITE_POL_24 (IMR4_WRITE_POL_24):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR4_WRITE_POL_23 (IMR4_WRITE_POL_23):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR4_WRITE_POL_22 (IMR4_WRITE_POL_22):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR4_WRITE_POL_21 (IMR4_WRITE_POL_21):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR4_WRITE_POL_20 (IMR4_WRITE_POL_20):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR4_WRITE_POL_19 (IMR4_WRITE_POL_19):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR4_WRITE_POL_18 (IMR4_WRITE_POL_18):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR4_WRITE_POL_17 (IMR4_WRITE_POL_17):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR4_WRITE_POL_16 (IMR4_WRITE_POL_16):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**IMR4_WRITE_POL_15 (IMR4_WRITE_POL_15):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR4_WRITE_POL_14 (IMR4_WRITE_POL_14):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR4_WRITE_POL_13 (IMR4_WRITE_POL_13):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR4_WRITE_POL_12 (IMR4_WRITE_POL_12):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR4_WRITE_POL_11 (IMR4_WRITE_POL_11):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR4_WRITE_POL_10 (IMR4_WRITE_POL_10):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR4_WRITE_POL_9 (IMR4_WRITE_POL_9):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR4_WRITE_POL_8 (IMR4_WRITE_POL_8):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR4_WRITE_POL_7 (IMR4_WRITE_POL_7):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR4_WRITE_POL_6 (IMR4_WRITE_POL_6):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR4_WRITE_POL_5 (IMR4_WRITE_POL_5):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**IMR4_WRITE_POL_4 (IMR4_WRITE_POL_4):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR4_WRITE_POL_3 (IMR4_WRITE_POL_3):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR4_WRITE_POL_2 (IMR4_WRITE_POL_2):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR4_WRITE_POL_1 (IMR4_WRITE_POL_1):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR4_WRITE_POL_0 (IMR4_WRITE_POL_0):** B-Unit IMR4 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR4 region, based on each agent's 6bit encoded SAI value.

5.9.32 IMR5 Base (B_CR_BIMR5BASE_0_0_0_MCHBAR)—Offset 6910h

This register, along with IMR5MASK, IMR5RAC and IMR5WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR5RAC and IMR5WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28:0	0h RW	**Base 0 IMR5 Base (IMR5_BASE):** Specifies bits 38:10 of the start address of IMR5 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR5MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR5 defined region.

5.9.33 IMR5 Mask (B_CR_BIMR5MASK_0_0_0_MCHBAR)—Offset 6914h

This register, along with IMR5BASE, IMR5RAC and IMR5WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR5RAC and IMR5WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester, depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester, depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR5 Mask (IMR5_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR5BASE[28:0] value. A match indicates that the incoming address falls within the IMR5 region.

5.9.34 IMR5 Control Policy (B_CR_BIMR5CP_0_0_0_MCHBAR)—Offset 6918h

This register controls the access policy to the Read Access Policy BIMR5RAC, the Write Access Policy BIMR5WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR5 Control Policy (IMR5_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR5RAC, BIMR5WAC and BIMR5CP registers, based on the value from each agent's 6bit SAI field.

5.9.35 IMR5 Read Access Policy (B_CR_BIMR5RAC_0_0_0_MCHBAR)—Offset 6920h

This register, along with IMR5BASE, IMR5MASK and IMR5WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR5. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR5 Read Access Policy 63 (IMR5_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR5 Read Access Policy 62 (IMR5_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR5 Read Access Policy 61 (IMR5_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
60	0h RO	**IMR5 Read Access Policy 60 (IMR5_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR5 Read Access Policy 59 (IMR5_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR5 Read Access Policy 58 (IMR5_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR5 Read Access Policy 57 (IMR5_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR5 Read Access Policy 56 (IMR5_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR5 Read Access Policy 55 (IMR5_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR5 Read Access Policy 54 (IMR5_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR5 Read Access Policy 53 (IMR5_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR5 Read Access Policy 52 (IMR5_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR5 Read Access Policy 51 (IMR5_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR5 Read Access Policy 50 (IMR5_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR5 Read Access Policy 49 (IMR5_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR5 Read Access Policy 48 (IMR5_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR5 Read Access Policy 47 (IMR5_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR5 Read Access Policy 46 (IMR5_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
45	0h RO	**IMR5 Read Access Policy 45 (IMR5_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR5 Read Access Policy 44 (IMR5_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR5 Read Access Policy 43 (IMR5_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR5 Read Access Policy 42 (IMR5_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR5 Read Access Policy 41 (IMR5_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR5 Read Access Policy 40 (IMR5_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR5 Read Access Policy 39 (IMR5_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR5 Read Access Policy 38 (IMR5_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR5 Read Access Policy 37 (IMR5_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR5 Read Access Policy 36 (IMR5_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR5 Read Access Policy 35 (IMR5_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR5 Read Access Policy 34 (IMR5_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR5 Read Access Policy 33 (IMR5_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR5 Read Access Policy 32 (IMR5_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR5 Read Access Policy 31 (IMR5_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW	**IMR5 Read Access Policy 30 (IMR5_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR5 Read Access Policy 29 (IMR5_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR5 Read Access Policy 28 (IMR5_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR5 Read Access Policy 27 (IMR5_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR5 Read Access Policy 26 (IMR5_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR5 Read Access Policy 25 (IMR5_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR5 Read Access Policy 24 (IMR5_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR5 Read Access Policy 23 (IMR5_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR5 Read Access Policy 22 (IMR5_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR5 Read Access Policy 21 (IMR5_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR5 Read Access Policy 20 (IMR5_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR5 Read Access Policy 19 (IMR5_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR5 Read Access Policy 18 (IMR5_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR5 Read Access Policy 17 (IMR5_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR5 Read Access Policy 16 (IMR5_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**IMR5 Read Access Policy 15 (IMR5_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR5 Read Access Policy 14 (IMR5_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR5 Read Access Policy 13 (IMR5_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR5 Read Access Policy 12 (IMR5_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR5 Read Access Policy 11 (IMR5_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR5 Read Access Policy 10 (IMR5_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR5 Read Access Policy 9 (IMR5_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR5 Read Access Policy 8 (IMR5_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR5 Read Access Policy 7 (IMR5_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR5 Read Access Policy 6 (IMR5_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR5 Read Access Policy 5 (IMR5_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR5 Read Access Policy 4 (IMR5_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR5 Read Access Policy 3 (IMR5_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR5 Read Access Policy 2 (IMR5_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR5 Read Access Policy 1 (IMR5_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**IMR5 Read Access Policy 0 (IMR5_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR5 region, based on each agent's 6bit encoded SAI value.

5.9.36 IMR5 Write Access Policy (B_CR_BIMR5WAC_0_0_0_MCHBAR)—Offset 6928h

This register, along with IMR5BASE, IMR5MASK and IMR5RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR5. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR5 Write Access Policy 63 (IMR5_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR5 Write Access Policy 62 (IMR5_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR5 Write Access Policy 61 (IMR5_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR5 Write Access Policy 60 (IMR5_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR5 Write Access Policy 59 (IMR5_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR5 Write Access Policy 58 (IMR5_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR5 Write Access Policy 57 (IMR5_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR5 Write Access Policy 56 (IMR5_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
55	0h RW	**IMR5 Write Access Policy 55 (IMR5_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR5 Write Access Policy 54 (IMR5_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR5 Write Access Policy 53 (IMR5_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR5 Write Access Policy 52 (IMR5_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR5 Write Access Policy 51 (IMR5_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR5 Write Access Policy 50 (IMR5_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR5 Write Access Policy 49 (IMR5_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR5 Write Access Policy 48 (IMR5_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR5 Write Access Policy 47 (IMR5_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR5 Write Access Policy 46 (IMR5_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR5 Write Access Policy 45 (IMR5_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR5 Write Access Policy 44 (IMR5_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR5 Write Access Policy 43 (IMR5_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR5 Write Access Policy 42 (IMR5_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR5 Write Access Policy 41 (IMR5_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
40	0h RW	**IMR5 Write Access Policy 40 (IMR5_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR5 Write Access Policy 39 (IMR5_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR5 Write Access Policy 38 (IMR5_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR5 Write Access Policy 37 (IMR5_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR5 Write Access Policy 36 (IMR5_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR5 Write Access Policy 35 (IMR5_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR5 Write Access Policy 34 (IMR5_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR5 Write Access Policy 33 (IMR5_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR5 Write Access Policy 32 (IMR5_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR5 Write Access Policy 31 (IMR5_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR5 Write Access Policy 30 (IMR5_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR5 Write Access Policy 29 (IMR5_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR5 Write Access Policy 28 (IMR5_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR5 Write Access Policy 27 (IMR5_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR5 Write Access Policy 26 (IMR5_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW	**IMR5 Write Access Policy 25 (IMR5_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR5 Write Access Policy 24 (IMR5_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR5 Write Access Policy 23 (IMR5_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR5 Write Access Policy 22 (IMR5_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR5 Write Access Policy 21 (IMR5_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR5 Write Access Policy 20 (IMR5_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR5 Write Access Policy 19 (IMR5_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR5 Write Access Policy 18 (IMR5_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR5 Write Access Policy 17 (IMR5_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR5 Write Access Policy 16 (IMR5_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR5 Write Access Policy 15 (IMR5_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR5 Write Access Policy 14 (IMR5_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR5 Write Access Policy 13 (IMR5_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR5 Write Access Policy 12 (IMR5_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR5 Write Access Policy 11 (IMR5_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO	**IMR5 Write Access Policy 10 (IMR5_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR5 Write Access Policy 9 (IMR5_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR5 Write Access Policy 8 (IMR5_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR5 Write Access Policy 7 (IMR5_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR5 Write Access Policy 6 (IMR5_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR5 Write Access Policy 5 (IMR5_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR5 Write Access Policy 4 (IMR5_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR5 Write Access Policy 3 (IMR5_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR5 Write Access Policy 2 (IMR5_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR5 Write Access Policy 1 (IMR5_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR5 Write Access Policy 0 (IMR5_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR5 region, based on each agent's 6bit encoded SAI value.

5.9.37 IMR6 Base (B_CR_BIMR6BASE_0_0_0_MCHBAR)—Offset 6930h

This register, along with IMR6MASK, IMR6RAC and IMR6WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR6RAC and IMR6WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR6 Base (IMR6_BASE):** Specifies bits 38:10 of the start address of IMR6 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR6MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR6 defined region.

5.9.38 IMR6 Mask (B_CR_BIMR6MASK_0_0_0_MCHBAR)—Offset 6934h

This register, along with IMR6BASE, IMR6RAC and IMR6WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR6RAC and IMR6WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit WB Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester, depending on the setting of the IA_IWB_EN bit.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW	**Asset Classification AC[1]: IA Implicit WB Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester, depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR6 Mask (IMR6_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR6BASE[28:0] value. A match indicates that the incoming address falls within the IMR6 region.

5.9.39 IMR6 Control Policy (B_CR_BIMR6CP_0_0_0_MCHBAR)—Offset 6938h

This register controls the access policy to the Read Access Policy BIMR6RAC, the Write Access Policy BIMR6WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR6 Control Policy (IMR6_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR6RAC, BIMR6WAC, BIMR6CP registers, based on the value from each agent's 6bit SAI field.

5.9.40 IMR6 Read Access Policy (B_CR_BIMR6RAC_0_0_0_MCHBAR)—Offset 6940h

This register, along with IMR6BASE, IMR6MASK and IMR6WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR6. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR6 Read Access Policy 63 (IMR6_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR6 Read Access Policy 62 (IMR6_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR6 Read Access Policy 61 (IMR6_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR6 Read Access Policy 60 (IMR6_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR6 Read Access Policy 59 (IMR6_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR6 Read Access Policy 58 (IMR6_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR6 Read Access Policy 57 (IMR6_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR6 Read Access Policy 56 (IMR6_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR6 Read Access Policy 55 (IMR6_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR6 Read Access Policy 54 (IMR6_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR6 Read Access Policy 53 (IMR6_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR6 Read Access Policy 52 (IMR6_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR6 Read Access Policy 51 (IMR6_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR6 Read Access Policy 50 (IMR6_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
49	0h RW	**IMR6 Read Access Policy 49 (IMR6_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR6 Read Access Policy 48 (IMR6_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR6 Read Access Policy 47 (IMR6_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR6 Read Access Policy 46 (IMR6_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR6 Read Access Policy 45 (IMR6_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR6 Read Access Policy 44 (IMR6_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR6 Read Access Policy 43 (IMR6_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR6 Read Access Policy 42 (IMR6_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR6 Read Access Policy 41 (IMR6_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR6 Read Access Policy 40 (IMR6_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR6 Read Access Policy 39 (IMR6_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR6 Read Access Policy 38 (IMR6_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR6 Read Access Policy 37 (IMR6_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR6 Read Access Policy 36 (IMR6_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR6 Read Access Policy 35 (IMR6_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
34	0h RW	**IMR6 Read Access Policy 34 (IMR6_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR6 Read Access Policy 33 (IMR6_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR6 Read Access Policy 32 (IMR6_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR6 Read Access Policy 31 (IMR6_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR6 Read Access Policy 30 (IMR6_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR6 Read Access Policy 29 (IMR6_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR6 Read Access Policy 28 (IMR6_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR6 Read Access Policy 27 (IMR6_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR6 Read Access Policy 26 (IMR6_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR6 Read Access Policy 25 (IMR6_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR6 Read Access Policy 24 (IMR6_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR6 Read Access Policy 23 (IMR6_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR6 Read Access Policy 22 (IMR6_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR6 Read Access Policy 21 (IMR6_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR6 Read Access Policy 20 (IMR6_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**IMR6 Read Access Policy 19 (IMR6_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR6 Read Access Policy 18 (IMR6_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR6 Read Access Policy 17 (IMR6_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR6 Read Access Policy 16 (IMR6_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR6 Read Access Policy 15 (IMR6_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR6 Read Access Policy 14 (IMR6_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR6 Read Access Policy 13 (IMR6_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR6 Read Access Policy 12 (IMR6_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR6 Read Access Policy 11 (IMR6_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR6 Read Access Policy 10 (IMR6_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR6 Read Access Policy 9 (IMR6_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR6 Read Access Policy 8 (IMR6_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR6 Read Access Policy 7 (IMR6_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR6 Read Access Policy 6 (IMR6_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR6 Read Access Policy 5 (IMR6_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**IMR6 Read Access Policy 4 (IMR6_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR6 Read Access Policy 3 (IMR6_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR6 Read Access Policy 2 (IMR6_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR6 Read Access Policy 1 (IMR6_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR6 Read Access Policy 0 (IMR6_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR6 region, based on each agent's 6bit encoded SAI value.

5.9.41 IMR6 Write Access Policy (B_CR_BIMR6WAC_0_0_0_MCHBAR)—Offset 6948h

This register, along with IMR6BASE, IMR6MASK and IMR6RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with a SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR6. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR6 Write Access Policy 63 (IMR6_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR6 Write Access Policy 62 (IMR6_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR6 Write Access Policy 61 (IMR6_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR6 Write Access Policy 60 (IMR6_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
59	0h RO	**IMR6 Write Access Policy 59 (IMR6_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR6 Write Access Policy 58 (IMR6_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR6 Write Access Policy 57 (IMR6_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR6 Write Access Policy 56 (IMR6_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR6 Write Access Policy 55 (IMR6_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR6 Write Access Policy 54 (IMR6_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR6 Write Access Policy 53 (IMR6_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR6 Write Access Policy 52 (IMR6_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR6 Write Access Policy 51 (IMR6_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR6 Write Access Policy 50 (IMR6_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR6 Write Access Policy 49 (IMR6_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR6 Write Access Policy 48 (IMR6_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR6 Write Access Policy 47 (IMR6_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR6 Write Access Policy 46 (IMR6_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR6 Write Access Policy 45 (IMR6_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
44	0h RW	**IMR6 Write Access Policy 44 (IMR6_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR6 Write Access Policy 43 (IMR6_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR6 Write Access Policy 42 (IMR6_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR6 Write Access Policy 41 (IMR6_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR6 Write Access Policy 40 (IMR6_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR6 Write Access Policy 39 (IMR6_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR6 Write Access Policy 38 (IMR6_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR6 Write Access Policy 37 (IMR6_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR6 Write Access Policy 36 (IMR6_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR6 Write Access Policy 35 (IMR6_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR6 Write Access Policy 34 (IMR6_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR6 Write Access Policy 33 (IMR6_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR6 Write Access Policy 32 (IMR6_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR6 Write Access Policy 31 (IMR6_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR6 Write Access Policy 30 (IMR6_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RW	**IMR6 Write Access Policy 29 (IMR6_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR6 Write Access Policy 28 (IMR6_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR6 Write Access Policy 27 (IMR6_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR6 Write Access Policy 26 (IMR6_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR6 Write Access Policy 25 (IMR6_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR6 Write Access Policy 24 (IMR6_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR6 Write Access Policy 23 (IMR6_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR6 Write Access Policy 22 (IMR6_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR6 Write Access Policy 21 (IMR6_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR6 Write Access Policy 20 (IMR6_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR6 Write Access Policy 19 (IMR6_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR6 Write Access Policy 18 (IMR6_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR6 Write Access Policy 17 (IMR6_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR6 Write Access Policy 16 (IMR6_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR6 Write Access Policy 15 (IMR6_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**IMR6 Write Access Policy 14 (IMR6_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR6 Write Access Policy 13 (IMR6_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR6 Write Access Policy 12 (IMR6_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR6 Write Access Policy 11 (IMR6_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR6 Write Access Policy 10 (IMR6_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR6 Write Access Policy 9 (IMR6_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR6 Write Access Policy 8 (IMR6_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR6 Write Access Policy 7 (IMR6_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR6 Write Access Policy 6 (IMR6_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR6 Write Access Policy 5 (IMR6_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR6 Write Access Policy 4 (IMR6_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR6 Write Access Policy 3 (IMR6_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR6 Write Access Policy 2 (IMR6_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR6 Write Access Policy 1 (IMR6_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR6 Write Access Policy 0 (IMR6_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR6 region, based on each agent's 6bit encoded SAI value.

5.9.42 IMR7 Base (B_CR_BIMR7BASE_0_0_0_MCHBAR)—Offset 6950h

This register, along with IMR7MASK, IMR7RAC and IMR7WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR7RAC and IMR7WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR7 Base (IMR7_BASE):** Specifies bits 38:10 of the start address of IMR7 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR7MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR7 defined region.

5.9.43 IMR7 Mask (B_CR_BIMR7MASK_0_0_0_MCHBAR)—Offset 6954h

This register, along with IMR7BASE, IMR7RAC and IMR7WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR7RAC and IMR7WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit WB Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester, depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit WB Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester, depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR7 Mask (IMR7_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR7BASE[28:0] value. A match indicates that the incoming address falls within the IMR7 region.

5.9.44 IMR7 Control Policy (B_CR_BIMR7CP_0_0_0_MCHBAR)—Offset 6958h

This register controls the access policy to the Read Access Policy BIMR7RAC, the Write Access Policy BIMR7WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR7 Control Policy (IMR7_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR7RAC, BIMR7WAC and BIMR7CP registers, based on the value from each agent's 6bit SAI field.

5.9.45 IMR7 Read Access Policy (B_CR_BIMR7RAC_0_0_0_MCHBAR)—Offset 6960h

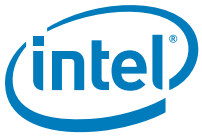
This register, along with IMR7BASE, IMR7MASK and IMR7WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR7. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR7 Read Access Policy 63 (IMR7_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR7 Read Access Policy 62 (IMR7_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR7 Read Access Policy 61 (IMR7_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR7 Read Access Policy 60 (IMR7_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR7 Read Access Policy 59 (IMR7_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR7 Read Access Policy 58 (IMR7_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR7 Read Access Policy 57 (IMR7_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR7 Read Access Policy 56 (IMR7_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR7 Read Access Policy 55 (IMR7_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR7 Read Access Policy 54 (IMR7_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.



Bit Range	Default & Access	Field Name (ID): Description
53	0h RO	**IMR7 Read Access Policy 53 (IMR7_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR7 Read Access Policy 52 (IMR7_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR7 Read Access Policy 51 (IMR7_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR7 Read Access Policy 50 (IMR7_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR7 Read Access Policy 49 (IMR7_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR7 Read Access Policy 48 (IMR7_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR7 Read Access Policy 47 (IMR7_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR7 Read Access Policy 46 (IMR7_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR7 Read Access Policy 45 (IMR7_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR7 Read Access Policy 44 (IMR7_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR7 Read Access Policy 43 (IMR7_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR7 Read Access Policy 42 (IMR7_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR7 Read Access Policy 41 (IMR7_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR7 Read Access Policy 40 (IMR7_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR7 Read Access Policy 39 (IMR7_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
38	0h RW	**IMR7 Read Access Policy 38 (IMR7_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR7 Read Access Policy 37 (IMR7_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR7 Read Access Policy 36 (IMR7_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR7 Read Access Policy 35 (IMR7_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR7 Read Access Policy 34 (IMR7_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR7 Read Access Policy 33 (IMR7_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR7 Read Access Policy 32 (IMR7_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR7 Read Access Policy 31 (IMR7_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR7 Read Access Policy 30 (IMR7_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR7 Read Access Policy 29 (IMR7_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR7 Read Access Policy 28 (IMR7_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR7 Read Access Policy 27 (IMR7_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR7 Read Access Policy 26 (IMR7_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR7 Read Access Policy 25 (IMR7_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR7 Read Access Policy 24 (IMR7_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**IMR7 Read Access Policy 23 (IMR7_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR7 Read Access Policy 22 (IMR7_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR7 Read Access Policy 21 (IMR7_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR7 Read Access Policy 20 (IMR7_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR7 Read Access Policy 19 (IMR7_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR7 Read Access Policy 18 (IMR7_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR7 Read Access Policy 17 (IMR7_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR7 Read Access Policy 16 (IMR7_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR7 Read Access Policy 15 (IMR7_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR7 Read Access Policy 14 (IMR7_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR7 Read Access Policy 13 (IMR7_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR7 Read Access Policy 12 (IMR7_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR7 Read Access Policy 11 (IMR7_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR7 Read Access Policy 10 (IMR7_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR7 Read Access Policy 9 (IMR7_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**IMR7 Read Access Policy 8 (IMR7_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR7 Read Access Policy 7 (IMR7_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR7 Read Access Policy 6 (IMR7_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR7 Read Access Policy 5 (IMR7_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR7 Read Access Policy 4 (IMR7_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR7 Read Access Policy 3 (IMR7_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR7 Read Access Policy 2 (IMR7_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR7 Read Access Policy 1 (IMR7_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR7 Read Access Policy 0 (IMR7_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR7 region, based on each agent's 6bit encoded SAI value.

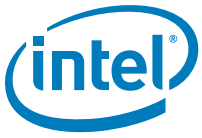
5.9.46 IMR7 Write Access Policy (B_CR_BIMR7WAC_0_0_0_MCHBAR)—Offset 6968h

This register, along with IMR7BASE, IMR7MASK and IMR7RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR7. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR7 Write Access Policy 63 (IMR7_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR7 Write Access Policy 62 (IMR7_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR7 Write Access Policy 61 (IMR7_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR7 Write Access Policy 60 (IMR7_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR7 Write Access Policy 59 (IMR7_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR7 Write Access Policy 58 (IMR7_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR7 Write Access Policy 57 (IMR7_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR7 Write Access Policy 56 (IMR7_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR7 Write Access Policy 55 (IMR7_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR7 Write Access Policy 54 (IMR7_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR7 Write Access Policy 53 (IMR7_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR7 Write Access Policy 52 (IMR7_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR7 Write Access Policy 51 (IMR7_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR7 Write Access Policy 50 (IMR7_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR7 Write Access Policy 49 (IMR7_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**IMR7 Write Access Policy 48 (IMR7_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR7 Write Access Policy 47 (IMR7_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR7 Write Access Policy 46 (IMR7_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR7 Write Access Policy 45 (IMR7_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR7 Write Access Policy 44 (IMR7_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR7 Write Access Policy 43 (IMR7_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR7 Write Access Policy 42 (IMR7_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR7 Write Access Policy 41 (IMR7_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR7 Write Access Policy 40 (IMR7_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR7 Write Access Policy 39 (IMR7_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR7 Write Access Policy 38 (IMR7_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR7 Write Access Policy 37 (IMR7_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR7 Write Access Policy 36 (IMR7_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR7 Write Access Policy 35 (IMR7_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR7 Write Access Policy 34 (IMR7_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
33	0h RW	**IMR7 Write Access Policy 33 (IMR7_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR7 Write Access Policy 32 (IMR7_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR7 Write Access Policy 31 (IMR7_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR7 Write Access Policy 30 (IMR7_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR7 Write Access Policy 29 (IMR7_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR7 Write Access Policy 28 (IMR7_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR7 Write Access Policy 27 (IMR7_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR7 Write Access Policy 26 (IMR7_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR7 Write Access Policy 25 (IMR7_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR7 Write Access Policy 24 (IMR7_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR7 Write Access Policy 23 (IMR7_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR7 Write Access Policy 22 (IMR7_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR7 Write Access Policy 21 (IMR7_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR7 Write Access Policy 20 (IMR7_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR7 Write Access Policy 19 (IMR7_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**IMR7 Write Access Policy 18 (IMR7_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR7 Write Access Policy 17 (IMR7_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR7 Write Access Policy 16 (IMR7_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR7 Write Access Policy 15 (IMR7_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR7 Write Access Policy 14 (IMR7_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR7 Write Access Policy 13 (IMR7_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR7 Write Access Policy 12 (IMR7_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR7 Write Access Policy 11 (IMR7_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR7 Write Access Policy 10 (IMR7_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR7 Write Access Policy 9 (IMR7_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR7 Write Access Policy 8 (IMR7_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR7 Write Access Policy 7 (IMR7_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR7 Write Access Policy 6 (IMR7_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR7 Write Access Policy 5 (IMR7_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR7 Write Access Policy 4 (IMR7_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**IMR7 Write Access Policy 3 (IMR7_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR7 Write Access Policy 2 (IMR7_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR7 Write Access Policy 1 (IMR7_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR7 Write Access Policy 0 (IMR7_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR7 region, based on each agent's 6bit encoded SAI value.

5.9.47 IMR8 Base (B_CR_BIMR8BASE_0_0_0_MCHBAR)—Offset 6970h

This register, along with IMR8MASK, IMR8RAC and IMR8WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR8RAC and IMR8WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR8 Base (IMR8_BASE):** Specifies bits 38:10 of the start address of IMR8 region. IMR region size must be a strict power of two at least 1KB and naturally aligned to the size. These bits are compared with the result of the IMR8MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR8 defined region.

5.9.48 IMR8 Mask (B_CR_BIMR8MASK_0_0_0_MCHBAR)—Offset 6974h

This register, along with IMR8BASE, IMR8RAC and IMR8WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR8RAC and IMR8WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR8 Mask (IMR8_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR8BASE[28:0] value. A match indicates that the incoming address falls within the IMR8 region.

5.9.49 IMR8 Control Policy (B_CR_BIMR8CP_0_0_0_MCHBAR)—Offset 6978h

This register controls the access policy to the Read Access Policy BIMR8RAC, the Write Access Policy BIMR8WAC, and, self-referentially to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR8 Control Policy (IMR8_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR8RAC, BIMR8WAC and BIMR8CP registers, based on the value from each agent's 6bit SAI field.

5.9.50 IMR8 Read Access Policy (B_CR_BIMR8RAC_0_0_0_MCHBAR)—Offset 6980h

This register, along with IMR8BASE, IMR8MASK and IMR8WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR8. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

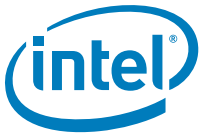
Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR8 Read Access Policy 63 (IMR8_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR8 Read Access Policy 62 (IMR8_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR8 Read Access Policy 61 (IMR8_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR8 Read Access Policy 60 (IMR8_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR8 Read Access Policy 59 (IMR8_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR8 Read Access Policy 58 (IMR8_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
57	0h RO	**IMR8 Read Access Policy 57 (IMR8_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR8 Read Access Policy 56 (IMR8_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR8 Read Access Policy 55 (IMR8_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR8 Read Access Policy 54 (IMR8_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR8 Read Access Policy 53 (IMR8_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR8 Read Access Policy 52 (IMR8_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR8 Read Access Policy 51 (IMR8_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR8 Read Access Policy 50 (IMR8_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR8 Read Access Policy 49 (IMR8_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR8 Read Access Policy 48 (IMR8_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR8 Read Access Policy 47 (IMR8_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR8 Read Access Policy 46 (IMR8_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR8 Read Access Policy 45 (IMR8_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR8 Read Access Policy 44 (IMR8_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR8 Read Access Policy 43 (IMR8_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.



Bit Range	Default & Access	Field Name (ID): Description
42	0h RW	**IMR8 Read Access Policy 42 (IMR8_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR8 Read Access Policy 41 (IMR8_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR8 Read Access Policy 40 (IMR8_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR8 Read Access Policy 39 (IMR8_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR8 Read Access Policy 38 (IMR8_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR8 Read Access Policy 37 (IMR8_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR8 Read Access Policy 36 (IMR8_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR8 Read Access Policy 35 (IMR8_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR8 Read Access Policy 34 (IMR8_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR8 Read Access Policy 33 (IMR8_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR8 Read Access Policy 32 (IMR8_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR8 Read Access Policy 31 (IMR8_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR8 Read Access Policy 30 (IMR8_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR8 Read Access Policy 29 (IMR8_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR8 Read Access Policy 28 (IMR8_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW	**IMR8 Read Access Policy 27 (IMR8_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR8 Read Access Policy 26 (IMR8_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR8 Read Access Policy 25 (IMR8_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR8 Read Access Policy 24 (IMR8_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR8 Read Access Policy 23 (IMR8_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR8 Read Access Policy 22 (IMR8_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR8 Read Access Policy 21 (IMR8_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR8 Read Access Policy 20 (IMR8_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR8 Read Access Policy 19 (IMR8_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR8 Read Access Policy 18 (IMR8_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR8 Read Access Policy 17 (IMR8_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR8 Read Access Policy 16 (IMR8_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR8 Read Access Policy 15 (IMR8_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR8 Read Access Policy 14 (IMR8_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR8 Read Access Policy 13 (IMR8_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**IMR8 Read Access Policy 12 (IMR8_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR8 Read Access Policy 11 (IMR8_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR8 Read Access Policy 10 (IMR8_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR8 Read Access Policy 9 (IMR8_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR8 Read Access Policy 8 (IMR8_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR8 Read Access Policy 7 (IMR8_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR8 Read Access Policy 6 (IMR8_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR8 Read Access Policy 5 (IMR8_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR8 Read Access Policy 4 (IMR8_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR8 Read Access Policy 3 (IMR8_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR8 Read Access Policy 2 (IMR8_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR8 Read Access Policy 1 (IMR8_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR8 Read Access Policy 0 (IMR8_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR8 region, based on each agent's 6bit encoded SAI value.

5.9.51 IMR8 Write Access Policy (B_CR_BIMR8WAC_0_0_0_MCHBAR)—Offset 6988h

This register, along with IMR8BASE, IMR8MASK and IMR8RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR8. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR8 Write Access Policy 63 (IMR8_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR8 Write Access Policy 62 (IMR8_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR8 Write Access Policy 61 (IMR8_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR8 Write Access Policy 60 (IMR8_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR8 Write Access Policy 59 (IMR8_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR8 Write Access Policy 58 (IMR8_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR8 Write Access Policy 57 (IMR8_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR8 Write Access Policy 56 (IMR8_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR8 Write Access Policy 55 (IMR8_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR8 Write Access Policy 54 (IMR8_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
53	0h RO	**IMR8 Write Access Policy 53 (IMR8_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR8 Write Access Policy 52 (IMR8_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR8 Write Access Policy 51 (IMR8_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR8 Write Access Policy 50 (IMR8_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR8 Write Access Policy 49 (IMR8_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR8 Write Access Policy 48 (IMR8_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR8 Write Access Policy 47 (IMR8_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR8 Write Access Policy 46 (IMR8_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR8 Write Access Policy 45 (IMR8_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR8 Write Access Policy 44 (IMR8_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR8 Write Access Policy 43 (IMR8_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR8 Write Access Policy 42 (IMR8_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR8 Write Access Policy 41 (IMR8_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR8 Write Access Policy 40 (IMR8_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR8 Write Access Policy 39 (IMR8_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
38	0h RW	**IMR8 Write Access Policy 38 (IMR8_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR8 Write Access Policy 37 (IMR8_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR8 Write Access Policy 36 (IMR8_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR8 Write Access Policy 35 (IMR8_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR8 Write Access Policy 34 (IMR8_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR8 Write Access Policy 33 (IMR8_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR8 Write Access Policy 32 (IMR8_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR8 Write Access Policy 31 (IMR8_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR8 Write Access Policy 30 (IMR8_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR8 Write Access Policy 29 (IMR8_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR8 Write Access Policy 28 (IMR8_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR8 Write Access Policy 27 (IMR8_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR8 Write Access Policy 26 (IMR8_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR8 Write Access Policy 25 (IMR8_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR8 Write Access Policy 24 (IMR8_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**IMR8 Write Access Policy 23 (IMR8_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR8 Write Access Policy 22 (IMR8_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR8 Write Access Policy 21 (IMR8_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR8 Write Access Policy 20 (IMR8_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR8 Write Access Policy 19 (IMR8_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR8 Write Access Policy 18 (IMR8_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR8 Write Access Policy 17 (IMR8_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR8 Write Access Policy 16 (IMR8_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR8 Write Access Policy 15 (IMR8_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR8 Write Access Policy 14 (IMR8_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR8 Write Access Policy 13 (IMR8_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR8 Write Access Policy 12 (IMR8_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR8 Write Access Policy 11 (IMR8_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR8 Write Access Policy 10 (IMR8_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR8 Write Access Policy 9 (IMR8_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**IMR8 Write Access Policy 8 (IMR8_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR8 Write Access Policy 7 (IMR8_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR8 Write Access Policy 6 (IMR8_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR8 Write Access Policy 5 (IMR8_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR8 Write Access Policy 4 (IMR8_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR8 Write Access Policy 3 (IMR8_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR8 Write Access Policy 2 (IMR8_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR8 Write Access Policy 1 (IMR8_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR8 Write Access Policy 0 (IMR8_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR8 region, based on each agent's 6bit encoded SAI value.

5.9.52 IMR9 Base (B_CR_BIMR9BASE_0_0_0_MCHBAR)—Offset 6990h

This register, along with IMR9MASK, IMR9RAC and IMR9WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR9RAC and IMR9WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 1 IMR9 Base (IMR9_BASE):** Specifies bits 38:10 of the start address of IMR9 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR9MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR9 defined region.

5.9.53 IMR9 Mask (B_CR_BIMR9MASK_0_0_0_MCHBAR)—Offset 6994h

This register, along with IMR9BASE, IMR9RAC and IMR9WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR9RAC and IMR9WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback data HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester, depending on the setting of the GT_IWB_EN bit.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 1 IMR9 Mask (IMR9_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR9BASE[28:0] value. A match indicates that the incoming address falls within the IMR9 region.

5.9.54 IMR9 Control Policy (B_CR_BIMR9CP_0_0_0_MCHBAR)—Offset 6998h

This register controls the access policy to the Read Access Policy BIMR9RAC, the Write Access Policy BIMR9WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR9 Control Policy (IMR9_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR9RAC, BIMR9WAC, BIMR9CP registers based on the value from each agent's 6bit SAI field.

5.9.55 IMR9 Read Access Policy (B_CR_BIMR9RAC_0_0_0_MCHBAR)—Offset 69A0h

This register, along with IMR9BASE, IMR9MASK and IMR9WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR9. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR9 Read Access Policy 63 (IMR9_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR9 Read Access Policy 62 (IMR9_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR9 Read Access Policy 61 (IMR9_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR9 Read Access Policy 60 (IMR9_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR9 Read Access Policy 59 (IMR9_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR9 Read Access Policy 58 (IMR9_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR9 Read Access Policy 57 (IMR9_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR9 Read Access Policy 56 (IMR9_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR9 Read Access Policy 55 (IMR9_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR9 Read Access Policy 54 (IMR9_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR9 Read Access Policy 53 (IMR9_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR9 Read Access Policy 52 (IMR9_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR9 Read Access Policy 51 (IMR9_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR9 Read Access Policy 50 (IMR9_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR9 Read Access Policy 49 (IMR9_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**IMR9 Read Access Policy 48 (IMR9_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR9 Read Access Policy 47 (IMR9_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR9 Read Access Policy 46 (IMR9_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR9 Read Access Policy 45 (IMR9_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR9 Read Access Policy 44 (IMR9_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR9 Read Access Policy 43 (IMR9_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR9 Read Access Policy 42 (IMR9_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR9 Read Access Policy 41 (IMR9_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR9 Read Access Policy 40 (IMR9_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR9 Read Access Policy 39 (IMR9_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR9 Read Access Policy 38 (IMR9_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR9 Read Access Policy 37 (IMR9_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR9 Read Access Policy 36 (IMR9_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR9 Read Access Policy 35 (IMR9_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR9 Read Access Policy 34 (IMR9_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
33	0h RW	**IMR9 Read Access Policy 33 (IMR9_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR9 Read Access Policy 32 (IMR9_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR9 Read Access Policy 31 (IMR9_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR9 Read Access Policy 30 (IMR9_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR9 Read Access Policy 29 (IMR9_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR9 Read Access Policy 28 (IMR9_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR9 Read Access Policy 27 (IMR9_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR9 Read Access Policy 26 (IMR9_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR9 Read Access Policy 25 (IMR9_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR9 Read Access Policy 24 (IMR9_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR9 Read Access Policy 23 (IMR9_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR9 Read Access Policy 22 (IMR9_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR9 Read Access Policy 21 (IMR9_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR9 Read Access Policy 20 (IMR9_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR9 Read Access Policy 19 (IMR9_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**IMR9 Read Access Policy 18 (IMR9_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR9 Read Access Policy 17 (IMR9_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR9 Read Access Policy 16 (IMR9_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR9 Read Access Policy 15 (IMR9_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR9 Read Access Policy 14 (IMR9_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR9 Read Access Policy 13 (IMR9_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR9 Read Access Policy 12 (IMR9_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR9 Read Access Policy 11 (IMR9_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR9 Read Access Policy 10 (IMR9_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR9 Read Access Policy 9 (IMR9_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR9 Read Access Policy 8 (IMR9_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR9 Read Access Policy 7 (IMR9_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR9 Read Access Policy 6 (IMR9_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR9 Read Access Policy 5 (IMR9_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR9 Read Access Policy 4 (IMR9_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**IMR9 Read Access Policy 3 (IMR9_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR9 Read Access Policy 2 (IMR9_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR9 Read Access Policy 1 (IMR9_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR9 Read Access Policy 0 (IMR9_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR9 region, based on each agent's 6bit encoded SAI value.

5.9.56 IMR9 Write Access Policy (B_CR_BIMR9WAC_0_0_0_MCHBAR)—Offset 69A8h

This register, along with IMR9BASE, IMR9MASK and IMR9RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR9. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR9 Write Access Policy 63 (IMR9_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR9 Write Access Policy 62 (IMR9_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR9 Write Access Policy 61 (IMR9_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR9 Write Access Policy 60 (IMR9_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR9 Write Access Policy 59 (IMR9_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
58	0h RO	**IMR9 Write Access Policy 58 (IMR9_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR9 Write Access Policy 57 (IMR9_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR9 Write Access Policy 56 (IMR9_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR9 Write Access Policy 55 (IMR9_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR9 Write Access Policy 54 (IMR9_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR9 Write Access Policy 53 (IMR9_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR9 Write Access Policy 52 (IMR9_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR9 Write Access Policy 51 (IMR9_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR9 Write Access Policy 50 (IMR9_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR9 Write Access Policy 49 (IMR9_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR9 Write Access Policy 48 (IMR9_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR9 Write Access Policy 47 (IMR9_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR9 Write Access Policy 46 (IMR9_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR9 Write Access Policy 45 (IMR9_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR9 Write Access Policy 44 (IMR9_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
43	0h RW	**IMR9 Write Access Policy 43 (IMR9_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR9 Write Access Policy 42 (IMR9_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR9 Write Access Policy 41 (IMR9_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR9 Write Access Policy 40 (IMR9_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR9 Write Access Policy 39 (IMR9_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR9 Write Access Policy 38 (IMR9_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR9 Write Access Policy 37 (IMR9_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR9 Write Access Policy 36 (IMR9_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR9 Write Access Policy 35 (IMR9_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR9 Write Access Policy 34 (IMR9_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR9 Write Access Policy 33 (IMR9_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR9 Write Access Policy 32 (IMR9_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR9 Write Access Policy 31 (IMR9_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR9 Write Access Policy 30 (IMR9_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR9 Write Access Policy 29 (IMR9_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RW	**IMR9 Write Access Policy 28 (IMR9_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR9 Write Access Policy 27 (IMR9_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR9 Write Access Policy 26 (IMR9_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR9 Write Access Policy 25 (IMR9_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR9 Write Access Policy 24 (IMR9_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR9 Write Access Policy 23 (IMR9_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR9 Write Access Policy 22 (IMR9_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR9 Write Access Policy 21 (IMR9_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR9 Write Access Policy 20 (IMR9_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR9 Write Access Policy 19 (IMR9_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR9 Write Access Policy 18 (IMR9_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR9 Write Access Policy 17 (IMR9_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR9 Write Access Policy 16 (IMR9_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR9 Write Access Policy 15 (IMR9_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR9 Write Access Policy 14 (IMR9_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**IMR9 Write Access Policy 13 (IMR9_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR9 Write Access Policy 12 (IMR9_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR9 Write Access Policy 11 (IMR9_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR9 Write Access Policy 10 (IMR9_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR9 Write Access Policy 9 (IMR9_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR9 Write Access Policy 8 (IMR9_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR9 Write Access Policy 7 (IMR9_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR9 Write Access Policy 6 (IMR9_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR9 Write Access Policy 5 (IMR9_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR9 Write Access Policy 4 (IMR9_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR9 Write Access Policy 3 (IMR9_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR9 Write Access Policy 2 (IMR9_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR9 Write Access Policy 1 (IMR9_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR9 Write Access Policy 0 (IMR9_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR9 region, based on each agent's 6bit encoded SAI value.

5.9.57 IMR10 Base (B_CR_BIMR10BASE_0_0_0_MCHBAR)—Offset 69B0h

This register, along with IMR10MASK, IMR10RAC and IMR10WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR10RAC and IMR10WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR10 Base (IMR10_BASE):** Specifies bits 38:10 of the start address of IMR10 region. IMR region size must be a strict power of two at least 1KB and naturally aligned to the size. These bits are compared with the result of the IMR10MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR10 defined region.

5.9.58 IMR10 Mask (B_CR_BIMR10MASK_0_0_0_MCHBAR)—Offset 69B4h

This register, along with IMR10BASE, IMR10RAC and IMR10WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR10RAC and IMR10WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback data HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR10 Mask (IMR10_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR10BASE[28:0] value. A match indicates that the incoming address falls within the IMR10 region.

5.9.59 IMR10 Control Policy (B_CR_BIMR10CP_0_0_0_MCHBAR)—Offset 69B8h

This register controls the access policy to the Read Access Policy BIMR10RAC, the Write Access Policy BIMR10WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR10 Control Policy (IMR10_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR10RAC, BIMR10WAC and BIMR10CP, registers based on the value from each agent's 6bit SAI field.

5.9.60 IMR10 Read Access Policy (B_CR_BIMR10RAC_0_0_0_MCHBAR)—Offset 69C0h

This register, along with IMR10BASE, IMR10MASK and IMR10WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR10. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR10 Read Access Policy 63 (IMR10_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR10 Read Access Policy 62 (IMR10_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR10 Read Access Policy 61 (IMR10_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR10 Read Access Policy 60 (IMR10_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR10 Read Access Policy 59 (IMR10_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR10 Read Access Policy 58 (IMR10_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR10 Read Access Policy 57 (IMR10_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR10 Read Access Policy 56 (IMR10_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR10 Read Access Policy 55 (IMR10_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR10 Read Access Policy 54 (IMR10_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
53	0h RO	**IMR10 Read Access Policy 53 (IMR10_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR10 Read Access Policy 52 (IMR10_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR10 Read Access Policy 51 (IMR10_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR10 Read Access Policy 50 (IMR10_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR10 Read Access Policy 49 (IMR10_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR10 Read Access Policy 48 (IMR10_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR10 Read Access Policy 47 (IMR10_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR10 Read Access Policy 46 (IMR10_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR10 Read Access Policy 45 (IMR10_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR10 Read Access Policy 44 (IMR10_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR10 Read Access Policy 43 (IMR10_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR10 Read Access Policy 42 (IMR10_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR10 Read Access Policy 41 (IMR10_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR10 Read Access Policy 40 (IMR10_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR10 Read Access Policy 39 (IMR10_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
38	0h RW	**IMR10 Read Access Policy 38 (IMR10_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR10 Read Access Policy 37 (IMR10_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR10 Read Access Policy 36 (IMR10_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR10 Read Access Policy 35 (IMR10_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR10 Read Access Policy 34 (IMR10_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR10 Read Access Policy 33 (IMR10_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR10 Read Access Policy 32 (IMR10_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR10 Read Access Policy 31 (IMR10_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR10 Read Access Policy 30 (IMR10_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR10 Read Access Policy 29 (IMR10_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR10 Read Access Policy 28 (IMR10_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR10 Read Access Policy 27 (IMR10_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR10 Read Access Policy 26 (IMR10_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR10 Read Access Policy 25 (IMR10_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR10 Read Access Policy 24 (IMR10_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**IMR10 Read Access Policy 23 (IMR10_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR10 Read Access Policy 22 (IMR10_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR10 Read Access Policy 21 (IMR10_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR10 Read Access Policy 20 (IMR10_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR10 Read Access Policy 19 (IMR10_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR10 Read Access Policy 18 (IMR10_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR10 Read Access Policy 17 (IMR10_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR10 Read Access Policy 16 (IMR10_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR10 Read Access Policy 15 (IMR10_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR10 Read Access Policy 14 (IMR10_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR10 Read Access Policy 13 (IMR10_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR10 Read Access Policy 12 (IMR10_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR10 Read Access Policy 11 (IMR10_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR10 Read Access Policy 10 (IMR10_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR10 Read Access Policy 9 (IMR10_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**IMR10 Read Access Policy 8 (IMR10_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR10 Read Access Policy 7 (IMR10_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR10 Read Access Policy 6 (IMR10_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR10 Read Access Policy 5 (IMR10_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR10 Read Access Policy 4 (IMR10_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR10 Read Access Policy 3 (IMR10_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR10 Read Access Policy 2 (IMR10_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR10 Read Access Policy 1 (IMR10_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR10 Read Access Policy 0 (IMR10_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR10 region, based on each agent's 6bit encoded SAI value.

5.9.61 IMR10 Write Access Policy (B_CR_BIMR10WAC_0_0_0_MCHBAR)—Offset 69C8h

This register along with IMR10BASE, IMR10MASK and IMR10RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR10. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR10 Write Access Policy 63 (IMR10_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR10 Write Access Policy 62 (IMR10_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR10 Write Access Policy 61 (IMR10_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR10 Write Access Policy 60 (IMR10_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR10 Write Access Policy 59 (IMR10_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR10 Write Access Policy 58 (IMR10_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR10 Write Access Policy 57 (IMR10_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR10 Write Access Policy 56 (IMR10_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR10 Write Access Policy 55 (IMR10_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR10 Write Access Policy 54 (IMR10_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR10 Write Access Policy 53 (IMR10_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR10 Write Access Policy 52 (IMR10_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR10 Write Access Policy 51 (IMR10_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR10 Write Access Policy 50 (IMR10_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR10 Write Access Policy 49 (IMR10_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**IMR10 Write Access Policy 48 (IMR10_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR10 Write Access Policy 47 (IMR10_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR10 Write Access Policy 46 (IMR10_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR10 Write Access Policy 45 (IMR10_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR10 Write Access Policy 44 (IMR10_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR10 Write Access Policy 43 (IMR10_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR10 Write Access Policy 42 (IMR10_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR10 Write Access Policy 41 (IMR10_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR10 Write Access Policy 40 (IMR10_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR10 Write Access Policy 39 (IMR10_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR10 Write Access Policy 38 (IMR10_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR10 Write Access Policy 37 (IMR10_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR10 Write Access Policy 36 (IMR10_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR10 Write Access Policy 35 (IMR10_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR10 Write Access Policy 34 (IMR10_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
33	0h RW	**IMR10 Write Access Policy 33 (IMR10_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR10 Write Access Policy 32 (IMR10_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR10 Write Access Policy 31 (IMR10_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR10 Write Access Policy 30 (IMR10_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR10 Write Access Policy 29 (IMR10_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR10 Write Access Policy 28 (IMR10_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR10 Write Access Policy 27 (IMR10_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR10 Write Access Policy 26 (IMR10_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR10 Write Access Policy 25 (IMR10_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR10 Write Access Policy 24 (IMR10_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR10 Write Access Policy 23 (IMR10_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR10 Write Access Policy 22 (IMR10_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR10 Write Access Policy 21 (IMR10_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR10 Write Access Policy 20 (IMR10_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR10 Write Access Policy 19 (IMR10_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**IMR10 Write Access Policy 18 (IMR10_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR10 Write Access Policy 17 (IMR10_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR10 Write Access Policy 16 (IMR10_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR10 Write Access Policy 15 (IMR10_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR10 Write Access Policy 14 (IMR10_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR10 Write Access Policy 13 (IMR10_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR10 Write Access Policy 12 (IMR10_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR10 Write Access Policy 11 (IMR10_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR10 Write Access Policy 10 (IMR10_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR10 Write Access Policy 9 (IMR10_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR10 Write Access Policy 8 (IMR10_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR10 Write Access Policy 7 (IMR10_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR10 Write Access Policy 6 (IMR10_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR10 Write Access Policy 5 (IMR10_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR10 Write Access Policy 4 (IMR10_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**IMR10 Write Access Policy 3 (IMR10_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR10 Write Access Policy 2 (IMR10_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR10 Write Access Policy 1 (IMR10_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR10 Write Access Policy 0 (IMR10_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR10 region, based on each agent's 6bit encoded SAI value.

5.9.62 IMR11 Base (B_CR_BIMR11BASE_0_0_0_MCHBAR)—Offset 69D0h

This register, along with IMR11MASK, IMR11RAC and IMR11WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR11RAC and IMR11WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR11 Base (IMR11_BASE):** Specifies bits 38:10 of the start address of IMR11 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR11MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR11 defined region.

5.9.63 IMR11 Mask (B_CR_BIMR11MASK_0_0_0_MCHBAR)—Offset 69D4h

This register, along with IMR11BASE, IMR11RAC and IMR11WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR11RAC and IMR11WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback data HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester, depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester, depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR11 Mask (IMR11_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR11BASE[28:0] value. A match indicates that the incoming address falls within the IMR11 region.

5.9.64 IMR11 Control Policy (B_CR_BIMR11CP_0_0_0_MCHBAR)—Offset 69D8h

This register controls the access policy to the Read Access Policy BIMR11RAC, the Write Access Policy BIMR11WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR11 Control Policy (IMR11_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR11RAC, BIMR11WAC and BIMR11CP registers, based on the value from each agent's 6bit SAI field.

5.9.65 IMR11 Read Access Policy (B_CR_BIMR11RAC_0_0_0_MCHBAR)—Offset 69E0h

This register, along with IMR11BASE, IMR11MASK and IMR11WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR11. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR11 Read Access Policy 63 (IMR11_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR11 Read Access Policy 62 (IMR11_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR11 Read Access Policy 61 (IMR11_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR11 Read Access Policy 60 (IMR11_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR11 Read Access Policy 59 (IMR11_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR11 Read Access Policy 58 (IMR11_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
57	0h RO	**IMR11 Read Access Policy 57 (IMR11_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR11 Read Access Policy 56 (IMR11_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR11 Read Access Policy 55 (IMR11_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR11 Read Access Policy 54 (IMR11_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR11 Read Access Policy 53 (IMR11_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR11 Read Access Policy 52 (IMR11_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR11 Read Access Policy 51 (IMR11_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR11 Read Access Policy 50 (IMR11_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR11 Read Access Policy 49 (IMR11_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR11 Read Access Policy 48 (IMR11_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR11 Read Access Policy 47 (IMR11_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR11 Read Access Policy 46 (IMR11_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR11 Read Access Policy 45 (IMR11_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR11 Read Access Policy 44 (IMR11_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR11 Read Access Policy 43 (IMR11_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
42	0h RW	**IMR11 Read Access Policy 42 (IMR11_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR11 Read Access Policy 41 (IMR11_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR11 Read Access Policy 40 (IMR11_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR11 Read Access Policy 39 (IMR11_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR11 Read Access Policy 38 (IMR11_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR11 Read Access Policy 37 (IMR11_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR11 Read Access Policy 36 (IMR11_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR11 Read Access Policy 35 (IMR11_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR11 Read Access Policy 34 (IMR11_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR11 Read Access Policy 33 (IMR11_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR11 Read Access Policy 32 (IMR11_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR11 Read Access Policy 31 (IMR11_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR11 Read Access Policy 30 (IMR11_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR11 Read Access Policy 29 (IMR11_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR11 Read Access Policy 28 (IMR11_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW	**IMR11 Read Access Policy 27 (IMR11_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR11 Read Access Policy 26 (IMR11_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR11 Read Access Policy 25 (IMR11_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR11 Read Access Policy 24 (IMR11_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR11 Read Access Policy 23 (IMR11_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR11 Read Access Policy 22 (IMR11_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR11 Read Access Policy 21 (IMR11_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR11 Read Access Policy 20 (IMR11_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR11 Read Access Policy 19 (IMR11_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR11 Read Access Policy 18 (IMR11_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR11 Read Access Policy 17 (IMR11_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR11 Read Access Policy 16 (IMR11_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR11 Read Access Policy 15 (IMR11_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR11 Read Access Policy 14 (IMR11_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR11 Read Access Policy 13 (IMR11_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**IMR11 Read Access Policy 12 (IMR11_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR11 Read Access Policy 11 (IMR11_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR11 Read Access Policy 10 (IMR11_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR11 Read Access Policy 9 (IMR11_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR11 Read Access Policy 8 (IMR11_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR11 Read Access Policy 7 (IMR11_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR11 Read Access Policy 6 (IMR11_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR11 Read Access Policy 5 (IMR11_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR11 Read Access Policy 4 (IMR11_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR11 Read Access Policy 3 (IMR11_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR11 Read Access Policy 2 (IMR11_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR11 Read Access Policy 1 (IMR11_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR11 Read Access Policy 0 (IMR11_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR11 region, based on each agent's 6bit encoded SAI value.

5.9.66 IMR11 Write Access Policy (B_CR_BIMR11WAC_0_0_0_MCHBAR)—Offset 69E8h

This register, along with IMR11BASE, IMR11MASK and IMR11RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR11. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR11 Write Access Policy 63 (IMR11_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR11 Write Access Policy 62 (IMR11_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR11 Write Access Policy 61 (IMR11_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR11 Write Access Policy 60 (IMR11_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR11 Write Access Policy 59 (IMR11_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR11 Write Access Policy 58 (IMR11_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR11 Write Access Policy 57 (IMR11_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR11 Write Access Policy 56 (IMR11_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR11 Write Access Policy 55 (IMR11_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR11 Write Access Policy 54 (IMR11_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
53	0h RO	**IMR11 Write Access Policy 53 (IMR11_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR11 Write Access Policy 52 (IMR11_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR11 Write Access Policy 51 (IMR11_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR11 Write Access Policy 50 (IMR11_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR11 Write Access Policy 49 (IMR11_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR11 Write Access Policy 48 (IMR11_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR11 Write Access Policy 47 (IMR11_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR11 Write Access Policy 46 (IMR11_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR11 Write Access Policy 45 (IMR11_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR11 Write Access Policy 44 (IMR11_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR11 Write Access Policy 43 (IMR11_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR11 Write Access Policy 42 (IMR11_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR11 Write Access Policy 41 (IMR11_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR11 Write Access Policy 40 (IMR11_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR11 Write Access Policy 39 (IMR11_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
38	0h RW	**IMR11 Write Access Policy 38 (IMR11_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR11 Write Access Policy 37 (IMR11_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR11 Write Access Policy 36 (IMR11_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR11 Write Access Policy 35 (IMR11_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR11 Write Access Policy 34 (IMR11_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR11 Write Access Policy 33 (IMR11_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR11 Write Access Policy 32 (IMR11_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR11 Write Access Policy 31 (IMR11_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR11 Write Access Policy 30 (IMR11_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR11 Write Access Policy 29 (IMR11_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR11 Write Access Policy 28 (IMR11_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR11 Write Access Policy 27 (IMR11_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR11 Write Access Policy 26 (IMR11_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR11 Write Access Policy 25 (IMR11_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR11 Write Access Policy 24 (IMR11_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**IMR11 Write Access Policy 23 (IMR11_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR11 Write Access Policy 22 (IMR11_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR11 Write Access Policy 21 (IMR11_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR11 Write Access Policy 20 (IMR11_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR11 Write Access Policy 19 (IMR11_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR11 Write Access Policy 18 (IMR11_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR11 Write Access Policy 17 (IMR11_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR11 Write Access Policy 16 (IMR11_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR11 Write Access Policy 15 (IMR11_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR11 Write Access Policy 14 (IMR11_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR11 Write Access Policy 13 (IMR11_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR11 Write Access Policy 12 (IMR11_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR11 Write Access Policy 11 (IMR11_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR11 Write Access Policy 10 (IMR11_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR11 Write Access Policy 9 (IMR11_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**IMR11 Write Access Policy 8 (IMR11_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR11 Write Access Policy 7 (IMR11_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR11 Write Access Policy 6 (IMR11_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR11 Write Access Policy 5 (IMR11_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR11 Write Access Policy 4 (IMR11_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR11 Write Access Policy 3 (IMR11_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR11 Write Access Policy 2 (IMR11_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR11 Write Access Policy 1 (IMR11_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR11 Write Access Policy 0 (IMR11_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR11 region, based on each agent's 6bit encoded SAI value.

5.9.67 IMR12 Base (B_CR_BIMR12BASE_0_0_0_MCHBAR)—Offset 69F0h

This register, along with IMR12MASK, IMR12RAC and IMR12WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR12RAC and IMR12WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR12 Base (IMR12_BASE):** Specifies bits 38:10 of the start address of IMR12 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR12MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR12 defined region.

5.9.68 IMR12 Mask (B_CR_BIMR12MASK_0_0_0_MCHBAR)—Offset 69F4h

This register, along with IMR12BASE, IMR12RAC and IMR12WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR12RAC and IMR12WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester, depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester, depending on the setting of the GT_IWB_EN bit.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR12 Mask (IMR12_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR12BASE[28:0] value. A match indicates that the incoming address falls within the IMR12 region.

5.9.69 IMR12 Control Policy (B_CR_BIMR12CP_0_0_0_MCHBAR)—Offset 69F8h

This register controls the access policy to the Read Access Policy BIMR12RAC, the Write Access Policy BIMR12WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR12 Control Policy (IMR12_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR12RAC, BIMR12WAC and BIMR12CP registers, based on the value from each agent's 6bit SAI field.

5.9.70 IMR12 Read Access Policy (B_CR_BIMR12RAC_0_0_0_MCHBAR)—Offset 6A00h

This register, along with IMR12BASE, IMR12MASK and IMR12WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR12. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR12 Read Access Policy 63 (IMR12_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR12 Read Access Policy 62 (IMR12_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR12 Read Access Policy 61 (IMR12_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR12 Read Access Policy 60 (IMR12_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR12 Read Access Policy 59 (IMR12_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR12 Read Access Policy 58 (IMR12_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR12 Read Access Policy 57 (IMR12_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR12 Read Access Policy 56 (IMR12_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR12 Read Access Policy 55 (IMR12_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR12 Read Access Policy 54 (IMR12_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR12 Read Access Policy 53 (IMR12_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR12 Read Access Policy 52 (IMR12_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR12 Read Access Policy 51 (IMR12_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR12 Read Access Policy 50 (IMR12_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR12 Read Access Policy 49 (IMR12_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**IMR12 Read Access Policy 48 (IMR12_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR12 Read Access Policy 47 (IMR12_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR12 Read Access Policy 46 (IMR12_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR12 Read Access Policy 45 (IMR12_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR12 Read Access Policy 44 (IMR12_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR12 Read Access Policy 43 (IMR12_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR12 Read Access Policy 42 (IMR12_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR12 Read Access Policy 41 (IMR12_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR12 Read Access Policy 40 (IMR12_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR12 Read Access Policy 39 (IMR12_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR12 Read Access Policy 38 (IMR12_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR12 Read Access Policy 37 (IMR12_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR12 Read Access Policy 36 (IMR12_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR12 Read Access Policy 35 (IMR12_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR12 Read Access Policy 34 (IMR12_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
33	0h RW	**IMR12 Read Access Policy 33 (IMR12_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR12 Read Access Policy 32 (IMR12_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR12 Read Access Policy 31 (IMR12_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR12 Read Access Policy 30 (IMR12_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR12 Read Access Policy 29 (IMR12_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR12 Read Access Policy 28 (IMR12_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR12 Read Access Policy 27 (IMR12_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR12 Read Access Policy 26 (IMR12_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR12 Read Access Policy 25 (IMR12_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR12 Read Access Policy 24 (IMR12_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR12 Read Access Policy 23 (IMR12_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR12 Read Access Policy 22 (IMR12_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR12 Read Access Policy 21 (IMR12_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR12 Read Access Policy 20 (IMR12_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR12 Read Access Policy 19 (IMR12_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**IMR12 Read Access Policy 18 (IMR12_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR12 Read Access Policy 17 (IMR12_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR12 Read Access Policy 16 (IMR12_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR12 Read Access Policy 15 (IMR12_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR12 Read Access Policy 14 (IMR12_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR12 Read Access Policy 13 (IMR12_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR12 Read Access Policy 12 (IMR12_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR12 Read Access Policy 11 (IMR12_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR12 Read Access Policy 10 (IMR12_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR12 Read Access Policy 9 (IMR12_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR12 Read Access Policy 8 (IMR12_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR12 Read Access Policy 7 (IMR12_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR12 Read Access Policy 6 (IMR12_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR12 Read Access Policy 5 (IMR12_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR12 Read Access Policy 4 (IMR12_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**IMR12 Read Access Policy 3 (IMR12_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR12 Read Access Policy 2 (IMR12_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR12 Read Access Policy 1 (IMR12_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR12 Read Access Policy 0 (IMR12_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR12 region, based on each agent's 6bit encoded SAI value.

5.9.71 IMR12 Write Access Policy (B_CR_BIMR12WAC_0_0_0_MCHBAR)—Offset 6A08h

This register, along with IMR12BASE, IMR12MASK and IMR12RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR12. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR12 Write Access Policy 63 (IMR12_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR12 Write Access Policy 62 (IMR12_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR12 Write Access Policy 61 (IMR12_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR12 Write Access Policy 60 (IMR12_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR12 Write Access Policy 59 (IMR12_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
58	0h RO	**IMR12 Write Access Policy 58 (IMR12_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR12 Write Access Policy 57 (IMR12_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR12 Write Access Policy 56 (IMR12_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR12 Write Access Policy 55 (IMR12_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR12 Write Access Policy 54 (IMR12_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR12 Write Access Policy 53 (IMR12_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR12 Write Access Policy 52 (IMR12_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR12 Write Access Policy 51 (IMR12_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR12 Write Access Policy 50 (IMR12_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR12 Write Access Policy 49 (IMR12_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR12 Write Access Policy 48 (IMR12_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR12 Write Access Policy 47 (IMR12_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR12 Write Access Policy 46 (IMR12_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR12 Write Access Policy 45 (IMR12_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR12 Write Access Policy 44 (IMR12_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
43	0h RW	**IMR12 Write Access Policy 43 (IMR12_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR12 Write Access Policy 42 (IMR12_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR12 Write Access Policy 41 (IMR12_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR12 Write Access Policy 40 (IMR12_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR12 Write Access Policy 39 (IMR12_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR12 Write Access Policy 38 (IMR12_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR12 Write Access Policy 37 (IMR12_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR12 Write Access Policy 36 (IMR12_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR12 Write Access Policy 35 (IMR12_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR12 Write Access Policy 34 (IMR12_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR12 Write Access Policy 33 (IMR12_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR12 Write Access Policy 32 (IMR12_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR12 Write Access Policy 31 (IMR12_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR12 Write Access Policy 30 (IMR12_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR12 Write Access Policy 29 (IMR12_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RW	**IMR12 Write Access Policy 28 (IMR12_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR12 Write Access Policy 27 (IMR12_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR12 Write Access Policy 26 (IMR12_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR12 Write Access Policy 25 (IMR12_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR12 Write Access Policy 24 (IMR12_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR12 Write Access Policy 23 (IMR12_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR12 Write Access Policy 22 (IMR12_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR12 Write Access Policy 21 (IMR12_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR12 Write Access Policy 20 (IMR12_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR12 Write Access Policy 19 (IMR12_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR12 Write Access Policy 18 (IMR12_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR12 Write Access Policy 17 (IMR12_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR12 Write Access Policy 16 (IMR12_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR12 Write Access Policy 15 (IMR12_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR12 Write Access Policy 14 (IMR12_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**IMR12 Write Access Policy 13 (IMR12_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR12 Write Access Policy 12 (IMR12_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR12 Write Access Policy 11 (IMR12_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR12 Write Access Policy 10 (IMR12_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR12 Write Access Policy 9 (IMR12_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR12 Write Access Policy 8 (IMR12_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR12 Write Access Policy 7 (IMR12_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR12 Write Access Policy 6 (IMR12_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR12 Write Access Policy 5 (IMR12_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR12 Write Access Policy 4 (IMR12_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR12 Write Access Policy 3 (IMR12_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR12 Write Access Policy 2 (IMR12_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR12 Write Access Policy 1 (IMR12_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR12 Write Access Policy 0 (IMR12_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR12 region, based on each agent's 6bit encoded SAI value.

5.9.72 IMR13 Base (B_CR_BIMR13BASE_0_0_0_MCHBAR)—Offset 6A10h

This register, along with IMR13MASK, IMR13RAC and IMR13WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR13RAC and IMR13WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR13 Base (IMR13_BASE):** Specifies bits 38:10 of the start address of IMR13 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR13MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR13 defined region.

5.9.73 IMR13 Mask (B_CR_BIMR13MASK_0_0_0_MCHBAR)—Offset 6A14h

This register, along with IMR13BASE, IMR13RAC and IMR13WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR13RAC and IMR13WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR13 Mask (IMR13_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR13BASE[28:0] value. A match indicates that the incoming address falls within the IMR13 region.

5.9.74 IMR13 Control Policy (B_CR_BIMR13CP_0_0_0_MCHBAR)—Offset 6A18h

This register controls the access policy to the Read Access Policy BIMR13RAC, the Write Access Policy BIMR13WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR13 Control Policy (IMR13_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR13RAC, BIMR13WAC and BIMR13CP registers, based on the value from each agent's 6bit SAI field.

5.9.75 IMR13 Read Access Policy (B_CR_BIMR13RAC_0_0_0_MCHBAR)—Offset 6A20h

This register, along with IMR13BASE, IMR13MASK and IMR13WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR13. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR13 Read Access Policy 63 (IMR13_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR13 Read Access Policy 62 (IMR13_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR13 Read Access Policy 61 (IMR13_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR13 Read Access Policy 60 (IMR13_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR13 Read Access Policy 59 (IMR13_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR13 Read Access Policy 58 (IMR13_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR13 Read Access Policy 57 (IMR13_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR13 Read Access Policy 56 (IMR13_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR13 Read Access Policy 55 (IMR13_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR13 Read Access Policy 54 (IMR13_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
53	0h RO	**IMR13 Read Access Policy 53 (IMR13_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR13 Read Access Policy 52 (IMR13_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR13 Read Access Policy 51 (IMR13_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR13 Read Access Policy 50 (IMR13_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR13 Read Access Policy 49 (IMR13_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR13 Read Access Policy 48 (IMR13_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR13 Read Access Policy 47 (IMR13_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR13 Read Access Policy 46 (IMR13_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR13 Read Access Policy 45 (IMR13_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR13 Read Access Policy 44 (IMR13_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR13 Read Access Policy 43 (IMR13_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR13 Read Access Policy 42 (IMR13_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR13 Read Access Policy 41 (IMR13_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR13 Read Access Policy 40 (IMR13_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR13 Read Access Policy 39 (IMR13_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
38	0h RW	**IMR13 Read Access Policy 38 (IMR13_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR13 Read Access Policy 37 (IMR13_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR13 Read Access Policy 36 (IMR13_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR13 Read Access Policy 35 (IMR13_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR13 Read Access Policy 34 (IMR13_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR13 Read Access Policy 33 (IMR13_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR13 Read Access Policy 32 (IMR13_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR13 Read Access Policy 31 (IMR13_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR13 Read Access Policy 30 (IMR13_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR13 Read Access Policy 29 (IMR13_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR13 Read Access Policy 28 (IMR13_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR13 Read Access Policy 27 (IMR13_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR13 Read Access Policy 26 (IMR13_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR13 Read Access Policy 25 (IMR13_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR13 Read Access Policy 24 (IMR13_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**IMR13 Read Access Policy 23 (IMR13_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR13 Read Access Policy 22 (IMR13_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR13 Read Access Policy 21 (IMR13_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR13 Read Access Policy 20 (IMR13_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR13 Read Access Policy 19 (IMR13_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR13 Read Access Policy 18 (IMR13_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR13 Read Access Policy 17 (IMR13_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR13 Read Access Policy 16 (IMR13_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR13 Read Access Policy 15 (IMR13_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR13 Read Access Policy 14 (IMR13_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR13 Read Access Policy 13 (IMR13_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR13 Read Access Policy 12 (IMR13_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR13 Read Access Policy 11 (IMR13_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR13 Read Access Policy 10 (IMR13_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR13 Read Access Policy 9 (IMR13_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**IMR13 Read Access Policy 8 (IMR13_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR13 Read Access Policy 7 (IMR13_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR13 Read Access Policy 6 (IMR13_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR13 Read Access Policy 5 (IMR13_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR13 Read Access Policy 4 (IMR13_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR13 Read Access Policy 3 (IMR13_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR13 Read Access Policy 2 (IMR13_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR13 Read Access Policy 1 (IMR13_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR13 Read Access Policy 0 (IMR13_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR13 region, based on each agent's 6bit encoded SAI value.

5.9.76 IMR13 Write Access Policy (B_CR_BIMR13WAC_0_0_0_MCHBAR)—Offset 6A28h

This register, along with IMR13BASE, IMR13MASK and IMR13RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR13. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR13 Write Access Policy 63 (IMR13_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR13 Write Access Policy 62 (IMR13_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR13 Write Access Policy 61 (IMR13_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR13 Write Access Policy 60 (IMR13_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR13 Write Access Policy 59 (IMR13_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR13 Write Access Policy 58 (IMR13_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR13 Write Access Policy 57 (IMR13_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR13 Write Access Policy 56 (IMR13_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR13 Write Access Policy 55 (IMR13_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR13 Write Access Policy 54 (IMR13_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR13 Write Access Policy 53 (IMR13_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR13 Write Access Policy 52 (IMR13_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR13 Write Access Policy 51 (IMR13_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR13 Write Access Policy 50 (IMR13_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR13 Write Access Policy 49 (IMR13_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**IMR13 Write Access Policy 48 (IMR13_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR13 Write Access Policy 47 (IMR13_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR13 Write Access Policy 46 (IMR13_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR13 Write Access Policy 45 (IMR13_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR13 Write Access Policy 44 (IMR13_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR13 Write Access Policy 43 (IMR13_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR13 Write Access Policy 42 (IMR13_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR13 Write Access Policy 41 (IMR13_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR13 Write Access Policy 40 (IMR13_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR13 Write Access Policy 39 (IMR13_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR13 Write Access Policy 38 (IMR13_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR13 Write Access Policy 37 (IMR13_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR13 Write Access Policy 36 (IMR13_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR13 Write Access Policy 35 (IMR13_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR13 Write Access Policy 34 (IMR13_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
33	0h RW	**IMR13 Write Access Policy 33 (IMR13_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR13 Write Access Policy 32 (IMR13_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR13 Write Access Policy 31 (IMR13_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR13 Write Access Policy 30 (IMR13_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR13 Write Access Policy 29 (IMR13_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR13 Write Access Policy 28 (IMR13_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR13 Write Access Policy 27 (IMR13_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR13 Write Access Policy 26 (IMR13_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR13 Write Access Policy 25 (IMR13_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR13 Write Access Policy 24 (IMR13_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR13 Write Access Policy 23 (IMR13_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR13 Write Access Policy 22 (IMR13_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR13 Write Access Policy 21 (IMR13_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR13 Write Access Policy 20 (IMR13_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR13 Write Access Policy 19 (IMR13_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**IMR13 Write Access Policy 18 (IMR13_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR13 Write Access Policy 17 (IMR13_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR13 Write Access Policy 16 (IMR13_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR13 Write Access Policy 15 (IMR13_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR13 Write Access Policy 14 (IMR13_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR13 Write Access Policy 13 (IMR13_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR13 Write Access Policy 12 (IMR13_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR13 Write Access Policy 11 (IMR13_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR13 Write Access Policy 10 (IMR13_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR13 Write Access Policy 9 (IMR13_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR13 Write Access Policy 8 (IMR13_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR13 Write Access Policy 7 (IMR13_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR13 Write Access Policy 6 (IMR13_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR13 Write Access Policy 5 (IMR13_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR13 Write Access Policy 4 (IMR13_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**IMR13 Write Access Policy 3 (IMR13_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR13 Write Access Policy 2 (IMR13_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR13 Write Access Policy 1 (IMR13_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR13 Write Access Policy 0 (IMR13_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR13 region, based on each agent's 6bit encoded SAI value.

5.9.77 IMR14 Base (B_CR_BIMR14BASE_0_0_0_MCHBAR)—Offset 6A30h

This register, along with IMR14MASK, IMR14RAC and IMR14WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR14RAC and IMR14WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR14 Base (IMR14_BASE):** Specifies bits 38:10 of the start address of IMR14 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR14MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR14 defined region.

5.9.78 IMR14 Mask (B_CR_BIMR14MASK_0_0_0_MCHBAR)—Offset 6A34h

This register, along with IMR14BASE, IMR14RAC and IMR14WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR14RAC and IMR14WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester, depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR14 Mask (IMR14_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR14BASE[28:0] value. A match indicates that the incoming address falls within the IMR14 region.

5.9.79 IMR14 Control Policy (B_CR_BIMR14CP_0_0_0_MCHBAR)—Offset 6A38h

This register controls the access policy to the Read Access Policy BIMR14RAC, the Write Access Policy BIMR14WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR14 Control Policy (IMR14_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR14RAC, BIMR14WAC and BIMR14CP registers, based on the value from each agent's 6bit SAI field.

5.9.80 IMR14 Read Access Policy (B_CR_BIMR14RAC_0_0_0_MCHBAR)—Offset 6A40h

This register, along with IMR14BASE, IMR14MASK and IMR14WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR14. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR14 Read Access Policy 63 (IMR14_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR14 Read Access Policy 62 (IMR14_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR14 Read Access Policy 61 (IMR14_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR14 Read Access Policy 60 (IMR14_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR14 Read Access Policy 59 (IMR14_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR14 Read Access Policy 58 (IMR14_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
57	0h RO	**IMR14 Read Access Policy 57 (IMR14_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR14 Read Access Policy 56 (IMR14_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR14 Read Access Policy 55 (IMR14_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR14 Read Access Policy 54 (IMR14_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR14 Read Access Policy 53 (IMR14_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR14 Read Access Policy 52 (IMR14_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR14 Read Access Policy 51 (IMR14_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR14 Read Access Policy 50 (IMR14_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR14 Read Access Policy 49 (IMR14_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR14 Read Access Policy 48 (IMR14_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR14 Read Access Policy 47 (IMR14_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR14 Read Access Policy 46 (IMR14_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR14 Read Access Policy 45 (IMR14_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR14 Read Access Policy 44 (IMR14_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR14 Read Access Policy 43 (IMR14_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
42	0h RW	**IMR14 Read Access Policy 42 (IMR14_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR14 Read Access Policy 41 (IMR14_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR14 Read Access Policy 40 (IMR14_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR14 Read Access Policy 39 (IMR14_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR14 Read Access Policy 38 (IMR14_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR14 Read Access Policy 37 (IMR14_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR14 Read Access Policy 36 (IMR14_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR14 Read Access Policy 35 (IMR14_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR14 Read Access Policy 34 (IMR14_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR14 Read Access Policy 33 (IMR14_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR14 Read Access Policy 32 (IMR14_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR14 Read Access Policy 31 (IMR14_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR14 Read Access Policy 30 (IMR14_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR14 Read Access Policy 29 (IMR14_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR14 Read Access Policy 28 (IMR14_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW	**IMR14 Read Access Policy 27 (IMR14_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR14 Read Access Policy 26 (IMR14_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR14 Read Access Policy 25 (IMR14_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR14 Read Access Policy 24 (IMR14_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR14 Read Access Policy 23 (IMR14_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR14 Read Access Policy 22 (IMR14_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR14 Read Access Policy 21 (IMR14_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR14 Read Access Policy 20 (IMR14_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR14 Read Access Policy 19 (IMR14_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR14 Read Access Policy 18 (IMR14_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR14 Read Access Policy 17 (IMR14_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR14 Read Access Policy 16 (IMR14_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR14 Read Access Policy 15 (IMR14_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR14 Read Access Policy 14 (IMR14_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR14 Read Access Policy 13 (IMR14_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**IMR14 Read Access Policy 12 (IMR14_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR14 Read Access Policy 11 (IMR14_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR14 Read Access Policy 10 (IMR14_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR14 Read Access Policy 9 (IMR14_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR14 Read Access Policy 8 (IMR14_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR14 Read Access Policy 7 (IMR14_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR14 Read Access Policy 6 (IMR14_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR14 Read Access Policy 5 (IMR14_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR14 Read Access Policy 4 (IMR14_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR14 Read Access Policy 3 (IMR14_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR14 Read Access Policy 2 (IMR14_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR14 Read Access Policy 1 (IMR14_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR14 Read Access Policy 0 (IMR14_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR14 region, based on each agent's 6bit encoded SAI value.

5.9.81 IMR14 Write Access Policy (B_CR_BIMR14WAC_0_0_0_MCHBAR)—Offset 6A48h

This register, along with IMR14BASE IMR14MASK and IMR14RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR14. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR14 Write Access Policy 63 (IMR14_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR14 Write Access Policy 62 (IMR14_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR14 Write Access Policy 61 (IMR14_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR14 Write Access Policy 60 (IMR14_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR14 Write Access Policy 59 (IMR14_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR14 Write Access Policy 58 (IMR14_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR14 Write Access Policy 57 (IMR14_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR14 Write Access Policy 56 (IMR14_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR14 Write Access Policy 55 (IMR14_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR14 Write Access Policy 54 (IMR14_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
53	0h RO	**IMR14 Write Access Policy 53 (IMR14_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR14 Write Access Policy 52 (IMR14_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR14 Write Access Policy 51 (IMR14_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR14 Write Access Policy 50 (IMR14_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR14 Write Access Policy 49 (IMR14_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR14 Write Access Policy 48 (IMR14_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR14 Write Access Policy 47 (IMR14_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR14 Write Access Policy 46 (IMR14_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR14 Write Access Policy 45 (IMR14_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR14 Write Access Policy 44 (IMR14_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR14 Write Access Policy 43 (IMR14_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR14 Write Access Policy 42 (IMR14_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR14 Write Access Policy 41 (IMR14_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR14 Write Access Policy 40 (IMR14_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR14 Write Access Policy 39 (IMR14_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
38	0h RW	**IMR14 Write Access Policy 38 (IMR14_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR14 Write Access Policy 37 (IMR14_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR14 Write Access Policy 36 (IMR14_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR14 Write Access Policy 35 (IMR14_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR14 Write Access Policy 34 (IMR14_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR14 Write Access Policy 33 (IMR14_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR14 Write Access Policy 32 (IMR14_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR14 Write Access Policy 31 (IMR14_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR14 Write Access Policy 30 (IMR14_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR14 Write Access Policy 29 (IMR14_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR14 Write Access Policy 28 (IMR14_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR14 Write Access Policy 27 (IMR14_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR14 Write Access Policy 26 (IMR14_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR14 Write Access Policy 25 (IMR14_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR14 Write Access Policy 24 (IMR14_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**IMR14 Write Access Policy 23 (IMR14_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR14 Write Access Policy 22 (IMR14_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR14 Write Access Policy 21 (IMR14_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR14 Write Access Policy 20 (IMR14_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR14 Write Access Policy 19 (IMR14_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR14 Write Access Policy 18 (IMR14_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR14 Write Access Policy 17 (IMR14_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR14 Write Access Policy 16 (IMR14_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR14 Write Access Policy 15 (IMR14_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR14 Write Access Policy 14 (IMR14_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR14 Write Access Policy 13 (IMR14_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR14 Write Access Policy 12 (IMR14_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR14 Write Access Policy 11 (IMR14_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR14 Write Access Policy 10 (IMR14_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR14 Write Access Policy 9 (IMR14_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**IMR14 Write Access Policy 8 (IMR14_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR14 Write Access Policy 7 (IMR14_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR14 Write Access Policy 6 (IMR14_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR14 Write Access Policy 5 (IMR14_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR14 Write Access Policy 4 (IMR14_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR14 Write Access Policy 3 (IMR14_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR14 Write Access Policy 2 (IMR14_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR14 Write Access Policy 1 (IMR14_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR14 Write Access Policy 0 (IMR14_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR14 region, based on each agent's 6bit encoded SAI value.

5.9.82 IMR15 Base (B_CR_BIMR15BASE_0_0_0_MCHBAR)—Offset 6A50h

This register, along with IMR15MASK, IMR15RAC and IMR15WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR15RAC and IMR15WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR15 Base (IMR15_BASE):** Specifies bits 38:10 of the start address of IMR15 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR15MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR15 defined region.

5.9.83 IMR15 Mask (B_CR_BIMR15MASK_0_0_0_MCHBAR)—Offset 6A54h

This register, along with IMR15BASE, IMR15RAC and IMR15WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR15RAC and IMR15WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester, depending on the setting of the GT_IWB_EN bit.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR15 Mask (IMR15_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR15BASE[28:0] value. A match indicates that the incoming address falls within the IMR15 region.

5.9.84 IMR15 Control Policy (B_CR_BIMR15CP_0_0_0_MCHBAR)—Offset 6A58h

This register controls the access policy to the Read Access Policy BIMR15RAC, the Write Access Policy BIMR15WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR15 Control Policy (IMR15_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR15RAC, BIMR15WAC and BIMR15CP registers, based on the value from each agent's 6bit SAI field.

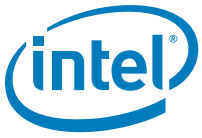
5.9.85 IMR15 Read Access Policy (B_CR_BIMR15RAC_0_0_0_MCHBAR)—Offset 6A60h

This register, along with IMR15BASE, IMR15MASK and IMR15WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR15. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR15 Read Access Policy 63 (IMR15_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR15 Read Access Policy 62 (IMR15_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR15 Read Access Policy 61 (IMR15_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR15 Read Access Policy 60 (IMR15_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR15 Read Access Policy 59 (IMR15_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR15 Read Access Policy 58 (IMR15_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR15 Read Access Policy 57 (IMR15_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR15 Read Access Policy 56 (IMR15_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR15 Read Access Policy 55 (IMR15_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR15 Read Access Policy 54 (IMR15_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR15 Read Access Policy 53 (IMR15_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR15 Read Access Policy 52 (IMR15_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR15 Read Access Policy 51 (IMR15_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR15 Read Access Policy 50 (IMR15_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR15 Read Access Policy 49 (IMR15_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**IMR15 Read Access Policy 48 (IMR15_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR15 Read Access Policy 47 (IMR15_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR15 Read Access Policy 46 (IMR15_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR15 Read Access Policy 45 (IMR15_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR15 Read Access Policy 44 (IMR15_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR15 Read Access Policy 43 (IMR15_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR15 Read Access Policy 42 (IMR15_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR15 Read Access Policy 41 (IMR15_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR15 Read Access Policy 40 (IMR15_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR15 Read Access Policy 39 (IMR15_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR15 Read Access Policy 38 (IMR15_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR15 Read Access Policy 37 (IMR15_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR15 Read Access Policy 36 (IMR15_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR15 Read Access Policy 35 (IMR15_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR15 Read Access Policy 34 (IMR15_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
33	0h RW	**IMR15 Read Access Policy 33 (IMR15_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR15 Read Access Policy 32 (IMR15_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR15 Read Access Policy 31 (IMR15_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR15 Read Access Policy 30 (IMR15_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR15 Read Access Policy 29 (IMR15_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR15 Read Access Policy 28 (IMR15_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR15 Read Access Policy 27 (IMR15_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR15 Read Access Policy 26 (IMR15_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR15 Read Access Policy 25 (IMR15_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR15 Read Access Policy 24 (IMR15_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR15 Read Access Policy 23 (IMR15_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR15 Read Access Policy 22 (IMR15_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR15 Read Access Policy 21 (IMR15_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR15 Read Access Policy 20 (IMR15_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR15 Read Access Policy 19 (IMR15_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**IMR15 Read Access Policy 18 (IMR15_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR15 Read Access Policy 17 (IMR15_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR15 Read Access Policy 16 (IMR15_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR15 Read Access Policy 15 (IMR15_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR15 Read Access Policy 14 (IMR15_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR15 Read Access Policy 13 (IMR15_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR15 Read Access Policy 12 (IMR15_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR15 Read Access Policy 11 (IMR15_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR15 Read Access Policy 10 (IMR15_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR15 Read Access Policy 9 (IMR15_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR15 Read Access Policy 8 (IMR15_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR15 Read Access Policy 7 (IMR15_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR15 Read Access Policy 6 (IMR15_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR15 Read Access Policy 5 (IMR15_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR15 Read Access Policy 4 (IMR15_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**IMR15 Read Access Policy 3 (IMR15_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR15 Read Access Policy 2 (IMR15_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR15 Read Access Policy 1 (IMR15_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR15 Read Access Policy 0 (IMR15_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR15 region, based on each agent's 6bit encoded SAI value.

5.9.86 IMR15 Write Access Policy (B_CR_BIMR15WAC_0_0_0_MCHBAR)—Offset 6A68h

This register, along with IMR15BASE, IMR15MASK and IMR15RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR15. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR15 Write Access Policy 63 (IMR15_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR15 Write Access Policy 62 (IMR15_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR15 Write Access Policy 61 (IMR15_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR15 Write Access Policy 60 (IMR15_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR15 Write Access Policy 59 (IMR15_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
58	0h RO	**IMR15 Write Access Policy 58 (IMR15_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR15 Write Access Policy 57 (IMR15_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR15 Write Access Policy 56 (IMR15_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR15 Write Access Policy 55 (IMR15_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR15 Write Access Policy 54 (IMR15_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR15 Write Access Policy 53 (IMR15_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR15 Write Access Policy 52 (IMR15_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR15 Write Access Policy 51 (IMR15_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR15 Write Access Policy 50 (IMR15_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR15 Write Access Policy 49 (IMR15_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR15 Write Access Policy 48 (IMR15_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR15 Write Access Policy 47 (IMR15_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR15 Write Access Policy 46 (IMR15_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR15 Write Access Policy 45 (IMR15_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR15 Write Access Policy 44 (IMR15_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
43	0h RW	**IMR15 Write Access Policy 43 (IMR15_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR15 Write Access Policy 42 (IMR15_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR15 Write Access Policy 41 (IMR15_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR15 Write Access Policy 40 (IMR15_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR15 Write Access Policy 39 (IMR15_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR15 Write Access Policy 38 (IMR15_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR15 Write Access Policy 37 (IMR15_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR15 Write Access Policy 36 (IMR15_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR15 Write Access Policy 35 (IMR15_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR15 Write Access Policy 34 (IMR15_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR15 Write Access Policy 33 (IMR15_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR15 Write Access Policy 32 (IMR15_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR15 Write Access Policy 31 (IMR15_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR15 Write Access Policy 30 (IMR15_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR15 Write Access Policy 29 (IMR15_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RW	**IMR15 Write Access Policy 28 (IMR15_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR15 Write Access Policy 27 (IMR15_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR15 Write Access Policy 26 (IMR15_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR15 Write Access Policy 25 (IMR15_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR15 Write Access Policy 24 (IMR15_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR15 Write Access Policy 23 (IMR15_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR15 Write Access Policy 22 (IMR15_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR15 Write Access Policy 21 (IMR15_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR15 Write Access Policy 20 (IMR15_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR15 Write Access Policy 19 (IMR15_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR15 Write Access Policy 18 (IMR15_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR15 Write Access Policy 17 (IMR15_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR15 Write Access Policy 16 (IMR15_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR15 Write Access Policy 15 (IMR15_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR15 Write Access Policy 14 (IMR15_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**IMR15 Write Access Policy 13 (IMR15_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR15 Write Access Policy 12 (IMR15_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR15 Write Access Policy 11 (IMR15_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR15 Write Access Policy 10 (IMR15_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR15 Write Access Policy 9 (IMR15_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR15 Write Access Policy 8 (IMR15_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR15 Write Access Policy 7 (IMR15_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR15 Write Access Policy 6 (IMR15_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR15 Write Access Policy 5 (IMR15_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR15 Write Access Policy 4 (IMR15_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR15 Write Access Policy 3 (IMR15_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR15 Write Access Policy 2 (IMR15_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR15 Write Access Policy 1 (IMR15_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR15 Write Access Policy 0 (IMR15_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR15 region, based on each agent's 6bit encoded SAI value.

5.9.87 IMR16 Base (B_CR_BIMR16BASE_0_0_0_MCHBAR)—Offset 6A70h

This register, along with IMR16MASK, IMR16RAC and IMR16WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR16RAC and IMR16WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR16 Base (IMR16_BASE):** Specifies bits 38:10 of the start address of IMR16 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR16MASK[28:0] applied to bits 38:10 of the incoming address, to determine if an access falls within the IMR16 defined region.

5.9.88 IMR16 Mask (B_CR_BIMR16MASK_0_0_0_MCHBAR)—Offset 6A74h

This register, along with IMR16BASE, IMR16RAC and IMR16WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR16RAC and IMR16WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback data HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester, depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR16 Mask (IMR16_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR16BASE[28:0] value. A match indicates that the incoming address falls within the IMR16 region.

5.9.89 IMR16 Control Policy (B_CR_BIMR16CP_0_0_0_MCHBAR)—Offset 6A78h

This register controls the access policy to the Read Access Policy BIMR16RAC, the Write Access Policy BIMR16WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR16 Control Policy (IMR16_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR16RAC, BIMR16WAC and BIMR16CP registers, based on the value from each agent's 6bit SAI field.

5.9.90 IMR16 Read Access Policy (B_CR_BIMR16RAC_0_0_0_MCHBAR)—Offset 6A80h

This register, along with IMR16BASE, IMR16MASK and IMR16WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR16. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR16 Read Access Policy 63 (IMR16_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR16 Read Access Policy 62 (IMR16_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR16 Read Access Policy 61 (IMR16_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR16 Read Access Policy 60 (IMR16_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR16 Read Access Policy 59 (IMR16_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR16 Read Access Policy 58 (IMR16_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR16 Read Access Policy 57 (IMR16_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR16 Read Access Policy 56 (IMR16_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR16 Read Access Policy 55 (IMR16_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR16 Read Access Policy 54 (IMR16_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
53	0h RO	**IMR16 Read Access Policy 53 (IMR16_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR16 Read Access Policy 52 (IMR16_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR16 Read Access Policy 51 (IMR16_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR16 Read Access Policy 50 (IMR16_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR16 Read Access Policy 49 (IMR16_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR16 Read Access Policy 48 (IMR16_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR16 Read Access Policy 47 (IMR16_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR16 Read Access Policy 46 (IMR16_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR16 Read Access Policy 45 (IMR16_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR16 Read Access Policy 44 (IMR16_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR16 Read Access Policy 43 (IMR16_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR16 Read Access Policy 42 (IMR16_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR16 Read Access Policy 41 (IMR16_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR16 Read Access Policy 40 (IMR16_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR16 Read Access Policy 39 (IMR16_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
38	0h RW	**IMR16 Read Access Policy 38 (IMR16_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR16 Read Access Policy 37 (IMR16_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR16 Read Access Policy 36 (IMR16_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR16 Read Access Policy 35 (IMR16_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR16 Read Access Policy 34 (IMR16_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR16 Read Access Policy 33 (IMR16_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR16 Read Access Policy 32 (IMR16_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR16 Read Access Policy 31 (IMR16_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR16 Read Access Policy 30 (IMR16_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR16 Read Access Policy 29 (IMR16_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR16 Read Access Policy 28 (IMR16_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR16 Read Access Policy 27 (IMR16_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR16 Read Access Policy 26 (IMR16_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR16 Read Access Policy 25 (IMR16_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR16 Read Access Policy 24 (IMR16_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**IMR16 Read Access Policy 23 (IMR16_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR16 Read Access Policy 22 (IMR16_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR16 Read Access Policy 21 (IMR16_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR16 Read Access Policy 20 (IMR16_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR16 Read Access Policy 19 (IMR16_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR16 Read Access Policy 18 (IMR16_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR16 Read Access Policy 17 (IMR16_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR16 Read Access Policy 16 (IMR16_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR16 Read Access Policy 15 (IMR16_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR16 Read Access Policy 14 (IMR16_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR16 Read Access Policy 13 (IMR16_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR16 Read Access Policy 12 (IMR16_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR16 Read Access Policy 11 (IMR16_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR16 Read Access Policy 10 (IMR16_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR16 Read Access Policy 9 (IMR16_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**IMR16 Read Access Policy 8 (IMR16_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR16 Read Access Policy 7 (IMR16_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR16 Read Access Policy 6 (IMR16_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR16 Read Access Policy 5 (IMR16_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR16 Read Access Policy 4 (IMR16_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR16 Read Access Policy 3 (IMR16_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR16 Read Access Policy 2 (IMR16_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR16 Read Access Policy 1 (IMR16_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR16 Read Access Policy 0 (IMR16_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR16 region, based on each agent's 6bit encoded SAI value.

5.9.91 IMR16 Write Access Policy (B_CR_BIMR16WAC_0_0_0_MCHBAR)—Offset 6A88h

This register, along with IMR16BASE, IMR16MASK and IMR16RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR16. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR16 Write Access Policy 63 (IMR16_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR16 Write Access Policy 62 (IMR16_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR16 Write Access Policy 61 (IMR16_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR16 Write Access Policy 60 (IMR16_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR16 Write Access Policy 59 (IMR16_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR16 Write Access Policy 58 (IMR16_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR16 Write Access Policy 57 (IMR16_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR16 Write Access Policy 56 (IMR16_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR16 Write Access Policy 55 (IMR16_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR16 Write Access Policy 54 (IMR16_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR16 Write Access Policy 53 (IMR16_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR16 Write Access Policy 52 (IMR16_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR16 Write Access Policy 51 (IMR16_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR16 Write Access Policy 50 (IMR16_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR16 Write Access Policy 49 (IMR16_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**IMR16 Write Access Policy 48 (IMR16_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR16 Write Access Policy 47 (IMR16_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR16 Write Access Policy 46 (IMR16_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR16 Write Access Policy 45 (IMR16_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR16 Write Access Policy 44 (IMR16_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR16 Write Access Policy 43 (IMR16_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR16 Write Access Policy 42 (IMR16_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR16 Write Access Policy 41 (IMR16_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR16 Write Access Policy 40 (IMR16_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR16 Write Access Policy 39 (IMR16_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR16 Write Access Policy 38 (IMR16_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR16 Write Access Policy 37 (IMR16_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR16 Write Access Policy 36 (IMR16_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR16 Write Access Policy 35 (IMR16_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR16 Write Access Policy 34 (IMR16_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
33	0h RW	**IMR16 Write Access Policy 33 (IMR16_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR16 Write Access Policy 32 (IMR16_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR16 Write Access Policy 31 (IMR16_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR16 Write Access Policy 30 (IMR16_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR16 Write Access Policy 29 (IMR16_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR16 Write Access Policy 28 (IMR16_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR16 Write Access Policy 27 (IMR16_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR16 Write Access Policy 26 (IMR16_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR16 Write Access Policy 25 (IMR16_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR16 Write Access Policy 24 (IMR16_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR16 Write Access Policy 23 (IMR16_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR16 Write Access Policy 22 (IMR16_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR16 Write Access Policy 21 (IMR16_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR16 Write Access Policy 20 (IMR16_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR16 Write Access Policy 19 (IMR16_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**IMR16 Write Access Policy 18 (IMR16_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR16 Write Access Policy 17 (IMR16_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR16 Write Access Policy 16 (IMR16_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR16 Write Access Policy 15 (IMR16_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR16 Write Access Policy 14 (IMR16_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR16 Write Access Policy 13 (IMR16_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR16 Write Access Policy 12 (IMR16_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR16 Write Access Policy 11 (IMR16_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR16 Write Access Policy 10 (IMR16_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR16 Write Access Policy 9 (IMR16_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR16 Write Access Policy 8 (IMR16_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR16 Write Access Policy 7 (IMR16_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR16 Write Access Policy 6 (IMR16_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR16 Write Access Policy 5 (IMR16_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR16 Write Access Policy 4 (IMR16_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**IMR16 Write Access Policy 3 (IMR16_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR16 Write Access Policy 2 (IMR16_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR16 Write Access Policy 1 (IMR16_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR16 Write Access Policy 0 (IMR16_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR16 region, based on each agent's 6bit encoded SAI value.

5.9.92 IMR17 Base (B_CR_BIMR17BASE_0_0_0_MCHBAR)—Offset 6A90h

This register, along with IMR17MASK, IMR17RAC and IMR17WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR17RAC and IMR17WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR17BASE (IMR17_BASE):** Specifies bits 38:10 of the start address of IMR17 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR17MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR17 defined region.

5.9.93 IMR17 Mask (B_CR_BIMR17MASK_0_0_0_MCHBAR)—Offset 6A94h

This register, along with IMR17BASE, IMR17RAC and IMR17WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR17RAC and IMR17WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester, depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR17 Mask (IMR17_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR17BASE[28:0] value. A match indicates that the incoming address falls within the IMR17 region.

5.9.94 IMR17 Control Policy (B_CR_BIMR17CP_0_0_0_MCHBAR)—Offset 6A98h

This register controls the access policy to the Read Access Policy BIMR17RAC, the Write Access Policy BIMR17WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR17 Control Policy (IMR17_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR17RAC, BIMR17WAC and BIMR17CP registers, based on the value from each agent's 6bit SAI field.

5.9.95 IMR17 Read Access Policy (B_CR_BIMR17RAC_0_0_0_MCHBAR)—Offset 6AA0h

This register, along with IMR17BASE, IMR17MASK and IMR17WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR17. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR17 Read Access Policy 63 (IMR17_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR17 Read Access Policy 62 (IMR17_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR17 Read Access Policy 61 (IMR17_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR17 Read Access Policy 60 (IMR17_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR17 Read Access Policy 59 (IMR17_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR17 Read Access Policy 58 (IMR17_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
57	0h RO	**IMR17 Read Access Policy 57 (IMR17_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR17 Read Access Policy 56 (IMR17_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR17 Read Access Policy 55 (IMR17_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR17 Read Access Policy 54 (IMR17_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR17 Read Access Policy 53 (IMR17_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR17 Read Access Policy 52 (IMR17_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR17 Read Access Policy 51 (IMR17_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR17 Read Access Policy 50 (IMR17_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR17 Read Access Policy 49 (IMR17_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR17 Read Access Policy 48 (IMR17_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR17 Read Access Policy 47 (IMR17_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR17 Read Access Policy 46 (IMR17_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR17 Read Access Policy 45 (IMR17_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR17 Read Access Policy 44 (IMR17_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR17 Read Access Policy 43 (IMR17_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
42	0h RW	**IMR17 Read Access Policy 42 (IMR17_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR17 Read Access Policy 41 (IMR17_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR17 Read Access Policy 40 (IMR17_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR17 Read Access Policy 39 (IMR17_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR17 Read Access Policy 38 (IMR17_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR17 Read Access Policy 37 (IMR17_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR17 Read Access Policy 36 (IMR17_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR17 Read Access Policy 35 (IMR17_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR17 Read Access Policy 34 (IMR17_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR17 Read Access Policy 33 (IMR17_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR17 Read Access Policy 32 (IMR17_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR17 Read Access Policy 31 (IMR17_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR17 Read Access Policy 30 (IMR17_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR17 Read Access Policy 29 (IMR17_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR17 Read Access Policy 28 (IMR17_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW	**IMR17 Read Access Policy 27 (IMR17_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR17 Read Access Policy 26 (IMR17_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR17 Read Access Policy 25 (IMR17_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR17 Read Access Policy 24 (IMR17_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR17 Read Access Policy 23 (IMR17_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR17 Read Access Policy 22 (IMR17_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR17 Read Access Policy 21 (IMR17_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR17 Read Access Policy 20 (IMR17_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR17 Read Access Policy 19 (IMR17_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR17 Read Access Policy 18 (IMR17_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR17 Read Access Policy 17 (IMR17_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR17 Read Access Policy 16 (IMR17_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR17 Read Access Policy 15 (IMR17_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR17 Read Access Policy 14 (IMR17_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR17 Read Access Policy 13 (IMR17_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**IMR17 Read Access Policy 12 (IMR17_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR17 Read Access Policy 11 (IMR17_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR17 Read Access Policy 10 (IMR17_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR17 Read Access Policy 9 (IMR17_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR17 Read Access Policy 8 (IMR17_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR17 Read Access Policy 7 (IMR17_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR17 Read Access Policy 6 (IMR17_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR17 Read Access Policy 5 (IMR17_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR17 Read Access Policy 4 (IMR17_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR17 Read Access Policy 3 (IMR17_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR17 Read Access Policy 2 (IMR17_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR17 Read Access Policy 1 (IMR17_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR17 Read Access Policy 0 (IMR17_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR17 region, based on each agent's 6bit encoded SAI value.

5.9.96 IMR17 Write Access Policy (B_CR_BIMR17WAC_0_0_0_MCHBAR)—Offset 6AA8h

This register, along with IMR17BASE, IMR17MASK and IMR17RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with a SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR17. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR17 Write Access Policy 63 (IMR17_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR17 Write Access Policy 62 (IMR17_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR17 Write Access Policy 61 (IMR17_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR17 Write Access Policy 60 (IMR17_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR17 Write Access Policy 59 (IMR17_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR17 Write Access Policy 58 (IMR17_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR17 Write Access Policy 57 (IMR17_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR17 Write Access Policy 56 (IMR17_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR17 Write Access Policy 55 (IMR17_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR17 Write Access Policy 54 (IMR17_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
53	0h RO	**IMR17 Write Access Policy 53 (IMR17_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR17 Write Access Policy 52 (IMR17_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR17 Write Access Policy 51 (IMR17_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR17 Write Access Policy 50 (IMR17_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR17 Write Access Policy 49 (IMR17_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR17 Write Access Policy 48 (IMR17_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR17 Write Access Policy 47 (IMR17_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR17 Write Access Policy 46 (IMR17_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR17 Write Access Policy 45 (IMR17_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR17 Write Access Policy 44 (IMR17_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR17 Write Access Policy 43 (IMR17_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR17 Write Access Policy 42 (IMR17_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR17 Write Access Policy 41 (IMR17_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR17 Write Access Policy 40 (IMR17_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR17 Write Access Policy 39 (IMR17_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
38	0h RW	**IMR17 Write Access Policy 38 (IMR17_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR17 Write Access Policy 37 (IMR17_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR17 Write Access Policy 36 (IMR17_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR17 Write Access Policy 35 (IMR17_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR17 Write Access Policy 34 (IMR17_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR17 Write Access Policy 33 (IMR17_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR17 Write Access Policy 32 (IMR17_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR17 Write Access Policy 31 (IMR17_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR17 Write Access Policy 30 (IMR17_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR17 Write Access Policy 29 (IMR17_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR17 Write Access Policy 28 (IMR17_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR17 Write Access Policy 27 (IMR17_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR17 Write Access Policy 26 (IMR17_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR17 Write Access Policy 25 (IMR17_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR17 Write Access Policy 24 (IMR17_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**IMR17 Write Access Policy 23 (IMR17_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR17 Write Access Policy 22 (IMR17_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR17 Write Access Policy 21 (IMR17_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR17 Write Access Policy 20 (IMR17_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR17 Write Access Policy 19 (IMR17_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR17 Write Access Policy 18 (IMR17_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR17 Write Access Policy 17 (IMR17_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR17 Write Access Policy 16 (IMR17_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR17 Write Access Policy 15 (IMR17_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR17 Write Access Policy 14 (IMR17_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR17 Write Access Policy 13 (IMR17_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR17 Write Access Policy 12 (IMR17_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR17 Write Access Policy 11 (IMR17_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR17 Write Access Policy 10 (IMR17_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR17 Write Access Policy 9 (IMR17_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**IMR17 Write Access Policy 8 (IMR17_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR17 Write Access Policy 7 (IMR17_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR17 Write Access Policy 6 (IMR17_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR17 Write Access Policy 5 (IMR17_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR17 Write Access Policy 4 (IMR17_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR17 Write Access Policy 3 (IMR17_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR17 Write Access Policy 2 (IMR17_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR17 Write Access Policy 1 (IMR17_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR17 Write Access Policy 0 (IMR17_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR17 region, based on each agent's 6bit encoded SAI value.

5.9.97 IMR18 Base (B_CR_BIMR18BASE_0_0_0_MCHBAR)—Offset 6AB0h

This register, along with IMR18MASK, IMR18RAC and IMR18WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR18RAC and IMR18WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:0	0h RW	**Base 0 IMR18 Base (IMR18_BASE):** Specifies bits 38:10 of the start address of IMR18 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR18MASK[28:0] applied to bits 38:10 of the incoming address, to determine if an access falls within the IMR18 defined region.

5.9.98 IMR18 Mask (B_CR_BIMR18MASK_0_0_0_MCHBAR)—Offset 6AB4h

This register, along with IMR18BASE, IMR18RAC and IMR18WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR18RAC and IMR18WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback data HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester depending on the setting of the GT_IWB_EN bit.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR18 Mask (IMR18_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR18BASE[28:0] value. A match indicates that the incoming address falls within the IMR18 region.

5.9.99 IMR18 Control Policy (B_CR_BIMR18CP_0_0_0_MCHBAR)—Offset 6AB8h

This register controls the access policy to the Read Access Policy BIMR18RAC, the Write Access Policy BIMR18WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR18 Control Policy (IMR18_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR18RAC, BIMR18WAC and BIMR18CP registers, based on the value from each agent's 6bit SAI field.

5.9.100 IMR18 Read Access Policy (B_CR_BIMR18RAC_0_0_0_MCHBAR)—Offset 6AC0h

This register, along with IMR18BASE, IMR18MASK and IMR18WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR18. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR18 Read Access Policy 63 (IMR18_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR18 Read Access Policy 62 (IMR18_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR18 Read Access Policy 61 (IMR18_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR18 Read Access Policy 60 (IMR18_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR18 Read Access Policy 59 (IMR18_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR18 Read Access Policy 58 (IMR18_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR18 Read Access Policy 57 (IMR18_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR18 Read Access Policy 56 (IMR18_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR18 Read Access Policy 55 (IMR18_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR18 Read Access Policy 54 (IMR18_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR18 Read Access Policy 53 (IMR18_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR18 Read Access Policy 52 (IMR18_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR18 Read Access Policy 51 (IMR18_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR18 Read Access Policy 50 (IMR18_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR18 Read Access Policy 49 (IMR18_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**IMR18 Read Access Policy 48 (IMR18_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR18 Read Access Policy 47 (IMR18_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR18 Read Access Policy 46 (IMR18_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR18 Read Access Policy 45 (IMR18_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR18 Read Access Policy 44 (IMR18_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR18 Read Access Policy 43 (IMR18_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR18 Read Access Policy 42 (IMR18_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR18 Read Access Policy 41 (IMR18_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR18 Read Access Policy 40 (IMR18_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR18 Read Access Policy 39 (IMR18_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR18 Read Access Policy 38 (IMR18_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR18 Read Access Policy 37 (IMR18_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR18 Read Access Policy 36 (IMR18_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR18 Read Access Policy 35 (IMR18_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR18 Read Access Policy 34 (IMR18_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
33	0h RW	**IMR18 Read Access Policy 33 (IMR18_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR18 Read Access Policy 32 (IMR18_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR18 Read Access Policy 31 (IMR18_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR18 Read Access Policy 30 (IMR18_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR18 Read Access Policy 29 (IMR18_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR18 Read Access Policy 28 (IMR18_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR18 Read Access Policy 27 (IMR18_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR18 Read Access Policy 26 (IMR18_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR18 Read Access Policy 25 (IMR18_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR18 Read Access Policy 24 (IMR18_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR18 Read Access Policy 23 (IMR18_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR18 Read Access Policy 22 (IMR18_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR18 Read Access Policy 21 (IMR18_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR18 Read Access Policy 20 (IMR18_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR18 Read Access Policy 19 (IMR18_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**IMR18 Read Access Policy 18 (IMR18_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR18 Read Access Policy 17 (IMR18_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR18 Read Access Policy 16 (IMR18_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR18 Read Access Policy 15 (IMR18_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR18 Read Access Policy 14 (IMR18_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR18 Read Access Policy 13 (IMR18_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR18 Read Access Policy 12 (IMR18_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR18 Read Access Policy 11 (IMR18_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR18 Read Access Policy 10 (IMR18_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR18 Read Access Policy 9 (IMR18_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR18 Read Access Policy 8 (IMR18_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR18 Read Access Policy 7 (IMR18_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR18 Read Access Policy 6 (IMR18_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR18 Read Access Policy 5 (IMR18_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR18 Read Access Policy 4 (IMR18_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**IMR18 Read Access Policy 3 (IMR18_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR18 Read Access Policy 2 (IMR18_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR18 Read Access Policy 1 (IMR18_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR18 Read Access Policy 0 (IMR18_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR18 region, based on each agent's 6bit encoded SAI value.

5.9.101 IMR18 Write Access Policy (B_CR_BIMR18WAC_0_0_0_MCHBAR)—Offset 6AC8h

This register, along with IMR18BASE, IMR18MASK and IMR18RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR18. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR18_WRITE_POL_63 (IMR18_WRITE_POL_63):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR18_WRITE_POL_62 (IMR18_WRITE_POL_62):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR18_WRITE_POL_61 (IMR18_WRITE_POL_61):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR18_WRITE_POL_60 (IMR18_WRITE_POL_60):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.

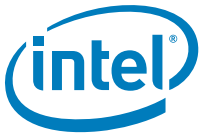
Bit Range	Default & Access	Field Name (ID): Description
59	0h RO	**IMR18_WRITE_POL_59 (IMR18_WRITE_POL_59):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR18_WRITE_POL_58 (IMR18_WRITE_POL_58):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR18_WRITE_POL_57 (IMR18_WRITE_POL_57):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR18_WRITE_POL_56 (IMR18_WRITE_POL_56):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR18_WRITE_POL_55 (IMR18_WRITE_POL_55):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR18_WRITE_POL_54 (IMR18_WRITE_POL_54):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR18_WRITE_POL_53 (IMR18_WRITE_POL_53):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR18_WRITE_POL_52 (IMR18_WRITE_POL_52):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR18_WRITE_POL_51 (IMR18_WRITE_POL_51):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR18_WRITE_POL_50 (IMR18_WRITE_POL_50):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR18_WRITE_POL_49 (IMR18_WRITE_POL_49):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**IMR18_WRITE_POL_48 (IMR18_WRITE_POL_48):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR18_WRITE_POL_47 (IMR18_WRITE_POL_47):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR18_WRITE_POL_46 (IMR18_WRITE_POL_46):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR18_WRITE_POL_45 (IMR18_WRITE_POL_45):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR18_WRITE_POL_44 (IMR18_WRITE_POL_44):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR18_WRITE_POL_43 (IMR18_WRITE_POL_43):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR18_WRITE_POL_42 (IMR18_WRITE_POL_42):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR18_WRITE_POL_41 (IMR18_WRITE_POL_41):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR18_WRITE_POL_40 (IMR18_WRITE_POL_40):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR18_WRITE_POL_39 (IMR18_WRITE_POL_39):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR18_WRITE_POL_38 (IMR18_WRITE_POL_38):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
37	0h RO	**IMR18_WRITE_POL_37 (IMR18_WRITE_POL_37):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR18_WRITE_POL_36 (IMR18_WRITE_POL_36):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR18_WRITE_POL_35 (IMR18_WRITE_POL_35):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR18_WRITE_POL_34 (IMR18_WRITE_POL_34):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR18_WRITE_POL_33 (IMR18_WRITE_POL_33):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR18_WRITE_POL_32 (IMR18_WRITE_POL_32):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR18_WRITE_POL_31 (IMR18_WRITE_POL_31):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR18_WRITE_POL_30 (IMR18_WRITE_POL_30):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR18_WRITE_POL_29 (IMR18_WRITE_POL_29):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR18_WRITE_POL_28 (IMR18_WRITE_POL_28):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR18_WRITE_POL_27 (IMR18_WRITE_POL_27):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
26	0h RW	**IMR18_WRITE_POL_26 (IMR18_WRITE_POL_26):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR18_WRITE_POL_25 (IMR18_WRITE_POL_25):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR18_WRITE_POL_24 (IMR18_WRITE_POL_24):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR18_WRITE_POL_23 (IMR18_WRITE_POL_23):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR18_WRITE_POL_22 (IMR18_WRITE_POL_22):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR18_WRITE_POL_21 (IMR18_WRITE_POL_21):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR18_WRITE_POL_20 (IMR18_WRITE_POL_20):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR18_WRITE_POL_19 (IMR18_WRITE_POL_19):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR18_WRITE_POL_18 (IMR18_WRITE_POL_18):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR18_WRITE_POL_17 (IMR18_WRITE_POL_17):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR18_WRITE_POL_16 (IMR18_WRITE_POL_16):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**IMR18_WRITE_POL_15 (IMR18_WRITE_POL_15):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR18_WRITE_POL_14 (IMR18_WRITE_POL_14):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR18_WRITE_POL_13 (IMR18_WRITE_POL_13):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR18_WRITE_POL_12 (IMR18_WRITE_POL_12):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR18_WRITE_POL_11 (IMR18_WRITE_POL_11):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR18_WRITE_POL_10 (IMR18_WRITE_POL_10):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR18_WRITE_POL_9 (IMR18_WRITE_POL_9):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR18_WRITE_POL_8 (IMR18_WRITE_POL_8):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR18_WRITE_POL_7 (IMR18_WRITE_POL_7):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR18_WRITE_POL_6 (IMR18_WRITE_POL_6):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR18_WRITE_POL_5 (IMR18_WRITE_POL_5):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.



Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**IMR18_WRITE_POL_4 (IMR18_WRITE_POL_4):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR18_WRITE_POL_3 (IMR18_WRITE_POL_3):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR18_WRITE_POL_2 (IMR18_WRITE_POL_2):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR18_WRITE_POL_1 (IMR18_WRITE_POL_1):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR18_WRITE_POL_0 (IMR18_WRITE_POL_0):** B-Unit IMR18 Write Access Policy: Bit vector used to determine which agents are allowed write access to the IMR18 region, based on each agent's 6bit encoded SAI value.

5.9.102 IMR19 Base (B_CR_BIMR19BASE_0_0_0_MCHBAR)—Offset 6AD0h

This register, along with IMR19MASK, IMR19RAC and IMR19WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR19RAC and IMR19WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the IMR region.
30	0h RW	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents.
29	0h RO	**Reserved (RESERVED_1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28:0	0h RW	**Base 0 IMR19 Base (IMR19_BASE):** Specifies bits 38:10 of the start address of IMR19 region. IMR region size must be a strict power of two, at least 1KB, and naturally aligned to the size. These bits are compared with the result of the IMR19MASK[28:0] applied to bits 38:10 of the incoming address to determine if an access falls within the IMR19 defined region.

5.9.103 IMR19 Mask (B_CR_BIMR19MASK_0_0_0_MCHBAR)—Offset 6AD4h

This register, along with IMR19BASE, IMR19RAC and IMR19WAC, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When an agent sends a request to the B-Unit, whether snooped or not, an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation if the agent's SAI field does not specify the correct Policy. The IMR's Policy is configured by the IMR19RAC and IMR19WAC registers.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback data HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester depending on the setting of the IA_IWB_EN bit.
30	0h RW	**Asset Classification AC[1]: IA Implicit WB Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_0):** Reserved.
28:0	0h RW	**Mask 0 IMR19 Mask (IMR19_MASK):** These bits are ANDed with bits 38:10 of the incoming address to determine if the combined result matches the IMR19BASE[28:0] value. A match indicates that the incoming address falls within the IMR19 region.

5.9.104 IMR19 Control Policy (B_CR_BIMR19CP_0_0_0_MCHBAR)—Offset 6AD8h

This register controls the access policy to the Read Access Policy BIMR19RAC, the Write Access Policy BIMR19WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**IMR19 Control Policy (IMR19_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BIMR19RAC, BIMR19WAC, BIMR19CP registers, based on the value from each agent's 6bit SAI field.

5.9.105 IMR19 Read Access Policy (B_CR_BIMR19RAC_0_0_0_MCHBAR)—Offset 6AE0h

This register, along with IMR19BASE, IMR19MASK and IMR19WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR19. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR19 Read Access Policy 63 (IMR19_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR19 Read Access Policy 62 (IMR19_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR19 Read Access Policy 61 (IMR19_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
60	0h RO	**IMR19 Read Access Policy 60 (IMR19_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR19 Read Access Policy 59 (IMR19_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR19 Read Access Policy 58 (IMR19_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR19 Read Access Policy 57 (IMR19_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR19 Read Access Policy 56 (IMR19_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
55	0h RW	**IMR19 Read Access Policy 55 (IMR19_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR19 Read Access Policy 54 (IMR19_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR19 Read Access Policy 53 (IMR19_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR19 Read Access Policy 52 (IMR19_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR19 Read Access Policy 51 (IMR19_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR19 Read Access Policy 50 (IMR19_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR19 Read Access Policy 49 (IMR19_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR19 Read Access Policy 48 (IMR19_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR19 Read Access Policy 47 (IMR19_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR19 Read Access Policy 46 (IMR19_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
45	0h RO	**IMR19 Read Access Policy 45 (IMR19_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR19 Read Access Policy 44 (IMR19_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR19 Read Access Policy 43 (IMR19_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR19 Read Access Policy 42 (IMR19_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR19 Read Access Policy 41 (IMR19_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
40	0h RW	**IMR19 Read Access Policy 40 (IMR19_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR19 Read Access Policy 39 (IMR19_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR19 Read Access Policy 38 (IMR19_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR19 Read Access Policy 37 (IMR19_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR19 Read Access Policy 36 (IMR19_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR19 Read Access Policy 35 (IMR19_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR19 Read Access Policy 34 (IMR19_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR19 Read Access Policy 33 (IMR19_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR19 Read Access Policy 32 (IMR19_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR19 Read Access Policy 31 (IMR19_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW	**IMR19 Read Access Policy 30 (IMR19_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR19 Read Access Policy 29 (IMR19_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR19 Read Access Policy 28 (IMR19_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR19 Read Access Policy 27 (IMR19_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR19 Read Access Policy 26 (IMR19_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
25	0h RW	**IMR19 Read Access Policy 25 (IMR19_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR19 Read Access Policy 24 (IMR19_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR19 Read Access Policy 23 (IMR19_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR19 Read Access Policy 22 (IMR19_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR19 Read Access Policy 21 (IMR19_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR19 Read Access Policy 20 (IMR19_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR19 Read Access Policy 19 (IMR19_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR19 Read Access Policy 18 (IMR19_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR19 Read Access Policy 17 (IMR19_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR19 Read Access Policy 16 (IMR19_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**IMR19 Read Access Policy 15 (IMR19_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR19 Read Access Policy 14 (IMR19_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR19 Read Access Policy 13 (IMR19_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR19 Read Access Policy 12 (IMR19_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR19 Read Access Policy 11 (IMR19_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
10	0h RO	**IMR19 Read Access Policy 10 (IMR19_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR19 Read Access Policy 9 (IMR19_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR19 Read Access Policy 8 (IMR19_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR19 Read Access Policy 7 (IMR19_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR19 Read Access Policy 6 (IMR19_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR19 Read Access Policy 5 (IMR19_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR19 Read Access Policy 4 (IMR19_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR19 Read Access Policy 3 (IMR19_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR19 Read Access Policy 2 (IMR19_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR19 Read Access Policy 1 (IMR19_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**IMR19 Read Access Policy 0 (IMR19_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the IMR19 region, based on each agent's 6bit encoded SAI value.

5.9.106 IMR19 Write Access Policy (B_CR_BIMR19WAC_0_0_0_MCHBAR)—Offset 6AE8h

This register, along with IMR19BASE, IMR19MASK and IMR19RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to IMR19. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**IMR19 Write Access Policy 63 (IMR19_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
62	0h RO	**IMR19 Write Access Policy 62 (IMR19_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
61	0h RO	**IMR19 Write Access Policy 61 (IMR19_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
60	0h RO	**IMR19 Write Access Policy 60 (IMR19_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
59	0h RO	**IMR19 Write Access Policy 59 (IMR19_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
58	0h RO	**IMR19 Write Access Policy 58 (IMR19_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
57	0h RO	**IMR19 Write Access Policy 57 (IMR19_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
56	0h RW	**IMR19 Write Access Policy 56 (IMR19_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
55	0h RW	**IMR19 Write Access Policy 55 (IMR19_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
54	0h RW	**IMR19 Write Access Policy 54 (IMR19_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
53	0h RO	**IMR19 Write Access Policy 53 (IMR19_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
52	0h RO	**IMR19 Write Access Policy 52 (IMR19_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
51	0h RO	**IMR19 Write Access Policy 51 (IMR19_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
50	0h RW	**IMR19 Write Access Policy 50 (IMR19_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
49	0h RW	**IMR19 Write Access Policy 49 (IMR19_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
48	0h RW	**IMR19 Write Access Policy 48 (IMR19_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
47	0h RO	**IMR19 Write Access Policy 47 (IMR19_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
46	0h RO	**IMR19 Write Access Policy 46 (IMR19_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
45	0h RO	**IMR19 Write Access Policy 45 (IMR19_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
44	0h RW	**IMR19 Write Access Policy 44 (IMR19_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
43	0h RW	**IMR19 Write Access Policy 43 (IMR19_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
42	0h RW	**IMR19 Write Access Policy 42 (IMR19_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
41	0h RW	**IMR19 Write Access Policy 41 (IMR19_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
40	0h RW	**IMR19 Write Access Policy 40 (IMR19_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
39	0h RO	**IMR19 Write Access Policy 39 (IMR19_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
38	0h RW	**IMR19 Write Access Policy 38 (IMR19_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
37	0h RO	**IMR19 Write Access Policy 37 (IMR19_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
36	0h RW	**IMR19 Write Access Policy 36 (IMR19_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
35	0h RO	**IMR19 Write Access Policy 35 (IMR19_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
34	0h RW	**IMR19 Write Access Policy 34 (IMR19_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
33	0h RW	**IMR19 Write Access Policy 33 (IMR19_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
32	0h RW	**IMR19 Write Access Policy 32 (IMR19_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
31	0h RO	**IMR19 Write Access Policy 31 (IMR19_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
30	0h RW	**IMR19 Write Access Policy 30 (IMR19_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
29	0h RW	**IMR19 Write Access Policy 29 (IMR19_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
28	0h RW	**IMR19 Write Access Policy 28 (IMR19_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
27	0h RW	**IMR19 Write Access Policy 27 (IMR19_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
26	0h RW	**IMR19 Write Access Policy 26 (IMR19_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW	**IMR19 Write Access Policy 25 (IMR19_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
24	0h RW	**IMR19 Write Access Policy 24 (IMR19_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
23	0h RO	**IMR19 Write Access Policy 23 (IMR19_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
22	0h RO	**IMR19 Write Access Policy 22 (IMR19_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
21	0h RW	**IMR19 Write Access Policy 21 (IMR19_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
20	0h RO	**IMR19 Write Access Policy 20 (IMR19_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
19	0h RO	**IMR19 Write Access Policy 19 (IMR19_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
18	0h RO	**IMR19 Write Access Policy 18 (IMR19_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
17	0h RW	**IMR19 Write Access Policy 17 (IMR19_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
16	0h RW	**IMR19 Write Access Policy 16 (IMR19_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
15	0h RO	**IMR19 Write Access Policy 15 (IMR19_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
14	0h RO	**IMR19 Write Access Policy 14 (IMR19_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
13	0h RW	**IMR19 Write Access Policy 13 (IMR19_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
12	0h RW	**IMR19 Write Access Policy 12 (IMR19_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
11	0h RO	**IMR19 Write Access Policy 11 (IMR19_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO	**IMR19 Write Access Policy 10 (IMR19_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
9	0h RO	**IMR19 Write Access Policy 9 (IMR19_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
8	0h RW	**IMR19 Write Access Policy 8 (IMR19_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
7	0h RO	**IMR19 Write Access Policy 7 (IMR19_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
6	0h RO	**IMR19 Write Access Policy 6 (IMR19_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
5	0h RW	**IMR19 Write Access Policy 5 (IMR19_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
4	0h RW	**IMR19 Write Access Policy 4 (IMR19_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
3	0h RW	**IMR19 Write Access Policy 3 (IMR19_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
2	0h RW	**IMR19 Write Access Policy 2 (IMR19_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
1	0h RW	**IMR19 Write Access Policy 1 (IMR19_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.
0	0h RW	**IMR19 Write Access Policy 0 (IMR19_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the IMR19 region, based on each agent's 6bit encoded SAI value.

5.9.107 MOT Out Base (B_CR_MOT_OUT_BASE_0_0_0_MCHBAR)—Offset 6AF0h

This register contains the value of the start address of the MOT debug data region. The smallest reserved region for MOT debug data, if enabled, is 16MB. The MOT region must be power of two sized and naturally aligned to its size. The MOT region is evenly distributed between the slices and interleaved on a 4K granularity. When generating addresses, B-Unit MOT H/W within each slice ensures that the addresses it generates are within the region mapped to that slice.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**IMR Enable (IMR_EN):** Enables access checking for the MOT region. Note: this does not enable MOT itself, but merely enables access control checks for transactions that attempt to access the MOT buffer.
30	0h RO	**Asset Classification AC[0]: Trace Enable (TR_EN):** Enables snooping of transactions to the IMR region by tracing agents such as MOT. Reserved and set to 0 for the MOT region, since otherwise this would enable recursive tracing and corrupt MOT buffer.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:14	0h RW	**MOT_OUT Base (MOT_OUT_BASE):** Specifies bits 38:24 of the start address of the MOT memory region. Region size must be a strict power of two, at least 16MB, and naturally aligned to the size. These bits are compared with the result of the MOT_OUT_MASK[28:14] applied to bits 38:24 of the incoming address to determine if an access falls within the MOT region.
13:0	0h RO	**Reserved (RESERVED_0):** Reserved.

5.9.108 MOT Out Mask (B_CR_MOT_OUT_MASK_0_0_0_MCHBAR)—Offset 6AF4h

This register specifies the size of the MOT region. If a request address [38:24] ANDed with MOT_OUT_MASK[28:14] matches the MOT_OUT_BASE[38:24], then the request falls within the MOT_OUT region.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Asset Classification AC[2]: GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester, depending on the setting of the IA_IWB_EN bit.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW	**Asset Classification AC[1]: IA Implicit WB Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester, depending on the setting of the GT_IWB_EN bit.
29	0h RO	**Reserved (RESERVED_1):** Reserved.
28:14	0h RW	**MOT Out Mask (MOT_OUT_MASK):** Specifies the size of the MOT region. If Request Address [38:24] ANDed with MOT_OUT_MASK[28:14] matches the MOT_OUT_BASE[28:14] then the request falls within the MOT_OUT region.
13:0	0h RO	**Reserved (RESERVED_0):** Reserved.

5.9.109 MOT Buffer Control Policy (B_CR_BMOT_BUF_CP_0_0_0_MCHBAR)—Offset 6AF8h

This register controls the access policy to BMOT_BUF_RAC, BMOT_BUF_WAC, and, self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010 202h RW	**MOT Buffer Control Policy (MOT_BUF_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BMOT_BUF_RAC, BMOT_BUF_WAC and BMOT_BUF_CP registers, based on the value from each agent's 6bit SAI field.

5.9.110 MOT Buffer Read Access Policy (B_CR_BMOT_BUF_RAC_0_0_0_MCHBAR)—Offset 6B00h

This register, along with MOTBASE, MOTMASK and MOT_BUF_WAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to MOT. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 60010017h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**MOT Read Access Policy 63 (MOT_BUF_READ_POL_63):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
62	0h RO	**MOT Read Access Policy 62 (MOT_BUF_READ_POL_62):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
61	0h RO	**MOT Read Access Policy 61 (MOT_BUF_READ_POL_61):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
60	0h RO	**MOT Read Access Policy 60 (MOT_BUF_READ_POL_60):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
59	0h RO	**MOT Read Access Policy 59 (MOT_BUF_READ_POL_59):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
58	0h RO	**MOT Read Access Policy 58 (MOT_BUF_READ_POL_58):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
57	0h RO	**MOT Read Access Policy 57 (MOT_BUF_READ_POL_57):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
56	0h RW	**MOT Read Access Policy 56 (MOT_BUF_READ_POL_56):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
55	0h RW	**MOT Read Access Policy 55 (MOT_BUF_READ_POL_55):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
54	0h RW	**MOT Read Access Policy 54 (MOT_BUF_READ_POL_54):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
53	0h RO	**MOT Read Access Policy 53 (MOT_BUF_READ_POL_53):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
52	0h RO	**MOT Read Access Policy 52 (MOT_BUF_READ_POL_52):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
51	0h RO	**MOT Read Access Policy 51 (MOT_BUF_READ_POL_51):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
50	0h RW	**MOT Read Access Policy 50 (MOT_BUF_READ_POL_50):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
49	0h RW	**MOT Read Access Policy 49 (MOT_BUF_READ_POL_49):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
48	0h RW	**MOT Read Access Policy 48 (MOT_BUF_READ_POL_48):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
47	0h RO	**MOT Read Access Policy 47 (MOT_BUF_READ_POL_47):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
46	0h RO	**MOT Read Access Policy 46 (MOT_BUF_READ_POL_46):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
45	0h RO	**MOT Read Access Policy 45 (MOT_BUF_READ_POL_45):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
44	0h RW	**MOT Read Access Policy 44 (MOT_BUF_READ_POL_44):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
43	0h RW	**MOT Read Access Policy 43 (MOT_BUF_READ_POL_43):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
42	0h RW	**MOT Read Access Policy 42 (MOT_BUF_READ_POL_42):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
41	0h RW	**MOT Read Access Policy 41 (MOT_BUF_READ_POL_41):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
40	0h RW	**MOT Read Access Policy 40 (MOT_BUF_READ_POL_40):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
39	0h RO	**MOT Read Access Policy 39 (MOT_BUF_READ_POL_39):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
38	0h RW	**MOT Read Access Policy 38 (MOT_BUF_READ_POL_38):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
37	0h RO	**MOT Read Access Policy 37 (MOT_BUF_READ_POL_37):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
36	0h RW	**MOT Read Access Policy 36 (MOT_BUF_READ_POL_36):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
35	0h RO	**MOT Read Access Policy 35 (MOT_BUF_READ_POL_35):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
34	0h RW	**MOT Read Access Policy 34 (MOT_BUF_READ_POL_34):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
33	0h RW	**MOT Read Access Policy 33 (MOT_BUF_READ_POL_33):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
32	0h RW	**MOT Read Access Policy 32 (MOT_BUF_READ_POL_32):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
31	0h RO	**MOT Read Access Policy 31 (MOT_BUF_READ_POL_31):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
30	1h RW	**MOT Read Access Policy 30 (MOT_BUF_READ_POL_30):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
29	1h RW	**MOT Read Access Policy 29 (MOT_BUF_READ_POL_29):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
28	0h RW	**MOT Read Access Policy 28 (MOT_BUF_READ_POL_28):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
27	0h RW	**MOT Read Access Policy 27 (MOT_BUF_READ_POL_27):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
26	0h RW	**MOT Read Access Policy 26 (MOT_BUF_READ_POL_26):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
25	0h RW	**MOT Read Access Policy 25 (MOT_BUF_READ_POL_25):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
24	0h RW	**MOT Read Access Policy 24 (MOT_BUF_READ_POL_24):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
23	0h RO	**MOT Read Access Policy 23 (MOT_BUF_READ_POL_23):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
22	0h RO	**MOT Read Access Policy 22 (MOT_BUF_READ_POL_22):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
21	0h RW	**MOT Read Access Policy 21 (MOT_BUF_READ_POL_21):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**MOT Read Access Policy 20 (MOT_BUF_READ_POL_20):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
19	0h RO	**MOT Read Access Policy 19 (MOT_BUF_READ_POL_19):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
18	0h RO	**MOT Read Access Policy 18 (MOT_BUF_READ_POL_18):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
17	0h RW	**MOT Read Access Policy 17 (MOT_BUF_READ_POL_17):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
16	1h RW	**MOT Read Access Policy 16 (MOT_BUF_READ_POL_16):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
15	0h RO	**MOT Read Access Policy 15 (MOT_BUF_READ_POL_15):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
14	0h RO	**MOT Read Access Policy 14 (MOT_BUF_READ_POL_14):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
13	0h RW	**MOT Read Access Policy 13 (MOT_BUF_READ_POL_13):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
12	0h RW	**MOT Read Access Policy 12 (MOT_BUF_READ_POL_12):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
11	0h RO	**MOT Read Access Policy 11 (MOT_BUF_READ_POL_11):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
10	0h RO	**MOT Read Access Policy 10 (MOT_BUF_READ_POL_10):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
9	0h RO	**MOT Read Access Policy 9 (MOT_BUF_READ_POL_9):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
8	0h RW	**MOT Read Access Policy 8 (MOT_BUF_READ_POL_8):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
7	0h RO	**MOT Read Access Policy 7 (MOT_BUF_READ_POL_7):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
6	0h RO	**MOT Read Access Policy 6 (MOT_BUF_READ_POL_6):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**MOT Read Access Policy 5 (MOT_BUF_READ_POL_5):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
4	1h RW	**MOT Read Access Policy 4 (MOT_BUF_READ_POL_4):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
3	0h RW	**MOT Read Access Policy 3 (MOT_BUF_READ_POL_3):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
2	1h RW	**MOT Read Access Policy 2 (MOT_BUF_READ_POL_2):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
1	1h RW	**MOT Read Access Policy 1 (MOT_BUF_READ_POL_1):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.
0	1h RW	**MOT Read Access Policy 0 (MOT_BUF_READ_POL_0):** Bit vector used to determine which agents are allowed read access to the MOT region, based on each agent's 6bit encoded SAI value.

5.9.111 MOT Buffer Write Access Policy (B_CR_BMOT_BUF_WAC_0_0_0_MCHBAR)—Offset 6B08h

This register, along with MOTBASE, MOTMASK and MOT_BUF_RAC, defines an isolated region of memory that can be masked to prohibit certain agents from accessing memory. It is programmed with an SAI Policy that indicates which agents in the system are allowed to perform read operations to MOT. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

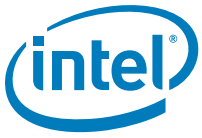
Default: 60010000h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**MOT Write Access Policy 63 (MOT_BUF_WRITE_POL_63):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
62	0h RO	**MOT Write Access Policy 62 (MOT_BUF_WRITE_POL_62):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
61	0h RO	**MOT Write Access Policy 61 (MOT_BUF_WRITE_POL_61):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
60	0h RO	**MOT Write Access Policy 60 (MOT_BUF_WRITE_POL_60):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
59	0h RO	**MOT Write Access Policy 59 (MOT_BUF_WRITE_POL_59):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
58	0h RO	**MOT Write Access Policy 58 (MOT_BUF_WRITE_POL_58):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
57	0h RO	**MOT Write Access Policy 57 (MOT_BUF_WRITE_POL_57):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
56	0h RW	**MOT Write Access Policy 56 (MOT_BUF_WRITE_POL_56):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
55	0h RW	**MOT Write Access Policy 55 (MOT_BUF_WRITE_POL_55):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
54	0h RW	**MOT Write Access Policy 54 (MOT_BUF_WRITE_POL_54):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
53	0h RO	**MOT Write Access Policy 53 (MOT_BUF_WRITE_POL_53):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
52	0h RO	**MOT Write Access Policy 52 (MOT_BUF_WRITE_POL_52):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
51	0h RO	**MOT Write Access Policy 51 (MOT_BUF_WRITE_POL_51):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
50	0h RW	**MOT Write Access Policy 50 (MOT_BUF_WRITE_POL_50):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
49	0h RW	**MOT Write Access Policy 49 (MOT_BUF_WRITE_POL_49):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
48	0h RW	**MOT Write Access Policy 48 (MOT_BUF_WRITE_POL_48):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
47	0h RO	**MOT Write Access Policy 47 (MOT_BUF_WRITE_POL_47):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
46	0h RO	**MOT Write Access Policy 46 (MOT_BUF_WRITE_POL_46):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
45	0h RO	**MOT Write Access Policy 45 (MOT_BUF_WRITE_POL_45):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
44	0h RW	**MOT Write Access Policy 44 (MOT_BUF_WRITE_POL_44):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
43	0h RW	**MOT Write Access Policy 43 (MOT_BUF_WRITE_POL_43):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
42	0h RW	**MOT Write Access Policy 42 (MOT_BUF_WRITE_POL_42):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
41	0h RW	**MOT Write Access Policy 41 (MOT_BUF_WRITE_POL_41):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
40	0h RW	**MOT Write Access Policy 40 (MOT_BUF_WRITE_POL_40):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
39	0h RO	**MOT Write Access Policy 39 (MOT_BUF_WRITE_POL_39):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
38	0h RW	**MOT Write Access Policy 38 (MOT_BUF_WRITE_POL_38):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
37	0h RO	**MOT Write Access Policy 37 (MOT_BUF_WRITE_POL_37):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
36	0h RW	**MOT Write Access Policy 36 (MOT_BUF_WRITE_POL_36):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
35	0h RO	**MOT Write Access Policy 35 (MOT_BUF_WRITE_POL_35):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
34	0h RW	**MOT Write Access Policy 34 (MOT_BUF_WRITE_POL_34):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
33	0h RW	**MOT Write Access Policy 33 (MOT_BUF_WRITE_POL_33):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
32	0h RW	**MOT Write Access Policy 32 (MOT_BUF_WRITE_POL_32):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
31	0h RO	**MOT Write Access Policy 31 (MOT_BUF_WRITE_POL_31):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
30	1h RW	**MOT Write Access Policy 30 (MOT_BUF_WRITE_POL_30):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
29	1h RW	**MOT Write Access Policy 29 (MOT_BUF_WRITE_POL_29):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.



Bit Range	Default & Access	Field Name (ID): Description
28	0h RW	**MOT Write Access Policy 28 (MOT_BUF_WRITE_POL_28):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
27	0h RW	**MOT Write Access Policy 27 (MOT_BUF_WRITE_POL_27):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
26	0h RW	**MOT Write Access Policy 26 (MOT_BUF_WRITE_POL_26):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
25	0h RW	**MOT Write Access Policy 25 (MOT_BUF_WRITE_POL_25):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
24	0h RW	**MOT Write Access Policy 24 (MOT_BUF_WRITE_POL_24):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
23	0h RO	**MOT Write Access Policy 23 (MOT_BUF_WRITE_POL_23):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
22	0h RO	**MOT Write Access Policy 22 (MOT_BUF_WRITE_POL_22):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
21	0h RW	**MOT Write Access Policy 21 (MOT_BUF_WRITE_POL_21):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
20	0h RO	**MOT Write Access Policy 20 (MOT_BUF_WRITE_POL_20):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
19	0h RO	**MOT Write Access Policy 19 (MOT_BUF_WRITE_POL_19):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
18	0h RO	**MOT Write Access Policy 18 (MOT_BUF_WRITE_POL_18):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**MOT Write Access Policy 17 (MOT_BUF_WRITE_POL_17):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
16	1h RW	**MOT Write Access Policy 16 (MOT_BUF_WRITE_POL_16):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
15	0h RO	**MOT Write Access Policy 15 (MOT_BUF_WRITE_POL_15):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
14	0h RO	**MOT Write Access Policy 14 (MOT_BUF_WRITE_POL_14):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
13	0h RW	**MOT Write Access Policy 13 (MOT_BUF_WRITE_POL_13):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
12	0h RW	**MOT Write Access Policy 12 (MOT_BUF_WRITE_POL_12):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
11	0h RO	**MOT Write Access Policy 11 (MOT_BUF_WRITE_POL_11):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
10	0h RO	**MOT Write Access Policy 10 (MOT_BUF_WRITE_POL_10):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
9	0h RO	**MOT Write Access Policy 9 (MOT_BUF_WRITE_POL_9):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
8	0h RW	**MOT Write Access Policy 8 (MOT_BUF_WRITE_POL_8):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
7	0h RO	**MOT Write Access Policy 7 (MOT_BUF_WRITE_POL_7):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
6	0h RO	**MOT Write Access Policy 6 (MOT_BUF_WRITE_POL_6):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**MOT Write Access Policy 5 (MOT_BUF_WRITE_POL_5):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
4	0h RW	**MOT Write Access Policy 4 (MOT_BUF_WRITE_POL_4):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
3	0h RW	**MOT Write Access Policy 3 (MOT_BUF_WRITE_POL_3):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
2	0h RW	**MOT Write Access Policy 2 (MOT_BUF_WRITE_POL_2):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
1	0h RW	**MOT Write Access Policy 1 (MOT_BUF_WRITE_POL_1):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.
0	0h RW	**MOT Write Access Policy 0 (MOT_BUF_WRITE_POL_0):** Bit vector used to determine which agents are allowed write access to the MOT region, based on each agent's 6bit encoded SAI value.

5.9.112 IMR Global BM Control Policy (B_CR_BIMRGLOBAL_BM_CP_0_0_0_MCHBAR)—Offset 6B10h

Defines the policy register that specifies who is allowed write access to BIMRGLOBAL_BM_WAC register.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**BM Control Policy (BM_CTRL_POL):** Bit vector used to determine which agents are allowed write access to BIMRGLOBAL_BM_WAC, based on each agent's 6bit encoded SAI value.

5.9.113 IMR Global BM Read Access Control (B_CR_BIMRGLOBAL_BM_RAC_0_0_0_MCHBAR)—Offset 6B18h

Defines the policy register that specifies who is allowed to read the BASE/MASK registers for IMR0-IMR15. This single common policy register protects reads to all base/mask registers.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: FFFFFFFFFFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:0	FFFFFFFFFFFFFFFFh RO	**BM Read Access Policy (BM_READ_POL):** Bit vector used to determine which agents are allowed read access to all IMRxBASE and IMRxMASK registers, based on each agent's 6bit encoded SAI value.

5.9.114 IMR Global BM Write Access Policy (B_CR_BIMRGLOBAL_BM_WAC_0_0_0_MCHBAR)—Offset 6B20h

Defines the policy register that specifies who is allowed to overwrite the BASE/MASK registers for IMR0-IMR15. This single common policy register protects writes to all base/mask registers.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**BM Write Access Policy (BM_WRITE_POL):** Bit vector used to determine which agents are allowed write access to all IMRxBASE and IMRxMASK registers, based on each agent's 6bit encoded SAI value.

5.9.115 Graphics Stolen Memory Control Policy (B_CR_BGSMCP_0_0_0_MCHBAR)—Offset 6B28h

This register controls the access policy to the Read Access Policy BGSMRAC, Write Access Policy BGSMWAC and self-referentially, to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**GSM Control Policy (GSM_CTRL_POL):** Bit vector used to determine which agents are allowed access to the BGSMRAC, BGSMWAC and BGSMCP registers, based on the value from each agent's 6bit SAI field.

5.9.116 GSM Read Access Policy (B_CR_BGSMRAC_0_0_0_MCHBAR)—Offset 6B30h

This register configures the Read Access Policy to the memory range from BGSM to TOLUD1. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 100060010100h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**SMM Read Access Policy 63 (GSM_SAI_POL_63):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
62	0h RO	**SMM Read Access Policy 62 (GSM_SAI_POL_62):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
61	0h RO	**SMM Read Access Policy 61 (GSM_SAI_POL_61):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
60	0h RO	**SMM Read Access Policy 60 (GSM_SAI_POL_60):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
59	0h RO	**SMM Read Access Policy 59 (GSM_SAI_POL_59):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
58	0h RO	**SMM Read Access Policy 58 (GSM_SAI_POL_58):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
57	0h RO	**SMM Read Access Policy 57 (GSM_SAI_POL_57):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
56	0h RW	**SMM Read Access Policy 56 (GSM_SAI_POL_56):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
55	0h RW	**SMM Read Access Policy 55 (GSM_SAI_POL_55):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
54	0h RW	**SMM Read Access Policy 54 (GSM_SAI_POL_54):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
53	0h RO	**SMM Read Access Policy 53 (GSM_SAI_POL_53):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
52	0h RO	**SMM Read Access Policy 52 (GSM_SAI_POL_52):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
51	0h RO	**SMM Read Access Policy 51 (GSM_SAI_POL_51):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
50	0h RW	**SMM Read Access Policy 50 (GSM_SAI_POL_50):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
49	0h RW	**SMM Read Access Policy 49 (GSM_SAI_POL_49):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
48	0h RW	**SMM Read Access Policy 48 (GSM_SAI_POL_48):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
47	0h RO	**SMM Read Access Policy 47 (GSM_SAI_POL_47):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
46	0h RO	**SMM Read Access Policy 46 (GSM_SAI_POL_46):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
45	0h RO	**SMM Read Access Policy 45 (GSM_SAI_POL_45):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
44	1h RW	**SMM Read Access Policy 44 (GSM_SAI_POL_44):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
43	0h RW	**SMM Read Access Policy 43 (GSM_SAI_POL_43):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
42	0h RW	**SMM Read Access Policy 42 (GSM_SAI_POL_42):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
41	0h RW	**SMM Read Access Policy 41 (GSM_SAI_POL_41):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
40	0h RW	**SMM Read Access Policy 40 (GSM_SAI_POL_40):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
39	0h RO	**SMM Read Access Policy 39 (GSM_SAI_POL_39):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
38	0h RW	**SMM Read Access Policy 38 (GSM_SAI_POL_38):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
37	0h RO	**SMM Read Access Policy 37 (GSM_SAI_POL_37):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
36	0h RW	**SMM Read Access Policy 36 (GSM_SAI_POL_36):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
35	0h RO	**SMM Read Access Policy 35 (GSM_SAI_POL_35):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
34	0h RW	**SMM Read Access Policy 34 (GSM_SAI_POL_34):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
33	0h RW	**SMM Read Access Policy 33 (GSM_SAI_POL_33):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
32	0h RW	**SMM Read Access Policy 32 (GSM_SAI_POL_32):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
31	0h RO	**SMM Read Access Policy 31 (GSM_SAI_POL_31):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
30	1h RW	**SMM Read Access Policy 30 (GSM_SAI_POL_30):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
29	1h RW	**SMM Read Access Policy 29 (GSM_SAI_POL_29):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
28	0h RW	**SMM Read Access Policy 28 (GSM_SAI_POL_28):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
27	0h RW	**SMM Read Access Policy 27 (GSM_SAI_POL_27):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
26	0h RW	**SMM Read Access Policy 26 (GSM_SAI_POL_26):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
25	0h RW	**SMM Read Access Policy 25 (GSM_SAI_POL_25):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**SMM Read Access Policy 24 (GSM_SAI_POL_24):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
23	0h RO	**SMM Read Access Policy 23 (GSM_SAI_POL_23):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
22	0h RO	**SMM Read Access Policy 22 (GSM_SAI_POL_22):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
21	0h RW	**SMM Read Access Policy 21 (GSM_SAI_POL_21):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
20	0h RO	**SMM Read Access Policy 20 (GSM_SAI_POL_20):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
19	0h RO	**SMM Read Access Policy 19 (GSM_SAI_POL_19):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
18	0h RO	**SMM Read Access Policy 18 (GSM_SAI_POL_18):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
17	0h RW	**SMM Read Access Policy 17 (GSM_SAI_POL_17):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
16	1h RW	**SMM Read Access Policy 16 (GSM_SAI_POL_16):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
15	0h RO	**SMM Read Access Policy 15 (GSM_SAI_POL_15):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
14	0h RO	**SMM Read Access Policy 14 (GSM_SAI_POL_14):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**SMM Read Access Policy 13 (GSM_SAI_POL_13):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
12	0h RW	**SMM Read Access Policy 12 (GSM_SAI_POL_12):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
11	0h RO	**SMM Read Access Policy 11 (GSM_SAI_POL_11):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
10	0h RO	**SMM Read Access Policy 10 (GSM_SAI_POL_10):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
9	0h RO	**SMM Read Access Policy 9 (GSM_SAI_POL_9):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
8	1h RW	**SMM Read Access Policy 8 (GSM_SAI_POL_8):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
7	0h RO	**SMM Read Access Policy 7 (GSM_SAI_POL_7):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
6	0h RO	**SMM Read Access Policy 6 (GSM_SAI_POL_6):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
5	0h RW	**SMM Read Access Policy 5 (GSM_SAI_POL_5):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
4	0h RW	**SMM Read Access Policy 4 (GSM_SAI_POL_4):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
3	0h RW	**SMM Read Access Policy 3 (GSM_SAI_POL_3):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**SMM Read Access Policy 2 (GSM_SAI_POL_2):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
1	0h RW	**SMM Read Access Policy 1 (GSM_SAI_POL_1):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
0	0h RW	**SMM Read Access Policy 0 (GSM_SAI_POL_0):** Bit vector used to determine which agents are allowed read access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.

5.9.117 GSM Write Access Policy (B_CR_BGSMWAC_0_0_0_MCHBAR)—Offset 6B38h

This register configures the Write Access Policy for the memory range from BGSM to TOLUD1. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 100060010100h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW	**GSM Write Access Policy 63 (GSM_SAI_POL_63):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
62	0h RO	**GSM Write Access Policy 62 (GSM_SAI_POL_62):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
61	0h RO	**GSM Write Access Policy 61 (GSM_SAI_POL_61):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
60	0h RO	**GSM Write Access Policy 60 (GSM_SAI_POL_60):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
59	0h RO	**GSM Write Access Policy 59 (GSM_SAI_POL_59):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
58	0h RO	**GSM Write Access Policy 58 (GSM_SAI_POL_58):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
57	0h RO	**GSM Write Access Policy 57 (GSM_SAI_POL_57):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
56	0h RW	**GSM Write Access Policy 56 (GSM_SAI_POL_56):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
55	0h RW	**GSM Write Access Policy 55 (GSM_SAI_POL_55):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
54	0h RW	**GSM Write Access Policy 54 (GSM_SAI_POL_54):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
53	0h RO	**GSM Write Access Policy 53 (GSM_SAI_POL_53):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
52	0h RO	**GSM Write Access Policy 52 (GSM_SAI_POL_52):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
51	0h RO	**GSM Write Access Policy 51 (GSM_SAI_POL_51):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
50	0h RW	**GSM Write Access Policy 50 (GSM_SAI_POL_50):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
49	0h RW	**GSM Write Access Policy 49 (GSM_SAI_POL_49):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**GSM Write Access Policy 48 (GSM_SAI_POL_48):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
47	0h RO	**GSM Write Access Policy 47 (GSM_SAI_POL_47):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
46	0h RO	**GSM Write Access Policy 46 (GSM_SAI_POL_46):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
45	0h RO	**GSM Write Access Policy 45 (GSM_SAI_POL_45):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
44	1h RW	**GSM Write Access Policy 44 (GSM_SAI_POL_44):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
43	0h RW	**GSM Write Access Policy 43 (GSM_SAI_POL_43):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
42	0h RW	**GSM Write Access Policy 42 (GSM_SAI_POL_42):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
41	0h RW	**GSM Write Access Policy 41 (GSM_SAI_POL_41):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
40	0h RW	**GSM Write Access Policy 40 (GSM_SAI_POL_40):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
39	0h RO	**GSM Write Access Policy 39 (GSM_SAI_POL_39):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
38	0h RW	**GSM Write Access Policy 38 (GSM_SAI_POL_38):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
37	0h RO	**GSM Write Access Policy 37 (GSM_SAI_POL_37):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
36	0h RW	**GSM Write Access Policy 36 (GSM_SAI_POL_36):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
35	0h RO	**GSM Write Access Policy 35 (GSM_SAI_POL_35):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
34	0h RW	**GSM Write Access Policy 34 (GSM_SAI_POL_34):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
33	0h RW	**GSM Write Access Policy 33 (GSM_SAI_POL_33):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
32	0h RW	**GSM Write Access Policy 32 (GSM_SAI_POL_32):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
31	0h RO	**GSM Write Access Policy 31 (GSM_SAI_POL_31):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
30	1h RW	**GSM Write Access Policy 30 (GSM_SAI_POL_30):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
29	1h RW	**GSM Write Access Policy 29 (GSM_SAI_POL_29):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
28	0h RW	**GSM Write Access Policy 28 (GSM_SAI_POL_28):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
27	0h RW	**GSM Write Access Policy 27 (GSM_SAI_POL_27):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
26	0h RW	**GSM Write Access Policy 26 (GSM_SAI_POL_26):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
25	0h RW	**GSM Write Access Policy 25 (GSM_SAI_POL_25):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
24	0h RW	**GSM Write Access Policy 24 (GSM_SAI_POL_24):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
23	0h RO	**GSM Write Access Policy 23 (GSM_SAI_POL_23):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
22	0h RO	**GSM Write Access Policy 22 (GSM_SAI_POL_22):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
21	0h RW	**GSM Write Access Policy 21 (GSM_SAI_POL_21):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
20	0h RO	**GSM Write Access Policy 20 (GSM_SAI_POL_20):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
19	0h RO	**GSM Write Access Policy 19 (GSM_SAI_POL_19):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
18	0h RO	**GSM Write Access Policy 18 (GSM_SAI_POL_18):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
17	0h RW	**GSM Write Access Policy 17 (GSM_SAI_POL_17):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
16	1h RW	**GSM Write Access Policy 16 (GSM_SAI_POL_16):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**GSM Write Access Policy 15 (GSM_SAI_POL_15):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
14	0h RO	**GSM Write Access Policy 14 (GSM_SAI_POL_14):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
13	0h RW	**GSM Write Access Policy 13 (GSM_SAI_POL_13):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
12	0h RW	**GSM Write Access Policy 12 (GSM_SAI_POL_12):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
11	0h RO	**GSM Write Access Policy 11 (GSM_SAI_POL_11):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
10	0h RO	**GSM Write Access Policy 10 (GSM_SAI_POL_10):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
9	0h RO	**GSM Write Access Policy 9 (GSM_SAI_POL_9):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
8	1h RW	**GSM Write Access Policy 8 (GSM_SAI_POL_8):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
7	0h RO	**GSM Write Access Policy 7 (GSM_SAI_POL_7):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
6	0h RO	**GSM Write Access Policy 6 (GSM_SAI_POL_6):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
5	0h RW	**GSM Write Access Policy 5 (GSM_SAI_POL_5):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GSM Write Access Policy 4 (GSM_SAI_POL_4):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
3	0h RW	**GSM Write Access Policy 3 (GSM_SAI_POL_3):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
2	0h RW	**GSM Write Access Policy 2 (GSM_SAI_POL_2):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
1	0h RW	**GSM Write Access Policy 1 (GSM_SAI_POL_1):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.
0	0h RW	**GSM Write Access Policy 0 (GSM_SAI_POL_0):** Bit vector used to determine which agents are allowed write access to the memory range from BGSM to TOLUD1, based on each agent's 6bit encoded SAI value.

5.9.118 TPM Control Policy (B_CR_TPM_CP_0_0_0_MCHBAR)—Offset 6B40h

Defines the control policy register for TPM group.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**TPM Control Policy (CTRL_POL):** Bit vector used to determine which agents are allowed write access to TPM_AC register, based on each agent's 6-bit encoded SAI value.

5.9.119 TPM Access Control (B_CR_TPM_AC_0_0_0_MCHBAR)—Offset 6B48h

Defines the policy register that specifies who is allowed read/write access to the TPM_SELECTOR register.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**TPM Access Policy (AC_POL):** Bit vector used to determine which agents are allowed read/write access to TPM_SELECTOR, based on each agent's 6-bit encoded SAI value.

5.9.120 BGSM Control Register (B_CR_BGSM_CTRL_0_0_0_MCHBAR)—Offset 6B50h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 19h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved (RESERVED_0):** Reserved.
4	1h RW	**RS0 Asset Classification Bit for Graphics and Data Stolen Memory (RS0_EN):** PII transactions from RS0 that hit the Graphics and Data Stolen Memory range will be allowed access only when both of the following conditions are met: a) Request SAI is in the legal permitted list as specified in the RAC/WAC policy registers and b) GSM_RS0_EN bit is set to 1. PII RS0 transactions targeting DRAM that do not hit any enabled IMR or special protected regions will always be allowed access.
3	1h RW	**GT Implicit WB Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback data HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester depending on the setting of the IA_IWB_EN bit.
2	0h RW	**IA Implicit WB Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester, depending on the setting of the GT_IWB_EN bit.
1	0h RW	**Trace Enable (TRACE_EN):** Enables snooping of transactions to the Graphics Stolen Memory region by tracing agents.

Bit Range	Default & Access	Field Name (ID): Description
0	1h RW	**Range Check Enable (RANGE_CHECK_EN):** Enables SAI checking for the memory range from BGSM to TOLUD-1

5.9.121 SMM Control Register (B_CR_BSMR_CTRL_0_0_0_MCHBAR)—Offset 6B54h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 7h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved (RESERVED_0):** Reserved.
4	0h RO	**RS0 Asset Classification Bit for SMM Region (RS0_EN):** No PII transaction is allowed access to SMM region. As such RS0 asset classification bit does not apply and hence provisioned as a readonly bit and set to 0.
3	0h RW	**GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback data HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester, depending on the setting of the IA_IWB_EN bit.
2	1h RW	**IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester depending on the setting of the GT_IWB_EN bit.
1	1h RW	**Trace Enable (TRACE_EN):** Enables snooping of transactions to the SMM region by tracing agents.
0	1h RW	**Range Check Enable (RANGE_CHECK_EN):** Enables SAI checking for the SMM memory range: TSEGMB to BGSM.

5.9.122 Default VTd Control Register (B_CR_BDEFVTDPMR_CTRL_0_0_0_MCHBAR)—Offset 6B58h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1Ch

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved (RESERVED_1):** Reserved.
4	1h RW	**RS0 Asset Classification Bit for the High and Low VTd PMRs (RS0_EN):** PII transactions from RS0 that hit VTd PMR high and low memory ranges will be allowed access only when both of the following conditions are met: a) Request SAI is in the legal permitted list as specified in the RAC/WAC policy registers and b) VTDPMR_RS0_EN bit is set to 1. PII RS0 transactions targeting DRAM that do not hit any enabled IMR or special protected regions will always be allowed access.
3	1h RW	**GT Implicit Writeback Enable (GT_IWB_EN):** Enables implicit writebacks to protected region from GT caching agent. When set to 1, enables implicit writeback data HITM data from GT to be returned to the requester. When set to 0, inhibits HITM data from GT from being returned to the requester. HITM data from IA cores may be returned to the requester, depending on the setting of the IA_IWB_EN bit.
2	1h RW	**IA Implicit Writeback Enable (IA_IWB_EN):** Enables implicit writebacks to protected region from IA caching agent. When set to 1, enables implicit writeback data HITM data from IA cores to be returned to the requester. When set to 0, inhibits HITM data from IA cores from being returned to the requester. HITM data from GT may be returned to the requester, depending on the setting of the GT_IWB_EN bit.
1	0h RW	**Trace Enable (TRACE_EN):** Enables snooping of transactions to the Default VTd PHM and PLM regions by tracing agents.
0	0h RO	**Reserved (RESERVED_0):** Reserved.

5.9.123 MOT Trigger Trace Control (B_CR_MOT_TRIG_TRACE_CTRL_0_0_0_MCHBAR)—Offset 6B7Ch

This register is the global MOT enable.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: E0000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Eh RW	**Flush Timer Period (FLUSH_TIMER_PERIOD):** Specifies the duration of the periodic MOT flush timer. Duration is 2^N cycles of a 19.2 MHz clock, where N is the value specified in the field.
27	0h RO	**Reserved (RESERVED_0):** Reserved.
26	0h RW/V	**Sticky Trigger 1 Match (STICKY_TRIGGER_1_MATCH):** 1 indicates Trigger 1 match. Cleared by powergood or explicit SW write.
25	0h RW/V	**Sticky Trigger 0 Match (STICKY_TRIGGER_0_MATCH):** 1 indicates Trigger 0 match. Cleared by powergood or explicit SW write.
24	0h RW/V	**Sticky Filter 1 Match (STICKY_FILTER_1_MATCH):** 1 indicates Filter 1 match. Cleared by powergood or explicit SW write.
23	0h RW/V	**Sticky Filter 0 Match (STICKY_FILTER_0_MATCH):** 1 indicates Filter 0 match. Cleared by powergood or explicit SW write.
22	0h RW/V	**MOT Storage Active (MOT_STORAGE_ACTIVE):** Current status of MOT storage to memory. Used to save/restore trigger state across power states.
21:16	0h RW	**MOT Trace Storage Stop Source (MOT_TRACE_STORAGE_STOP_SOURCE):** A bit field allowing multiple triggers to result in a trace storage stop. Storage stop is the logical OR of trigger sources selected. Note that selecting the same trigger to start and stop trace storage results in start trace storage only. • Bit position 5: External Trigger in 1 • Bit position 4: External Trigger in 0 • Bit position 3: MOT Trigger 1 • Bit position 2: MOT Trigger 0 • Bit position 1: MOT Filter 1 match • Bit position 0: MOT Filter 0 match
15:10	0h RW	**MOT Trace Storage Start Source (MOT_TRACE_STORAGE_START_SOURCE):** A bit field allowing multiple triggers to result in a trace storage start. Storage stop is the logical OR of trigger sources selected. Note that selecting the same trigger to start and stop trace storage results in start trace storage only. For bit positions, see description for MOT_TRACE_STORAGE_STOP_SOURCE field.
9	0h RW	**Enable External Trigger in 1 (ENABLE_EXTERNAL_TRIGGER_IN_1):** • 1 to enable external trigger 1 to MOT from rdu_mid • 0 to disable external trigger 1 to MOT from rdu_mid
8	0h RW	**Enable External Trigger in 0 (ENABLE_EXTERNAL_TRIGGER_IN_0):** • 1 to enable external trigger 0 to MOT from rdu_mid • 0 to disable external trigger 0 to MOT from rdu_mid

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RW	**Trigger Out Source (TRIGGER_OUT_SOURCE):** Select source of trigger sent to rdu_mid. • 00b: Filter 0 • 01b: Filter 1 • 10b: Trigger 0 • 11b: Trigger 1
5	0h RW	**Enable External Trigger Out 0 (ENABLE_EXTERNAL_TRIGGER_OUT_0):** • 1: enable external trigger out to from MOT to rdu_mid • 0: disable external trigger out to from MOT to rdu_mid
4	0h RW	**Enable MOT Trigger 1 (ENABLE_MOT_TRIGGER_1):** • 1: enable MOT trigger 1 • 0: disable MOT trigger 1
3	0h RW	**Enable MOT Trigger 0 (ENABLE_MOT_TRIGGER_0):** • 1: enable MOT trigger 0 • 0: disable MOT trigger 0
2	0h RW	**Enable MOT Filter 1 (ENABLE_MOT_FILTER_1):** • 1: enable MOT filter 1 • 0: disable MOT filter 1
1	0h RW	**Enable MOT Filter 0 (ENABLE_MOT_FILTER_0):** • 1: enable MOT filter 0 • 0: disable MOT filter 0
0	0h RW	**Global MOT Enable (ENABLE_MOT):** • 1: enable MOT • 0: disable MOT

5.9.124 MOT Slice 0 Memory Pointer (B_CR_MOT_SLICE_0_MEM_PTR_0_0_0_MCHBAR)—Offset 6B80h

This register contains the memory address pointer used to determine where the MOT slice 0 cache lines are stored. On a write, the B-Unit logic will set itself to the value of the write Extraction of memory contents is performed as reads. On a read, the data returned should match the current value of the pointer reflecting incrementing updates from cache lines that have been stored. It also pins MOT to near or far memory.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 2h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_0):** Reserved.
38:6	0h RW/V	**MOT Memory Pointer (MOT_MEMORY_POINTER):** The current pointer into MOT slice 0 region. Cache line granularity bits [38:6].
5:2	0h RO	**Reserved (RESERVED_1):** Reserved.
1	1h RW	**Near or Far Memory (NEAR_OR_FAR_MEMORY):** Pin MOT slice 0 to near1 or far0 memory. This logic is implemented in the 2LM. Thus, this register bit is shadowed in its entirety in the 2LM. Unused by MOT.
0	0h RW/V	**MOT Buffer Wrap (MOT_BUFFER_WRAP):** Indication that the MOT slice 0 buffer has wrapped since the last clear of this write cleared by power good or explicit SW write.

5.9.125 MOT Slice 1 Memory Pointer (B_CR_MOT_SLICE_1_MEM_PTR_0_0_0_MCHBAR)—Offset 6B88h

This register contains the memory address pointer used to determine where the MOT slice 1 cache lines are stored. On a write, the B-Unit logic will set itself to the value of the write. Extraction of memory contents are performed as reads. On a read, the data returned should match the current value of the pointer, reflecting incrementing updates from cache lines that have been stored. It also pins MOT to near or far memory.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 2h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_0):** Reserved.
38:6	0h RW/V	**MOT Memory Pointer (MOT_MEMORY_POINTER):** The current pointer into MOT slice 1 region. Cache line granularity bits [38:6].
5:2	0h RO	**Reserved (RESERVED_1):** Reserved.
1	1h RW	**Near or Far Memory (NEAR_OR_FAR_MEMORY):** Pin MOT slice 1 to near1 or far0 memory. This logic is implemented in the 2LM. Thus, this register is shadowed in its entirety in the 2LM.
0	0h RW/V	**MOT Buffer Wrap (MOT_BUFFER_WRAP):** Indication that the MOT slice 1 buffer has wrapped since the last clear of this write cleared by power good or explicit SW write.

5.9.126 MOT Slice 0 Record ID (B_CR_MOT_SLICE_0_RECORD_ID_0_0_0_MCHBAR)—Offset 6B90h

This register contains the unique MOT record ID and start trace indication for slice 0. This state needs to be stored in a CR to allow it to persist across autoPG and s0ix transitions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved (RESERVED_0):** Reserved.
26	0h RW/V	**First Packet Captured (FIRST_PKT_CAPTURED):** Indicates that MOT has captured the first data packet after tracing started.
25:0	0h RW/V	**Record ID (RECORD_ID):** The current MOT unique record ID number.

5.9.127 MOT Slice 1 Record ID (B_CR_MOT_SLICE_1_RECORD_ID_0_0_0_MCHBAR)—Offset 6B94h

This register contains the unique MOT record ID and start trace indication for slice 0. This state needs to be stored in a CR to allow it to persist across autoPG and s0ix transitions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved (RESERVED_0):** Reserved.
26	0h RW/V	**First Packet Captured (FIRST_PKT_CAPTURED):** Indicates that MOT has captured the first data packet after tracing started.
25:0	0h RW/V	**Record ID (RECORD_ID):** The current MOT unique record ID number.

5.9.128 MOT Filter Match 0 (B_CR_MOT_FILTER_MATCH0_0_0_0_MCHBAR)—Offset 6BA0h

This register contains the value of the MOT 0 access filter Match address.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_0):** Reserved.
38:5	0h RW	**MOT 0 Filter Match Address (MOT_0_FILTER_MATCH_ADDRESS):** Access address to match. Match results in trace of access. Half cache line granularity bits 38:5 to support legacy devices.
4:0	0h RO	**Reserved (RESERVED_1):** Reserved.

5.9.129 MOT Filter Mask (B_CR_MOT_FILTER_MASK0_0_0_0_MCHBAR)—Offset 6BA8h

This register contains the value of the MOT 0 access filter Mask address.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 7FFFFFFFE0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_0):** Reserved.
38:5	3FFFFFFFFh RW	**MOT 0 Filter Mask Address (MOT_0_FILTER_MASK_ADDRESS):** Access address bits to mask. A value of 1 ignores the corresponding address bit. Half cache line granularity bits 38:5 to support legacy devices.
4:0	0h RO	**Reserved (RESERVED_1):** Reserved.

5.9.130 MOT Filter Match 1 (B_CR_MOT_FILTER_MATCH1_0_0_0_MCHBAR)—Offset 6BB0h

This register contains the value of the MOT 1 access filter Match address.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_0):** Reserved.
38:5	0h RW	**MOT 1 Filter Match Address (MOT_1_FILTER_MATCH_ADDRESS):** Access address to match. Match results in trace of access. Half cache line granularity bits 38:5 to support legacy devices.
4:0	0h RO	**Reserved (RESERVED_1):** Reserved.

5.9.131 MOT Filter Mask 1 (B_CR_MOT_FILTER_MASK1_0_0_0_MCHBAR)—Offset 6BB8h

This register contains the value of the MOT 1 access filter Mask address.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 7FFFFFFFE0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_0):** Reserved.
38:5	3FFFFFFFFh RW	**MOT 1 Filter Mask Address (MOT_1_FILTER_MASK_ADDRESS):** Access address bits to mask. A value of 1 ignores the corresponding address bit. Half cache line granularity bits 38:5 to support legacy devices.
4:0	0h RO	**Reserved (RESERVED_1):** Reserved.

5.9.132 MOT Filter Misc 0 (B_CR_MOT_FILTER_MISC0_0_0_0_MCHBAR)—Offset 6BC0h

This register contains the value of the MOT 0 access filter Match/Mask Agent LPID.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:35	0h RO	**Reserved (RESERVED_0)**
34:19	0h RW	**IA Core Match (IA_CORE_MATCH):** Match if transaction originated from one of up to 16 IA cores (one bit per logical processor).
18	0h RW	**GT Match (GT_MATCH):** • 1: match • 0: ignore
17:2	0h RW	**VC Match (VC_MATCH):** Match if transaction originated from one of up to 16 virtual channel cores (one bit per VC).
1	0h RW	**Address Match Polarity (ADDR_MATCH_POLARITY):** • 1: filter inversion • 0: match criteria
0	0h RW	**Access Type Match Read or Write (ACCESS_TYPE_MATCH_READ_OR_WRITE):** • 1: match writes • 0: match reads

5.9.133 MOT Filter Misc 1 (B_CR_MOT_FILTER_MISC1_0_0_0_MCHBAR)—Offset 6BC8h

This register contains the value of the MOT 1 access filter Match/Mask Agent LPID.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:35	0h RO	**Reserved (RESERVED_0)**
34:19	0h RW	**IA Core Match (IA_CORE_MATCH):** Match if transaction originated from one of up to 16 IA cores (one bit per logical processor).
18	0h RW	**GT Match (GT_MATCH):** • 1: match • 0: ignore
17:2	0h RW	**VC Match (VC_MATCH):** Match if transaction originated from one of up to 16 virtual channel cores (one bit per VC).
1	0h RW	**Address Match Polarity (ADDR_MATCH_POLARITY):** • 1: filter inversion • 0: match criteria
0	0h RW	**Access Type Match Reads or Writes (ACCESS_TYPE_MATCH_READ_OR_WRITE):** • 1: match writes • 0: match reads

5.9.134 MOT Trigger Match 0 (B_CR_MOT_TRIGGER_MATCH0_0_0_0_MCHBAR)—Offset 6BD0h

This register contains the value of the MOT 0 access trigger Match address.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_0):** Reserved.
38:5	0h RW	**MOT 0 Trigger Match Address (MOT_0_TRIGGER_MATCH_ADDRESS):** Access address to match. Match results in trace of access. Half cache line granularity bits 38:5 to support legacy devices.
4:0	0h RO	**Reserved (RESERVED_1):** Reserved.

5.9.135 MOT Trigger Mask 0 (B_CR_MOT_TRIGGER_MASK0_0_0_0_MCHBAR)—Offset 6BD8h

This register contains the value of the MOT 0 access trigger Mask address.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 7FFFFFFFE0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_0):** Reserved.
38:5	3FFFFFFFFh RW	**MOT 0 Trigger Mask Address (MOT_0_TRIGGER_MASK_ADDRESS):** Access address bits to mask. A value of 1 ignores the corresponding address bit. Half cache line granularity bits 38:5 to support legacy devices.
4:0	0h RO	**Reserved (RESERVED_1):** Reserved.

5.9.136 MOT Trigger Match 1 (B_CR_MOT_TRIGGER_MATCH1_0_0_0_MCHBAR)—Offset 6BE0h

This register contains the value of the MOT 1 access trigger Match address.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_0):** Reserved.
38:5	0h RW	**MOT1 Trigger Match Address (MOT_1_TRIGGER_MATCH_ADDRESS):** Access address to match. Match results in trace of access. Half cache line granularity bits 38:5 to support legacy devices.
4:0	0h RO	**Reserved (RESERVED_1):** Reserved.

5.9.137 MOT Trigger Mask 1 (B_CR_MOT_TRIGGER_MASK1_0_0_0_MCHBAR)—Offset 6BE8h

This register contains the value of the MOT 1 access trigger Mask address.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 7FFFFFFFE0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_0):** Reserved.
38:5	3FFFFFFFFh RW	**MOT 1 Trigger Mask Address (MOT_1_TRIGGER_MASK_ADDRESS):** Access address bits to mask. A value of 1 ignores the corresponding address bit. Half cache line granularity bits 38:5 to support legacy devices.
4:0	0h RO	**Reserved (RESERVED_1):** Reserved.

5.9.138 MOT Trigger Misc 0 (B_CR_MOT_TRIGGER_MISC0_0_0_0_MCHBAR)—Offset 6BF0h

This register contains the value of the MOT 0 access trigger Match/Mask Agent LPID.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:35	0h RO	**Reserved (RESERVED_0)**
34:19	0h RW	**IA Core Match (IA_CORE_MATCH):** Match if transaction originated from one of up to 16 IA cores (one bit per logical processor).
18	0h RW	**GT Match (GT_MATCH):** • 1: match • 0: ignore
17:2	0h RW	**VC Match (VC_MATCH):** Match if transaction originated from one of up to 16 virtual channel cores (one bit per VC).

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Address Match Polarity (ADDR_MATCH_POLARITY):** • 1: filter inversion • 0: match criteria
0	0h RW	**Access Type -- Match Read or Write (ACCESS_TYPE_MATCH_READ_OR_WRITE):** • 1: match writes • 0: match reads

5.9.139 MOT Trigger Misc 1 (B_CR_MOT_TRIGGER_MISC1_0_0_0_MCHBAR)—Offset 6BF8h

This register contains the value of the MOT 1 access trigger Match/Mask Agent LPID.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:35	0h RO	**Reserved (RESERVED_0)**
34:19	0h RW	**IA Core Match (IA_CORE_MATCH):** Match if transaction originated from one of up to 16 IA cores (one bit per logical processor).
18	0h RW	**GT Match (GT_MATCH):** • 1: match • 0: ignore
17:2	0h RW	**VC Match (VC_MATCH):** Match if transaction originated from one of up to 16 virtual channel cores (one bit per VC).
1	0h RW	**Address Match Polarity (ADDR_MATCH_POLARITY):** • 1: filter inversion • 0: match criteria
0	0h RW	**Access Type -- Match Read or Write (ACCESS_TYPE_MATCH_READ_OR_WRITE):** • 1: match writes • 0: match reads

5.9.140 MOT PSMI Sync (B_CR_MOT_PSMI_SYNC_0_0_0_MCHBAR)—Offset 6C00h

This register is used for PSMI sync.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved (RESERVED_0):** Reserved.
1	0h RW/V	**PSMI Sync 1 (PSMI_SYNC1):** Set by PSMI microcode. Once set, cleared by HW after creation of first MOT record in Slice1.
0	0h RW/V	**PSMI Sync 0 (PSMI_SYNC0):** Set by PSMI microcode. Once set, cleared by HW after creation of first MOT record in Slice0.

5.9.141 BIOSWR Control Policy (B_CR_BIOSWR_CP_0_0_0_MCHBAR)—Offset 6C08h

This register specifies the control policy for the BIOSWR security policy group. It controls write access to the Read Access Policy BIOSWR_RAC, Write Access Policy BIOSWR_WAC configuration registers, and self-referentially to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**Memory Range Control Policy (MEM_RANGE_CTRL_POL):** Bit vector used to determine which agents are allowed write access to the BIOSWR_RAC, BIOSWR_WAC, and BIOSWR_CP registers, based on the value from each agent's 6bit SAI field.

5.9.142 BIOSWR Read Access Policy (B_CR_BIOSWR_RAC_0_0_0_MCHBAR)—Offset 6C10h

This register configures the Read Access Policy for the BIOSWR security policy group. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine read access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 80000C00630D0217h

Bit Range	Default & Access	Field Name (ID): Description
63:0	80000C00630D0217h RW	**Memory Range Policy (MEM_RANGE_POL):** Bit vector used to determine which agents are allowed read access, based on each agent's 6bit encoded SAI value.

5.9.143 BIOSWR Write Access Policy (B_CR_BIOSWR_WAC_0_0_0_MCHBAR)—Offset 6C18h

This register configures the Write Access Policy for the BIOSWR security policy group. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C00610C0212h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C00610C0212h RW	**Memory Range Policy (MEM_RANGE_POL):** Bit vector used to determine which agents are allowed write access, based on each agent's 6bit encoded SAI value.

5.9.144 TPM Selector (B_CR_TPM_SELECTOR_0_0_0_MCHBAR)—Offset 6C24h

Specifies where the TPM lives in the platform. B-Unit uses this register to source decode for requests whose addresses fall within the fixed address range for the TPM.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved (RESERVED_0):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**TPM Selector (TPM_SELECTOR):** • 0h: fTPM enabled. Target of TPM accesses is the CSE. • 1h: SPI TPM enabled. Target of TPM accesses is SPI. • 2h: LPC TPM enabled. Target of TPM accesses is LPC. • 3h: All TPMs disabled. Target of TPM accesses is the PSF Error Handler.

5.9.145 B-Unit Pcode/Ucode Write, All Read Control Policy Register (B_CR_P_U_CODEWR_ALLRD_CP_0_0_0_MCHBAR)—Offset 6C28h

This register controls the access policy to the Read Access Policy P_U_CODEWR_ALLRD_RAC and Write Access Policy P_U_CODEWR_ALLRD_WAC configuration registers, and self-referentially to itself. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine both read access and write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001000202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001000202h RW	**B-Unit Pcode/Ucode Write, All Read Control Policy (IA_CTRL_POL):** Bit vector used to determine which agents are allowed access to the P_U_CODEWR_ALLRD_RAC, P_U_CODEWR_ALLRD_WAC, and P_U_CODEWR_ALLRD_CP registers, based on the value from the agent's 6bit SAI field.

5.9.146 B-Unit Pcode/Ucode Read Access Policy (B_CR_P_U_CODEWR_ALLRD_RAC_0_0_0_MCHBAR)—Offset 6C30h

This register configures the Read Access Policy for the B-Unit Pcode/Ucode Write, All Read registers.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: FFFFFFFFFFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:0	FFFFFFFFF FFFFFFFh RO	**B-Unit Pcode/Ucode Write, All Read SAI Read Access Policy (IA_SAI_POL):** Bit vector used to determine which agents are allowed read access to the B-Unit Pcode/Ucode Write, All Read policy registers, based on each agent's 6bit encoded SAI value.

5.9.147 B-Unit Pcode/Ucode Write Access Policy (B_CR_P_U_CODEWR_ALLRD_WAC_0_0_0_MCHBAR)—Offset 6C38h

This register configures the Write Access Policy for the B-Unit Pcode/Ucode Write, All Read policy registers. The requesting agent's 6bit encoded SAI value is used as an index into this register's bits to determine write access.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001000202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001000 202h RW	**B-Unit Pcode/Ucode Write, All Read SAI Write Access Policy (IA_SAI_POL):** Bit vector used to determine which agents are allowed write access to the B-Unit IA Core Configuration registers, based on each agent's 6bit encoded SAI value.

5.9.148 Default VTd BAR (B_CR_DEFVTDBAR_0_0_0_MCHBAR)—Offset 6C80h

BIOS must write DEFVTDBAR and then immediately follow it up with a read to DEFVTDBAR to ensure that all copies of DEFVTDBAR in the system are updated.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:40	0h RO	**Reserved (RESERVED_0):** Reserved.
39	0h RO	**DEFVTDBAR 40 Bit (DEFVTDBAR_40_BIT):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
38:12	0h RW	**Default IOMMU VTd Config Space Base (DEFVTDBAR):** If DEFVTDBAR is enabled, this field corresponds to bits 38:12 of the base address default IOMMU VTd configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the default VTd IOMMU register set. If DEFVTDBAR is enabled and incoming Request Address[38:12] matches DEFVTDBAR[38:12] the request targets the Default VTd BAR.
11:2	0h RO	**Reserved (RESERVED_1):** Reserved.
1	0h RW	**Lock Register Content (LOCK):** Locks the contents of the register including itself. Unused by the B-Unit, and does not implement the intended lock functionality. B-Unit includes this bit to support shadow copies of the register that rely on this lock bit.
0	0h RW/L	**DEFVTDBAR Enable (DEFVTDBAREN):** • 0: DEFVTDBAR is disabled and does not claim any memory • 1: DEFVTDBAR memory mapped accesses are claimed and decoded appropriately. This bit will remain 0 if VTd capability is disabled.

5.9.149 Gfx VTd BAR (B_CR_GFXVTDBAR_0_0_0_MCHBAR)—Offset 6C88h

BIOS must write GFXVTDBAR and then immediately follow it up with read of DEVEN_0_0_0_PCI, then write (with value from read operation) to DEVEN_0_0_0_PCI to ensure that all copies of GFXVTDBAR in the system are updated.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_0):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
38:12	0h RW	**GFXVT Base Address (GFXVTBAR):** This field corresponds to bits 38 to 12 of the base address GFXVT configuration space. BIOS will program this register, resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the GFXVT register set. If GFXVTBAR is enabled and incoming Request Address[38:12] matches GFXVTBAR[38:12] the request targets the Gfx VTd BAR.
11:2	0h RO	**Reserved (RESERVED_1):** Reserved.
1	0h RW	**Lock Register Content (LOCK):** Locks the contents of the register, including itself. Unused by the B-Unit, and does not implement the intended lock functionality. B-Unit includes this bit to support shadow copies of the register that rely on this lock bit.
0	0h RW/L	**GFXVTBAR Enable (GFXVTBAREN):** • 0: GFXVTBAR is disabled and does not claim any memory • 1: GFXVTBAR memory mapped accesses are claimed and decoded appropriately. This bit will remain 0 if VTd capability is disabled.

5.9.150 B-Unit Lites Group 0 Control (B_CR_LITES0_CTL_0_0_0_MCHBAR)—Offset 6C90h

This register controls the functionality of the B-Unit Lites Group 0 mask/match functionality.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RW	**IDI Length Match (IDI_LENGTH_MATCH):** Enables length matching for IDI requests for Lites Group 0. Each bit, when set to 1, enables match for that length for an IDI request. Lites logic supports only lengths 0-16B for PRd and PortIn and only 64B for all other opcodes. • Bit 31:64B • Bit 30:16B • Bit 29:15B • Bit 28:14B • Bit 27:13B • Bit 26:12B • Bit 25:11B • Bit 24:10B • Bit 23:9B • Bit 22:8B • Bit 21:7B • Bit 20:6B • Bit 19:5B • Bit 18:4B • Bit 17:3B • Bit 16:2B • Bit 15:1B • Bit 14:0B
13:12	0h RW	**PII Length Match (PII_LENGTH_MATCH):** Enables length matching for PII requests for Lites Group 0. Each bit, when set to 1, enables length match for the PII request. • Bit 13:64B • Bit 12:32B
11:10	0h RO	**Reserved (RESERVED_0):** Reserved.
9:8	0h RW	**Slice Match (SLICE_MATCH):** • 00: All mask/match hits are suppressed • 01: Mask/Match hits enabled only for Slice0 • 10: Mask/match hits enabled only for Slice1 • 11: Mask/Match hits enabled for both Slices
7:4	0h RW	**DWord Select (DWORD_SELECT):** Selects the dword within the 512bit data field that is compared for data mask/matches for Lites Group 0.
3	0h RW	**Enable Data Match (ENABLE_DATA_MATCH):** When set, this field enables data matching on Lites Group 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Alternate U2C Request View (ALTU2CREQVIEW):** When set, address match/mask, opcode match and agent match registers are used to generate matches for the U2C request observation point. When clear, Badmit observation point matches are reported on the U2C request observation point.
1	0h RW	**Invert Address Match (INVERT_ADDR_MATCH):** When set, inverts the polarity of the address match/mask logic, i.e., reports a match for addresses that are not in the specified range.
0	0h RW	**Enable Group (ENABLE_GROUP):** Enables all match filters for Lites Group 0. The following are the observation points that contain match filters: Badmit logic within each slice after a transaction is successfully admitted into the B-Unit, U2C request launch, PMI datain for each PMI channel for read data, PMI dataout for each PMI channel for writes, data write from requesters to BRAM in each slice, and read data return on the live bypass and nonlive bypass paths in each slice. To report a match at an observation point, all match criteria for that point must be satisfied.

5.9.151 B-Unit Lites Group 0 Opcode Match Filter (B_CR_LITES0_OPCODE_MATCH_0_0_0_MCHBAR)—Offset 6C94h

This register contains the IDI and PII opcodes that will enable a Lites Group0 opcode match on a transaction.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Opcode Match (OPCODE_MATCH):** Bit vector that enables a match on the opcode for C2U IDI requests, PII A2B requests, and U2C IDI requests. All three observation points, Badmit in both slices and the U2C request interface, use this same opcode match register. Each bit, when set, enables a match on the corresponding opcode, and, when clear, will suppress a match on the corresponding opcode. To match on any opcode, set all bits to 1. • Bit 31: C2U_Req_CRd • Bit 30: C2U_Req_DRd • Bit 29: C2U_Req_DRdPTE • Bit 28: C2U_Req_SetMonitor • Bit 27: C2U_Req_RFO,U2C_Req_LTWrite_piclet • Bit 26: C2U_Req_PRd,U2C_Req_VLW_piclet • Bit 25: C2U_Req_UcRdF • Bit 24: C2U_Req_PortIn,U2C_Req_SnpCode • Bit 23: C2U_Req_IntA,U2C_Req_SnpData • Bit 22: C2U_Req_Lock • Bit 21: C2U_Req_SplitLock,U2C_Req_IntLog_piclet • Bit 20: C2U_Req_Unlock,U2C_Req_IntPhy_piclet • Bit 19: C2U_Req_ItoM • Bit 18: C2U_Req_SpCyc,U2C_Req_SnpInv • Bit 17: C2U_Req_RdMonitor,U2C_Req_StopReq • Bit 16: C2U_Req_ClrMonitor,U2C_Req_StartReq • Bit 15: C2U_Req_CLFlush • Bit 14: C2U_Req_WbMtoI,U2C_Req_IntLog_MSI • Bit 13: C2U_Req_WbMtoE,U2C_Req_IntPhy_MSI • Bit 12: C2U_Req_WiL • Bit 11: C2U_Req_WCiL • Bit 10: C2U_Req_WCilF • Bit 9: C2U_Req_PortOut • Bit 8: C2U_Req_IntPriUp,U2C_Req_LTWrite • Bit 7: C2U_Req_IntLog • Bit 6: C2U_Req_IntPhy • Bit 5: C2U_Req_EOI,U2C_Req_VLW • Bit 4: C2U_Req_ItoMWr • Bit 3: A2B_Req_SnoopedRead • Bit 2: A2B_Req_UnSnoopedRead,U2C_Req_IntPhy_IPI • Bit 1: A2B_Req_SnoopedWrite • Bit 0: A2B_Req_UnSnoopedWrite,U2C_Req_IntLog_IPI

5.9.152 B-Unit Lites Group 0 Agent Match Filter (B_CR_LITES0_AGENT_MATCH_0_0_0_MCHBAR)—Offset 6C98h

This register designates which agents are enabled to trigger a Lites Group0 AgentID match on a transaction.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**GT Match (GT_MATCH):** This field is used to match IDI transactions from GT for Lites Group0. When set, enables a match for a transaction originating from GT. When clear, suppresses a match for a transaction from GT.
30:16	0h RW	**VC Match (VC_MATCH):** This field is used to match VC Channel ID for PII transactions for Lites Group0. Each bit, when set, enables a match for a transaction originating from that VC. When clear, suppresses a match for a transaction from that VC. • Bit 30: VC14 • Bit 29: VC13 • Bit 28: VC12 • Bit 27: VC11 • Bit 26: VC10 • Bit 25: VC9 • Bit 24: VC8 • Bit 23: VC7 • Bit 22: VC6 • Bit 21: VC5 • Bit 20: VC4 • Bit 19: VC3 • Bit 18: VC2 • Bit 17: VC1 • Bit 16: VC0

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**CPU Core Match (CPU_CORE_MATCH):** This field is used to match Logical Processor Core ID for CPU IDI transactions for Lites Group 0. Each bit, when set, enables a match for a transaction originating from that core. When clear, suppresses a match for a transaction from that core. • Bit 15: CPU7 Core1 • Bit 14: CPU7 Core0 • Bit 13: CPU6 Core1 • Bit 12: CPU6 Core0 • Bit 11: CPU5 Core1 • Bit 10: CPU5 Core0 • Bit 9: CPU4 Core1 • Bit 8: CPU4 Core0 • Bit 7: CPU3 Core1 • Bit 6: CPU3 Core0 • Bit 5: CPU2 Core1 • Bit 4: CPU2 Core0 • Bit 3: CPU1 Core1 • Bit 2: CPU1 Core0 • Bit 1: CPU0 Core1 • Bit 0: CPU0 Core0

5.9.153 B-Unit Lites Group 0 U2C IntData Match Filter (B_CR_LITES0_U2CINTDATA_MATCH_0_0_0_MCHBAR)—Offset 6C9Ch

When U2C alternate view is enabled, this register specifies match criteria for U2C IntData.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Mask for U2C Request IntData[15:0] (INTDATA_MASK):** This mask is for generating Lites Group 0 U2C request alternative view match. Only bits [7:0] of this field are used; bits [15:8] are ignored. If a mask bit in this register is 0, then the corresponding bit in the INTDATA_MATCH field is ignored. If the mask bit is 1, then the corresponding bit in the INTDATA_MATCH[7:0] field must match its corresponding u2c request IntData[15:8] bit for a match.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**IntData Match (INTDATA_MATCH):** U2C Request IntData[15:8] value is compared with bits [7:0] of this field to generate a match for the U2C request address match. Bits [15:8] of this field are ignored. Note that matching based on the IntData[7:0] bits is not supported.

5.9.154 B-Unit Lites Group 0 Address Match Filter LITES0_ADDR_MATCH (B_CR_LITES0_ADDR_MATCH_0_0_0_MCHBAR)—Offset 6CA0h

This register, together with the LITES0_ADDR_MASK register, specifies the request address values that trigger a Lites Group 0 address match on a transaction.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_1):** Reserved.
38:3	0h RW	**Address Match (ADDRESS_MATCH):** Address value to match for Lites.
2:0	0h RO	**Reserved (RESERVED_0):** Reserved.

5.9.155 B-Unit Lites Group 0 Address Mask Filter LITES0_ADDR_MASK (B_CR_LITES0_ADDR_MASK_0_0_0_MCHBAR)—Offset 6CA8h

This register, together with the LITES0_ADDR_MATCH register, specifies the request address values that trigger a Lites Group 0 address match on a transaction.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_1):** Reserved.
38:3	0h RW	**Address Mask (ADDRESS_MASK):** Address mask value used for comparing request address during filter operation for Lites. If the mask bit in this register is 0, then the corresponding bit in the ADDR_MATCH register is ignored. If the mask bit is 1, then the corresponding bit in the ADDR_MATCH register must match the corresponding request address bit for a match.
2:0	0h RO	**Reserved (RESERVED_0):** Reserved.

5.9.156 B-Unit Lites Group 0 Data Match Filter LITES0_DATA_MATCH (B_CR_LITES0_DATA_MATCH_0_0_0_MCHBAR)—Offset 6CB0h

This register, together with LITES0_DATA_MASK, specifies the data values that will trigger a Lites Group 0 data filter match. All data observation points -- PMI data in, PMI data out, read data to agent (both live and nonlive) and write data from agent -- use the same Group 0 data match/mask registers for generating a match. Data match/mask can be enabled for only one DW of the transaction data. The specific DW can be selected via DWORD_SELECT.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data Match (DATA_MATCH):** Data value to match for Lites.

5.9.157 B-Unit Lites Group 0 Data Mask Filter LITES0_DATA_MASK (B_CR_LITES0_DATA_MASK_0_0_0_MCHBAR)—Offset 6CB4h

This register, together with LITES0_DATA_MATCH, specifies the data values that will trigger a Lites Group 0 data filter match for Lites. All data observation points -- PMI data in, PMI data out, read data to agent (both live and nonlive) and write data from agent -- use the same Group 0 data match/mask registers for generating a Group 0 data filter match. Data match/mask can be enabled for only one DW of the transaction data. The specific DW can be selected via DWORD_SELECT.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data Mask (DATA_MASK):** Data mask value used for comparing data during filter operations for Lites. If the mask bit in this register is 0, then the corresponding bit in the DATA_MATCH register is ignored. If the mask bit is 1, then the corresponding bit in the DATA_MATCH register must match the corresponding bit of the request data for a match.

5.9.158 B-Unit Lites Group 1 Control (B_CR_LITES1_CTL_0_0_0_MCHBAR)—Offset 6CC0h

This register controls the B-Unit Lites Group 1 mask/match functionality.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RW	**IDI Length Match (IDI_LENGTH_MATCH):** Enables length matching for IDI requests for Lites Group 1. Each bit, when set to 1, enables match for that length for an IDI request. Lites logic supports only lengths 0-16B for PRd and PortIn and only 64B for all other opcodes. • Bit 31:64B • Bit 30:16B • Bit 29:15B • Bit 28:14B • Bit 27:13B • Bit 26:12B • Bit 25:11B • Bit 24:10B • Bit 23:9B • Bit 22:8B • Bit 21:7B • Bit 20:6B • Bit 19:5B • Bit 18:4B • Bit 17:3B • Bit 16:2B • Bit 15:1B • Bit 14:0B
13:12	0h RW	**PII Length Match (PII_LENGTH_MATCH):** Enables length matching for PII requests for Lites Group 1. Each bit, when set to 1, enables length match for the PII request. • Bit 13:64B • Bit 12:32B
11:10	0h RO	**Reserved (RESERVED_0):** Reserved.
9:8	0h RW	**Slice Match (SLICE_MATCH):** • 00: All mask/match hits are suppressed • 01: mask/match hits enabled only for Slice0 • 10: mask/match hits enabled only for Slice1 • 11: mask/match hits enabled for both Slices
7:4	0h RW	**DWord Select (DWORD_SELECT):** Selects the dword within the 512bit data field that is compared for data mask/matches for Lites Group 1.
3	0h RW	**Enable Data Match (ENABLE_DATA_MATCH):** When set, this field enables data matching on Lites Group 1.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Alternate U2C Request View (ALTU2CREQVIEW):** When set, address match/mask opcode match and agent match registers are used to generate matches for the U2C request observation point. When clear, Badmit observation point matches are reported on the U2C request observation point.
1	0h RW	**Invert Address Match (INVERT_ADDR_MATCH):** When set, inverts the polarity of the address match/mask logic, i.e., reports a match for addresses that are not in the specified range.
0	0h RW	**Enable Group (ENABLE_GROUP):** Enables all match filters for Lites Group 1. The following are the observation points that contain match filters: Badmit logic within each slice after a transaction is successfully admitted into the B-Unit, U2C request launch, PMI datain for each PMI channel for read data, PMI dataout for each PMI channel for writes, data write from requesters to BRAM in each slice, and read data return on the live bypass and nonlive bypass paths in each slice. To report a match at an observation point, all match criteria for that point must be satisfied.

5.9.159 B-Unit Lites Group 1 Opcode Match Filter (B_CR_LITES1_OPCODE_MATCH_0_0_0_MCHBAR)—Offset 6CC4h

This register contains the IDI and PII opcodes that will enable a Lites Group1 opcode match on a transaction.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Opcode Match (OPCODE_MATCH):** Bit vector that enables a match on the opcode for C2U IDI requests, PII A2B requests, and U2C IDI requests. All three observation points -- Badmit in both slices, and the U2C request interface -- use this same opcode match register. Each bit, when set, enables a match on the corresponding opcode, and when clear will suppress a match on the corresponding opcode. To match on any opcode, set all bits to 1. • Bit 31: C2U_Req_CRd • Bit 30: C2U_Req_DRd • Bit 29: C2U_Req_DRdPTE • Bit 28: C2U_Req_SetMonitor • Bit 27: C2U_Req_RFO,U2C_Req_LTWrite_piclet • Bit 26: C2U_Req_PRd,U2C_Req_VLW_piclet • Bit 25: C2U_Req_UcRdF • Bit 24: C2U_Req_PortIn,U2C_Req_SnpCode • Bit 23: C2U_Req_IntA,U2C_Req_SnpData • Bit 22: C2U_Req_Lock • Bit 21: C2U_Req_SplitLock,U2C_Req_IntLog_piclet • Bit 20: C2U_Req_Unlock,U2C_Req_IntPhy_piclet • Bit 19: C2U_Req_ItoM • Bit 18: C2U_Req_SpCyc,U2C_Req_SnpInv • Bit 17: C2U_Req_RdMonitor,U2C_Req_StopReq • Bit 16: C2U_Req_ClrMonitor,U2C_Req_StartReq • Bit 15: C2U_Req_CLFlush • Bit 14: C2U_Req_WbMtoI,U2C_Req_IntLog_MSI • Bit 13: C2U_Req_WbMtoE,U2C_Req_IntPhy_MSI • Bit 12: C2U_Req_WiL • Bit 11: C2U_Req_WCiL • Bit 10: C2U_Req_WCilF • Bit 9: C2U_Req_PortOut • Bit 8: C2U_Req_IntPriUp,U2C_Req_LTWrite • Bit 7: C2U_Req_IntLog • Bit 6: C2U_Req_IntPhy • Bit 5: C2U_Req_EOI,U2C_Req_VLW • Bit 4: C2U_Req_ItoMWr • Bit 3: A2B_Req_SnoopedRead • Bit 2: A2B_Req_UnSnoopedRead,U2C_Req_IntPhy_IPI • Bit 1: A2B_Req_SnoopedWrite • Bit 0: A2B_Req_UnSnoopedWrite,U2C_Req_IntLog_IPI

5.9.160 B-Unit Lites Group 1 Agent Match Filter (B_CR_LITES1_AGENT_MATCH_0_0_0_MCHBAR)—Offset 6CC8h

This register designates which agents are enabled to trigger a Lites Group1 AgentID match on a transaction.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**GT Match (GT_MATCH):** This field is used to match IDI transactions from GT for Lites Group1. When set, enables a match for a transaction originating from GT. When clear, suppresses a match for a transaction from GT.
30:16	0h RW	**VC Match (VC_MATCH):** This field is used to match VC Channel ID for PII transactions for Lites Group1. Each bit, when set, enables a match for a transaction originating from that VC. When clear, each bit suppresses a match for a transaction from that VC. • Bit 30: VC14 • Bit 29: VC13 • Bit 28: VC12 • Bit 27: VC11 • Bit 26: VC10 • Bit 25: VC9 • Bit 24: VC8 • Bit 23: VC7 • Bit 22: VC6 • Bit 21: VC5 • Bit 20: VC4 • Bit 19: VC3 • Bit 18: VC2 • Bit 17: VC1 • Bit 16: VC0

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**CPU Core Match (CPU_CORE_MATCH):** This field is used to match Logical Processor Core ID for CPU IDI transactions, for Lites Group 1. Each bit, when set, enables a match for a transaction originating from that core. When clear, each bit suppresses a match for a transaction from that core. • Bit 15: CPU7 Core1 • Bit 14: CPU7 Core0 • Bit 13: CPU6 Core1 • Bit 12: CPU6 Core0 • Bit 11: CPU5 Core1 • Bit 10: CPU5 Core0 • Bit 9: CPU4 Core1 • Bit 8: CPU4 Core0 • Bit 7: CPU3 Core1 • Bit 6: CPU3 Core0 • Bit 5: CPU2 Core1 • Bit 4: CPU2 Core0 • Bit 3: CPU1 Core1 • Bit 2: CPU1 Core0 • Bit 1: CPU0 Core1 • Bit 0: CPU0 Core0

5.9.161 B-Unit Lites Group 1 U2C IntData Match Filter (B_CR_LITES1_U2CINTDATA_MATCH_0_0_0_MCHBAR)—Offset 6CCCh

When U2C alternate view is enabled, this register specifies match criteria for U2C IntData.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**IntData Mask (INTDATA_MASK):** This mask is for generating Lites Group 1 U2C request alternative view match. Only bits [7:0] of this field are used; bits [15:8] are ignored. If a mask bit in this register is 0, then the corresponding bit in the INTDATA_MATCH field is ignored. If the mask bit is 1, then the corresponding bit in the INTDATA_MATCH[7:0] field must match its corresponding u2c request IntData[15:8] bit for a match.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**IntData Match (INTDATA_MATCH):** U2C Request IntData[15:8] value is compared with bits [7:0] of this field to generate a match for the U2C request address match. Bits [15:8] of this field are ignored. Note that matching based on the IntData[7:0] bits is not supported.

5.9.162 B-Unit Lites Group 1 Address Match Filter LITES1_ADDR_MATCH (B_CR_LITES1_ADDR_MATCH_0_0_0_MCHBAR)—Offset 6CD0h

This register, together with the LITES1_ADDR_MASK register, specifies the request address values that trigger a Lites Group 1 address match on a transaction.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_1):** Reserved.
38:3	0h RW	**Address Match (ADDRESS_MATCH):** Address value to match for Lites
2:0	0h RO	**Reserved (RESERVED_0):** Reserved.

5.9.163 B-Unit Lites Group 1 Address Mask Filter LITES1_ADDR_MASK (B_CR_LITES1_ADDR_MASK_0_0_0_MCHBAR)—Offset 6CD8h

This register, together with the LITES1_ADDR_MATCH register, specifies the request address values that trigger a Lites Group 1 address match on a transaction.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_1):** Reserved.
38:3	0h RW	**Address Mask (ADDRESS_MASK):** Address mask value used for comparing request address during filter operation for Lites. If the mask bit in this register is 0, then the corresponding bit in the ADDR_MATCH register is ignored. If the mask bit is 1, then the corresponding bit in the ADDR_MATCH register must match the corresponding request address bit for a match.
2:0	0h RO	**Reserved (RESERVED_0):** Reserved.

5.9.164 B-Unit Lites Group 1 Data Match Filter LITES1_DATA_MATCH (B_CR_LITES1_DATA_MATCH_0_0_0_MCHBAR)—Offset 6CE0h

This register, together with LITES1_DATA_MASK, specifies the data values that will trigger a Lites Group 1 data filter match. All data observation points -- PMI data in, PMI data out, read data to agent (both live and nonlive) and write data from agent -- use the same Group 1 data match/mask registers for generating a match. Data match/mask can be enabled for only one DW of the transaction data. The specific DW can be selected via DWORD_SELECT.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data Match (DATA_MATCH):** Data value to match for Lites.

5.9.165 B-Unit Lites Group 1 Data Mask Filter LITES1_DATA_MASK (B_CR_LITES1_DATA_MASK_0_0_0_MCHBAR)—Offset 6CE4h

This register, together with LITES1_DATA_MATCH, specifies the data values that will trigger a Lites Group 1 data filter match for Lites. All data observation points -- PMI data in, PMI data out, read data to agent (both live and nonlive) and write data from agent -- use the same Group 1 data match/mask registers for generating a Group 1 data filter match. Data match/mask can be enabled for only one DW of the transaction data. The specific DW can be selected via DWORD_SELECT.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data Mask (DATA_MASK):** Data mask value used for comparing data during filter operations for Lites. If the mask bit in this register is 0, then the corresponding bit in the DATA_MATCH register is ignored. If the mask bit is 1, then the corresponding bit in the DATA_MATCH register must match the corresponding bit of the request data for a match.

5.9.166 B-Unit Lites Group 2 Control (B_CR_LITES2_CTL_0_0_0_MCHBAR)—Offset 6CF0h

This register controls the functionality of the B-Unit Lites Group 2 mask/match functionality.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RW	**IDI Length Match (IDI_LENGTH_MATCH):** Enables length matching for IDI requests for Lites Group 2. Each bit, when set to 1, enables match for that length for an IDI request. Lites logic supports only lengths 0-16B for PRd and PortIn and only 64B for all other opcodes. • Bit 31:64B • Bit 30:16B • Bit 29:15B • Bit 28:14B • Bit 27:13B • Bit 26:12B • Bit 25:11B • Bit 24:10B • Bit 23:9B • Bit 22:8B • Bit 21:7B • Bit 20:6B • Bit 19:5B • Bit 18:4B • Bit 17:3B • Bit 16:2B • Bit 15:1B • Bit 14:0B
13:12	0h RW	**PII Length Match (PII_LENGTH_MATCH):** Enables length matching for PII requests for Lites Group 2. Each bit, when set to 1, enables length match for the PII request. • Bit 13:64B • Bit 12:32B
11:10	0h RO	**Reserved (RESERVED_0):** Reserved.
9:8	0h RW	**Slice Match (SLICE_MATCH):** • 00: All mask/match hits are suppressed • 01: Mask/Match hits enabled only for Slice0 • 10: Mask/match hits enabled only for Slice1 • 11: Mask/Match hits enabled for both Slices
7:4	0h RW	**Dword Select (DWORD_SELECT):** Selects the dword within the 512bit data field that is compared for data mask/matches for Lites Group 2.
3	0h RW	**Enable Data Match (ENABLE_DATA_MATCH):** When set, this field enables data matching on Lites Group 2.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Alternname UC2 Request View (ALTU2CREQVIEW):** When set, address match/mask opcode match and agent match registers are used to generate matches for the U2C request observation point. When clear, Badmit observation point matches are reported on the U2C request observation point.
1	0h RW	**Invert Address Match (INVERT_ADDR_MATCH):** When set, inverts the polarity of the address match/mask logic, i.e., reports a match for addresses that are not in the specified range.
0	0h RW	**Enable Group (ENABLE_GROUP):** Enables all match filters for Lites Group 2. The following are the observation points that contain match filters: Badmit logic within each slice after a transaction is successfully admitted into the B-Unit, U2C request launch PMI datain for each PMI channel read data, PMI dataout for each PMI channel write data, agent data write to BRAM in each slice, read data return on the live bypass and nonlive bypass paths in each slice. To report a match at an observation point all match criteria for that point must be satisfied.

5.9.167 B-Unit Lites Group 2 Opcode Match Filter (B_CR_LITES2_OPCODE_MATCH_0_0_0_MCHBAR)—Offset 6CF4h

This register contains the IDI and PII opcodes that will enable a Lites Group2 opcode match on a transaction.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Opcode Match (OPCODE_MATCH):** Bit vector that enables a match on the opcode for C2U IDI requests, PII A2B requests, and U2C IDI requests. All three observation points -- Badmit in both slices, and the U2C request interface -- use this same opcode match register. Each bit, when set, enables a match on the corresponding opcode and when clear will suppress a match on the corresponding opcode. To match on any opcode, set all bits to 1. • Bit 31: C2U_Req_CRd • Bit 30: C2U_Req_DRd • Bit 29: C2U_Req_DRdPTE • Bit 28: C2U_Req_SetMonitor • Bit 27: C2U_Req_RFO,U2C_Req_LTWrite_piclet • Bit 26: C2U_Req_PRd,U2C_Req_VLW_piclet • Bit 25: C2U_Req_UcRdF • Bit 24: C2U_Req_PortIn,U2C_Req_SnpCode • Bit 23: C2U_Req_IntA,U2C_Req_SnpData • Bit 22: C2U_Req_Lock • Bit 21: C2U_Req_SplitLock,U2C_Req_IntLog_piclet • Bit 20: C2U_Req_Unlock,U2C_Req_IntPhy_piclet • Bit 19: C2U_Req_ItoM • Bit 18: C2U_Req_SpCyc,U2C_Req_SnpInv • Bit 17: C2U_Req_RdMonitor,U2C_Req_StopReq • Bit 16: C2U_Req_ClrMonitor,U2C_Req_StartReq • Bit 15: C2U_Req_CLFlush • Bit 14: C2U_Req_WbMtoI,U2C_Req_IntLog_MSI • Bit 13: C2U_Req_WbMtoE,U2C_Req_IntPhy_MSI • Bit 12: C2U_Req_WiL • Bit 11: C2U_Req_WCiL • Bit 10: C2U_Req_WCilF • Bit 9: C2U_Req_PortOut • Bit 8: C2U_Req_IntPriUp,U2C_Req_LTWrite • Bit 7: C2U_Req_IntLog • Bit 6: C2U_Req_IntPhy • Bit 5: C2U_Req_EOI,U2C_Req_VLW • Bit 4: C2U_Req_ItoMWr • Bit 3: A2B_Req_SnoopedRead • Bit 2: A2B_Req_UnSnoopedRead,U2C_Req_IntPhy_IPI • Bit 1: A2B_Req_SnoopedWrite • Bit 0: A2B_Req_UnSnoopedWrite,U2C_Req_IntLog_IPI •

5.9.168 B-Unit Lites Group 2 Agent Match Filter (B_CR_LITES2_AGENT_MATCH_0_0_0_MCHBAR)—Offset 6CF8h

This register designates which agents are enabled to trigger a Lites Group2 AgentID match on a transaction.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**GT Match (GT_MATCH):** This field is used to match IDI ransactions from GT for Lites Group2. When set, enables a match for a transaction originating from GT. When clear, suppresses a match for a transaction from GT.
30:16	0h RW	**VC Match (VC_MATCH):** This field is used to match VC Channel ID, for PII transactions for Lites Group2. Each bit, when set, enables a match for a transaction originating from that VC. When clear, suppresses a match for a transaction from that VC. • Bit 30: VC14 • Bit 29: VC13 • Bit 28: VC12 • Bit 27: VC11 • Bit 26: VC10 • Bit 25: VC9 • Bit 24: VC8 • Bit 23: VC7 • Bit 22: VC6 • Bit 21: VC5 • Bit 20: VC4 • Bit 19: VC3 • Bit 18: VC2 • Bit 17: VC1 • Bit 16: VC0

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**CPU Core Match (CPU_CORE_MATCH):** This field is used to match Logical Processor Core ID for CPU IDI transactions for Lites Group 2. Each bit, when set, enables a match for a transaction originating from that core. When clear, suppresses a match for a transaction from that core. • Bit 15: CPU7 Core1 • Bit 14: CPU7 Core0 • Bit 13: CPU6 Core1 • Bit 12: CPU6 Core0 • Bit 11: CPU5 Core1 • Bit 10: CPU5 Core0 • Bit 9: CPU4 Core1 • Bit 8: CPU4 Core0 • Bit 7: CPU3 Core1 • Bit 6: CPU3 Core0 • Bit 5: CPU2 Core1 • Bit 4: CPU2 Core0 • Bit 3: CPU1 Core1 • Bit 2: CPU1 Core0 • Bit 1: CPU0 Core1 • Bit 0: CPU0 Core0

5.9.169 B-Unit Lites Group 2 U2C IntData Match Filter (B_CR_LITES2_U2CINTDATA_MATCH_0_0_0_MCHBAR)—Offset 6CFCh

When U2C alternate view is enabled, this register specifies match criteria for U2C IntData.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**IntData Mask (INTDATA_MASK):** This mask is for generating Lites Group 2 U2C request alternative view match. Only bits [7:0] of this field are used; bits [15:8] are ignored. If a mask bit in this register is 0, then the corresponding bit in the INTDATA_MATCH field is ignored. If the mask bit is 1, then the corresponding bit in the INTDATA_MATCH[7:0] field must match its corresponding u2c request IntData[15:8] bit for a match.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**IntData Match (INTDATA_MATCH):** U2C Request IntData[15:8] value is compared with bits [7:0] of this field to generate a match for the U2C request address match. Bits [15:8] of this field are ignored. Note that matching based on the IntData[7:0] bits is not supported.

5.9.170 B-Unit Lites Group 2 Address Match Filter LITES2_ADDR_MATCH (B_CR_LITES2_ADDR_MATCH_0_0_0_MCHBAR)—Offset 6D00h

This register, together with the LITES2_ADDR_MASK register, specifies the request address values that trigger a Lites Group 2 address match on a transaction.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_1):** Reserved.
38:3	0h RW	**Address Match (ADDRESS_MATCH):** Address value to match for Lites.
2:0	0h RO	**Reserved (RESERVED_0):** Reserved.

5.9.171 B-Unit Lites Group 2 Address Mask Filter LITES2_ADDR_MASK (B_CR_LITES2_ADDR_MASK_0_0_0_MCHBAR)—Offset 6D08h

This register, together with the LITES2_ADDR_MATCH register, specifies the request address values that trigger a Lites Group 2 address match on a transaction.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_1):** Reserved.
38:3	0h RW	**Address Mask (ADDRESS_MASK):** Address mask value used for comparing request address during filter operation for Lites. If the mask bit in this register is 0, then the corresponding bit in the ADDR_MATCH register is ignored. If the mask bit is 1, then the corresponding bit in the ADDR_MATCH register must match the corresponding request address bit for a match.
2:0	0h RO	**Reserved (RESERVED_0):** Reserved.

5.9.172 B-Unit Lites Group 2 Data Match Filter LITES2_DATA_MATCH (B_CR_LITES2_DATA_MATCH_0_0_0_MCHBAR)—Offset 6D10h

This register, together with LITES2_DATA_MASK, specifies the data values that will trigger a Lites Group 2 data filter match. All data observation points PMI data in PMI data out read data to agent both live and nonlive and write data from agent use the same Group 2 data match/mask registers for generating a match. Data match/mask can be enabled for only one DW of the transaction data. The specific DW can be selected via DWORD_SELECT.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data Match (DATA_MATCH):** Data value to match for Lites

5.9.173 B-Unit Lites Group 2 Data Mask Filter LITES2_DATA_MASK (B_CR_LITES2_DATA_MASK_0_0_0_MCHBAR)—Offset 6D14h

This register, together with LITES2_DATA_MATCH, specifies the data values that will trigger a Lites Group 2 data filter match for Lites. All data observation points PMI data in PMI data out read data to agent both live and nonlive and write data from agent use the same Group 2 data match/mask registers for generating a Group 2 data filter match. Data match/mask can be enabled for only one DW of the transaction data. The specific DW can be selected via DWORD_SELECT.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data Mask (DATA_MASK):** Data mask value used for comparing data during filter operations for Lites. If the mask bit in this register is 0, then the corresponding bit in the DATA_MATCH register is ignored. If the mask bit is 1, then the corresponding bit in the DATA_MATCH register must match the corresponding bit of the request data for a match.

5.9.174 B-Unit Lites Group 3 Control (B_CR_LITES3_CTL_0_0_0_MCHBAR)—Offset 6D20h

This register controls the functionality of the B-Unit Lites Group 3 mask/match functionality.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RW	**IDI Length Match (IDI_LENGTH_MATCH):** Enables length matching for IDI requests for Lites Group 3. Each bit, when set to 1, enables match for that length for an IDI request. Lites logic supports only lengths 0-16B for PRd and PortIn and only 64B for all other opcodes. • Bit 31:64B • Bit 30:16B • Bit 29:15B • Bit 28:14B • Bit 27:13B • Bit 26:12B • Bit 25:11B • Bit 24:10B • Bit 23:9B • Bit 22:8B • Bit 21:7B • Bit 20:6B • Bit 19:5B • Bit 18:4B • Bit 17:3B • Bit 16:2B • Bit 15:1B • Bit 14:0B
13:12	0h RW	**PII Length Match (PII_LENGTH_MATCH):** Enables length matching for PII requests for Lites Group 3. Each bit, when set to 1, enables length match for the PII request: • Bit 13:64B • Bit 12:32B
11:10	0h RO	**Reserved (RESERVED_0):** Reserved.
9:8	0h RW	**Slice Match (SLICE_MATCH):** • 00: All mask/match hits are suppressed • 01: mask/match hits enabled only for Slice0 • 10: mask/match hits enabled only for Slice1 • 11: mask/match hits enabled for both Slices
7:4	0h RW	**Dword Select (DWORD_SELECT):** Selects the dword within the 512bit data field that is compared for data mask/matches for Lites Group 3.
3	0h RW	**Enable Data Match (ENABLE_DATA_MATCH):** When set, this field enables data matching on Lites Group 3.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Alternate U2C Request View (ALTU2CREQVIEW):** When set, address match/mask, opcode match and agent match registers are used to generate matches for the U2C request observation point. When clear, Badmit observation point matches are reported on the U2C request observation point.
1	0h RW	**Invert Address Match (INVERT_ADDR_MATCH):** When set inverts the polarity of the address match/mask logic i.e. reports a match for addresses that are not in the specified range.
0	0h RW	**Enable Group (ENABLE_GROUP):** Enables all match filters for Lites Group 3. The following are the observation points that contain match filters Badmit logic within each slice after a transaction is successfully admitted into the B-Unit U2C request launch PMI datain for each PMI channel read data PMI dataout for each PMI channel write data agent data write to BRAM in each slice read data return on the live bypass and nonlive bypass paths in each slice. To report a match at an observation point all match criteria for that point must be satisfied.

5.9.175 B-Unit Lites Group 3 Opcode Match Filter (B_CR_LITES3_OPCODE_MATCH_0_0_0_MCHBAR)—Offset 6D24h

This register contains the IDI and PII opcodes that will enable a Lites Group3 opcode match on a transaction.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Opcode Match (OPCODE_MATCH):** Bit vector that enables a match on the opcode for C2U IDI requests, PII A2B requests, and U2C IDI requests. All three observation points -- Badmit in both slices, and the U2C request interface -- use this same opcode match register. Each bit, when set, enables a match on the corresponding opcode, and when clear will suppress a match on the corresponding opcode. To match on any opcode, set all bits to 1. • Bit 31: C2U_Req_CRd • Bit 30: C2U_Req_DRd • Bit 29: C2U_Req_DRdPTE • Bit 28: C2U_Req_SetMonitor • Bit 27: C2U_Req_RFO,U2C_Req_LTWrite_piclet • Bit 26: C2U_Req_PRd,U2C_Req_VLW_piclet • Bit 25: C2U_Req_UcRdF • Bit 24: C2U_Req_PortIn,U2C_Req_SnpCode • Bit 23: C2U_Req_IntA,U2C_Req_SnpData • Bit 22: C2U_Req_Lock • Bit 21: C2U_Req_SplitLock,U2C_Req_IntLog_piclet • Bit 20: C2U_Req_Unlock,U2C_Req_IntPhy_piclet • Bit 19: C2U_Req_ItoM • Bit 18: C2U_Req_SpCyc,U2C_Req_SnpInv • Bit 17: C2U_Req_RdMonitor,U2C_Req_StopReq • Bit 16: C2U_Req_ClrMonitor,U2C_Req_StartReq • Bit 15: C2U_Req_CLFlush • Bit 14: C2U_Req_WbMtoI,U2C_Req_IntLog_MSI • Bit 13: C2U_Req_WbMtoE,U2C_Req_IntPhy_MSI • Bit 12: C2U_Req_WiL • Bit 11: C2U_Req_WCiL • Bit 10: C2U_Req_WCilF • Bit 9: C2U_Req_PortOut • Bit 8: C2U_Req_IntPriUp,U2C_Req_LTWrite • Bit 7: C2U_Req_IntLog • Bit 6: C2U_Req_IntPhy • Bit 5: C2U_Req_EOI,U2C_Req_VLW • Bit 4: C2U_Req_ItoMWr • Bit 3: A2B_Req_SnoopedRead • Bit 2: A2B_Req_UnSnoopedRead,U2C_Req_IntPhy_IPI • Bit 1: A2B_Req_SnoopedWrite • Bit 0: A2B_Req_UnSnoopedWrite,U2C_Req_IntLog_IPI

5.9.176 B-Unit Lites Group 3 Agent Match Filter (B_CR_LITES3_AGENT_MATCH_0_0_0_MCHBAR)—Offset 6D28h

This register designates which agents are enabled to trigger a Lites Group3 AgentID match on a transaction.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**GT Match (GT_MATCH):** This field is used to match IDI transactions from GT for Lites Group3. When set, enables a match for a transaction originating from GT. When clear, suppresses a match for a transaction from GT.
30:16	0h RW	**VC Match (VC_MATCH):** This field is used to match VC Channel ID for PII transactions, for Lites Group3. Each bit, when set, enables a match for a transaction originating from that VC. When clear, the bit suppresses a match for a transaction from that VC. • Bit 30: VC14 • Bit 29: VC13 • Bit 28: VC12 • Bit 27: VC11 • Bit 26: VC10 • Bit 25: VC9 • Bit 24: VC8 • Bit 23: VC7 • Bit 22: VC6 • Bit 21: VC5 • Bit 20: VC4 • Bit 19: VC3 • Bit 18: VC2 • Bit 17: VC1 • Bit 16: VC0

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**CPU Core Match (CPU_CORE_MATCH):** This field is used to match Logical Processor Core ID for CPU IDI transactions, for Lites Group 3. Each bit, when set, enables a match for a transaction originating from that core. When clear, the bit suppresses a match for a transaction from that core. • Bit 15: CPU7 Core1 • Bit 14: CPU7 Core0 • Bit 13: CPU6 Core1 • Bit 12: CPU6 Core0 • Bit 11: CPU5 Core1 • Bit 10: CPU5 Core0 • Bit 9: CPU4 Core1 • Bit 8: CPU4 Core0 • Bit 7: CPU3 Core1 • Bit 6: CPU3 Core0 • Bit 5: CPU2 Core1 • Bit 4: CPU2 Core0 • Bit 3: CPU1 Core1 • Bit 2: CPU1 Core0 • Bit 1: CPU0 Core1 • Bit 0: CPU0 Core0

5.9.177 B-Unit Lites Group 3 U2C IntData Match Filter (B_CR_LITES3_U2CINTDATA_MATCH_0_0_0_MCHBAR)—Offset 6D2Ch

When U2C alternate view is enabled, this register specifies match criteria for U2C IntData.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**IntData Mask (INTDATA_MASK):** This mask is for generating Lites Group 3 U2C request alternative view match. Only bits [7:0] of this field are used; bits [15:8] are ignored. If a mask bit in this register is 0, then the corresponding bit in the INTDATA_MATCH field is ignored. If the mask bit is 1, then the corresponding bit in the INTDATA_MATCH[7:0] field must match its corresponding u2c request IntData[15:8] bit for a match.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**IntData Match (INTDATA_MATCH):** U2C Request IntData[15:8] value is compared with bits [7:0] of this field to generate a match for the U2C request address match. Bits [15:8] of this field are ignored. Note that matching based on the IntData[7:0] bits is not supported.

5.9.178 B-Unit Lites Group 3 Address Match Filter LITES3_ADDR_MATCH (B_CR_LITES3_ADDR_MATCH_0_0_0_MCHBAR)—Offset 6D30h

This register, together with the LITES3_ADDR_MASK register, specifies the request address values that trigger a Lites Group 3 address match on a transaction.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_1):** Reserved.
38:3	0h RW	**Address Match (ADDRESS_MATCH):** Address value to match for Lites.
2:0	0h RO	**Reserved (RESERVED_0):** Reserved.

5.9.179 B-Unit Lites Group 3 Address Mask Filter LITES3_ADDR_MASK (B_CR_LITES3_ADDR_MASK_0_0_0_MCHBAR)—Offset 6D38h

This register, together with the LITES3_ADDR_MATCH register, specifies the request address values that trigger a Lites Group 3 address match on a transaction.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_1):** Reserved.
38:3	0h RW	**Address Mask (ADDRESS_MASK):** Address mask value used for comparing request address during filter operation for Lites. If the mask bit in this register is 0, then the corresponding bit in the ADDR_MATCH register is ignored. If the mask bit is 1, then the corresponding bit in the ADDR_MATCH register must match the corresponding request address bit for a match.
2:0	0h RO	**Reserved (RESERVED_0):** Reserved.

5.9.180 B-Unit Lites Group 3 Data Match Filter LITES3_DATA_MATCH (B_CR_LITES3_DATA_MATCH_0_0_0_MCHBAR)—Offset 6D40h

This register, together with LITES3_DATA_MASK, specifies the data values that will trigger a Lites Group 3 data filter match. All data observation points -- PMI data in, PMI data out, read data to agent (both live and nonlive) and write data from agent -- use the same Group 3 data match/mask registers for generating a match. Data match/mask can be enabled for only one DW of the transaction data. The specific DW can be selected via DWORD_SELECT.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DATA_MATCH (DATA_MATCH):** Data value to match for Lites

5.9.181 B-Unit Lites Group 3 Data Mask Filter LITES3_DATA_MASK (B_CR_LITES3_DATA_MASK_0_0_0_MCHBAR)—Offset 6D44h

This register, together with LITES3_DATA_MATCH, specifies the data values that will trigger a Lites Group 3 data filter match for Lites. All data observation points -- PMI data in, PMI data out, read data to agent (both live and nonlive) and write data from agent -- use the same Group 3 data match/mask registers for generating a Group 3 data filter match. Data match/mask can be enabled for only one DW of the transaction data. The specific DW can be selected via DWORD_SELECT.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data Mask (DATA_MASK):** Data mask value used for comparing data during filter operations for Lites. If the mask bit in this register is 0, then the corresponding bit in the DATA_MATCH register is ignored. If the mask bit is 1, then the corresponding bit in the DATA_MATCH register must match the corresponding bit of the request data for a match.

5.9.182 B-Unit Lites and Emon Master Control LITESEMONCTL (B_CR_LITESEMON_CTL_0_0_0_MCHBAR)—Offset 6D48h

This register controls the functionality of the B-Unit Lites Debug functionality and Emon exposure to VISA.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Lites (ENABLE_LITES):** • 0: Lites logic is disabled. All Lites Views will be driven to 0s. • 1: Lites logic is enabled.
30:27	0h RW	**Emon Barb CQ Select (EMON_BARB_CQ_SELECT):** Select barb conflictQ FIFO. • 0000 to 0111: pii0 to pii7 • 1xx0: idi slice0 • 1xx1: idi slice1
26:24	0h RW	**Emon Barb Ingress Select (EMON_BARB_INGRESS_SELECT):** Select barb ingress FIFO. • 000: IDI attach point -0 -mono | per slice fifo0 • 001: IDI attach point -0 -slice fifo1 • 010: IDI attach point -1 -mono | per slice fifo1 • 011: IDI attach point -1 - slice fifo • 100: IDI attach point -2 -mono | GT slice0 • 101: IDI attach point -2 - slice fifo | GT slice1 • 110: IDI attach point -3 -mono | per slice fifo0 • 111: IDI attach point -3 - slice fifo1

Bit Range	Default & Access	Field Name (ID): Description
23:13	0h RW	**Emon VC Mask (EMON_VC_MASK):** B-Unit and T-Unit expose only the Emons corresponding to the VC(s) specified in this field (it is a mask).
12:5	0h RW	**Emon IDI Mask (EMON_IDI_MASK):** B-Unit and T-Unit expose only the Emons corresponding to the IDI agent(s) specified in this field (it is a mask). IDI agent refers to GLM modules and GT not Sunits.
4:2	0h RW	**Lites IDI Select (LITES_IDI_SELECT):** B-Unit and T-Unit expose only the views corresponding to the IDI agent specified in this field. IDI agents only refer to GT and GLM modules, not Sunits. Used only on the C2U response views.
1	0h RW	**Lites Slice Select (LITES_SLICE_SELECT):** When set to 0, B-Unit and T-Unit expose only Slice0 views. No Lites observability of any transaction routed to Slice 1. When set to 1, B-Unit and T-Unit expose only Slice1 views. No Lites observability of any transaction routed to Slice0.
0	0h RW	**Lites PMI Select (LITES_PMI_SELECT):** When set to 0, B-Unit exposes only PMI channel 0 views in either slice. No Lites observability of any transaction routed to PMI channel 1 in either slice. When set to 1, B-Unit exposes only PMI Channel 1 views in either slice.

5.9.183 B-Unit Arbiter Control BARBCTRL0 (B_CR_BARBCTRL0)—Offset 6D4Ch

Specifies the weighting for Agents 03 used by the B-Unit's Badmit Arbiter. The value specified in the Agent Weight field is used by the Badmit arbiters weight counters to determine the number of requests from an agent that are allowed to be granted before updating the requester's age register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4040404h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RESERVED_0):** Reserved.
29:24	4h RW	**Agent 3 Weight (AGENT3_WEIGHT):** Arbiter weight for Agent 3.
23:22	0h RO	**Reserved (RESERVED_1):** Reserved.
21:16	4h RW	**Agent 2 Weight (AGENT2_WEIGHT):** Arbiter weight for Agent 2.

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved (RESERVED_2):** Reserved.
13:8	4h RW	**Agent 1 Weight (AGENT1_WEIGHT):** Arbiter weight for Agent 1.
7:6	0h RO	**Reserved (RESERVED_3):** Reserved.
5:0	4h RW	**Agent 0 Weight (AGENT0_WEIGHT):** Arbiter weight for Agent 0.

5.9.184 B-Unit Arbiter Control BARBCTRL1 (B_CR_BARBCTRL1)—Offset 6D50h

Specifies the weighting for Agents 4-7 used by the B-Unit's Badmit Arbiter. The value specified in the Agent Weight field is used by the Badmit arbiter's weight counters to determine the number of requests from an agent that are allowed to be granted before updating the requester's age register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4040404h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RESERVED_0):** Reserved.
29:24	4h RW	**Agent 7 Weight (AGENT7_WEIGHT):** Arbiter weight for Agent 7.
23:22	0h RO	**Reserved (RESERVED_1):** Reserved.
21:16	4h RW	**Agent 6 Weight (AGENT6_WEIGHT):** Arbiter weight for Agent 6.
15:14	0h RO	**Reserved (RESERVED_2):** Reserved.
13:8	4h RW	**Agent 5 Weight (AGENT5_WEIGHT):** Arbiter weight for Agent 5.
7:6	0h RO	**Reserved (RESERVED_3):** Reserved.
5:0	4h RW	**Agent 4 Weight (AGENT4_WEIGHT):** Arbiter weight for Agent 4.

5.9.185 B-Unit Scheduler Control (B_CR_BSCHWT0)—Offset 6D54h

Specifies the weighting for Agents 0-3 used by the B-Unit Scheduler. The value is used by the B-Unit Scheduler to determine how many requests can be granted for the agent before the agent's requests are masked by the Scheduler Arbiter, to allow other agents' requests to be granted.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4040404h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RESERVED_0):** Reserved.
29:24	4h RW	**Agent 3 Weight (AGENT3_WEIGHT):** Arbiter weight for Agent 3.
23:22	0h RO	**Reserved (RESERVED_1):** Reserved.
21:16	4h RW	**Agent 2 Weight (AGENT2_WEIGHT):** Arbiter weight for Agent 2.
15:14	0h RO	**Reserved (RESERVED_2):** Reserved.
13:8	4h RW	**Agent 1 Weight (AGENT1_WEIGHT):** Arbiter weight for Agent 1.
7:6	0h RO	**Reserved (RESERVED_3):** Reserved.
5:0	4h RW	**Agent 0 Weight (AGENT0_WEIGHT):** Arbiter weight for Agent 0.

5.9.186 B-Unit Scheduler Control (B_CR_BSCHWT1)—Offset 6D58h

Specifies the weighting for Agents 4-7 used by the B-Unit Scheduler. The value is used by the B-Unit Scheduler to determine how many requests can be granted for the agent before the agent's requests are masked by the Scheduler Arbiter to allow other agents' requests to be granted.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4040404h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RESERVED_0):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29:24	4h RW	**Agent 7 Weight (AGENT7_WEIGHT):** Arbiter weight for Agent 7.
23:22	0h RO	**Reserved (RESERVED_1):** Reserved.
21:16	4h RW	**Agent 6 Weight (AGENT6_WEIGHT):** Arbiter weight for Agent 6.
15:14	0h RO	**Reserved (RESERVED_2):** Reserved.
13:8	4h RW	**Agent 5 Weight (AGENT5_WEIGHT):** Arbiter weight for Agent 5.
7:6	0h RO	**Reserved (RESERVED_3):** Reserved.
5:0	4h RW	**Agent 4 Weight (AGENT4_WEIGHT):** Arbiter weight for Agent 4.

5.9.187 B-Unit Scheduler Control (B_CR_BSCHWT2)—Offset 6D5Ch

Specifies the weighting for Agents 8-11 used by the B-Unit Scheduler. The value is used by the B-Unit Scheduler to determine how many requests can be granted for the agent before the agent's requests are masked by the Scheduler Arbiter to allow other agents' requests to be granted.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4040404h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RESERVED_0):** Reserved.
29:24	4h RW	**Agent 11 Weight (AGENT11_WEIGHT):** Arbiter weight for Agent 11.
23:22	0h RO	**Reserved (RESERVED_1):** Reserved.
21:16	4h RW	**Agent 10 Weight (AGENT10_WEIGHT):** Arbiter weight for Agent 10.
15:14	0h RO	**Reserved (RESERVED_2):** Reserved.
13:8	4h RW	**Agent 9 Weight (AGENT9_WEIGHT):** Arbiter weight for Agent 9.
7:6	0h RO	**Reserved (RESERVED_3):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
5:0	4h RW	**Agent 8 Weight (AGENT8_WEIGHT):** Arbiter weight for Agent 8.

5.9.188 B-Unit Scheduler Control (B_CR_BSCHWT3)—Offset 6D60h

Specifies the weighting for Agents 12-15 used by the B-Unit Scheduler. The value is used by the B-Unit Scheduler to determine how many requests can be granted for the agent before the agent's requests are masked by the Scheduler Arbiter to allow other agents' requests to be granted.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4040404h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RESERVED_0):** Reserved.
29:24	4h RW	**Agent 15 Weight (AGENT15_WEIGHT):** Arbiter weight for Agent 15.
23:22	0h RO	**Reserved (RESERVED_1):** Reserved.
21:16	4h RW	**Agent 14 Weight (AGENT14_WEIGHT):** Arbiter weight for Agent 14.
15:14	0h RO	**Reserved (RESERVED_2):** Reserved.
13:8	4h RW	**Agent 13 Weight (AGENT13_WEIGHT):** Arbiter weight for Agent 13.
7:6	0h RO	**Reserved (RESERVED_3):** Reserved.
5:0	4h RW	**Agent 12 Weight (AGENT12_WEIGHT):** Arbiter weight for Agent 12.

5.9.189 B-Unit Flush Control (B_CR_BWFLUSH)—Offset 6D64h

Controls the policy used to determine when dirty entries must be flushed to DRAM. When the number of dirty entries is lower than a high watermark dirty_hwm the B-Unit will opportunistically flush data to DRAM after the write flush timeout value. When the number of dirty entries exceeds the high water mark, the B-Unit will initiate a highpriority flush and push dirty data to DRAM until the count is once again below the low water mark.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FF010000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	FFh RW	**Flush Threshold (FLUSH_THRESHOLD):** All write commands are blocked at Badmit if the number of write commands in the Flush Pool exceeeds this value.
23:17	0h RO	**Reserved (RESERVED_0):** Reserved.
16	1h RO/V	**All Entries Flushed (ALL_ENTRIES_FLUSHED):** All dirty entries in the B-Unit, in both slices, have been flushed.
15:8	0h RW	**Dirty Low Water Mark (DIRTY_LWM):** Low water mark for dirty entries retained by the B-Unit. B-Unit will immediately attempt to flush any dirty entry, hence setting the low water mark to 0.
7:0	0h RW	**Dirty High Water Mark (DIRTY_HWM):** High water mark for dirty entries retained by the B-Unit. B-Unit will immediately attempt to flush any dirty entry, hence setting the low water mark to 0.

5.9.190 B-Unit Flush Weights (B_CR_BFLWT)—Offset 6D68h

Controls B-Unit alternate scheduling of reads and writes to DRAM.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 404h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Disable Flush Weights (DISABLE_FLUSH_WEIGHTS):** When set to 1, disables flush weights. Flushing of dirty entries will start when Dirty Limit is HWM, and continue until Dirty Limit is LWM. No reads will be scheduled in between.
30:14	0h RO	**Reserved (RESERVED_1):** Reserved.
13:8	4h RW	**Write Weights (WRITE_WEIGHTS):** Number of write requests sent to a PMI channel before switching to scheduling read requests, when use of flush weights is not disabled.
7:6	0h RO	**Reserved (RESERVED_0):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
5:0	4h RW	**Read Weights (READ_WEIGHTS):** Number of read requests sent to a PMI channel before switching to scheduling write requests, when use of flush weights is not disabled.

5.9.191 Weighted Scheduling Control of High Priority ISOC and Other Requests (B_CR_BISOCWT)—Offset 6D6Ch

Controls alternate scheduling of High Priority ISOC requests and other requests.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 80003F0Fh

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Enable ISOC Requests (ENABLE_ISOC_WEIGHTS):** When set to 1, enables switching from scheduling High Priority ISOC requests to scheduling Best Effort and Low Priority ISOC requests, based on ISOC weights and NONISOC weights.
30:14	0h RO	**Reserved (RESERVED_1):** Reserved.
13:8	3Fh RW	**ISOC Request Weights (ISOC_REQUEST_WEIGHTS):** Weight for high priority isochronous requests.
7:6	0h RO	**Reserved (RESERVED_0):** Reserved.
5:0	Fh RW	**Non ISOC Request Weights (NON_ISOC_REQUEST_WEIGHTS):** Weight for non-high priority isochronous and best effort requests.

5.9.192 B-Unit Control (B_CR_BCTRL2)—Offset 6D70h

Contains basic control information used by the B-Unit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: F0034h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Read Invalidate Timer (ENABLE_READ_INVALIDATE_TIMER):** When set to 1, enables the BRAM to clear the RD_DONE bit and flush dirty data when a timer expires. Used when parity is not enabled, to force the B-Unit to not indefinitely cache previously read lines, and also to cause a flush of dirty data that has been written to the BRAM entry.
30:26	0h RO	**Reserved (RESERVED_2):** Reserved.
25	0h RW	**DRAM_ECC_ENABLE (DRAM_ECC_ENABLE):** If DRAM ECC is enabled, the data error bits from the Dunit is used for indicating the derror for the corresponding transactions to the agents and forcing the poison bit when BUNIT PARITY is unsupported and Read for partial writes are enabled
24	0h RW	**MOT Disable Stall Arbiter on Error (MOT_DISABLE_STALL_ARB_ON_ERR):** If the HH widget gets an error, allow transactions to get arbitrated.
23:16	Fh RW	**BRAM Read Invalidate Time (BRAM_READ_INVALIDATE_TIME):** Timer threshold to clear rd_done bits or flush a BRAM entry, if dirty. The value specified is in multiples of 250ns. For each time interval specified, the read done status of one BRAM entry will be cleared based on a BTAG index which is then incremented to point to the next BRAM entry.
15:8	0h RW	**Casual Timer (CASUAL_TIMER):** The number of clock cycles that the B-Unit waits before starting a casual dirty flush. Casual Flush feature will not be enabled by PND2 architecture. Instead, a dirty write will be made eligible for scheduling immediately.
7:6	0h RO	**Reserved (RESERVED_1):** Reserved.
5	1h RW	**Enable 64B Write (ENABLE_64B_WRITE):** When set, B-unit will send 64B PMI Write requests for transactions requiring write access to DRAM. Must always be set to one, otherwise functional errors may occur.
4	1h RW	**Enable 64B Read (ENABLE_64B_READ):** When set, B-unit will send 64B PMI read requests for transactions requiring read access to DRAM. Must always be set to one, otherwise functional errors may occur.
3	0h RO	**Demand Scrub Enable (DEMAND_SCRUB_ENABLE):** This mode causes B-Unit to automatically issue a flush to PMI, thus writing correct data back to memory for any read request that returns with a correctable data error.
2	1h RW	**Enable Read Done for Write (ENABLE_READ_DONE_FOR_WRITE):** Enable Any writes (IWB or normal writes) to set the read_done bit in bstat, which enables return of data from the BRAM cache instead of Memory.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Miss Valid Entries (MISS_VALID_ENTRIES):** This mode causes reads to clean valid B-Unit buffer entries to look like misses instead of hits. When this bit is set -- even when all requested bytes are valid and present in the BRAM data buffer -- B-Unit will send read requests over the PMI interface to re-fetch the data from DRAM, instead of returning it from the BRAM.
0	0h RW	**Dirty Stall (DIRTY_STALL):** This mode causes reads or writes from any requester interface to dirty valid B-Unit buffer entries to stall on the appropriate requester interface until the entry has been flushed from the B-Unit.

5.9.193 Asset Classification Bits (B_CR_AC_RS0_0_0_0_MCHBAR)—Offset 6D74h

B-Unit Asset Classification AC[3] bits for IMRs and Special Protected Memory Region. Controls whether RS0 Root Space 0 transactions from PII are allowed access to IMRs and Protected Memory Region.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved (RESERVED_0):** Reserved.
20	1h RW	**MOT RS Asset Classification (MOT_RS0_EN):** RS Asset Classification bit for the MOT buffer. PII transactions from RS0 that hit the MOT buffer will be allowed access only when both of the following conditions are met: a) Request SAI is in the legal permitted list, as specified in the RAC/WAC policy registers, and b) MOT_RS0_EN bit is set to 1. PII RS0 transactions targeting DRAM that do not hit any enabled IMR or special protected regions will always be allowed access.
19:0	0h RW	**IMR RS Asset Classification (IMR_RS0_EN):** RS Asset Classification bit for IMRs 0-19. PII transactions from RS0 that hit an enabled IMR address range will be allowed access only when both of the following conditions are met: a) Request SAI is in the legal permitted list as specified in the IMRs RAC/WAC policy registers and b) IMR_AC_RS bit corresponding to the IMR is set to 1. PII RS0 transactions targeting DRAM that do not hit any enabled IMR or special protected regions will always be allowed access.

5.9.194 IDI Real-Time Feature Configuration Bits (B_CR_RT_EN_0_0_0_MCHBAR)—Offset 6D78h

IDI Real-Time Feature Configuration register. Controls which IDI attachpoint support Real-Time traffic/transactions.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:16	0h RW	**IDI Agent Real-Time Traffic Mask Bits (RT_IDI_AGENT):** IDI Agent Real-Time Traffic Mask Bits. Controls which IDI Agent supports Real-Time Traffic/Transactions. Only one IDI Agent needs to be selected for real-time traffic. Currently we don't support multiple IDI agents to be enabled for real-time traffic at the same time. This field will be active only when Bit 0:RT_ENABLE is set to '1'
15:1	0h RO	Reserved.
0	0h RW	**Real-Time Enable (RT_ENABLE):** Global enable bit for Real-Time Support

5.9.195 B-Unit Control Register 3 (B_CR_BCTRL3)—Offset 6D7Ch

Specifies miscellaneous controls for the the B-Unit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 140h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8	1h RW	**Disable C2U Ingress Slice Anti-Starvation (SLICE_ANTI_STARVE_DISABLE):** When set, B-unit will always make an available request in each instantiated per-slice C2U Ingress FIFO for all IDI attach points eligible for arbitration in their respective odd/even sa2xclk clock. When clear, B-unit will mask a C2U Ingress Slice's available request from arbitration when SLICE_ANTI_STARVE_THRESHOLD consecutive requests has been granted for that IDI attach point from the other Slice Ingress FIFO. Has no effect for IDI attach points that do not have per-slice Ingress FIFOs
7:0	40h RW	**C2U Ingress Slice Anti-Starvation Threshold (SLICE_ANTI_STARVE_THRESHOLD):** Specifies the threshold for the number of consecutive requests B-admit arbiter will grant from the same Slice ingress FIFO for an IDI attachpoint, while the other Slice also has a request available

5.9.196 Asymmetric Memory Region 0 With No Interleaving Configuration (B_CR_ASYM_MEM_REGION0_0_0_0_MCHBAR)—Offset 6E40h

Specification of asymmetric memory region 0 (in slice 0) for the configuration with 2 asymmetric memory regions. The register has no affect is SLICE_0_MEM_DISABLED is set.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Asymmetric Region in Slice 0, With No Interleaving (SLICE0_ASYM_ENABLE):** Setting this bit to 0 disables asymmetric memory region 0; setting it to 1 enables the region.
30	0h RW	**Channel Select for ASYM Region Slice 0 (SLICE0_ASYM_CHANNEL_SELECT):** Specifies Channel Selected for ASYM Region Mapped To Slice 0
29:19	0h RW	**Limit Address for Asymmetric Memory Region, Slice 0, With No Interleaving (SLICE0_ASYM_LIMIT):** Specifies bits [38:28] of the highest address of asymmetric memory region 0 (in slice 0); all the lower bits of the region's highest address are equal to 1.
18:15	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:4	0h RW	**Base Address for Asymmetric Memory Region, Slice 0, With No Interleaving (SLICE0_ASYM_BASE):** Specifies bits [38:28] of the base address of asymmetric memory region 0 (in slice 0); all the lower bits of the region's base address are equal to 0.
3:0	0h RO	Reserved.

5.9.197 Asymmetric Memory Region 1 With No Interleaving Configuration (B_CR_ASYM_MEM_REGION1_0_0_0_MCHBAR)—Offset 6E44h

Specification of asymmetric memory region 1 (in slice 1) for the configuration with 2 asymmetric memory regions. The register has no affect is SLICE_1_DISABLED is set.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Asymmetric Region in Slice 1, With No Interleaving. (SLICE1_ASYM_ENABLE):** Setting this bit to 0 disables asymmetric memory region 1; setting it to 1 enables the region.
30	0h RW	**Channel Select for ASYM SLICE 1 (SLICE1_ASYM_CHANNEL_SELECT):** Specifies Channel Selected for ASYM Region Mapped To Slice 1.
29:19	0h RW	**Limit Address for Asymmetric Memory Region, Slice 1, With No Interleaving (SLICE1_ASYM_LIMIT):** Specifies bits [38:28] of the highest address of asymmetric memory region 1 (in slice 1); all the lower bits of the region's highest address are equal to 1.
18:15	0h RO	Reserved.
14:4	0h RW	**Base Address for Asymmetric Memory Region, Slice 1, With No Interleaving (SLICE1_ASYM_BASE):** Specifies bits [38:28] of the base address of asymmetric memory region 1 (in slice 1); all the lower bits of the region's base address are equal to 0.
3:0	0h RO	Reserved.

5.9.198 B-Unit Machine Check Mode Low (B_CR_BMCMODE_LOW)—Offset 6E48h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved (RESERVED_0):** Reserved.
0	1h RW	**Machine Check Signal Mode (MC_SIGNAL_MODE):** When set to 1, B-Unit will not allow any transaction with uncorrectable error or subsequent memory transaction to propagate through to Requester. This will essentially hang CPU and CPU will end up with IERR shutdown. Issue: When set to zero B-Unit will allow transaction with an uncorrectable error to propagate and signal MC event to CPU if enabled in IA32_MC5_CTL. If enabled MC event will be taken by CPU cores at the end of instruction boundary after it detected by ROB

5.9.199 B-Unit Machine Check Mode High (B_CR_BMCMODE_HIGH)—Offset 6E4Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved (RESERVED_0):** Reserved.

5.9.200 Two-Way Asymmetric Memory Region Configuration (B_CR_ASYM_2WAY_MEM_REGION_0_0_0_MCHBAR)—Offset 6E50h

Specification of asymmetric memory region for the configuration with 2way Interleaved Asymmetric memory. It is only supported if all Slices and all Channels are Enabled

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Two-Way Asymmetric Memory Configuration (ASYM_2WAY_INTERLEAVE_ENABLE):** Setting this bit to 0 disables 2Way Asymmetric Interleaving; setting it to 1 enables the region.
30:28	0h RO	Reserved.
27:17	0h RW	**Limit Address for Two-Way Asymmetric Memory Region (ASYM_2WAY_LIMIT):** Specifies bits [38:28] of the highest address of Interleave Asymmetric Region; all the lower bits of the region's highest address are equal to 1.
16:15	0h RO	Reserved.
14:4	0h RW	**Base Address for Two-Way Asymmetric Memory Region (ASYM_2WAY_BASE):** Specifies bits [38:28] of the base address of Interleave Asymmetric Region; all the lower bits of the region's base address are equal to 0.
3:2	0h RW	**Two-Way Asymmetric Interleave Mode (ASYM_2WAY_INTLV_MODE):** Going with 2 bits here. 2'b00 : Asymmetric memory Split between Channel 0 of Slice 0 and Slice 1 2'b01 : Asymmetric memory split between Channel 1 of Slice 0 and Slice 1 2'b10 : Asymmetric memory split between Channel 0 and Channel 1 of Slice 0 2'b11 : Asymmetric memory split between Channel 0 and Channel 1 of Slice 1
1:0	0h RO	Reserved.

5.10 Registers Summary

Table 5-10. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
7800h	7803h	Interrupt Redirection Control (INTR_REDIR_CTL_MCHBAR)—Offset 7800h	150000h
7804h	7807h	X2B_BARB_CTL1 (X2B_BARB_CTL1_MCHBAR)—Offset 7804h	0h
7808h	780Bh	Clock Gating Control (CLKGATE_CTL_MCHBAR)—Offset 7808h	0h
780Ch	780Fh	Miscellaneous Controls (MISC_CTL_MCHBAR)—Offset 780Ch	0h
7810h	7813h	Control (CTL_MCHBAR)—Offset 7810h	4B000000h
7814h	7817h	PSMI Control (PSMI_CTL_MCHBAR)—Offset 7814h	0h
7818h	781Bh	Miscellaneous T2A selector (T2A_SELECTOR_MISC_MCHBAR)—Offset 7818h	38000AA0h
781Ch	781Fh	VC Read Ordering CFG (VC_READ_ORDERING_CFG_MCHBAR)—Offset 781Ch	F9F3h
7820h	7823h	VC Write Ordering CFG (VC_WRITE_ORDERING_CFG_MCHBAR)—Offset 7820h	F9F3h

Table 5-10. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
7824h	7827h	IDI0 C2U Credit Control (IDI0_C2U_CREDIT_CTRL_MCHBAR)—Offset 7824h	6104h
7828h	782Bh	IDI1 C2U Credit Control (IDI1_C2U_CREDIT_CTRL_MCHBAR)—Offset 7828h	6104h
782Ch	782Fh	IDI2 C2U Credit Control (IDI2_C2U_CREDIT_CTRL_MCHBAR)—Offset 782Ch	A290h
7830h	7833h	IDI3 C2U Credit Control (IDI3_C2U_CREDIT_CTRL_MCHBAR)—Offset 7830h	0h
7834h	7837h	IDI4 C2U Credit Control (IDI4_C2U_CREDIT_CTRL_MCHBAR)—Offset 7834h	0h
7838h	783Bh	IDI5 C2U Credit Control (IDI5_C2U_CREDIT_CTRL_MCHBAR)—Offset 7838h	0h
783Ch	783Fh	IDI6 C2U Credit Control (IDI6_C2U_CREDIT_CTRL_MCHBAR)—Offset 783Ch	0h
7840h	7843h	IDI7 C2U Credit Control (IDI7_C2U_CREDIT_CTRL_MCHBAR)—Offset 7840h	0h
7844h	7847h	PII2 A2T Credit Control (PII2_A2T_CREDIT_CTRL_MCHBAR)—Offset 7844h	808h
7848h	784Fh	BIOSWR Control Policy (T_CR_BIOSWR_CP_0_0_0_MCHBAR)—Offset 7848h	C0061010202h
7850h	7857h	BIOSWR Read Access Control (T_CR_BIOSWR_RAC_0_0_0_MCHBAR)—Offset 7850h	80000C00630D0217h
7858h	785Fh	BIOSWR Write Access Control (T_CR_BIOSWR_WAC_0_0_0_MCHBAR)—Offset 7858h	C00610C0212h
7860h	7867h	TUnit Pcode/Ucode Write, All Read Control Policy Register (T_CR_P_U_CODEWR_ALLRD_CP_0_0_0_MCHBAR)—Offset 7860h	40001000202h
7868h	786Fh	TUnit Pcode/Ucode Read Access Control (T_CR_P_U_CODEWR_ALLRD_RAC_0_0_0_MCHBAR)—Offset 7868h	FFFFFFFFFFFFFFFFh
7870h	7877h	TUnit Pcode/Ucode Write Access Control (T_CR_P_U_CODEWR_ALLRD_WAC_0_0_0_MCHBAR)—Offset 7870h	40801008602h

5.10.1 Interrupt Redirection Control (INTR_REDIR_CTL_MCHBAR)—Offset 7800h

Interrupt redirection control.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 150000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved 2 (RESERVED_2):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**INTPRIUP Gap DIS (INTPRIUP_GAP_DIS):** When the T-unit receives the data for intpriupdate IDI transaction, if the data specifies legacy clustered mode, then the T-Unit will assume there is a gap in the logical apic id field, such that: cluster_id[3:0] == logical_id[19:16] and agent_id[3:0] == logical_id[3:0]. These two fields are stored without a gap in the T-Unit CRs. If this CR bit is a one, then T-Unit will not assume a gap in the incoming data, and will just use the lower 8 bits of logical_id for the legacy cluster case.
20	1h RW	**INTPRIUP Enable (INTPRIUP_EN):** Enable an intpriupdate IDI transaction to modify the corresponding core's enable bit, physical APIC ID, and logical APIC ID.
19	0h RW	**INTPRIUP DFR CF (INTPRIUP_DFR_CF):** Enable an intpriupdate IDI transaction to modify the destination format bit (dt/dfr), which is common to all cores, if the core's APIC enable bit is set in the transaction data.
18	1h RW	**INTPRIUP DFR Enable (INTPRIUP_DFR_EN):** Enable an intpriupdate IDI transaction to modify the destination format bit (dt/dfr), which is common to all cores.
17	0h RW	**INTPRIUP X2APIC CF (INTPRIUP_X2APIC_CF):** Enable an intpriupdate IDI transaction to modify the extended APIC mode bit, which is common to all cores, if the core's APIC enable bit is set in the transaction data.
16	1h RW	**INTPRIUP X2APIC Enable (INTPRIUP_X2APIC_EN):** Enable an intpriupdate IDI transaction to modify the extended APIC mode bit, which is common to all cores.
15:9	0h RO	**Reserved 1 (RESERVED_1):** Reserved.
8:6	0h RW	**Hash Vector (HASH_VECTOR):** Not supported. Vector-based interrupt redirection control: • 000: Select bits 7:4/5:4 for vector cluster/flat algorithm; • 001: Select bits 6:3/4:3; • 010: Select bits 4:1/2:1; • 011: Select bits 3:0/1:0; • Others: Reserved.
5:4	0h RO	**Reserved 0 (RESERVED_0):** Reserved.
3	0h RW	**Cluster DESTFX DIS (CLUSTER_DESTFX_DIS):** When doing redirection on a logical cluster mode interrupt with a cluster id of all ones, the default is zero.
2:0	0h RW	**Redirection Mode Select (REDIR_MODE_SEL):** Redirection Mode Select for Logical Interrupts: • 000: Fixed priority • 001: Round robin • 100: PAIR Power Aware Interrupt Redirection w/ Fixed priority

5.10.2 X2B_BARB_CTL1 (X2B_BARB_CTL1_MCHBAR)—Offset 7804h

Various weights for the X2B data arbiter.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved 1 (RESERVED_1):** Reserved.
23:22	0h RW	**IDI7 Write Data Weight (IDI7_WRITE_DATA_WEIGHT):** IDI Attach Point 7 Write Data Weight only exists if this IDI attach exists.
21:20	0h RW	**IDI6 Write Data Weight (IDI6_WRITE_DATA_WEIGHT):** IDI Attach Point 6 Write Data Weight only exists if this IDI attach exists.
19:18	0h RW	**IDI5 Write Data Weight (IDI5_WRITE_DATA_WEIGHT):** IDI Attach Point 5 Write Data Weight only exists if this IDI attach exists.
17:16	0h RW	**IDI4 Write Data Weight (IDI4_WRITE_DATA_WEIGHT):** IDI Attach Point 4 Write Data Weight only exists if this IDI attach exists.
15:14	0h RW	**IDI3 Write Data Weight (IDI3_WRITE_DATA_WEIGHT):** IDI Attach Point 3 Write Data Weight only exists if this IDI attach exists.
13:12	0h RW	**IDI2 Write Data Weight (IDI2_WRITE_DATA_WEIGHT):** IDI Attach Point 2 Write Data Weight only exists if this IDI attach exists.
11:10	0h RW	**IDI1 Write Data Weight (IDI1_WRITE_DATA_WEIGHT):** IDI Attach Point 1 Write Data Weight only exists if this IDI attach exists.
9:8	0h RW	**IDI0 Write Data Weight (IDI0_WRITE_DATA_WEIGHT):** IDI Attach Point 0 Write Data Weight only exists if this IDI attach exists.
7:2	0h RO	**Reserved 0 (RESERVED_0):** Reserved.
1:0	0h RW	**PII2 Read Data Completion Weight (PII2_READ_DATA_COMP_WEIGHT)**

5.10.3 Clock Gating Control (CLKGATE_CTL_MCHBAR)—Offset 7808h

Each bit controls a separate Clock Gating Domain. BIOS should write all bits in this register to 1.

- 0: Overrides clock gating and forces the clock gating domain to behave like a freerunning clock.
- 1: Enables Clock Gating.

The reset value for this register is controlled by an SA strap. SOCs can tie this strap to a constant, a fuse or an output from another unit. NOTE: This has to be revisited for the new PND2 T-Unit structure clock gating control.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved 8 (RESERVED_8):** Reserved.
30	0h RO	**Reserved 7 (RESERVED_7):** Reserved.
29	0h RO	**Reserved 6 (RESERVED_6):** Reserved.
28	0h RO	**Reserved 5 (RESERVED_5):** Reserved.
27	0h RO	**Reserved 4 (RESERVED_4):** Reserved.
26	0h RO	**Reserved 3 (RESERVED_3):** Reserved.
25	0h RW	**IDI_U2C_CRDT_CNT_CLK_GATE_EN (IDI_U2C_CRDT_CNT_CLK_GATE_EN):** IDI U2C Credit Counters Clock Gate Enable
24	0h RW	**BT_FREE_CLK_GATE_EN (BT_FREE_CLK_GATE_EN):** BT Free Clock Gate Enable
23	0h RW	**Monitor Logic Clock Gate Enable (MON_LOG_CLK_GATE_EN)**
22	0h RW	**A2T Queue Clock Gate Enable (A2T_Q_CLK_GATE_EN)**
21	0h RW	**T2A Queue Clock Gate Enable (T2A_Q_CLK_GATE_EN):** T2A queue clock gate enable. NOTE: Need both request and writepull.
20	0h RW	**A2TAPIC Clock Gate Enable (A2TAPIC_CLK_GATE_EN)**
19	0h RW	**B2X Data Selector Clock Gate Enable (B2X_DATSEL_CLK_GATE_EN)**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**X2B Data Selector Clock Gate Enable (X2B_DATSEL_CLK_GATE_EN)**
17	0h RW	**U2C Response Selector Clock Gate Enable (U2C_RESP_SEL_CLK_GATE_EN)**
16	0h RW	**T2A Request Selector Clock Gate Enable (T2A_REQ_SEL_CLK_GATE_EN)**
15	0h RW	**C2APIC FIFO Clock Gate Enable (C2APIC_FIFO_CLK_GATE_EN)**
14	0h RW	**U2C Request FIFO Clock Gate Enable (U2C_REQ_FIFO_CLK_GATE_EN):** NOTE: This should be the U2C request shim.
13	0h RW	**U2C Request Selector Clock Gate Enable (U2C_REQ_SEL_CLK_GATE_EN):** NOTE: Need per slice enable.
12	0h RW	**Upstream Ordering Block Clock Gate Enable (UOB_CLK_GATE_EN)**
11	0h RW	**Tracker Scoreboard Oldest Clock Gate Enable (TRKR_SB_OLDST_CLK_GATE_EN):** Tracker Scoreboard oldest of available queue clock gate enable.
10	0h RW	**Tracker Scoreboard U2C Response Status Clock Gate Enable (TRK_SCBD_U2C_RSP_STAT_CLK_GATE_EN)**
9	0h RW	**Tracker Scoreboard T2A Request Status Clock Gate Enable (TRKR_SB_T2A_REQSTAT_CLK_GATE_EN)**
8	0h RW	**Tracker Scoreboard B2X Data Status Clock Gate Enable (TRKR_SB_B2X_DATSTAT_CLK_GATE_EN)**
7	0h RW	**Tracker Scoreboard Write Status Clock Gate Enable (TRKR_SB_WRSTAT_CLK_GATE_EN)**
6	0h RW	**Tracker Scoreboard Snoop Status Clock Gate Enable (TRKR_SB_SNP_STAT_CLK_GATE_EN)**
5	0h RW	**Tracker Scoreboard Request Clock Gate Enable (TRKR_SB_REQ_CLK_GATE_EN)**
4	0h RW	**Tracker Scoreboard Violation Clock Gate Enable (TRKR_SB_VIOL_CLK_GATE_EN)**
3	0h RW	**Tracker Scoreboard Valid Clock Gate Enable (TRKR_SB_VALID_CLK_GATE_EN)**
2	0h RW	**Tracker Scoreboard Clock Gate Enable (TRKR_SB_CLK_GATE_EN)**
1	0h RW	**IOSF SB Config Register Clock Gate Enable (IOSF_SB_CFG_REG_CLK_GATE_EN)**
0	0h RW	**IOSF SB Message Clock Gate Enable (IOSF_SB_MSG_CLK_GATE_EN)**

5.10.4 Miscellaneous Controls (MISC_CTL_MCHBAR)—Offset 780Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:24	0h RO/V	**Snoop Ready Vector (SNP_RDY_VEC):** Allows Debug to dynamically read this state in the T-Unit.
23:19	0h RO	Reserved.
18:16	0h RO/V	**Snoop Required Vector (SNP_REQ_VEC):** Allows Debug to dynamically read this state in the T-Unit.
15	0h RW	**C2U Data Tracking Disabled (C2U_DATA_TRACK_DIS):** When set, this bit disables the tracking of c2u_data for IDI shutdown qualification. A stop_idi sideband request requires that T-unit drain all u2c requests, and wait for all outstanding c2u responses and c2u data to return, before responding with the u2c_done sideband message to GLM. The bug was that T-unit was not waiting on c2u_data.
14	0h RO	**IWB_FORWARDING_EN (IWB_FORWARDING_EN):** When an IWB comes into to B-unit, let it write the BRAM, even if the btag entry is locked waiting on the memory read return. Also, once written into the BRAM, let the tub2xdata logic consider the ooaq entry as ready to receive data. These two allowances will forward the IWB data to the requestor, without waiting on the memory read return.
13:12	0h RW	**Spare 2 (SPARE2):** Spare bits for hardware.
11:7	0h RW	**Spare (SPARE):** Readable and Writable Spare bits. SPARE[0] has been consumed. It is used by PCODE to bypass IDI_SHUTDOWN detection and will force IDI CSM FSM indicator to 1 for pgcb/idle detection.
6	0h RW	**GO-ACK FIFO Empty Check Disable (GO_ACK_FIFO_EMPTY_CHECK_DIS):** When set, the T-unit will NOT wait for the per-agent GO-ACK FIFO to be empty before accepting a stopidi request from the associated agent.
5	0h RW	**IDI_SHUTDOWN Bypass (IDI_SHUTDOWN_BYP):** Used by PCODE to bypass IDI_SHUTDOWN detection and will force IDI CSM FSM indicator to 1 for pgcb/idle detection.

Bit Range	Default & Access	Field Name (ID): Description
4:1	0h RW	**DPTE Count (DPTE_CNT):** This field controls the number of cycles between sending Dynamic Prefetch Throttle Update Events to each IDI Attach Point. The 4-bit value in this field is N and the Count is 2 to the Nth power. • 0: T-Unit can send a DPTE every cycle. • 1: T-Unit can send a DPTE every 2 cycles. • 2: T-Unit can send a DPTE every 4 cycles. • 3: T-Unit can send a DPTE every 8 cycles. • 4: T-Unit can send a DPTE every 16 cycles. • 15: T-Unit can send a DPTE every 32768 cycles.
0	0h RW	**DPTE Enable (DPTE_EN):** • 0: Dynamic Prefetch Throttle Events are Disabled. • 1: Dynamic Prefetch Throttle Events are Enabled.

5.10.5 Control (CTL_MCHBAR)—Offset 7810h

Control register for various T-Unit knobs.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4B000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved 1 (RESERVED_1):** Reserved.
30	1h RW	**ISOCH_BW_FIX_DIS (ISOCH_BW_FIX_DIS):** Disable A-Unit blocking snooped traffic during IA/GT P-state transitions.
29:24	Bh RW	**ISOCH Shared Reserve (ISOCH_SHARED_RESV):** The number of shared T2A cmd credits to reserve for ISOCH level traffic.
23:22	0h RO	**Reserved 0 (RESERVED_0):** Reserved R/W bits.
21	0h RW	**Use PIC_End NACK (USE_PIC_END_NACK):** Normally, when GLM asserts pm_block_req and interrupt_ready is cleared, T-Unit finishes any active interrupt and then responds back with pic_end. For VLW and LTWrites, which are broadcast interrupts, this bit allows an alternative protocol, in which T-unit sees a VLW or LTWrite active in the apic pipeline, and responds with pic_end_nack instead or pic_end. This tells GLM to not go to sleep, so that all cores will eventually be awake and T-Unit can deliver the broadcast interrupt. This bit is not meant to be used, because normally VLW and LTWrites will go into the piclet. Only use this bit if you have special knowledge.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Disable Snooping GT (DISABLE_SNOOPING_GT):** • 0: Default. Snoop GT as normal. • 1: Never snoop GT for any access from an agent.
19	0h RW	**Disable Opportunistic Slice 1 Schedule (DISABLE_OPPORTUNISTIC_SLICE1_SCHEDULE):** • 0: Default. Global B2X data selector will opportunistically schedule TSlice1 B2X selected data in the odd cycle if TSlice0 B2X selected data is not available. • 1: Global B2X data selector will always schedule TSlice1 B2X selected data only in the even cycle.
18	0h RW	**Disable IOSF High Priority Read Data Return (DISABLE_ISOC_HIGHPRI_RDDATA_RETURN):** Disables IOSF high priority read data returns and treats all read data scheduling as normal priority.
17	0h RW	**Enable NPC Collector (ENABLE_NPC_COLLECTOR):** This bit is not connected to anything.
16	0h RW	**Enable In Order APIC (ENABLE_IN_ORDER_APIC):** When 0, has no affect; When 1, forces all interrupts to bypass the piclets, and wait until all targeted cores are awake before delivering the interrupt. The APIC block will send int_wake to P-Unit for each targeted core. Note that using this bit could cause deadlock.
15	0h RW	**TG Enable High Priority Write Pulls (TG_HIGHPRI_WRITE_PULLS):** Enable High Priority Write Pulls. When 1 the X2B Data Selector will prioritize write pulls that the B-Unit has flagged as high priority over other write pulls.
14	0h RW	**TG Disable Live BRAM Bypass to PII2 (TG_LIVE_DATA_PII2):** Disable Live BRAM Bypass to PII2 Mode. When 1 all data to PII2 Agents will be returned from reading the BRAM.
13	0h RW	**TG Half Tunnel (TG_HALF_TUNNEL):** Enable IDI Half Tunneling. This should only be enabled in an Intel Debug setting on Dual Core SOCs.
12	0h RW	**TG Disable nonDRAM Snoops (TG_NDRAMSNP):** Disable nonDRAM Snoops. • 0: SA will snoop nonDRAM Memory Addresses, including Memory Mapped IO MMIO and Memory Mapped Enhanced Config Space. • 1: SA will not snoop nonDRAM Memory Addresses. This includes the standard Memory Read/Write opcodes as well as SetMonitor. There is one exception since the SA will always issue Snoop Invalidate for CLFlush opcodes even if the address is not DRAM. Note: the Monitor Logic can still be armed and triggered using a nonDRAM address.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**TG Read Data BW Mode (TG_RD_BW_MODE):** Read Data BW Mode. This Configuration Mode only affects behavior on SOCs that support two 64bit DDR3 Channels. For these SOCs this mode bit performs the following function: • 0: Enhanced Read BW mode for 2x64b DDR3 Channels. • 1: Basic Read BW mode. All other SOCs this mode bit performs the following function: • 0: Basic Read BW mode. • 1: Reserved.
10	0h RW	**TG Disable Downstream Posted Push Logic Mode (TG_DW_POST_PUSH_LOG):** Disable Downstream Posted Push Logic Mode. • 0: DRAM Read Completions to IOSF VC0 are stalled in the BRAM until all prior downstream Posted Requests from IDI are pushed into the Aunit. This ensures proper PCI Producer/ Consumer Ordering Rules. • 1: Disables the Posted Push Logic. Note this mode violates the Producer/Consumer Ordering rules.
9	0h RW	**TG Set Monitor Snoop Configuration (TG_MON_SNP_CFG):** Set Monitor Snoop Configuration. Defines the Snoop opcode that will be sent for Set Monitor requests from IDI Agents: • 0:SnpCode default • 1:SnpInv
8	0h RW	**Broadcast APIC (BCAST_APIC):** Broadcast APIC Mode. When 1 T-Unit will wake up all IDI attach points and broadcast APIC messages to all attach points not just the IDI attach points that needs to receive the APIC message. Note: The T-Unit does not change the APIC ID to the broadcast APIC ID. What is meant by Broadcast is the Interrupt message is sent to all IDI Attach Points. For directed interrupts the directed interrupt is sent to all Attach Points with the unmodified APIC ID. For redirected interrupts the T-Unit performs the standard redirection algorithm fixed roundrobin or PAIR selects 1 APIC ID to send the message but then sends the message to all IDI Attach Points.
7	0h RW	**SnpInv (SNPINV):** SnpInv only when 1 T-Unit will only send SnpInv. This disables all other Snoop types e.g. SnpCode SnpData.
6	0h RW	**UC Code Read Snoop Configuration (UC_CODE_RD_CFG):** Code Read Snoop Configuration. The SA will send the following U2C Request for Code Reads from IDI Agents. • 0: SnpCode default. • 1: SnpInv.

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**PII2 Snooped Read (PII2_SNP_RD):** PII2 Snooped Read Configuration. The SA will send the following U2C Request for Snooped Reads from PII2 Agents. • 00b: Reserved. • 01b: SnpCode. • 10b: SnpData. • 11b: SnpInv default. Note: In order to use SnpCode or SnpData the B-Unit must be configured to disable the Owned Feature.
3	0h RW	**Always Snoop IDI Requests (ALWAYS_SNP_IDI):** IDI initiated requests will always be snooped even if Selfsnoop is not set and even if a Snoop Filter indicates no need to snoop.
2	0h RW	**Disable Live BRAM Bypass to IDI (DIS_LIVE_BRAM_BYP_IDI):** Disable Live BRAM Bypass to IDI Mode. When 1 all data to IDI Agents will be returned from reading the BRAM.
1	0h RW	**Outstanding Snoop (OUTSTND_SNP):** 1: Outstanding Snoop Mode. When 1, do not send any snoops if there is an outstanding Snoop from an IDI Read or Write to ECAM memory mapped Config space that has not yet received all Snoop Replies. Also, do not send any snoops if there is an outstanding Snoop from an IDI Read to MMIO that has not yet received all Snoop Replies. For all other IDI Requests, do not send any snoops if there is an outstanding Snoop that has not yet been GOed. Note: This mode does not affect the issuance of U2C Requests that are destined to the Core APICs i.e. DPTEvent IntLog IntPhy VLW LTWrite and MIscEvent. It only affects the issuance of SnpCode, SnpData, and SnpInv.
0	0h RW	**Always Snoop PII2 Requests (ALWAYS_SNP_PII2):** Always Snoop PII2 Requests Mode. Before setting this bit note the following: There is a performance optimization in the B-Unit to allow multiple Snooped Writes from PII2 Agents to the same line. The B-Unit converts all but the 1st Snoop Write to be NonSnooped. Because of this, the Snoop Everything Mode should only be enabled if 1 of the following is true: T-Unit 1 Outstanding Snoop Mode is enabled OR B-Unit has been configured to disable request combining. Even when this mode is enabled the T-Unit will never snoop Memory Requests that map to MMIO from a PII2 Agent. These requests are treated as IMR violations and also the snoop is suppressed.

5.10.6 PSMI Control (PSMI_CTL_MCHBAR)—Offset 7814h

PSMI Control register. NOTE: This register needs to be redefined for SA PSMI on the SoC.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved 2 (RESERVED_2):** Reserved.
7	0h RO	**Reserved 1 (RESERVED_1):** Reserved.
6:5	0h RW	**Select IDI Attach Point (SEL_IDI_ATTACH):** Selects IDI Attach Point. i.e. Module to capture/replay. • 00b: IDI Attach Point 0 • 01b: IDI Attach Point 1 • 10b: Reserved • 11b: Reserved
4:3	0h RW	**PSMI Gear Ratio (PSMI_GEAR_RATIO):** PSMI Gear Ratio Select. • 00b: IDI transfers can occur every CZclock default • 01b: IDI transfers can occur every 2 CZclocks • 10b: IDI transfers can occur every 4 CZclocks • 11b: IDI transfers can occur every 8 CZclocks
2	0h RO	**Reserved (RESERVED_0):** Reserved.
1	0h RW	**PSMI Replay Mode (PSMI_REPLAY_MODE)**
0	0h RW	**SA Capture Mode (SA_CAPTURE_MODE):** Note: If SA Capture Mode is enabled then SSA Replay Mode and P-Unit Replay Mode are ignored.

5.10.7 Miscellaneous T2A selector (T2A_SELECTOR_MISC_MCHBAR)—Offset 7818h

This register will provide miscellaneous defeatures and controls for the T2A selector downstream block in the T-Unit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 38000AA0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	38h RW	**PII_IDLE_THRESHOLD (PII_IDLE_THRESHOLD):** Number of 1x cycles that BT-unit PII idle conditions should exist before the ISM requests idle. The restart time of PII BGFs is on the order of 150 to 210 ns. To avoid this penalty, idle should not be entered too quickly.

Bit Range	Default & Access	Field Name (ID): Description
23:13	0h RW	**Spare 1 (Spare1):** Spare register bits for read/write.
12:9	5h RW	**Maximum Downstream Nonposted Requests Issued For VC0b (MAX_DS_NP_VC0B):** Maximum number of downstream nonposted requests the T2A selector can issue for VC0b. This value should be programmed to less than or equal to the MAX_DS_NP field value but hardware will cap it at that value regardless.
8:5	5h RW	**Maximum Downstream Nonposted Requests Issued For VC0a (MAX_DS_NP_VC0A):** Maximum number of downstream nonposted requests the T2A selector can issue for VC0a. This value should be programmed to less than or equal to the MAX_DS_NP field value but hardware will cap it at that value regardless.
4:0	0h RW	**Spare 0 (Spare0):** Spare register bits for read/write.

5.10.8 VC Read Ordering CFG (VC_READ_ORDERING_CFG_MCHBAR)—Offset 781Ch

Register that indicates whether a particular B2T agent ID is configured to be inorder 1 or can be outoforder 0 for read accesses. This is will cause the access to be routed through the upstream ordering block value of 1 in the VCs bit or not value of 0 in the VCs bit. This register is not meant to be a dynamic ability to change inorder/outoforder nature and should be programmed by BIOS before devices are allowed to access memory. Note that reset value should work without a write. The IDI attaches are not upstream VCs or subject to the Upstream Ordering Block but to keep the handling generic bits will be hardwired to 0 for each IDI attach in the system.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: F9F3h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved 0 (RESERVED_0):** Reserved for future VC growth.
15	1h RW	**UPSTREAM_VC15 (UPSTREAM_VC15_IN_ORDER):** Configuration bit for upstream VC15 inorder read handling. 1 indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.
14	1h RW	**UPSTREAM_VC14 (UPSTREAM_VC14_IN_ORDER):** Configuration bit for upstream VC14 inorder read handling. 1 indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.

Bit Range	Default & Access	Field Name (ID): Description
13	1h RW	**UPSTREAM_VC13 (UPSTREAM_VC13_IN_ORDER):** Configuration bit for upstream VC13 inorder read handling. 1 indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.
12	1h RW	**UPSTREAM_VC12 (UPSTREAM_VC12_IN_ORDER):** Configuration bit for upstream VC12 inorder read handling. 1 indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.
11	1h RW	**UPSTREAM_VC11 (UPSTREAM_VC11_IN_ORDER):** Configuration bit for upstream VC11 inorder read handling. 1 indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.
10	0h RW	**UPSTREAM_VC1BMMU_IN_ORDER (UPSTREAM_VC1BMMU_IN_ORDER):** Configuration bit for upstream VC1Bmmus inorder read handling. 1 indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.
9	0h RW	**UPSTREAM_VC0BMMU_IN_ORDER (UPSTREAM_VC0BMMU_IN_ORDER):** Configuration bit for upstream VC0Bmmus inorder read handling. 1 indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.
8	1h RW	**UPSTREAM_VC0AMMU_IN_ORDER (UPSTREAM_VC0AMMU_IN_ORDER):** Configuration bit for upstream VC0Ammus inorder read handling. 1 indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.
7	1h RW	**Upstream VCBR In Order (UPSTREAM_VCBR_IN_ORDER):** Configuration bit for upstream VCbrs inorder read handling. • 1: Indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block • 0: Indicates that it is an outoforder VC
6	1h RW	**Upstream VC2C In Order (UPSTREAM_VC2C_IN_ORDER):** Configuration bit for upstream VC2cs inorder read handling. • 1: Indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block • 0: Indicates that it is an outoforder VC
5	1h RW	**Upstream VC2B In Order (UPSTREAM_VC2B_IN_ORDER):** Configuration bit for upstream VC2bs inorder read handling. • 1: Indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block • 0: Indicates that it is an outoforder VC
4	1h RW	**Upstream VC2A In Order (UPSTREAM_VC2A_IN_ORDER):** Configuration bit for upstream VC2as inorder read handling. • 1 indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block. • 0 indicates that it is an outoforder VC.
3	0h RW	**Upstream VC1B In Order (UPSTREAM_VC1B_IN_ORDER):** Configuration bit for upstream VC1bs inorder read handling. • 1 indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block. • 0 indicates that it is an outoforder VC.
2	0h RW	**Upstream VC1A In Order (UPSTREAM_VC1A_IN_ORDER):** Configuration bit for upstream VC1as inorder read handling. • 1 indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block. • 0 indicates that it is an outoforder VC.
1	1h RW	**Upstream VC0B In Order (UPSTREAM_VC0B_IN_ORDER):** Configuration bit for upstream VC0bs inorder read handling. • 1 indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block. • 0 indicates that it is an outoforder VC.

Bit Range	Default & Access	Field Name (ID): Description
0	1h RW	**Upstream VC0A In Order (UPSTREAM_VC0A_IN_ORDER):** Configuration bit for upstream VC0as inorder read handling. • 1 indicates that it is an inorder VC and reads must be handled by the Upstream Ordering Block. • 0 indicates that it is an outoforder VC.

5.10.9 VC Write Ordering CFG (VC_WRITE_ORDERING_CFG_MCHBAR)—Offset 7820h

Register that indicates whether a particular B2T agent ID is configured to be inorder 1 or can be outoforder 0 for write accesses. This is will cause the access to be routed through the upstream ordering block value of 1 in the VCs bit or not value of 0 in the VCs bit. This register is not meant to be a dynamic ability to change inorder/outoforder nature and should be programmed by BIOS before devices are allowed to access memory note that reset value should work without a write. The IDI attaches are not upstream VCs or subject to the Upstream Ordering Block but to keep the handling generic bits will be hardwired to 0 for each IDI attach in the system.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: F9F3h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved 0 (RESERVED_0):** Reserved for future VC growth.
15	1h RW	**UPSTREAM_VC15 (UPSTREAM_VC15_IN_ORDER):** Configuration bit for upstream VC15 inorder write handling. 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.
14	1h RW	**UPSTREAM_VC14 (UPSTREAM_VC14_IN_ORDER):** Configuration bit for upstream VC14 inorder write handling. 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.
13	1h RW	**UPSTREAM_VC13 (UPSTREAM_VC13_IN_ORDER):** Configuration bit for upstream VC13 inorder write handling. 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.
12	1h RW	**UPSTREAM_VC12 (UPSTREAM_VC12_IN_ORDER):** Configuration bit for upstream VC12 inorder write handling. 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**UPSTREAM_VC11 (UPSTREAM_VC11_IN_ORDER):** Configuration bit for upstream VC11 inorder write handling. 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.
10	0h RW	**UPSTREAM_VC1BMMU_IN_ORDER (UPSTREAM_VC1BMMU_IN_ORDER):** Configuration bit for upstream VC1Bmmus inorder write handling. 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.
9	0h RW	**UPSTREAM_VC0BMMU_IN_ORDER (UPSTREAM_VC0BMMU_IN_ORDER):** Configuration bit for upstream VC0Bmmus inorder write handling. 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. 0 indicates that it is an outoforder VC.
8	1h RW	**Upstream VC0MMU In Order (UPSTREAM_VC0AMMU_IN_ORDER):** Configuration bit for upstream VC0mmus inorder write handling. • 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. • 0 indicates that it is an outoforder VC.
7	1h RW	**Upstream VCBR In Order (UPSTREAM_VCBR_IN_ORDER):** Configuration bit for upstream VCbrs inorder write handling. • 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. • 0 indicates that it is an outoforder VC.
6	1h RW	**Upstream VC2C In Order (UPSTREAM_VC2C_IN_ORDER):** Configuration bit for upstream VC2cs inorder write handling. • 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. • 0 indicates that it is an outoforder VC.
5	1h RW	**Upstream VC2B In Order (UPSTREAM_VC2B_IN_ORDER):** Configuration bit for upstream VC2bs inorder write handling. • 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. • 0 indicates that it is an outoforder VC.
4	1h RW	**Upstream VC2A In Order (UPSTREAM_VC2A_IN_ORDER):** Configuration bit for upstream VC2as inorder write handling. • 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. • 0 indicates that it is an outoforder VC.
3	0h RW	**Upstream VC1B In Order (UPSTREAM_VC1B_IN_ORDER):** Configuration bit for upstream VC1bs inorder write handling. • 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. • 0 indicates that it is an outoforder VC.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Upstream VC1A In Order (UPSTREAM_VC1A_IN_ORDER):** Configuration bit for upstream VC1as inorder write handling. • 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. • 0 indicates that it is an outoforder VC.
1	1h RW	**Upstream VC0B In Order (UPSTREAM_VC0B_IN_ORDER):** Configuration bit for upstream VC0bs inorder write handling. • 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. • 0 indicates that it is an outoforder VC.
0	1h RW	**Upstream VC0A In Order (UPSTREAM_VC0A_IN_ORDER):** Configuration bit for upstream VC0as inorder write handling. • 1 indicates that it is an inorder VC and writes must be handled by the Upstream Ordering Block. • 0 indicates that it is an outoforder VC.

5.10.10 IDI0 C2U Credit Control (IDI0_C2U_CREDIT_CTRL_MCHBAR)—Offset 7824h

This register will provide the number of credits that IDI C2U channels should be initialized to and other control mechanisms around IDI start/stop flows. A register will be provided per IDI attach to allow for individual IDI tuning. This register will be for the agent attached to IDI0.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6104h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved 0 (RESERVED_0):** Reserved.
17:12	6h RW	**IDI IA C2U Data Credit Initialization (IDI_IA_C2U_DATA_CREDIT_INIT):** This register is the number of credits to initialize C2U data credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress data queue size in B-Unit. This provides an ability to limit data credits at the next IDI start request change will only take place after the next IDI start request. The default value of this register should work out of reset.

Bit Range	Default & Access	Field Name (ID): Description
11:6	4h RW	**IDI IA C2U Response Credit Initialization (IDI_IA_C2U_RSP_CREDIT_INIT):** This register is the number of credits to initialize C2U response credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U response shim ingress queue size in T-Unit. This provides an ability to limit response credits at the next IDI start request. Change will only take place after next IDI start request. The default value of this register should work out of reset.
5:0	4h RW	**IDI IA C2U Request Credit Initialization (IDI_IA_C2U_REQ_CREDIT_INIT):** This register is the number of credits to initialize C2U requests credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress queue size in Badmit. This provides an ability to limit request credits at the next IDI start request. Change will only take place after next IDI start request. The default value of this register should work out of reset.

5.10.11 IDI1 C2U Credit Control (IDI1_C2U_CREDIT_CTRL_MCHBAR)—Offset 7828h

This register will provide the number of credits that IDI C2U channels should be initialized to and other control mechanisms around IDI start/stop flows. A register will be provided per IDI attach to allow for individual IDI tuning. This register will be for the agent attached to IDI1.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6104h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved 0 (RESERVED_0):** Reserved
17:12	6h RW	**IDI IA C2U Data Credit Initialization (IDI_IA_C2U_DATA_CREDIT_INIT):** This register is the number of credits to initialize C2U data credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress data queue size in B-Unit. This provides an ability to limit data credits at the next IDI start request. Change will only take place after next IDI start request. The default value of this register should work out of reset.

Bit Range	Default & Access	Field Name (ID): Description
11:6	4h RW	**IDI IA C2U Response Credit Initialization (IDI_IA_C2U_RSP_CREDIT_INIT):** This bit field contains the number of credits to initialize C2U response credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U response shim ingress queue size in T-Unit. This provides an ability to limit response credits at the next IDI start request. Change will only take place after next IDI start request. The default value of this register should work out of reset.
5:0	4h RW	**IDI IA C2U Request Credit Initialization (IDI_IA_C2U_REQ_CREDIT_INIT):** This register is the number of credits to initialize C2U requests credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress queue size in Badmit. This provides an ability to limit request credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.

5.10.12 IDI2 C2U Credit Control (IDI2_C2U_CREDIT_CTRL_MCHBAR)—Offset 782Ch

This register will provide the number of credits that IDI C2U channels should be initialized to and other control mechanisms around IDI start / stop flows. A register will be provided per IDI attach to allow for individual IDI tuning. This register will be for the agent attached to IDI2.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: A290h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved 0 (RESERVED_0):** Reserved
17:12	Ah RW	**IDI C2U Data Credit Initialization (IDI_C2U_DATA_CREDIT_INIT):** This register is the number of credits to initialize C2U data credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress data queue size in B-Unit. This provides an ability to limit data credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.

Bit Range	Default & Access	Field Name (ID): Description
11:6	Ah RW	**IDI C2U Response Credit Initialization (IDI_C2U_RSP_CREDIT_INIT):** This register is the number of credits to initialize C2U response credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U response shim ingress queue size in T-Unit. This provides an ability to limit response credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.
5:0	10h RW	**IDI C2U Request Credit Initialization (IDI_C2U_REQ_CREDIT_INIT):** This register is the number of credits to initialize C2U requests credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress queue size in Badmit. This provides an ability to limit request credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.

5.10.13 IDI3 C2U Credit Control (IDI3_C2U_CREDIT_CTRL_MCHBAR)—Offset 7830h

This register will provide the number of credits that IDI C2U channels should be initialized to and other control mechanisms around IDI start/stop flows. A register will be provided per IDI attach to allow for individual IDI tuning. This register will be for the agent attached to IDI3.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved 0 (RESERVED_0):** Reserved.
17:12	0h RO	**IDI IA C2U Data Credit Initialization (IDI_IA_C2U_DATA_CREDIT_INIT):** This register is the number of credits to initialize C2U data credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress data queue size in B-Unit. This provides an ability to limit data credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RO	**IDI IA C2U Response Credit Initialization (IDI_IA_C2U_RSP_CREDIT_INIT):** This register is the number of credits to initialize C2U response credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U response shim ingress queue size in T-Unit. This provides an ability to limit response credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.
5:0	0h RO	**IDI IA C2U Request Credit Initialization (IDI_IA_C2U_REQ_CREDIT_INIT):** This register is the number of credits to initialize C2U requests credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress queue size in Badmit. This provides an ability to limit request credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.

5.10.14 IDI4 C2U Credit Control (IDI4_C2U_CREDIT_CTRL_MCHBAR)—Offset 7834h

This register will provide the number of credits that IDI C2U channels should be initialized to and other control mechanisms around IDI start/stop flows. A register will be provided per IDI attach to allow for individual IDI tuning. This register will be for the agent attached to IDI4.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved 0 (RESERVED_0):** Reserved
17:12	0h RO	**IDI IA C2U Data Credit Initialization (IDI_IA_C2U_DATA_CREDIT_INIT):** This register is the number of credits to initialize C2U data credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress data queue size in B-Unit. This provides an ability to limit data credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RO	**IDI IA C2U Response Credit Initialization (IDI_IA_C2U_RSP_CREDIT_INIT):** This register is the number of credits to initialize C2U response credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U response shim ingress queue size in T-Unit. This provides an ability to limit response credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.
5:0	0h RO	**IDI IA C2U Request Credit Initialization (IDI_IA_C2U_REQ_CREDIT_INIT):** This register is the number of credits to initialize C2U requests credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress queue size in Badmit. This provides an ability to limit request credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.

5.10.15 IDI5 C2U Credit Control (IDI5_C2U_CREDIT_CTRL_MCHBAR)—Offset 7838h

This register will provide the number of credits that IDI C2U channels should be initialized to and other control mechanisms around IDI start/stop flows. A register will be provided per IDI attach to allow for individual IDI tuning. This register will be for the agent attached to IDI5.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved 0 (RESERVED_0):** Reserved
17:12	0h RO	**IDI IA C2U Data Credit Initialization (IDI_IA_C2U_DATA_CREDIT_INIT):** This register is the number of credits to initialize C2U data credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress data queue size in B-Unit. This provides an ability to limit data credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RO	**IDI IA C2U Response Credit Initialization (IDI_IA_C2U_RSP_CREDIT_INIT):** This register is the number of credits to initialize C2U response credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U response shim ingress queue size in T-Unit. This provides an ability to limit response credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.
5:0	0h RO	**IDI IA C2U Request Credit Initialization (IDI_IA_C2U_REQ_CREDIT_INIT):** This register is the number of credits to initialize C2U requests credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress queue size in Badmit. This provides an ability to limit request credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.

5.10.16 IDI6 C2U Credit Control (IDI6_C2U_CREDIT_CTRL_MCHBAR)—Offset 783Ch

This register will provide the number of credits that IDI C2U channels should be initialized to and other control mechanisms around IDI start/stop flows. A register will be provided per IDI attach to allow for individual IDI tuning. This register will be for the agent attached to IDI6.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved 0 (RESERVED_0):** Reserved.
17:12	0h RO	**IDI IA C2U Data Credit Initialization (IDI_IA_C2U_DATA_CREDIT_INIT):** This register is the number of credits to initialize C2U data credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress data queue size in B-Unit. This provides an ability to limit data credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RO	**IDI IA C2U Response Credit Initialization (IDI_IA_C2U_RSP_CREDIT_INIT):** This register is the number of credits to initialize C2U response credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U response shim ingress queue size in T-Unit. This provides an ability to limit response credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.
5:0	0h RO	**IDI IA C2U Request Credit Initialization (IDI_IA_C2U_REQ_CREDIT_INIT):** This register is the number of credits to initialize C2U requests credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress queue size in Badmit. This provides an ability to limit request credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.

5.10.17 IDI7 C2U Credit Control (IDI7_C2U_CREDIT_CTRL_MCHBAR)—Offset 7840h

This register will provide the number of credits that IDI C2U channels should be initialized to and other control mechanisms around IDI start/stop flows. A register will be provided per IDI attach to allow for individual IDI tuning. This register will be for the agent attached to IDI4.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved 0 (RESERVED_0):** Reserved.
17:12	0h RO	**IDI IA C2U Data Credit Initialization (IDI_IA_C2U_DATA_CREDIT_INIT):** This register is the number of credits to initialize C2U data credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress data queue size in B-Unit. This provides an ability to limit data credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RO	**IDI IA C2U Response Credit Initialization (IDI_IA_C2U_RSP_CREDIT_INIT):** This register is the number of credits to initialize C2U response credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U response shim ingress queue size in T-Unit. This provides an ability to limit response credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.
5:0	0h RO	**IDI IA C2U Request Credit Initialization (IDI_IA_C2U_REQ_CREDIT_INIT):** This register is the number of credits to initialize C2U requests credits for the IDI attach point associated with this register. It is not legal to program this field to a value larger than the C2U ingress queue size in Badmit. This provides an ability to limit request credits at the next IDI start request change will only take place after next IDI start request. The default value of this register should work out of reset.

5.10.18 PII2 A2T Credit Control (PII2_A2T_CREDIT_CTRL_MCHBAR)—Offset 7844h

This register will provide the number of credits that the T-Unit will initialize for the A2T credit initialization on PII2.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 808h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved 0 (RESERVED_0):** Reserved.
15:8	8h RW	**PII2 A2T VC0B Credit Initialization (PII2_A2T_VC0B_CREDIT_INIT):** This field is the number of credits to initialize A2T VC0b requests credits. It is not legal to program this field to a value larger than the A2T VC0b FIFO ingress queue size in the UAM block. This provides an ability to limit request credits at the PII2 credit initialization change will only take place at next credit initialization. The default value of this register should work out of reset.

Bit Range	Default & Access	Field Name (ID): Description
7:0	8h RW	**PII2 A2T VC0A Credit Initialization (PII2_A2T_VC0A_CREDIT_INIT):** This field is the number of credits to initialize A2T VC0a requests credits. It is not legal to program this field to a value larger than the A2T VC0a FIFO ingress queue size in the UAM block. This provides an ability to limit request credits at the PII2 credit initialization change will only take place at next credit initialization. The default value of this register should work out of reset.

5.10.19 BIOSWR Control Policy (T_CR_BIOSWR_CP_0_0_0_MCHBAR)—Offset 7848h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C0061010202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C0061010202h RW	**Access Control Policy (ACCESS_CTRL_POL):** The Access Control Policy for this register and the T-Unit Read/write Policy Registers.

5.10.20 BIOSWR Read Access Control (T_CR_BIOSWR_RAC_0_0_0_MCHBAR)—Offset 7850h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 80000C00630D0217h

Bit Range	Default & Access	Field Name (ID): Description
63:0	80000C00630D0217h RW	**Read Policy (READ_POL):** The Read Policy for the T-Unit Registers.

5.10.21 BIOSWR Write Access Control (T_CR_BIOSWR_WAC_0_0_0_MCHBAR)—Offset 7858h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C00610C0212h

Bit Range	Default & Access	Field Name (ID): Description
63:0	C00610C0212h RW	**Write Policy (WRITE_POL):** The Write Policy for the T-Unit Registers.

5.10.22 TUnit Pcode/Ucode Write, All Read Control Policy Register (T_CR_P_U_CODEWR_ALLRD_CP_0_0_0_MCHBAR)—Offset 7860h

TUnit Pcode/Ucode Write, All Read control policy: This register controls the access policy to the Tunit P_U_CODEWR_ALLRD_RAC P_U_CODEWR_ALLRD_WAC

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001000202h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001000202h RW	**ACCESS_CTRL_POL (ACCESS_CTRL_POL):** The Access Control Policy for this register and the Tunit ucode Read/write Policy Registers.

5.10.23 TUnit Pcode/Ucode Read Access Control (T_CR_P_U_CODEWR_ALLRD_RAC_0_0_0_MCHBAR)—Offset 7868h

Pcode/Ucode Write, All Read Read Access Control Policy: This register controls the read access policy to the Tunit P_U_CODEWR_ALLRD

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: FFFFFFFFFFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:0	FFFFFFFFFFFFFFFFh RO	**READ_POL (READ_POL):** The Read Policy for the Tunit ucode Registers.

5.10.24 TUnit Pcode/Ucode Write Access Control (T_CR_P_U_CODEWR_ALLRD_WAC_0_0_0_MCHBAR)—Offset 7870h

Pcode/Ucode Write, All Read Write Access Control Policy: This register controls the write access policy to the Tunit P_U_CODEWR_ALLRD

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40801008602h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40801008602h RW	**WRITE_POL (WRITE_POL):** The Write Policy for the Tunit ucode Registers.

5.11 Registers Summary

Table 5-11. Summary of cpgc_t_submap Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4800h	4803h	SAI Control Policy LSB (CPGC2_ACCESS_CONTROL_POLICY_L)—Offset 4800h	61010202h
4804h	4807h	SAI Control Policy MSB (CPGC2_ACCESS_CONTROL_POLICY_H)—Offset 4804h	C00h
4808h	480Bh	SAI Read Policy LSB (CPGC2_ACCESS_READ_POLICY_L)—Offset 4808h	FFFFFF3Fh
480Ch	480Fh	SAI Read Policy MSB (CPGC2_ACCESS_READ_POLICY_H)—Offset 480Ch	1371FFFh
4810h	4813h	SAI Write Policy LSB (CPGC2_ACCESS_WRITE_POLICY_L)—Offset 4810h	1000212h
4814h	4817h	SAI Write Policy MSB (CPGC2_ACCESS_WRITE_POLICY_H)—Offset 4814h	C00h
4818h	481Bh	Address Decode Repeats (CPGC2_ADDRESS_CONTROL)—Offset 4818h	0h
481Ch	481Ch	Address Instruction (CPGC2_ADDRESS_INSTRUCTION[0])—Offset 481Ch	0h
481Dh	481Dh	Address Instruction (CPGC2_ADDRESS_INSTRUCTION[1])—Offset 481Dh	0h
481Eh	481Eh	Address Instruction (CPGC2_ADDRESS_INSTRUCTION[2])—Offset 481Eh	0h
481Fh	481Fh	Address Instruction (CPGC2_ADDRESS_INSTRUCTION[3])—Offset 481Fh	0h
4820h	4820h	Data Instruction (CPGC2_DATA_INSTRUCTION[0])—Offset 4820h	0h
4821h	4821h	Data Instruction (CPGC2_DATA_INSTRUCTION[1])—Offset 4821h	0h
4822h	4822h	Data Instruction (CPGC2_DATA_INSTRUCTION[2])—Offset 4822h	0h
4823h	4823h	Data Instruction (CPGC2_DATA_INSTRUCTION[3])—Offset 4823h	0h
4824h	4827h	Data Rotation Repeats (CPGC2_DATA_CONTROL)—Offset 4824h	0h
4828h	482Bh	Address and Data Repeats Status (CPGC2_ADDRESS_DATA_STATUS)—Offset 4828h	0h

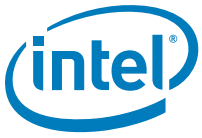


Table 5-11. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
482Ch	482Ch	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[0])—Offset 482Ch	0h
482Dh	482Dh	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[1])—Offset 482Dh	0h
482Eh	482Eh	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[2])—Offset 482Eh	0h
482Fh	482Fh	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[3])—Offset 482Fh	0h
4830h	4830h	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[4])—Offset 4830h	0h
4831h	4831h	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[5])—Offset 4831h	0h
4832h	4832h	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[6])—Offset 4832h	0h
4833h	4833h	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[7])—Offset 4833h	0h
4834h	4834h	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[0])—Offset 4834h	0h
4835h	4835h	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[1])—Offset 4835h	0h
4836h	4836h	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[2])—Offset 4836h	0h
4837h	4837h	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[3])—Offset 4837h	0h
4838h	4838h	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[4])—Offset 4838h	0h
4839h	4839h	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[5])—Offset 4839h	0h
483Ah	483Ah	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[6])—Offset 483Ah	0h
483Bh	483Bh	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[7])—Offset 483Bh	0h
483Ch	483Fh	Wait Timer Current (CPGC2_ALGORITHM_WAIT_COUNT_CURRENT)—Offset 483Ch	0h
4840h	4843h	Algorithm Wait Event Control (CPGC2_ALGORITHM_WAIT_EVENT_CONTROL)—Offset 4840h	0h
4844h	4847h	Base Repeats (CPGC2_BASE_REPEATS)—Offset 4844h	0h
4848h	484Bh	Current Base Repeats (CPGC2_BASE_REPEATS_CURRENT)—Offset 4848h	0h
484Ch	484Fh	Base Column Repeats (CPGC2_BASE_COL_REPEATS)—Offset 484Ch	0h
4850h	4853h	Block Repeats (CPGC2_BLOCK_REPEATS)—Offset 4850h	0h
4854h	4857h	Current Block Repeats (CPGC2_BLOCK_REPEATS_CURRENT)—Offset 4854h	0h
4858h	4858h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[0])—Offset 4858h	0h
4859h	4859h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[1])—Offset 4859h	0h
485Ah	485Ah	Command Instruction (CPGC2_COMMAND_INSTRUCTION[2])—Offset 485Ah	0h

Table 5-11. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
485Bh	485Bh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[3])—Offset 485Bh	0h
485Ch	485Ch	Command Instruction (CPGC2_COMMAND_INSTRUCTION[4])—Offset 485Ch	0h
485Dh	485Dh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[5])—Offset 485Dh	0h
485Eh	485Eh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[6])—Offset 485Eh	0h
485Fh	485Fh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[7])—Offset 485Fh	0h
4860h	4860h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[8])—Offset 4860h	0h
4861h	4861h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[9])—Offset 4861h	0h
4862h	4862h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[10])—Offset 4862h	0h
4863h	4863h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[11])—Offset 4863h	0h
4864h	4864h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[12])—Offset 4864h	0h
4865h	4865h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[13])—Offset 4865h	0h
4866h	4866h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[14])—Offset 4866h	0h
4867h	4867h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[15])—Offset 4867h	0h
4868h	4868h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[16])—Offset 4868h	0h
4869h	4869h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[17])—Offset 4869h	0h
486Ah	486Ah	Command Instruction (CPGC2_COMMAND_INSTRUCTION[18])—Offset 486Ah	0h
486Bh	486Bh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[19])—Offset 486Bh	0h
486Ch	486Ch	Command Instruction (CPGC2_COMMAND_INSTRUCTION[20])—Offset 486Ch	0h
486Dh	486Dh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[21])—Offset 486Dh	0h
486Eh	486Eh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[22])—Offset 486Eh	0h
486Fh	486Fh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[23])—Offset 486Fh	0h
4870h	4873h	Hammer Repeats (CPGC2_HAMMER_REPEATS)—Offset 4870h	0h
4874h	4877h	Current Hammer Repeats (CPGC2_HAMMER_REPEATS_CURRENT)—Offset 4874h	0h
4878h	4878h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[0])—Offset 4878h	0h
4879h	4879h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[1])—Offset 4879h	0h
487Ah	487Ah	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[2])—Offset 487Ah	0h

Table 5-11. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
487Bh	487Bh	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[3])—Offset 487Bh	0h
487Ch	487Ch	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[4])—Offset 487Ch	0h
487Dh	487Dh	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[5])—Offset 487Dh	0h
487Eh	487Eh	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[6])—Offset 487Eh	0h
487Fh	487Fh	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[7])—Offset 487Fh	0h
4880h	4880h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[8])—Offset 4880h	0h
4881h	4881h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[9])—Offset 4881h	0h
4882h	4882h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[10])—Offset 4882h	0h
4883h	4883h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[11])—Offset 4883h	0h
4884h	4884h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[12])—Offset 4884h	0h
4885h	4885h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[13])—Offset 4885h	0h
4886h	4886h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[14])—Offset 4886h	0h
4887h	4887h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[15])—Offset 4887h	0h
4888h	4888h	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[0])—Offset 4888h	0h
4889h	4889h	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[1])—Offset 4889h	0h
488Ah	488Ah	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[2])—Offset 488Ah	0h
488Bh	488Bh	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[3])—Offset 488Bh	0h
488Ch	488Ch	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[4])—Offset 488Ch	0h
488Dh	488Dh	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[5])—Offset 488Dh	0h
488Eh	488Eh	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[6])—Offset 488Eh	0h
488Fh	488Fh	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[7])—Offset 488Fh	0h
4890h	4890h	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[8])—Offset 4890h	0h
4891h	4891h	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[9])—Offset 4891h	0h
4892h	4892h	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[10])—Offset 4892h	0h
4893h	4893h	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[11])—Offset 4893h	0h
4894h	4897h	Offset Repeats (CPGC2_OFFSET_REPEATS[0])—Offset 4894h	0h

Table 5-11. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4898h	489Bh	Offset Repeats (CPGC2_OFFSET_REPEATS[1])—Offset 4898h	0h
489Ch	489Fh	Current Offset Repeats (CPGC2_OFFSET_REPEATS_CURRENT)—Offset 489Ch	0h
48A0h	48A3h	Region Low Row Address (CPGC2_REGION_LOW_ROW)—Offset 48A0h	0h
48A4h	48A7h	Region Low Col Address (CPGC2_REGION_LOW_COL)—Offset 48A4h	0h
48A8h	48ABh	Block Low Row Current (CPGC2_BLOCK_ORIGIN_ROW_CURRENT)—Offset 48A8h	0h
48ACh	48AFh	Current Base Address Rank and Column (CPGC2_BASE_ADDRESS_COL_RANK_CURRENT)—Offset 48ACh	0h
48B0h	48B3h	Current Base Address Bank and Row (CPGC2_BASE_ADDRESS_ROW_BANK_CURRENT)—Offset 48B0h	0h
48B4h	48B7h	Current Offset Address Column (CPGC2_OFFSET_ADDRESS_COL_CURRENT)—Offset 48B4h	0h
48B8h	48BBh	Current Offset Address Row (CPGC2_OFFSET_ADDRESS_ROW_CURRENT)—Offset 48B8h	0h
48BCh	48BFh	Address Size (CPGC2_ADDRESS_SIZE)—Offset 48BCh	0h
48C0h	48C3h	Base Address Control (CPGC2_BASE_ADDRESS_CONTROL)—Offset 48C0h	0h
48C4h	48C7h	Address PRBS Control (CPGC2_ADDRESS_PRBS_CONTROL)—Offset 48C4h	0h
48C8h	48CBh	Address PRBS Seed (CPGC2_ADDRESS_PRBS_SEED)—Offset 48C8h	0h
48CCh	48CFh	Current Address PRBS Status (CPGC2_ADDRESS_PRBS_CURRENT)—Offset 48CCh	0h
48D0h	48D3h	Address PRBS Save (CPGC2_ADDRESS_PRBS_SAVE)—Offset 48D0h	0h
48D4h	48D7h	Command FSM Current State (CPGC2_CMD_FSM_CURRENT)—Offset 48D4h	0h
48D8h	48DBh	Algorithm Wait Timer Configuration (CPGC2_WAIT_2_START_CONFIG)—Offset 48D8h	0h
48DCh	48DFh	VISA Mux Selection (CPGC2_VISA_MUX_SEL)—Offset 48DCh	0h
48E0h	48E3h	Loopback Squencer Configuration (CPGC_LB_SEQ_CFG)—Offset 48E0h	0h
48E4h	48E7h	Loopback Sequencer Control (CPGC_LB_SEQ_CTL)—Offset 48E4h	0h
48E8h	48EBh	Loopback Loopcount Tx Status (CPGC_LB_SEQ_LOOPCOUNT_TX_STATUS)—Offset 48E8h	0h
48ECh	48EFh	Loopback Loopcount Rx Status (CPGC_LB_SEQ_LOOPCOUNT_RX_STATUS)—Offset 48ECh	0h
48F0h	48F3h	Pattern Length Status (CPGC_LB_SEQ_PL_RX_STATUS)—Offset 48F0h	0h
48F4h	48F7h	Refresh Control (CPGC_MISC_REFRESH_CTL)—Offset 48F4h	0h
48F8h	48FBh	ZQ Control (CPGC_MISC_ZQ_CTL)—Offset 48F8h	0h
48FCh	48FFh	ODT Control (CPGC_MISC_ODT_CTL)—Offset 48FCh	0h
4900h	4903h	CKE Control (CPGC_MISC_CKE_CTL)—Offset 4900h	0h
4904h	4907h	Command Rate (CPGC_MISC_CMD_RATE)—Offset 4904h	100Ah
4908h	490Bh	External Trigger Control (CPGC_MISC_EXT_TRIGGER)—Offset 4908h	0h
490Ch	490Fh	Sequence Control (CPGC_SEQ_CTL)—Offset 490Ch	0h
4910h	4913h	Sequence Configuration A (CPGC_SEQ_CFG_A)—Offset 4910h	200000h
4914h	4917h	Sequence Configuration B (CPGC_SEQ_CFG_B)—Offset 4914h	0h

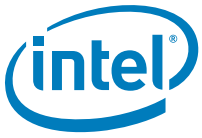


Table 5-11. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4918h	491Bh	Sequence Status (CPGC_SEQ_STATUS)—Offset 4918h	0h
4920h	4923h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[0])—Offset 4920h	0h
4924h	4927h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[1])—Offset 4924h	0h
4928h	492Bh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[2])—Offset 4928h	0h
492Ch	492Fh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[3])—Offset 492Ch	0h
4930h	4933h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[4])—Offset 4930h	0h
4934h	4937h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[5])—Offset 4934h	0h
4938h	493Bh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[6])—Offset 4938h	0h
493Ch	493Fh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[7])—Offset 493Ch	0h
4940h	4943h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[8])—Offset 4940h	0h
4944h	4947h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[9])—Offset 4944h	0h
4948h	494Bh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[10])—Offset 4948h	0h
494Ch	494Fh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[11])—Offset 494Ch	0h
4950h	4953h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[12])—Offset 4950h	0h
4954h	4957h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[13])—Offset 4954h	0h
4958h	495Bh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[14])—Offset 4958h	0h
495Ch	495Fh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[15])—Offset 495Ch	0h
4960h	4963h	Mode3 Fail Status LSB (CPGC2_RASTER_REPO_CONTENT_ECC1)—Offset 4960h	0h
4964h	4967h	Mode3 Fail Status MSB (CPGC2_RASTER_REPO_CONTENT_ECC2)—Offset 4964h	0h
4968h	496Bh	Read Command Count (CPGC2_READ_COMMAND_COUNT_CURRENT)—Offset 4968h	0h
496Ch	496Fh	Mask Errors on First N Reads (CPGC2_MASK_ERRS_FIRST_N_READS)—Offset 496Ch	0h
4970h	4973h	Raster Repository Status (CPGC2_RASTER_REPO_STATUS)—Offset 4970h	0h
4974h	4977h	Error Summary A (CPGC2_ERR_SUMMARY_A)—Offset 4974h	0h
4978h	497Bh	Error Summary B (CPGC2_ERR_SUMMARY_B)—Offset 4978h	0h
497Ch	497Fh	Future use Reserved (CPGC2_ERR_SUMMARY_C)—Offset 497Ch	0h
4980h	4983h	Data Pattern Generation Buffer Control (CPGC_DPAT_BUF_CTL)—Offset 4980h	0h
4984h	4987h	Data Pattern Generation Configuration (CPGC_DPAT_CFG)—Offset 4984h	0h

Table 5-11. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4988h	498Bh	LFSR Configuration and Lane Rotate (CPGC_DPAT_XTRA_LFSR_CFG)—Offset 4988h	0h
498Ch	498Fh	Unisequencer Data Pattern Buffer (CPGC_DPAT_UNISEQ[0])—Offset 498Ch	AA55AA55h
4990h	4993h	Unisequencer Data Pattern Buffer (CPGC_DPAT_UNISEQ[1])—Offset 4990h	AA55AA55h
4994h	4997h	Unisequencer Data Pattern Buffer (CPGC_DPAT_UNISEQ[2])—Offset 4994h	AA55AA55h
4998h	499Bh	Unisequencer LMN Control (CPGC_DPAT_UNISEQ_LMN[0])—Offset 4998h	1010100h
499Ch	499Fh	Unisequencer LMN Control (CPGC_DPAT_UNISEQ_LMN[1])—Offset 499Ch	1010100h
49A0h	49A3h	Unisequencer LMN Control (CPGC_DPAT_UNISEQ_LMN[2])—Offset 49A0h	1010100h
49A4h	49A7h	Invert and DC Control (CPGC_DPAT_INVDCCTL)—Offset 49A4h	AA0000h
49A8h	49ABh	Data Invert/DC Enable Low (CPGC_DPAT_INV_DC_MASK_LO)—Offset 49A8h	0h
49ACh	49AFh	Data Invert/DC Enable High (CPGC_DPAT_INV_DC_MASK_HI)—Offset 49ACh	0h
49B0h	49B3h	Byte Enable Mask Lower (CPGC_DPAT_DRAMDM)—Offset 49B0h	FFFFFFFFh
49B4h	49B7h	Byte Enable Mask Upper (CPGC_DPAT_XDRAMDM)—Offset 49B4h	FFFFFFFFh
49B8h	49BBh	Unisequencer Status - Write (CPGC_DPAT_UNISEQ_WRSTAT[0])—Offset 49B8h	0h
49BCh	49BFh	Unisequencer Status - Write (CPGC_DPAT_UNISEQ_WRSTAT[1])—Offset 49BCh	0h
49C0h	49C3h	Unisequencer Status - Write (CPGC_DPAT_UNISEQ_WRSTAT[2])—Offset 49C0h	0h
49C4h	49C7h	Unisequencer Status - Read (CPGC_DPAT_UNISEQ_RDSTAT[0])—Offset 49C4h	DEADBEEFh
49C8h	49CBh	Unisequencer Status - Read (CPGC_DPAT_UNISEQ_RDSTAT[1])—Offset 49C8h	DEADBEEFh
49CCh	49CFh	Unisequencer Status - Read (CPGC_DPAT_UNISEQ_RDSTAT[2])—Offset 49CCh	DEADBEEFh
49D0h	49D3h	LMN Status - Write (CPGC_DPAT_LMN_WRSTAT[0])—Offset 49D0h	0h
49D4h	49D7h	LMN Status - Write (CPGC_DPAT_LMN_WRSTAT[1])—Offset 49D4h	0h
49D8h	49DBh	LMN Status - Write (CPGC_DPAT_LMN_WRSTAT[2])—Offset 49D8h	0h
49DCh	49DFh	LMN Status - Read (CPGC_DPAT_LMN_RDSTAT[0])—Offset 49DCh	DEADBEEFh
49E0h	49E3h	LMN Status - Read (CPGC_DPAT_LMN_RDSTAT[1])—Offset 49E0h	DEADBEEFh
49E4h	49E7h	LMN Status - Read (CPGC_DPAT_LMN_RDSTAT[2])—Offset 49E4h	DEADBEEFh
49E8h	49EBh	Unisequencer Save Status - Write (CPGC_DPAT_UNISEQ_WRSAVE[0])—Offset 49E8h	DEADBEEFh
49ECh	49EFh	Unisequencer Save Status - Write (CPGC_DPAT_UNISEQ_WRSAVE[1])—Offset 49ECh	DEADBEEFh
49F0h	49F3h	Unisequencer Save Status - Write (CPGC_DPAT_UNISEQ_WRSAVE[2])—Offset 49F0h	DEADBEEFh
49F4h	49F7h	Unisequencer Save Status - Read (CPGC_DPAT_UNISEQ_RDSAVE[0])—Offset 49F4h	0h

Table 5-11. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
49F8h	49FBh	Unisequencer Save Status - Read (CPGC_DPAT_UNISEQ_RDSAVE[1])—Offset 49F8h	0h
49FCh	49FFh	Unisequencer Save Status - Read (CPGC_DPAT_UNISEQ_RDSAVE[2])—Offset 49FCh	0h
4A00h	4A03h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[0])—Offset 4A00h	AAAAAAAAh
4A04h	4A07h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[1])—Offset 4A04h	AAAAAAAAh
4A08h	4A0Bh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[2])—Offset 4A08h	AAAAAAAAh
4A0Ch	4A0Fh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[3])—Offset 4A0Ch	AAAAAAAAh
4A10h	4A13h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[4])—Offset 4A10h	AAAAAAAAh
4A14h	4A17h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[5])—Offset 4A14h	AAAAAAAAh
4A18h	4A1Bh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[6])—Offset 4A18h	AAAAAAAAh
4A1Ch	4A1Fh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[7])—Offset 4A1Ch	AAAAAAAAh
4A20h	4A23h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[8])—Offset 4A20h	AAAAAAAAh
4A24h	4A27h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[9])—Offset 4A24h	AAAAAAAAh
4A28h	4A2Bh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[10])—Offset 4A28h	AAAAAAAAh
4A2Ch	4A2Fh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[11])—Offset 4A2Ch	AAAAAAAAh
4A30h	4A33h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[12])—Offset 4A30h	AAAAAAAAh
4A34h	4A37h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[13])—Offset 4A34h	AAAAAAAAh
4A38h	4A3Bh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[14])—Offset 4A38h	AAAAAAAAh
4A3Ch	4A3Fh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[15])—Offset 4A3Ch	AAAAAAAAh
4A40h	4A43h	Error Checker Control (CPGC_ERR_CTL)—Offset 4A40h	0h
4A44h	4A47h	Lane Error Mask Lower Bytes (CPGC_ERR_LNEN_LO)—Offset 4A44h	0h
4A48h	4A4Bh	Lane Error Mask Upper Bytes or Extended Chunk Enable (CPGC_ERR_LNEN_HI)—Offset 4A48h	0h
4A4Ch	4A4Fh	Lane Error Mask ECC (CPGC_ERR_XLNEN)—Offset 4A4Ch	FFh
4A50h	4A53h	Lane Error Status Lower Bytes (CPGC_ERR_STAT03)—Offset 4A50h	0h
4A54h	4A57h	Lane Error Status Upper Bytes or Extended Chunk Error Status (CPGC_ERR_STAT47)—Offset 4A54h	0h
4A58h	4A5Bh	ECC Lane Error Status (CPGC_ERR_ECC_CHNK_RANK_STAT)—Offset 4A58h	0h
4A5Ch	4A5Fh	ByteGroup Error Status (CPGC_ERR_BYTE_NTH_PAR_STAT)—Offset 4A5Ch	0h
4A60h	4A63h	Error Counter Control (CPGC_ERR_CNTRCTL[0])—Offset 4A60h	0h
4A64h	4A67h	Error Counter Control (CPGC_ERR_CNTRCTL[1])—Offset 4A64h	0h
4A68h	4A6Bh	Error Counter Control (CPGC_ERR_CNTRCTL[2])—Offset 4A68h	0h
4A6Ch	4A6Fh	Error Counter Control (CPGC_ERR_CNTRCTL[3])—Offset 4A6Ch	0h
4A70h	4A73h	Error Counter Control (CPGC_ERR_CNTRCTL[4])—Offset 4A70h	0h
4A74h	4A77h	Error Counter Control (CPGC_ERR_CNTRCTL[5])—Offset 4A74h	0h
4A78h	4A7Bh	Error Counter Control (CPGC_ERR_CNTRCTL[6])—Offset 4A78h	0h
4A7Ch	4A7Fh	Error Counter Control (CPGC_ERR_CNTRCTL[7])—Offset 4A7Ch	0h
4A80h	4A83h	Error Counter Control (CPGC_ERR_CNTRCTL[8])—Offset 4A80h	0h
4A84h	4A87h	Error Counter (CPGC_ERR_CNTR[0])—Offset 4A84h	0h

Table 5-11. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4A88h	4A8Bh	Error Counter (CPGC_ERR_CNTR[1])—Offset 4A88h	0h
4A8Ch	4A8Fh	Error Counter (CPGC_ERR_CNTR[2])—Offset 4A8Ch	0h
4A90h	4A93h	Error Counter (CPGC_ERR_CNTR[3])—Offset 4A90h	0h
4A94h	4A97h	Error Counter (CPGC_ERR_CNTR[4])—Offset 4A94h	0h
4A98h	4A9Bh	Error Counter (CPGC_ERR_CNTR[5])—Offset 4A98h	0h
4A9Ch	4A9Fh	Error Counter (CPGC_ERR_CNTR[6])—Offset 4A9Ch	0h
4AA0h	4AA3h	Error Counter (CPGC_ERR_CNTR[7])—Offset 4AA0h	0h
4AA4h	4AA7h	Error Counter (CPGC_ERR_CNTR[8])—Offset 4AA4h	0h
4AA8h	4AABh	Error Counter Overflow (CPGC_ERR_CNTR_OV)—Offset 4AA8h	0h
4AACh	4AAFh	Error Log Control and Status (CPGC_ERRLOG_CTL_STAT)—Offset 4AACh	0h
4AB0h	4AB3h	Error Log Data Access (CPGC_ERRLOG_DATA)—Offset 4AB0h	0h
4AB4h	4AB7h	Loopback Error Status (CPGC_ERR_TEST_ERR_STAT)—Offset 4AB4h	0h
4AB8h	4ABBh	Rank Logical To Physical Map (CPGC_SEQ_RANK_L2P_MAPPING)—Offset 4AB8h	76543210h
4ABCh	4ABFh	Bank Logical to Physical Map Low (CPGC_SEQ_BANK_L2P_MAPPING_A)—Offset 4ABCh	76543210h
4AC0h	4AC3h	Bank Logical to Physical Map High (CPGC_SEQ_BANK_L2P_MAPPING_B)—Offset 4AC0h	FEDCBA98h
4AC4h	4AC7h	Rank Address Swizzle (CPGC_SEQ_RANK_ADDR_SWIZZLE)—Offset 4AC4h	FEDCh
4AC8h	4ACBh	Bank Address Swizzle (CPGC_SEQ_BANK_ADDR_SWIZZLE)—Offset 4AC8h	DEB38h
4ACCh	4ACFh	Row Address Swizzle Low (CPGC_SEQ_ROW_ADDR_SWIZZLE_A)—Offset 4ACCh	A418820h
4AD0h	4AD3h	Row Address Swizzle Mid (CPGC_SEQ_ROW_ADDR_SWIZZLE_B)—Offset 4AD0h	16A4A0E6h
4AD4h	4AD7h	Row Address Swizzle High (CPGC_SEQ_ROW_ADDR_SWIZZLE_C)—Offset 4AD4h	2307B9ACh
4AD8h	4ADBh	Row Address XOR (CPGC_SEQ_ROW_ADDR_SWIZZLE_X)—Offset 4AD8h	FFFFFh
4ADCh	4ADFh	Column Address Swizzle Low (CPGC_SEQ_COL_ADDR_SWIZZLE_A)—Offset 4ADCh	65432100h
4AE0h	4AE3h	Column Address Swizzle High (CPGC_SEQ_COL_ADDR_SWIZZLE_B)—Offset 4AE0h	87h
4AE8h	4AEBh	DQ Inversion Lookup Data Low (CPGC_SEQ_ROW_ADDR_DQ_MAP0)—Offset 4AE8h	0h
4AECh	4AEFh	DQ Inversion Lookup Data High (CPGC_SEQ_ROW_ADDR_DQ_MAP1)—Offset 4AECh	0h

5.11.1 SAI Control Policy LSB (CPGC2_ACCESS_CONTROL_POLICY_L)—Offset 4800h

Lower half of the SAI Control Policy.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 61010202h

Bit Range	Default & Access	Field Name (ID): Description
31:0	61010202h RW	**Access Control Policy LSB (Control_Policy_L):** Lower half of the SAI Control Policy Value [31:0].

5.11.2 SAI Control Policy MSB (CPGC2_ACCESS_CONTROL_POLICY_H)—Offset 4804h

Upper half of the SAI Control Policy.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	C00h RW	**Access Control Policy MSB (Control_Policy_H):** Upper half of the SAI Control Policy Value [63:32].

5.11.3 SAI Read Policy LSB (CPGC2_ACCESS_READ_POLICY_L)—Offset 4808h

Lower half of the SAI Read Policy.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFFFF3Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFF3Fh RW	**Access Read Policy LSB (Read_Policy_L):** Lower half of the SAI Read Policy Value [31:0].

5.11.4 SAI Read Policy MSB (CPGC2_ACCESS_READ_POLICY_H)—Offset 480Ch

Upper half of the SAI Read Policy.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1371FFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	1371FFFh RW	**Access Read Policy MSB (Read_Policy_H):** Upper half of the SAI Read Policy Value [63:32].

5.11.5 SAI Write Policy LSB (CPGC2_ACCESS_WRITE_POLICY_L)—Offset 4810h

Lower half of the SAI Write Policy.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1000212h

Bit Range	Default & Access	Field Name (ID): Description
31:0	1000212h RW	**Access Write Policy LSB (Write_Policy_L):** Lower half of the SAI Write Policy Value [31:0].

5.11.6 SAI Write Policy MSB (CPGC2_ACCESS_WRITE_POLICY_H)—Offset 4814h

Upper half of the SAI Write Policy.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	C00h RW	**Access Write Policy MSB (Write_Policy_H):** Upper half of the SAI Write Policy Value [63:32].

5.11.7 Address Decode Repeats (CPGC2_ADDRESS_CONTROL)—Offset 4818h

If Algorithm_Address_#.Bits(6:6) is set to 1, then Address Decode is enabled.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5:0	0h RW	**Address Decode Repeats (Address_Decode_Rotate_Repeats):** Number of times the current Address_Instruction will repeat if Address_Decode_Enable is set (as N-1) (0=1 time). If for the current Address_Instruction, Address_Decode_Enable is set, then at the start of that Address_Instruction, initialize the XOR_Address_Pattern to a single 1 in the LSB of Column Address. Otherwise, it is initialized to all zero's. For (Address_Decode_Rotate_Repeat_Current = 0; Current_ Address_Decode_Rotate_Repeat_Current <= Address_Decode_Rotate_Repeat; Address_Decode_Rotate_Repeat_Current ++) Execute the entire Algorithm (Block Traversal, Algorithm_Instruction, Commands) with the following behavior: At the end of each complete Block Traversal, rotate the XOR Address Pattern 1 bit position from LSB to MSB (Column through Region_Bits_Column, Region_Bits_Row, Region_Num_Banks, and through Region_Num_Ranks). Region_Size.Num_Bank and Region_Size.Num_Rank numbers are converted to the equivalent number of adddress bits to cover their range (ceil(log2(Num+1))) and should be programmed to a power of 2 value (minus 1): 1,3,7, or 15. If only one Rank is being tested, then you should limit the amount in this register to the sum of the number of address bits without Rank bits.

5.11.8 Address Instruction (CPGC2_ADDRESS_INSTRUCTION[0])—Offset 481Ch

Address Instruction controlling Address_Order and Address_Direction reversal and decode rotation/loop.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Address Instruction (Last):** If set, then this is the last Address Instruction and the test will terminate following full execution of this instruction. If there are no Last bits set in the Address Instruction list, then the test will not stop due to a completion of the test, but will be an Infinite Test.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Address Decode Enable (Address_Decode_Enable):** Enables rotating XOR of address bits. Used in concert with the Address_Decode_Enable field in the Command_Instruction list. This bit enables repeating of the current Address_Instruction for Address_Decode_Rotate_Repeats times.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(10) Inv(FastX) - North West** Increment Column and Decrement Row and Carry Decrement Column into Row. **(0)(11) Diagonal2 - East** Increment Row and Carry Increment into Column. **(1)(11) Inv(Diagonal2) West** Decrement Row and Carry Decrement into Column. Note that the Bank and Rank Address direction follows the same as the Column (Increment or Decrement). Note for diagonal directions, a Carry results in twice the normal increment/decrement of the Row field. Incrementing fields start at 0, and Decrementing fields start at 2^(field_block_size)-2^(field_increment)= top of block.
2:0	0h RW	**Address Order (Address_Order):** Controls the fastest changing address field, and how that carries into higher order fields. 000 Rank, Bank, Row/Col. 001 Rank, Row/Col, Bank. 010 Bank, Rank, Row/Col. 011 Bank, Row/Col, Rank. 100 Row/Col, Rank, Bank. 101 Row/Col, Bank, Rank. 110 Row/Col (Used for Offset) Rank and Bank are unchanged. 111 Row-Col (Used for Stripe Offset) No Carry from any field to another. Carry order between Row and Column is dependent on the Address_Direction field.

5.11.9 Address Instruction (CPGC2_ADDRESS_INSTRUCTION[1])—Offset 481Dh

Address Instruction controlling Address_Order and Address_Direction reversal and decode rotation/loop.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Address Instruction (Last):** If set, then this is the last Address Instruction and the test will terminate following full execution of this instruction. If there are no Last bits set in the Address Instruction list, then the test will not stop due to a completion of the test, but will be an Infinite Test.
6	0h RW	**Address Decode Enable (Address_Decode_Enable):** Enables rotating XOR of address bits. Used in concert with the Address_Decode_Enable field in the Command_Instruction list. This bit enables repeating of the current Address_Instruction for Address_Decode_Rotate_Repeats times.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(10) Inv(FastX) - North West** Increment Column and Decrement Row and Carry Decrement Column into Row. **(0)(11) Diagonal2 - East** Increment Row and Carry Increment into Column. **(1)(11) Inv(Diagonal2) West** Decrement Row and Carry Decrement into Column. Note that the Bank and Rank Address direction follows the same as the Column (Increment or Decrement). Note for diagonal directions, a Carry results in twice the normal increment/decrement of the Row field. Incrementing fields start at 0, and Decrementing fields start at 2^(field_block_size)-2^(field_increment)= top of block.

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RW	**Address Order (Address_Order):** Controls the fastest changing address field, and how that carries into higher order fields. 000 Rank, Bank, Row/Col. 001 Rank, Row/Col, Bank. 010 Bank, Rank, Row/Col. 011 Bank, Row/Col, Rank. 100 Row/Col, Rank, Bank. 101 Row/Col, Bank, Rank. 110 Row/Col (Used for Offset) Rank and Bank are unchanged. 111 Row-Col (Used for Stripe Offset) No Carry from any field to another. Carry order between Row and Column is dependent on the Address_Direction field.

5.11.10 Address Instruction (CPGC2_ADDRESS_INSTRUCTION[2])—Offset 481Eh

Address Instruction controlling Address_Order and Address_Direction reversal and decode rotation/loop.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Address Instruction (Last):** If set, then this is the last Address Instruction and the test will terminate following full execution of this instruction. If there are no Last bits set in the Address Instruction list, then the test will not stop due to a completion of the test, but will be an Infinite Test.
6	0h RW	**Address Decode Enable (Address_Decode_Enable):** Enables rotating XOR of address bits. Used in concert with the Address_Decode_Enable field in the Command_Instruction list. This bit enables repeating of the current Address_Instruction for Address_Decode_Rotate_Repeats times.

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(10) Inv(FastX) - North West** Increment Column and Decrement Row and Carry Decrement Column into Row. **(0)(11) Diagonal2 - East** Increment Row and Carry Increment into Column. **(1)(11) Inv(Diagonal2) West** Decrement Row and Carry Decrement into Column. Note that the Bank and Rank Address direction follows the same as the Column (Increment or Decrement). Note for diagonal directions, a Carry results in twice the normal increment/decrement of the Row field. Incrementing fields start at 0, and Decrementing fields start at 2^(field_block_size)-2^(field_increment)= top of block.
2:0	0h RW	**Address Order (Address_Order):** Controls the fastest changing address field, and how that carries into higher order fields. 000 Rank, Bank, Row/Col. 001 Rank, Row/Col, Bank. 010 Bank, Rank, Row/Col. 011 Bank, Row/Col, Rank. 100 Row/Col, Rank, Bank. 101 Row/Col, Bank, Rank. 110 Row/Col (Used for Offset) Rank and Bank are unchanged. 111 Row-Col (Used for Stripe Offset) No Carry from any field to another. Carry order between Row and Column is dependent on the Address_Direction field.

5.11.11 Address Instruction (CPGC2_ADDRESS_INSTRUCTION[3])—Offset 481Fh

Address Instruction controlling Address_Order and Address_Direction reversal and decode rotation/loop.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Address Instruction (Last):** If set, then this is the last Address Instruction and the test will terminate following full execution of this instruction. If there are no Last bits set in the Address Instruction list, then the test will not stop due to a completion of the test, but will be an Infinite Test.
6	0h RW	**Address Decode Enable (Address_Decode_Enable):** Enables rotating XOR of address bits. Used in concert with the Address_Decode_Enable field in the Command_Instruction list. This bit enables repeating of the current Address_Instruction for Address_Decode_Rotate_Repeats times.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(10) Inv(FastX) - North West** Increment Column and Decrement Row and Carry Decrement Column into Row. **(0)(11) Diagonal2 - East** Increment Row and Carry Increment into Column. **(1)(11) Inv(Diagonal2) West** Decrement Row and Carry Decrement into Column. Note that the Bank and Rank Address direction follows the same as the Column (Increment or Decrement). Note for diagonal directions, a Carry results in twice the normal increment/decrement of the Row field. Incrementing fields start at 0, and Decrementing fields start at 2^(field_block_size)-2^(field_increment)= top of block.

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RW	**Address Order (Address_Order):** Controls the fastest changing address field, and how that carries into higher order fields. 000 Rank, Bank, Row/Col. 001 Rank, Row/Col, Bank. 010 Bank, Rank, Row/Col. 011 Bank, Row/Col, Rank. 100 Row/Col, Rank, Bank. 101 Row/Col, Bank, Rank. 110 Row/Col (Used for Offset) Rank and Bank are unchanged. 111 Row-Col (Used for Stripe Offset) No Carry from any field to another. Carry order between Row and Column is dependent on the Address_Direction field.

5.11.12 Data Instruction (CPGC2_DATA_INSTRUCTION[0])—Offset 4820h

Data Instruction controlling Alternate Data rotation, Background inversion pattern and Data Inversion.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Data Instruction (Last):** Last Data_Instruction indication, execution is continued at Data_Instruction[0] if the test does not otherwise terminate. This bit is implied to be set for Data_Instruction[3].
6	0h RW	**Invert Data (Invert_Data):** Globally Invert all data. Combined with the Algorithm_Instruction Invert_Data field, and the Command_Instruction or Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5:4	0h RW	**Data Background (Data_Background):** 00 - Solid 01 - Column Stripes 10 - Row Stripes 11 - Checkerboard

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Data Select Rotate Enable (Data_Select_Rotation_Enable):** Enables rotating lane pattern data. Used in concert with the Data_Select_Rotation_Enable field in the Data_Instruction list. This bit enables repeating of the current Data_Instruction for Data_Select_Rotation_Repeat times. Data generated using the advanced pattern generation will rotate by one data bit (LSB toward MSB) for each Data_Select_Rotation_Repeat. For the purpose of this shift, the order follows the Address_Instruction Address_Order and the Algorithm_Instruction[0] Address_Direction.
2:0	0h RO	Reserved.

5.11.13 Data Instruction (CPGC2_DATA_INSTRUCTION[1])—Offset 4821h

Data Instruction controlling Alternate Data rotation, Background inversion pattern and Data Inversion.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Data Instruction (Last):** Last Data_Instruction indication, execution is continued at Data_Instruction[0] if the test does not otherwise terminate. This bit is implied to be set for Data_Instruction[3].
6	0h RW	**Invert Data (Invert_Data):** Globally Invert all data. Combined with the Algorithm_Instruction Invert_Data field, and the Command_Instruction or Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5:4	0h RW	**Data Background (Data_Background):** 00 - Solid 01 - Column Stripes 10 - Row Stripes 11 - Checkerboard

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Data Select Rotate Enable (Data_Select_Rotation_Enable):** Enables rotating lane pattern data. Used in concert with the Data_Select_Rotation_Enable field in the Data_Instruction list. This bit enables repeating of the current Data_Instruction for Data_Select_Rotation_Repeat times. Data generated using the advanced pattern generation will rotate by one data bit (LSB toward MSB) for each Data_Select_Rotation_Repeat. For the purpose of this shift, the order follows the Address_Instruction Address_Order and the Algorithm_Instruction[0] Address_Direction.
2:0	0h RO	Reserved.

5.11.14 Data Instruction (CPGC2_DATA_INSTRUCTION[2])—Offset 4822h

Data Instruction controlling Alternate Data rotation, Background inversion pattern and Data Inversion.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Data Instruction (Last):** Last Data_Instruction indication, execution is continued at Data_Instruction[0] if the test does not otherwise terminate. This bit is implied to be set for Data_Instruction[3].
6	0h RW	**Invert Data (Invert_Data):** Globally Invert all data. Combined with the Algorithm_Instruction Invert_Data field, and the Command_Instruction or Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5:4	0h RW	**Data Background (Data_Background):** 00 - Solid 01 - Column Stripes 10 - Row Stripes 11 - Checkerboard

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Data Select Rotate Enable (Data_Select_Rotation_Enable):** Enables rotating lane pattern data. Used in concert with the Data_Select_Rotation_Enable field in the Data_Instruction list. This bit enables repeating of the current Data_Instruction for Data_Select_Rotation_Repeat times. Data generated using the advanced pattern generation will rotate by one data bit (LSB toward MSB) for each Data_Select_Rotation_Repeat. For the purpose of this shift, the order follows the Address_Instruction Address_Order and the Algorithm_Instruction[0] Address_Direction.
2:0	0h RO	Reserved.

5.11.15 Data Instruction (CPGC2_DATA_INSTRUCTION[3])—Offset 4823h

Data Instruction controlling Alternate Data rotation, Background inversion pattern and Data Inversion.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Data Instruction (Last):** Last Data_Instruction indication, execution is continued at Data_Instruction[0] if the test does not otherwise terminate. This bit is implied to be set for Data_Instruction[3].
6	0h RW	**Invert Data (Invert_Data):** Globally Invert all data. Combined with the Algorithm_Instruction Invert_Data field, and the Command_Instruction or Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5:4	0h RW	**Data Background (Data_Background):** 00 - Solid 01 - Column Stripes 10 - Row Stripes 11 - Checkerboard

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Data Select Rotate Enable (Data_Select_Rotation_Enable):** Enables rotating lane pattern data. Used in concert with the Data_Select_Rotation_Enable field in the Data_Instruction list. This bit enables repeating of the current Data_Instruction for Data_Select_Rotation_Repeat times. Data generated using the advanced pattern generation will rotate by one data bit (LSB toward MSB) for each Data_Select_Rotation_Repeat. For the purpose of this shift, the order follows the Address_Instruction Address_Order and the Algorithm_Instruction[0] Address_Direction.
2:0	0h RO	Reserved.

5.11.16 Data Rotation Repeats (CPGC2_DATA_CONTROL)—Offset 4824h

Number of times an enabled Data_Instruction will be repeated.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**Data Rotation Repeats (Data_Select_Rotation_Repeats):** Any Data_Instruction with Data_Select_Rotation_Enable will repeat this many times. As N-1. (0=1 time)

5.11.17 Address and Data Repeats Status (CPGC2_ADDRESS_DATA_STATUS)—Offset 4828h

Current number of remaining repeats for Data and Address Repeats loops.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	0h RO/V	**Current Remaining Data Rotation Loops (Data_Select_Rotation_Repeats_Current):** Current state of Data_Select_Rotation_Repeats loop (down count).
15:6	0h RO	Reserved.
5:0	0h RO/V	**Current Remaining Address Decode Loops (Address_Decode_Rotate_Repeats_Current):** Current state of Address_Decode_Rotate_Repeats loop (down count).

5.11.18 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[0])—Offset 482Ch

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.11.19 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[1])—Offset 482Dh

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.11.20 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[2])—Offset 482Eh

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.11.21 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[3])—Offset 482Fh

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.11.22 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[4])—Offset 4830h

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.11.23 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[5])—Offset 4831h

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.11.24 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[6])—Offset 4832h

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.11.25 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[7])—Offset 4833h

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.11.26 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[0])—Offset 4834h

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgement must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.11.27 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[1])—Offset 4835h

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgement must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.11.28 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[2])—Offset 4836h

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgement must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.11.29 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[3])—Offset 4837h

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgement must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.11.30 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[4])—Offset 4838h

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgement must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.11.31 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[5])—Offset 4839h

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgement must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.11.32 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[6])—Offset 483Ah

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgement must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.11.33 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[7])—Offset 483Bh

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgement must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.11.34 Wait Timer Current (CPGC2_ALGORITHM_WAIT_COUNT_CURRENT)—Offset 483Ch

Current wait timer value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW/1C/V	**Current Wait Timer (Wait_Timer_Current):** Current wait timer value. See Wait_Time description. (down count)

5.11.35 Algorithm Wait Event Control (CPGC2_ALGORITHM_WAIT_EVENT_CONTROL)—Offset 4840h

Algorithm wait event control.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Select Event (Select_Event):** Select_Event is decoded in the following ways. Select_Event = 00 = Read/Write Pending CAS cue is empty Select_Event = 01 = CKE Power Down Select_Event = 10 = Refresh Select_Event = 11 = Self Refresh
29:26	0h RO	Reserved.
25:24	0h RW	**Wait Clock Frequency (Wait_Clock_Frequency):** 00 - 1GHz 01 - 1MHz 10 - 1KHz 11 - Native DUNIT clock
23:20	0h RW	**Select Event Hold Timer (Timer):** Exponential timer (timer value calculated as 2^Timer). If WaitEventStart is set in the currently executing Algorithm Instruction, this timer dynamically replaces the current Wait_Time counter following the Select_Event occurring (such as SelfRefresh or PowerDown) , to add a fixed delay for the Select_Event condition to remain before CPGC activity resumes.
19:16	0h RO	Reserved.
15:0	0h RW	**Wait Time (Wait_Time):** Number of clocks at Wait_Clock_Frequency to wait before starting current Algorithm_Instruction if Wait_Start = 1.

5.11.36 Base Repeats (CPGC2_BASE_REPEATS)—Offset 4844h

Base Address Loopcount.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Repeats (Base_Repeats):** Base Address Loopcount - Typically the number of Base Addresses within the Block (Row*Col*Bank*Rank) As N-1 value. This is the number of times the current Algorithm Instruction will be executed.

5.11.37 Current Base Repeats (CPGC2_BASE_REPEATS_CURRENT)—Offset 4848h

Current Base Address Loopcount.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current Remaining Base Loops (Base_Repeats_Current):** Current remaining Base Address loops (down count).

5.11.38 Base Column Repeats (CPGC2_BASE_COL_REPEATS)—Offset 484Ch

Base Address Loopcount - Alternate.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Column Repeats (Base_Col_Repeats):** Alternate Base_Address_Loopcount. Often used to initialze a Row or Column worth of data. This is used when Base_Range_Row field of ALGORITHM_INSTRUCTION_CTL is activated. This is the number of times the current Algorithm Instruction will be executed.

5.11.39 Block Repeats (CPGC2_BLOCK_REPEATS)—Offset 4850h

Block Loopcount.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Block Repeats (Block_Repeats):** Block Loopcount. Typically the number of Blocks to be tested to traverse the entire Tested Region. (2^region_size/2^block_size -1) As N-1 value. This is the number of times the entire list of Algorithm Instructions will be executed.

5.11.40 Current Block Repeats (CPGC2_BLOCK_REPEATS_CURRENT)—Offset 4854h

Current Block Loopcount.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current Remaining Block Loops (Block_Repeats_Current):** Current Block Loopcount (down count).

5.11.41 Command Instruction (CPGC2_COMMAND_INSTRUCTION[0])—Offset 4858h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.42 Command Instruction (CPGC2_COMMAND_INSTRUCTION[1])—Offset 4859h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.43 Command Instruction (CPGC2_COMMAND_INSTRUCTION[2])—Offset 485Ah

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.44 Command Instruction (CPGC2_COMMAND_INSTRUCTION[3])—Offset 485Bh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.45 Command Instruction (CPGC2_COMMAND_INSTRUCTION[4])—Offset 485Ch

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.46 Command Instruction (CPGC2_COMMAND_INSTRUCTION[5])—Offset 485Dh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.47 Command Instruction (CPGC2_COMMAND_INSTRUCTION[6])—Offset 485Eh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.48 Command Instruction (CPGC2_COMMAND_INSTRUCTION[7])—Offset 485Fh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.49 Command Instruction (CPGC2_COMMAND_INSTRUCTION[8])—Offset 4860h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.50 Command Instruction (CPGC2_COMMAND_INSTRUCTION[9])—Offset 4861h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.51 Command Instruction (CPGC2_COMMAND_INSTRUCTION[10])—Offset 4862h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.52 Command Instruction (CPGC2_COMMAND_INSTRUCTION[11])—Offset 4863h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.53 Command Instruction (CPGC2_COMMAND_INSTRUCTION[12])—Offset 4864h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.54 Command Instruction (CPGC2_COMMAND_INSTRUCTION[13])—Offset 4865h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.55 Command Instruction (CPGC2_COMMAND_INSTRUCTION[14])—Offset 4866h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.56 Command Instruction (CPGC2_COMMAND_INSTRUCTION[15])—Offset 4867h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.57 Command Instruction (CPGC2_COMMAND_INSTRUCTION[16])—Offset 4868h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.58 Command Instruction (CPGC2_COMMAND_INSTRUCTION[17])—Offset 4869h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.59 Command Instruction (CPGC2_COMMAND_INSTRUCTION[18])—Offset 486Ah

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.60 Command Instruction (CPGC2_COMMAND_INSTRUCTION[19])—Offset 486Bh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.61 Command Instruction (CPGC2_COMMAND_INSTRUCTION[20])—Offset 486Ch

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.62 Command Instruction (CPGC2_COMMAND_INSTRUCTION[21])—Offset 486Dh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.63 Command Instruction (CPGC2_COMMAND_INSTRUCTION[22])—Offset 486Eh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.64 Command Instruction (CPGC2_COMMAND_INSTRUCTION[23])—Offset 486Fh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.11.65 Hammer Repeats (CPGC2_HAMMER_REPEATS)—Offset 4870h

Hammer Loopcount.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Hammer Repeats (Hammer_Repeats):** Hammer_Repeats is the number of times any command is repeated at the same address when the Hammer control bit is set in the Command_Instruction (if not an offset command).

5.11.66 Current Hammer Repeats (CPGC2_HAMMER_REPEATS_CURRENT)—Offset 4874h

Current Hammer Loopcount.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current Remaining Hammer Repeats (Hammer_Repeats_Current):** Current Hammer Loopcount (down count).

5.11.67 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[0])—Offset 4878h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.68 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[1])—Offset 4879h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.69 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[2])—Offset 487Ah

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.70 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[3])—Offset 487Bh

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.71 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[4])—Offset 487Ch

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.72 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[5])—Offset 487Dh

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.73 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[6])—Offset 487Eh

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.74 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[7])—Offset 487Fh

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.75 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[8])—Offset 4880h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.76 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[9])—Offset 4881h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.77 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[10])—Offset 4882h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.78 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[11])—Offset 4883h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.79 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[12])—Offset 4884h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.80 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[13])—Offset 4885h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.81 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[14])—Offset 4886h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.82 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[15])—Offset 4887h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.11.83 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[0])—Offset 4888h

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.11.84 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[1])—Offset 4889h

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.11.85 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[2])—Offset 488Ah

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.11.86 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[3])—Offset 488Bh

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.11.87 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[4])—Offset 488Ch

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.11.88 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[5])—Offset 488Dh

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.11.89 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[6])—Offset 488Eh

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.11.90 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[7])—Offset 488Fh

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.11.91 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[8])—Offset 4890h

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.11.92 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[9])—Offset 4891h

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.11.93 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[10])—Offset 4892h

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.11.94 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[11])—Offset 4893h

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.11.95 Offset Repeats (CPGC2_OFFSET_REPEATS[0])—Offset 4894h

Set the loopcount for Offset (Distance from Base). Selected by Command_Instruction.Offset_Group bit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Offset Repeats (Offset_Repeats):** Set the loopcount for Offset (Distance from Base). The entire list of Offset Commands are executed for each loop.

5.11.96 Offset Repeats (CPGC2_OFFSET_REPEATS[1])—Offset 4898h

Set the loopcount for Offset (Distance from Base). Selected by Command_Instruction.Offset_Group bit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Offset Repeats (Offset_Repeats):** Set the loopcount for Offset (Distance from Base). The entire list of Offset Commands are executed for each loop.

5.11.97 Current Offset Repeats (CPGC2_OFFSET_REPEATS_CURRENT)—Offset 489Ch

Current Offset Loopcount.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current Remaining Offset Repeats (Offset_Repeats_Current):** Current Offset Loopcount (down count).

5.11.98 Region Low Row Address (CPGC2_REGION_LOW_ROW)—Offset 48A0h

Region low row address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:0	0h RW	**Low Row (Low_Row):** Set the bottom Row for the physical memory being tested. This value is added to all Region Row Addresses computed.

5.11.99 Region Low Col Address (CPGC2_REGION_LOW_COL)—Offset 48A4h

Region low column address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10:2	0h RW	**Low Column (Low_Col):** Set the lowest Column for the physical memory being tested. This value is added to all Region Column Addresses computed.
1:0	0h RO	Reserved.

5.11.100 Block Low Row Current (CPGC2_BLOCK_ORIGIN_ROW_CURRENT)—Offset 48A8h

Block low row current.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:0	0h RO/V	**Current Block Origin Row (Block_Origin_Row_Current):** Current row within the testing region of memory Updated as the block traverses through the region.

5.11.101 Current Base Address Rank and Column (CPGC2_BASE_ADDRESS_COL_RANK_CURRENT)—Offset 48ACh

Current Base Address both Rank and Column.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18:16	0h RO/V	**Current Rank Base Address (Base_Rank_Current):** Current Base Address Rank within the block.
15:11	0h RO	Reserved.
10:2	0h RO/V	**Current Column Base Address (Base_Col_Current):** Current Base Address Column within the block.
1:0	0h RO	Reserved.

5.11.102 Current Base Address Bank and Row (CPGC2_BASE_ADDRESS_ROW_BANK_CURRENT)—Offset 48B0h

Current Base Address both Bank and Row.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:24	0h RO/V	**Current Bank Base Address (Base_Bank_Current):** Current Base Address Bank within the block.
23:18	0h RO	Reserved.
17:0	0h RO/V	**Current Row Base Address (Base_Row_Current):** Current Base Address Row within the block.

5.11.103 Current Offset Address Column (CPGC2_OFFSET_ADDRESS_COL_CURRENT)—Offset 48B4h

Current Offset Address - Column

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10:2	0h RO/V	**Current Column Offset Address (Offset_Col_Current):** Current Offset Address Column within the block. Only valid if the current Command_Instruction pointed to by Command_Instruction_Current is an Offset command.
1:0	0h RO	Reserved.

5.11.104 Current Offset Address Row (CPGC2_OFFSET_ADDRESS_ROW_CURRENT)—Offset 48B8h

Current Offset Address - Row

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:0	0h RO/V	**Current Row Offset Address (Offset_Row_Current):** Current Offset Address Row within the block. Only valid if the current Command_Instruction pointed to by Command_Instruction_Current is an Offset command.

5.11.105 Address Size (CPGC2_ADDRESS_SIZE)—Offset 48BCh

Set the size of the Region and Block.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:24	0h RW	**Region Row Size (Region_Size_Bits_Row):** 2^Region_Size_Bits_Row is the number of rows in the testing region. Must be >= to Block_Size_Bits_Row.
23:20	0h RW	**Region Column Size (Region_Size_Bits_Col):** 2^Region_Size_Bits_Col is the number of columns in the testing region. It is also used as the Block_Size_Bits_Col value to set the size of the block. Minimum value is 1 if Address_Decode_Enable =1. , so this normally needs to be set to the number of Column bits of the memory.
19:16	0h RW	**Block Ranks Size (Block_Size_Num_Ranks):** Number of Ranks to test for a Block (as N-1 = top rank number). All Rank Addresses go through the Rank Address Lookup table.
15:12	0h RW	**Block Banks Size (Block_Size_Num_Banks):** Number of Banks to test for a Block (as N-1 = top bank number). All Bank Address values go through the Bank Address Lookup table.
11:9	0h RO	Reserved.
8:4	0h RW	**Block Row Size (Block_Size_Bits_Row):** 2^Block_Size_Bits_Row is the number of rows for a Block. If block traversal is used, then this must be at least 4 rows (=2). Minimum value is 1 if Address_Decode_Enable =1.
3:0	0h RW	**Block Column Size (Block_Size_Bits_Col):** Reserved for use as Block_Size_Bits_Col - Fixed as same as Region_Size_Bits_Col for the SoC. There is no column traversal of a block.

5.11.106 Base Address Control (CPGC2_BASE_ADDRESS_CONTROL)—Offset 48C0h

Control handling of Base Address - inversion and increment rates and increment amounts.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26	0h RW	**Address Inversion Rate (Address_Inversion_Rate):** Address_Inversion_Rate determines if the enabled Address Fields toggle inversion on the Command Sequence Boundary (following a Command_Instruction with the Last bit set) or every Command_Instruction. 0 Invert enabled Address fields after executing the Command_Instruction with the Last bit set. 1 Invert enabled Address fields following each Command_Instruction
25:22	0h RW	**Address Inversion Enable (Address_Inversion_Enable):** Address_Inversion_Enable enables particular Address Fields to be inverted. [25] Rank_Inversion_Enable. [24] Bank_Inversion_Enable. [23] Row_Inversion_Enable. [22] Col_Inversion_Enable.
21	0h RW	**Address Increment Rate (Address_Order0_Inc_Rate):** Address_Order0_Inc_Rate determines if the Address Order 0 Field is incremented on the Command Sequence Boundary (following a Command_Instruction with the Last bit set) or every Command_Instruction. 0 Increment Address after executing the Command_Instruction with the Last bit set. 1 Increment Address following each Command_Instruction.
20:18	0h RO/V	**Rank Increment (Fixed) (Reserved_Rank_Inc):** All Base Rank addresses are incremented (or decremented) by 2^Rank_Inc (unsigned value).
17:15	0h RO/V	**Bank Increment (Fixed) (Reserved_Bank_Inc):** All Base Bank addresses are incremented (or decremented) by 2^Bank_Inc (unsigned value).
14:11	0h RW	**Column Increment (Col_Inc):** All Base and Offset Column addresses are incremented (or decremented) by 2^Col_Inc (unsigned value).

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO	Reserved.
9:6	0h RW	**Row Increment (Row_Inc):** All Base and Offset Row addresses are incremented (or decremented) by 2^Row_Inc (unsigned value).
5	0h RW	**Block Move Half Block (Block_Move_Half_Block):** if Block_Move_One_Row =1 then the Block is moved by 1 row Else if Block_Move_Half_Bock = 1 then the Block is moved by 2^(Block_Size_Bits_Row)/2 Rows Else the Block is moved by = 2^(Row_Block_Size).
4	0h RW	**Block Move One Row (Block_Move_One_Row):** See Block_Move_Half_Block for description.
3:0	0h RO	Reserved.

5.11.107 Address PRBS Control (CPGC2_ADDRESS_PRBS_CONTROL)—Offset 48C4h

Control PRBS Address generator.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25	0h RW	**Address_PRBS_High Row map enable (Address_PRBS_High_Row):** The higher order bits of the PRBS Address Generator (bits 3 through Address_PRBS_Size-1) will be on the same Row bits when the PRBS Address is selected.
24	0h RW	**Address_PRBS_High Column map enable (Address_PRBS_High_Col):** The higher order bits of the PRBS Address Generator (bits 3 through Address_PRBS_Size-1) will be on the same Column bits when the PRBS Address is selected.
23:18	0h RO	Reserved.
17	0h RW	**Address_PRBS_Mid Row map enable (Address_PRBS_Mid_Row):** Bits [2:1] of the Row address will be bits [2:1] of the PRBS Address Generator when the PRBS Address is selected.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Address_PRBS_Mid Column map enable (Address_PRBS_Mid_Col):** Bits [2:1] of the Column address will be bits [2:1] of the PRBS Address Generator when the PRBS Address is selected.
15:10	0h RO	Reserved.
9	0h RW	**Address_PRBS_Low Row map enable (Address_PRBS_Low_Row):** LSB of Row address will be the LSB of the PRBS Address Generator when the PRBS Address is selected.
8	0h RW	**Address_PRBS_Low Column map enable (Address_PRBS_Low_Col):** LSB of Column address will be the LSB of the PRBS Address Generator when the PRBS Address is selected.
7	0h RW	**Address PRBS Enable (Address_PRBS_Enable):** If Address_PRBS_Enable is active, and Address_Decode_Enable is not active in the current Address_Instruction, thenn each command is enabled to use the PRBS address if the Address_Decode_or_PRBS_En bit is set.
6:4	0h RO	Reserved.
3:0	0h RW	**Address PRBS Size (Address_PRBS_Size):** Size of PRBS for address generation if Address_PRBS_Enable is active. See text for PRBS Polynomials being used for each setting.

5.11.108 Address PRBS Seed (CPGC2_ADDRESS_PRBS_SEED)—Offset 48C8h

Seed for Address PRBS generator.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:0	0h RW	**Address PRBS Seed (Address_PRBS_Seed):** Seed for Address PRBS generator.

5.11.109 Current Address PRBS Status (CPGC2_ADDRESS_PRBS_CURRENT)—Offset 48CCh

Current value of Address PRBS generator.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:0	0h RO/V	**Current Address PRBS (Address_PRBS_Current):** Current value of Address PRBS generator. Address advances as Address_Order0_Inc_Rate. The Seed is re-loaded (from Save) at each Algorithm_Instruction boundary.

5.11.110 Address PRBS Save (CPGC2_ADDRESS_PRBS_SAVE)—Offset 48D0h

Currently saved Address PRBS seed.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:0	0h RO/V	**Address PRBS Save (Address_PRBS_Save):** Saved value of Address PRBS generator. Value is saved automatically during block advance, and restored (from Seed) when Block Traversal (Repeats) is complete.

5.11.111 Command FSM Current State (CPGC2_CMD_FSM_CURRENT)—Offset 48D4h

Current state of Command FSM - used at stop-on-error to determine the current progress in the test at the time of the error.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:28	0h RO/V	**Address Instuction Pointer (Address_Instruction_Current):** Current Address_Instruction pointer.
27:26	0h RO	Reserved.
25:24	0h RO/V	**Data Instruction Pointer (Data_Instruction_Current):** Current Data_Instruction pointer.
23:18	0h RO	Reserved.
17:15	0h RO/V	**Algorithm Instruction Pointer (Algorithm_Instruction_Current):** Current Algorithm_Instruction pointer.
14:13	0h RO	Reserved.
12:8	0h RO/V	**Command Instruction Pointer (Command_Instruction_Current):** Current Command_Instruction pointer.
7	0h RO	Reserved.
6	0h RO/V	**Offset Group Select Pointer (Offset_Group_Instruction_Current):** Current Offset_Group as pointed to by the Current Command_Instruction (if an Offset instruction).
5:3	0h RO/V	**Offset Address Instruction Pointer (Offset_Address_Instruction_Current):** Current Offset_Address_Instruction pointer.
2:0	0h RO/V	**Offset Command Instruction Pointer (Offset_Command_Instruction_Current):** Current Offset_Command_Instruction pointer.

5.11.112 Algorithm Wait Timer Configuration (CPGC2_WAIT_2_START_CONFIG)—Offset 48D8h

Configure the timebase for the Algorithm Wait Timer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Increment value (Increment_Value):** See Prescaler field for information on this field.

Bit Range	Default & Access	Field Name (ID): Description
27:26	0h RO	Reserved.
25:16	0h RW	**Clock Frequency (Clock_Freq):** When a setting of 1MHz or 1KHz is used in Wait_Clock_Frequency, this field provides a way to tell the hardware the native Memory Controller clock frequency, which is fed into the Prescaler automatically (with a 1 Increment_Value also automatically fed into the counter).
15:10	0h RO	Reserved.
9:0	0h RW	**Prescaler (Prescaler_for_Clock_Freq):** In order to make the 'standard' 1 GHz clock for the CPGC specified Wait_Clock_Frequency setting, we need to provide a pre-scaler, and Increment Value to modify the existing Wait_Timer_Current advancement. This field will divide the native Memory Controller clock by the provided value, with '1' being 'No Divide'. After that divide, the Wait_Timer_Current will advance by the 'Increment_Value' field. In this way, we are creating a clock ratio able to 'multiply' the native Memory Controller clock by 'Increment_Value/Prescaler'. For small values of Wait_Time, the error will be substantial, and it may be better to modify the programming to the '11' Native Clock setting and manually compute the required Wait_Time for the desired delay.

5.11.113 VISA Mux Selection (CPGC2_VISA_MUX_SEL)—Offset 48DCh

Selection for VISA mux controls.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:13	0h RW	**Error Group 1 (Err1_grp_Sel):** Err Group 1 Select.
12:11	0h RW	**Error Group 0 (Err0_grp_Sel):** Err Group 0 Select.
10:9	0h RW	**DPAT Group 1 (Dpat1_grp_Sel):** Dpat Group 1 Select.
8:7	0h RW	**DPAT Group 0 (Dpat0_grp_Sel):** Dpat Group 0 Select.
6:5	0h RW	**Command Group 1 (Cmd1_grp_Sel):** Cmd Group 1 Select.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Command Group 0 (Cmd0_grp_Sel):** Cmd Group 0 Select.
2	0h RW	**Error-Command (Err1_or_Cmd1):** Err group 1 or Cmd group 1 select.
1	0h RW	**Command-DPAT (Cmd0_or_Dpat1):** Cmd group 0 or Dpat group 1 select.
0	0h RW	**DPAT-Error (Dpat0_or_Err0):** Dpat group 0 or Err group 0 select.

5.11.114 Loopback Squencer Configuration (CPGC_LB_SEQ_CFG)—Offset 48E0h

Loopback Sequencer Config.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Start Test Delay (START_TEST_DELAY):** Start_Test_Delay is the delay period (in byte clocks) to execute a test(i.e transition to Loopback.Pattern) after the link is in Loopback.Idle and Local_Start_Test is asserted. If Local_Start_Test is set upon the initial entry to Loopback.Idle then a test (entry to Loopback.Pattern) will immediately start after Start_Test_Delay number of byte clocks is enforced. During Start_Test_test the Valid must not be asserted (i.e Loopback.PM) and no comparison of data will be taking place. Start_Test_Delay=0 is reserved and not allowed. Start_Test_Delay=1 will result in a 1byte clock delay. Start_Test_Delay=2 will result in a 2byte clock delay.
23:21	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20:16	0h RW	**Loopcount (LOOPCOUNT):** 2^(Loopcount) determines the length of a test. One Loopcount consists of Pattern_Length followed by PM_Length. Pattern_Length corresponds to the Loopback Master generating patterns and the Loopback.Slave and/or Loopback Master performing error checking occueeing (valid is assered). PM_Length corresponds to the functional power savings mode (valid is not asserted). Loopcount=0 means the test is infinite. Loopcount=1 means the test will end after two loops. Loopcount=2 means the test will end after four loops. Loopcount=3 means the test will end after eight loops.
15:8	0h RW	**PM Length (PM_LENGTH):** PM_Length(i.e Loopback.PM) forms the second half of the loopcount sequence with Pattern_Length (i.e Loopback.Pattern)forming the first half. PM_Length is used in conjection with Pattern_Length and Loopcount to go in and out of Power Savings Modes in an identical way to how the functional power saving mode behave. This includes post amble, pre-amble, etc. PM_Length duration is defined in total # of byte clocks. If PM_Length is set to 0 then no power saving modes will be entered. If the end of the test has not been reached, (Curren_Loopcount !=Loopcount) the loopcount is incremented and the sequence repeats (Pattern_Length followed by PM_Length). If the end of the test has not been reached (Current_Loopcount=Loopcount) the link transitions back to Loopback.Idle following the PM state.
7:0	0h RW	**Pattern Length (PATTERN_LENGTH):** Pattern_Length (i.e Loopback.Pattern) forms the first half of the Loopcount sequence with PM_Length (i.e Loopback.PM) forming the second half. Pattern_Length is the portion of Loopcount when patterns are generated(Loopback Master) and compared (Loopback Master and optionally the Loopback Slave). Pattern_Length suration is defined in total # of byte clocks. A zero value is illegal. The Sum of Pattern_Length and PM_Length (Duration of a Loopcount)must always be set to a value of two or more.

5.11.115 Loopback Sequencer Control (CPGC_LB_SEQ_CTL)—Offset 48E4h

Loopback sequencer control.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:12	0h RW	**Initialization Mode (INITIALIZATION_MODE):** A change to Initialization_Mode occurs immediately. 00 - OFF - REUT is clock gated. 01 - LSM Mode - Enter Loopback.Idle state through the appropriate Link Layer bits as a Loopback Master or Loopback Slave. 10 - Force Master - Force entry to Loopback.Idle as a Loopback Master (Supported if Force_Loopback capability is set). 11 - Force Slave - Force entry to Loopback.Idle as Loopback Slave (Supported if Force_Loopback capability is set). Note: A user must be careful to transition both sides of the Link to Loopback.Idle if switching Initialization_Mode from Force Master or Force Slave to LSM Mode or undefined behavior can be expected. Note: Initialization Mode should not be changed while Local_Start_Test is set, or while Test_In_Progress is set.
11:7	0h RO	Reserved.
6	0h RW	**Bind Stop on Error (BIND_STOP_ON_ERROR):** Test will stop based on Global_Error (external input) and Local_Error will drive Global_Error.
5	0h RW	**Bind Clear Errors (BIND_CLEAR_ERRORS):** Local_Clear_Errors will clear all other REUT instances that have this bit set.
4	0h RW	**Bind Stop Test (BIND_STOP_TEST):** Local_Stop_Test will stop all other REUT instances that have this bit set.
3	0h RW	**Bind Start Test (BIND_START_TEST):** Local_Start_Test will start all other REUT instances that have this bit set.
2	0h RW/V	**Local Clear Errors (LOCAL_CLEAR_ERRORS):** Setting Local_Clear_Errors to 1 will immediately clear all local Error registers (i.e. CPGC_ERR_* registers). Local_Clear_Errors will immediately clear to 0 after clearing affected registers. If this bit fails to auto-clear, then there is no clock and the clear will occur at the start of the next test.
1	0h RW/V	**Local Stop Test (LOCAL_STOP_TEST):** If Local_Stop_Test is set to 1 and a Loopback test is in progress (i.e. Test_In_Progress=1) then a transition to Loopback. Idle will occur as soon as possible (i.e. Link enters Loopback.PM). Local_Stop_Test will immediately clear to 0 after stopping a Loopback test (i.e. Local_Stop_Test=0 while in Loopback.Idle).

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Local Start Test (LOCAL_START_TEST):** If Local_Start_Test is set a Sequence will immediately start, or wait until entry to Loopback state. A complete Sequence is defined by the following behavior: 1) An initial delay of Start_Test_Delay byte clocks must first occur in Loopback.PM (with Valid de-asserted). 2) Transition to Loopback.Pattern (Valid asserted) for a duration of Pattern_Length Byte clocks during which data is generated and compared by the Loopback Master and optionally compared by the Loopback Slave. 3) Increment Loopcounter. 4) Optionally Transition to Loopback.PM (with Valid deasserted), if so programmed, for a duration of PM_Length Byte clocks during which power modes are functionally enforced as what would happen normally based on the length of the PM_Length duration. 5) If Current Loopcount !=2^Loopcount then go to step 2. 6) If Current Loopcount !=2^Loopcount then the Link returns to Loopback.Idle, Local_Start_Test is cleared for the Master. Local_Start_Test is not cleared on the Loopback.Slave.

5.11.116 Loopback Loopcount Tx Status (CPGC_LB_SEQ_LOOPCOUNT_TX_STATUS)—Offset 48E8h

Indicates the current TX Loopcount value in the Sequence.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current Loopcount (CURRENT_LOOPCOUNT):** Current_Loopcount indicates how many times the full Sequence has been executed in the TX path. Current_Loopcount is cleared by Local_Clear_Errors.

5.11.117 Loopback Loopcount Rx Status (CPGC_LB_SEQ_LOOPCOUNT_RX_STATUS)—Offset 48ECh

Indicates the current RX Loopcount value in the Sequence.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current Loopcount (CURRENT_LOOPCOUNT):** Current_Loopcount indicates how many times the full Sequence has been executed in the RX path. Current_Loopcount is cleared by Local_Clear_Errors.

5.11.118 Pattern Length Status (CPGC_LB_SEQ_PL_RX_STATUS)—Offset 48F0h

Indicates how many Bytes are left in Loopback.Pattern.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RO/V	**Current Pattern Length (CURRENT_PATTERN_LENGTH):** Current_Pattern_Length is used in conjuntion with Stop_On_Error_Control conditons to determine where the last failure occurred within Loopback.Pattern. Current_Pattern_Length indicates how many Bytes were left in Loopback.Pattern when the error occurred. Current_Pattern_Length is cleared by Local_Clear_Errors.

5.11.119 Refresh Control (CPGC_MISC_REFRESH_CTL)—Offset 48F4h

CPGC MISC REFRESH CTL

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Panic Refresh Only (PANIC_REFRESH_ONLY):** Reserved
30:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Start Test on RefZQ (REFZQ_EN_START_TEST_SYNC):** Reserved
7:4	0h RO	Reserved.
3:0	0h RW	**Rank Mask of Refresh (REFRESH_RANK_MASK):** Reserved

5.11.120 ZQ Control (CPGC_MISC_ZQ_CTL)—Offset 48F8h

CPGC MISC ZQ CTL

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Always do ZQ (ALWAYS_DO_ZQ):** Reserved
30:2	0h RO	Reserved.
1:0	0h RW	**Rank Mask of ZQ (ZQ_RANK_MASK):** Reserved

5.11.121 ODT Control (CPGC_MISC_ODT_CTL)—Offset 48FCh

CPGC MISC ODT CTL

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**DDR Training MPR Pattern (MPR_Train_DDR_On):** Reserved
30:18	0h RO	Reserved.
17:16	0h RW	**Rank ODT On (ODT_ON):** Reserved
15:2	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Rank ODT Override (ODT_OVERRIDE):** Reserved

5.11.122 CKE Control (CPGC_MISC_CKE_CTL)—Offset 4900h

CPGC MISC CKE CTL

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:16	0h RW	**Rank CKE On (CKE_ON):** Reserved
15:9	0h RO	Reserved.
8	0h RW	**Start Test on CKE (CKE_EN_START_TEST_SYNC):** Reserved
7:2	0h RO	Reserved.
1:0	0h RW	**Rank CKE Override (CKE_OVERRIDE):** Reserved

5.11.123 Command Rate (CPGC_MISC_CMD_RATE)—Offset 4904h

CPGC CMD_RATE

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 100Ah

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**MRW uses 2 clocks CS (init_mrw_2n_cs):** Reserved
30:14	0h RO	Reserved.
13:12	1h RW	**CK to CKE delay (ck_to_cke_delay):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RW	**Reset Delay (reset_delay):** Reserved
7:4	0h RW	**Reset On Command (reset_on_command):** Reserved
3:1	5h RW	**Command Rate Limit (cmd_rate_limit):** Reserved
0	0h RW	**Enable Command Rate Limit (enable_cmd_rate_limit):** Reserved

5.11.124 External Trigger Control (CPGC_MISC_EXT_TRIGGER)—Offset 4908h

CPGC MISC EXT TRIGGER

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RW	**Trigger Out on Test Done (TRIGGER_OUT_ON_TEST_DONE):** Reserved
2	0h RW	**Trigger Out on Error (TRIGGER_OUT_ON_ERROR):** Reserved
1	0h RW	**Trigger Out on Start (TRIGGER_OUT_GLOBAL_START):** Reserved
0	0h RW	**Trigger in to Start (TRIGGER_IN_GLOBAL_START):** Reserved

5.11.125 Sequence Control (CPGC_SEQ_CTL)—Offset 490Ch

Sequence Control Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	0h RW/V	**Continue Single Step (CONTINUE_SINGLE_MODE):** When in Single_Command_Mode setting this bit will enable a new command to be issued. This bit immediately clears after being set.
8	0h RW	**Single Step/Cmd Mode (SINGLE_CMD_MODE):** Enter Single Command mode were we will issue one command from CPGC and then pause command issuing. This may be resumed by setting Continue_Single_Mode, or normal continuous operation resumed by clearing this bit.
7:3	0h RO	Reserved.
2	0h RW/V	**Clear Errors (CLEAR_ERRORS):** Setting this bit will immediately clear all error registers and error status. This bit will automatically self clear.
1	0h RW/V	**Stop Test (STOP_TEST):** Forces an exit from the tests running on this engine/channel. Note that this will also cause a test stop for all engines with GLB_STOP_BIND set. This bit will self clear.
0	0h RW/V	**Start Test (START_TEST):** Used to initiate a transition to active mode on this engine/channel (note that INIT_MODE has to be programmed first). Note that this will also cause a test start for all engines with GLB_START_BIND set. This bit will self clear.

5.11.126 Sequence Configuration A (CPGC_SEQ_CFG_A)—Offset 4910h

Sequence Configuration Low Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 200000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22	0h RW	**Request Data Size (REQUEST_DATA_SIZE):** Size of requests CPGC is issuing, 64B and 32B transactions and is encoded as follows: 0 - 32 Byte Transactions 1 - 64 Byte Transactions

Bit Range	Default & Access	Field Name (ID): Description
21	1h RW	**CPGC Control (CPGC_CONTROL):** Used to indicate the OPIO(MCDRAM) or CPGC(DDR) mode. 1 - CPGC Mode. 0 - OPIO Mode.
20:15	0h RO	Reserved.
14:12	0h RW	**Initialization Mode (INITIALIZATION_MODE):** 000 - IDLE MODE 001 - ACTIVE MODE 010 - DIRECT MODE 011 - ACTIVE MODE 100 - MRS MODE 101 - ERROR DUMP MODE (Reserved) 110 - WDB FILL MODE (Reserved) 111 - REWIND MODE (Reserved)
11	0h RW	**Bind Stop Test (GLOBAL_STOP_BIND):** Setting this bit will bind this channel engine to all other channel engines. A test stop (both forced and due to a stop condition) for any channel engine with GLOBAL_STOP_BIND set will cause the same action to occur on all engines with GLOBAL_STOP_BIND set. This feature is usually used when synchronization between multiple engines/ channels necessitates a global control of all supported engines. Note: this field is only available if multiple channels/engines are supported for the current implementation, otherwise it is reserved.
10	0h RW	**Bind Start Test (GLOBAL_START_BIND):** Setting this bit will bind this channel engine to all other channel engines. A test start for any channel with GLOBAL_START_BIND set will cause the same action to occur on all engines with GLOBAL_START_BIND set. This feature is usually used when synchronization between multiple engines/channels necessitates a global control of all supported engines. Note: this field is only available if multiple channels/engines are supported for the current implementation, otherwise it is reserved.
9	0h RW	**Bind Stop-on-Error (GLOBAL_STOP_ON_ERR_BIND):** Setting this bit will bind this channel engine to all other channel engines. A test stop (due to an error condition) for any channel with GLOBAL_STOP_ON_ERR_BIND set will cause the same action to occur on all engines with GLOBAL_STOP_ON_ERR_BIND set. This feature is usually used when synchronization between multiple engines/channels necessitates a global control of all supported engines. Note: this field is only available if multiple channels/engines are supported for the current implementation, otherwise it is reserved.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Bind Clera Errors (GLOBAL_CLEAR_ERR_BIND):** Setting this bit will bind this channel engine to all other channel engines. Clearing all error registers and error status for any channel with GLOBAL_CLEAR_ERR_BIND set will cause the same action to occur on all engines with GLOBAL_CLEAR_ERR_BIND set. This feature is usually used when synchronization between multiple engines/channels necessitates a global control of all supported engines. Note: this field is only available if multiple channels/engines are supported for the current implementation, otherwise it is reserved.
7	0h RO	Reserved.
6	0h RW	**Constant Write Strobe (ENABLE_CONSTANT_WRITE_STROBE):** Reserved
5:0	0h RO	Reserved.

5.11.127 Sequence Configuration B (CPGC_SEQ_CFG_B)—Offset 4914h

Sequence Config High.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW	**Start Delay (START_DELAY):** Number of clock cycles (in CPGC-S clock domain) the start of the test is delayed by after START_TEST has been asserted by the user. This is usually used to synchronize multiple SoC CPGC engines on multiple channels according to a defined phase relationship.

5.11.128 Sequence Status (CPGC_SEQ_STATUS)—Offset 4918h

Sequence Test Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Test Done (TEST_DONE):** This bit will be set when the test is complete (or has been forced to exit due to a stop condition). Bit is cleared on a reset or when user starts another test.
30	0h RO/V	**Test Busy (TEST_BUSY):** This bit will be set when once a test has started. Bit is cleared on a reset or once test is done (or has been forced to exit due a stop condition).
29	0h RO/V	**Algorithm Done (ALGO_DONE):** This bit will be set when all the algorithms are complete. It is cleared on a reset.
28	0h RO/V	**Single Step/Cmd Paused (SINGLE_MODE_PAUSED):** This bit will be set when a command has been issued and we are paused due to Single_Command_Mode. The test may be continued by either clearing Single_Command_Mode or by setting Continue_Single_Mode.
27:0	0h RO	Reserved.

5.11.129 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[0])—Offset 4920h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.130 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[1])—Offset 4924h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.131 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[2])—Offset 4928h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.132 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[3])—Offset 492Ch

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.133 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[4])—Offset 4930h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.134 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[5])—Offset 4934h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.135 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[6])—Offset 4938h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.136 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[7])—Offset 493Ch

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.137 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[8])—Offset 4940h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.138 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[9])—Offset 4944h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.139 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[10])—Offset 4948h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.140 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[11])—Offset 494Ch

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.141 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[12])—Offset 4950h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.142 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[13])—Offset 4954h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.143 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[14])—Offset 4958h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.144 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[15])—Offset 495Ch

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.11.145 Mode3 Fail Status LSB (CPGC2_RASTER_REPO_CONTENT_ECC1)—Offset 4960h

Lower half of the Raster Repository Mode3 Fail Status.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO/V/P	**ECC Chunk 3 (ECC_chunk3):** ECC chunk 3 raster when in Mode 1.
27:26	0h RO/V/P	**Bank3 Fail Count (fail_count3):** Bank 3 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.
25	0h RO/V/P	**Bank3 Any Fail (fail_any3):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
24	0h RO/V/P	**Bank3 Excessive Fail (fail_excess3):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.
23:20	0h RO/V/P	**ECC Chunk 2 (ECC_chunk2):** ECC chunk 2 raster when in Mode 1.
19:18	0h RO/V/P	**Bank2 Fail Count (fail_count2):** Bank 2 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.
17	0h RO/V/P	**Bank2 Any Fail (fail_any2):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
16	0h RO/V/P	**Bank2 Excessive Fail (fail_excess2):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.
15:12	0h RO/V/P	**ECC Chunk 1 (ECC_chunk1):** ECC chunk 1 raster when in Mode 1.
11:10	0h RO/V/P	**Bank1 Fail Count (fail_count1):** Bank 1 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO/V/P	**Bank1 Any Fail (fail_any1):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
8	0h RO/V/P	**Bank1 Excessive Fail (fail_excess1):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.
7:4	0h RO/V/P	**ECC Chunk 0 (ECC_chunk0):** ECC chunk 0 raster when in Mode 1.
3:2	0h RO/V/P	**Bank0 Fail Count (fail_count0):** Bank 0 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.
1	0h RO/V/P	**Bank0 Any Fail (fail_any0):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
0	0h RO/V/P	**Bank0 Excessive Fail (fail_excess0):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.

5.11.146 Mode3 Fail Status MSB (CPGC2_RASTER_REPO_CONTENT_ECC2)—Offset 4964h

Upper half of the Raster Repository Mode3 Fail Status.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO/V/P	**ECC Chunk 7 (ECC_chunk7):** ECC chunk 7 raster when in Mode 1.
27:26	0h RO/V/P	**Bank7 Fail Count (fail_count7):** Bank 7 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.
25	0h RO/V/P	**Bank7 Any Fail (fail_any7):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
24	0h RO/V/P	**Bank7 Excessive Fail (fail_excess7):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.
23:20	0h RO/V/P	**ECC Chunk 6 (ECC_chunk6):** ECC chunk 6 raster when in Mode 1.
19:18	0h RO/V/P	**Bank6 Fail Count (fail_count6):** Bank 6 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO/V/P	**Bank6 Any Fail (fail_any6):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
16	0h RO/V/P	**Bank6 Excessive Fail (fail_excess6):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.
15:12	0h RO/V/P	**ECC Chunk 5 (ECC_chunk5):** ECC chunk 5 raster when in Mode 1.
11:10	0h RO/V/P	**Bank5 Fail Count (fail_count5):** Bank 5 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.
9	0h RO/V/P	**Bank5 Any Fail (fail_any5):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
8	0h RO/V/P	**Bank5 Excessive Fail (fail_excess5):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.
7:4	0h RO/V/P	**ECC Chunk 4 (ECC_chunk4):** ECC chunk 4 raster when in Mode 1.
3:2	0h RO/V/P	**Bank4 Fail Count (fail_count4):** Bank 4 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.
1	0h RO/V/P	**Bank4 Any Fail (fail_any4):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
0	0h RO/V/P	**Bank4 Excessive Fail (fail_excess4):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.

5.11.147 Read Command Count (CPGC2_READ_COMMAND_COUNT_CURRENT)—Offset 4968h

Current count of reads.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Current Read Command Count (Read_Command_Count_Current):** Current count of reads - freezes on stop_on_error conditions at the number of reads including the error that caused the stop.

5.11.148 Mask Errors on First N Reads (CPGC2_MASK_ERRS_FIRST_N_READS)—Offset 496Ch

Masking for the first N read operations - all errors are ignored.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/P	**Mask First N Reads (Mask_First_N_Reads):** 0=no masking, N= number of reads that will not result in any error indication for the raster repository.

5.11.149 Raster Repository Status (CPGC2_RASTER_REPO_STATUS)—Offset 4970h

Raster repository status.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Raster Repository Clear (RasterRepoClear):** Reset the raster repo entries. This bit auto-clears.
30	0h RW/P	**Stop on Raster Full (StopOnRaster):** If Raster Mode 1, test will stop after loading the bitmap into the raster. If Raster Mode 2, test will stop after loading 8 errors in the raster.
29:18	0h RO	Reserved.
17:16	0h RW/P	**Raster Repository Mode (RasterRepoMode):** 00 Mode 1 BitMap Mode. 01 Mode 2 Summary Mode. 10 mode 3 Filtered Failed Row Mode.
15:12	0h RO	Reserved.
11:10	0h RW/P	**Excess Failure Maximum (FailMax):** Maximum number of failing address before an additional failing address will set fail_excess for any bank. 00 one failure, 01 - two failures, 10 - three failures, 11- four failures.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO/V/P	**Summary Any Fail (FailAnyAll):** 0 - indicates no failing addresses. 1 - indicates 1 or more failing addresses.
8	0h RO/V/P	**Summary Excessive Fail (FailExcessAll):** 0 - indicates less than or exactly max_fail failing addresses on all banks. 1 - indicates at least one bank's errors exceed the max_fail limit.
7	0h RO	Reserved.
6:4	0h RO/V/P	**Number of Summary Entries (NumErrLogged):** Indicates the current number of errors loaded in the raster repo in Mode 2. Max value is 8.
3	0h RO	Reserved.
2	0h RO/V/P	**Raster Repository Full (RasterRepoFull):** Indicates when the no. of errors logged exceed max value of 8.
1	0h RO/V/P	**Summary Valid (SummaryValid):** Indicates when the summary information of the erroneous bitmap is loaded in the current summary buffer. This information consist of Algorithmic data, Physical Addr (Rank, Bank,Row,Col) and 8 2-bit error summary for every chunk.
0	0h RO/V/P	**Bitmap valid (BitmapValid):** Indicates when Mode 1 erroneous bitmap data is loaded in the raster repo.

5.11.150 Error Summary A (CPGC2_ERR_SUMMARY_A)—Offset 4974h

Most recent error sumary data, not yet written to the Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V/P	**Algorithm Summary (Algorithm_Summary):** Algorithm_Summary - currently formated as: [2:0] Offset_Command_Instruction_Current. [5:3] Offset_Address_Instruction_Current. [10:6] Command_Instruction_Current. [13:11] Algorithm_Instruction_Current. [15:14] Data_Instruction_Current.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V/P	**Error Summary (Error_Summary):** Error_Summary - formatted as a pair of adjacent bits for each chunk, 00=no error in that chunk, 01=one error in that chunk, 10=two errors in that chunk, 11=three or more errors in that chunk.

5.11.151 Error Summary B (CPGC2_ERR_SUMMARY_B)—Offset 4978h

Most recent error sumary data, not yet written to the Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO/V/P	**Physical Address (Physical_Address_Summary):** Error_Summary - Physical Address encoded as: [7:0] Column, [25:8] Row, [28:26] Bank, [29] Rank.
1:0	0h RO/V/P	**Algorithm Summary (Algorithm_Summary):** Algorithm_Summary - currently formated as: [1:0] Address_Instruction_Current.

5.11.152 Future use Reserved (CPGC2_ERR_SUMMARY_C)—Offset 497Ch

Reserved for expansion of Error_Summary.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Future use Reserved (DG_Reserved):** Reserved for expansion of Error_Summary (bits 7:0).

5.11.153 Data Pattern Generation Buffer Control (CPGC_DPAT_BUF_CTL)—Offset 4980h

Data Pattern Buffer Control Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:24	0h RO/V	**Read Buffer Pointer (RD_BUF_PTR):** Pointer to current entry in the data pattern buffers used for generating the read data.
23:20	0h RO/V	**Write Buffer Pointer (WR_BUF_PTR):** Pointer to current entry in the data pattern buffers used for generating the write data.
19	0h RO	Reserved.
18:16	0h RW	**Buffer End Pointer (BUF_END_PNTR):** Pointer to last data pattern buffer entry before wrapping back to BUF_STRT_PTR if incrementing is enabled through being different from BUF_STRT_PTR. Note: The actual size of this field depends on the # of lines supported for data generation. i.e If 1 or 2 lines are supported then it is a 1 bit field, if 8 lines are supported then 3 bits are available. Currently the RTL uses internal CPGC buffers so it has 4 lines and requires 2 bits.
15:11	0h RO	Reserved.
10:8	0h RW	**Buffer Start Pointer (BUF_STRT_PNTR):** Pointer to first buffer entry. Also used as the only entry if BUF_INC_EN is not enabled. Note: The actual size of this field depends on the # of lines supported for data generation (DATA_PAT_DEPTH_CAP), i.e If 1 or 2 lines are supported then it is a 1 bit field, if 16 lines are supported then the whole 4 bits are available. Currently the RTL uses internal CPGC buffers so it has 8 lines and requires 3 bits.
7	0h RO	Reserved.
6	0h RW	**Buffer Pointer Increment Scale (BUF_PNTR_INC_SCALE):** If set, the buffer pointer will be incremented at a linear rate given by BUF_PTR_INC_RATE, otherwise the buffer pointer will be incremented at an exponential rate given by BUF_PTR_INC_RATE. 1=Buffer Pointer Increment Rate field is treated as a linear number. 0=Buffer Pointer Increment Rate field is treated is an exponential number.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Buffer Pointer Increment Rate (BUF_PNTR_INC_RATE):** 0: Each buffer entry will be used for 2^BUF_PTR_INC_RATE number of bursts (64Bytes). 1: Each buffer entry will be used for BUF_PTR_INC_RATE + 1 number of 8-UI -- before incrementing the buffer pointer by 1. Note: To disable Buffer Pointer increments, set BUF_END_PTR==BUF_STRT_PTR.

5.11.154 Data Pattern Generation Configuration (CPGC_DPAT_CFG)—Offset 4984h

Data Pattern Configuration Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:24	0h RW	**Reload LFSR Seed Rate (RELOAD_LFSR_SEED_RATE):** Reload_LFSR_Seed_Rate only exists if the LFSR_Save_Restore capability is set to 1. Reload_LFSR_Seed_Rate and Save_LFSR_Seed_Rate is most often used in conjunction with Lane_Rotate_Rate where the user desires to replay the same deterministic LFSR stress as the victim aggressor patterns shifts Lanes left. When the victim aggressor pattern returns to the starting position the current LFSR stress is saved using Save_LFSR_Seed_Rate to allow the LFSR stress to advance for the new period. 2^(Reload_LFSR_Seed_Rate-1) defines the periodic Loopcount interval that the current LFSR Seed UNISEQ#_RDSTAT.Uniseq_RdStat is reloaded from CPGC_UNISEQ#_RDSAVE.Pattern_Buffer. When the Save_LFSR_Seed_Rate and Reload_LFSR_Seed_Rate is reached in the same Bit only the saving of the LFSR seed takes place. Examples: 0=Disable - The current LFSR seed is never reloaded. 1=The current LFSR seed is reloaded every Loopcount. 2=The current LFSR seed is reloaded every other Loopcount. 3=The current LFSR seed is reloaded every fourth Loopcount.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RW	**Save LFSR Seed Rate (SAVE_LFSR_SEED_RATE):** Save_LFSR_Seed_Rate only exists if the LFSR_Save_Restore capability is set to 1. See Reload_LFSR_Seed_Rate for use model. UNISEQ#_RDSAVE.Pattern_Buffer is initially loaded at the start of a test with UNISEQ#_RDSTAT.Uniseq_RdStat (the Seed). 2^(Reload_LFSR_Seed_Rate-1) * (Save_LFSR_Seed_Rate) defines the periodic Loopcount interval that the current LFSR Seed is saved into UNISEQ#_RDSAVE.Pattern_Buffer. When the Save_LFSR_Seed_Rate and Reload_LFSR_Seed_Rate is reached in the same Loopcount only the saving of the LFSR seed takes place. Examples: 0=Disable - The current LFSR seed (UNISEQ#_RDSTAT.Uniseq_RdStat) is saved only at the start of test into UNISEQ#_RDSAVE.Pattern_Buffer. 1=Illegal (Would save every Reload and effectively disable both Save and Reload). 2=The current LFSR seed is saved every other 2^(Reload_LFSR_Seed_Rate-1) Loopcounts. 3=The current LFSR seed is saved every third Reload (and Reload does not happen).
15	0h RW	**Reserved for future use (ECC_DATA_SOURCE_SEL):** Indicates whether byte 0 (Dq0-Dq7) or byte 7 (dq56-dq63) is transmitted and compared for the ECC byte. 0=byte group 0 will be transmitted and compared for the ECC byte. 1=byte group 7 will be transmitted and compared for the ECC byte. Hardware directs if ECC is included within Generation and Checking. This bit may be reserved if ECC is not supported, or if this functionality is controlled from a different register.
14	0h RW	**Reserved for future use (ECC_REPLACE_BYTE_CONTROL):** ECC_Replace_Byte_Control is used by the Read data path to mux the received ECC byte into the same byte group indicated by ECC_Data_Source_Sel. This is needed to capture ECC cacheline errors into the WDB when Enable_WDB_Error_Capture is set to 1. This bit may be reserved if ECC is not supported, or if this functionality is controlled from a different register.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**ECC Disable (ECC_DISABLE):** Setting this bit will internally disable all related ECC features in CPGC having the effect of generating all '1 in the ECC CPGC interface outputs, and of Binding to '0 all the ECC interface CPGC inputs. ECC masks and error comparisons will be disabled as well. If ECC is supported, but not directly passed to CPGC, then this bit when set will enable the ECC_REPLACE_BYTE_CONTROL and ECC_DATA_SOURCE_SEL functionality, to allow driving of ECC from another ByteLane, and replacing the incoming data with ECC for that ByteLane. When ECC is disabled with this bit, then the output of CPGC will be determined based on BE_TRAIN_ERR_EN and may output all 1's or the content of the DRAMDM and XDRAMDM registers as Byte-Enables.
12:10	0h RO	Reserved.
9	0h RW	**Read Address As Data (READ_ADDRESS_AS_DATA):** When Read_Address_as_Data is set to '1' any address fields that the CADB is overriding during a Select cycle should be used for comparing the incoming data. Otherwise, the functional path decoded address field should be used for comparing the incoming data. This override of the data will not respect any inversion, rotation or other data modification. It will only be active (override the normal output/reference) when Alternate_Data is active in either the Command_Instruction or the Offset_Command_Instruction as appropriate . The functional path decoded address field used for read comparison is repeated in chunk and should follow the Data Construction rules described below on what bytegroup relates to what decoded address: Chunk0 - Byte0 =Column(7:0). Chunk0 - Byte1 =Column(9:8) <- as many Column bits as supported. Chunk0 - Byte2 =Row(0:7). Chunk0 - Byte3 =Row(15:8). Chunk0 - Byte4 =Row(17:16)<- as many Row bits as supported. Chunk0 - Byte5 =Bank(3:0) [Note: Bank Group may be part of this field] <- as many Bank bits as supported. Chunk0 - Byte6 =Rank(1:0) <- as many Rank bits as supported (would be CS# if CADB output supported). Chunk0 - Byte7 =Reserved (set to 0).

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Write Address As Data (WRITE_ADDRESS_AS_DATA):** When Write_Address_as_Data is set to '1', any address fields that the CADB is overriding during a Select cycle should be used for generating the write data. Otherwise, the functional path decoded address field should be used for generating the write data. Data Construction rules follow the same as for READ_ADDRESS_AS_DATA. This format is subject to change based on memory technology supported and other reasons. What is to be guaranteed is that every Cacheline of data will be unique to each address.
7:6	0h RW	**Unisequencer 2 Mode (UNISEQ2_MODE):** Defines the operational mode for unified sequence 2 as follows: 00 - LMN Mode. 01 - Pattern Buffer Mode. 10 - LFSR Mode. 11 - Reserved for future use.
5	0h RO	Reserved.
4:3	0h RW	**Unisequencer 1 Mode (UNISEQ1_MODE):** Defines the operational mode for unified sequence 1 as follows: 00 - LMN Mode. 01 - Pattern Buffer Mode. 10 - LFSR Mode. 11 - Reserved for future use.
2	0h RO	Reserved.
1:0	0h RW	**Unisequencer 0 Mode (UNISEQ0_MODE):** Defines the operational mode for unified sequence 0 as follows: 00 - LMN Mode. 01 - Pattern Buffer Mode. 10 - LFSR Mode. 11 - Reserved for future use.

5.11.155 LFSR Configuration and Lane Rotate (CPGC_DPAT_XTRA_LFSR_CFG)—Offset 4988h

Unisequencer LFSR configuration and Lane Rotation.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Lane Rotate Rate (LANE_ROTATE_RATE):** Lane_Rotate_Rate only exists if the Lane_Rotation_Support capability exists. 2^(Lane_Rotate_Rate-1) indicates the periodic Loopcount rate when the EXTBUF_# registers are rotated up by one bit. Lane_Rotate_Rate=0 disables all rotation. Lane_Rotate_Rate=1 causes the EXTBUF_# registers to be rotated every one Loopcount. Lane_Rotate_Rate=2 causes the EXTBUF_# registers to be rotated every other Loopcount. Etc.. When the EXTBUF_# registers are rotated Bit 0 shifts to Bit 1 all the way up to the Max-1 Bit and the Max bit shifts to Bit0.
23	0h RW	**Unisequencer 2 LFSR Stagger Enable (UNISEQ2_LFSR_STAGGER):** 0=No Stagger, 1=Stagger. This bit must not be set unless Uniseq2_Mode is programmed to Select LFSR or the behavior is undefined.
22:21	0h RO	Reserved.
20:18	0h RW	**Unisequencer 2 LFSR Polynomial Select (UNISEQ2_LFSR_POLYNOMIAL_SIZE):** Possible Polynomial Sizes: 0x0=Use 8 bit LFSR (x8 + x6 + x5 + x4) 0x1=Use 15 bit LFSR (x15 + x14) 0x2=Use 31 bit LFSR (x31 + x28) 0x3=Use 23 bit LFSR (x23 + x18) 0x4=Use 7 bit LFSR (x7 + x6) 0x5=Use 16 bit LFSR (x16+x5+x4+x3) 0x6=Use 23 bit LFSR (x23+x21+x18+x15+x7+x2) 0x7=Use 32 bit LFSR (x32+x31+x30+x10)
17:16	0h RO	Reserved.
15	0h RW	**Unisequencer 1 LFSR Stagger Enable (UNISEQ1_LFSR_STAGGER):** 0=No Stagger, 1=Stagger. This bit must not be set unless Uniseq1_Mode is programmed to Select LFSR or the behavior is undefined.
14:13	0h RO	Reserved.
12:10	0h RW	**Unisequencer 1 LFSR Polynomial Select (UNISEQ1_LFSR_POLYNOMIAL_SIZE):** Possible Polynomial Sizes: 0x0=Use 8 bit LFSR (x8 + x6 + x5 + x4) 0x1=Use 15 bit LFSR (x15 + x14) 0x2=Use 31 bit LFSR (x31 + x28) 0x3=Use 23 bit LFSR (x23 + x18) 0x4=Use 7 bit LFSR (x7 + x6) 0x5=Use 16 bit LFSR (x16+x5+x4+x3) 0x6=Use 23 bit LFSR (x23+x21+x18+x15+x7+x2) 0x7=Use 32 bit LFSR (x32+x31+x30+x10)

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RO	Reserved.
7	0h RW	**Unisequencer 0 LFSR Stagger Enable (UNISEQ0_LFSR_STAGGER):** 0=No Stagger, 1=Stagger. This bit must not be set unless Uniseq0_Mode is programmed to Select LFSR or the behavior is undefined.
6:5	0h RO	Reserved.
4:2	0h RW	**Unisequencer 0 LFSR Polynomial Select (UNISEQ0_LFSR_POLYNOMIAL_SIZE):** Possible Polynomial Sizes: 0x0=Use 8 bit LFSR (x8 + x6 + x5 + x4) 0x1=Use 15 bit LFSR (x15 + x14) 0x2=Use 31 bit LFSR (x31 + x28) 0x3=Use 23 bit LFSR (x23 + x18) 0x4=Use 7 bit LFSR (x7 + x6) 0x5=Use 16 bit LFSR (x16+x5+x4+x3) 0x6=Use 23 bit LFSR (x23+x21+x18+x15+x7+x2) 0x7=Use 32 bit LFSR (x32+x31+x30+x10)
1:0	0h RO	Reserved.

5.11.156 Unisequencer Data Pattern Buffer (CPGC_DPAT_UNISEQ[0])—Offset 498Ch

Data Pattern Unified Sequencer 0 Seed Register.

Access Method

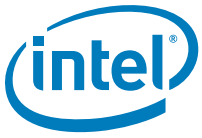
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AA55AA55h

Bit Range	Default & Access	Field Name (ID): Description
31:0	AA55AA55h RW	**Pattern Buffer (PATTERN_BUFFER):** If UniSeq#_Mode is set to Pattern Buffer mode, then this field represents the initial content of the rotating pattern buffer for the unified sequencer. If UniSeq#_Mode is set to LFSR mode, then this field represents the 32-bit LFSR seed for the unified sequencer. Note: This is a shared register, it has a meaning according to the UniSeq# mode. **For PRBS lengths less than or equal to 8, the seed must contain 16 bits of the initial PRBS sequence.**

5.11.157 Unisequencer Data Pattern Buffer (CPGC_DPAT_UNISEQ[1])—Offset 4990h

Data Pattern Unified Sequencer 0 Seed Register.



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AA55AA55h

Bit Range	Default & Access	Field Name (ID): Description
31:0	AA55AA55h RW	**Pattern Buffer (PATTERN_BUFFER):** If UniSeq#_Mode is set to Pattern Buffer mode, then this field represents the initial content of the rotating pattern buffer for the unified sequencer. If UniSeq#_Mode is set to LFSR mode, then this field represents the 32-bit LFSR seed for the unified sequencer. Note: This is a shared register, it has a meaning according to the UniSeq# mode. **For PRBS lengths less than or equal to 8, the seed must contain 16 bits of the initial PRBS sequence.**

5.11.158 Unisequencer Data Pattern Buffer (CPGC_DPAT_UNISEQ[2])—Offset 4994h

Data Pattern Unified Sequencer 0 Seed Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AA55AA55h

Bit Range	Default & Access	Field Name (ID): Description
31:0	AA55AA55h RW	**Pattern Buffer (PATTERN_BUFFER):** If UniSeq#_Mode is set to Pattern Buffer mode, then this field represents the initial content of the rotating pattern buffer for the unified sequencer. If UniSeq#_Mode is set to LFSR mode, then this field represents the 32-bit LFSR seed for the unified sequencer. Note: This is a shared register, it has a meaning according to the UniSeq# mode. **For PRBS lengths less than or equal to 8, the seed must contain 16 bits of the initial PRBS sequence.**

5.11.159 Unisequencer LMN Control (CPGC_DPAT_UNISEQ_LMN[0])—Offset 4998h

Data Pattern Unified Sequencer 0 LMN Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	1h RW	**N Count (N_CNT):** N_Count only exists if LMN_Support capability is set to 1. After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
23:16	1h RW	**M Count (M_CNT):** M_Count only exists if LMN_Support capability is set to 1. After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
15:8	1h RW	**L Count (L_CNT):** If LMN_Support capability is set to 0 then: A periodic square wave is generated that has the following behavior. 1) Drive L_Polarity for L_Count Bits. 2) Drive inverse of L_Polarity for L_Count Bits. 3) Go to step 1. Else if LMN_Support is set to 1 then: After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency is set to 1. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
7:4	0h RW	**L Count High-bits (L_COUNTER_HI):** Additional 4 bits to increase the size of L Count up to 12.
3	0h RO	Reserved.
2	0h RW	**L Counter Mode Enable (L_COUNT_EN):** Used in concatenation with FREQ_SWEEP_EN to enable 3 possible modes of LMN behavior.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Frequence Sweep Mode Enable (FREQ_SWEEP_EN):** Used in concatenation with L_COUNT_EN to enable 3 possible modes of LMN behavior: {L_COUNT_EN,FREQ_SWEEP_EN} {0,0} - Normal LMN. {0,1} - Sweep clock pattern from 2*M period down to 2*N_Count period and repeat. {1,0} - L-Counter - drive clock pattern of 2*L period. {1,1} - Currently same as L-Counter mode - reserved for future use. If Normal LMN mode, then the following pattern is continuously repeated: 1) Drive L_Count bits with the polarity set by L_Polarity. 2) Drive M_Count bits with the inverse of L_Polarity. 3) Drive N_Count bits with the value of L_Polarity. 4) Go to step 2. If any L_Count, M_Count, or N_Count=0 then the state will freeze at the polarity driven for that stage. If Sweep mode, then the following pattern is continuously repeated: 1) Drive L_Count bits with the polarity set by L_Polarity. 2) X_count=M_Count 3) Drive X_Count bits with the inverse of L_Polarity. 4) Drive X_Count bits with the value of L_Polarity. 5) Drive X_Count bits with the inverse of L_Polarity. 6) If X_Count==N_Count then go to step 9. 7) X_Count=X_Count-1 8) Go to step 10. 9) X_Count=M_Count 10) Drive X_Count bits with the value of L_Polarity. 11) Go to step 3. If LCount mode, then the following pattern is continuously repeated: 1) Drive L_Polarity for L_Count Bits. 2) Drive inverse of L_Polarity for L_Count Bits. 3) Go to step 1. If {0,1}, L_Count, M_Count, and N_Count must never be programmed to 0 and is considered undefined. If {1,0}, L_Count must never be programmed to 0 and is considered undefined. If {0,1}, M_Count and N_Count must be greater than or equal to 8 or behavior may be implementation specific. If {0,1}, N_Count must be programmed less than M_Count.
0	0h RW	**Initial Output (L_SEL):** The initial logic output of the sequencer is defined as follows: 0 - Output Logic '0' for L_CNT UIs. 1 - Output Logic '1' for L_CNT UIs.

5.11.160 Unisequencer LMN Control (CPGC_DPAT_UNISEQ_LMN[1])—Offset 499Ch

Data Pattern Unified Sequencer 0 LMN Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	1h RW	**N Count (N_CNT):** N_Count only exists if LMN_Support capability is set to 1. After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
23:16	1h RW	**M Count (M_CNT):** M_Count only exists if LMN_Support capability is set to 1. After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
15:8	1h RW	**L Count (L_CNT):** If LMN_Support capability is set to 0 then: A periodic square wave is generated that has the following behavior. 1) Drive L_Polarity for L_Count Bits. 2) Drive inverse of L_Polarity for L_Count Bits. 3) Go to step 1. Else if LMN_Support is set to 1 then: After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency is set to 1. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
7:4	0h RW	**L Count High-bits (L_COUNTER_HI):** Additional 4 bits to increase the size of L Count up to 12.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	Reserved.
2	0h RW	**L Counter Mode Enable (L_COUNT_EN):** Used in concatenation with FREQ_SWEEP_EN to enable 3 possible modes of LMN behavior.
1	0h RW	**Frequence Sweep Mode Enable (FREQ_SWEEP_EN):** Used in concatenation with L_COUNT_EN to enable 3 possible modes of LMN behavior: {L_COUNT_EN,FREQ_SWEEP_EN} {0,0} - Normal LMN. {0,1} - Sweep clock pattern from 2*M period down to 2*N_Count period and repeat. {1,0} - L-Counter - drive clock pattern of 2*L period. {1,1} - Currently same as L-Counter mode - reserved for future use. If Normal LMN mode, then the following pattern is continuously repeated: 1) Drive L_Count bits with the polarity set by L_Polarity. 2) Drive M_Count bits with the inverse of L_Polarity. 3) Drive N_Count bits with the value of L_Polarity. 4) Go to step 2. If any L_Count, M_Count, or N_Count=0 then the state will freeze at the polarity driven for that stage. If Sweep mode, then the following pattern is continuously repeated: 1) Drive L_Count bits with the polarity set by L_Polarity. 2) X_count=M_Count 3) Drive X_Count bits with the inverse of L_Polarity. 4) Drive X_Count bits with the value of L_Polarity. 5) Drive X_Count bits with the inverse of L_Polarity. 6) If X_Count==N_Count then go to step 9. 7) X_Count=X_Count-1 8) Go to step 10. 9) X_Count=M_Count 10) Drive X_Count bits with the value of L_Polarity. 11) Go to step 3. If LCount mode, then the following pattern is continuously repeated: 1) Drive L_Polarity for L_Count Bits. 2) Drive inverse of L_Polarity for L_Count Bits. 3) Go to step 1. If {0,1}, L_Count, M_Count, and N_Count must never be programmed to 0 and is considered undefined. If {1,0}, L_Count must never be programmed to 0 and is considered undefined. If {0,1}, M_Count and N_Count must be greater than or equal to 8 or behavior may be implementation specific. If {0,1}, N_Count must be programmed less than M_Count.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Initial Output (L_SEL):** The initial logic output of the sequencer is defined as follows: 0 - Output Logic '0' for L_CNT UIs. 1 - Output Logic '1' for L_CNT UIs.

5.11.161 Unisequencer LMN Control (CPGC_DPAT_UNISEQ_LMN[2])—Offset 49A0h

Data Pattern Unified Sequencer 0 LMN Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	1h RW	**N Count (N_CNT):** N_Count only exists if LMN_Support capability is set to 1. After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
23:16	1h RW	**M Count (M_CNT):** M_Count only exists if LMN_Support capability is set to 1. After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).

Bit Range	Default & Access	Field Name (ID): Description
15:8	1h RW	**L Count (L_CNT):** If LMN_Support capability is set to 0 then: A periodic square wave is generated that has the following behavior. 1) Drive L_Polarity for L_Count Bits. 2) Drive inverse of L_Polarity for L_Count Bits. 3) Go to step 1. Else if LMN_Support is set to 1 then: After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency is set to 1. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
7:4	0h RW	**L Count High-bits (L_COUNTER_HI):** Additional 4 bits to increase the size of L Count up to 12.
3	0h RO	Reserved.
2	0h RW	**L Counter Mode Enable (L_COUNT_EN):** Used in concatenation with FREQ_SWEEP_EN to enable 3 possible modes of LMN behavior.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Frequence Sweep Mode Enable (FREQ_SWEEP_EN):** Used in concatenation with L_COUNT_EN to enable 3 possible modes of LMN behavior: {L_COUNT_EN,FREQ_SWEEP_EN} {0,0} - Normal LMN. {0,1} - Sweep clock pattern from 2*M period down to 2*N_Count period and repeat. {1,0} - L-Counter - drive clock pattern of 2*L period. {1,1} - Currently same as L-Counter mode - reserved for future use. If Normal LMN mode, then the following pattern is continuously repeated: 1) Drive L_Count bits with the polarity set by L_Polarity. 2) Drive M_Count bits with the inverse of L_Polarity. 3) Drive N_Count bits with the value of L_Polarity. 4) Go to step 2. If any L_Count, M_Count, or N_Count=0 then the state will freeze at the polarity driven for that stage. If Sweep mode, then the following pattern is continuously repeated: 1) Drive L_Count bits with the polarity set by L_Polarity. 2) X_count=M_Count 3) Drive X_Count bits with the inverse of L_Polarity. 4) Drive X_Count bits with the value of L_Polarity. 5) Drive X_Count bits with the inverse of L_Polarity. 6) If X_Count==N_Count then go to step 9. 7) X_Count=X_Count-1 8) Go to step 10. 9) X_Count=M_Count 10) Drive X_Count bits with the value of L_Polarity. 11) Go to step 3. If LCount mode, then the following pattern is continuously repeated: 1) Drive L_Polarity for L_Count Bits. 2) Drive inverse of L_Polarity for L_Count Bits. 3) Go to step 1. If {0,1}, L_Count, M_Count, and N_Count must never be programmed to 0 and is considered undefined. If {1,0}, L_Count must never be programmed to 0 and is considered undefined. If {0,1}, M_Count and N_Count must be greater than or equal to 8 or behavior may be implementation specific. If {0,1}, N_Count must be programmed less than M_Count.
0	0h RW	**Initial Output (L_SEL):** The initial logic output of the sequencer is defined as follows: 0 - Output Logic '0' for L_CNT UIs. 1 - Output Logic '1' for L_CNT UIs.

5.11.162 Invert and DC Control (CPGC_DPAT_INVDCCTL)—Offset 49A4h

Data Pattern Inversion/DC Control Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AA0000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Mask Rotate Enable (MASK_ROTATE_EN):** If set, the inversion/DC mask will rotate to the left at a rate defined by the MASK_ROTATE_RATE field.
30	0h RW	**DC Mask Mode Enable (DC_OR_INV):** Selects between using the inversion/DC mask for inversion or DC as follows: 0 - Mask used for inversion. 1 - Mask used for driving a DC signal of polarity DC_POL.
29	0h RW	**DC Polarity (DC_POL):** Selects the polarity of the signal to be driven through the inversion/DC mask if DC_OR_INV is set to 1: 0 - Drive a logic low (zero). 1 - Drive a logic high (one).
28:25	0h RO	Reserved.
24:16	AAh RW	**Byte Group Mapping (BYTEGROUP_MAPPING):** Select between the two bytes of unique lanes being generated by the DPAT pattern generator, to be applied in each DQ byte group, as many byte groups as required by the number of DQ pins. MSB is always for the ECC byte group, used only if ECC is present.
15:12	0h RO	Reserved.
11:8	0h RW	**Mask Roate Rate (MASK_ROTATE_RATE):** If inversion mask rotation is enabled through MASK_ROTATE_EN, the mask will rotate to the left every time 2^MASK_ROTATE_RATE bursts (64Bytes) have been have been issued.
7:0	0h RW	**ECC ByteGroup Invert/DC Enable (ECC_INV_DC_MASK):** A value of for any of the bits means the corresponding ECC lane(s) will be inverted or a DC value driven on it. Note that this field is used to load bits [71:64] of the continuous shift register composed of this field along with DATA_INV_DC_MASK_HI and DATA_INV_DC_MASK_LO. Note: this field is only available if ECC is supported for the current implementation, otherwise it is reserved.

5.11.163 Data Invert/DC Enable Low (CPGC_DPAT_INV_DC_MASK_LO)—Offset 49A8h

Low Data Pattern Inversion/DC Mask Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data Invert/DC Enable Low (DATA_INV_DC_MASK_LO):** A value of '1' for any of the bits means the corresponding data lane(s) will be inverted or a DC value driven on it. Note that this field is used to load bits [31:0] of the continuous shift register composed of this field along with ECC_INV_DC_MASK and DATA_INV_DC_MASK_HI. DPAT generator only uses the appropriate bits based on the widest bus that this CPGC block is designed to support. This register is also used to provide the Initial value for the Alternate Data pattern generator.

5.11.164 Data Invert/DC Enable High (CPGC_DPAT_INV_DC_MASK_HI)—Offset 49ACh

High Data Pattern Inversion/DC Mask Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data Invert/DC Enable High (DATA_INV_DC_MASK_HI):** A value of '1' for any of the bits means the corresponding data lane(s) will be inverted or a DC value driven on it. Note that this field is used to load bits [63:32] of the continuous shift register composed of this field along with ECC_INV_DC_MASK and DATA_INV_DC_MASK_LO.

5.11.165 Byte Enable Mask Lower (CPGC_DPAT_DRAMDM)—Offset 49B0h

Data Pattern DRAM Data Mask Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**Byte Enable Mask Lower (DATA_MASK_LO):** A byte enable field with each bit corresponding to a data byte sent during a burst such that: 0 - Mask the Corresponding Byte. 1 - No Mask to the Corresponding Byte. The byte-to-bit mapping is given by Byte[n] -> bit[n]. This register is for the first half cacheline of data. It is only used when ECC is not present or is disabled.

5.11.166 Byte Enable Mask Upper (CPGC_DPAT_XDRAMDM)—Offset 49B4h

Extended Data Pattern DRAM Data Mask Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**Byte Enable Mask Upper (DATA_MASK_HI):** A byte enable field with each bit corresponding to a data byte sent during a burst such that: 0 - Mask the Corresponding Byte. 1 - No Mask to the Corresponding Byte. The byte-to-bit mapping is given by Byte[n+32] -> bit[n]. This register is for the Second half cacheline of data. It is only used when ECC is not present or is disabled.

5.11.167 Unisequencer Status - Write (CPGC_DPAT_UNISEQ_WRSTAT[0])—Offset 49B8h

Write Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Status (UNISEQ_WRSTAT):** The current contents of the Pattern/LFSR buffer in write generation domain.

5.11.168 Unisequencer Status - Write (CPGC_DPAT_UNISEQ_WRSTAT[1])—Offset 49BCh

Write Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Status (UNISEQ_WRSTAT):** The current contents of the Pattern/LFSR buffer in write generation domain.

5.11.169 Unisequencer Status - Write (CPGC_DPAT_UNISEQ_WRSTAT[2])—Offset 49C0h

Write Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Status (UNISEQ_WRSTAT):** The current contents of the Pattern/LFSR buffer in write generation domain.

5.11.170 Unisequencer Status - Read (CPGC_DPAT_UNISEQ_RDSTAT[0])—Offset 49C4h

Read Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Status (UNISEQ_RDSTAT):** Reflects the current and final status of the pattern buffer in the read domain. If PATBUF mode, then Pattern_Buffer is used as a fixed buffer that is output in serial fashion. After all the bits in the Pattern_Buffer have been transmitted the pattern will simply repeat itself continuously while a Loopback Test is in progress. If LFSR mode, then Pattern_Buffer is used as a seed to a fixed LFSR that is output in serial fashion. Over time the LFSR pattern will repeat itself continuously while a Loopback Test is in progress. In LFSR Mode the contents of Pattern_Buffer will interact with the LFSR in the following ways: If LFSR_Save_Restore is set then CPGC_REG_DPAT_UNISEQ_WRSAVE.Pattern_Buffer will interact with CPGC_UNISEQ#_RDSTAT in the following ways: 1) CPGC_UNISEQ#_RDSTAT will be periodically saved into CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Save_LFSR_Seed_Rate (see Save_LFSR_Seed_Rate for more details). 2) CPGC_UNISEQ#_RDSTAT will be periodically reloaded with CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Reload_LFSR_Seed_Rate (see Reload_LFSR_Seed_Rate for more details).

5.11.171 Unisequencer Status - Read (CPGC_DPAT_UNISEQ_RDSTAT[1])—Offset 49C8h

Read Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Status (UNISEQ_RDSTAT):** Reflects the current and final status of the pattern buffer in the read domain. If PATBUF mode, then Pattern_Buffer is used as a fixed buffer that is output in serial fashion. After all the bits in the Pattern_Buffer have been transmitted the pattern will simply repeat itself continuously while a Loopback Test is in progress. If LFSR mode, then Pattern_Buffer is used as a seed to a fixed LFSR that is output in serial fashion. Over time the LFSR pattern will repeat itself continuously while a Loopback Test is in progress. In LFSR Mode the contents of Pattern_Buffer will interact with the LFSR in the following ways: If LFSR_Save_Restore is set then CPGC_REG_DPAT_UNISEQ_WRSAVE.Pattern_Buffer will interact with CPGC_UNISEQ#_RDSTAT in the following ways: 1) CPGC_UNISEQ#_RDSTAT will be periodically saved into CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Save_LFSR_Seed_Rate (see Save_LFSR_Seed_Rate for more details). 2) CPGC_UNISEQ#_RDSTAT will be periodically reloaded with CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Reload_LFSR_Seed_Rate (see Reload_LFSR_Seed_Rate for more details).

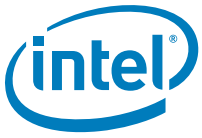
5.11.172 Unisequencer Status - Read (CPGC_DPAT_UNISEQ_RDSTAT[2])—Offset 49CCh

Read Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Status (UNISEQ_RDSTAT):** Reflects the current and final status of the pattern buffer in the read domain. If PATBUF mode, then Pattern_Buffer is used as a fixed buffer that is output in serial fashion. After all the bits in the Pattern_Buffer have been transmitted the pattern will simply repeat itself continuously while a Loopback Test is in progress. If LFSR mode, then Pattern_Buffer is used as a seed to a fixed LFSR that is output in serial fashion. Over time the LFSR pattern will repeat itself continuously while a Loopback Test is in progress. In LFSR Mode the contents of Pattern_Buffer will interact with the LFSR in the following ways: If LFSR_Save_Restore is set then CPGC_REG_DPAT_UNISEQ_WRSAVE.Pattern_Buffer will interact with CPGC_UNISEQ#_RDSTAT in the following ways: 1) CPGC_UNISEQ#_RDSTAT will be periodically saved into CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Save_LFSR_Seed_Rate (see Save_LFSR_Seed_Rate for more details). 2) CPGC_UNISEQ#_RDSTAT will be periodically reloaded with CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Reload_LFSR_Seed_Rate (see Reload_LFSR_Seed_Rate for more details).

5.11.173 LMN Status - Write (CPGC_DPAT_LMN_WRSTAT[0])—Offset 49D0h

Write LMN Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Status (LMN_WRSTAT):** The current contents of the LMN buffer in write comparison domain.

5.11.174 LMN Status - Write (CPGC_DPAT_LMN_WRSTAT[1])—Offset 49D4h

Write LMN Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Status (LMN_WRSTAT):** The current contents of the LMN buffer in write comparison domain.

5.11.175 LMN Status - Write (CPGC_DPAT_LMN_WRSTAT[2])—Offset 49D8h

Write LMN Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Status (LMN_WRSTAT):** The current contents of the LMN buffer in write comparison domain.

5.11.176 LMN Status - Read (CPGC_DPAT_LMN_RDSTAT[0])—Offset 49DCh

Read LMN Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Status (LMN_RDSTAT):** The current contents of the LMN buffer in read comparison domain.

5.11.177 LMN Status - Read (CPGC_DPAT_LMN_RDSTAT[1])—Offset 49E0h

Read LMN Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Status (LMN_RDSTAT):** The current contents of the LMN buffer in read comparison domain.

5.11.178 LMN Status - Read (CPGC_DPAT_LMN_RDSTAT[2])—Offset 49E4h

Read LMN Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Status (LMN_RDSTAT):** The current contents of the LMN buffer in read comparison domain.

5.11.179 Unisequencer Save Status - Write (CPGC_DPAT_UNISEQ_WRSAVE[0])—Offset 49E8h

Write PRBS Save Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Save Status (PATTERN_BUFFER):** The current contents of the Save register before the test stops in the write domain.

5.11.180 Unisequencer Save Status - Write (CPGC_DPAT_UNISEQ_WRSAVE[1])—Offset 49ECh

Write PRBS Save Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Save Status (PATTERN_BUFFER):** The current contents of the Save register before the test stops in the write domain.

5.11.181 Unisequencer Save Status - Write (CPGC_DPAT_UNISEQ_WRSAVE[2])—Offset 49F0h

Write PRBS Save Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Save Status (PATTERN_BUFFER):** The current contents of the Save register before the test stops in the write domain.

5.11.182 Unisequencer Save Status - Read (CPGC_DPAT_UNISEQ_RDSAVE[0])—Offset 49F4h

Read PRBS Save Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Save Status (PATTERN_BUFFER):** CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer will reflect either the initial or last saved value of CPGC_UNISEQ#_RDSTAT. If PATBUF mode, then Pattern_Buffer is used as a fixed buffer that is output in serial fashion. After all the bits in the Pattern_Buffer have been transmitted the pattern will simply repeat itself continuously while a Loopback Test is in progress. If LFSR mode, then Pattern_Buffer is used as a seed to a fixed LFSR that is output in serial fashion. Over time the LFSR pattern will repeat itself continuously while a Loopback Test is in progress. In LFSR Mode the contents of Pattern_Buffer will interact with the LFSR in the following ways: If LFSR_Save_Restore is set then CPGC_REG_DPAT_UNISEQ_WRSAVE.Pattern_Buffer will interact with CPGC_UNISEQ#_RDSTAT in the following ways: 1) CPGC_UNISEQ#_RDSTAT will be periodically saved into CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Save_LFSR_Seed_Rate (see Save_LFSR_Seed_Rate for more details). 2) CPGC_UNISEQ#_RDSTAT will be periodically reloaded with CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Reload_LFSR_Seed_Rate (see Reload_LFSR_Seed_Rate for more details).

5.11.183 Unisequencer Save Status - Read (CPGC_DPAT_UNISEQ_RDSAVE[1])—Offset 49F8h

Read PRBS Save Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Save Status (PATTERN_BUFFER):** CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer will reflect either the initial or last saved value of CPGC_UNISEQ#_RDSTAT. If PATBUF mode, then Pattern_Buffer is used as a fixed buffer that is output in serial fashion. After all the bits in the Pattern_Buffer have been transmitted the pattern will simply repeat itself continuously while a Loopback Test is in progress. If LFSR mode, then Pattern_Buffer is used as a seed to a fixed LFSR that is output in serial fashion. Over time the LFSR pattern will repeat itself continuously while a Loopback Test is in progress. In LFSR Mode the contents of Pattern_Buffer will interact with the LFSR in the following ways: If LFSR_Save_Restore is set then CPGC_REG_DPAT_UNISEQ_WRSAVE.Pattern_Buffer will interact with CPGC_UNISEQ#_RDSTAT in the following ways: 1) CPGC_UNISEQ#_RDSTAT will be periodically saved into CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Save_LFSR_Seed_Rate (see Save_LFSR_Seed_Rate for more details). 2) CPGC_UNISEQ#_RDSTAT will be periodically reloaded with CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Reload_LFSR_Seed_Rate (see Reload_LFSR_Seed_Rate for more details).

5.11.184 Unisequencer Save Status - Read (CPGC_DPAT_UNISEQ_RDSAVE[2])—Offset 49FCh

Read PRBS Save Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Save Status (PATTERN_BUFFER):** CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer will reflect either the initial or last saved value of CPGC_UNISEQ#_RDSTAT. If PATBUF mode, then Pattern_Buffer is used as a fixed buffer that is output in serial fashion. After all the bits in the Pattern_Buffer have been transmitted the pattern will simply repeat itself continuously while a Loopback Test is in progress. If LFSR mode, then Pattern_Buffer is used as a seed to a fixed LFSR that is output in serial fashion. Over time the LFSR pattern will repeat itself continuously while a Loopback Test is in progress. In LFSR Mode the contents of Pattern_Buffer will interact with the LFSR in the following ways: If LFSR_Save_Restore is set then CPGC_REG_DPAT_UNISEQ_WRSAVE.Pattern_Buffer will interact with CPGC_UNISEQ#_RDSTAT in the following ways: 1) CPGC_UNISEQ#_RDSTAT will be periodically saved into CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Save_LFSR_Seed_Rate (see Save_LFSR_Seed_Rate for more details). 2) CPGC_UNISEQ#_RDSTAT will be periodically reloaded with CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Reload_LFSR_Seed_Rate (see Reload_LFSR_Seed_Rate for more details).

5.11.185 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[0])—Offset 4A00h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.

Bit Range	Default & Access	Field Name (ID): Description
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.186 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[1])—Offset 4A04h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.187 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[2])—Offset 4A08h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.188 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[3])—Offset 4A0Ch

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.

Bit Range	Default & Access	Field Name (ID): Description
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.189 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[4])—Offset 4A10h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.190 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[5])—Offset 4A14h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.191 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[6])—Offset 4A18h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.

Bit Range	Default & Access	Field Name (ID): Description
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.192 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[7])—Offset 4A1Ch

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.193 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[8])—Offset 4A20h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.194 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[9])—Offset 4A24h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.

Bit Range	Default & Access	Field Name (ID): Description
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.195 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[10])—Offset 4A28h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

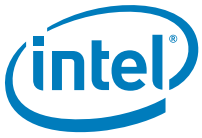
Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.196 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[11])—Offset 4A2Ch

DPAT Pattern Select Buffer.

Access Method



Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.197 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[12])—Offset 4A30h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.

Bit Range	Default & Access	Field Name (ID): Description
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.198 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[13])—Offset 4A34h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.199 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[14])—Offset 4A38h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.200 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[15])—Offset 4A3Ch

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.

Bit Range	Default & Access	Field Name (ID): Description
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.11.201 Error Checker Control (CPGC_ERR_CTL)—Offset 4A40h

Control for Error Checker.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/P	**Cache Line Error Check Enable (ERRCHK_MASK_CACHELINE):** Defines a periodic burst mask that repeats every 64Bytes of data as follows: Bit 0 - Burst 0 Bit 1 - Burst 1 ... Bit 7 - Burst 7 Only bursts with a corresponding bit value of '1' will be checked for errors. A burst is defined as a burst length of 64 bytes of data. In Loopback each bit of this register controls the check of each ByteTime (8-bits) on the bus.
23:16	0h RW/P	**Chunk Error Check Enable (ERRCHK_MASK_CHUNK):** Defines which chunk within the burst of data (i.e. bit within a burst of 8-bits for each lane) to check for errors. Only chunks with a corresponding bit value of '0' will be checked for errors. This field is only used for full width (64bit) DQ busses. Otherwise the upper 32 bits of the Lane Mask is used as the Chunk Enable. This field is also used for Loopback mode for all DQ sizes.
15:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW/P	**Stop On Error Control (STOP_ON_ERROR_CTL):** Defines test stop conditions based on error checking as follows: 00 - Never stop: Prevents any error from stopping the test. 01 - Stop On Nth Error: Stop once STOP_ERR_CNTR has accumulated at least (STOP_ON_N + 1) errors. 10 - Stop On All Byte Groups Error: Stop if every byte group indicates that at least one of its lanes accumulated at least one error. That is, if all bits BYTEGRP_ERR_STAT, (and ECC_GRP_ERR_STAT if supported), are all set. 11 - Stop On All Lanes Error: Stop if every lane within every byte group has accumulated at least one error. That is, if all bits in LANE_ERR_STAT_LO, LANE_ERR_STAT_HI, (and LANE_ERR_STATECC if supported) are all set.
11:9	0h RO	Reserved.
8	0h RW/P	**BE Training Enable (BE_TRAIN_ERR_EN):** Enable BE Training Error Detection Feature. Note this bit overrides the BE_TRAIN_ERR_EN bit in CPGC2_ALGORITHM_INSTRUCTION_CTRL.
7:6	0h RO	Reserved.
5:0	0h RW/P	**Stop On Nth Error Count (STOP_ON_N):** If STOP_ON_ERROR is set to Stop on Nth Error Mode, the test will stop after (STOP_ON_N + 1) or more errors have been accumulated in the ERR_CNTR.

5.11.202 Lane Error Mask Lower Bytes (CPGC_ERR_LNEN_LO)—Offset 4A44h

Error Lane Mask for Byte Groups 0-3.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/P	**Lower Data Lane Error Mask (DATA_ERRCHK_MASK_LO):** A mask used to disable error checking on data lanes [31:0]. Lanes selected through this mask will not be checked for errors. The lane-to-bit mapping for this mask is given by the following formula: Lane[n] -> bit[n]. Functionality will change with special mapping when buswidth is < 64 (or 72) such that ChunkMask will move to this field starting at bit [...:32] extending the necessary number of bits for a full cache line of data. The mask in ERR_CTL will be unused for these busses/modes.

5.11.203 Lane Error Mask Upper Bytes or Extended Chunk Enable (CPGC_ERR_LNEN_HI)—Offset 4A48h

Error Lane Mask for Byte Groups 4-7 or Extended Chunk Check Enable.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/P	**Upper Data Lane Error Mask (DATA_ERRCHK_MASK_HI):** A mask used to disable error checking on data lanes [63:32]. Lanes selected through this mask will not be checked for errors. The lane-to-bit mapping for this mask is given by the following formula: Lane[n+32] -> bit[n]. Functionality will change with special mapping when buswidth is < 64 (or 72) such that ChunkMask will move to this field starting at bit [...:32] extending the necessary number of bits for a full cache line of data. The mask in ERR_CTL will be unused for these busses/modes.

5.11.204 Lane Error Mask ECC (CPGC_ERR_XLNEN)—Offset 4A4Ch

ECC Lane Error Mask.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFh

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	FFh RW/P	**ECC Lane Error Mask (ECC_ERRCHK_MASK):** A mask used to disable error checking on ECC lanes. Lanes selected through the mask will not be checked for errors. The lane-to-bit mapping is 1-to-1 and hence bit 1 corresponds to ECC lane 0, bit 1 corresponds to ECC lane 1, and so on. Note: This field is available only if ECC is supported. The default state is to disable ECC checking.

5.11.205 Lane Error Status Lower Bytes (CPGC_ERR_STAT03)—Offset 4A50h

Error Status DQ Lanes 31-0 Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Lower Data Lane Error Status (LANE_ERR_STAT_LO):** Indicates if a mismatch was detected between the WR and the RD data on one of the lanes belonging to byte groups 0 - 3. Hence lanes [32:0] map to bits [32:0] respectively. The error status information is encoded as follows: 0: No mismatches detected on corresponding lane. 1: At least one mismatch detected on corresponding lane. Cleared on Local Clear Errors.

5.11.206 Lane Error Status Upper Bytes or Extended Chunk Error Status (CPGC_ERR_STAT47)—Offset 4A54h

Error Status DQ Lanes 63-32 Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Upper Data Lane Error Status (LANE_ERR_STAT_HI):** Indicates if a mismatch was detected between the WR and the RD data on one of the lanes belonging to byte groups 4 - 7. Hence lanes [63:32] map to bits [32:0] respectively. If there are less than 32 data lanes, then this register is used to indicate the Extended Chunk Error Status, and the Chunk Error Status in ECC_CHNK_RANK_STAT is not used. Chunks 0 through 15 (32-bit bus) or 0 through 31 (16-bit bus). The error status information is encoded as follows: 0: No mismatches detected on corresponding lane (chunk). 1: At least one mismatch detected on corresponding lane (chunk). Cleared on Local Clear Errors.

5.11.207 ECC Lane Error Status (CPGC_ERR_ECC_CHNK_RANK_STAT)—Offset 4A58h

Error Status for ECC, Chunks and Ranks.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:16	0h RO/V/P	**Rank Error Status (RANK_ERR_STAT):** A status field where each bit corresponds to a specific rank. If set, the corresponding rank has accumulated at least one error. Cleared on Local Clear Errors.
15:8	0h RO/V/P	**Chunk Error Status (CHUNK_ERR_STAT):** A flag field where each bit corresponds to a specific chunk (i.e. bit within a burst of 8-bits). If set, the corresponding chunk (UI) has accumulated at least one error. Cleared on Local Clear Errors.
7:0	0h RO/V/P	**ECC Lane Error Status (ECC_LANE_ERR_STAT):** A fag field which indicates if a mismatch was detected between the WR and the RD data on one of the lanes belonging to the ECC byte group. The error status information is encoded as follows: 0: No mismatches detected on corresponding lane. 1: At least one mismatch detected on corresponding lane. Note: this field is only available if ECC is supported for the current implementation, otherwise it is reserved. If BE Training Enable is set then this field indicates that the particular BE lane had a fault during the write pass. Cleared on Local Clear Errors.

5.11.208 ByteGroup Error Status (CPGC_ERR_BYTE_NTH_PAR_STAT)—Offset 4A5Ch

Error Status for ByteGroup and Error Stop.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	0h RO/V/P	**Nth Error Count Status (Nth_ERROR):** Nth_Error indicates the current Nth Error that has occurred. Nth_Error will roll over upon saturating to its maximum values. An Nth error is defined as 1 or more lane miscompares within a single comparison cycle (i.e. Chunk).
23	0h RO	Reserved.
22:20	0h RO/V/P	**Read Chunk Number Status (RD_CHUNK_NUM_STAT):** RD_Chunk_Num_Status corresponds to the chunk number being read out of the WDB (EXTBUF)for a RdCAS operation while logging an error during Loopback.Pattern. RD_Chunk_Num_Status is needed in conjunction with the lower 3 column address bits of the cacheline experiencing the error in order to deterministically rewind the LFSR/PB/LMN counter after the test is stopped due to an error condition. This is due to the pipelined nature of the data path since a cacheline can be read out of the WDB (EXTBUF) at the same time an error is being detected against an earlier read. Using RD_Chunk_Num_Status and the lower 3 column address bits of the cacheline experiencing the error allows the user to determine the skid between the LFSR/PB/LMN counter and the error detection. RD_Chunk_Num_Status can be cleared by one of two ways. 1. Local_Clear_Errors or (Global_Control and Global_Clear_Errors) to 1. 2. Writing RD_Chunk_Num_Status=0x0. One may also choose to clear individual bits in RD_Chunk_Num_Status. Setting bits in RD_Chunk_Num_Status is undefined and should be avoided. Writing a 0 to bits in RD_Chunk_Num_Status can be cleared independently of Data_Error_Status, ECC_Error_Status, Rank_Error_Status, Chunk_Error_Status, and Byte_Group_Error_Status.
19:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C/V/P	**ECC ByteGroup Error Status (ECCGRP_ERR_STAT):** A set bit implies that the ECC bytegroup has at least one lane that accumulated at least one error. Can also be cleared on Local Clear Errors (or Global_Control and a Global_Clear_Errors) .
7:0	0h RW/1C/V/P	**Data ByteGroup Error Status (BYTEGRP_ERR_STAT):** A flag field with each bit corresponding to a specific byte group. Bit 0 corresponds to byte group 0, bit 1 corresponds to byte group 1, bit 2 corresponds to byte group 2, and so on. A set bit implies that the corresponding byte group has at least one lane that accumulated at least one error. When BE Training Enable is set, then this field will indicate that a data error has occured that was not due to the corresponding BE signal. Can also be cleared on Local Clear Errors (or Global_Control and a Global_Clear_Errors) .

5.11.209 Error Counter Control (CPGC_ERR_CNTRCTL[0])—Offset 4A60h

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.11.210 Error Counter Control (CPGC_ERR_CNTRCTL[1])—Offset 4A64h

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.11.211 Error Counter Control (CPGC_ERR_CNTRCTL[2])—Offset 4A68h

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.11.212 Error Counter Control (CPGC_ERR_CNTRCTL[3])—Offset 4A6Ch

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.11.213 Error Counter Control (CPGC_ERR_CNTRCTL[4])—Offset 4A70h

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.11.214 Error Counter Control (CPGC_ERR_CNTRCTL[5])—Offset 4A74h

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.11.215 Error Counter Control (CPGC_ERR_CNTRCTL[6])—Offset 4A78h

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.11.216 Error Counter Control (CPGC_ERR_CNTRCTL[7])—Offset 4A7Ch

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.11.217 Error Counter Control (CPGC_ERR_CNTRCTL[8])—Offset 4A80h

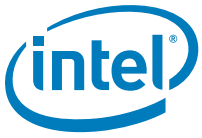
Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.



Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.11.218 Error Counter (CPGC_ERR_CNTR[0])—Offset 4A84h

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.11.219 Error Counter (CPGC_ERR_CNTR[1])—Offset 4A88h

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.11.220 Error Counter (CPGC_ERR_CNTR[2])—Offset 4A8Ch

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.11.221 Error Counter (CPGC_ERR_CNTR[3])—Offset 4A90h

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.11.222 Error Counter (CPGC_ERR_CNTR[4])—Offset 4A94h

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.11.223 Error Counter (CPGC_ERR_CNTR[5])—Offset 4A98h

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.11.224 Error Counter (CPGC_ERR_CNTR[6])—Offset 4A9Ch

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.11.225 Error Counter (CPGC_ERR_CNTR[7])—Offset 4AA0h

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.11.226 Error Counter (CPGC_ERR_CNTR[8])—Offset 4AA4h

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.11.227 Error Counter Overflow (CPGC_ERR_CNTR_OV)—Offset 4AA8h

Indicates the current error counter overflow value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8:0	0h RW/1C/V/P	**Error Counter Overflow Status (ERROR_COUNTER_OVERFLOW):** Contains the overflow flags for all Error Counters. Bit 0 corresponds to ERROR_COUNTER_0. Bit 1 corresponds to ERROR_COUNTER_1. .. Bit 8 corresponds to ERROR_COUNTER_8. Error Counter Overflow Status can be cleared by one of two ways: 1. Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) to 1. 2. Writing the correspoing Error Counter Overflow Status bit to 1. Writing a 0 to bits in Counter_Overflow_Status can be cleared independently of Data_Error_Status, Byte_Group_Error_Status, Chunk_Error_Status, and ECC_Error_Status.

5.11.228 Error Log Control and Status (CPGC_ERRLOG_CTL_STAT)—Offset 4AACh

Error Logging Control and Status - All Error Log information must be read out before doing a Local Clear Errors.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW/1S	**Error Log Clear Read Buffer Pointer (CLR_DUN_RDBUF_PTR):** Initializes the Error Log Current Read Pointer. Do this prior to the start of a test.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1S	**Error Log Increment Chunk Count (INC_CHUNK_COUNT):** Advance to next portion of data which is then available in the Error Log Data Register.
14	0h RW/1S	**Error Log Auto Seek to Error (ERRLOG_AUTO):** Asserting this bit will have the effect of CPGC automatically generating the needed Read transactions such as the current Read Pointer targets the last failing cachline. Instead of manually browsing, user can set this bit and logic will make sure that CURR_RD_PTR==ERROR_RD_PTR. This bit will always return '0' if read by software.
13	0h RW/1S	**Error Log Increment Current Read Pointer (ERRLOG_MOVE):** Asserting this bit will have the effect of incrementing by one the Current Read Pointer at the actual Read Data Buffer. User can manually browse through the Read Data Buffer and dump its contents. This bit will always return '0' if read by software.
12	0h RW/P	**Error Log Auto Chunk Increment (ERRLOG_AUTO_CHNK_INC):** Signal that will allow auto-increment feature for each 32bit data chunk read from the Error Log Data register. Note: If this bit is set, when doing the last 32bit data access via reading the Error Log Data register, the Error Log Current Read Pointer will auto increment as well.
11:9	0h RO	Reserved.
8:5	0h RO/V/P	**Error Log Error Read Pointer (ERROR_RD_PTR):** Provides the Read Pointer location that caused the error that triggered STOP_ON_ERROR. This will be used for knowing exactly which entry in the Read Data Buffer contains the faulty cacheline data.
4	0h RO	Reserved.
3:0	0h RO/V/P	**Error Log Current Read Pointer (CURR_RD_PTR):** Provides the current Read Pointer location indexed at the Read Data Buffer. This will be used for knowing how many Reads the user needs to issue to return the pointer to the actual failing entry.

5.11.229 Error Log Data Access (CPGC_ERRLOG_DATA)—Offset 4AB0h

Error Logging Data Access Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Error Log Data (ERRLOG_DATA):** 32 bits of data corresponding to one of eight (or four for ANN) 32 bit PMI chunks available per Read Pointer location. If ERRLOG_AUTO_CHNK_INC is set, then each read to this register will read out a successive 32 bit PMI chunk of data.

5.11.230 Loopback Error Status (CPGC_ERR_TEST_ERR_STAT)—Offset 4AB4h

Indicates when a test is complete and if any errors occurred for Loopback mode.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RO/V	**Loopback Test in Progress (TEST_IN_PROGRESS):** Used to indicate a loopback test is in progress.
0	0h RO/V/P	**Loopback Local Error Status (ERROR_STATUS):** Bit set during the loopback test. Cleared when Local_Clear_Error in Loopback Sequencer Control is set.

5.11.231 Rank Logical To Physical Map (CPGC_SEQ_RANK_L2P_MAPPING)—Offset 4AB8h

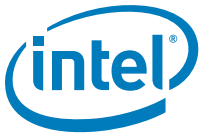
Rank Logical to Physical Mapping Lookup Table Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 76543210h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:28	7h RW	**Rank 7 Mapping (L2P_RANK7_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).



Bit Range	Default & Access	Field Name (ID): Description
27	0h RO	Reserved.
26:24	6h RW	**Rank 6 Mapping (L2P_RANK6_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).
23	0h RO	Reserved.
22:20	5h RW	**Rank 5 Mapping (L2P_RANK5_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).
19	0h RO	Reserved.
18:16	4h RW	**Rank 4 Mapping (L2P_RANK4_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).
15	0h RO	Reserved.
14:12	3h RW	**Rank 3 Mapping (L2P_RANK3_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).
11	0h RO	Reserved.
10:8	2h RW	**Rank 2 Mapping (L2P_RANK2_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).
7	0h RO	Reserved.
6:4	1h RW	**Rank 1 Mapping (L2P_RANK1_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).
3	0h RO	Reserved.
2:0	0h RW	**Rank 0 Mapping (L2P_RANK0_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).

5.11.232 Bank Logical to Physical Map Low (CPGC_SEQ_BANK_L2P_MAPPING_A)—Offset 4ABCh

Bank Logical to Physical Mapping Lookup Table Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 76543210h

Bit Range	Default & Access	Field Name (ID): Description
31:28	7h RW	**Bank 7 Mapping (L2P_BANK7_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
27:24	6h RW	**Bank 6 Mapping (L2P_BANK6_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
23:20	5h RW	**Bank 5 Mapping (L2P_BANK5_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
19:16	4h RW	**Bank 4 Mapping (L2P_BANK4_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
15:12	3h RW	**Bank 3 Mapping (L2P_BANK3_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
11:8	2h RW	**Bank 2 Mapping (L2P_BANK2_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
7:4	1h RW	**Bank 1 Mapping (L2P_BANK1_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
3:0	0h RW	**Bank 0 Mapping (L2P_BANK0_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).

5.11.233 Bank Logical to Physical Map High (CPGC_SEQ_BANK_L2P_MAPPING_B)—Offset 4AC0h

Bank Logical to Physical Mapping Lookup Table Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FEDCBA98h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RW	**Bank 15 Mapping (L2P_BANK15_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
27:24	Eh RW	**Bank 14 Mapping (L2P_BANK14_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
23:20	Dh RW	**Bank 13 Mapping (L2P_BANK13_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
19:16	Ch RW	**Bank 12 Mapping (L2P_BANK12_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
15:12	Bh RW	**Bank 11 Mapping (L2P_BANK11_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
11:8	Ah RW	**Bank 10 Mapping (L2P_BANK10_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
7:4	9h RW	**Bank 9 Mapping (L2P_BANK9_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
3:0	8h RW	**Bank 8 Mapping (L2P_BANK8_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).

5.11.234 Rank Address Swizzle (CPGC_SEQ_RANK_ADDR_SWIZZLE)—Offset 4AC4h

This register is used to swizzle the Logical to Physical Rank bits.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FEDCh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:12	Fh RW	**Rank 3 Swizzle (L2P_RANK3_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other. Only Rank address bits available to the memory controller are valid, others should be set to 0xF.
11:8	Eh RW	**Rank 2 Swizzle (L2P_RANK2_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.
7:4	Dh RW	**Rank 1 Swizzle (L2P_RANK1_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.
3:0	Ch RW	**Rank 0 Swizzle (L2P_RANK0_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.

5.11.235 Bank Address Swizzle (CPGC_SEQ_BANK_ADDR_SWIZZLE)—Offset 4AC8h

This register is used to swizzle the Logical Bank and Row address bits to Physical Bank bits.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEB38h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:15	1Bh RW	**Bank 3 Swizzle (L2P_BANK3_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Bank address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value. Only Bank address bits available to the memory controller are valid, others should be set to 0x1F.
14:10	1Ah RW	**Bank 2 Swizzle (L2P_BANK2_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Bank address. The bits are essentially swizzled with each other.
9:5	19h RW	**Bank 1 Swizzle (L2P_BANK1_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Bank address. The bits are essentially swizzled with each other.

Bit Range	Default & Access	Field Name (ID): Description
4:0	18h RW	**Bank 0 Swizzle (L2P_BANK0_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Bank address. The bits are essentially swizzled with each other.

5.11.236 Row Address Swizzle Low (CPGC_SEQ_ROW_ADDR_SWIZZLE_A)—Offset 4ACCh

This register is used to swizzle the Logical to Physical Row bits.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: A418820h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:25	5h RW	**Row 5 Swizzle (L2P_ROW5_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
24:20	4h RW	**Row 4 Swizzle (L2P_ROW4_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
19:15	3h RW	**Row 3 Swizzle (L2P_ROW3_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
14:10	2h RW	**Row 2 Swizzle (L2P_ROW2_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
9:5	1h RW	**Row 1 Swizzle (L2P_ROW1_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.

Bit Range	Default & Access	Field Name (ID): Description
4:0	0h RW	**Row 0 Swizzle (L2P_ROW0_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.

5.11.237 Row Address Swizzle Mid (CPGC_SEQ_ROW_ADDR_SWIZZLE_B)—Offset 4AD0h

This register is used to swizzle the Logical to Physical Row bits.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 16A4A0E6h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:25	Bh RW	**Row 11 Swizzle (L2P_ROW11_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
24:20	Ah RW	**Row 10 Swizzle (L2P_ROW10_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
19:15	9h RW	**Row 9 Swizzle (L2P_ROW9_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
14:10	8h RW	**Row 8 Swizzle (L2P_ROW8_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
9:5	7h RW	**Row 7 Swizzle (L2P_ROW7_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.

Bit Range	Default & Access	Field Name (ID): Description
4:0	6h RW	**Row 6 Swizzle (L2P_ROW6_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.

5.11.238 Row Address Swizzle High (CPGC_SEQ_ROW_ADDR_SWIZZLE_C)—Offset 4AD4h

This register is used to swizzle the Logical to Physical Row bits.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2307B9ACh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:25	11h RW	**Row 17 Swizzle (L2P_ROW17_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value. Only Row address bits available to the memory controller are valid, others should be set to 0x1F.
24:20	10h RW	**Row 16 Swizzle (L2P_ROW16_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
19:15	Fh RW	**Row 15 Swizzle (L2P_ROW15_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
14:10	Eh RW	**Row 14 Swizzle (L2P_ROW14_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
9:5	Dh RW	**Row 13 Swizzle (L2P_ROW13_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.

Bit Range	Default & Access	Field Name (ID): Description
4:0	Ch RW	**Row 12 Swizzle (L2P_ROW12_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.

5.11.239 Row Address XOR (CPGC_SEQ_ROW_ADDR_SWIZZLE_X)—Offset 4AD8h

Row XOR source selection for lower order Row addresses.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW	**Address DQ Invert Enable (ADDR_DQ_INV_EN):** Enables the lookup table to invert the DQs based on select Row address bits.
28:20	0h RO	Reserved.
19:15	1Fh RW	**Row 3 XOR Swizzle (L2P_ROW3_XOR_SWIZZLE):** Row XOR source selection for lower order Row addresses. Select 31 if only using a direct mapping with no XOR.
14:10	1Fh RW	**Row 2 XOR Swizzle (L2P_ROW2_XOR_SWIZZLE):** Row XOR source selection for lower order Row addresses. Select 31 if only using a direct mapping with no XOR.
9:5	1Fh RW	**Row 1 XOR Swizzle (L2P_ROW1_XOR_SWIZZLE):** Row XOR source selection for lower order Row addresses. Select 31 if only using a direct mapping with no XOR.
4:0	1Fh RW	**Row 0 XOR Swizzle (L2P_ROW0_XOR_SWIZZLE):** Row XOR source selection for lower order Row addresses. Select 31 if only using a direct mapping with no XOR. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.

5.11.240 Column Address Swizzle Low (CPGC_SEQ_COL_ADDR_SWIZZLE_A)—Offset 4ADCh

This register is used to swizzle the Logical to Physical COL bits.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 65432100h

Bit Range	Default & Access	Field Name (ID): Description
31:28	6h RW	**Column 6 Swizzle (L2P_COL6_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other. Rank Bits start at select value of 12. A value of 11 will select a constant '0' value.
27:24	5h RW	**Column 5 Swizzle (L2P_COL5_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.
23:20	4h RW	**Column 4 Swizzle (L2P_COL4_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.
19:16	3h RW	**Column 3 Swizzle (L2P_COL3_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.
15:12	2h RW	**Column 2 Swizzle (L2P_COL2_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.
11:8	1h RW	**Column 1 Swizzle (L2P_COL1_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.
7:4	0h RW	**Column 0 Swizzle (L2P_COL0_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other. Column Address Bit 0 always corresponds to the logical A[6] for 64B requests and A[5] for 32B requests.
3:0	0h RO	Reserved.

5.11.241 Column Address Swizzle High (CPGC_SEQ_COL_ADDR_SWIZZLE_B)—Offset 4AE0h

This register is used to swizzle the Logical to Physical COL bits.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 87h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:4	8h RW	**Column 8 Swizzle (L2P_COL8_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other. Rank Bits start at select value of 12. A value of 11 will select a constant '0' value. Only Row address bits available to the memory controller are valid, others should be set to 11.
3:0	7h RW	**Column 7 Swizzle (L2P_COL7_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.

5.11.242 DQ Inversion Lookup Data Low (CPGC_SEQ_ROW_ADDR_DQ_MAP0)—Offset 4AE8h

DQ Map Register 0 - This register should be 64-bit aligned at an even address - 0x0 or 0x8.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** Data written to this register will be placed in the DQ Map register as a stack. Data is read from the bottom of the stack (higher locations). The last write covers Row addresses of Row[11:4] = (0..31). Reading requires you to write into the stack to get the next location. Since this is destructive, if the data is to be preserved, then the data read should be used for the write.

5.11.243 DQ Inversion Lookup Data High (CPGC_SEQ_ROW_ADDR_DQ_MAP1)—Offset 4AECh

DQ Map Register 1 - This register should be 64-bit aligned at the following odd address - 0x4 or 0xC.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** Data written to this register will be placed in the DQ Map register as a stack. Data is read from the bottom of the stack (higher locations). The last write covers Row addresses of Row[11:4] = (32..63). Reading requires you to write into the stack to get the next location. Since this is destructive, if the data is to be preserved, then the data read should be used for the write.

5.12 Registers Summary

Table 5-12. Summary of cpgc_t_submap Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3C00h	3C03h	SAI Control Policy LSB (CPGC2_ACCESS_CONTROL_POLICY_L)—Offset 3C00h	61010202h
3C04h	3C07h	SAI Control Policy MSB (CPGC2_ACCESS_CONTROL_POLICY_H)—Offset 3C04h	C00h
3C08h	3C0Bh	SAI Read Policy LSB (CPGC2_ACCESS_READ_POLICY_L)—Offset 3C08h	FFFFFF3Fh
3C0Ch	3C0Fh	SAI Read Policy MSB (CPGC2_ACCESS_READ_POLICY_H)—Offset 3C0Ch	1371FFFh
3C10h	3C13h	SAI Write Policy LSB (CPGC2_ACCESS_WRITE_POLICY_L)—Offset 3C10h	1000212h
3C14h	3C17h	SAI Write Policy MSB (CPGC2_ACCESS_WRITE_POLICY_H)—Offset 3C14h	C00h
3C18h	3C1Bh	Address Decode Repeats (CPGC2_ADDRESS_CONTROL)—Offset 3C18h	0h
3C1Ch	3C1Ch	Address Instruction (CPGC2_ADDRESS_INSTRUCTION[0])—Offset 3C1Ch	0h
3C1Dh	3C1Dh	Address Instruction (CPGC2_ADDRESS_INSTRUCTION[1])—Offset 3C1Dh	0h
3C1Eh	3C1Eh	Address Instruction (CPGC2_ADDRESS_INSTRUCTION[2])—Offset 3C1Eh	0h
3C1Fh	3C1Fh	Address Instruction (CPGC2_ADDRESS_INSTRUCTION[3])—Offset 3C1Fh	0h
3C20h	3C20h	Data Instruction (CPGC2_DATA_INSTRUCTION[0])—Offset 3C20h	0h
3C21h	3C21h	Data Instruction (CPGC2_DATA_INSTRUCTION[1])—Offset 3C21h	0h
3C22h	3C22h	Data Instruction (CPGC2_DATA_INSTRUCTION[2])—Offset 3C22h	0h
3C23h	3C23h	Data Instruction (CPGC2_DATA_INSTRUCTION[3])—Offset 3C23h	0h
3C24h	3C27h	Data Rotation Repeats (CPGC2_DATA_CONTROL)—Offset 3C24h	0h
3C28h	3C2Bh	Address and Data Repeats Status (CPGC2_ADDRESS_DATA_STATUS)—Offset 3C28h	0h
3C2Ch	3C2Ch	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[0])—Offset 3C2Ch	0h
3C2Dh	3C2Dh	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[1])—Offset 3C2Dh	0h
3C2Eh	3C2Eh	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[2])—Offset 3C2Eh	0h
3C2Fh	3C2Fh	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[3])—Offset 3C2Fh	0h

Table 5-12. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3C30h	3C30h	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[4])—Offset 3C30h	0h
3C31h	3C31h	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[5])—Offset 3C31h	0h
3C32h	3C32h	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[6])—Offset 3C32h	0h
3C33h	3C33h	Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[7])—Offset 3C33h	0h
3C34h	3C34h	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[0])—Offset 3C34h	0h
3C35h	3C35h	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[1])—Offset 3C35h	0h
3C36h	3C36h	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[2])—Offset 3C36h	0h
3C37h	3C37h	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[3])—Offset 3C37h	0h
3C38h	3C38h	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[4])—Offset 3C38h	0h
3C39h	3C39h	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[5])—Offset 3C39h	0h
3C3Ah	3C3Ah	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[6])—Offset 3C3Ah	0h
3C3Bh	3C3Bh	Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[7])—Offset 3C3Bh	0h
3C3Ch	3C3Fh	Wait Timer Current (CPGC2_ALGORITHM_WAIT_COUNT_CURRENT)—Offset 3C3Ch	0h
3C40h	3C43h	Algorithm Wait Event Control (CPGC2_ALGORITHM_WAIT_EVENT_CONTROL)—Offset 3C40h	0h
3C44h	3C47h	Base Repeats (CPGC2_BASE_REPEATS)—Offset 3C44h	0h
3C48h	3C4Bh	Current Base Repeats (CPGC2_BASE_REPEATS_CURRENT)—Offset 3C48h	0h
3C4Ch	3C4Fh	Base Column Repeats (CPGC2_BASE_COL_REPEATS)—Offset 3C4Ch	0h
3C50h	3C53h	Block Repeats (CPGC2_BLOCK_REPEATS)—Offset 3C50h	0h
3C54h	3C57h	Current Block Repeats (CPGC2_BLOCK_REPEATS_CURRENT)—Offset 3C54h	0h
3C58h	3C58h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[0])—Offset 3C58h	0h
3C59h	3C59h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[1])—Offset 3C59h	0h
3C5Ah	3C5Ah	Command Instruction (CPGC2_COMMAND_INSTRUCTION[2])—Offset 3C5Ah	0h
3C5Bh	3C5Bh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[3])—Offset 3C5Bh	0h
3C5Ch	3C5Ch	Command Instruction (CPGC2_COMMAND_INSTRUCTION[4])—Offset 3C5Ch	0h
3C5Dh	3C5Dh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[5])—Offset 3C5Dh	0h
3C5Eh	3C5Eh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[6])—Offset 3C5Eh	0h

Table 5-12. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3C5Fh	3C5Fh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[7])—Offset 3C5Fh	0h
3C60h	3C60h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[8])—Offset 3C60h	0h
3C61h	3C61h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[9])—Offset 3C61h	0h
3C62h	3C62h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[10])—Offset 3C62h	0h
3C63h	3C63h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[11])—Offset 3C63h	0h
3C64h	3C64h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[12])—Offset 3C64h	0h
3C65h	3C65h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[13])—Offset 3C65h	0h
3C66h	3C66h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[14])—Offset 3C66h	0h
3C67h	3C67h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[15])—Offset 3C67h	0h
3C68h	3C68h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[16])—Offset 3C68h	0h
3C69h	3C69h	Command Instruction (CPGC2_COMMAND_INSTRUCTION[17])—Offset 3C69h	0h
3C6Ah	3C6Ah	Command Instruction (CPGC2_COMMAND_INSTRUCTION[18])—Offset 3C6Ah	0h
3C6Bh	3C6Bh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[19])—Offset 3C6Bh	0h
3C6Ch	3C6Ch	Command Instruction (CPGC2_COMMAND_INSTRUCTION[20])—Offset 3C6Ch	0h
3C6Dh	3C6Dh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[21])—Offset 3C6Dh	0h
3C6Eh	3C6Eh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[22])—Offset 3C6Eh	0h
3C6Fh	3C6Fh	Command Instruction (CPGC2_COMMAND_INSTRUCTION[23])—Offset 3C6Fh	0h
3C70h	3C73h	Hammer Repeats (CPGC2_HAMMER_REPEATS)—Offset 3C70h	0h
3C74h	3C77h	Current Hammer Repeats (CPGC2_HAMMER_REPEATS_CURRENT)—Offset 3C74h	0h
3C78h	3C78h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[0])—Offset 3C78h	0h
3C79h	3C79h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[1])—Offset 3C79h	0h
3C7Ah	3C7Ah	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[2])—Offset 3C7Ah	0h
3C7Bh	3C7Bh	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[3])—Offset 3C7Bh	0h
3C7Ch	3C7Ch	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[4])—Offset 3C7Ch	0h
3C7Dh	3C7Dh	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[5])—Offset 3C7Dh	0h
3C7Eh	3C7Eh	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[6])—Offset 3C7Eh	0h

Table 5-12. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3C7Fh	3C7Fh	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[7])—Offset 3C7Fh	0h
3C80h	3C80h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[8])—Offset 3C80h	0h
3C81h	3C81h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[9])—Offset 3C81h	0h
3C82h	3C82h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[10])—Offset 3C82h	0h
3C83h	3C83h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[11])—Offset 3C83h	0h
3C84h	3C84h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[12])—Offset 3C84h	0h
3C85h	3C85h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[13])—Offset 3C85h	0h
3C86h	3C86h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[14])—Offset 3C86h	0h
3C87h	3C87h	Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[15])—Offset 3C87h	0h
3C88h	3C88h	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[0])—Offset 3C88h	0h
3C89h	3C89h	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[1])—Offset 3C89h	0h
3C8Ah	3C8Ah	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[2])—Offset 3C8Ah	0h
3C8Bh	3C8Bh	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[3])—Offset 3C8Bh	0h
3C8Ch	3C8Ch	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[4])—Offset 3C8Ch	0h
3C8Dh	3C8Dh	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[5])—Offset 3C8Dh	0h
3C8Eh	3C8Eh	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[6])—Offset 3C8Eh	0h
3C8Fh	3C8Fh	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[7])—Offset 3C8Fh	0h
3C90h	3C90h	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[8])—Offset 3C90h	0h
3C91h	3C91h	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[9])—Offset 3C91h	0h
3C92h	3C92h	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[10])—Offset 3C92h	0h
3C93h	3C93h	Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[11])—Offset 3C93h	0h
3C94h	3C97h	Offset Repeats (CPGC2_OFFSET_REPEATS[0])—Offset 3C94h	0h
3C98h	3C9Bh	Offset Repeats (CPGC2_OFFSET_REPEATS[1])—Offset 3C98h	0h
3C9Ch	3C9Fh	Current Offset Repeats (CPGC2_OFFSET_REPEATS_CURRENT)—Offset 3C9Ch	0h
3CA0h	3CA3h	Region Low Row Address (CPGC2_REGION_LOW_ROW)—Offset 3CA0h	0h
3CA4h	3CA7h	Region Low Col Address (CPGC2_REGION_LOW_COL)—Offset 3CA4h	0h
3CA8h	3CABh	Block Low Row Current (CPGC2_BLOCK_ORIGIN_ROW_CURRENT)—Offset 3CA8h	0h

Table 5-12. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3CACh	3CAFh	Current Base Address Rank and Column (CPGC2_BASE_ADDRESS_COL_RANK_CURRENT)—Offset 3CACh	0h
3CB0h	3CB3h	Current Base Address Bank and Row (CPGC2_BASE_ADDRESS_ROW_BANK_CURRENT)—Offset 3CB0h	0h
3CB4h	3CB7h	Current Offset Address Column (CPGC2_OFFSET_ADDRESS_COL_CURRENT)—Offset 3CB4h	0h
3CB8h	3CBBh	Current Offset Address Row (CPGC2_OFFSET_ADDRESS_ROW_CURRENT)—Offset 3CB8h	0h
3CBCh	3CBFh	Address Size (CPGC2_ADDRESS_SIZE)—Offset 3CBCh	0h
3CC0h	3CC3h	Base Address Control (CPGC2_BASE_ADDRESS_CONTROL)—Offset 3CC0h	0h
3CC4h	3CC7h	Address PRBS Control (CPGC2_ADDRESS_PRBS_CONTROL)—Offset 3CC4h	0h
3CC8h	3CCBh	Address PRBS Seed (CPGC2_ADDRESS_PRBS_SEED)—Offset 3CC8h	0h
3CCCh	3CCFh	Current Address PRBS Status (CPGC2_ADDRESS_PRBS_CURRENT)—Offset 3CCCh	0h
3CD0h	3CD3h	Address PRBS Save (CPGC2_ADDRESS_PRBS_SAVE)—Offset 3CD0h	0h
3CD4h	3CD7h	Command FSM Current State (CPGC2_CMD_FSM_CURRENT)—Offset 3CD4h	0h
3CD8h	3CDBh	Algorithm Wait Timer Configuration (CPGC2_WAIT_2_START_CONFIG)—Offset 3CD8h	0h
3CDCh	3CDFh	VISA Mux Selection (CPGC2_VISA_MUX_SEL)—Offset 3CDCh	0h
3CE0h	3CE3h	Loopback Sequencer Configuration (CPGC_LB_SEQ_CFG)—Offset 3CE0h	0h
3CE4h	3CE7h	Loopback Sequencer Control (CPGC_LB_SEQ_CTL)—Offset 3CE4h	0h
3CE8h	3CEBh	Loopback Loopcount Tx Status (CPGC_LB_SEQ_LOOPCOUNT_TX_STATUS)—Offset 3CE8h	0h
3CECh	3CEFh	Loopback Loopcount Rx Status (CPGC_LB_SEQ_LOOPCOUNT_RX_STATUS)—Offset 3CECh	0h
3CF0h	3CF3h	Pattern Length Status (CPGC_LB_SEQ_PL_RX_STATUS)—Offset 3CF0h	0h
3CF4h	3CF7h	Refresh Control (CPGC_MISC_REFRESH_CTL)—Offset 3CF4h	0h
3CF8h	3CFBh	ZQ Control (CPGC_MISC_ZQ_CTL)—Offset 3CF8h	0h
3CFCh	3CFFh	ODT Control (CPGC_MISC_ODT_CTL)—Offset 3CFCh	0h
3D00h	3D03h	CKE Control (CPGC_MISC_CKE_CTL)—Offset 3D00h	0h
3D04h	3D07h	Command Rate (CPGC_MISC_CMD_RATE)—Offset 3D04h	100Ah
3D08h	3D0Bh	External Trigger Control (CPGC_MISC_EXT_TRIGGER)—Offset 3D08h	0h
3D0Ch	3D0Fh	Sequence Control (CPGC_SEQ_CTL)—Offset 3D0Ch	0h
3D10h	3D13h	Sequence Configuration A (CPGC_SEQ_CFG_A)—Offset 3D10h	200000h
3D14h	3D17h	Sequence Configuration B (CPGC_SEQ_CFG_B)—Offset 3D14h	0h
3D18h	3D1Bh	Sequence Status (CPGC_SEQ_STATUS)—Offset 3D18h	0h
3D20h	3D23h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[0])—Offset 3D20h	0h
3D24h	3D27h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[1])—Offset 3D24h	0h
3D28h	3D2Bh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[2])—Offset 3D28h	0h

Table 5-12. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3D2Ch	3D2Fh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[3])—Offset 3D2Ch	0h
3D30h	3D33h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[4])—Offset 3D30h	0h
3D34h	3D37h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[5])—Offset 3D34h	0h
3D38h	3D3Bh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[6])—Offset 3D38h	0h
3D3Ch	3D3Fh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[7])—Offset 3D3Ch	0h
3D40h	3D43h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[8])—Offset 3D40h	0h
3D44h	3D47h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[9])—Offset 3D44h	0h
3D48h	3D4Bh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[10])—Offset 3D48h	0h
3D4Ch	3D4Fh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[11])—Offset 3D4Ch	0h
3D50h	3D53h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[12])—Offset 3D50h	0h
3D54h	3D57h	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[13])—Offset 3D54h	0h
3D58h	3D5Bh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[14])—Offset 3D58h	0h
3D5Ch	3D5Fh	Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[15])—Offset 3D5Ch	0h
3D60h	3D63h	Mode3 Fail Status LSB (CPGC2_RASTER_REPO_CONTENT_ECC1)—Offset 3D60h	0h
3D64h	3D67h	Mode3 Fail Status MSB (CPGC2_RASTER_REPO_CONTENT_ECC2)—Offset 3D64h	0h
3D68h	3D6Bh	Read Command Count (CPGC2_READ_COMMAND_COUNT_CURRENT)—Offset 3D68h	0h
3D6Ch	3D6Fh	Mask Errors on First N Reads (CPGC2_MASK_ERRS_FIRST_N_READS)—Offset 3D6Ch	0h
3D70h	3D73h	Raster Repository Status (CPGC2_RASTER_REPO_STATUS)—Offset 3D70h	0h
3D74h	3D77h	Error Summary A (CPGC2_ERR_SUMMARY_A)—Offset 3D74h	0h
3D78h	3D7Bh	Error Summary B (CPGC2_ERR_SUMMARY_B)—Offset 3D78h	0h
3D7Ch	3D7Fh	Future use Reserved (CPGC2_ERR_SUMMARY_C)—Offset 3D7Ch	0h
3D80h	3D83h	Data Pattern Generation Buffer Control (CPGC_DPAT_BUF_CTL)—Offset 3D80h	0h
3D84h	3D87h	Data Pattern Generation Configuration (CPGC_DPAT_CFG)—Offset 3D84h	0h
3D88h	3D8Bh	LFSR Configuration and Lane Rotate (CPGC_DPAT_XTRA_LFSR_CFG)—Offset 3D88h	0h
3D8Ch	3D8Fh	Unisequencer Data Pattern Buffer (CPGC_DPAT_UNISEQ[0])—Offset 3D8Ch	AA55AA55h
3D90h	3D93h	Unisequencer Data Pattern Buffer (CPGC_DPAT_UNISEQ[1])—Offset 3D90h	AA55AA55h

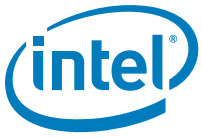


Table 5-12. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3D94h	3D97h	Unisequencer Data Pattern Buffer (CPGC_DPAT_UNISEQ[2])—Offset 3D94h	AA55AA55h
3D98h	3D9Bh	Unisequencer LMN Control (CPGC_DPAT_UNISEQ_LMN[0])—Offset 3D98h	1010100h
3D9Ch	3D9Fh	Unisequencer LMN Control (CPGC_DPAT_UNISEQ_LMN[1])—Offset 3D9Ch	1010100h
3DA0h	3DA3h	Unisequencer LMN Control (CPGC_DPAT_UNISEQ_LMN[2])—Offset 3DA0h	1010100h
3DA4h	3DA7h	Invert and DC Control (CPGC_DPAT_INVDCCTL)—Offset 3DA4h	AA0000h
3DA8h	3DABh	Data Invert/DC Enable Low (CPGC_DPAT_INV_DC_MASK_LO)—Offset 3DA8h	0h
3DACh	3DAFh	Data Invert/DC Enable High (CPGC_DPAT_INV_DC_MASK_HI)—Offset 3DACh	0h
3DB0h	3DB3h	Byte Enable Mask Lower (CPGC_DPAT_DRAMDM)—Offset 3DB0h	FFFFFFFFh
3DB4h	3DB7h	Byte Enable Mask Upper (CPGC_DPAT_XDRAMDM)—Offset 3DB4h	FFFFFFFFh
3DB8h	3DBBh	Unisequencer Status - Write (CPGC_DPAT_UNISEQ_WRSTAT[0])—Offset 3DB8h	0h
3DBCh	3DBFh	Unisequencer Status - Write (CPGC_DPAT_UNISEQ_WRSTAT[1])—Offset 3DBCh	0h
3DC0h	3DC3h	Unisequencer Status - Write (CPGC_DPAT_UNISEQ_WRSTAT[2])—Offset 3DC0h	0h
3DC4h	3DC7h	Unisequencer Status - Read (CPGC_DPAT_UNISEQ_RDSTAT[0])—Offset 3DC4h	DEADBEEFh
3DC8h	3DCBh	Unisequencer Status - Read (CPGC_DPAT_UNISEQ_RDSTAT[1])—Offset 3DC8h	DEADBEEFh
3DCCh	3DCFh	Unisequencer Status - Read (CPGC_DPAT_UNISEQ_RDSTAT[2])—Offset 3DCCh	DEADBEEFh
3DD0h	3DD3h	LMN Status - Write (CPGC_DPAT_LMN_WRSTAT[0])—Offset 3DD0h	0h
3DD4h	3DD7h	LMN Status - Write (CPGC_DPAT_LMN_WRSTAT[1])—Offset 3DD4h	0h
3DD8h	3DDBh	LMN Status - Write (CPGC_DPAT_LMN_WRSTAT[2])—Offset 3DD8h	0h
3DDCh	3DDFh	LMN Status - Read (CPGC_DPAT_LMN_RDSTAT[0])—Offset 3DDCh	DEADBEEFh
3DE0h	3DE3h	LMN Status - Read (CPGC_DPAT_LMN_RDSTAT[1])—Offset 3DE0h	DEADBEEFh
3DE4h	3DE7h	LMN Status - Read (CPGC_DPAT_LMN_RDSTAT[2])—Offset 3DE4h	DEADBEEFh
3DE8h	3DEBh	Unisequencer Save Status - Write (CPGC_DPAT_UNISEQ_WRSAVE[0])—Offset 3DE8h	DEADBEEFh
3DECh	3DEFh	Unisequencer Save Status - Write (CPGC_DPAT_UNISEQ_WRSAVE[1])—Offset 3DECh	DEADBEEFh
3DF0h	3DF3h	Unisequencer Save Status - Write (CPGC_DPAT_UNISEQ_WRSAVE[2])—Offset 3DF0h	DEADBEEFh
3DF4h	3DF7h	Unisequencer Save Status - Read (CPGC_DPAT_UNISEQ_RDSAVE[0])—Offset 3DF4h	0h
3DF8h	3DFBh	Unisequencer Save Status - Read (CPGC_DPAT_UNISEQ_RDSAVE[1])—Offset 3DF8h	0h
3DFCh	3DFFh	Unisequencer Save Status - Read (CPGC_DPAT_UNISEQ_RDSAVE[2])—Offset 3DFCh	0h
3E00h	3E03h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[0])—Offset 3E00h	AAAAAAAAh
3E04h	3E07h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[1])—Offset 3E04h	AAAAAAAAh
3E08h	3E0Bh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[2])—Offset 3E08h	AAAAAAAAh

Table 5-12. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3E0Ch	3E0Fh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[3])—Offset 3E0Ch	AAAAAAAAh
3E10h	3E13h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[4])—Offset 3E10h	AAAAAAAAh
3E14h	3E17h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[5])—Offset 3E14h	AAAAAAAAh
3E18h	3E1Bh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[6])—Offset 3E18h	AAAAAAAAh
3E1Ch	3E1Fh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[7])—Offset 3E1Ch	AAAAAAAAh
3E20h	3E23h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[8])—Offset 3E20h	AAAAAAAAh
3E24h	3E27h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[9])—Offset 3E24h	AAAAAAAAh
3E28h	3E2Bh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[10])—Offset 3E28h	AAAAAAAAh
3E2Ch	3E2Fh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[11])—Offset 3E2Ch	AAAAAAAAh
3E30h	3E33h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[12])—Offset 3E30h	AAAAAAAAh
3E34h	3E37h	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[13])—Offset 3E34h	AAAAAAAAh
3E38h	3E3Bh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[14])—Offset 3E38h	AAAAAAAAh
3E3Ch	3E3Fh	Extended Pattern Buffer (CPGC_DPAT_EXTBUF[15])—Offset 3E3Ch	AAAAAAAAh
3E40h	3E43h	Error Checker Control (CPGC_ERR_CTL)—Offset 3E40h	0h
3E44h	3E47h	Lane Error Mask Lower Bytes (CPGC_ERR_LNEN_LO)—Offset 3E44h	0h
3E48h	3E4Bh	Lane Error Mask Upper Bytes or Extended Chunk Enable (CPGC_ERR_LNEN_HI)—Offset 3E48h	0h
3E4Ch	3E4Fh	Lane Error Mask ECC (CPGC_ERR_XLNEN)—Offset 3E4Ch	FFh
3E50h	3E53h	Lane Error Status Lower Bytes (CPGC_ERR_STAT03)—Offset 3E50h	0h
3E54h	3E57h	Lane Error Status Upper Bytes or Extended Chunk Error Status (CPGC_ERR_STAT47)—Offset 3E54h	0h
3E58h	3E5Bh	ECC Lane Error Status (CPGC_ERR_ECC_CHNK_RANK_STAT)—Offset 3E58h	0h
3E5Ch	3E5Fh	ByteGroup Error Status (CPGC_ERR_BYTE_NTH_PAR_STAT)—Offset 3E5Ch	0h
3E60h	3E63h	Error Counter Control (CPGC_ERR_CNTRCTL[0])—Offset 3E60h	0h
3E64h	3E67h	Error Counter Control (CPGC_ERR_CNTRCTL[1])—Offset 3E64h	0h
3E68h	3E6Bh	Error Counter Control (CPGC_ERR_CNTRCTL[2])—Offset 3E68h	0h
3E6Ch	3E6Fh	Error Counter Control (CPGC_ERR_CNTRCTL[3])—Offset 3E6Ch	0h
3E70h	3E73h	Error Counter Control (CPGC_ERR_CNTRCTL[4])—Offset 3E70h	0h
3E74h	3E77h	Error Counter Control (CPGC_ERR_CNTRCTL[5])—Offset 3E74h	0h
3E78h	3E7Bh	Error Counter Control (CPGC_ERR_CNTRCTL[6])—Offset 3E78h	0h
3E7Ch	3E7Fh	Error Counter Control (CPGC_ERR_CNTRCTL[7])—Offset 3E7Ch	0h
3E80h	3E83h	Error Counter Control (CPGC_ERR_CNTRCTL[8])—Offset 3E80h	0h
3E84h	3E87h	Error Counter (CPGC_ERR_CNTR[0])—Offset 3E84h	0h
3E88h	3E8Bh	Error Counter (CPGC_ERR_CNTR[1])—Offset 3E88h	0h
3E8Ch	3E8Fh	Error Counter (CPGC_ERR_CNTR[2])—Offset 3E8Ch	0h
3E90h	3E93h	Error Counter (CPGC_ERR_CNTR[3])—Offset 3E90h	0h
3E94h	3E97h	Error Counter (CPGC_ERR_CNTR[4])—Offset 3E94h	0h
3E98h	3E9Bh	Error Counter (CPGC_ERR_CNTR[5])—Offset 3E98h	0h
3E9Ch	3E9Fh	Error Counter (CPGC_ERR_CNTR[6])—Offset 3E9Ch	0h
3EA0h	3EA3h	Error Counter (CPGC_ERR_CNTR[7])—Offset 3EA0h	0h

Table 5-12. Summary of cpgc_t_submap Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3EA4h	3EA7h	Error Counter (CPGC_ERR_CNTR[8])—Offset 3EA4h	0h
3EA8h	3EABh	Error Counter Overflow (CPGC_ERR_CNTR_OV)—Offset 3EA8h	0h
3EACh	3EAFh	Error Log Control and Status (CPGC_ERRLOG_CTL_STAT)—Offset 3EACh	0h
3EB0h	3EB3h	Error Log Data Access (CPGC_ERRLOG_DATA)—Offset 3EB0h	0h
3EB4h	3EB7h	Loopback Error Status (CPGC_ERR_TEST_ERR_STAT)—Offset 3EB4h	0h
3EB8h	3EBBh	Rank Logical To Physical Map (CPGC_SEQ_RANK_L2P_MAPPING)—Offset 3EB8h	76543210h
3EBCh	3EBFh	Bank Logical to Physical Map Low (CPGC_SEQ_BANK_L2P_MAPPING_A)—Offset 3EBCh	76543210h
3EC0h	3EC3h	Bank Logical to Physical Map High (CPGC_SEQ_BANK_L2P_MAPPING_B)—Offset 3EC0h	FEDCBA98h
3EC4h	3EC7h	Rank Address Swizzle (CPGC_SEQ_RANK_ADDR_SWIZZLE)—Offset 3EC4h	FEDCh
3EC8h	3ECBh	Bank Address Swizzle (CPGC_SEQ_BANK_ADDR_SWIZZLE)—Offset 3EC8h	DEB38h
3ECCh	3ECFh	Row Address Swizzle Low (CPGC_SEQ_ROW_ADDR_SWIZZLE_A)—Offset 3ECCh	A418820h
3ED0h	3ED3h	Row Address Swizzle Mid (CPGC_SEQ_ROW_ADDR_SWIZZLE_B)—Offset 3ED0h	16A4A0E6h
3ED4h	3ED7h	Row Address Swizzle High (CPGC_SEQ_ROW_ADDR_SWIZZLE_C)—Offset 3ED4h	2307B9ACh
3ED8h	3EDBh	Row Address XOR (CPGC_SEQ_ROW_ADDR_SWIZZLE_X)—Offset 3ED8h	FFFFFh
3EDCh	3EDFh	Column Address Swizzle Low (CPGC_SEQ_COL_ADDR_SWIZZLE_A)—Offset 3EDCh	65432100h
3EE0h	3EE3h	Column Address Swizzle High (CPGC_SEQ_COL_ADDR_SWIZZLE_B)—Offset 3EE0h	87h
3EE8h	3EEBh	DQ Inversion Lookup Data Low (CPGC_SEQ_ROW_ADDR_DQ_MAP0)—Offset 3EE8h	0h
3EECh	3EEFh	DQ Inversion Lookup Data High (CPGC_SEQ_ROW_ADDR_DQ_MAP1)—Offset 3EECh	0h

5.12.1 SAI Control Policy LSB (CPGC2_ACCESS_CONTROL_POLICY_L)—Offset 3C00h

Lower half of the SAI Control Policy.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 61010202h

Bit Range	Default & Access	Field Name (ID): Description
31:0	61010202h RW	**Access Control Policy LSB (Control_Policy_L):** Lower half of the SAI Control Policy Value [31:0].

5.12.2 SAI Control Policy MSB (CPGC2_ACCESS_CONTROL_POLICY_H)—Offset 3C04h

Upper half of the SAI Control Policy.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	C00h RW	**Access Control Policy MSB (Control_Policy_H):** Upper half of the SAI Control Policy Value [63:32].

5.12.3 SAI Read Policy LSB (CPGC2_ACCESS_READ_POLICY_L)—Offset 3C08h

Lower half of the SAI Read Policy.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFFFF3Fh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFF3Fh RW	**Access Read Policy LSB (Read_Policy_L):** Lower half of the SAI Read Policy Value [31:0].

5.12.4 SAI Read Policy MSB (CPGC2_ACCESS_READ_POLICY_H)—Offset 3C0Ch

Upper half of the SAI Read Policy.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1371FFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	1371FFFh RW	**Access Read Policy MSB (Read_Policy_H):** Upper half of the SAI Read Policy Value [63:32].

5.12.5 SAI Write Policy LSB (CPGC2_ACCESS_WRITE_POLICY_L)—Offset 3C10h

Lower half of the SAI Write Policy.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1000212h

Bit Range	Default & Access	Field Name (ID): Description
31:0	1000212h RW	**Access Write Policy LSB (Write_Policy_L):** Lower half of the SAI Write Policy Value [31:0].

5.12.6 SAI Write Policy MSB (CPGC2_ACCESS_WRITE_POLICY_H)—Offset 3C14h

Upper half of the SAI Write Policy.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: C00h

Bit Range	Default & Access	Field Name (ID): Description
31:0	C00h RW	**Access Write Policy MSB (Write_Policy_H):** Upper half of the SAI Write Policy Value [63:32].

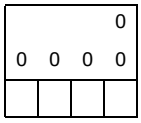
5.12.7 Address Decode Repeats (CPGC2_ADDRESS_CONTROL)—Offset 3C18h

If Algorithm_Address_#.Bits(6:6) is set to 1, then Address Decode is enabled.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5:0	0h RW	**Address Decode Repeats (Address_Decode_Rotate_Repeats):** Number of times the current Address_Instruction will repeat if Address_Decode_Enable is set (as N-1) (0=1 time). If for the current Address_Instruction, Address_Decode_Enable is set, then at the start of that Address_Instruction, initialize the XOR_Address_Pattern to a single 1 in the LSB of Column Address. Otherwise, it is initialized to all zero's. For (Address_Decode_Rotate_Repeat_Current = 0; Current_ Address_Decode_Rotate_Repeat_Current <= Address_Decode_Rotate_Repeat; Address_Decode_Rotate_Repeat_Current ++) Execute the entire Algorithm (Block Traversal, Algorithm_Instruction, Commands) with the following behavior: At the end of each complete Block Traversal, rotate the XOR Address Pattern 1 bit position from LSB to MSB (Column through Region_Bits_Column, Region_Bits_Row, Region_Num_Banks, and through Region_Num_Ranks). Region_Size.Num_Bank and Region_Size.Num_Rank numbers are converted to the equivalent number of adddress bits to cover their range (ceil(log2(Num+1))) and should be programmed to a power of 2 value (minus 1): 1,3,7, or 15. If only one Rank is being tested, then you should limit the amount in this register to the sum of the number of address bits without Rank bits.

5.12.8 Address Instruction (CPGC2_ADDRESS_INSTRUCTION[0])—Offset 3C1Ch

Address Instruction controlling Address_Order and Address_Direction reversal and decode rotation/loop.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Address Instruction (Last):** If set, then this is the last Address Instruction and the test will terminate following full execution of this instruction. If there are no Last bits set in the Address Instruction list, then the test will not stop due to a completion of the test, but will be an Infinite Test.
6	0h RW	**Address Decode Enable (Address_Decode_Enable):** Enables rotating XOR of address bits. Used in concert with the Address_Decode_Enable field in the Command_Instruction list. This bit enables repeating of the current Address_Instruction for Address_Decode_Rotate_Repeats times.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(10) Inv(FastX) - North West** Increment Column and Decrement Row and Carry Decrement Column into Row. **(0)(11) Diagonal2 - East** Increment Row and Carry Increment into Column. **(1)(11) Inv(Diagonal2) West** Decrement Row and Carry Decrement into Column. Note that the Bank and Rank Address direction follows the same as the Column (Increment or Decrement). Note for diagonal directions, a Carry results in twice the normal increment/decrement of the Row field. Incrementing fields start at 0, and Decrementing fields start at 2^(field_block_size)-2^(field_increment)= top of block.
2:0	0h RW	**Address Order (Address_Order):** Controls the fastest changing address field, and how that carries into higher order fields. 000 Rank, Bank, Row/Col. 001 Rank, Row/Col, Bank. 010 Bank, Rank, Row/Col. 011 Bank, Row/Col, Rank. 100 Row/Col, Rank, Bank. 101 Row/Col, Bank, Rank. 110 Row/Col (Used for Offset) Rank and Bank are unchanged. 111 Row-Col (Used for Stripe Offset) No Carry from any field to another. Carry order between Row and Column is dependent on the Address_Direction field.

5.12.9 Address Instruction (CPGC2_ADDRESS_INSTRUCTION[1])—Offset 3C1Dh

Address Instruction controlling Address_Order and Address_Direction reversal and decode rotation/loop.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Address Instruction (Last):** If set, then this is the last Address Instruction and the test will terminate following full execution of this instruction. If there are no Last bits set in the Address Instruction list, then the test will not stop due to a completion of the test, but will be an Infinite Test.
6	0h RW	**Address Decode Enable (Address_Decode_Enable):** Enables rotating XOR of address bits. Used in concert with the Address_Decode_Enable field in the Command_Instruction list. This bit enables repeating of the current Address_Instruction for Address_Decode_Rotate_Repeats times.

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(10) Inv(FastX) - North West** Increment Column and Decrement Row and Carry Decrement Column into Row. **(0)(11) Diagonal2 - East** Increment Row and Carry Increment into Column. **(1)(11) Inv(Diagonal2) West** Decrement Row and Carry Decrement into Column. Note that the Bank and Rank Address direction follows the same as the Column (Increment or Decrement). Note for diagonal directions, a Carry results in twice the normal increment/decrement of the Row field. Incrementing fields start at 0, and Decrementing fields start at 2^(field_block_size)-2^(field_increment)= top of block.
2:0	0h RW	**Address Order (Address_Order):** Controls the fastest changing address field, and how that carries into higher order fields. 000 Rank, Bank, Row/Col. 001 Rank, Row/Col, Bank. 010 Bank, Rank, Row/Col. 011 Bank, Row/Col, Rank. 100 Row/Col, Rank, Bank. 101 Row/Col, Bank, Rank. 110 Row/Col (Used for Offset) Rank and Bank are unchanged. 111 Row-Col (Used for Stripe Offset) No Carry from any field to another. Carry order between Row and Column is dependent on the Address_Direction field.

5.12.10 Address Instruction (CPGC2_ADDRESS_INSTRUCTION[2])—Offset 3C1Eh

Address Instruction controlling Address_Order and Address_Direction reversal and decode rotation/loop.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Address Instruction (Last):** If set, then this is the last Address Instruction and the test will terminate following full execution of this instruction. If there are no Last bits set in the Address Instruction list, then the test will not stop due to a completion of the test, but will be an Infinite Test.
6	0h RW	**Address Decode Enable (Address_Decode_Enable):** Enables rotating XOR of address bits. Used in concert with the Address_Decode_Enable field in the Command_Instruction list. This bit enables repeating of the current Address_Instruction for Address_Decode_Rotate_Repeats times.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(10) Inv(FastX) - North West** Increment Column and Decrement Row and Carry Decrement Column into Row. **(0)(11) Diagonal2 - East** Increment Row and Carry Increment into Column. **(1)(11) Inv(Diagonal2) West** Decrement Row and Carry Decrement into Column. Note that the Bank and Rank Address direction follows the same as the Column (Increment or Decrement). Note for diagonal directions, a Carry results in twice the normal increment/decrement of the Row field. Incrementing fields start at 0, and Decrementing fields start at 2^(field_block_size)-2^(field_increment)= top of block.

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RW	**Address Order (Address_Order):** Controls the fastest changing address field, and how that carries into higher order fields. 000 Rank, Bank, Row/Col. 001 Rank, Row/Col, Bank. 010 Bank, Rank, Row/Col. 011 Bank, Row/Col, Rank. 100 Row/Col, Rank, Bank. 101 Row/Col, Bank, Rank. 110 Row/Col (Used for Offset) Rank and Bank are unchanged. 111 Row-Col (Used for Stripe Offset) No Carry from any field to another. Carry order between Row and Column is dependent on the Address_Direction field.

5.12.11 Address Instruction (CPGC2_ADDRESS_INSTRUCTION[3])—Offset 3C1Fh

Address Instruction controlling Address_Order and Address_Direction reversal and decode rotation/loop.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Address Instruction (Last):** If set, then this is the last Address Instruction and the test will terminate following full execution of this instruction. If there are no Last bits set in the Address Instruction list, then the test will not stop due to a completion of the test, but will be an Infinite Test.
6	0h RW	**Address Decode Enable (Address_Decode_Enable):** Enables rotating XOR of address bits. Used in concert with the Address_Decode_Enable field in the Command_Instruction list. This bit enables repeating of the current Address_Instruction for Address_Decode_Rotate_Repeats times.

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(10) Inv(FastX) - North West** Increment Column and Decrement Row and Carry Decrement Column into Row. **(0)(11) Diagonal2 - East** Increment Row and Carry Increment into Column. **(1)(11) Inv(Diagonal2) West** Decrement Row and Carry Decrement into Column. Note that the Bank and Rank Address direction follows the same as the Column (Increment or Decrement). Note for diagonal directions, a Carry results in twice the normal increment/decrement of the Row field. Incrementing fields start at 0, and Decrementing fields start at 2^(field_block_size)-2^(field_increment)= top of block.
2:0	0h RW	**Address Order (Address_Order):** Controls the fastest changing address field, and how that carries into higher order fields. 000 Rank, Bank, Row/Col. 001 Rank, Row/Col, Bank. 010 Bank, Rank, Row/Col. 011 Bank, Row/Col, Rank. 100 Row/Col, Rank, Bank. 101 Row/Col, Bank, Rank. 110 Row/Col (Used for Offset) Rank and Bank are unchanged. 111 Row-Col (Used for Stripe Offset) No Carry from any field to another. Carry order between Row and Column is dependent on the Address_Direction field.

5.12.12 Data Instruction (CPGC2_DATA_INSTRUCTION[0])—Offset 3C20h

Data Instruction controlling Alternate Data rotation, Background inversion pattern and Data Inversion.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Data Instruction (Last):** Last Data_Instruction indication, execution is continued at Data_Instruction[0] if the test does not otherwise terminate. This bit is implied to be set for Data_Instruction[3].
6	0h RW	**Invert Data (Invert_Data):** Globally Invert all data. Combined with the Algorithm_Instruction Invert_Data field, and the Command_Instruction or Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5:4	0h RW	**Data Background (Data_Background):** 00 - Solid 01 - Column Stripes 10 - Row Stripes 11 - Checkerboard
3	0h RW	**Data Select Rotate Enable (Data_Select_Rotation_Enable):** Enables rotating lane pattern data. Used in concert with the Data_Select_Rotation_Enable field in the Data_Instruction list. This bit enables repeating of the current Data_Instruction for Data_Select_Rotation_Repeat times. Data generated using the advanced pattern generation will rotate by one data bit (LSB toward MSB) for each Data_Select_Rotation_Repeat. For the purpose of this shift, the order follows the Address_Instruction Address_Order and the Algorithm_Instruction[0] Address_Direction.
2:0	0h RO	Reserved.

5.12.13 Data Instruction (CPGC2_DATA_INSTRUCTION[1])—Offset 3C21h

Data Instruction controlling Alternate Data rotation, Background inversion pattern and Data Inversion.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Data Instruction (Last):** Last Data_Instruction indication, execution is continued at Data_Instruction[0] if the test does not otherwise terminate. This bit is implied to be set for Data_Instruction[3].

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Invert Data (Invert_Data):** Globally Invert all data. Combined with the Algorithm_Instruction Invert_Data field, and the Command_Instruction or Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5:4	0h RW	**Data Background (Data_Background):** 00 - Solid 01 - Column Stripes 10 - Row Stripes 11 - Checkerboard
3	0h RW	**Data Select Rotate Enable (Data_Select_Rotation_Enable):** Enables rotating lane pattern data. Used in concert with the Data_Select_Rotation_Enable field in the Data_Instruction list. This bit enables repeating of the current Data_Instruction for Data_Select_Rotation_Repeat times. Data generated using the advanced pattern generation will rotate by one data bit (LSB toward MSB) for each Data_Select_Rotation_Repeat. For the purpose of this shift, the order follows the Address_Instruction Address_Order and the Algorithm_Instruction[0] Address_Direction.
2:0	0h RO	Reserved.

5.12.14 Data Instruction (CPGC2_DATA_INSTRUCTION[2])—Offset 3C22h

Data Instruction controlling Alternate Data rotation, Background inversion pattern and Data Inversion.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Data Instruction (Last):** Last Data_Instruction indication, execution is continued at Data_Instruction[0] if the test does not otherwise terminate. This bit is implied to be set for Data_Instruction[3].
6	0h RW	**Invert Data (Invert_Data):** Globally Invert all data. Combined with the Algorithm_Instruction Invert_Data field, and the Command_Instruction or Offset_Command_Instruction Invert_Data field to determine the final data polarity.

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Data Background (Data_Background):** 00 - Solid 01 - Column Stripes 10 - Row Stripes 11 - Checkerboard
3	0h RW	**Data Select Rotate Enable (Data_Select_Rotation_Enable):** Enables rotating lane pattern data. Used in concert with the Data_Select_Rotation_Enable field in the Data_Instruction list. This bit enables repeating of the current Data_Instruction for Data_Select_Rotation_Repeat times. Data generated using the advanced pattern generation will rotate by one data bit (LSB toward MSB) for each Data_Select_Rotation_Repeat. For the purpose of this shift, the order follows the Address_Instruction Address_Order and the Algorithm_Instruction[0] Address_Direction.
2:0	0h RO	Reserved.

5.12.15 Data Instruction (CPGC2_DATA_INSTRUCTION[3])—Offset 3C23h

Data Instruction controlling Alternate Data rotation, Background inversion pattern and Data Inversion.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Data Instruction (Last):** Last Data_Instruction indication, execution is continued at Data_Instruction[0] if the test does not otherwise terminate. This bit is implied to be set for Data_Instruction[3].
6	0h RW	**Invert Data (Invert_Data):** Globally Invert all data. Combined with the Algorithm_Instruction Invert_Data field, and the Command_Instruction or Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5:4	0h RW	**Data Background (Data_Background):** 00 - Solid 01 - Column Stripes 10 - Row Stripes 11 - Checkerboard

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Data Select Rotate Enable (Data_Select_Rotation_Enable):** Enables rotating lane pattern data. Used in concert with the Data_Select_Rotation_Enable field in the Data_Instruction list. This bit enables repeating of the current Data_Instruction for Data_Select_Rotation_Repeat times. Data generated using the advanced pattern generation will rotate by one data bit (LSB toward MSB) for each Data_Select_Rotation_Repeat. For the purpose of this shift, the order follows the Address_Instruction Address_Order and the Algorithm_Instruction[0] Address_Direction.
2:0	0h RO	Reserved.

5.12.16 Data Rotation Repeats (CPGC2_DATA_CONTROL)—Offset 3C24h

Number of times an enabled Data_Instruction will be repeated.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**Data Rotation Repeats (Data_Select_Rotation_Repeats):** Any Data_Instruction with Data_Select_Rotation_Enable will repeat this many times. As N-1. (0=1 time)

5.12.17 Address and Data Repeats Status (CPGC2_ADDRESS_DATA_STATUS)—Offset 3C28h

Current number of remaining repeats for Data and Address Repeats loops.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	0h RO/V	**Current Remaining Data Rotation Loops (Data_Select_Rotation_Repeats_Current):** Current state of Data_Select_Rotation_Repeats loop (down count).
15:6	0h RO	Reserved.
5:0	0h RO/V	**Current Remaining Address Decode Loops (Address_Decode_Rotate_Repeats_Current):** Current state of Address_Decode_Rotate_Repeats loop (down count).

5.12.18 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[0])—Offset 3C2Ch

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.12.19 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[1])—Offset 3C2Dh

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.12.20 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[2])—Offset 3C2Eh

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.12.21 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[3])—Offset 3C2Fh

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.

Bit Range	Default & Access	Field Name (ID): Description
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.12.22 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[4])—Offset 3C30h

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

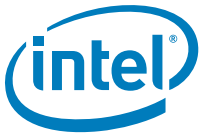
Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.12.23 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[5])—Offset 3C31h

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.



Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.12.24 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[6])—Offset 3C32h

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.12.25 Algorithm Instruction (CPGC2_ALGORITHM_INSTRUCTION[7])—Offset 3C33h

Algorithm Instruction controlling the starting Command_Instruction and data and address direction reversal.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Algorithm Instruction (Last):** If set this is the last Algorithm instruction, and the memory block is moved at its completion. Execution continues at the first Algorithm_Instruction until the test is complete. Algorithm_Instruction[7] has this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Algorithm_Instruction. Combined with the Data_Instruction Invert_Data field, and the Command_Instruction and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RW	**Inverse Direction (Inverse_Direction):** Invert the direction as set in the current Address_Instruction for the duration of this Algorithm_Instruction.

Bit Range	Default & Access	Field Name (ID): Description
4:0	0h RW	**Command Start Pointer (Command_Start_Pointer):** Starting Command_Instruction for exection of this Algorithm_Instruction. The Command_Inxtruction_Current cycles from Command_Start_Pointer, incrementing until a Command_Instruction contains the Last bit set, and then repeats for each Base_Address, Base_Repeats. Pointer to which one of the 24 command list to start with.

5.12.26 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[0])—Offset 3C34h

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgment must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset to zero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequency = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algorithm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.12.27 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[1])—Offset 3C35h

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgment must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.12.28 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[2])—Offset 3C36h

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgment must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.12.29 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[3])—Offset 3C37h

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgment must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.12.30 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[4])—Offset 3C38h

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgment must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.12.31 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[5])—Offset 3C39h

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgment must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.12.32 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[6])—Offset 3C3Ah

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgment must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.12.33 Algorithm Instruction Control (CPGC2_ALGORITHM_INSTRUCTION_CTRL[7])—Offset 3C3Bh

Control portion of each Algorithm_Instruction.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**BE Training Check Enable (BE_Train_Err_En):** Enable the BE Training Error Detection feature for individual Algorithm Instructions. This bit is inactive unless the BE_TRAIN_ERR_ENABLE bit is set in CPGC_ERR_CTL.
6	0h RW	**Select On (Select_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during chip select cycles.
5	0h RW	**Deselect On (Deselect_On):** If set, the CADB will be able to issue harassment patterns into the command and address bus during non Chip Select cycles.
4	0h RW	**Wait Event Start (Wait_Event_Start):** Wait_Event_Start causes the delay in beginning the current Algorithm_Instruction until the Event indicated by Select_Event has been acknowledged to have occurred. The Select_Event is acknowledged to be in progress. The latency between the event and the acknowledgment must be a known fixed value (preventing a hang situation). The Current_Repeat_Value is reset tzero.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Wait Count Start (Wait_Count_Start):** Wait_Count_Start and Wait_Time are used to synchronize a specific time an Algorithm should start. Wait_Time is commonly used for Pause Refresh test where the read to a particular address needs to be a specific time away from when the write to an address occurs. If Wait_Count_Start = 0 then the start of the Algorithm_Instruction is not stalled. If Wait_Count_Start = 1 then the start of the Algorithm_Instruction is stalled until the Wait_Time_Current is equal to the Wait_Time. Wait_Time_Current represent the current count value from when it was last reset either by a Test starting or Wait_Count_Clear. Wait_Time_Current is a free running counter that accurately reflects the time from when it was last reset by using the following formula. Time elapsed = Wait_Timer_Current * (1/(frequency selected by Count_Value_Frequency). If Wait_Count_Clear = 1 then prior to starting the current Algorithm_Instruction, Wait_Time_Current is reset tzero. Wait_Time_Current is frozen if a Test encounters any stop condition. Wait_Time_Current is reset to zer0 when a test starts (Start_Test is asserted). Wait_Time_Current rolls over at the maximum value back tzero. Wait_Clock_Frequency(1:0) set the frequency that increment Current_Repeat_Value. The possible frequencies that can be selected are the following. Wait_Clock_Frequency = 00 = 1GHz (time = 1ns). Wait_Clock_Frequency = 01 = 1MHZ (time = 1us). Wait_Clock_Frequency = 10 = 1KHZ (time = 1ms). Wait_Clock_Frequence = 11 = DUNIT clock.
2	0h RW	**Wait Count Clear (Wait_Count_Clear):** Reset the Wait Timer at the start of this Algorithm Instruction.
1	0h RW	**Base Range Row (Base_Range_Row):** Instead of using the Base_Repeats setting, use Base_Col_Repeats setting for the size of the block for this instruction as the size of the block. This may be used for a rapid short test hitting all banks to open pages etc, or to initialize a row worth of data.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**FastY Init (FastY_Init):** FastY_Init is used to allow a background write initialization type algorithm to use FastY with Columns as the LSB address field to ensure the fastest initialization possible. ^(wD1) is a the most typical background Init function. MEMTEL uses the keyword INIT() to reference this feature. FastY_Init enables the current Algortihm_Instruction to override the current Address_Instruction[].Address_Direction and Address_Order. If set, then use the Address_Direction=000 (FastY) and Address_Order=000 (Rank, Bank, Row/Col), else use the settings defined in the current Address_Instruction.

5.12.34 Wait Timer Current (CPGC2_ALGORITHM_WAIT_COUNT_CURRENT)—Offset 3C3Ch

Current wait timer value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW/1C/V	**Current Wait Timer (Wait_Timer_Current):** Current wait timer value. See Wait_Time description. (down count)

5.12.35 Algorithm Wait Event Control (CPGC2_ALGORITHM_WAIT_EVENT_CONTROL)—Offset 3C40h

Algorithm wait event control.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Select Event (Select_Event):** Select_Event is decoded in the following ways. Select_Event = 00 = Read/Write Pending CAS cue is empty Select_Event = 01 = CKE Power Down Select_Event = 10 = Refresh Select_Event = 11 = Self Refresh
29:26	0h RO	Reserved.
25:24	0h RW	**Wait Clock Frequency (Wait_Clock_Frequency):** 00 - 1GHz 01 - 1MHz 10 - 1KHz 11 - Native DUNIT clock
23:20	0h RW	**Select Event Hold Timer (Timer):** Exponential timer (timer value calculated as 2^Timer). If WaitEventStart is set in the currently executing Algorithm Instruction, this timer dynamically replaces the current Wait_Time counter following the Select_Event occurring (such as SelfRefresh or PowerDown), to add a fixed delay for the Select_Event condition to remain before CPGC activity resumes.
19:16	0h RO	Reserved.
15:0	0h RW	**Wait Time (Wait_Time):** Number of clocks at Wait_Clock_Frequency to wait before starting current Algorithm_Instruction if Wait_Start = 1.

5.12.36 Base Repeats (CPGC2_BASE_REPEATS)—Offset 3C44h

Base Address Loopcount.

Access Method

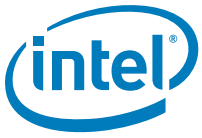
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Repeats (Base_Repeats):** Base Address Loopcount - Typically the number of Base Addresses within the Block (Row*Col*Bank*Rank) As N-1 value. This is the number of times the current Algorithm Instruction will be executed.

5.12.37 Current Base Repeats (CPGC2_BASE_REPEATS_CURRENT)—Offset 3C48h

Current Base Address Loopcount.



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current Remaining Base Loops (Base_Repeats_Current):** Current remaining Base Address loops (down count).

5.12.38 Base Column Repeats (CPGC2_BASE_COL_REPEATS)—Offset 3C4Ch

Base Address Loopcount - Alternate.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Column Repeats (Base_Col_Repeats):** Alternate Base_Address_Loopcount. Often used to initialize a Row or Column worth of data. This is used when Base_Range_Row field of ALGORITHM_INSTRUCTION_CTL is activated. This is the number of times the current Algorithm Instruction will be executed.

5.12.39 Block Repeats (CPGC2_BLOCK_REPEATS)—Offset 3C50h

Block Loopcount.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Block Repeats (Block_Repeats):** Block Loopcount. Typically the number of Blocks to be tested to traverse the entire Tested Region. (2^region_size/2^block_size -1) As N-1 value. This is the number of times the entire list of Algorithm Instructions will be executed.

5.12.40 Current Block Repeats (CPGC2_BLOCK_REPEATS_CURRENT)—Offset 3C54h

Current Block Loopcount.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current Remaining Block Loops (Block_Repeats_Current):** Current Block Loopcount (down count).

5.12.41 Command Instruction (CPGC2_COMMAND_INSTRUCTION[0])—Offset 3C58h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.42 Command Instruction (CPGC2_COMMAND_INSTRUCTION[1])—Offset 3C59h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.43 Command Instruction (CPGC2_COMMAND_INSTRUCTION[2])—Offset 3C5Ah

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.44 Command Instruction (CPGC2_COMMAND_INSTRUCTION[3])—Offset 3C5Bh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.45 Command Instruction (CPGC2_COMMAND_INSTRUCTION[4])—Offset 3C5Ch

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.46 Command Instruction (CPGC2_COMMAND_INSTRUCTION[5])—Offset 3C5Dh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.47 Command Instruction (CPGC2_COMMAND_INSTRUCTION[6])—Offset 3C5Eh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.48 Command Instruction (CPGC2_COMMAND_INSTRUCTION[7])—Offset 3C5Fh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.49 Command Instruction (CPGC2_COMMAND_INSTRUCTION[8])—Offset 3C60h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.50 Command Instruction (CPGC2_COMMAND_INSTRUCTION[9])—Offset 3C61h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.51 Command Instruction (CPGC2_COMMAND_INSTRUCTION[10])—Offset 3C62h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.52 Command Instruction (CPGC2_COMMAND_INSTRUCTION[11])—Offset 3C63h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.53 Command Instruction (CPGC2_COMMAND_INSTRUCTION[12])—Offset 3C64h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.54 Command Instruction (CPGC2_COMMAND_INSTRUCTION[13])—Offset 3C65h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.55 Command Instruction (CPGC2_COMMAND_INSTRUCTION[14])—Offset 3C66h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.56 Command Instruction (CPGC2_COMMAND_INSTRUCTION[15])—Offset 3C67h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.57 Command Instruction (CPGC2_COMMAND_INSTRUCTION[16])—Offset 3C68h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.58 Command Instruction (CPGC2_COMMAND_INSTRUCTION[17])—Offset 3C69h

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.59 Command Instruction (CPGC2_COMMAND_INSTRUCTION[18])—Offset 3C6Ah

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.60 Command Instruction (CPGC2_COMMAND_INSTRUCTION[19])—Offset 3C6Bh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.61 Command Instruction (CPGC2_COMMAND_INSTRUCTION[20])—Offset 3C6Ch

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.62 Command Instruction (CPGC2_COMMAND_INSTRUCTION[21])—Offset 3C6Dh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.63 Command Instruction (CPGC2_COMMAND_INSTRUCTION[22])—Offset 3C6Eh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.64 Command Instruction (CPGC2_COMMAND_INSTRUCTION[23])—Offset 3C6Fh

Command Instruction controlling access type, data polarity, and offset sequence selection.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Command Instruction (Last):** If set this is the last Command Instruction for this Algorithm Command Sequence.Command_Instruction[23] has this bit set implicitly. Execution continues at the Command_Instruction pointed to by the Algorithm_Instruction's Command_Start_Pointer until the end of the Algorithm_Instruction.
6	0h RW	**Invert Data (Invert_Data):** Invert the data used for this command. This is combined with the Algorithm_Instruction and Data_Instruction Invert_Data bits for Base accesses. For Offset accesses, it is further combined with the Offset_Command Invert_Data bit.
5	0h RW	**Address Decode or PRBS Enable (Address_Decode_or_PRBS_En):** Enable rotating XOR of address bits or PRBS address generation. If the Address_Decode_Enable field in the Address_Instruction list is active, and [name] is also active, then for the access of this Command_Instruction, the address will be XOR with the XOR_Address_Pattern. If the Address_Decode_Enable field in the Address_Instruction list is inactive (0), and the Address_PRBS_Enable bit in the Address_PRBS_Control register is set, then the desired address bits will be replaced with the PRBS generated value.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Base command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Command Enable (Offset):** If set, this is an Offset operation, and the selected Offset_Group will be executed in its place. In this case the Write, Hammer, and Alternate_Data fields are ignored.
1	0h RW	**Offset Group Selection (Offset_Group):** Selects which Offset_Group will be used if Offset field is set.
0	0h RW	**Write Command (Write):** A Base Write operation will be performed.

5.12.65 Hammer Repeats (CPGC2_HAMMER_REPEATS)—Offset 3C70h

Hammer Loopcount.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Hammer Repeats (Hammer_Repeats):** Hammer_Repeats is the number of times any command is repeated at the same address when the Hammer control bit is set in the Command_Instruction (if not an offset command).

5.12.66 Current Hammer Repeats (CPGC2_HAMMER_REPEATS_CURRENT)—Offset 3C74h

Current Hammer Loopcount.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current Remaining Hammer Repeats (Hammer_Repeats_Current):** Current Hammer Loopcount (down count).

5.12.67 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[0])—Offset 3C78h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.68 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[1])—Offset 3C79h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.69 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[2])—Offset 3C7Ah

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.70 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[3])—Offset 3C7Bh

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.71 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[4])—Offset 3C7Ch

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.72 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[5])—Offset 3C7Dh

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.73 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[6])—Offset 3C7Eh

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.74 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[7])—Offset 3C7Fh

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.75 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[8])—Offset 3C80h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.76 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[9])—Offset 3C81h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.77 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[10])—Offset 3C82h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.78 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[11])—Offset 3C83h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.79 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[12])—Offset 3C84h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.80 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[13])—Offset 3C85h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.81 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[14])—Offset 3C86h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.82 Offset Address Instruction (CPGC2_OFFSET_ADDRESS_INSTRUCTION[15])—Offset 3C87h

Offset Address Direction Instructions. Note that these registers are grouped as two sets of 8 Offset_Address registers and their associated set of 6 Offset_Command registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][7:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Address Instruction (Last):** Last Offset_Address_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[7] and Offset_Address_Instruction[15] have this bit set implicitly.
6	0h RW	**Stripe Enable (Stripe):** Normal Offsets use Address_Order=110. This allows full traversal of the entire Block by and offset. If Stripe is active, then there is no carry between Row and Column. This will keep the offset address within the same Row, or the same Column or on the same diagonal.
5:3	0h RW	**Address Direction (Address_Direction): Address_Direction** There are 4 basic address directions and their inverse for a total of 8. We will denote this as a combination of a 1-bit field and a 2-bit field. **(0)(00) FastY -North** Increment Column and Carry Increment into Row. **(1)(00) Inv(FastY) - South** Decrement Column and Carry Decrement into Row. **(0)(01) Diagonal North East** Increment Row and Column together and Carry Increment Column into Row. **(1)(01) Inv(Diagonal) South West** Decrement Row and Column together and Carry Decrement Column into Row. **(0)(10) FastX East** Increment Row and Carry Increment into Column. **(1)(10) Inv(FastX) - West** Decrement Row and Carry Decrement into Column. **(0)(11) Diagonal2 - South East** Decrement Column and Increment Row and Carry Increment Column into Row. **(1)(11) Inv(Diagonal2) North West** Increment Column and Decrement Row and Carry Decrement Column into Row. Offset accesses begin one 'step' in the given direction from the current Base_Address.
2	0h RW	**Periodic Data Inversion Enable (Periodic_Data_Inv_En):** Enabled periodic data inversion - based on Address_Direction (OrderX field) -normally invert every 2^Block_Size_Bits_Row/Col, modified based on Periodic_Data_Inversion_Adjustment.
1:0	0h RW	**Periodic Data Inversion Adjustment (Periodic_Data_Inv_Adj):** Reduce or increase the inversion interval by -1,0,1 based on the value in this field. 00 - no adjust 01 - interval is increased by 1 11 - interval is decreased by 1 10 - reserved

5.12.83 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[0])—Offset 3C88h

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.12.84 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[1])—Offset 3C89h

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.12.85 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[2])—Offset 3C8Ah

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.12.86 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[3])—Offset 3C8Bh

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.12.87 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[4])—Offset 3C8Ch

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.12.88 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[5])—Offset 3C8Dh

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.12.89 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[6])—Offset 3C8Eh

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.12.90 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[7])—Offset 3C8Fh

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.12.91 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[8])—Offset 3C90h

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.12.92 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[9])—Offset 3C91h

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.12.93 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[10])—Offset 3C92h

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.12.94 Offset Command Instruction (CPGC2_OFFSET_COMMAND_INSTRUCTION[11])—Offset 3C93h

Offset Command Instructions. Note that these registers are grouped as two sets of 6 Offset_Command registers and their associated set of 8 Offset_Address registers. Thus we have two Offset_Groups. Selected by Command_Instruction.Offset_Group bit. i.e. an array [1:0][5:0].

Access Method

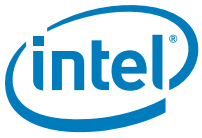
Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Last Offset Command Instruction. (Last):** Last Offset_Command_Instruction. The offset instruction is complete after all Offset_Address, Offset_Repeats, and Offset_Commands have finished. Offset_Address_Instruction[5] and Offset_Address_Instruction[11] have this bit set implicitly.
6	0h RW	**Invert Data (Invert_Data):** Invert all data for this Offset_Command_Instruction. Combine the Data_Instruction Invert_Data field, the Algorithm_Instruction Invert_Data field, Command_Instruction Invert_Data field and Offset_Command_Instruction Invert_Data field to determine the final data polarity.
5	0h RO	Reserved.
4	0h RW	**Alternate Data Select (Alternate_Data):** Use the alternate zero data source instead of the UniSequencers and Pattern_Select.
3	0h RW	**Hammer Enable (Hammer):** This Offset command will be repeated Hammer_Repeats times.
2	0h RW	**Offset Access Enable (Offset):** 1=Normal Offset Command/ Address, 0=Use Base Address and Offset_Command_Instruction Write bit.
1	0h RO	Reserved.
0	0h RW	**Write Command (Write):** A Write operation will be performed at the Offset (or Base if the Offset field = 0) Address.

5.12.95 Offset Repeats (CPGC2_OFFSET_REPEATS[0])—Offset 3C94h

Set the loopcount for Offset (Distance from Base). Selected by Command_Instruction.Offset_Group bit.



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Offset Repeats (Offset_Repeats):** Set the loopcount for Offset (Distance from Base). The entire list of Offset Commands are executed for each loop.

5.12.96 Offset Repeats (CPGC2_OFFSET_REPEATS[1])—Offset 3C98h

Set the loopcount for Offset (Distance from Base). Selected by Command_Instruction.Offset_Group bit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Offset Repeats (Offset_Repeats):** Set the loopcount for Offset (Distance from Base). The entire list of Offset Commands are executed for each loop.

5.12.97 Current Offset Repeats (CPGC2_OFFSET_REPEATS_CURRENT)—Offset 3C9Ch

Current Offset Loopcount.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current Remaining Offset Repeats (Offset_Repeats_Current):** Current Offset Loopcount (down count).

5.12.98 Region Low Row Address (CPGC2_REGION_LOW_ROW)—Offset 3CA0h

Region low row address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:0	0h RW	**Low Row (Low_Row):** Set the bottom Row for the physical memory being tested. This value is added to all Region Row Addresses computed.

5.12.99 Region Low Col Address (CPGC2_REGION_LOW_COL)—Offset 3CA4h

Region low column address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10:2	0h RW	**Low Column (Low_Col):** Set the lowest Column for the physical memory being tested. This value is added to all Region Column Addresses computed.
1:0	0h RO	Reserved.

5.12.100 Block Low Row Current (CPGC2_BLOCK_ORIGIN_ROW_CURRENT)—Offset 3CA8h

Block low row current.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:0	0h RO/V	**Current Block Origin Row (Block_Origin_Row_Current):** Current row within the testing region of memory Updated as the block traverses through the region.

5.12.101 Current Base Address Rank and Column (CPGC2_BASE_ADDRESS_COL_RANK_CURRENT)—Offset 3CACh

Current Base Address both Rank and Column.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18:16	0h RO/V	**Current Rank Base Address (Base_Rank_Current):** Current Base Address Rank within the block.
15:11	0h RO	Reserved.
10:2	0h RO/V	**Current Column Base Address (Base_Col_Current):** Current Base Address Column within the block.
1:0	0h RO	Reserved.

5.12.102 Current Base Address Bank and Row (CPGC2_BASE_ADDRESS_ROW_BANK_CURRENT)—Offset 3CB0h

Current Base Address both Bank and Row.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:24	0h RO/V	**Current Bank Base Address (Base_Bank_Current):** Current Base Address Bank within the block.
23:18	0h RO	Reserved.
17:0	0h RO/V	**Current Row Base Address (Base_Row_Current):** Current Base Address Row within the block.

5.12.103 Current Offset Address Column (CPGC2_OFFSET_ADDRESS_COL_CURRENT)—Offset 3CB4h

Current Offset Address - Column

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10:2	0h RO/V	**Current Column Offset Address (Offset_Col_Current):** Current Offset Address Column within the block. Only valid if the current Command_Instruction pointed to by Command_Instruction_Current is an Offset command.
1:0	0h RO	Reserved.

5.12.104 Current Offset Address Row (CPGC2_OFFSET_ADDRESS_ROW_CURRENT)—Offset 3CB8h

Current Offset Address - Row

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:0	0h RO/V	**Current Row Offset Address (Offset_Row_Current):** Current Offset Address Row within the block. Only valid if the current Command_Instruction pointed to by Command_Instruction_Current is an Offset command.

5.12.105 Address Size (CPGC2_ADDRESS_SIZE)—Offset 3CBCh

Set the size of the Region and Block.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:24	0h RW	**Region Row Size (Region_Size_Bits_Row):** 2^Region_Size_Bits_Row is the number of rows in the testing region. Must be >= to Block_Size_Bits_Row.
23:20	0h RW	**Region Column Size (Region_Size_Bits_Col):** 2^Region_Size_Bits_Col is the number of columns in the testing region. It is also used as the Block_Size_Bits_Col value to set the size of the block. Minimum value is 1 if Address_Decode_Enable =1, so this normally needs to be set to the number of Column bits of the memory.
19:16	0h RW	**Block Ranks Size (Block_Size_Num_Ranks):** Number of Ranks to test for a Block (as N-1 = top rank number). All Rank Addresses go through the Rank Address Lookup table.
15:12	0h RW	**Block Banks Size (Block_Size_Num_Banks):** Number of Banks to test for a Block (as N-1 = top bank number). All Bank Address values go through the Bank Address Lookup table.
11:9	0h RO	Reserved.
8:4	0h RW	**Block Row Size (Block_Size_Bits_Row):** 2^Block_Size_Bits_Row is the number of rows for a Block. If block traversal is used, then this must be at least 4 rows (=2). Minimum value is 1 if Address_Decode_Enable =1.
3:0	0h RW	**Block Column Size (Block_Size_Bits_Col):** Reserved for use as Block_Size_Bits_Col - Fixed as same as Region_Size_Bits_Col for the SoC. There is no column traversal of a block.

5.12.106 Base Address Control (CPGC2_BASE_ADDRESS_CONTROL)—Offset 3CC0h

Control handling of Base Address - inversion and increment rates and increment amounts.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26	0h RW	**Address Inversion Rate (Address_Inversion_Rate):** Address_Inversion_Rate determines if the enabled Address Fields toggle inversion on the Command Sequence Boundary (following a Command_Instruction with the Last bit set) or every Command_Instruction. 0 Invert enabled Address fields after executing the Command_Instruction with the Last bit set. 1 Invert enabled Address fields following each Command_Instruction
25:22	0h RW	**Address Inversion Enable (Address_Inversion_Enable):** Address_Inversion_Enable enables particular Address Fields to be inverted. [25] Rank_Inversion_Enable. [24] Bank_Inversion_Enable. [23] Row_Inversion_Enable. [22] Col_Inversion_Enable.
21	0h RW	**Address Increment Rate (Address_Order0_Inc_Rate):** Address_Order0_Inc_Rate determines if the Address Order 0 Field is incremented on the Command Sequence Boundary (following a Command_Instruction with the Last bit set) or every Command_Instruction. 0 Increment Address after executing the Command_Instruction with the Last bit set. 1 Increment Address following each Command_Instruction.
20:18	0h RO/V	**Rank Increment (Fixed) (Reserved_Rank_Inc):** All Base Rank addresses are incremented (or decremented) by 2^Rank_Inc (unsigned value).
17:15	0h RO/V	**Bank Increment (Fixed) (Reserved_Bank_Inc):** All Base Bank addresses are incremented (or decremented) by 2^Bank_Inc (unsigned value).
14:11	0h RW	**Column Increment (Col_Inc):** All Base and Offset Column addresses are incremented (or decremented) by 2^Col_Inc (unsigned value).

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO	Reserved.
9:6	0h RW	**Row Increment (Row_Inc):** All Base and Offset Row addresses are incremented (or decremented) by 2^Row_Inc (unsigned value).
5	0h RW	**Block Move Half Block (Block_Move_Half_Block):** if Block_Move_One_Row =1 then the Block is moved by 1 row Else if Block_Move_Half_Bock = 1 then the Block is moved by 2^(Block_Size_Bits_Row)/2 Rows Else the Block is moved by = 2^(Row_Block_Size).
4	0h RW	**Block Move One Row (Block_Move_One_Row):** See Block_Move_Half_Block for description.
3:0	0h RO	Reserved.

5.12.107 Address PRBS Control (CPGC2_ADDRESS_PRBS_CONTROL)—Offset 3CC4h

Control PRBS Address generator.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25	0h RW	**Address_PRBS_High Row map enable (Address_PRBS_High_Row):** The higher order bits of the PRBS Address Generator (bits 3 through Address_PRBS_Size-1) will be on the same Row bits when the PRBS Address is selected.
24	0h RW	**Address_PRBS_High Column map enable (Address_PRBS_High_Col):** The higher order bits of the PRBS Address Generator (bits 3 through Address_PRBS_Size-1) will be on the same Column bits when the PRBS Address is selected.
23:18	0h RO	Reserved.
17	0h RW	**Address_PRBS_Mid Row map enable (Address_PRBS_Mid_Row):** Bits [2:1] of the Row address will be bits [2:1] of the PRBS Address Generator when the PRBS Address is selected.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Address_PRBS_Mid Column map enable (Address_PRBS_Mid_Col):** Bits [2:1] of the Column address will be bits [2:1] of the PRBS Address Generator when the PRBS Address is selected.
15:10	0h RO	Reserved.
9	0h RW	**Address_PRBS_Low Row map enable (Address_PRBS_Low_Row):** LSB of Row address will be the LSB of the PRBS Address Generator when the PRBS Address is selected.
8	0h RW	**Address_PRBS_Low Column map enable (Address_PRBS_Low_Col):** LSB of Column address will be the LSB of the PRBS Address Generator when the PRBS Address is selected.
7	0h RW	**Address PRBS Enable (Address_PRBS_Enable):** If Address_PRBS_Enable is active, and Address_Decode_Enable is not active in the current Address_Instruction, then each command is enabled to use the PRBS address if the Address_Decode_or_PRBS_En bit is set.
6:4	0h RO	Reserved.
3:0	0h RW	**Address PRBS Size (Address_PRBS_Size):** Size of PRBS for address generation if Address_PRBS_Enable is active. See text for PRBS Polynomials being used for each setting.

5.12.108 Address PRBS Seed (CPGC2_ADDRESS_PRBS_SEED)—Offset 3CC8h

Seed for Address PRBS generator.

Access Method

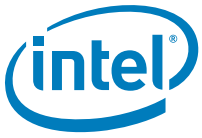
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:0	0h RW	**Address PRBS Seed (Address_PRBS_Seed):** Seed for Address PRBS generator.

5.12.109 Current Address PRBS Status (CPGC2_ADDRESS_PRBS_CURRENT)—Offset 3CCCh

Current value of Address PRBS generator.



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:0	0h RO/V	**Current Address PRBS (Address_PRBS_Current):** Current value of Address PRBS generator. Address advances as Address_Order0_Inc_Rate. The Seed is re-loaded (from Save) at each Algorithm_Instruction boundary.

5.12.110 Address PRBS Save (CPGC2_ADDRESS_PRBS_SAVE)—Offset 3CD0h

Currently saved Address PRBS seed.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:0	0h RO/V	**Address PRBS Save (Address_PRBS_Save):** Saved value of Address PRBS generator. Value is saved automatically during block advance, and restored (from Seed) when Block Traversal (Repeats) is complete.

5.12.111 Command FSM Current State (CPGC2_CMD_FSM_CURRENT)—Offset 3CD4h

Current state of Command FSM - used at stop-on-error to determine the current progress in the test at the time of the error.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:28	0h RO/V	**Address Instruction Pointer (Address_Instruction_Current):** Current Address_Instruction pointer.
27:26	0h RO	Reserved.
25:24	0h RO/V	**Data Instruction Pointer (Data_Instruction_Current):** Current Data_Instruction pointer.
23:18	0h RO	Reserved.
17:15	0h RO/V	**Algorithm Instruction Pointer (Algorithm_Instruction_Current):** Current Algorithm_Instruction pointer.
14:13	0h RO	Reserved.
12:8	0h RO/V	**Command Instruction Pointer (Command_Instruction_Current):** Current Command_Instruction pointer.
7	0h RO	Reserved.
6	0h RO/V	**Offset Group Select Pointer (Offset_Group_Instruction_Current):** Current Offset_Group as pointed to by the Current Command_Instruction (if an Offset instruction).
5:3	0h RO/V	**Offset Address Instruction Pointer (Offset_Address_Instruction_Current):** Current Offset_Address_Instruction pointer.
2:0	0h RO/V	**Offset Command Instruction Pointer (Offset_Command_Instruction_Current):** Current Offset_Command_Instruction pointer.

5.12.112 Algorithm Wait Timer Configuration (CPGC2_WAIT_2_START_CONFIG)—Offset 3CD8h

Configure the time base for the Algorithm Wait Timer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default:

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Increment value (Increment_Value):** See Prescaler field for information on this field.
27:26	0h RO	Reserved.
25:16	0h RW	**Clock Frequency (Clock_Freq):** When a setting of 1MHz or 1KHz is used in Wait_Clock_Frequency, this field provides a way to tell the hardware the native Memory Controller clock frequency, which is fed into the Prescaler automatically (with a 1 Increment_Value also automatically fed into the counter).
15:10	0h RO	Reserved.
9:0	0h RW	**Prescaler (Prescaler_for_Clock_Freq):** In order to make the 'standard' 1 GHz clock for the CPGC specified Wait_Clock_Frequency setting, we need to provide a pre-scaler, and Increment Value to modify the existing Wait_Timer_Current advancement. This field will divide the native Memory Controller clock by the provided value, with '1' being 'No Divide'. After that divide, the Wait_Timer_Current will advance by the 'Increment_Value' field. In this way, we are creating a clock ratio able to 'multiply' the native Memory Controller clock by 'Increment_Value/Prescaler'. For small values of Wait_Time, the error will be substantial, and it may be better to modify the programming to the '11' Native Clock setting and manually compute the required Wait_Time for the desired delay.

5.12.113 VISA Mux Selection (CPGC2_VISA_MUX_SEL)—Offset 3CDCh

Selection for VISA mux controls.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:13	0h RW	**Error Group 1 (Err1_grp_Sel):** Err Group 1 Select.
12:11	0h RW	**Error Group 0 (Err0_grp_Sel):** Err Group 0 Select.
10:9	0h RW	**DPAT Group 1 (Dpat1_grp_Sel):** Dpat Group 1 Select.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW	**DPAT Group 0 (Dpat0_grp_Sel):** Dpat Group 0 Select.
6:5	0h RW	**Command Group 1 (Cmd1_grp_Sel):** Cmd Group 1 Select.
4:3	0h RW	**Command Group 0 (Cmd0_grp_Sel):** Cmd Group 0 Select.
2	0h RW	**Error-Command (Err1_or_Cmd1):** Err group 1 or Cmd group 1 select.
1	0h RW	**Command-DPAT (Cmd0_or_Dpat1):** Cmd group 0 or Dpat group 1 select.
0	0h RW	**DPAT-Error (Dpat0_or_Err0):** Dpat group 0 or Err group 0 select.

5.12.114 Loopback Sequencer Configuration (CPGC_LB_SEQ_CFG)—Offset 3CE0h

Loopback Sequencer Config.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Start Test Delay (START_TEST_DELAY):** Start_Test_Delay is the delay period (in byte clocks) to execute a test(i.e transition to Loopback.Pattern) after the link is in Loopback.Idle and Local_Start_Test is asserted. If Local_Start_Test is set upon the initial enttry to Loopback.Idle then a test (entry to Loopback.Pattern) will immediately start after Start_Test_Delay number of byte clocks is enforced. During Start_Test_test the Valid must not be asserted (i.e Loopback.PM) and no comparison of data will be taking place. Start_Test_Delay=0 is reserved and not allowed. Start_Test_Delay=1 will result in a 1byte clock delay. Start_Test_Delay=2 will result in a 2byte clock delay.
23:21	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20:16	0h RW	**Loopcount (LOOPCOUNT):** 2^(Loopcount) determines the length of a test. One Loopcount consists of Pattern_Length followed by PM_Length. Pattern_Length corresponds to the Loopback Master generating patterns and the Loopback. Slave and/or Loopback Master performing error checking occurring (valid is asserted). PM_Length corresponds to the functional power savings mode (valid is not asserted). Loopcount=0 means the test is infinite. Loopcount=1 means the test will end after two loops. Loopcount=2 means the test will end after four loops. Loopcount=3 means the test will end after eight loops.
15:8	0h RW	**PM Length (PM_LENGTH):** PM_Length(i.e Loopback.PM) forms the second half of the loopcount sequence with Pattern_Length (i.e Loopback.Pattern)forming the first half. PM_Length is used in conjunction with Pattern_Length and Loopcount to go in and out of Power Savings Modes in an identical way to how the functional power saving mode behave. This includes post amble, pre-amble, etc. PM_Length duration is defined in total # of byte clocks. If PM_Length is set to 0 then no power saving modes will be entered. If the end of the test has not been reached, (Current_Loopcount!=Loopcount) the loopcount is incremented and the sequence repeats (Pattern_Length followed by PM_Length). If the end of the test has not been reached (Current_Loopcount=Loopcount) the link transitions back to Loopback.Idle following the PM state.
7:0	0h RW	**Pattern Length (PATTERN_LENGTH):** Pattern_Length (i.e Loopback.Pattern) forms the first half of the Loopcount sequence with PM_Length (i.e Loopback.PM) forming the second half. Pattern_Length is the portion of Loopcount when patterns are generated (Loopback Master) and compared (Loopback Master and optionally the Loopback Slave). Pattern_Length duration is defined in total # of byte clocks. A zero value is illegal. The Sum of Pattern_Length and PM_Length (Duration of a Loopcount) must always be set to a value of two or more.

5.12.115 Loopback Sequencer Control (CPGC_LB_SEQ_CTL)—Offset 3CE4h

Loopback sequencer control.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:12	0h RW	**Initialization Mode (INITIALIZATION_MODE):** A change to Initialization_Mode occurs immediately. 00 - OFF - REUT is clock gated. 01 - LSM Mode - Enter Loopback.Idle state through the appropriate Link Layer bits as a Loopback Master or Loopback Slave. 10 - Force Master - Force entry to Loopback.Idle as a Loopback Master (Supported if Force_Loopback capability is set). 11 - Force Slave - Force entry to Loopback.Idle as Loopback Slave (Supported if Force_Loopback capability is set). Note: A user must be careful to transition both sides of the Link to Loopback.Idle if switching Initialization_Mode from Force Master or Force Slave to LSM Mode or undefined behavior can be expected. Note: Initialization Mode should not be changed while Local_Start_Test is set, or while Test_In_Progress is set.
11:7	0h RO	Reserved.
6	0h RW	**Bind Stop on Error (BIND_STOP_ON_ERROR):** Test will stop based on Global_Error (external input) and Local_Error will drive Global_Error.
5	0h RW	**Bind Clear Errors (BIND_CLEAR_ERRORS):** Local_Clear_Errors will clear all other REUT instances that have this bit set.
4	0h RW	**Bind Stop Test (BIND_STOP_TEST):** Local_Stop_Test will stop all other REUT instances that have this bit set.
3	0h RW	**Bind Start Test (BIND_START_TEST):** Local_Start_Test will start all other REUT instances that have this bit set.
2	0h RW/V	**Local Clear Errors (LOCAL_CLEAR_ERRORS):** Setting Local_Clear_Errors to 1 will immediately clear all local Error registers (i.e. CPGC_ERR_* registers). Local_Clear_Errors will immediately clear to 0 after clearing affected registers. If this bit fails to auto-clear, then there is no clock and the clear will occur at the start of the next test.
1	0h RW/V	**Local Stop Test (LOCAL_STOP_TEST):** If Local_Stop_Test is set to 1 and a Loopback test is in progress (i.e. Test_In_Progress=1) then a transition to Loopback. Idle will occur as soon as possible (i.e. Link enters Loopback.PM). Local_Stop_Test will immediately clear to 0 after stopping a Loopback test (i.e. Local_Stop_Test=0 while in Loopback.Idle).

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Local Start Test (LOCAL_START_TEST):** If Local_Start_Test is set a Sequence will immediately start, or wait until entry to Loopback state. A complete Sequence is defined by the following behavior: 1) An initial delay of Start_Test_Delay byte clocks must first occur in Loopback.PM (with Valid de-asserted). 2) Transition to Loopback.Pattern (Valid asserted) for a duration of Pattern_Length Byte clocks during which data is generated and compared by the Loopback Master and optionally compared by the Loopback Slave. 3) Increment Loopcounter. 4) Optionally Transition to Loopback.PM (with Valid de-asserted), if so programmed, for a duration of PM_Length Byte clocks during which power modes are functionally enforced as what would happen normally based on the length of the PM_Length duration. 5) If Current Loopcount !=2^Loopcount then go to step 2. 6) If Current Loopcount !=2^Loopcount then the Link returns to Loopback.Idle, Local_Start_Test is cleared for the Master. Local_Start_Test is not cleared on the Loopback.Slave.

5.12.116 Loopback Loopcount Tx Status (CPGC_LB_SEQ_LOOPCOUNT_TX_STATUS)—Offset 3CE8h

Indicates the current TX Loopcount value in the Sequence.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current Loopcount (CURRENT_LOOPCOUNT):** Current_Loopcount indicates how many times the full Sequence has been executed in the TX path. Current_Loopcount is cleared by Local_Clear_Errors.

5.12.117 Loopback Loopcount Rx Status (CPGC_LB_SEQ_LOOPCOUNT_RX_STATUS)—Offset 3CECh

Indicates the current RX Loopcount value in the Sequence.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current Loopcount (CURRENT_LOOPCOUNT):** Current_Loopcount indicates how many times the full Sequence has been executed in the RX path. Current_Loopcount is cleared by Local_Clear_Errors.

5.12.118 Pattern Length Status (CPGC_LB_SEQ_PL_RX_STATUS)—Offset 3CF0h

Indicates how many Bytes are left in Loopback.Pattern.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RO/V	**Current Pattern Length (CURRENT_PATTERN_LENGTH):** Current_Pattern_Length is used in conjunction with Stop_On_Error_Control conditons to determine where the last failure occurred within Loopback.Pattern. Current_Pattern_Length indicates how many Bytes were left in Loopback. Pattern when the error occurred. Current_Pattern_Length is cleared by Local_Clear_Errors.

5.12.119 Refresh Control (CPGC_MISC_REFRESH_CTL)—Offset 3CF4h

CPGC MISC REFRESH CTL

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Panic Refresh Only (PANIC_REFRESH_ONLY):** Reserved
30:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Start Test on RefZQ (REFZQ_EN_START_TEST_SYNC):** Reserved
7:4	0h RO	Reserved.
3:0	0h RW	**Rank Mask of Refresh (REFRESH_RANK_MASK):** Reserved

5.12.120 ZQ Control (CPGC_MISC_ZQ_CTL)—Offset 3CF8h

CPGC MISC ZQ CTL

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Always do ZQ (ALWAYS_DO_ZQ):** Reserved
30:2	0h RO	Reserved.
1:0	0h RW	**Rank Mask of ZQ (ZQ_RANK_MASK):** Reserved

5.12.121 ODT Control (CPGC_MISC_ODT_CTL)—Offset 3CFCh

CPGC MISC ODT CTL

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**DDR Training MPR Pattern (MPR_Train_DDR_On):** Reserved
30:18	0h RO	Reserved.
17:16	0h RW	**Rank ODT On (ODT_ON):** Reserved
15:2	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Rank ODT Override (ODT_OVERRIDE):** Reserved

5.12.122 CKE Control (CPGC_MISC_CKE_CTL)—Offset 3D00h

CPGC MISC CKE CTL

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:16	0h RW	**Rank CKE On (CKE_ON):** Reserved
15:9	0h RO	Reserved.
8	0h RW	**Start Test on CKE (CKE_EN_START_TEST_SYNC):** Reserved
7:2	0h RO	Reserved.
1:0	0h RW	**Rank CKE Override (CKE_OVERRIDE):** Reserved

5.12.123 Command Rate (CPGC_MISC_CMD_RATE)—Offset 3D04h

CPGC CMD_RATE

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 100Ah

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**MRW uses 2 clocks CS (init_mrw_2n_cs):** Reserved
30:14	0h RO	Reserved.
13:12	1h RW	**CK to CKE delay (ck_to_cke_delay):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RW	**Reset Delay (reset_delay):** Reserved
7:4	0h RW	**Reset On Command (reset_on_command):** Reserved
3:1	5h RW	**Command Rate Limit (cmd_rate_limit):** Reserved
0	0h RW	**Enable Command Rate Limit (enable_cmd_rate_limit):** Reserved

5.12.124 External Trigger Control (CPGC_MISC_EXT_TRIGGER)—Offset 3D08h

CPGC MISC EXT TRIGGER

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RW	**Trigger Out on Test Done (TRIGGER_OUT_ON_TEST_DONE):** Reserved
2	0h RW	**Trigger Out on Error (TRIGGER_OUT_ON_ERROR):** Reserved
1	0h RW	**Trigger Out on Start (TRIGGER_OUT_GLOBAL_START):** Reserved
0	0h RW	**Trigger in to Start (TRIGGER_IN_GLOBAL_START):** Reserved

5.12.125 Sequence Control (CPGC_SEQ_CTL)—Offset 3D0Ch

Sequence Control Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	0h RW/V	**Continue Single Step (CONTINUE_SINGLE_MODE):** When in Single_Command_Mode setting this bit will enable a new command to be issued. This bit immediately clears after being set.
8	0h RW	**Single Step/Cmd Mode (SINGLE_CMD_MODE):** Enter Single Command mode were we will issue one command from CPGC and then pause command issuing. This may be resumed by setting Continue_Single_Mode, or normal continuous operation resumed by clearing this bit.
7:3	0h RO	Reserved.
2	0h RW/V	**Clear Errors (CLEAR_ERRORS):** Setting this bit will immediately clear all error registers and error status. This bit will automatically self clear.
1	0h RW/V	**Stop Test (STOP_TEST):** Forces an exit from the tests running on this engine/channel. Note that this will also cause a test stop for all engines with GLB_STOP_BIND set. This bit will self clear.
0	0h RW/V	**Start Test (START_TEST):** Used to initiate a transition to active mode on this engine/channel (note that INIT_MODE has to be programmed first). Note that this will also cause a test start for all engines with GLB_START_BIND set. This bit will self clear.

5.12.126 Sequence Configuration A (CPGC_SEQ_CFG_A)—Offset 3D10h

Sequence Configuration Low Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 200000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22	0h RW	**Request Data Size (REQUEST_DATA_SIZE):** Size of requests CPGC is issuing, 64B and 32B transactions and is encoded as follows: 0 - 32 Byte Transactions 1 - 64 Byte Transactions

Bit Range	Default & Access	Field Name (ID): Description
21	1h RW	**CPGC Control (CPGC_CONTROL):** Used to indicate the OPIO(MCDRAM) or CPGC(DDR) mode. 1 - CPGC Mode. 0 - OPIO Mode.
20:15	0h RO	Reserved.
14:12	0h RW	**Initialization Mode (INITIALIZATION_MODE):** 000 - IDLE MODE 001 - ACTIVE MODE 010 - DIRECT MODE 011 - ACTIVE MODE 100 - MRS MODE 101 - ERROR DUMP MODE (Reserved) 110 - WDB FILL MODE (Reserved) 111 - REWIND MODE (Reserved)
11	0h RW	**Bind Stop Test (GLOBAL_STOP_BIND):** Setting this bit will bind this channel engine to all other channel engines. A test stop (both forced and due to a stop condition) for any channel engine with GLOBAL_STOP_BIND set will cause the same action to occur on all engines with GLOBAL_STOP_BIND set. This feature is usually used when synchronization between multiple engines/ channels necessitates a global control of all supported engines. Note: this field is only available if multiple channels/engines are supported for the current implementation, otherwise it is reserved.
10	0h RW	**Bind Start Test (GLOBAL_START_BIND):** Setting this bit will bind this channel engine to all other channel engines. A test start for any channel with GLOBAL_START_BIND set will cause the same action to occur on all engines with GLOBAL_START_BIND set. This feature is usually used when synchronization between multiple engines/channels necessitates a global control of all supported engines. Note: this field is only available if multiple channels/engines are supported for the current implementation, otherwise it is reserved.
9	0h RW	**Bind Stop-on-Error (GLOBAL_STOP_ON_ERR_BIND):** Setting this bit will bind this channel engine to all other channel engines. A test stop (due to an error condition) for any channel with GLOBAL_STOP_ON_ERR_BIND set will cause the same action to occur on all engines with GLOBAL_STOP_ON_ERR_BIND set. This feature is usually used when synchronization between multiple engines/channels necessitates a global control of all supported engines. Note: this field is only available if multiple channels/engines are supported for the current implementation, otherwise it is reserved.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Bind Clear Errors (GLOBAL_CLEAR_ERR_BIND):** Setting this bit will bind this channel engine to all other channel engines. Clearing all error registers and error status for any channel with GLOBAL_CLEAR_ERR_BIND set will cause the same action to occur on all engines with GLOBAL_CLEAR_ERR_BIND set. This feature is usually used when synchronization between multiple engines/channels necessitates a global control of all supported engines. Note: this field is only available if multiple channels/engines are supported for the current implementation, otherwise it is reserved.
7	0h RO	Reserved.
6	0h RW	**Constant Write Strobe (ENABLE_CONSTANT_WRITE_STROBE):** Reserved
5:0	0h RO	Reserved.

5.12.127 Sequence Configuration B (CPGC_SEQ_CFG_B)—Offset 3D14h

Sequence Config High.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW	**Start Delay (START_DELAY):** Number of clock cycles (in CPGC-S clock domain) the start of the test is delayed by after START_TEST has been asserted by the user. This is usually used to synchronize multiple SoC CPGC engines on multiple channels according to a defined phase relationship.

5.12.128 Sequence Status (CPGC_SEQ_STATUS)—Offset 3D18h

Sequence Test Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Test Done (TEST_DONE):** This bit will be set when the test is complete (or has been forced to exit due to a stop condition). Bit is cleared on a reset or when user starts another test.
30	0h RO/V	**Test Busy (TEST_BUSY):** This bit will be set when once a test has started. Bit is cleared on a reset or once test is done (or has been forced to exit due a stop condition).
29	0h RO/V	**Algorithm Done (ALGO_DONE):** This bit will be set when all the algorithms are complete. It is cleared on a reset.
28	0h RO/V	**Single Step/Cmd Paused (SINGLE_MODE_PAUSED):** This bit will be set when a command has been issued and we are paused due to Single_Command_Mode. The test may be continued by either clearing Single_Command_Mode or by setting Continue_Single_Mode.
27:0	0h RO	Reserved.

5.12.129 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[0])—Offset 3D20h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.130 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[1])—Offset 3D24h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.131 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[2])—Offset 3D28h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.132 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[3])—Offset 3D2Ch

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.133 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[4])—Offset 3D30h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.134 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[5])—Offset 3D34h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.135 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[6])—Offset 3D38h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.136 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[7])—Offset 3D3Ch

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.137 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[8])—Offset 3D40h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.138 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[9])—Offset 3D44h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.139 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[10])—Offset 3D48h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.140 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[11])—Offset 3D4Ch

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.141 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[12])—Offset 3D50h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.142 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[13])—Offset 3D54h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.143 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[14])—Offset 3D58h

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.144 Raster Repository Content (CPGC2_RASTER_REPO_CONTENT[15])—Offset 3D5Ch

Flat register read access to Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Content of Raster Repository (Content):** Flat register read access to Raster Repository. The format of this is 2 consecutive addresses contain a complete 64-bit data chunk error bit-map, or one Error_Summary entry. In Mode3, there are up to 4 Row addresses for read failures for the associated Bank, based on the indicators in RASTER_REPO_CONTENT_ECC*.

5.12.145 Mode3 Fail Status LSB (CPGC2_RASTER_REPO_CONTENT_ECC1)—Offset 3D60h

Lower half of the Raster Repository Mode3 Fail Status.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO/V/P	**ECC Chunk 3 (ECC_chunk3):** ECC chunk 3 raster when in Mode 1.
27:26	0h RO/V/P	**Bank3 Fail Count (fail_count3):** Bank 3 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.
25	0h RO/V/P	**Bank3 Any Fail (fail_any3):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
24	0h RO/V/P	**Bank3 Excessive Fail (fail_excess3):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.
23:20	0h RO/V/P	**ECC Chunk 2 (ECC_chunk2):** ECC chunk 2 raster when in Mode 1.
19:18	0h RO/V/P	**Bank2 Fail Count (fail_count2):** Bank 2 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.
17	0h RO/V/P	**Bank2 Any Fail (fail_any2):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
16	0h RO/V/P	**Bank2 Excessive Fail (fail_excess2):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.
15:12	0h RO/V/P	**ECC Chunk 1 (ECC_chunk1):** ECC chunk 1 raster when in Mode 1.
11:10	0h RO/V/P	**Bank1 Fail Count (fail_count1):** Bank 1 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO/V/P	**Bank1 Any Fail (fail_any1):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
8	0h RO/V/P	**Bank1 Excessive Fail (fail_excess1):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.
7:4	0h RO/V/P	**ECC Chunk 0 (ECC_chunk0):** ECC chunk 0 raster when in Mode 1.
3:2	0h RO/V/P	**Bank0 Fail Count (fail_count0):** Bank 0 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.
1	0h RO/V/P	**Bank0 Any Fail (fail_any0):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
0	0h RO/V/P	**Bank0 Excessive Fail (fail_excess0):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.

5.12.146 Mode3 Fail Status MSB (CPGC2_RASTER_REPO_CONTENT_ECC2)—Offset 3D64h

Upper half of the Raster Repository Mode3 Fail Status.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO/V/P	**ECC Chunk 7 (ECC_chunk7):** ECC chunk 7 raster when in Mode 1.
27:26	0h RO/V/P	**Bank7 Fail Count (fail_count7):** Bank 7 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.
25	0h RO/V/P	**Bank7 Any Fail (fail_any7):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
24	0h RO/V/P	**Bank7 Excessive Fail (fail_excess7):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.
23:20	0h RO/V/P	**ECC Chunk 6 (ECC_chunk6):** ECC chunk 6 raster when in Mode 1.
19:18	0h RO/V/P	**Bank6 Fail Count (fail_count6):** Bank 6 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO/V/P	**Bank6 Any Fail (fail_any6):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
16	0h RO/V/P	**Bank6 Excessive Fail (fail_excess6):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.
15:12	0h RO/V/P	**ECC Chunk 5 (ECC_chunk5):** ECC chunk 5 raster when in Mode 1.
11:10	0h RO/V/P	**Bank5 Fail Count (fail_count5):** Bank 5 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.
9	0h RO/V/P	**Bank5 Any Fail (fail_any5):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
8	0h RO/V/P	**Bank5 Excessive Fail (fail_excess5):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.
7:4	0h RO/V/P	**ECC Chunk 4 (ECC_chunk4):** ECC chunk 4 raster when in Mode 1.
3:2	0h RO/V/P	**Bank4 Fail Count (fail_count4):** Bank 4 Number of failing address. 0=none or 1, 1=2, 2=3, and 3=4 entries.
1	0h RO/V/P	**Bank4 Any Fail (fail_any4):** 0 - indicates no failing address, 1 - indicates 1 or more failing address in the corresponding Content entry.
0	0h RO/V/P	**Bank4 Excessive Fail (fail_excess4):** 0 indicates no more than fail_max failing addresses, 1 - indicates more than fail_max failing addresses.

5.12.147 Read Command Count (CPGC2_READ_COMMAND_COUNT_CURRENT)—Offset 3D68h

Current count of reads.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Current Read Command Count (Read_Command_Count_Current):** Current count of reads - freezes on stop_on_error conditions at the number of reads including the error that caused the stop.

5.12.148 Mask Errors on First N Reads (CPGC2_MASK_ERRS_FIRST_N_READS)—Offset 3D6Ch

Masking for the first N read operations - all errors are ignored.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/P	**Mask First N Reads (Mask_First_N_Reads):** 0=no masking, N= number of reads that will not result in any error indication for the raster repository.

5.12.149 Raster Repository Status (CPGC2_RASTER_REPO_STATUS)—Offset 3D70h

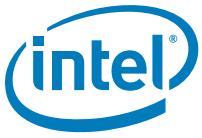
Raster repository status.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Raster Repository Clear (RasterRepoClear):** Reset the raster repo entries. This bit auto-clears.
30	0h RW/P	**Stop on Raster Full (StopOnRaster):** If Raster Mode 1, test will stop after loading the bitmap into the raster. If Raster Mode 2, test will stop after loading 8 errors in the raster.
29:18	0h RO	Reserved.
17:16	0h RW/P	**Raster Repository Mode (RasterRepoMode):** 00 Mode 1 BitMap Mode. 01 Mode 2 Summary Mode. 10 mode 3 Filtered Failed Row Mode.
15:12	0h RO	Reserved.
11:10	0h RW/P	**Excess Failure Maximum (FailMax):** Maximum number of failing address before an additional failing address will set fail_excess for any bank. 00 one failure, 01 - two failures, 10 - three failures, 11- four failures.



Bit Range	Default & Access	Field Name (ID): Description
9	0h RO/V/P	**Summary Any Fail (FailAnyAll):** 0 - indicates no failing addresses. 1 - indicates 1 or more failing addresses.
8	0h RO/V/P	**Summary Excessive Fail (FailExcessAll):** 0 - indicates less than or exactly max_fail failing addresses on all banks. 1 - indicates at least one bank's errors exceed the max_fail limit.
7	0h RO	Reserved.
6:4	0h RO/V/P	**Number of Summary Entries (NumErrLogged):** Indicates the current number of errors loaded in the raster repo in Mode 2. Max value is 8.
3	0h RO	Reserved.
2	0h RO/V/P	**Raster Repository Full (RasterRepoFull):** Indicates when the no. of errors logged exceed max value of 8.
1	0h RO/V/P	**Summary Valid (SummaryValid):** Indicates when the summary information of the erroneous bitmap is loaded in the current summary buffer. This information consist of Algorithmic data, Physical Addr (Rank, Bank,Row,Col) and 8 2-bit error summary for every chunk.
0	0h RO/V/P	**Bitmap valid (BitmapValid):** Indicates when Mode 1 erroneous bitmap data is loaded in the raster repo.

5.12.150 Error Summary A (CPGC2_ERR_SUMMARY_A)—Offset 3D74h

Most recent error sumary data, not yet written to the Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V/P	**Algorithm Summary (Algorithm_Summary):** Algorithm_Summary - currently formatted as: [2:0] Offset_Command_Instruction_Current. [5:3] Offset_Address_Instruction_Current. [10:6] Command_Instruction_Current. [13:11] Algorithm_Instruction_Current. [15:14] Data_Instruction_Current.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V/P	**Error Summary (Error_Summary):** Error_Summary - formatted as a pair of adjacent bits for each chunk, 00=no error in that chunk, 01=one error in that chunk, 10=two errors in that chunk, 11=three or more errors in that chunk.

5.12.151 Error Summary B (CPGC2_ERR_SUMMARY_B)—Offset 3D78h

Most recent error summary data, not yet written to the Raster Repository.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO/V/P	**Physical Address (Physical_Address_Summary):** Error_Summary - Physical Address encoded as: [7:0] Column, [25:8] Row, [28:26] Bank, [29] Rank.
1:0	0h RO/V/P	**Algorithm Summary (Algorithm_Summary):** Algorithm_Summary - currently formated as: [1:0] Address_Instruction_Current.

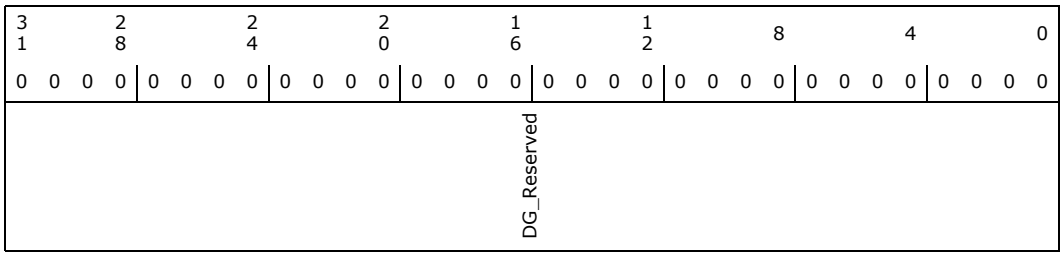
5.12.152 Future use Reserved (CPGC2_ERR_SUMMARY_C)—Offset 3D7Ch

Reserved for expansion of Error_Summary.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Future use Reserved (DG_Reserved):** Reserved for expansion of Error_Summary (bits 7:0).

5.12.153 Data Pattern Generation Buffer Control (CPGC_DPAT_BUF_CTL)—Offset 3D80h

Data Pattern Buffer Control Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:24	0h RO/V	**Read Buffer Pointer (RD_BUF_PTR):** Pointer to current entry in the data pattern buffers used for generating the read data.
23:20	0h RO/V	**Write Buffer Pointer (WR_BUF_PTR):** Pointer to current entry in the data pattern buffers used for generating the write data.
19	0h RO	Reserved.
18:16	0h RW	**Buffer End Pointer (BUF_END_PNTR):** Pointer to last data pattern buffer entry before wrapping back to BUF_STRT_PTR if incrementing is enabled through being different from BUF_STRT_PTR. Note: The actual size of this field depends on the # of lines supported for data generation. i.e If 1 or 2 lines are supported then it is a 1 bit field, if 8 lines are supported then 3 bits are available. Currently the RTL uses internal CPGC buffers so it has 4 lines and requires 2 bits.
15:11	0h RO	Reserved.
10:8	0h RW	**Buffer Start Pointer (BUF_STRT_PNTR):** Pointer to first buffer entry. Also used as the only entry if BUF_INC_EN is not enabled. Note: The actual size of this field depends on the # of lines supported for data generation (DATA_PAT_DEPTH_CAP), i.e If 1 or 2 lines are supported then it is a 1 bit field, if 16 lines are supported then the whole 4 bits are available. Currently the RTL uses internal CPGC buffers so it has 8 lines and requires 3 bits.
7	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Buffer Pointer Increment Scale (BUF_PNTR_INC_SCALE):** If set, the buffer pointer will be incremented at a linear rate given by BUF_PTR_INC_RATE, otherwise the buffer pointer will be incremented at an exponential rate given by BUF_PTR_INC_RATE. 1=Buffer Pointer Increment Rate field is treated as a linear number. 0=Buffer Pointer Increment Rate field is treated is an exponential number.
5:0	0h RW	**Buffer Pointer Increment Rate (BUF_PNTR_INC_RATE):** 0: Each buffer entry will be used for 2^BUF_PTR_INC_RATE number of bursts (64Bytes). 1: Each buffer entry will be used for BUF_PTR_INC_RATE + 1 number of 8-UI -- before incrementing the buffer pointer by 1. Note: To disable Buffer Pointer increments, set BUF_END_PTR==BUF_STRT_PTR.

5.12.154 Data Pattern Generation Configuration (CPGC_DPAT_CFG)—Offset 3D84h

Data Pattern Configuration Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28:24	0h RW	**Reload LFSR Seed Rate (RELOAD_LFSR_SEED_RATE):** Reload_LFSR_Seed_Rate only exists if the LFSR_Save_Restore capability is set to 1. Reload_LFSR_Seed_Rate and Save_LFSR_Seed_Rate is most often used in conjunction with Lane_Rotate_Rate where the user desires to replay the same deterministic LFSR stress as the victim aggressor patterns shifts Lanes left. When the victim aggressor pattern returns to the starting position the current LFSR stress is saved using Save_LFSR_Seed_Rate to allow the LFSR stress to advance for the new period. 2^(Reload_LFSR_Seed_Rate-1) defines the periodic Loopcount interval that the current LFSR Seed UNISEQ#_RDSTAT.Uniseq_RdStat is reloaded from CPGC_UNISEQ#_RDSAVE.Pattern_Buffer. When the Save_LFSR_Seed_Rate and Reload_LFSR_Seed_Rate is reached in the same Bit only the saving of the LFSR seed takes place. Examples: 0=Disable - The current LFSR seed is never reloaded. 1=The current LFSR seed is reloaded every Loopcount. 2=The current LFSR seed is reloaded every other Loopcount. 3=The current LFSR seed is reloaded every fourth Loopcount.
23:16	0h RW	**Save LFSR Seed Rate (SAVE_LFSR_SEED_RATE):** Save_LFSR_Seed_Rate only exists if the LFSR_Save_Restore capability is set to 1. See Reload_LFSR_Seed_Rate for use model. UNISEQ#_RDSAVE.Pattern_Buffer is initially loaded at the start of a test with UNISEQ#_RDSTAT.Uniseq_RdStat (the Seed). 2^(Reload_LFSR_Seed_Rate-1) * (Save_LFSR_Seed_Rate) defines the periodic Loopcount interval that the current LFSR Seed is saved into UNISEQ#_RDSAVE.Pattern_Buffer. When the Save_LFSR_Seed_Rate and Reload_LFSR_Seed_Rate is reached in the same Loopcount only the saving of the LFSR seed takes place. Examples: 0=Disable - The current LFSR seed (UNISEQ#_RDSTAT.Uniseq_RdStat) is saved only at the start of test into UNISEQ#_RDSAVE.Pattern_Buffer. 1=Illegal (Would save every Reload and effectively disable both Save and Reload). 2=The current LFSR seed is saved every other 2^(Reload_LFSR_Seed_Rate-1) Loopcounts. 3=The current LFSR seed is saved every third Reload (and Reload does not happen).

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Reserved for future use (ECC_DATA_SOURCE_SEL):** Indicates whether byte 0 (Dq0-Dq7) or byte 7 (dq56-dq63) is transmitted and compared for the ECC byte. 0=byte group 0 will be transmitted and compared for the ECC byte. 1=byte group 7 will be transmitted and compared for the ECC byte. Hardware directs if ECC is included within Generation and Checking. This bit may be reserved if ECC is not supported, or if this functionality is controlled from a different register.
14	0h RW	**Reserved for future use (ECC_REPLACE_BYTE_CONTROL):** ECC_Replace_Byte_Control is used by the Read data path to mux the received ECC byte into the same byte group indicated by ECC_Data_Source_Sel. This is needed to capture ECC cacheline errors into the WDB when Enable_WDB_Error_Capture is set to 1. This bit may be reserved if ECC is not supported, or if this functionality is controlled from a different register.
13	0h RW	**ECC Disable (ECC_DISABLE):** Setting this bit will internally disable all related ECC features in CPGC having the effect of generating all '1 in the ECC CPGC interface outputs, and of Binding to '0 all the ECC interface CPGC inputs. ECC masks and error comparisons will be disabled as well. If ECC is supported, but not directly passed to CPGC, then this bit when set will enable the ECC_REPLACE_BYTE_CONTROL and ECC_DATA_SOURCE_SEL functionality, to allow driving of ECC from another Byte Lane, and replacing the incoming data with ECC for that Byte Lane. When ECC is disabled with this bit, then the output of CPGC will be determined based on BE_TRAIN_ERR_EN and may output all 1's or the content of the DRAMDM and XDRAMDM registers as Byte-Enables.
12:10	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Read Address As Data (READ_ADDRESS_AS_DATA):** When Read_Address_as_Data is set to '1' any address fields that the CADB is overriding during a Select cycle should be used for comparing the incoming data. Otherwise, the functional path decoded address field should be used for comparing the incoming data. This override of the data will not respect any inversion, rotation or other data modification. It will only be active (override the normal output/reference) when Alternate_Data is active in either the Command_Instruction or the Offset_Command_Instruction as appropriate . The functional path decoded address field used for read comparison is repeated in chunk and should follow the Data Construction rules described below on what bytegroup relates to what decoded address: Chunk0 - Byte0 =Column(7:0). Chunk0 - Byte1 =Column(9:8) <- as many Column bits as supported. Chunk0 - Byte2 =Row(0:7). Chunk0 - Byte3 =Row(15:8). Chunk0 - Byte4 =Row(17:16)<- as many Row bits as supported. Chunk0 - Byte5 =Bank(3:0) [Note: Bank Group may be part of this field] <- as many Bank bits as supported. Chunk0 - Byte6 =Rank(1:0) <- as many Rank bits as supported (would be CS# if CADB output supported). Chunk0 - Byte7 =Reserved (set to 0).
8	0h RW	**Write Address As Data (WRITE_ADDRESS_AS_DATA):** When Write_Address_as_Data is set to '1', any address fields that the CADB is overriding during a Select cycle should be used for generating the write data. Otherwise, the functional path decoded address field should be used for generating the write data. Data Construction rules follow the same as for READ_ADDRESS_AS_DATA. This format is subject to change based on memory technology supported and other reasons. What is to be guaranteed is that every Cache line of data will be unique to each address.
7:6	0h RW	**Unisequencer 2 Mode (UNISEQ2_MODE):** Defines the operational mode for unified sequence 2 as follows: 00 - LMN Mode. 01 - Pattern Buffer Mode. 10 - LFSR Mode. 11 - Reserved for future use.
5	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RW	**Unisequencer 1 Mode (UNISEQ1_MODE):** Defines the operational mode for unified sequence 1 as follows: 00 - LMN Mode. 01 - Pattern Buffer Mode. 10 - LFSR Mode. 11 - Reserved for future use.
2	0h RO	Reserved.
1:0	0h RW	**Unisequencer 0 Mode (UNISEQ0_MODE):** Defines the operational mode for unified sequence 0 as follows: 00 - LMN Mode. 01 - Pattern Buffer Mode. 10 - LFSR Mode. 11 - Reserved for future use.

5.12.155 LFSR Configuration and Lane Rotate (CPGC_DPAT_XTRA_LFSR_CFG)—Offset 3D88h

Unisequencer LFSR configuration and Lane Rotation.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	0h RW	**Lane Rotate Rate (LANE_ROTATE_RATE):** Lane_Rotate_Rate only exists if the Lane_Rotation_Support capability exists. 2^(Lane_Rotate_Rate-1) indicates the periodic Loopcount rate when the EXTBUF_# registers are rotated up by one bit. Lane_Rotate_Rate=0 disables all rotation. Lane_Rotate_Rate=1 causes the EXTBUF_# registers to be rotated every one Loopcount. Lane_Rotate_Rate=2 causes the EXTBUF_# registers to be rotated every other Loopcount. Etc.. When the EXTBUF_# registers are rotated Bit 0 shifts to Bit 1 all the way up to the Max-1 Bit and the Max bit shifts to Bit0.
23	0h RW	**Unisequencer 2 LFSR Stagger Enable (UNISEQ2_LFSR_STAGGER):** 0=No Stagger, 1=Stagger. This bit must not be set unless Uniseq2_Mode is programmed to Select LFSR or the behavior is undefined.
22:21	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20:18	0h RW	**Unisequencer 2 LFSR Polynomial Select (UNISEQ2_LFSR_POLYNOMIAL_SIZE):** Possible Polynomial Sizes: 0x0=Use 8 bit LFSR (x8 + x6 + x5 + x4) 0x1=Use 15 bit LFSR (x15 + x14) 0x2=Use 31 bit LFSR (x31 + x28) 0x3=Use 23 bit LFSR (x23 + x18) 0x4=Use 7 bit LFSR (x7 + x6) 0x5=Use 16 bit LFSR (x16+x5+x4+x3) 0x6=Use 23 bit LFSR (x23+x21+x18+x15+x7+x2) 0x7=Use 32 bit LFSR (x32+x31+x30+x10)
17:16	0h RO	Reserved.
15	0h RW	**Unisequencer 1 LFSR Stagger Enable (UNISEQ1_LFSR_STAGGER):** 0=No Stagger, 1=Stagger. This bit must not be set unless Uniseq1_Mode is programmed to Select LFSR or the behavior is undefined.
14:13	0h RO	Reserved.
12:10	0h RW	**Unisequencer 1 LFSR Polynomial Select (UNISEQ1_LFSR_POLYNOMIAL_SIZE):** Possible Polynomial Sizes: 0x0=Use 8 bit LFSR (x8 + x6 + x5 + x4) 0x1=Use 15 bit LFSR (x15 + x14) 0x2=Use 31 bit LFSR (x31 + x28) 0x3=Use 23 bit LFSR (x23 + x18) 0x4=Use 7 bit LFSR (x7 + x6) 0x5=Use 16 bit LFSR (x16+x5+x4+x3) 0x6=Use 23 bit LFSR (x23+x21+x18+x15+x7+x2) 0x7=Use 32 bit LFSR (x32+x31+x30+x10)
9:8	0h RO	Reserved.
7	0h RW	**Unisequencer 0 LFSR Stagger Enable (UNISEQ0_LFSR_STAGGER):** 0=No Stagger, 1=Stagger. This bit must not be set unless Uniseq0_Mode is programmed to Select LFSR or the behavior is undefined.
6:5	0h RO	Reserved.
4:2	0h RW	**Unisequencer 0 LFSR Polynomial Select (UNISEQ0_LFSR_POLYNOMIAL_SIZE):** Possible Polynomial Sizes: 0x0=Use 8 bit LFSR (x8 + x6 + x5 + x4) 0x1=Use 15 bit LFSR (x15 + x14) 0x2=Use 31 bit LFSR (x31 + x28) 0x3=Use 23 bit LFSR (x23 + x18) 0x4=Use 7 bit LFSR (x7 + x6) 0x5=Use 16 bit LFSR (x16+x5+x4+x3) 0x6=Use 23 bit LFSR (x23+x21+x18+x15+x7+x2) 0x7=Use 32 bit LFSR (x32+x31+x30+x10)

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	Reserved.

5.12.156 Unisequencer Data Pattern Buffer (CPGC_DPAT_UNISEQ[0])—Offset 3D8Ch

Data Pattern Unified Sequencer 0 Seed Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AA55AA55h

Bit Range	Default & Access	Field Name (ID): Description
31:0	AA55AA55h RW	**Pattern Buffer (PATTERN_BUFFER):** If UniSeq#_Mode is set to Pattern Buffer mode, then this field represents the initial content of the rotating pattern buffer for the unified sequencer. If UniSeq#_Mode is set to LFSR mode, then this field represents the 32-bit LFSR seed for the unified sequencer. Note: This is a shared register, it has a meaning according to the UniSeq# mode. **For PRBS lengths less than or equal to 8, the seed must contain 16 bits of the initial PRBS sequence.**

5.12.157 Unisequencer Data Pattern Buffer (CPGC_DPAT_UNISEQ[1])—Offset 3D90h

Data Pattern Unified Sequencer 0 Seed Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AA55AA55h

Bit Range	Default & Access	Field Name (ID): Description
31:0	AA55AA55h RW	**Pattern Buffer (PATTERN_BUFFER):** If UniSeq#_Mode is set to Pattern Buffer mode, then this field represents the initial content of the rotating pattern buffer for the unified sequencer. If UniSeq#_Mode is set to LFSR mode, then this field represents the 32-bit LFSR seed for the unified sequencer. Note: This is a shared register, it has a meaning according to the UniSeq# mode. **For PRBS lengths less than or equal to 8, the seed must contain 16 bits of the initial PRBS sequence.**

5.12.158 Unisequencer Data Pattern Buffer (CPGC_DPAT_UNISEQ[2])—Offset 3D94h

Data Pattern Unified Sequencer 0 Seed Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AA55AA55h

Bit Range	Default & Access	Field Name (ID): Description
31:0	AA55AA55h RW	**Pattern Buffer (PATTERN_BUFFER):** If UniSeq#_Mode is set to Pattern Buffer mode, then this field represents the initial content of the rotating pattern buffer for the unified sequencer. If UniSeq#_Mode is set to LFSR mode, then this field represents the 32-bit LFSR seed for the unified sequencer. Note: This is a shared register, it has a meaning according to the UniSeq# mode. **For PRBS lengths less than or equal to 8, the seed must contain 16 bits of the initial PRBS sequence.**

5.12.159 Unisequencer LMN Control (CPGC_DPAT_UNISEQ_LMN[0])—Offset 3D98h

Data Pattern Unified Sequencer 0 LMN Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	1h RW	**N Count (N_CNT):** N_Count only exists if LMN_Support capability is set to 1. After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).

Bit Range	Default & Access	Field Name (ID): Description
23:16	1h RW	**M Count (M_CNT):** M_Count only exists if LMN_Support capability is set to 1. After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
15:8	1h RW	**L Count (L_CNT):** If LMN_Support capability is set to 0 then: A periodic square wave is generated that has the following behavior. 1) Drive L_Polarity for L_Count Bits. 2) Drive inverse of L_Polarity for L_Count Bits. 3) Go to step 1. Else if LMN_Support is set to 1 then: After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency is set to 1. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
7:4	0h RW	**L Count High-bits (L_COUNTER_HI):** Additional 4 bits to increase the size of L Count up to 12.
3	0h RO	Reserved.
2	0h RW	**L Counter Mode Enable (L_COUNT_EN):** Used in concatenation with FREQ_SWEEP_EN to enable 3 possible modes of LMN behavior.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Frequence Sweep Mode Enable (FREQ_SWEEP_EN):** Used in concatenation with L_COUNT_EN to enable 3 possible modes of LMN behavior: {L_COUNT_EN,FREQ_SWEEP_EN} {0,0} - Normal LMN. {0,1} - Sweep clock pattern from 2*M period down to 2*N_Count period and repeat. {1,0} - L-Counter - drive clock pattern of 2*L period. {1,1} - Currently same as L-Counter mode - reserved for future use. If Normal LMN mode, then the following pattern is continuously repeated: 1) Drive L_Count bits with the polarity set by L_Polarity. 2) Drive M_Count bits with the inverse of L_Polarity. 3) Drive N_Count bits with the value of L_Polarity. 4) Go to step 2. If any L_Count, M_Count, or N_Count=0 then the state will freeze at the polarity driven for that stage. If Sweep mode, then the following pattern is continuously repeated: 1) Drive L_Count bits with the polarity set by L_Polarity. 2) X_count=M_Count 3) Drive X_Count bits with the inverse of L_Polarity. 4) Drive X_Count bits with the value of L_Polarity. 5) Drive X_Count bits with the inverse of L_Polarity. 6) If X_Count==N_Count then go to step 9. 7) X_Count=X_Count-1 8) Go to step 10. 9) X_Count=M_Count 10) Drive X_Count bits with the value of L_Polarity. 11) Go to step 3. If LCount mode, then the following pattern is continuously repeated: 1) Drive L_Polarity for L_Count Bits. 2) Drive inverse of L_Polarity for L_Count Bits. 3) Go to step 1. If {0,1}, L_Count, M_Count, and N_Count must never be programmed to 0 and is considered undefined. If {1,0}, L_Count must never be programmed to 0 and is considered undefined. If {0,1}, M_Count and N_Count must be greater than or equal to 8 or behavior may be implementation specific. If {0,1}, N_Count must be programmed less than M_Count.
0	0h RW	**Initial Output (L_SEL):** The initial logic output of the sequencer is defined as follows: 0 - Output Logic '0' for L_CNT UIs. 1 - Output Logic '1' for L_CNT UIs.

5.12.160 Unisequencer LMN Control (CPGC_DPAT_UNISEQ_LMN[1])—Offset 3D9Ch

Data Pattern Unified Sequencer 0 LMN Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	1h RW	**N Count (N_CNT):** N_Count only exists if LMN_Support capability is set to 1. After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
23:16	1h RW	**M Count (M_CNT):** M_Count only exists if LMN_Support capability is set to 1. After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
15:8	1h RW	**L Count (L_CNT):** If LMN_Support capability is set to 0 then: A periodic square wave is generated that has the following behavior. 1) Drive L_Polarity for L_Count Bits. 2) Drive inverse of L_Polarity for L_Count Bits. 3) Go to step 1. Else if LMN_Support is set to 1 then: After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency is set to 1. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
7:4	0h RW	**L Count High-bits (L_COUNTER_HI):** Additional 4 bits to increase the size of L Count up to 12.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	Reserved.
2	0h RW	**L Counter Mode Enable (L_COUNT_EN):** Used in concatenation with FREQ_SWEEP_EN to enable 3 possible modes of LMN behavior.
1	0h RW	**Frequency Sweep Mode Enable (FREQ_SWEEP_EN):** Used in concatenation with L_COUNT_EN to enable 3 possible modes of LMN behavior: {L_COUNT_EN,FREQ_SWEEP_EN} {0,0} - Normal LMN. {0,1} - Sweep clock pattern from 2*M period down to 2*N_Count period and repeat. {1,0} - L-Counter - drive clock pattern of 2*L period. {1,1} - Currently same as L-Counter mode - reserved for future use. If Normal LMN mode, then the following pattern is continuously repeated: 1) Drive L_Count bits with the polarity set by L_Polarity. 2) Drive M_Count bits with the inverse of L_Polarity. 3) Drive N_Count bits with the value of L_Polarity. 4) Go to step 2. If any L_Count, M_Count, or N_Count=0 then the state will freeze at the polarity driven for that stage. If Sweep mode, then the following pattern is continuously repeated: 1) Drive L_Count bits with the polarity set by L_Polarity. 2) X_count=M_Count 3) Drive X_Count bits with the inverse of L_Polarity. 4) Drive X_Count bits with the value of L_Polarity. 5) Drive X_Count bits with the inverse of L_Polarity. 6) If X_Count==N_Count then go to step 9. 7) X_Count=X_Count-1 8) Go to step 10. 9) X_Count=M_Count 10) Drive X_Count bits with the value of L_Polarity. 11) Go to step 3. If LCount mode, then the following pattern is continuously repeated: 1) Drive L_Polarity for L_Count Bits. 2) Drive inverse of L_Polarity for L_Count Bits. 3) Go to step 1. If {0,1}, L_Count, M_Count, and N_Count must never be programmed to 0 and is considered undefined. If {1,0}, L_Count must never be programmed to 0 and is considered undefined. If {0,1}, M_Count and N_Count must be greater than or equal to 8 or behavior may be implementation specific. If {0,1}, N_Count must be programmed less than M_Count.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Initial Output (L_SEL):** The initial logic output of the sequencer is defined as follows: 0 - Output Logic '0' for L_CNT UIs. 1 - Output Logic '1' for L_CNT UIs.

5.12.161 Unisequencer LMN Control (CPGC_DPAT_UNISEQ_LMN[2])—Offset 3DA0h

Data Pattern Unified Sequencer 0 LMN Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	1h RW	**N Count (N_CNT):** N_Count only exists if LMN_Support capability is set to 1. After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
23:16	1h RW	**M Count (M_CNT):** M_Count only exists if LMN_Support capability is set to 1. After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).

Bit Range	Default & Access	Field Name (ID): Description
15:8	1h RW	**L Count (L_CNT):** If LMN_Support capability is set to 0 then: A periodic square wave is generated that has the following behavior. 1) Drive L_Polarity for L_Count Bits. 2) Drive inverse of L_Polarity for L_Count Bits. 3) Go to step 1. Else if LMN_Support is set to 1 then: After L_Count bits are driven at the beginning of a test then periodic pattern is continuously repeated depending on the value of Enable_Sweep_Frequency is set to 1. If Enable_Sweep_Frequency=0 then a steady state frequency is driven (see Enable_Sweep_Frequency for exact behavior). If Enable_Sweep_Frequency=1 then a frequency sweep is continuously generated ranging from 2*(M) to 2*(N) driven (see Enable_Sweep_Frequency for exact behavior).
7:4	0h RW	**L Count High-bits (L_COUNTER_HI):** Additional 4 bits to increase the size of L Count up to 12.
3	0h RO	Reserved.
2	0h RW	**L Counter Mode Enable (L_COUNT_EN):** Used in concatenation with FREQ_SWEEP_EN to enable 3 possible modes of LMN behavior.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Frequency Sweep Mode Enable (FREQ_SWEEP_EN):** Used in concatenation with L_COUNT_EN to enable 3 possible modes of LMN behavior: {L_COUNT_EN,FREQ_SWEEP_EN} {0,0} - Normal LMN. {0,1} - Sweep clock pattern from 2*M period down to 2*N_Count period and repeat. {1,0} - L-Counter - drive clock pattern of 2*L period. {1,1} - Currently same as L-Counter mode - reserved for future use. If Normal LMN mode, then the following pattern is continuously repeated: 1) Drive L_Count bits with the polarity set by L_Polarity. 2) Drive M_Count bits with the inverse of L_Polarity. 3) Drive N_Count bits with the value of L_Polarity. 4) Go to step 2. If any L_Count, M_Count, or N_Count=0 then the state will freeze at the polarity driven for that stage. If Sweep mode, then the following pattern is continuously repeated: 1) Drive L_Count bits with the polarity set by L_Polarity. 2) X_count=M_Count 3) Drive X_Count bits with the inverse of L_Polarity. 4) Drive X_Count bits with the value of L_Polarity. 5) Drive X_Count bits with the inverse of L_Polarity. 6) If X_Count==N_Count then go to step 9. 7) X_Count=X_Count-1 8) Go to step 10. 9) X_Count=M_Count 10) Drive X_Count bits with the value of L_Polarity. 11) Go to step 3. If LCount mode, then the following pattern is continuously repeated: 1) Drive L_Polarity for L_Count Bits. 2) Drive inverse of L_Polarity for L_Count Bits. 3) Go to step 1. If {0,1}, L_Count, M_Count, and N_Count must never be programmed to 0 and is considered undefined. If {1,0}, L_Count must never be programmed to 0 and is considered undefined. If {0,1}, M_Count and N_Count must be greater than or equal to 8 or behavior may be implementation specific. If {0,1}, N_Count must be programmed less than M_Count.
0	0h RW	**Initial Output (L_SEL):** The initial logic output of the sequencer is defined as follows: 0 - Output Logic '0' for L_CNT UIs. 1 - Output Logic '1' for L_CNT UIs.

5.12.162 Invert and DC Control (CPGC_DPAT_INVDCCTL)—Offset 3DA4h

Data Pattern Inversion/DC Control Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AA0000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Mask Rotate Enable (MASK_ROTATE_EN):** If set, the inversion/DC mask will rotate to the left at a rate defined by the MASK_ROTATE_RATE field.
30	0h RW	**DC Mask Mode Enable (DC_OR_INV):** Selects between using the inversion/DC mask for inversion or DC as follows: 0 - Mask used for inversion. 1 - Mask used for driving a DC signal of polarity DC_POL.
29	0h RW	**DC Polarity (DC_POL):** Selects the polarity of the signal to be driven through the inversion/DC mask if DC_OR_INV is set to 1: 0 - Drive a logic low (zero). 1 - Drive a logic high (one).
28:25	0h RO	Reserved.
24:16	AAh RW	**Byte Group Mapping (BYTEGROUP_MAPPING):** Select between the two bytes of unique lanes being generated by the DPAT pattern generator, to be applied in each DQ byte group, as many byte groups as required by the number of DQ pins. MSB is always for the ECC byte group, used only if ECC is present.
15:12	0h RO	Reserved.
11:8	0h RW	**Mask Rotate Rate (MASK_ROTATE_RATE):** If inversion mask rotation is enabled through MASK_ROTATE_EN, the mask will rotate to the left every time 2^MASK_ROTATE_RATE bursts (64Bytes) have been have been issued.
7:0	0h RW	**ECC ByteGroup Invert/DC Enable (ECC_INV_DC_MASK):** A value of for any of the bits means the corresponding ECC lane(s) will be inverted or a DC value driven on it. Note that this field is used to load bits [71:64] of the continuous shift register composed of this field along with DATA_INV_DC_MASK_HI and DATA_INV_DC_MASK_LO. Note: this field is only available if ECC is supported for the current implementation, otherwise it is reserved.

5.12.163 Data Invert/DC Enable Low (CPGC_DPAT_INV_DC_MASK_LO)—Offset 3DA8h

Low Data Pattern Inversion/DC Mask Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data Invert/DC Enable Low (DATA_INV_DC_MASK_LO):** A value of '1' for any of the bits means the corresponding data lane(s) will be inverted or a DC value driven on it. Note that this field is used to load bits [31:0] of the continuous shift register composed of this field along with ECC_INV_DC_MASK and DATA_INV_DC_MASK_HI. DPAT generator only uses the appropriate bits based on the widest bus that this CPGC block is designed to support. This register is also used to provide the Initial value for the Alternate Data pattern generator.

5.12.164 Data Invert/DC Enable High (CPGC_DPAT_INV_DC_MASK_HI)—Offset 3DACh

High Data Pattern Inversion/DC Mask Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data Invert/DC Enable High (DATA_INV_DC_MASK_HI):** A value of '1' for any of the bits means the corresponding data lane(s) will be inverted or a DC value driven on it. Note that this field is used to load bits [63:32] of the continuous shift register composed of this field along with ECC_INV_DC_MASK and DATA_INV_DC_MASK_LO.

5.12.165 Byte Enable Mask Lower (CPGC_DPAT_DRAMDM)—Offset 3DB0h

Data Pattern DRAM Data Mask Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**Byte Enable Mask Lower (DATA_MASK_LO):** A byte enable field with each bit corresponding to a data byte sent during a burst such that: 0 - Mask the Corresponding Byte. 1 - No Mask to the Corresponding Byte. The byte-to-bit mapping is given by Byte[n] -> bit[n]. This register is for the first half cacheline of data. It is only used when ECC is not present or is disabled.

5.12.166 Byte Enable Mask Upper (CPGC_DPAT_XDRAMDM)—Offset 3DB4h

Extended Data Pattern DRAM Data Mask Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**Byte Enable Mask Upper (DATA_MASK_HI):** A byte enable field with each bit corresponding to a data byte sent during a burst such that: 0 - Mask the Corresponding Byte. 1 - No Mask to the Corresponding Byte. The byte-to-bit mapping is given by Byte[n+32] -> bit[n]. This register is for the Second half cacheline of data. It is only used when ECC is not present or is disabled.

5.12.167 Unisequencer Status - Write (CPGC_DPAT_UNISEQ_WRSTAT[0])—Offset 3DB8h

Write Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Status (UNISEQ_WRSTAT):** The current contents of the Pattern/LFSR buffer in write generation domain.

5.12.168 Unisequencer Status - Write (CPGC_DPAT_UNISEQ_WRSTAT[1])—Offset 3DBCh

Write Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Status (UNISEQ_WRSTAT):** The current contents of the Pattern/LFSR buffer in write generation domain.

5.12.169 Unisequencer Status - Write (CPGC_DPAT_UNISEQ_WRSTAT[2])—Offset 3DC0h

Write Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Status (UNISEQ_WRSTAT):** The current contents of the Pattern/LFSR buffer in write generation domain.

5.12.170 Unisequencer Status - Read (CPGC_DPAT_UNISEQ_RDSTAT[0])—Offset 3DC4h

Read Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Status (UNISEQ_RDSTAT):** Reflects the current and final status of the pattern buffer in the read domain. If PATBUF mode, then Pattern_Buffer is used as a fixed buffer that is output in serial fashion. After all the bits in the Pattern_Buffer have been transmitted the pattern will simply repeat itself continuously while a Loopback Test is in progress. If LFSR mode, then Pattern_Buffer is used as a seed to a fixed LFSR that is output in serial fashion. Over time the LFSR pattern will repeat itself continuously while a Loopback Test is in progress. In LFSR Mode the contents of Pattern_Buffer will interact with the LFSR in the following ways: If LFSR_Save_Restore is set then CPGC_REG_DPAT_UNISEQ_WRSAVE.Pattern_Buffer will interact with CPGC_UNISEQ#_RDSTAT in the following ways: 1) CPGC_UNISEQ#_RDSTAT will be periodically saved into CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Save_LFSR_Seed_Rate (see Save_LFSR_Seed_Rate for more details). 2) CPGC_UNISEQ#_RDSTAT will be periodically reloaded with CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Reload_LFSR_Seed_Rate (see Reload_LFSR_Seed_Rate for more details).

5.12.171 Unisequencer Status - Read (CPGC_DPAT_UNISEQ_RDSTAT[1])—Offset 3DC8h

Read Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Status (UNISEQ_RDSTAT):** Reflects the current and final status of the pattern buffer in the read domain. If PATBUF mode, then Pattern_Buffer is used as a fixed buffer that is output in serial fashion. After all the bits in the Pattern_Buffer have been transmitted the pattern will simply repeat itself continuously while a Loopback Test is in progress. If LFSR mode, then Pattern_Buffer is used as a seed to a fixed LFSR that is output in serial fashion. Over time the LFSR pattern will repeat itself continuously while a Loopback Test is in progress. In LFSR Mode the contents of Pattern_Buffer will interact with the LFSR in the following ways: If LFSR_Save_Restore is set then CPGC_REG_DPAT_UNISEQ_WRSAVE.Pattern_Buffer will interact with CPGC_UNISEQ#_RDSTAT in the following ways: 1) CPGC_UNISEQ#_RDSTAT will be periodically saved into CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Save_LFSR_Seed_Rate (see Save_LFSR_Seed_Rate for more details). 2) CPGC_UNISEQ#_RDSTAT will be periodically reloaded with CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Reload_LFSR_Seed_Rate (see Reload_LFSR_Seed_Rate for more details).

5.12.172 Unisequencer Status - Read (CPGC_DPAT_UNISEQ_RDSTAT[2])—Offset 3DCCh

Read Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Status (UNISEQ_RDSTAT):** Reflects the current and final status of the pattern buffer in the read domain. If PATBUF mode, then Pattern_Buffer is used as a fixed buffer that is output in serial fashion. After all the bits in the Pattern_Buffer have been transmitted the pattern will simply repeat itself continuously while a Loopback Test is in progress. If LFSR mode, then Pattern_Buffer is used as a seed to a fixed LFSR that is output in serial fashion. Over time the LFSR pattern will repeat itself continuously while a Loopback Test is in progress. In LFSR Mode the contents of Pattern_Buffer will interact with the LFSR in the following ways: If LFSR_Save_Restore is set then CPGC_REG_DPAT_UNISEQ_WRSAVE.Pattern_Buffer will interact with CPGC_UNISEQ#_RDSTAT in the following ways: 1) CPGC_UNISEQ#_RDSTAT will be periodically saved into CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Save_LFSR_Seed_Rate (see Save_LFSR_Seed_Rate for more details). 2) CPGC_UNISEQ#_RDSTAT will be periodically reloaded with CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Reload_LFSR_Seed_Rate (see Reload_LFSR_Seed_Rate for more details).

5.12.173 LMN Status - Write (CPGC_DPAT_LMN_WRSTAT[0])—Offset 3DD0h

Write LMN Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Status (LMN_WRSTAT):** The current contents of the LMN buffer in write comparison domain.

5.12.174 LMN Status - Write (CPGC_DPAT_LMN_WRSTAT[1])—Offset 3DD4h

Write LMN Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Status (LMN_WRSTAT):** The current contents of the LMN buffer in write comparison domain.

5.12.175 LMN Status - Write (CPGC_DPAT_LMN_WRSTAT[2])—Offset 3DD8h

Write LMN Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Status (LMN_WRSTAT):** The current contents of the LMN buffer in write comparison domain.

5.12.176 LMN Status - Read (CPGC_DPAT_LMN_RDSTAT[0])—Offset 3DDCh

Read LMN Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Status (LMN_RDSTAT):** The current contents of the LMN buffer in read comparison domain.

5.12.177 LMN Status - Read (CPGC_DPAT_LMN_RDSTAT[1])—Offset 3DE0h

Read LMN Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Status (LMN_RDSTAT):** The current contents of the LMN buffer in read comparison domain.

5.12.178 LMN Status - Read (CPGC_DPAT_LMN_RDSTAT[2])—Offset 3DE4h

Read LMN Status Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Status (LMN_RDSTAT):** The current contents of the LMN buffer in read comparison domain.

5.12.179 Unisequencer Save Status - Write (CPGC_DPAT_UNISEQ_WRSAVE[0])—Offset 3DE8h

Write PRBS Save Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Save Status (PATTERN_BUFFER):** The current contents of the Save register before the test stops in the write domain.

5.12.180 Unisequencer Save Status - Write (CPGC_DPAT_UNISEQ_WRSAVE[1])—Offset 3DECh

Write PRBS Save Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Save Status (PATTERN_BUFFER):** The current contents of the Save register before the test stops in the write domain.

5.12.181 Unisequencer Save Status - Write (CPGC_DPAT_UNISEQ_WRSAVE[2])—Offset 3DF0h

Write PRBS Save Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEADBEEFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	DEADBEEFh RO/V	**Save Status (PATTERN_BUFFER):** The current contents of the Save register before the test stops in the write domain.

5.12.182 Unisequencer Save Status - Read (CPGC_DPAT_UNISEQ_RDSAVE[0])—Offset 3DF4h

Read PRBS Save Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Save Status (PATTERN_BUFFER):** CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer will reflect either the initial or last saved value of CPGC_UNISEQ#_RDSTAT. If PATBUF mode, then Pattern_Buffer is used as a fixed buffer that is output in serial fashion. After all the bits in the Pattern_Buffer have been transmitted the pattern will simply repeat itself continuously while a Loopback Test is in progress. If LFSR mode, then Pattern_Buffer is used as a seed to a fixed LFSR that is output in serial fashion. Over time the LFSR pattern will repeat itself continuously while a Loopback Test is in progress. In LFSR Mode the contents of Pattern_Buffer will interact with the LFSR in the following ways: If LFSR_Save_Restore is set then CPGC_REG_DPAT_UNISEQ_WRSAVE.Pattern_Buffer will interact with CPGC_UNISEQ#_RDSTAT in the following ways: 1) CPGC_UNISEQ#_RDSTAT will be periodically saved into CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Save_LFSR_Seed_Rate (see Save_LFSR_Seed_Rate for more details). 2) CPGC_UNISEQ#_RDSTAT will be periodically reloaded with CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Reload_LFSR_Seed_Rate (see Reload_LFSR_Seed_Rate for more details).

5.12.183 Unisequencer Save Status - Read (CPGC_DPAT_UNISEQ_RDSAVE[1])—Offset 3DF8h

Read PRBS Save Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Save Status (PATTERN_BUFFER):** CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer will reflect either the initial or last saved value of CPGC_UNISEQ#_RDSTAT. If PATBUF mode, then Pattern_Buffer is used as a fixed buffer that is output in serial fashion. After all the bits in the Pattern_Buffer have been transmitted the pattern will simply repeat itself continuously while a Loopback Test is in progress. If LFSR mode, then Pattern_Buffer is used as a seed to a fixed LFSR that is output in serial fashion. Over time the LFSR pattern will repeat itself continuously while a Loopback Test is in progress. In LFSR Mode the contents of Pattern_Buffer will interact with the LFSR in the following ways: If LFSR_Save_Restore is set then CPGC_REG_DPAT_UNISEQ_WRSAVE.Pattern_Buffer will interact with CPGC_UNISEQ#_RDSTAT in the following ways: 1) CPGC_UNISEQ#_RDSTAT will be periodically saved into CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Save_LFSR_Seed_Rate (see Save_LFSR_Seed_Rate for more details). 2) CPGC_UNISEQ#_RDSTAT will be periodically reloaded with CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Reload_LFSR_Seed_Rate (see Reload_LFSR_Seed_Rate for more details).

5.12.184 Unisequencer Save Status - Read (CPGC_DPAT_UNISEQ_RDSAVE[2])—Offset 3DFCh

Read PRBS Save Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Save Status (PATTERN_BUFFER):** CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer will reflect either the initial or last saved value of CPGC_UNISEQ#_RDSTAT. If PATBUF mode, then Pattern_Buffer is used as a fixed buffer that is output in serial fashion. After all the bits in the Pattern_Buffer have been transmitted the pattern will simply repeat itself continuously while a Loopback Test is in progress. If LFSR mode, then Pattern_Buffer is used as a seed to a fixed LFSR that is output in serial fashion. Over time the LFSR pattern will repeat itself continuously while a Loopback Test is in progress. In LFSR Mode the contents of Pattern_Buffer will interact with the LFSR in the following ways: If LFSR_Save_Restore is set then CPGC_REG_DPAT_UNISEQ_WRSAVE.Pattern_Buffer will interact with CPGC_UNISEQ#_RDSTAT in the following ways: 1) CPGC_UNISEQ#_RDSTAT will be periodically saved into CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Save_LFSR_Seed_Rate (see Save_LFSR_Seed_Rate for more details). 2) CPGC_UNISEQ#_RDSTAT will be periodically reloaded with CPGC_REG_DPAT_UNISEQ#_RDSAVE.Pattern_Buffer based on Reload_LFSR_Seed_Rate (see Reload_LFSR_Seed_Rate for more details).

5.12.185 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[0])—Offset 3E00h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.

Bit Range	Default & Access	Field Name (ID): Description
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.186 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[1])—Offset 3E04h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

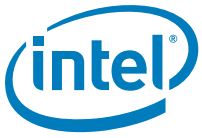
Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.187 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[2])—Offset 3E08h

DPAT Pattern Select Buffer.

Access Method



Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.188 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[3])—Offset 3E0Ch

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.

Bit Range	Default & Access	Field Name (ID): Description
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.189 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[4])—Offset 3E10h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

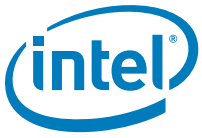
Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.190 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[5])—Offset 3E14h

DPAT Pattern Select Buffer.

Access Method



Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.191 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[6])—Offset 3E18h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.

Bit Range	Default & Access	Field Name (ID): Description
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.192 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[7])—Offset 3E1Ch

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

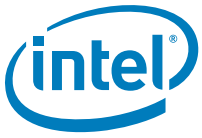
Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.193 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[8])—Offset 3E20h

DPAT Pattern Select Buffer.

Access Method



Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.194 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[9])—Offset 3E24h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.

Bit Range	Default & Access	Field Name (ID): Description
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.195 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[10])—Offset 3E28h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.196 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[11])—Offset 3E2Ch

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.197 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[12])—Offset 3E30h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.

Bit Range	Default & Access	Field Name (ID): Description
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.198 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[13])—Offset 3E34h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.199 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[14])—Offset 3E38h

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.200 Extended Pattern Buffer (CPGC_DPAT_EXTBUF[15])—Offset 3E3Ch

DPAT Pattern Select Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: AAAAAAAAh

Bit Range	Default & Access	Field Name (ID): Description
31:24	AAh RW	**Data Line 3 (DATA_LINE3):** Contents of Pattern Buffer for Cache Line 3. EXTBUF[0] corresponds to Lane 0 (32 UI of data maximum). EXTBUF[1] corresponds to Lane 1 (32 UI of data maximum). ..... EXTBUF[15] corresponds to Lane 15. These 16 lanes are replicated across the number of active DQ lanes on the memory interface.

Bit Range	Default & Access	Field Name (ID): Description
23:16	AAh RW	**Data Line 2 (DATA_LINE2):** Contents of Pattern Buffer for Cache Line 2. Line 2 (and same for Lines 3..0) refers to the 8-UI partial cache line as pointed to current status at CPGC_DPAT_BUF_CTL. This advancement is controlled by CPGC_DPAT_BUF_CTL.
15:8	AAh RW	**Data Line 1 (DATA_LINE1):** Contents of Pattern Buffer for Cache Line 1.
7:0	AAh RW	**Data Line 0 (DATA_LINE0):** Contents of Pattern Buffer for Cache Line 0.

5.12.201 Error Checker Control (CPGC_ERR_CTL)—Offset 3E40h

Control for Error Checker.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/P	**Cache Line Error Check Enable (ERRCHK_MASK_CACHELINE):** Defines a periodic burst mask that repeats every 64Bytes of data as follows: Bit 0 - Burst 0 Bit 1 - Burst 1 ... Bit 7 - Burst 7 Only bursts with a corresponding bit value of '1' will be checked for errors. A burst is defined as a burst length of 64 bytes of data. In Loopback each bit of this register controls the check of each ByteTime (8-bits) on the bus.
23:16	0h RW/P	**Chunk Error Check Enable (ERRCHK_MASK_CHUNK):** Defines which chunk within the burst of data (i.e. bit within a burst of 8-bits for each lane) to check for errors. Only chunks with a corresponding bit value of '0' will be checked for errors. This field is only used for full width (64bit) DQ busses. Otherwise the upper 32 bits of the Lane Mask is used as the Chunk Enable. This field is also used for Loopback mode for all DQ sizes.
15:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW/P	**Stop On Error Control (STOP_ON_ERROR_CTL):** Defines test stop conditions based on error checking as follows: 00 - Never stop: Prevents any error from stopping the test. 01 - Stop On Nth Error: Stop once STOP_ERR_CNTR has accumulated at least (STOP_ON_N + 1) errors. 10 - Stop On All Byte Groups Error: Stop if every byte group indicates that at least one of its lanes accumulated at least one error. That is, if all bits BYTEGRP_ERR_STAT, (and ECC_GRP_ERR_STAT if supported), are all set. 11 - Stop On All Lanes Error: Stop if every lane within every byte group has accumulated at least one error. That is, if all bits in LANE_ERR_STAT_LO, LANE_ERR_STAT_HI, (and LANE_ERR_STATECC if supported) are all set.
11:9	0h RO	Reserved.
8	0h RW/P	**BE Training Enable (BE_TRAIN_ERR_EN):** Enable BE Training Error Detection Feature. Note this bit overrides the BE_TRAIN_ERR_EN bit in CPGC2_ALGORITHM_INSTRUCTION_CTRL.
7:6	0h RO	Reserved.
5:0	0h RW/P	**Stop On Nth Error Count (STOP_ON_N):** If STOP_ON_ERROR is set to Stop on Nth Error Mode, the test will stop after (STOP_ON_N + 1) or more errors have been accumulated in the ERR_CNTR.

5.12.202 Lane Error Mask Lower Bytes (CPGC_ERR_LNEN_LO)—Offset 3E44h

Error Lane Mask for Byte Groups 0-3.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/P	**Lower Data Lane Error Mask (DATA_ERRCHK_MASK_LO):** A mask used to disable error checking on data lanes [31:0]. Lanes selected through this mask will not be checked for errors. The lane-to-bit mapping for this mask is given by the following formula: Lane[n] -> bit[n]. Functionality will change with special mapping when buswidth is < 64 (or 72) such that ChunkMask will move to this field starting at bit [...:32] extending the necessary number of bits for a full cache line of data. The mask in ERR_CTL will be unused for these busses/modes.

5.12.203 Lane Error Mask Upper Bytes or Extended Chunk Enable (CPGC_ERR_LNEN_HI)—Offset 3E48h

Error Lane Mask for Byte Groups 4-7 or Extended Chunk Check Enable.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/P	**Upper Data Lane Error Mask (DATA_ERRCHK_MASK_HI):** A mask used to disable error checking on data lanes [63:32]. Lanes selected through this mask will not be checked for errors. The lane-to-bit mapping for this mask is given by the following formula: Lane[n+32] -> bit[n]. Functionality will change with special mapping when buswidth is < 64 (or 72) such that ChunkMask will move to this field starting at bit [...:32] extending the necessary number of bits for a full cache line of data. The mask in ERR_CTL will be unused for these busses/modes.

5.12.204 Lane Error Mask ECC (CPGC_ERR_XLNEN)—Offset 3E4Ch

ECC Lane Error Mask.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFh

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	FFh RW/P	**ECC Lane Error Mask (ECC_ERRCHK_MASK):** A mask used to disable error checking on ECC lanes. Lanes selected through the mask will not be checked for errors. The lane-to-bit mapping is 1-to-1 and hence bit 1 corresponds to ECC lane 0, bit 1 corresponds to ECC lane 1, and so on. Note: This field is available only if ECC is supported. The default state is to disable ECC checking.

5.12.205 Lane Error Status Lower Bytes (CPGC_ERR_STAT03)—Offset 3E50h

Error Status DQ Lanes 31-0 Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Lower Data Lane Error Status (LANE_ERR_STAT_LO):** Indicates if a mismatch was detected between the WR and the RD data on one of the lanes belonging to byte groups 0 - 3. Hence lanes [32:0] map to bits [32:0] respectively. The error status information is encoded as follows: 0: No mismatches detected on corresponding lane. 1: At least one mismatch detected on corresponding lane. Cleared on Local Clear Errors.

5.12.206 Lane Error Status Upper Bytes or Extended Chunk Error Status (CPGC_ERR_STAT47)—Offset 3E54h

Error Status DQ Lanes 63-32 Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Upper Data Lane Error Status (LANE_ERR_STAT_HI):** Indicates if a mismatch was detected between the WR and the RD data on one of the lanes belonging to byte groups 4 - 7. Hence lanes [63:32] map to bits [32:0] respectively. If there are less than 32 data lanes, then this register is used to indicate the Extended Chunk Error Status, and the Chunk Error Status in ECC_CHNK_RANK_STAT is not used. Chunks 0 through 15 (32-bit bus) or 0 through 31 (16-bit bus). The error status information is encoded as follows: 0: No mismatches detected on corresponding lane (chunk). 1: At least one mismatch detected on corresponding lane (chunk). Cleared on Local Clear Errors.

5.12.207 ECC Lane Error Status (CPGC_ERR_ECC_CHNK_RANK_STAT)—Offset 3E58h

Error Status for ECC, Chunks and Ranks.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:16	0h RO/V/P	**Rank Error Status (RANK_ERR_STAT):** A status field where each bit corresponds to a specific rank. If set, the corresponding rank has accumulated at least one error. Cleared on Local Clear Errors.
15:8	0h RO/V/P	**Chunk Error Status (CHUNK_ERR_STAT):** A flag field where each bit corresponds to a specific chunk (i.e. bit within a burst of 8-bits). If set, the corresponding chunk (UI) has accumulated at least one error. Cleared on Local Clear Errors.
7:0	0h RO/V/P	**ECC Lane Error Status (ECC_LANE_ERR_STAT):** A fag field which indicates if a mismatch was detected between the WR and the RD data on one of the lanes belonging to the ECC byte group. The error status information is encoded as follows: 0: No mismatches detected on corresponding lane. 1: At least one mismatch detected on corresponding lane. Note: this field is only available if ECC is supported for the current implementation, otherwise it is reserved. If BE Training Enable is set then this field indicates that the particular BE lane had a fault during the write pass. Cleared on Local Clear Errors.

5.12.208 ByteGroup Error Status (CPGC_ERR_BYTE_NTH_PAR_STAT)—Offset 3E5Ch

Error Status for ByteGroup and Error Stop.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	0h RO/V/P	**Nth Error Count Status (Nth_ERROR):** Nth_Error indicates the current Nth Error that has occurred. Nth_Error will roll over upon saturating to its maximum values. An Nth error is defined as 1 or more lane miscompares within a single comparison cycle (i.e. Chunk).
23	0h RO	Reserved.
22:20	0h RO/V/P	**Read Chunk Number Status (RD_CHUNK_NUM_STAT):** RD_Chunk_Num_Status corresponds to the chunk number being read out of the WDB (EXTBUF)for a RdCAS operation while logging an error during Loopback.Pattern. RD_Chunk_Num_Status is needed in conjunction with the lower 3 column address bits of the cacheline experiencing the error in order to deterministically rewind the LFSR/PB/LMN counter after the test is stopped due to an error condition. This is due to the pipelined nature of the data path since a cacheline can be read out of the WDB (EXTBUF) at the same time an error is being detected against an earlier read. Using RD_Chunk_Num_Status and the lower 3 column address bits of the cacheline experiencing the error allows the user to determine the skid between the LFSR/PB/LMN counter and the error detection. RD_Chunk_Num_Status can be cleared by one of two ways. 1. Local_Clear_Errors or (Global_Control and Global_Clear_Errors) to 1. 2. Writing RD_Chunk_Num_Status=0x0. One may also choose to clear individual bits in RD_Chunk_Num_Status. Setting bits in RD_Chunk_Num_Status is undefined and should be avoided. Writing a 0 to bits in RD_Chunk_Num_Status can be cleared independently of Data_Error_Status, ECC_Error_Status, Rank_Error_Status, Chunk_Error_Status, and Byte_Group_Error_Status.
19:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C/V/P	**ECC ByteGroup Error Status (ECCGRP_ERR_STAT):** A set bit implies that the ECC bytegroup has at least one lane that accumulated at least one error. Can also be cleared on Local Clear Errors (or Global_Control and a Global_Clear_Errors) .
7:0	0h RW/1C/V/P	**Data ByteGroup Error Status (BYTEGRP_ERR_STAT):** A flag field with each bit corresponding to a specific byte group. Bit 0 corresponds to byte group 0, bit 1 corresponds to byte group 1, bit 2 corresponds to byte group 2, and so on. A set bit implies that the corresponding byte group has at least one lane that accumulated at least one error. When BE Training Enable is set, then this field will indicate that a data error has occured that was not due to the corresponding BE signal. Can also be cleared on Local Clear Errors (or Global_Control and a Global_Clear_Errors) .

5.12.209 Error Counter Control (CPGC_ERR_CNTRCTL[0])—Offset 3E60h

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.12.210 Error Counter Control (CPGC_ERR_CNTRCTL[1])—Offset 3E64h

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.12.211 Error Counter Control (CPGC_ERR_CNTRCTL[2])—Offset 3E68h

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.12.212 Error Counter Control (CPGC_ERR_CNTRCTL[3])—Offset 3E6Ch

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.12.213 Error Counter Control (CPGC_ERR_CNTRCTL[4])—Offset 3E70h

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.12.214 Error Counter Control (CPGC_ERR_CNTRCTL[5])—Offset 3E74h

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.12.215 Error Counter Control (CPGC_ERR_CNTRCTL[6])—Offset 3E78h

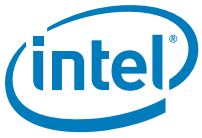
Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.



Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.12.216 Error Counter Control (CPGC_ERR_CNTRCTL[7])—Offset 3E7Ch

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.12.217 Error Counter Control (CPGC_ERR_CNTRCTL[8])—Offset 3E80h

Counter Control is used to control what is captured in the CPGC_ERR_ERRCNTR#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8:7	0h RW/P	**Error Counter Control (COUNTER_CONTROL):** Counter_Control determines what gets counted by CPGC_ERR_CNTR_#.Error_Counter. 00=Count Errors on all Lanes - The Error Counter will capture the OR of all errors across all unmasked Lanes in a Chunk. For example, if 1 lane or 72 lanes experience an error in a Chunk then the CPGC_ERR_CNTR_#.Error_Counter will be incremented by only 1. 01=Count Errors on a particular Lane - The Error Counter will count the exact number of errors on the Lane indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. 10=Count Errors on a particular Byte Group - The Error Counter will count the number of errors on the Byte group indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER. ECC is byte group 8. An error within one Chunk within the selected ByteGroup is counted as 1 error. 11=Count Errors on a particular Chunk - The Error Counter will count the number of errors on the a particular chunk in the cacheline indicated by CPGC_ERR_CNTRCTL.COUNTER_POINTER, across all lanes.
6:0	0h RW/P	**Error Counter Pointer (COUNTER_POINTER):** Used in conjunction with Counter_Control to indicate which Lane, which ByteLane or which Chunk the CPGC_ERR_CNTR_#.Error_Counter will count errors on.

5.12.218 Error Counter (CPGC_ERR_CNTR[0])—Offset 3E84h

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.12.219 Error Counter (CPGC_ERR_CNTR[1])—Offset 3E88h

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.12.220 Error Counter (CPGC_ERR_CNTR[2])—Offset 3E8Ch

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.12.221 Error Counter (CPGC_ERR_CNTR[3])—Offset 3E90h

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.12.222 Error Counter (CPGC_ERR_CNTR[4])—Offset 3E94h

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.12.223 Error Counter (CPGC_ERR_CNTR[5])—Offset 3E98h

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.12.224 Error Counter (CPGC_ERR_CNTR[6])—Offset 3E9Ch

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.12.225 Error Counter (CPGC_ERR_CNTR[7])—Offset 3EA0h

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.12.226 Error Counter (CPGC_ERR_CNTR[8])—Offset 3EA4h

Indicates the current error counter value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:0	0h RO/V/P	**Error Counter Status (ERROR_COUNTER):** CPGC_ERR_ERRCNTR indicates the current error counter value which is configured by CPGC_ERR_CNTRCTL.Counter_Control. The Counter_Status will not saturate and will wrap around, but any overflow of this counter will set the corresponding overflow status bit in CPGC_ERR_ERRCNTR_OVERFLOW_STATUS.ERROR_COUNTER_OVERFLOW. Counter_Status can only be cleared by setting Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) .

5.12.227 Error Counter Overflow (CPGC_ERR_CNTR_OV)—Offset 3EA8h

Indicates the current error counter overflow value.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8:0	0h RW/1C/V/P	**Error Counter Overflow Status (ERROR_COUNTER_OVERFLOW):** Contains the overflow flags for all Error Counters. Bit 0 corresponds to ERROR_COUNTER_0. Bit 1 corresponds to ERROR_COUNTER_1. .. Bit 8 corresponds to ERROR_COUNTER_8. Error Counter Overflow Status can be cleared by one of two ways: 1. Local_Clear_Errors (or Global_Control and a Global_Clear_Errors) to 1. 2. Writing the correspoing Error Counter Overflow Status bit to 1. Writing a 0 to bits in Counter_Overflow_Status can be cleared independently of Data_Error_Status, Byte_Group_Error_Status, Chunk_Error_Status, and ECC_Error_Status.

5.12.228 Error Log Control and Status (CPGC_ERRLOG_CTL_STAT)—Offset 3EACh

Error Logging Control and Status - All Error Log information must be read out before doing a Local Clear Errors.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW/1S	**Error Log Clear Read Buffer Pointer (CLR_DUN_RDBUF_PTR):** Initializes the Error Log Current Read Pointer. Do this prior to the start of a test.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1S	**Error Log Increment Chunk Count (INC_CHUNK_COUNT):** Advance to next portion of data which is then available in the Error Log Data Register.
14	0h RW/1S	**Error Log Auto Seek to Error (ERRLOG_AUTO):** Asserting this bit will have the effect of CPGC automatically generating the needed Read transactions such as the current Read Pointer targets the last failing cacheline. Instead of manually browsing, user can set this bit and logic will make sure that CURR_RD_PTR==ERROR_RD_PTR. This bit will always return '0' if read by software.
13	0h RW/1S	**Error Log Increment Current Read Pointer (ERRLOG_MOVE):** Asserting this bit will have the effect of incrementing by one the Current Read Pointer at the actual Read Data Buffer. User can manually browse through the Read Data Buffer and dump its contents. This bit will always return '0' if read by software.
12	0h RW/P	**Error Log Auto Chunk Increment (ERRLOG_AUTO_CHNK_INC):** Signal that will allow auto-increment feature for each 32bit data chunk read from the Error Log Data register. Note: If this bit is set, when doing the last 32bit data access via reading the Error Log Data register, the Error Log Current Read Pointer will auto increment as well.
11:9	0h RO	Reserved.
8:5	0h RO/V/P	**Error Log Error Read Pointer (ERROR_RD_PTR):** Provides the Read Pointer location that caused the error that triggered STOP_ON_ERROR. This will be used for knowing exactly which entry in the Read Data Buffer contains the faulty cacheline data.
4	0h RO	Reserved.
3:0	0h RO/V/P	**Error Log Current Read Pointer (CURR_RD_PTR):** Provides the current Read Pointer location indexed at the Read Data Buffer. This will be used for knowing how many Reads the user needs to issue to return the pointer to the actual failing entry.

5.12.229 Error Log Data Access (CPGC_ERRLOG_DATA)—Offset 3EB0h

Error Logging Data Access Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**Error Log Data (ERRLOG_DATA):** 32 bits of data corresponding to one of eight (or four for ANN) 32 bit PMI chunks available per Read Pointer location. If ERRLOG_AUTO_CHNK_INC is set, then each read to this register will read out a successive 32 bit PMI chunk of data.

5.12.230 Loopback Error Status (CPGC_ERR_TEST_ERR_STAT)—Offset 3EB4h

Indicates when a test is complete and if any errors occurred for Loopback mode.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RO/V	**Loopback Test in Progress (TEST_IN_PROGRESS):** Used to indicate a loopback test is in progress.
0	0h RO/V/P	**Loopback Local Error Status (ERROR_STATUS):** Bit set during the loopback test. Cleared when Local_Clear_Error in Loopback Sequencer Control is set.

5.12.231 Rank Logical To Physical Map (CPGC_SEQ_RANK_L2P_MAPPING)—Offset 3EB8h

Rank Logical to Physical Mapping Lookup Table Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 76543210h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:28	7h RW	**Rank 7 Mapping (L2P_RANK7_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).

Bit Range	Default & Access	Field Name (ID): Description
27	0h RO	Reserved.
26:24	6h RW	**Rank 6 Mapping (L2P_RANK6_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).
23	0h RO	Reserved.
22:20	5h RW	**Rank 5 Mapping (L2P_RANK5_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).
19	0h RO	Reserved.
18:16	4h RW	**Rank 4 Mapping (L2P_RANK4_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).
15	0h RO	Reserved.
14:12	3h RW	**Rank 3 Mapping (L2P_RANK3_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).
11	0h RO	Reserved.
10:8	2h RW	**Rank 2 Mapping (L2P_RANK2_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).
7	0h RO	Reserved.
6:4	1h RW	**Rank 1 Mapping (L2P_RANK1_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).
3	0h RO	Reserved.
2:0	0h RW	**Rank 0 Mapping (L2P_RANK0_MAPPING):** Defines what physical Rank address (Memory Controller Rank Mapping) is mapped to this logical Rank address (Sequence Address Logic Domain).

5.12.232 Bank Logical to Physical Map Low (CPGC_SEQ_BANK_L2P_MAPPING_A)—Offset 3EBCh

Bank Logical to Physical Mapping Lookup Table Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 76543210h

Bit Range	Default & Access	Field Name (ID): Description
31:28	7h RW	**Bank 7 Mapping (L2P_BANK7_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
27:24	6h RW	**Bank 6 Mapping (L2P_BANK6_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
23:20	5h RW	**Bank 5 Mapping (L2P_BANK5_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
19:16	4h RW	**Bank 4 Mapping (L2P_BANK4_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
15:12	3h RW	**Bank 3 Mapping (L2P_BANK3_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
11:8	2h RW	**Bank 2 Mapping (L2P_BANK2_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
7:4	1h RW	**Bank 1 Mapping (L2P_BANK1_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
3:0	0h RW	**Bank 0 Mapping (L2P_BANK0_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).

5.12.233 Bank Logical to Physical Map High (CPGC_SEQ_BANK_L2P_MAPPING_B)—Offset 3EC0h

Bank Logical to Physical Mapping Lookup Table Register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FEDCBA98h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RW	**Bank 15 Mapping (L2P_BANK15_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
27:24	Eh RW	**Bank 14 Mapping (L2P_BANK14_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
23:20	Dh RW	**Bank 13 Mapping (L2P_BANK13_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
19:16	Ch RW	**Bank 12 Mapping (L2P_BANK12_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
15:12	Bh RW	**Bank 11 Mapping (L2P_BANK11_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
11:8	Ah RW	**Bank 10 Mapping (L2P_BANK10_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
7:4	9h RW	**Bank 9 Mapping (L2P_BANK9_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).
3:0	8h RW	**Bank 8 Mapping (L2P_BANK8_MAPPING):** Defines what physical Bank address (Memory Controller Bank Mapping) is mapped to this logical Bank address (Sequence Address Logic Domain).

5.12.234 Rank Address Swizzle (CPGC_SEQ_RANK_ADDR_SWIZZLE)—Offset 3EC4h

This register is used to swizzle the Logical to Physical Rank bits.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FEDCh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:12	Fh RW	**Rank 3 Swizzle (L2P_RANK3_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other. Only Rank address bits available to the memory controller are valid, others should be set to 0xF.
11:8	Eh RW	**Rank 2 Swizzle (L2P_RANK2_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.
7:4	Dh RW	**Rank 1 Swizzle (L2P_RANK1_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.
3:0	Ch RW	**Rank 0 Swizzle (L2P_RANK0_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.

5.12.235 Bank Address Swizzle (CPGC_SEQ_BANK_ADDR_SWIZZLE)—Offset 3EC8h

This register is used to swizzle the Logical Bank and Row address bits to Physical Bank bits.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: DEB38h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:15	1Bh RW	**Bank 3 Swizzle (L2P_BANK3_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Bank address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value. Only Bank address bits available to the memory controller are valid, others should be set to 0x1F.
14:10	1Ah RW	**Bank 2 Swizzle (L2P_BANK2_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Bank address. The bits are essentially swizzled with each other.
9:5	19h RW	**Bank 1 Swizzle (L2P_BANK1_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Bank address. The bits are essentially swizzled with each other.

Bit Range	Default & Access	Field Name (ID): Description
4:0	18h RW	**Bank 0 Swizzle (L2P_BANK0_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Bank address. The bits are essentially swizzled with each other.

5.12.236 Row Address Swizzle Low (CPGC_SEQ_ROW_ADDR_SWIZZLE_A)—Offset 3ECCh

This register is used to swizzle the Logical to Physical Row bits.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: A418820h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:25	5h RW	**Row 5 Swizzle (L2P_ROW5_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
24:20	4h RW	**Row 4 Swizzle (L2P_ROW4_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
19:15	3h RW	**Row 3 Swizzle (L2P_ROW3_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
14:10	2h RW	**Row 2 Swizzle (L2P_ROW2_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
9:5	1h RW	**Row 1 Swizzle (L2P_ROW1_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.

Bit Range	Default & Access	Field Name (ID): Description
4:0	0h RW	**Row 0 Swizzle (L2P_ROW0_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.

5.12.237 Row Address Swizzle Mid (CPGC_SEQ_ROW_ADDR_SWIZZLE_B)—Offset 3ED0h

This register is used to swizzle the Logical to Physical Row bits.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 16A4A0E6h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:25	Bh RW	**Row 11 Swizzle (L2P_ROW11_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
24:20	Ah RW	**Row 10 Swizzle (L2P_ROW10_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
19:15	9h RW	**Row 9 Swizzle (L2P_ROW9_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
14:10	8h RW	**Row 8 Swizzle (L2P_ROW8_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
9:5	7h RW	**Row 7 Swizzle (L2P_ROW7_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.

Bit Range	Default & Access	Field Name (ID): Description
4:0	6h RW	**Row 6 Swizzle (L2P_ROW6_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.

5.12.238 Row Address Swizzle High (CPGC_SEQ_ROW_ADDR_SWIZZLE_C)—Offset 3ED4h

This register is used to swizzle the Logical to Physical Row bits.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2307B9ACh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:25	11h RW	**Row 17 Swizzle (L2P_ROW17_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value. Only Row address bits available to the memory controller are valid, others should be set to 0x1F.
24:20	10h RW	**Row 16 Swizzle (L2P_ROW16_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
19:15	Fh RW	**Row 15 Swizzle (L2P_ROW15_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
14:10	Eh RW	**Row 14 Swizzle (L2P_ROW14_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.
9:5	Dh RW	**Row 13 Swizzle (L2P_ROW13_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.

Bit Range	Default & Access	Field Name (ID): Description
4:0	Ch RW	**Row 12 Swizzle (L2P_ROW12_SWIZZLE):** Defines how a particular Logical Row or Bank bit is remapped to a Physical Row address. The bits are essentially swizzled with each other. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.

5.12.239 Row Address XOR (CPGC_SEQ_ROW_ADDR_SWIZZLE_X)—Offset 3ED8h

Row XOR source selection for lower order Row addresses.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW	**Address DQ Invert Enable (ADDR_DQ_INV_EN):** Enables the lookup table to invert the DQs based on select Row address bits.
28:20	0h RO	Reserved.
19:15	1Fh RW	**Row 3 XOR Swizzle (L2P_ROW3_XOR_SWIZZLE):** Row XOR source selection for lower order Row addresses. Select 31 if only using a direct mapping with no XOR.
14:10	1Fh RW	**Row 2 XOR Swizzle (L2P_ROW2_XOR_SWIZZLE):** Row XOR source selection for lower order Row addresses. Select 31 if only using a direct mapping with no XOR.
9:5	1Fh RW	**Row 1 XOR Swizzle (L2P_ROW1_XOR_SWIZZLE):** Row XOR source selection for lower order Row addresses. Select 31 if only using a direct mapping with no XOR.
4:0	1Fh RW	**Row 0 XOR Swizzle (L2P_ROW0_XOR_SWIZZLE):** Row XOR source selection for lower order Row addresses. Select 31 if only using a direct mapping with no XOR. Bank Bits start at select value of 24. A value of 31 will select a constant '0' value.

5.12.240 Column Address Swizzle Low (CPGC_SEQ_COL_ADDR_SWIZZLE_A)—Offset 3EDCh

This register is used to swizzle the Logical to Physical COL bits.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 65432100h

Bit Range	Default & Access	Field Name (ID): Description
31:28	6h RW	**Column 6 Swizzle (L2P_COL6_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other. Rank Bits start at select value of 12. A value of 11 will select a constant '0' value.
27:24	5h RW	**Column 5 Swizzle (L2P_COL5_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.
23:20	4h RW	**Column 4 Swizzle (L2P_COL4_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.
19:16	3h RW	**Column 3 Swizzle (L2P_COL3_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.
15:12	2h RW	**Column 2 Swizzle (L2P_COL2_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.
11:8	1h RW	**Column 1 Swizzle (L2P_COL1_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.
7:4	0h RW	**Column 0 Swizzle (L2P_COL0_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other. Column Address Bit 0 always corresponds to the logical A[6] for 64B requests and A[5] for 32B requests.
3:0	0h RO	Reserved.

5.12.241 Column Address Swizzle High (CPGC_SEQ_COL_ADDR_SWIZZLE_B)—Offset 3EE0h

This register is used to swizzle the Logical to Physical COL bits.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 87h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:4	8h RW	**Column 8 Swizzle (L2P_COL8_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other. Rank Bits start at select value of 12. A value of 11 will select a constant '0' value. Only Row address bits available to the memory controller are valid, others should be set to 11.
3:0	7h RW	**Column 7 Swizzle (L2P_COL7_SWIZZLE):** Defines how a particular Logical COL or RANK bit is remapped to a Physical COL address. The bits are essentially swizzled with each other.

5.12.242 DQ Inversion Lookup Data Low (CPGC_SEQ_ROW_ADDR_DQ_MAP0)—Offset 3EE8h

DQ Map Register 0 - This register should be 64-bit aligned at an even address - 0x0 or 0x8.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** Data written to this register will be placed in the DQ Map register as a stack. Data is read from the bottom of the stack (higher locations). The last write covers Row addresses of Row[11:4] = (0..31). Reading requires you to write into the stack to get the next location. Since this is destructive, if the data is to be preserved, then the data read should be used for the write. See documentation for details.

5.12.243 DQ Inversion Lookup Data High (CPGC_SEQ_ROW_ADDR_DQ_MAP1)—Offset 3EECh

DQ Map Register 1 - This register should be 64-bit aligned at the following odd address - 0x4 or 0xC.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** Data written to this register will be placed in the DQ Map register as a stack. Data is read from the bottom of the stack (higher locations). The last write covers Row addresses of Row[11:4] = (32..63). Reading requires you to write into the stack to get the next location. Since this is destructive, if the data is to be preserved, then the data read should be used for the write.

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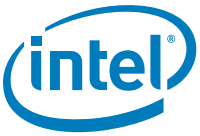

6 Graphics

6.1 Registers Summary

Table 6-1. Summary of pcs_regs Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
FF4h	FF7h	(CTXREG1)—Offset FF4h	0h
FF8h	FFBh	(ECOREG1)—Offset FF8h	0h
31030h	31033h	(PAVP1)—Offset 31030h	0h
323A4h	323A7h	(PAVP2)—Offset 323A4h	0h

6.1.1 (CTXREG1)—Offset FF4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**CTXSIZE:** (p)Register to store value for number of CTX DWORD.(/p)

6.1.2 (ECOREG1)—Offset FF8h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**LOCK:** (p)Lock bit for this register(/p)
30:0	0h RW	**ECOREG**

6.1.3 (PAVP1)—Offset 31030h

PAVP register for SAI testing

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h WO	**DATA:** (p)PAVP register for SAI testing(/p)

6.1.4 (PAVP2)—Offset 323A4h

PAVP register for SAI testing

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h WO	**DATA:** (p)PAVP register for SAI testing(/p)

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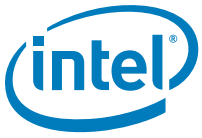


7 Display

7.1 Registers Summary

Table 7-1. Summary of pcs_regs Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
10h	13h	LJPLL_RW_CONTROL_1 (LJPLL_CR_RW_CONTROL_1)—Offset 10h	0h
14h	17h	LJPLL_RW_CONTROL_2 (LJPLL_CR_RW_CONTROL_2)—Offset 14h	0h
20h	27h	depll_cp (depll_cp)—Offset 20h	40001200211h
28h	2Fh	depll_rac (depll_rac)—Offset 28h	40001200211h
30h	37h	depll_wac (depll_wac)—Offset 30h	40001200211h

7.1.1 LJPLL_RW_CONTROL_1 (LJPLL_CR_RW_CONTROL_1)—Offset 10h

LJPLL CR

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**SSC_FRAC_STEP (SSC_FRAC_STEP):** ssc fraction step
7:0	0h RW	**SSC_RATIO_STEP (SSC_RATIO_STEP):** SSC ratio step

7.1.2 LJPLL_RW_CONTROL_2 (LJPLL_CR_RW_CONTROL_2)—Offset 14h

LJPLL CR

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**PLL_RSVD_1 (PLL_RSVD_1):** PLL Rsvd
11:10	0h RW	**SSC_MODE (SSC_MODE):** SSC mode select
9	0h RW	**SSC_EN (SSC_EN):** SSC enable
8:0	0h RW	**SSC_CYC_TO_PEAK_M1 (SSC_CYC_TO_PEAK_M1):** Ssc cycle to peak

7.1.3 depll_cp (depll_cp)—Offset 20h

Policy DEPLL_POLICY_GROUP CP Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001200211h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001200211h RW	**sai[63:0] (sai)**

7.1.4 depll_rac (depll_rac)—Offset 28h

Policy DEPLL_POLICY_GROUP RAC Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001200211h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001200211h RW	**sai[63:0] (sai)**

7.1.5 depll_wac (depll_wac)—Offset 30h

Policy DEPLL_POLICY_GROUP WAC Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001200211h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001200211h RW	**sai[63:0] (sai)**

7.2 Registers Summary

Table 7-2. Summary of pcs_regs Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
50h	53h	GMCH Graphics Control (GGC_0_0_0_PCI)—Offset 50h	500h
54h	57h	Device Enable (DEVEN_0_0_0_PCI)—Offset 54h	BFh
5Ch	5Fh	DMA Protected Range (DPR_0_0_0_PCI)—Offset 5Ch	0h
A8h	ABh	TOUUD_LO_0_0_0_PCI (TOUUD_LO_0_0_0_PCI)—Offset A8h	0h
ACh	AFh	TOUUD_HI_0_0_0_PCI (TOUUD_HI_0_0_0_PCI)—Offset ACh	0h
B0h	B3h	Base Data of Stolen Memory (BDSM_0_0_0_PCI)—Offset B0h	0h
B4h	B7h	Base of GTT Stolen Memory (BGSM_0_0_0_PCI)—Offset B4h	0h
B8h	BBh	TSEG Base Memory (TSEGMB_0_0_0_PCI)—Offset B8h	0h
BCh	BFh	Top Of Low Usable DRAM (TOLUD_0_0_0_PCI)—Offset BCh	0h
E4h	E7h	Capabilities A (CAPID0_A_0_0_0_PCI)—Offset E4h	0h
E8h	EBh	Capabilities B (CAPID0_B_0_0_0_PCI)—Offset E8h	0h

7.2.1 GMCH Graphics Control (GGC_0_0_0_PCI)—Offset 50h

GMCH Graphics Control Register.

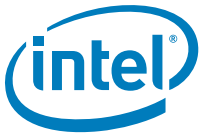
Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 500h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:8	5h RW/L	**Graphics Mode Select (GMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.Hardware does not clear or set any of these bits automatically based on IGD being disabled/ enabled.BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.BIOS Requirement: Given new sizes allow down to 8MB allocation, BIOS has to ensure there is sufficient space for WOPCM and basic GFX Stolen functions.00h: 0MB01h: 32MB02h: 64MB03h: 96MB04h: 128MB05h: 160MB (default)06h: 192MB07h: 224MB08h: 256MB09h: 288MB0Ah: 320MB0Bh: 352MB0Ch: 384MB0Dh: 416MB0Eh: 448MB0Fh: 480MB10h: 512MB11h - 1Fh: Reserved20h:1024MB21h - 2Fh: Reserved30h:1536MB31h - 3Fh: Reserved40h: 2048MB41h - EFh: ReservedF0h: 4MBF1h: 8MBF2h: 12MBF3h: 16MBF4h: 20MBF5h: 24MBF6h: 28MBF7h: 32MBF8h: 36MBF9h: 40MBFAh: 44MBFBh: 48MBFCh: 52MBFDh: 56MBFEh: 60MBFFh: ReservedHardware functionality in case of programming this value to Reserved is not guaranteed.
7:6	0h RW/L	**GTT Graphics Memory Size (GGMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register.Hardware functionality in case of programming this value to Reserved is not guaranteed.0x0: No Preallocated Memory0x1: 2MB of Preallocated Memory0x2: 4MB of Preallocated Memory0x3: 8MB of Preallocated Memory
5:3	0h RO	**RESERVED (RSVD_0):** Reserved
2	0h RW/L	**Versatile Acceleration Mode Enable (VAMEN):** Enables the use of the iGFX engines for Versatile Acceleration.1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h.0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
1	0h RW/L	**IGD VGA Disable (IVD):** 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00.1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80.BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory.This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0_A[IGD] = 1) or via a register (DEVEN[3] = 0).
0	0h RW/L	**GGC Lock (GGCLCK):** When set to 1b, this bit will lock all bits in this register.



7.2.2 Device Enable (DEVEN_0_0_0_PCI)—Offset 54h

Allows for enabling/disabling of PCI devices and functions that are within the CPU package. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: BFh

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**RESERVED (RSVD_3)**
14	0h RW	**Chap Enable (D7EN)**
13	0h RW	**Device 6 Enable (D6EN)**
12:11	0h RO	**RESERVED (RSVD_2)**
10	0h RW/L	**Device 5 Enable (D5EN)**
9:8	0h RO	**RESERVED (RSVD_1)**
7	1h RW/L	**Device 4 Enable (D4EN)**
6	0h RO	**RESERVED (RSVD_0)**
5	1h RW/L	**Device 3 enable for Display HD Audio (D3EN)**
4	1h RW/L	**Internal Graphics Engine (D2EN):** 0: Bus 0 Device 2 is disabled and hidden1: Bus 0 Device 2 is enabled and visibleThis bit will be set to 0b and remain 0b if Device 2 capability is disabled.
3	1h RW/L	**PEG10 Enable (D1F0EN)**
2	1h RW/L	**PEG11 Enable (D1F1EN)**
1	1h RW/L	**PEG12 Enable (D1F2EN)**
0	1h RO	**Host Bridge (D0EN)**

7.2.3 DMA Protected Range (DPR_0_0_0_PCI)—Offset 5Ch

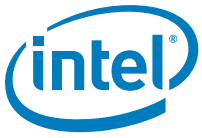
DMA protected range register.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO/V	**Top of DPR (TOPOFDPR):** Top address + 1 of DPR. This is the base of TSEG. Bits 19:0 of the BASE reported here are 0x0_0000.
19:12	0h RO	**RESERVED (RSVD_1):** Reserved
11:4	0h RW/L	**DPRSIZE (DPRSIZE):** This is the size of memory, in MB, that will be protected from DMA accesses. A value of 0x00 in this field means no additional memory is protected.The maximum amount of memory that will be protected is 255MB.The amount of memory reported in this field will be protected from all DMA accesses, including translated CPU accesses and graphics. The top of the protected range is the BASE of TSEG -1.Note: If TSEG is not enabled, then the top of this range becomes the base of stolen graphics, or ME stolen space or TOLUD, whichever would have been the location of TSEG, assuming it had been enabled.The DPR range works independently of any other range, including the NoDMA.TABLE protection or the PMRC checks in VTd, and is done post any VTd translation or LT NoDMA lookup. Therefore incomming cycles are checked against this range after the VTd translation and faulted if they hit this protected range, even if they passed the VTd translation or were clean in the NoDMA lookup. All the memory checks are OR'ed with respect to NOT being allowed to go to memory. So if either PMRC, DPR, NoDMA table lookup, NoDMA.TABLE.PROTECT OR a VTd translation disallows the cycle, then the cycle is not allowed to go to memory. Or in other words, all of the above checks must pass before a cycle is allowed to DRAM.HW reports the status of DPR enable/disabled through the PRS field in this register.
3	0h RO	**RESERVED (RSVD_0):** Reserved
2	0h RW/L	**EPM (EPM):** This field controls DMA accesses to the DMA Protected Range (DPR) region.0: DPR is disabled.1: DPR is enabled. All DMA requests accessing DPR region are blocked.HW reports the status of DPR enable/disabled through the PRS field in this register.
1	0h RO/V	**Protected Range Status (PRS):** This field indicated the status of DPR.0: DPR protection disabled.1: DPR protection enabled.
0	0h RW/L	**Lock (LOCK):** All bits which may be updated by SW in this register are locked down when this bit is set.



7.2.4 TOUUD_LO_0_0_0_PCI (TOUUD_LO_0_0_0_PCI)—Offset A8h

Top of Upper Usable DRAM This 64 bit register defines the Top of Upper Usable DRAM. Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled this value must be set to reclaim limit 1byte 1MB aligned since reclaim limit is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4GB. BIOS Restriction: Minimum value for TOUUD is 4GB.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**TOUUD (TOUUD):** This register contains bits 38 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system. Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled this value must be set to reclaim limit 1MB aligned since reclaim limit 1byte is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4GB. Note: for 40bit addressing have to add a bit to this field
19:1	0h RO	**RESERVED_0 (RESERVED_0):** Reserved should return 0s on read
0	0h RW	**LOCK_RESERVED (LOCK_RESERVED):** This lock bit only impacts the Display copy of this register. In the Cunit all register protection is implemented with SAI policy groups. This bit is maintained in the Cunit for software observability. Diplay description: This bit will lock all writeable settings in this register including itself client definition.

7.2.5 TOUUD_HI_0_0_0_PCI (TOUUD_HI_0_0_0_PCI)—Offset ACh

Top of Upper Usable DRAM This 64 bit register defines the Top of Upper Usable DRAM. Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled this value must be set to reclaim limit 1byte 1MB aligned since reclaim limit is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4GB. BIOS Restriction: Minimum value for TOUUD is 4GB.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
6:0	0h RW	**TOUUD_HI (TOUUD_HI):** This register contains bits 38 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system. Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled this value must be set to reclaim limit 1MB aligned since reclaim limit 1byte is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4GB. Note: for 40bit addressing have to add a bit to this field

7.2.6 Base Data of Stolen Memory (BDSM_0_0_0_PCI)—Offset B0h

This register contains the base address of graphics data stolen DRAM memory.

Access Method

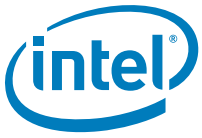
Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/L	**Graphics Base of Stolen Memory (BDSM):** This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 52 bits 6:4) from TOLUD (PCI Device 0 offset BC bits 31:20).
19:1	0h RO	**RESERVED (RSVD_0):** Reserved
0	0h RW/L	**Lock (LOCK):** This bit will lock all writeable settings in this register, including itself.

7.2.7 Base of GTT Stolen Memory (BGSM_0_0_0_PCI)—Offset B4h

This register contains the base address of stolen DRAM memory for the GTT.



Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/L	**Graphics Base of GTT Stolen Memory (BGSM):** This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 11:8) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).
19:1	0h RO	**RESERVED (RSVD_0):** Reserved
0	0h RW/L	**Lock (LOCK):** This bit will lock all writeable settings in this register, including itself.

7.2.8 TSEG Base Memory (TSEGMB_0_0_0_PCI)—Offset B8h

This 32 bit register defines the TSEG Base.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/L	**TSEG Memory Base (TSEGMB):** This register contains the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory which must be at or below Graphics Base of GTT Stolen Memory (PCI Device 0 Offset B4 bits 31:20).Bios must program the value of TSEGMB to be the same as BGSM when TSEG is disabled.
19:1	0h RO	**RESERVED (RSVD_0):** Reserved
0	0h RW/L	**Lock (LOCK):** This bit will lock all writeable settings in this register, including itself.

7.2.9 Top Of Low Usable DRAM (TOLUD_0_0_0_PCI)—Offset BCh

This 32 bit register defines the low usable DRAM.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/L	**Top of Low Usable DRAM (TOLUD):** This register contains bits 31 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system.The top of low usable DRAM is the lowest address above both graphics stolen memory and Tseg.
19:1	0h RO	**RESERVED (RSVD_0):** Reserved
0	0h RW/L	**Lock (LOCK):** This bit will lock all writeable settings in this register, including itself.

7.2.10 Capabilities A (CAPID0_A_0_0_0_PCI)—Offset E4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Display HD Audio Disable (DHDAD)**
30	0h RW	**PEG12 Disable (PEG12D)**
29	0h RW	**PEG11 Disable (PEG11D)**
28	0h RW	**PEG10 Disable (PEG10D)**
27	0h RW	**PCI Express Link Width Upconfig Disable (PELWUD)**
26	0h RW	**DMI Width (DW)**
25	0h RW	**ECC Disable (ECCDIS)**
24	0h RW	**Force DRAM ECC Enabled (FDEE)**
23	0h RW	**VTd Disable (VTDD):** 0 - Enable VTd1 - Disable VTd
22	0h RW	**DMI Gen 2 Disable (DMIG2DIS)**
21	0h RW	**PEG Gen 2 Disable (PEGG2DIS)**

Bit Range	Default & Access	Field Name (ID): Description
20:19	0h RW	**DDR Size (DDRSZ)**
18	0h RW	**Bclk overclocking disable (PCIE_RATIO_DIS)**
17	0h RW	**Disable 1N Mode (D1NM)**
16	0h RW	**Full ULT Fuse Read Disable (FUFRD)**
15	0h RW	**Camarillo Device Disable (CDD)**
14	0h RW	**2 DIMMS per Channel Disable (DDPCD)**
13	0h RW	**X2APIC Enabled (X2APIC_EN)**
12	0h RW	**Performance Dual Channel Disable (PDCD)**
11	0h RW	**Internal Graphics Disable (IGD):** 0b: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessable. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory.1b: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control. Device 2 is disabled and hidden.
10	0h RO	Reserved.
9:8	0h RW	**Capability Device ID (CDID)**
7:4	0h RW	**Compatibility Rev ID (CRID):** This is an 8-bit value that indicates the revision identification number for the Host Device 0.
3	0h RW	**DDR Overclocking (DDR_OVERCLOCK)**
2	0h RW	**IA Overclocking Enabled by DSKU (OC_ENABLED_DSKU)**
1	0h RW	**DDR Write VRef (DDR_WRTVREF)**
0	0h RW	**DDR3L Enable (DDR3L_EN)**

7.2.11 Capabilities B (CAPID0_B_0_0_0_PCI)—Offset E8h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Reserved_31 (SPARE31)**
30	0h RW	**IA Overclocking DSKU Control Disable (OC_CTL_DSKU_DIS)**
29	0h RW	**IA Overclocking Enable (OC_ENABLED)**
28	0h RW	**SMT Capability (SMT)**
27:25	0h RW	**Cache Size Capability (CACHESZ)**
24	0h RW	**SVMDIS (SVMDIS):** 0 - SVM mode enabled1 - SVM mode disabled
23:21	0h RW	**DDR3 Maximum Frequency Capability with 100 Memory (PLL_REF100_CFG)**
20	0h RW	**Gen3 Disable Fuse for PCIe PEG Controllers (PEGG3_DIS)**
19	0h RW	**Package Type (PKGTYP)**
18	0h RW	**Additive Graphics Enabled (ADDGFXEN):** 0 - Additive Graphics Disabled1 - Additive Graphics Enabled
17	0h RW	**Additive Graphics Capable (ADDGFXCAP):** 0 - Capable of Additive Graphics1 - Not capable of Additive Graphics
16	0h RW	**Primary PEG Port x16 Disable (PEGX16D)**
15:12	0h RW	**Reserved_15_12 (SPARE15_12)**
11	0h RO	Reserved.
10:8	0h RW	**Reserved_10_8 (SPARE10_8)**
7	0h RO	Reserved.
6:4	0h RW	**DDR3 Maximum Frequency Capability (DMFC)**
3	0h RW	**Reserved_3 (SPARE3)**
2	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Dual PEG Force x1 when VGA Enabled (DPEGFX1)**
0	0h RW	**Single PEG Force x1 when VGA Enabled (SPEGFX1)**

7.3 Registers Summary

Table 7-3. Summary of pcs_regs Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	(VID2_0_2_0_PCI)—Offset 0h	0h
2h	3h	Device Identification (DID2_0_2_0_PCI)—Offset 2h	A84h
4h	5h	(PCICMD_0_2_0_PCI)—Offset 4h	0h
6h	7h	(PCISTS2_0_2_0_PCI)—Offset 6h	0h
8h	Bh	(RID2_CC_0_2_0_PCI)—Offset 8h	0h
Ch	Ch	(CLS_0_2_0_PCI)—Offset Ch	0h
Dh	Dh	(MLT2_0_2_0_PCI)—Offset Dh	0h
Eh	Eh	(HDR2_0_2_0_PCI)—Offset Eh	0h
Fh	Fh	(BIST_0_2_0_PCI)—Offset Fh	0h
10h	13h	(GTTMMADR_LO_0_2_0_PCI)—Offset 10h	0h
14h	17h	(GTTMMADR_HI_0_2_0_PCI)—Offset 14h	0h
18h	1Bh	(GMADR_LO_0_2_0_PCI)—Offset 18h	0h
1Ch	1Fh	(GMADR_HI_0_2_0_PCI)—Offset 1Ch	0h
20h	23h	(IOBAR_0_2_0_PCI)—Offset 20h	0h
2Ch	2Dh	(SVID2_0_2_0_PCI)—Offset 2Ch	0h
2Eh	2Fh	(SID2_0_2_0_PCI)—Offset 2Eh	0h
3Ch	3Ch	(INTRLINE_0_2_0_PCI)—Offset 3Ch	0h
3Dh	3Dh	(INTRPIN_0_2_0_PCI)—Offset 3Dh	0h
3Eh	3Eh	(MINGNT_0_2_0_PCI)—Offset 3Eh	0h
3Fh	3Fh	(MAXLAT_0_2_0_PCI)—Offset 3Fh	0h
58h	58h	(DEV2CTL_0_2_0_PCI)—Offset 58h	0h
60h	61h	(HSRW_0_2_0_PCI)—Offset 60h	0h
62h	62h	(MSAC_0_2_0_PCI)—Offset 62h	0h
63h	63h	(VTD_STATUS_0_2_0_PCI)—Offset 63h	0h
ACh	ADh	(MSI_CAPID_0_2_0_PCI)—Offset ACh	0h
AEh	AFh	(MC_0_2_0_PCI)—Offset AEh	0h
B0h	B3h	(MA_0_2_0_PCI)—Offset B0h	0h
B4h	B5h	(MD_0_2_0_PCI)—Offset B4h	0h
D4h	D5h	(PMCS_0_2_0_PCI)—Offset D4h	0h
E0h	E1h	(SWSMI_0_2_0_PCI)—Offset E0h	0h
E8h	E9h	(SWSCI_0_2_0_PCI)—Offset E8h	0h
F8h	FBh	(SRID_0_2_0_PCI)—Offset F8h	0h

Table 7-3. Summary of pcs_regs Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
FCh	FFh	(ASLS_0_2_0_PCI)—Offset FCh	0h
104h	105h	(PASID_CAP_0_2_0_PCI)—Offset 104h	0h
106h	106h	(PASID_CTRL_0_2_0_PCI)—Offset 106h	0h
204h	205h	(ATS_CAP_0_2_0_PCI)—Offset 204h	0h
206h	207h	(ATS_CTRL_0_2_0_PCI)—Offset 206h	0h
304h	305h	(PR_CTRL_0_2_0_PCI)—Offset 304h	0h
306h	307h	(PR_STATUS_0_2_0_PCI)—Offset 306h	0h
30Ch	30Fh	(OPRA_0_2_0_PCI)—Offset 30Ch	0h

7.3.1 (VID2_0_2_0_PCI)—Offset 0h

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.2 Device Identification (DID2_0_2_0_PCI)—Offset 2h

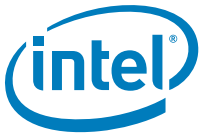
This register combined with the Vendor Identification register uniquely identifies any PCI device.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: A84h

Bit Range	Default & Access	Field Name (ID): Description
15:7	15h RO/V	**Device Identification Number MSB (DID_MSB):** This is the upper part of a 16 bit value assigned to the device.
6:2	1h RO/V	**Device Identification Number STRAPS (DID_STRAPS):** These are bits 6:2 of the 16 bit value, updated from straps.
1:0	0h RO/V	**Device Identification Number SKU (DID_SKU):** This is the lower part of a 16 bit value assigned to the device.



7.3.3 (PCICMD_0_2_0_PCI)—Offset 4h

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.4 (PCISTS2_0_2_0_PCI)—Offset 6h

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.5 (RID2_CC_0_2_0_PCI)—Offset 8h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.3.6 (CLS_0_2_0_PCI)—Offset Ch

Regiter used for GT save/restore definition in PUNIT It is just a byte used as a single field.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Data**

7.3.7 (MLT2_0_2_0_PCI)—Offset Dh

Regiter used for GT save/restore definition in PUNIT It is just a byte used as a single field.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Data**

7.3.8 (HDR2_0_2_0_PCI)—Offset Eh

Regiter used for GT save/restore definition in PUNIT It is just a byte used as a single field.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Data**

7.3.9 (BIST_0_2_0_PCI)—Offset Fh

Regiter used for GT save/restore definition in PUNIT It is just a byte used as a single field.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Data**

7.3.10 (GTTMMADR_LO_0_2_0_PCI)—Offset 10h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.3.11 (GTTMMADR_HI_0_2_0_PCI)—Offset 14h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.3.12 (GMADR_LO_0_2_0_PCI)—Offset 18h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.3.13 (GMADR_HI_0_2_0_PCI)—Offset 1Ch

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.3.14 (IOBAR_0_2_0_PCI)—Offset 20h

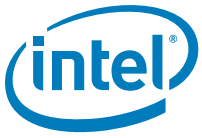
Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**



7.3.15 (SVID2_0_2_0_PCI)—Offset 2Ch

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.16 (SID2_0_2_0_PCI)—Offset 2Eh

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.17 (INTRLINE_0_2_0_PCI)—Offset 3Ch

Regiter used for GT save/restore definition in PUNIT It is just a byte used as a single field.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Data**

7.3.18 (INTRPIN_0_2_0_PCI)—Offset 3Dh

Regiter used for GT save/restore definition in PUNIT It is just a byte used as a single field.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Data**

7.3.19 (MINGNT_0_2_0_PCI)—Offset 3Eh

Regiter used for GT save/restore definition in PUNIT It is just a byte used as a single field.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Data**

7.3.20 (MAXLAT_0_2_0_PCI)—Offset 3Fh

Regiter used for GT save/restore definition in PUNIT It is just a byte used as a single field.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Data**

7.3.21 (DEV2CTL_0_2_0_PCI)—Offset 58h

Regiter used for GT save/restore definition in PUNIT It is just a byte used as a single field.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Data**

7.3.22 (HSRW_0_2_0_PCI)—Offset 60h

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.23 (MSAC_0_2_0_PCI)—Offset 62h

Regiter used for GT save/restore definition in PUNIT It is just a byte used as a single field.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Data**

7.3.24 (VTD_STATUS_0_2_0_PCI)—Offset 63h

Regiter used for GT save/restore definition in PUNIT It is just a byte used as a single field.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Data**

7.3.25 (MSI_CAPID_0_2_0_PCI)—Offset ACh

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.26 (MC_0_2_0_PCI)—Offset AEh

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.27 (MA_0_2_0_PCI)—Offset B0h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.3.28 (MD_0_2_0_PCI)—Offset B4h

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.29 (PMCS_0_2_0_PCI)—Offset D4h

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.30 (SWSMI_0_2_0_PCI)—Offset E0h

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.31 (SWSCI_0_2_0_PCI)—Offset E8h

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.32 (SRID_0_2_0_PCI)—Offset F8h

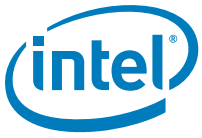
Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**



7.3.33 (ASLS_0_2_0_PCI)—Offset FCh

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.3.34 (PASID_CAP_0_2_0_PCI)—Offset 104h

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.35 (PASID_CTRL_0_2_0_PCI)—Offset 106h

Regiter used for GT save/restore definition in PUNIT It is just a byte used as a single field.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Data**

7.3.36 (ATS_CAP_0_2_0_PCI)—Offset 204h

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.37 (ATS_CTRL_0_2_0_PCI)—Offset 206h

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.38 (PR_CTRL_0_2_0_PCI)—Offset 304h

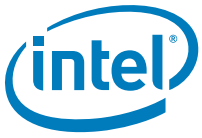
Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**



7.3.39 (PR_STATUS_0_2_0_PCI)—Offset 306h

Regiter used for GT save/restore definition in PUNIT It is just the word used as a single field.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data**

7.3.40 (OPRA_0_2_0_PCI)—Offset 30Ch

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.4 Registers Summary

Table 7-4. Summary of pcs_regs Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6C88h	6C8Fh	GFXVTDBAR_0_0_0_MCHBAR_C (MCHBAR_FULL)—Offset 6C88h	0h

7.4.1 GFXVTDBAR_0_0_0_MCHBAR_C (MCHBAR_FULL)—Offset 6C88h

This is the base address for the Graphics VT configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset the GFXVT configuration space is disabled and must be enabled by writing a 1 to GFXVTBAREN. BIOS programs this register after which the register cannot be altered.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**RESERVED_1 (RESERVED_1):** Reserved
38:12	0h RW	**GFXVTBAR (GFXVTBAR):** This field corresponds to bits 39 to 12 of the base address GFXVT configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the GFXVT register set. All the Bits in this register are locked in LT mode.
11:2	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
1	0h RW	**LOCK (LOCK):** This lock bit only impacts the Display copy of this register. In the Cunit all register protection is implemented with SAI policy groups. This bit is maintained in the Cunit for software observability. Diplay description: Locks the contents of the register including itself.
0	0h RW/L	**GFXVTBAREN (GFXVTBAREN):** 0: GFXVTBAR is disabled and does not claim any memory 1: GFXVTBAR memory mapped accesses are claimed and decoded appropriately This bit will remain 0 if VTd capability is disabled.

7.5 Registers Summary

Table 7-5. Summary of pcs_regs Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
101010h	101013h	(GU_CNTL)—Offset 101010h	0h
101014h	101017h	(CLOCK_GATE_DIS)—Offset 101014h	0h
10101Ch	10101Fh	(GU_ECO)—Offset 10101Ch	0h
101020h	101023h	(PCBR_LSB)—Offset 101020h	0h
101024h	101027h	(PCBR_MSB)—Offset 101024h	0h
108180h	108183h	(MPMEN)—Offset 108180h	0h
1081C0h	1081C3h	(MPLMBASE)—Offset 1081C0h	0h
108200h	108203h	(MPLMLIMIT)—Offset 108200h	0h
108240h	108243h	(MPHMBASE_LSB)—Offset 108240h	0h
108244h	108247h	(MPHMBASE_MSB)—Offset 108244h	0h
108280h	108283h	(MPHMLIMIT_LSB)—Offset 108280h	0h
108284h	108287h	(MPHMLIMIT_MSB)—Offset 108284h	0h

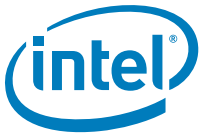


Table 7-5. Summary of pcs_regs Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
108300h	108303h	(MGCMD)—Offset 108300h	0h
110000h	110003h	(SVM_DEV_MODE_CNFG)—Offset 110000h	0h
12000Ch	12000Fh	(DEV2SEQSTS)—Offset 12000Ch	0h
124830h	124833h	(RTADDR_LSB)—Offset 124830h	0h
124834h	124837h	(RTADDR_MSB)—Offset 124834h	0h

7.5.1 (GU_CNTL)—Offset 101010h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.5.2 (CLOCK_GATE_DIS)—Offset 101014h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

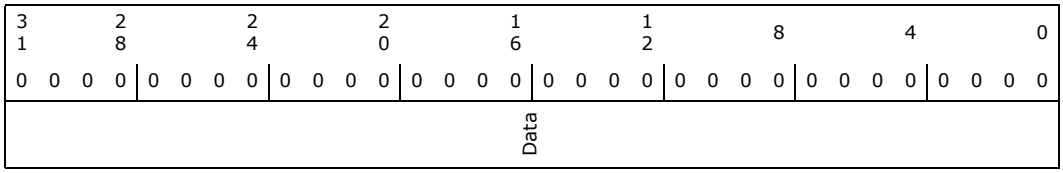
7.5.3 (GU_ECO)—Offset 10101Ch

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.5.4 (PCBR_LSB)—Offset 101020h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.5.5 (PCBR_MSB)—Offset 101024h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.5.6 (MPMEN)—Offset 108180h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.5.7 (MPLMBASE)—Offset 1081C0h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.5.8 (MPLMLIMIT)—Offset 108200h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.5.9 (MPHMBASE_LSB)—Offset 108240h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.5.10 (MPHMBASE_MSB)—Offset 108244h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.5.11 (MPHMLIMIT_LSB)—Offset 108280h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.5.12 (MPHMLIMIT_MSB)—Offset 108284h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.5.13 (MGCMD)—Offset 108300h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.5.14 (SVM_DEV_MODE_CNFG)—Offset 110000h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.5.15 (DEV2SEQSTS)—Offset 12000Ch

This register reflects the status of Device 2 sequencer flows and FSM.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**RSVD**
8	0h RO	**IOMMU_IDLE**
7:4	0h RO	**RSVD1**
3:0	0h RO	**FSM**

7.5.16 (RTADDR_LSB)—Offset 124830h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.5.17 (RTADDR_MSB)—Offset 124834h

Regiter used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6 Registers Summary

Table 7-6. Summary of pcs_regs Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
18h	1Bh	(GCMD_REG_0_0_0_VTDBAR)—Offset 18h	0h
1Ch	1Fh	(GSTS_REG_0_0_0_VTDBAR)—Offset 1Ch	0h
20h	27h	(RTADDR_REG_0_0_0_VTDBAR)—Offset 20h	0h
28h	2Fh	(CCMD_REG_0_0_0_VTDBAR)—Offset 28h	0h
34h	37h	(FSTS_REG_0_0_0_VTDBAR)—Offset 34h	0h
38h	3Bh	(FECTL_REG_0_0_0_VTDBAR)—Offset 38h	0h
3Ch	3Fh	(FEDATA_REG_0_0_0_VTDBAR)—Offset 3Ch	0h
40h	43h	(FEADDR_REG_0_0_0_VTDBAR)—Offset 40h	0h
44h	47h	(FEUADDR_REG_0_0_0_VTDBAR)—Offset 44h	0h
64h	67h	(PMEN_REG_0_0_0_VTDBAR)—Offset 64h	0h
68h	6Bh	(PLMBASE_REG_0_0_0_VTDBAR)—Offset 68h	0h
6Ch	6Fh	(PLMLIMIT_REG_0_0_0_VTDBAR)—Offset 6Ch	0h
70h	77h	(PHMBASE_REG_0_0_0_VTDBAR)—Offset 70h	0h
78h	7Fh	(PHMLIMIT_REG_0_0_0_VTDBAR)—Offset 78h	0h
80h	87h	(IQH_REG_0_0_0_VTDBAR)—Offset 80h	0h
88h	8Fh	(IQT_REG_0_0_0_VTDBAR)—Offset 88h	0h
90h	97h	(IQA_REG_0_0_0_VTDBAR)—Offset 90h	0h
9Ch	9Fh	(ICS_REG_0_0_0_VTDBAR)—Offset 9Ch	0h
A0h	A3h	(IECTL_REG_0_0_0_VTDBAR)—Offset A0h	0h
A4h	A7h	(IEDATA_REG_0_0_0_VTDBAR)—Offset A4h	0h
A8h	ABh	(IEADDR_REG_0_0_0_VTDBAR)—Offset A8h	0h
ACh	AFh	(IEUADDR_REG_0_0_0_VTDBAR)—Offset ACh	0h
B8h	BFh	(IRTA_REG_0_0_0_VTDBAR)—Offset B8h	0h
DCh	DFh	(PRESTS_REG_0_0_0_VTDBAR)—Offset DCh	0h
E0h	E3h	(PRECTL_REG_0_0_0_VTDBAR)—Offset E0h	0h
E4h	E7h	(PREDATA_REG_0_0_0_VTDBAR)—Offset E4h	0h
E8h	EBh	(PREADDR_REG_0_0_0_VTDBAR)—Offset E8h	0h
ECh	EFh	(PREUADDR_REG_0_0_0_VTDBAR)—Offset ECh	0h
400h	407h	(FRCDL_REG_0_0_0_VTDBAR)—Offset 400h	0h
408h	40Fh	(FRCDH_REG_0_0_0_VTDBAR)—Offset 408h	0h
500h	507h	(IVA_REG_0_0_0_VTDBAR)—Offset 500h	0h
508h	50Fh	(IOTLB_REG_0_0_0_VTDBAR)—Offset 508h	0h
F00h	F07h	(INTRTADDR_0_0_0_VTDBAR)—Offset F00h	0h

Table 7-6. Summary of pcs_regs Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
F08h	F0Fh	(INTIRTA_0_0_0_VTDBAR)—Offset F08h	0h

7.6.1 (GCMD_REG_0_0_0_VTDBAR)—Offset 18h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.2 (GSTS_REG_0_0_0_VTDBAR)—Offset 1Ch

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.3 (RTADDR_REG_0_0_0_VTDBAR)—Offset 20h

Register used for GT save/restore definition in PUNIT It is just the whole qword used as a single field.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW	**Data**

7.6.4 (CCMD_REG_0_0_0_VTDBAR)—Offset 28h

Register used for GT save/restore definition in PUNIT It is just the whole qword used as a single field.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW	**Data**

7.6.5 (FSTS_REG_0_0_0_VTDBAR)—Offset 34h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.6 (FECTL_REG_0_0_0_VTDBAR)—Offset 38h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.7 (FEDATA_REG_0_0_0_VTDBAR)—Offset 3Ch

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.8 (FEADDR_REG_0_0_0_VTDBAR)—Offset 40h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

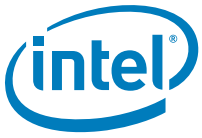
7.6.9 (FEUADDR_REG_0_0_0_VTDBAR)—Offset 44h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.10 (PMEN_REG_0_0_0_VTDBAR)—Offset 64h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.11 (PLMBASE_REG_0_0_0_VTDBAR)—Offset 68h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.12 (PLMLIMIT_REG_0_0_0_VTDBAR)—Offset 6Ch

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.13 (PHMBASE_REG_0_0_0_VTDBAR)—Offset 70h

Register used for GT save/restore definition in PUNIT It is just the whole qword used as a single field.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW	**Data**

7.6.14 (PHMLIMIT_REG_0_0_0_VTDBAR)—Offset 78h

Register used for GT save/restore definition in PUNIT It is just the whole qword used as a single field.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW	**Data**

7.6.15 (IQH_REG_0_0_0_VTDBAR)—Offset 80h

Register used for GT save/restore definition in PUNIT It is just the whole qword used as a single field.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW	**Data**

7.6.16 (IQT_REG_0_0_0_VTDBAR)—Offset 88h

Register used for GT save/restore definition in PUNIT It is just the whole qword used as a single field.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW	**Data**

7.6.17 (IQA_REG_0_0_0_VTDBAR)—Offset 90h

Register used for GT save/restore definition in PUNIT It is just the whole qword used as a single field.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW	**Data**

7.6.18 (ICS_REG_0_0_0_VTDBAR)—Offset 9Ch

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.19 (IECTL_REG_0_0_0_VTDBAR)—Offset A0h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.20 (IEDATA_REG_0_0_0_VTDBAR)—Offset A4h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.21 (IEADDR_REG_0_0_0_VTDBAR)—Offset A8h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.22 (IEUADDR_REG_0_0_0_VTDBAR)—Offset ACh

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.23 (IRTA_REG_0_0_0_VTDBAR)—Offset B8h

Register used for GT save/restore definition in PUNIT It is just the whole qword used as a single field.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW	**Data**

7.6.24 (PRESTS_REG_0_0_0_VTDBAR)—Offset DCh

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.25 (PRECTL_REG_0_0_0_VTDBAR)—Offset E0h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.26 (PREDATA_REG_0_0_0_VTDBAR)—Offset E4h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.27 (PREADDR_REG_0_0_0_VTDBAR)—Offset E8h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.28 (PREUADDR_REG_0_0_0_VTDBAR)—Offset ECh

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.6.29 (FRCDL_REG_0_0_0_VTDBAR)—Offset 400h

Register used for GT save/restore definition in PUNIT It is just the whole qword used as a single field.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW	**Data**

7.6.30 (FRCDH_REG_0_0_0_VTDBAR)—Offset 408h

Register used for GT save/restore definition in PUNIT It is just the whole qword used as a single field.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW	**Data**

7.6.31 (IVA_REG_0_0_0_VTDBAR)—Offset 500h

Register used for GT save/restore definition in PUNIT It is just the whole qword used as a single field.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW	**Data**

7.6.32 (IOTLB_REG_0_0_0_VTDBAR)—Offset 508h

Register used for GT save/restore definition in PUNIT It is just the whole qword used as a single field.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW	**Data**

7.6.33 (INTRTADDR_0_0_0_VTDBAR)—Offset F00h

Register used for GT save/restore definition in PUNIT It is just the whole qword used as a single field.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW	**Data**

7.6.34 (INTIRTA_0_0_0_VTDBAR)—Offset F08h

Register used for GT save/restore definition in PUNIT It is just the whole qword used as a single field.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW	**Data**

7.7 Registers Summary

Table 7-7. Summary of pcs_regs Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
42060h	42063h	(RM_TIMEOUT)—Offset 42060h	0h
42400h	42403h	Display Engine Power1 (DE_POWER1)—Offset 42400h	0h
42404h	42407h	Display Engine Power2 (DE_POWER2)—Offset 42404h	0h
44074h	44077h	(TIMESTAMP_OVERRIDE)—Offset 44074h	0h
44200h	44203h	(MASTER_INT_CTL)—Offset 44200h	0h
44444h	44447h	Display Engine Port Interrupts (DE_PORT_INTERRUPT_IMR)—Offset 44444h	CF80003Bh
4444Ch	4444Fh	Display Engine Port Interrupts (DE_PORT_INTERRUPT_IER)—Offset 4444Ch	0h
444E4h	444E7h	(PCU_INTERRUPT_IMR)—Offset 444E4h	0h
444ECh	444EFh	(PCU_INTERRUPT_IER)—Offset 444ECh	0h
45004h	45007h	Display Arbitration Control 2 (ARB_CTL2)—Offset 45004h	E80h
45280h	45283h	(WM_DBG)—Offset 45280h	0h
45504h	45507h	(DC_STATE_EN)—Offset 45504h	0h
45520h	45523h	(DC_STATE_DEBUG)—Offset 45520h	0h
46408h	4640Bh	(NDE_RSTWRN_OPT)—Offset 46408h	0h
46530h	46533h	(CLKGATE_DIS_0)—Offset 46530h	0h
46534h	46537h	(CLKGATE_DIS_MISC)—Offset 46534h	0h
50210h	50213h	(MSG_PCU_INT)—Offset 50210h	0h
50400h	50403h	(KVMR1)—Offset 50400h	0h

Table 7-7. Summary of pcs_regs Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
50800h	50803h	(PAVP1)—Offset 50800h	0h
50804h	50807h	(PAVP2)—Offset 50804h	0h
51008h	5100Bh	(DFSM2)—Offset 51008h	0h
5100Ch	5100Fh	(DFSM3)—Offset 5100Ch	0h
8F0E0h	8F0E3h	DMC RMBUS Trap (DMC_RMBUS_TRAP)—Offset 8F0E0h	0h
C4030h	C4033h	(HOTPLUG_CTL)—Offset C4030h	0h
C4034h	C4037h	(HPD_PULSE_CNT_B)—Offset C4034h	0h
C4038h	C403Bh	(HPD_FILTER_CNT)—Offset C4038h	0h
C4044h	C4047h	(HPD_PULSE_CNT_C)—Offset C4044h	0h
C404Ch	C404Fh	(HPD_PULSE_CNT_A)—Offset C404Ch	0h
130094h	130097h	(GSADBG)—Offset 130094h	0h
1300B0h	1300B3h	(GSA_AUDIO_BDF)—Offset 1300B0h	0h
1300B4h	1300B7h	(GSA_TOUCH_BDF)—Offset 1300B4h	0h

7.7.1 (RM_TIMEOUT)—Offset 42060h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.2 Display Engine Power1 (DE_POWER1)—Offset 42400h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Power Well 2 State (POWER_WELL_2_STATE):** This field indicates the status of display power well 2.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RO	**Display Pipes enabled (DISPLAY_PIPES_ENABLED):** This field indicates if any display pipes are enabled.
29	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
28	0h RO	**Power Well 1 State (POWER_WELL_1_STATE):** This field indicates the status of display power well 1.
27:26	0h RO	**SRD Status (SRD_STATUS):** This field indicates the live status of the SRD link on eDP DDI-A
25	0h RO	**KVM Session Status (KVM_SESSION_STATUS):** This field indicates the status of KVM session.
24:13	0h RO	**RESERVED_1 (RESERVED_1):** Reserved
12:10	0h RO	**Enabled Pipe Scalers (ENABLED_PIPE_SCALERS):** The total number of pipe scalers enabled.
9:8	0h RO	**RESERVED_2 (RESERVED_2):** Reserved
7:4	0h RO	**Transmit Lanes Enabled (TRANSMIT_LANES_ENABLED):** The total number of DDI lanes enabled.
3	0h RO	**RESERVED_3 (RESERVED_3):** Reserved
2:0	0h RO	**Enabled DPLLs (ENABLED_DPLL):** The total number of Display PLLs enabled.

7.7.3 Display Engine Power2 (DE_POWER2)—Offset 42404h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**DE Bandwidth counter (DE_BANDWIDTH_COUNTER):** This counter increments on every cache line put arriving at the DE. The bandwidth is estimated by taking the difference between two reads at a known interval. Access is actually read/write variant. Writes to this register will load the write data into the counter. The GDR_DFT regisetr Hold_DE_POWER2 bit can be set to stop the count from incrementing.

7.7.4 (TIMESTAMP_OVERRIDE)—Offset 44074h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.5 (MASTER_INT_CTL)—Offset 44200h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.6 Display Engine Port Interrupts (DE_PORT_INTERRUPT_IMR)—Offset 44444h

This table indicates which events are mapped to each bit of the Display Engine Port Interrupt registers. The IER enabled Display Engine Port Interrupt IIR (sticky) bits are ORed together to generate the DE_Port Interrupts Pending bit in the Master Interrupt Control register. 0x44440 = ISR 0x44444 = IMR 0x44448 = IIR 0x4444C = IER

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: CF80003Bh

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**MIPI C (MIPI_C):** The ISR is an active high level indicating an interrupt is set in MIPIC_INTR_STAT_REG or MIPIC_INTR_STAT_REG_1.

Bit Range	Default & Access	Field Name (ID): Description
30	1h RW	**MIPI A (MIPI_A):** The ISR is an active high level indicating an interrupt is set in MIPIA_INTR_STAT_REG or MIPIA_INTR_STAT_REG_1.
29:28	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
27	1h RW	**AUX Channel D (AUX_CHANNEL_D):** The ISR is an active high pulse on the AUX DDI D done event. This event will not occur for SRD AUX done.
26	1h RW	**AUX Channel C (AUX_CHANNEL_C):** The ISR is an active high pulse on the AUX DDI C done event. This event will not occur for SRD AUX done.
25	1h RW	**AUX Channel B (AUX_CHANNEL_B):** The ISR is an active high pulse on the AUX DDI B done event. This event will not occur for SRD AUX done.
24	1h RW	**MIPI C TE (MIPI_C_TE):** The ISR is an active high pulse indicating a TE interrupt is set in MIPIC_STATUS.
23	1h RW	**MIPI A TE (MIPI_A_TE):** The ISR is an active high pulse indicating a TE interrupt is set in MIPIA_STATUS.
22:6	0h RO	**RESERVED_1 (RESERVED_1):** Reserved
5	1h RW	**DDI C Hotplug (DDI_C_HOTPLUG):** The ISR gives the live state of the DDI C HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled.
4	1h RW	**DDI B Hotplug (DDI_B_HOTPLUG):** The ISR gives the live state of the DDI B HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled.
3	1h RW	**DDI A Hotplug (DDI_A_HOTPLUG):** The ISR gives the live state of the DDI A HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled.
2	0h RO	**RESERVED_2 (RESERVED_2):** Reserved
1	1h RW	**GMBUS (GMBUS):** The ISR is an active high pulse when any of the unmasked events in GMBUS4 Interrupt Mask register occur.
0	1h RW	**AUX Channel A (AUX_CHANNEL_A):** The ISR is an active high pulse on the AUX DDI A done event. This event will not occur for SRD AUX done.

7.7.7 Display Engine Port Interrupts (DE_PORT_INTERRUPT_IER)—Offset 4444Ch

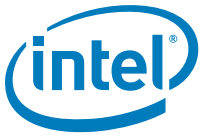
This table indicates which events are mapped to each bit of the Display Engine Port Interrupt registers. The IER enabled Display Engine Port Interrupt IIR (sticky) bits are ORed together to generate the DE_Port Interrupts Pending bit in the Master Interrupt Control register. 0x44440 = ISR 0x44444 = IMR 0x44448 = IIR 0x4444C = IER

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**MIPI C (MIPI_C):** The ISR is an active high level indicating an interrupt is set in MIPIC_INTR_STAT_REG or MIPIC_INTR_STAT_REG_1.
30	0h RW	**MIPI A (MIPI_A):** The ISR is an active high level indicating an interrupt is set in MIPIA_INTR_STAT_REG or MIPIA_INTR_STAT_REG_1.
29:28	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
27	0h RW	**AUX Channel D (AUX_CHANNEL_D):** The ISR is an active high pulse on the AUX DDI D done event. This event will not occur for SRD AUX done.
26	0h RW	**AUX Channel C (AUX_CHANNEL_C):** The ISR is an active high pulse on the AUX DDI C done event. This event will not occur for SRD AUX done.
25	0h RW	**AUX Channel B (AUX_CHANNEL_B):** The ISR is an active high pulse on the AUX DDI B done event. This event will not occur for SRD AUX done.
24	0h RW	**MIPI C TE (MIPI_C_TE):** The ISR is an active high pulse indicating a TE interrupt is set in MIPIC_STATUS.
23	0h RW	**MIPI A TE (MIPI_A_TE):** The ISR is an active high pulse indicating a TE interrupt is set in MIPIA_STATUS.
22:6	0h RO	**RESERVED_1 (RESERVED_1):** Reserved
5	0h RW	**DDI C Hotplug (DDI_C_HOTPLUG):** The ISR gives the live state of the DDI C HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled.
4	0h RW	**DDI B Hotplug (DDI_B_HOTPLUG):** The ISR gives the live state of the DDI B HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled.



Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**DDI A Hotplug (DDI_A_HOTPLUG):** The ISR gives the live state of the DDI A HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled.
2	0h RO	**RESERVED_2 (RESERVED_2):** Reserved
1	0h RW	**GMBUS (GMBUS):** The ISR is an active high pulse when any of the unmasked events in GMBUS4 Interrupt Mask register occur.
0	0h RW	**AUX Channel A (AUX_CHANNEL_A):** The ISR is an active high pulse on the AUX DDI A done event. This event will not occur for SRD AUX done.

7.7.8 (PCU_INTERRUPT_IMR)—Offset 444E4h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.9 (PCU_INTERRUPT_IER)—Offset 444ECh

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.10 Display Arbitration Control 2 (ARB_CTL2)—Offset 45004h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: E80h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VRH Memory Wake (VRH_MEMORY_WAKE)**
30	0h RO	**Reserved (RSVD_0)**
29:28	0h RW	**LP WD Write Request Limit (LP_WD_WRITE_REQUEST_LIMIT)**
27:14	0h RO	**Reserved (RSVD_1)**
13	0h RW	**Decomp CCS PAVP Enc (DECOMP_CCS_PAVP_ENC)**
12	0h RW	**Arbiter Trickle Feed Allow on HP Request (ARB_TRICKLE_ALLOW_HP)**
11	1h RW	**Audio Memory Wake (AUDIO_MEMORY_WAKE)**
10:9	3h RW	**Inflight LP Read Request Limit (LP_RD_REQUEST_LIMIT)**
8	0h RO	**Reserved (RSVD_2)**
7	1h RW	**LP Read Write Arb (LP_READ_WRITE_ARB)**
6	0h RO	**Reserved (RSVD_3)**
5:4	0h RW	**Inflight HP Read Request Limit (HP_RD_REQUEST_LIMIT)**
3	0h RW	**Enable IPC (ENABLE_IPC):** Enables the Isochronous Priority Control. If enabled, Display sends demoted requests once the transition watermark is reached. If transition watermark is not enabled, Display sends demoted requests when the display buffer is full. 0b - Disable, 1b - Enable
2	0h RO	**Reserved (RSVD_4)**
1:0	0h RW	**RTID FIFO Watermark (RTID_FIFO_WM)**

7.7.11 (WM_DBG)—Offset 45280h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.12 (DC_STATE_EN)—Offset 45504h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.13 (DC_STATE_DEBUG)—Offset 45520h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.14 (NDE_RSTWRN_OPT)—Offset 46408h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.15 (CLKGATE_DIS_0)—Offset 46530h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.16 (CLKGATE_DIS_MISC)—Offset 46534h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.17 (MSG_PCU_INT)—Offset 50210h

Access: Sent from PCU to North Display. This message is used to forward PCU interrupts to Display Engine. A message received with a 1b in a data bit will indicate an interrupt event occurred. This message is also known as the PCU Interrupt Message (PIM).

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h WO	**PCU_Interrupts**

7.7.18 (KVMR1)—Offset 50400h

KVMR1

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RW	**KVMR1**
3:0	0h RSV	**RESERVED**

7.7.19 (PAVP1)—Offset 50800h

PAVP1

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**PAVP1**

7.7.20 (PAVP2)—Offset 50804h

PAVP2

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**PAVP2**

7.7.21 (DFSM2)—Offset 51008h

This register contains fuse and strap settings for display. This register is not reset by a debug reset or FLR. Access is RO_FW. Only writes from PCU (cfgspace 0x11111 and srcID 0x10) to Display on the message channel will update the register value. Writes from other sources will complete normally without updating the value. Any source can read the register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Bank_1_EBB_Trim_data**
15:0	0h RW	**Bank_0_EBB_Trim_data**

7.7.22 (DFSM3)—Offset 5100Ch

This register contains fuse and strap settings for display. This register is not reset by a debug reset or FLR. Access is RO_FW. Only writes from PCU (cfgspace 0x11111 and srcID 0x10) to Display on the message channel will update the register value. Writes from other sources will complete normally without updating the value. Any source can read the register.

Access Method

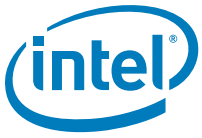
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Bank_3_EBB_Trim_data**
15:0	0h RW	**Bank_2_EBB_Trim_data**

7.7.23 DMC RMBUS Trap (DMC_RMBUS_TRAP)—Offset 8F0E0h

This register controls the RMBUS trapping.



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RMBUS Trap Enable (RMBUS_TRAP_ENABLE):** This field enables the RMBUS trap. 0b - Disable, 1b - Enable
30	0h RW	**Trap Delayed Arm (TRAP_DELAYED_ARM)**
29	0h RW	**Trap Discard (TRAP_DISCARD)**
28	0h RW	**Trap Address Type (TRAP_ADDRESS_TYPE)**
27	0h RW	**Wait Clear (WAIT_CLEAR)**
26:20	0h RO	**Reserved (RSVD_0)**
19:2	0h RW	**Trap Address (TRAP_ADDRESS)**
1:0	0h RO	**Reserved (RSVD_1)**

7.7.24 (HOTPLUG_CTL)—Offset C4030h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.25 (HPD_PULSE_CNT_B)—Offset C4034h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.26 (HPD_FILTER_CNT)—Offset C4038h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.27 (HPD_PULSE_CNT_C)—Offset C4044h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.28 (HPD_PULSE_CNT_A)—Offset C404Ch

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.29 (GSADBG)—Offset 130094h

Access is RO_FW. Only writes from non-IA sources (srcID not 0x00) will update the register value. Writes from other sources will complete normally without updating the value. Any source can read the register. This register is not reset by the device 2 FLR.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GSADBG**

7.7.30 (GSA_AUDIO_BDF)—Offset 1300B0h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

7.7.31 (GSA_TOUCH_BDF)—Offset 1300B4h

Register used for GT save/restore definition in PUNIT It is just the whole dword used as a single field.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data**

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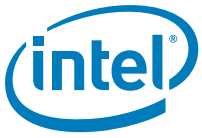

8 MDSI

8.1 Registers Summary

Table 8-1. Summary of pcs_regs Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
10h	13h	LJPLL_RW_CONTROL_1 (LJPLL_CR_RW_CONTROL_1)—Offset 10h	0h
14h	17h	LJPLL_RW_CONTROL_2 (LJPLL_CR_RW_CONTROL_2)—Offset 14h	0h
20h	27h	dsipll_cp (dsipll_cp)—Offset 20h	40001200211h
28h	2Fh	dsipll_rac (dsipll_rac)—Offset 28h	40001200211h
30h	37h	dsipll_wac (dsipll_wac)—Offset 30h	40001200211h

8.1.1 LJPLL_RW_CONTROL_1 (LJPLL_CR_RW_CONTROL_1)—Offset 10h

LJPLL CR

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**SSC_FRAC_STEP (SSC_FRAC_STEP):** ssc fraction step
7:0	0h RW	**SSC_RATIO_STEP (SSC_RATIO_STEP):** SSC ratio step

8.1.2 LJPLL_RW_CONTROL_2 (LJPLL_CR_RW_CONTROL_2)—Offset 14h

LJPLL CR

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**PLL_RSVD_1 (PLL_RSVD_1):** PLL Rsvd
11:10	0h RW	**SSC_MODE (SSC_MODE):** SSC mode select
9	0h RW	**SSC_EN (SSC_EN):** SSC enable
8:0	0h RW	**SSC_CYC_TO_PEAK_M1 (SSC_CYC_TO_PEAK_M1):** Ssc cycle to peak

8.1.3 dsipll_cp (dsipll_cp)—Offset 20h

Policy DSIPLL_POLICY_GROUP CP Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001200211h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001200211h RW	**sai[63:0] (sai)**

8.1.4 dsipll_rac (dsipll_rac)—Offset 28h

Policy DSIPLL_POLICY_GROUP RAC Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001200211h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001200211h RW	**sai[63:0] (sai)**

8.1.5 dsipll_wac (dsipll_wac)—Offset 30h

Policy DSIPLL_POLICY_GROUP WAC Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 40001200211h

Bit Range	Default & Access	Field Name (ID): Description
63:0	40001200211h RW	**sai[63:0] (sai)**

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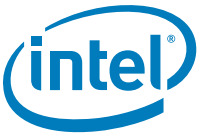


9 System Agent

9.1 Registers Summary

Table 9-1. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
48h	4Bh	B-Unit Copy of the MCHBAR (B_CR_MCHBAR_LO_0_0_0_PCI)—Offset 48h	FDFF8001h
4Ch	4Fh	B-Unit Copy of the MCHBAR (B_CR_MCHBAR_HI_0_0_0_PCI)—Offset 4Ch	0h
50h	51h	B-Unit Shadow of GGC (B_CR_GGC_0_0_0_PCI)—Offset 50h	0h
54h	57h	B-Unit Shadow of the DEVEN Register (B_CR_DEVEN_0_0_0_PCI)—Offset 54h	33h
60h	63h	B-Unit PCI Express Enhanced Configuration Range Base Address Low (B_CR_PCIEXBAR_LO_0_0_0_PCI)—Offset 60h	0h
64h	67h	B-Unit PCI Express Enhanced Configuration Range Base Address High (B_CR_PCIEXBAR_HI_0_0_0_PCI)—Offset 64h	0h
A8h	ABh	Top of Upper Usable DRAM Low (B_CR_TOUUD_LO_0_0_0_PCI)—Offset A8h	0h
ACh	AFh	Top of Upper Usable DRAM High (B_CR_TOUUD_HI_0_0_0_PCI)—Offset ACh	1h
B4h	B7h	Base of Graphics Stolen Memory (B_CR_BGSM_0_0_0_PCI)—Offset B4h	0h
B8h	BBh	B-Unit Copy of the TSEG Memory Base (B_CR_TSEGMB_0_0_0_PCI)—Offset B8h	100000h
BCh	BFh	Top of Lower Usable DRAM (B_CR_TOLUD_0_0_0_PCI)—Offset BCh	40000000h
E4h	E7h	Capability ID0 A (B_CR_CAPID0_A_0_0_0_PCI)—Offset E4h	0h
E8h	EBh	Capability ID0 B (B_CR_CAPID0_B_0_0_0_PCI)—Offset E8h	0h

9.1.1 B-Unit Copy of the MCHBAR (B_CR_MCHBAR_LO_0_0_0_PCI)—Offset 48h

This register contains the lower 32bits of the MCHBAR.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: FDFF8001h

Bit Range	Default & Access	Field Name (ID): Description
31:15	1FBFFh RW	**Base Address of MCHBAR (BASE_ADDR):** Defines the base address of the MCHBAR. MCHBAR[38:15] is {MCHBAR_HI[6:0],MCHBAR_LO[31:15]}. If incoming Request Address[38:15] matches MCHBAR[38:15] then request hits an address in the MCHBAR range.

Bit Range	Default & Access	Field Name (ID): Description
14:4	0h RO	**Base Address Not Implemented (BASE_ADDR_NOT_IMPLEMENTED):** Hardwired to 0 to indicate size of BAR 32kB.
3:1	0h RO	**Reserved (RESERVED_0):** Prefetchable space.
0	1h RW	**MCHBAR Enable (MCHBAREN):** • 0: MCHBAR is disabled and does not claim any memory • 1: MCHBAR memory mapped accesses are claimed and decoded appropriately

9.1.2 B-Unit Copy of the MCHBAR (B_CR_MCHBAR_HI_0_0_0_PCI)—Offset 4Ch

This register contains the upper 32 bits of the MCHBAR.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RESERVED_0):** Reserved.
6:0	0h RW	**Base Address of MCHBAR (BASE_ADDR):** Defines the base address of the MCHBAR. If incoming Request Address[38:15] matches MCHBAR[38:15], then request hits an address in the MCHBAR range.

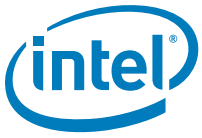
9.1.3 B-Unit Shadow of GGC (B_CR_GGC_0_0_0_PCI)—Offset 50h

B-Unit shadow of the GMCH Graphics Control Register.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 0 **Function:** 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Graphics Memory Select (GMS):** This field is used to select the amount of Main Memory that is preallocated to support the Internal Graphics device in VGA nonlinear and Native linear modes. The BIOS ensures that memory is preallocated only when Internal graphics is enabled. This register is also Intel TXT lockable. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD bit 1 of this register is 0. • 00h:0MB • 01h:32MB • 02h:64MB • 03h:96MB • 04h:128MB • 05h:160MB • 06h:192MB • 07h:224MB • 08h:256MB • 09h:288MB • 0Ah:320MB • 0Bh:352MB • 0Ch:384MB • 0Dh:416MB • 0Eh:448MB • 0Fh:480MB • 10h:512MB • 20h:...1024MB... • 30h:...1536MB... • 3Fh:...2016MB • 40h-FFh:Illegal value
7:6	0h RW	**Size of Graphics Translation Table Memory (GGMS):** This field is used to select the amount of Main Memory that is preallocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is preallocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. 0x0:No Preallocated Memory 0x1:2MB of Preallocated Memory 0x2:4MB of Preallocated Memory 0x3:8MB of Preallocated Memory
5:3	0h RO	**Reserved (RESERVED_0):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Versatile Acceleration Mode Enable (VAMEN):** Enables the use of the iGFX enbines for Versatile Acceleration. • 1: iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. • 0: iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
1	0h RW/L	**IGA VGD Disable (IVD):** • 0: Enable. Device 2 IGD claims VGA memory and IO cycles, and the SubClass Code within Device 2 Class Code register is 00. • 1: Disable. Device 2 IGD does not claim VGA cycles Mem and IO, and the Sub Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field bits 7:3 of this register preallocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override B_CR_CAPID0_A[IGD] 1 or via a register DEVEN[3] 0. This register is locked by Intel TXT lock.
0	0h RW	**GGCLCK (GGCLCK):** Reserved. Unused by the B-Unit.

9.1.4 B-Unit Shadow of the DEVEN Register (B_CR_DEVEN_0_0_0_PCI)—Offset 54h

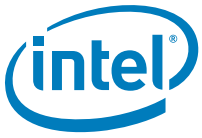
The DEVEN register allows for enabling/disabling of PCI devices and functions that are within the CPU package.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 33h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved (RESERVED_1):** Reserved.
5	1h RW	**Device 3 Function 0 Enable (D3F0EN):** • 0: Bus 0 Device 3 Function 0 is disabled and hidden • 1: Bus 0 Device 3 Function 0 is enabled and visible This bit will be set to 0b and remain 0b if Device 3 capability is disabled.
4	1h RW	**Device 2 Function 0 Enable (D2F0EN):** • 0: Bus 0 Device 2 Function 0 is disabled and hidden • 1: Bus 0 Device 2 Function 0 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled.
3:2	0h RO	**Reserved (RESERVED_0):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
1	1h RW	**Device 0 Function 1 Enable (D0F1EN):** • 0: Bus 0 Device 1 Function 0 is disabled and hidden • 1: Bus 0 Device 1 Function 0 is enabled and visible This bit will be set to 0b and remain 0b if Device 0/0/1 capability is disabled.
0	1h RO	**Device 0 Function 0 Enable (D0F0EN):** Bus 0 Device 0 Function 0 may not be disabled, and is therefore hardwired to 1.

9.1.5 B-Unit PCI Express Enhanced Configuration Range Base Address Low (B_CR_PCIEXBAR_LO_0_0_0_PCI)—Offset 60h

Defines the base address of the PCI Express Enhanced Configuration region. This register contains the lower 32bits of PCIEXBAR.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**PCI Express Base Address (PCIEXBAR):** PCIEXBAR[38:28] is {PCIEXBAR_HI[6:0],PCIEXBAR_LO[31:28]}. Describes bits [38:28] of the base address of the contiguous 256MB region for PCI Express Enhanced Configuration region. If bits [38:28] of the request address matches the PCIEXBAR[38:28] then the request targets the PCI Express Enhanced Configuration Space region. A posted memory operation from an IDI agent will be treated as a nonposted operation by the T-Unit and A-Unit.
27	0h RO	**ADMSK128 (ADMSK128):** Reserved. Unused by SoC since PCIEXBAR is a fixed 256MB region in SoCs.
26	0h RO	**ADMSK64 (ADMSK64):** Reserved. Unused by SoC since PCIEXBAR is a fixed 256MB region in SoCs.
25:3	0h RO	**Reserved (RESERVED_1):** Reserved.
2:1	0h RO	**Length of the Region (LENGTH):** Reserved and set to 0 indicating a fixed 256 MB region.
0	0h RW	**PCIEXBAR Range Enable (PCIEXBAREN):** • 0: PCIEXBAR range is disabled. Address may target DRAM or MMIO, depending on other address decode rules. • 1: PCIEXBAR range is enabled. Incoming request address must be compared with PCIEXBAR to determine whether the request targets PCI Express Enhanced Configuration region.

9.1.6 B-Unit PCI Express Enhanced Configuration Range Base Address High (B_CR_PCIEXBAR_HI_0_0_0_PCI)—Offset 64h

Defines part of the base address of the PCI Express Enhanced Configuration region. See bit field description.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RESERVED_0):** Reserved.
6:0	0h RW	**PCI Express Base Address (PCIEXBAR):** PCIEXBAR[38:28] is {PCIEXBAR_HI[6:0],PCIEXBAR_LO[31:28]}. Describes bits [38:28] of the base address of the contiguous 256MB region for PCI Express Enhanced Configuration region. If bits [38:28] of the request address matches the PCIEXBAR[38:28] then the request targets the PCI Express Enhanced Configuration Space region. A posted memory operation from an IDI agent will be treated as a nonposted operation by the T-unit and A-unit.

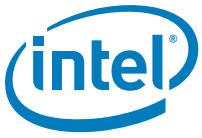
9.1.7 Top of Upper Usable DRAM Low (B_CR_TOUUD_LO_0_0_0_PCI)—Offset A8h

Defines the top of the upper usable DRAM range and start of the upper MMIO address range. Formerly defined in BMBOUND_HI. This register contains the lower 32 bits of TOUUD.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Top of Upper Usable DRAM (TOUUD):** TOUUD[38:20] is {TOUUD_HI[6:0],TOUUD_LO[31:20]}. Upper usable DRAM address range ends at the preceding byte. Upper MMIO Range starts at this address and extends up to the maximum system addressable memory range. Bits 38:20 are compared with bits 38:20 of the incoming request address to determine whether the request targets the upper usable DRAM range or upper MMIO range. If Request Address[38:20]>=TOUUD[38:20] and any bit in Request Address[38:32] is set, request is determined to target the upper MMIO range.
19:1	0h RO	**Reserved (RESERVED_1):** Reserved.
0	0h RW	**LOCK (LOCK):** Reserved. Lock is unused by B-Unit. Register overwrites are protected via SAI access control policy registers.

9.1.8 Top of Upper Usable DRAM High (B_CR_TOUUD_HI_0_0_0_PCI)—Offset ACh

Defines the top of the upper usable DRAM range and start of the upper MMIO address range. Formerly defined in BMBOUND_HI. This register contains the upper 32 bits of TOUUD.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RESERVED_0):** Reserved.
6:0	1h RW	**Top of Upper Usable DRAM (TOUUD):** TOUUD[38:20] is {TOUUD_HI[6:0],TOUUD_LO[31:20]}. Upper usable DRAM address range ends at the preceding byte. Upper MMIO Range starts at this address and extends up to the maximum system addressable memory range. Bits 38:20 are compared with bits 38:20 of the incoming request address to determine whether the request targets the upper usable DRAM range or upper MMIO range. If Request Address[38:20]>=TOUUD[38:20] and any bit in Request Address[38:32] is set, request is determined to target the upper MMIO range.

9.1.9 Base of Graphics Stolen Memory (B_CR_BGSM_0_0_0_PCI)—Offset B4h

Defines the Base of the Graphics Stolen Memory. In addition, the SMM range is defined to end at the preceding byte. See TSEGMB register.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Base of Graphics Stolen Memory (BGSM):** This register contains the base address of the Graphics Stolen Memory. The limit for the Graphics Stolen Memory is TOLUD-1. Incoming Request Address[31:20] is compared against BGSM[31:20] and TOLUD[31:20] to determine if the address falls in the range. The comparison check is as follows: BGSM[31:20]<=Address[31:20] && Address[31:20]<TOLUD[31:20] and Address[38:32]==0.
19:1	0h RO	**Reserved (RESERVED_0):** Reserved.
0	0h RW	**LOCK (LOCK):** Reserved. Lock is unused by B-Unit. Register overwrites are protected via SAI access control policy registers.

9.1.10 B-Unit Copy of the TSEG Memory Base (B_CR_TSEGMB_0_0_0_PCI)—Offset B8h

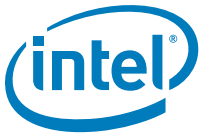
B-Unit copy of the TSEGMB. TSEGMB defines the base of the SMM range and the BGSM register defines the limit of the SMM range. Note: In prior SoCs the base register was defined in SMMRRL register and the limit was defined in the SMMRRH register.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	1h RW	**Base address of TSEG DRAM Memory (TSEGMB):** BIOS determines the base of TSEG memory which must be at or below Graphics Base of GTT Stolen Memory BGSM. SMM range starts at this base and ends at BGSM1. Incoming Request Address [31:20] will be compared with TSEGMB[31:20] and BGSM[31:20] to determine if the request targets the SMM range. The comparison check is as follows: Address[31:20]>=TSEGMB[31:20] && Address[31:20]<BGSM[31:20] and Address[38:32]==0. If the check passes, the request targets the SMM range. If the protection for the range is enabled, then the request SAI is compared against allowed SAIs specified by BSMRRAC and BSMRWAC registers to determine if access is allowed.



Bit Range	Default & Access	Field Name (ID): Description
19:1	0h RO	**Reserved (RESERVED_0):** Reserved.
0	0h RW	**LOCK (LOCK):** Reserved. Lock is unused by B-Unit. Register overwrites are protected via SAI access control policy registers.

9.1.11 Top of Lower Usable DRAM (B_CR_TOLUD_0_0_0_PCI)—Offset BCh

This register defines the Top of Lower Usable DRAM range and start of the Lower MMIO Address range. Formerly defined in BMBOUND.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 40000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	400h RW	**Top of Lower Usable DRAM (TOLUD):** Defines the top of lower usable DRAM, which ends at the preceding byte. Lower MMIO Address range starts at this address and continues up to the 4GB Address 0xFFFF_FFFF. Bits 31:20 are compared with incoming request Address[31:20] to determine whether the request targets lower usable DRAM range or the lower MMIO range. If Request Address[31:20]>=TOLUD[31:20] and Request Address[38:32]==0 then the Request Address falls in the Lower MMIO Address range.
19:1	0h RO	**Reserved (RESERVED_0):** Reserved.
0	0h RW	**LOCK (LOCK):** Reserved. Lock is unused by B-Unit. Register overwrites are protected via SAI access control policy registers.

9.1.12 Capability ID0 A (B_CR_CAPID0_A_0_0_0_PCI)—Offset E4h

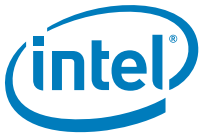
Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Spare 31-24 (SPARE31_24):** Reserved for future capabilities.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**VTd Disable (VTDD):** • 0: Enable VTd • 1: Disable VTd
22	0h RW	**Fuse Spare 22 (FUSE_SPARE22):** Fuse backed spare.
21	0h RW	**Fuse Spare 21 (FUSE_SPARE21):** Fuse backed spare.
20	0h RW	**Fuse Spare 20 (FUSE_SPARE20):** Fuse backed spare.
19	0h RW	**Fuse Spare 19 (FUSE_SPARE19):** Fuse backed spare.
18	0h RW	**Fuse Spare 18 (FUSE_SPARE18):** Fuse backed spare.
17	0h RW	**Fuse Spare 17 (FUSE_SPARE17):** Fuse backed spare.
16	0h RW	**Fuse Spare 16 (FUSE_SPARE16):** Fuse backed spare.
15	0h RW	**Camarillo DPTF Disable (CDD):** • 0: DPTF Camarillo associated memory spaces are accessible. • 1: DPTF Camarillo associated memory and IO spaces are disabled. DEVEN_0_0_0_PCI field for DPTF can not be set.
14	0h RW	**Fuse Spare 14 (FUSE_SPARE14):** Fuse backed spare.
13	0h RW	**Fuse Spare 13 (FUSE_SPARE13):** Fuse backed spare.
12	0h RW	**Fuse Spare 12 (FUSE_SPARE12):** Fuse backed spare.
11	0h RW	**Internal Graphics Disable (IGD):** • 0: There is a graphics engine within this CPU. Internal Graphics Device 2 is enabled, and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the CPU. All nonSMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2, IO registers within Device 2, and VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6, if PCI Express GFX attach is supported. A selected amount of Graphics Memory space is preallocated from the main memory, based on Graphics Mode Select GMS in the GGC Register. Graphics Memory is preallocated above TSEG Memory. • 1: There is no graphics engine within this CPU. Internal Graphics Device 2 and all of its memory and I/O functions are disabled. Configuration cycles targeted to Device 2 will be passed on to DMI. In addition, all clocks to internal graphics logic are turned off. All nonSMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6. DEVEN [4:3] Device 0 offset 54h have no meaning. Device 2 Functions 0 and 1 are disabled and hidden.



Bit Range	Default & Access	Field Name (ID): Description
10	0h RO	**Device ID Override Enable (DIDOE):** Controls if there is an override of Dev2 GFX device ID. • 0: Disable ability to override DID -- For production • 1: Enable ability to override DID -- For debug and samples only
9:8	0h RO	**Control Device ID Value (CDID):** Controls the value of Dev2 GFX device ID. Identifier assigned to the core/primary PCI device.The corresponding two bit capability ID programming is: • 00: Desktop • 01: Mobile • 10: Server • 11: Marketing Spare
7:0	0h RW	**Spare 7-0 (SPARE7_0):** Reserved for future capabilities.

9.1.13 Capability ID0 B (B_CR_CAPID0_B_0_0_0_PCI)—Offset E8h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Imaging Unit Memory/IO Disable (IMGU_DIS):** • 0: Imaging Unit associated memory spaces are accessible. • 1: Imaging Unit associated memory and IO spaces are disabled. DEVEN_0_0_0_PCI field for Iunit can not be set.
30	0h RW	**Fuse Spare 30 (FUSE_SPARE30):** Fuse backed spare.
29	0h RW	**Fuse Spare 29 (FUSE_SPARE29):** Fuse backed spares potentially to be used for PKGTYP encoding.
28	0h RW	**Fuse Spare 28 (FUSE_SPARE28):** Fuse backed spares potentially to be used for PKGTYP encoding.
27	0h RW	**Fuse Spare 27 (FUSE_SPARE27):** Fuse backed spares potentially to be used for PKGTYP encoding.
26	0h RW	**Fuse Spare 26 (FUSE_SPARE26):** Fuse backed spares potentially to be used for PKGTYP encoding.
25	0h RW	**Fuse Spare 25 (FUSE_SPARE25):** Fuse backed spares potentially to be used for PKGTYP encoding.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**SVM Disable (SVMDIS):** • 0: Enable SVM mode • 1: Disable SVM mode
23:0	0h RW	**Spare 23-0 (SPARE23_0):** Reserved for future capabilities.

9.2 Registers Summary

Table 9-2. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4h	5h	B-Unit Copy of PCICMD for IGD (B_CR_PCICMD_0_2_0_PCI)—Offset 4h	0h
10h	13h	B-Unit Copy of GTTMMADR (B_CR_GTTMMADR_LO_0_2_0_PCI)—Offset 10h	4h
14h	17h	B-Unit Copy of GTTMMADR (B_CR_GTTMMADR_HI_0_2_0_PCI)—Offset 14h	0h
18h	1Bh	B-Unit Copy of GMADR (B_CR_GMADR_LO_0_2_0_PCI)—Offset 18h	4h
1Ch	1Fh	B-Unit Copy of GMADR (B_CR_GMADR_HI_0_2_0_PCI)—Offset 1Ch	0h
20h	23h	B-Unit Copy of the IOBAR (B_CR_IOBAR_0_2_0_PCI)—Offset 20h	1h
58h	58h	B-Unit Copy of Device 2 Control Register (B_CR_DEV2CTL_0_2_0_PCI)—Offset 58h	0h
62h	62h	B-Unit Copy of MSAC (B_CR_MSAC_0_2_0_PCI)—Offset 62h	1h
78h	79h	B-Unit Copy of Device 2 Control Register (B_CR_DEVICECTL_0_2_0_PCI)—Offset 78h	0h
D4h	D5h	B-Unit Copy of PMCS for IGD (B_CR_PMCS_0_2_0_PCI)—Offset D4h	0h

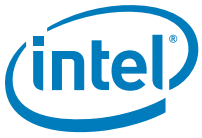
9.2.1 B-Unit Copy of PCICMD for IGD (B_CR_PCICMD_0_2_0_PCI)—Offset 4h

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved (RESERVED_0):** Reserved.
10	0h RW/V	**INTx Disable (INTDIS):** This bit disables the device from asserting INTx. • 0: Enable the assertion of this devices INTx signal. • 1: Disable the assertion of this devices INTx signal. DO_INTx messages will not be sent to DMI.
9	0h RO	**FB2B (FB2B):** Not Implemented. Hardwired to 0.



Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**SEN (SEN):** Not Implemented. Hardwired to 0.
7	0h RO	**WCC (WCC):** Not Implemented. Hardwired to 0.
6	0h RO	**PER (PER):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives the IGD ignores any parity error that it detects and continues with normal operation.
5	0h RO	**VPS (VPS):** This bit is hardwired to 0 to disable snooping.
4	0h RO	**MWIE (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	0h RO	**SCE (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	0h RW/V	**BME (BME):** • 0: Disable IGD bus mastering. • 1: Enable the IGD to function as a PCI compliant master. .
1	0h RW/V	**MAE (MAE):** This bit controls the IGD's response to memory space accesses. • 0: Disable. • 1: Enable. Device 2 Function Level Reset must reset this bit.
0	0h RW/V	**IOAE (IOAE):** This bit controls the IGD's response to I/O space accesses. • 0: Disable. • 1: Enable. Device 2 Function Level Reset must reset this bit.

9.2.2 B-Unit Copy of GTTMMADR (B_CR_GTTMMADR_LO_0_2_0_PCI)—Offset 10h

This register contains the lower 32 bits of GTTMMADR.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V	**Memory Base Address (MBA):** GTTMMADR[38:24] is {GTTMMADR_HI[6:0],GTTMMADR_LO[31:24]}. These bits, which are set by the OS, correspond to address signals [38:24]. 16MB combined for MMIO and Global GTT table aperture. 2MB are for MMIO, 6MB are reserved and 8 MB are for GTT.

Bit Range	Default & Access	Field Name (ID): Description
23:4	0h RO	**Address Mask (ADM):** Hardwired to 0s to indicate at least 16MB address range.
3	0h RO	**Prefetch Memory Enable (PREFMEM):** Hardwired to 0 to prevent prefetching.
2:1	2h RO	**Memory Base Address Type (MEMTYP):** • 00: To indicate 32 bit base address • 01: Reserved • 10: To indicate 64 bit base address • 11: Reserved
0	0h RO	**Memory or IO Space (MIOS):** Hardwired to 0 to indicate memory space.

9.2.3 B-Unit Copy of GTTMMADR (B_CR_GTTMMADR_HI_0_2_0_PCI)—Offset 14h

This register contains the upper 32 bits of GTTMMADR.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RESERVED_0):** Reserved. Must be set to 0 since addressing above 512GB is not supported.
6:0	0h RW/V	**Memory Base Address (MBA):** These bits are set by the OS, and correspond to address signals [38:24]. 16MB combined for MMIO and Global GTT table aperture. 2MB are for MMIO, 6MB are reserved and 8 MB are for GTT.

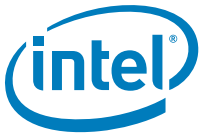
9.2.4 B-Unit Copy of GMADR (B_CR_GMADR_LO_0_2_0_PCI)—Offset 18h

This register contains the lower 32 bits of GMADR.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Memory Base Address or Address Map 4096 (ADMSK4096):** This Bit is either part of the Memory Base Address R/W, or part of the Address Mask RO, depending on the value of MSAC[4:0].
30	0h RW/V	**Memory Base Address or Address Map 2048 (ADMSK2048):** This Bit is either part of the Memory Base Address R/W, or part of the Address Mask RO, depending on the value of MSAC[4:0].
29	0h RW/V	**Memory Base Address or Address Map 1024 (ADMSK1024):** This Bit is either part of the Memory Base Address R/W, or part of the Address Mask RO, depending on the value of MSAC[4:0].
28	0h RW/V	**Memory Base Address or Address Map 512 (ADMSK512):** This Bit is either part of the Memory Base Address R/W, or part of the Address Mask RO, depending on the value of MSAC[4:0].
27	0h RW/V	**Memory Base Address or Address Map 256 (ADMSK256):** This Bit is either part of the Memory Base Address R/W, or part of the Address Mask RO, depending on the value of MSAC[4:0].
26:4	0h RO	**Address Mask (ADM):** Hardwired to 0s to indicate at least 128MB address range.
3	0h RO	**Prefetch Memory Enable (PREFMEM):** Hardwired to 0 to prevent prefetching.
2:1	2h RO	**Memory Base Address Type (MEMTYP):** • 00: To indicate 32 bit base address • 01: Reserved • 10: To indicate 64 bit base address • 11: Reserved
0	0h RO	**Memory or IO Space (MIOS):** Hardwired to 0 to indicate memory space.

9.2.5 B-Unit Copy of GMADR (B_CR_GMADR_HI_0_2_0_PCI)—Offset 1Ch

This register contains the upper 32 bits of GMADR.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RESERVED_0):** Reserved. Must be set to 0 since addressing above 512GB is not supported.
6:0	0h RW/V	**Memory Base Address (MBA):** These bits are set by the OS, and correspond to address signals [38:32].

9.2.6 B-Unit Copy of the IOBAR (B_CR_IOBAR_0_2_0_PCI)—Offset 20h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 2 **Function:** 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RESERVED_1):** Reserved.
15:6	0h RW/V	**IO Base Address Register Select (IOBASE):** These bits correspond to address signals [15:6]. If there is a match then address hits the IOBAR. Device 2 FLR must reset this field.
5:3	0h RO	**Reserved (RESERVED_0):** Reserved.
2:1	0h RO	**Memory Base Address Type (MEMTYPE):** Hardwired to 0s to indicate 32bit address.
0	1h RO	**Memory or IO Space (MIOS):** Hardwired to 1 to indicate IO space.

9.2.7 B-Unit Copy of Device 2 Control Register (B_CR_DEV2CTL_0_2_0_PCI)—Offset 58h

Access Method

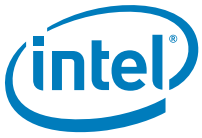
Type: CFG Register (Size: 8 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved (RESERVED_0):** Reserved.
0	0h RW/V	**IOBAR Disable (IOBARDIS):** System BIOS can choose to disable and hide the IOBAR for systems that do not require legacy IOBAR access to Gfx MMIO registers. • 0: IOBAR is enabled and exposed at offset 0x20 in Device 2 Configuration space. Default • 1: IOBAR is disabled and not visible in PCI Configuration Space. Behaves as if hardwired to zeros.

9.2.8 B-Unit Copy of MSAC (B_CR_MSAC_0_2_0_PCI)—Offset 62h

This data is used to determine the size of Aperture GMADR, and affects certain bits of the GMADR register.



Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 2 **Function:** 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved (RESERVED_0):** Reserved.
4	0h RW/V	**Aperture Size 4 (APSZ4):** Refer to description for APSZ0 [0:0].
3	0h RW/V	**Aperture Size 3 (APSZ3):** Refer to description for APSZ0 [0:0].
2	0h RW/V	**Aperture Size 2 (APSZ2):** Refer to description for APSZ0 [0:0].
1	0h RW/V	**Aperture Size 1 (APSZ1):** Refer to description for APSZ0 [0:0].
0	1h RW/V	**Aperture Size 0 (APSZ0):** This field is used in conjunction with other APSZ fields to determine the size of Aperture GMADR. It affects certain bits of the GMADR register. The description below is for all APSZ fields [4:0]: • 00000b: 128MB GMADR.B[26:4] is hardwired to 0. • 00001b: 256MB GMADR.B[27]=0, RO. • 00010b: illegal hardware will treat this as 00011. • 00011b: 512MB GMADR.B[28:27]=0, RO. • 00100b-00110b: illegal hardware will treat this as 00111. • 00111b: 1024MB GMADR.B[29:27]=0,RO. • 01000b-01110b: illegal hardware will treat this as 01111. • 01111b: 2048MB GMADR.B[30:27]=0,RO. • 10000b-11110b: illegal hardware will treat this as 11111. • 11111b: 4096MB GMADR.B[31:27]=0,RO

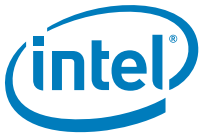
9.2.9 B-Unit Copy of Device 2 Control Register (B_CR_DEVICECTL_0_2_0_PCI)—Offset 78h

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/V	**Initiate Function Level Reset (INITIATE_FLR):** A write of 1b initiates Function Level Reset to the Function. The value read by software from this bit is always 0b. B-Unit uses only this bit for Dev2 FLR. The rest of the bits in this register are ignored by the B-Unit.
14:12	0h RO	**Max Read Request Size (MAX_READ_REQUEST_SIZE):** Functions that do not generate Read Requests larger than 128 bytes and Functions that do not generate Read Requests on their own behalf are permitted to implement this field as Read Only RO with a value of 000b.
11	0h RO	**Enable No Snoop (ENABLE_NO_SNOOP):** This bit is permitted to be hardwired to 0b if a function would never set the No Snoop attribute in transactions it initiates. The graphics device never generates a PCI Express TLP.
10	0h RO	**Aux Power PM Enable (AUX_PM_ENABLE):** Functions that do not implement this capability hardwire this bit to 0b.
9	0h RO	**Phantom Functions Enable (PHANTOM_FUNCTIONS_ENABLE):** Functions that do not implement this capability hardwire this bit to 0b.
8	0h RO	**Extended Tag Field Enable (EXTENDED_TAG_ENABLE):** Functions that do not implement this capability hardwire this bit to 0b.
7:5	0h RO	**Max Payload Size (MAX_PAYLOAD_SIZE):** Functions that support only the 128byte max payload size are permitted to hardwire this field to 000b.
4	0h RO	**Enable Relaxed Ordering (RO_ENABLE):** A Function is permitted to hardwire this bit to 0b if it never sets the Relaxed Ordering attribute in transactions it initiates as a Requester. The graphics device never generates a PCI Express TLP.
3	0h RO	**Unsupported Request Response Enable (UR_ENABLE):** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
2	0h RO	**Fatal Error Enable (FATAL_ERR_ENABLE):** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
1	0h RO	**NonFatal Error Enable (NONFATAL_ERR_ENABLE):** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
0	0h RO	**Correctable Error Enable (CORRECTABLE_ERR_ENABLE):** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.



9.2.10 B-Unit Copy of PMCS for IGD (B_CR_PMCS_0_2_0_PCI)—Offset D4h

This is the B-Unit Copy of the Power Management Control/Status Register for the Internal Graphics Device.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 2 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Power Management Event Status (PMESTS):** This bit is 0 to indicate that the Internal Graphics Device does not support Power Management Event generation from D3 (cold).
14:13	0h RO	**Data Scale (DSCALE):** The Internal Graphics Device does not support data register. This bit always returns 00 when read write operations have no effect.
12:9	0h RO	**Data Select (DSEL):** The IGD does not support data register. This bit always returns 0h when read write operations have no effect.
8	0h RO	**Power Management Event Enable (PMEEN):** This bit is 0 to indicate that PME assertion from D3 (cold) is disabled.
7:2	0h RO	**Reserved (RESERVED_1):** Reserved.
1:0	0h RW/V	**Power State (PWRSTAT):** This field indicates the current power state of the IGD, and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, the write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0, the graphics controller is optionally reset to initial values. • 00: D0 Default • 01: D1 Not Supported • 10: D2 Not Supported • 11: D3

9.3 Registers Summary

Table 9-3. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4h	5h	PCICMD for I-Unit in Device 3 Mode (B_CR_PCICMD_0_3_0_PCI)—Offset 4h	0h
10h	13h	B-Unit Copy of I-Unit BAR (B_CR_ISPMMADR_LO_0_3_0_PCI)—Offset 10h	4h
14h	17h	B-Unit Copy of I-Unit BAR (B_CR_ISPMMADR_HI_0_3_0_PCI)—Offset 14h	0h

Table 9-3. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
78h	79h	B-Unit Copy of Device 3 Control Register (B_CR_DEVICECTL_0_3_0_PCI)—Offset 78h	0h
D4h	D5h	B-Unit Copy of PMCS for I-Unit Device 0/3/0 (B_CR_PMCS_0_3_0_PCI)—Offset D4h	0h

9.3.1 PCICMD for I-Unit in Device 3 Mode (B_CR_PCICMD_0_3_0_PCI)—Offset 4h

B-Unit copy of PCICMD for I-Unit when operating in Device 3 mode.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 3 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved (RESERVED_0):** Reserved.
1	0h RW/V	**Memory Access Enable (MAE):** This bit controls the IGD's response to memory space accesses. • 0: Disable. • 1: Enable.
0	0h RW/V	**IO Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. • 0: Disable. • 1: Enable.

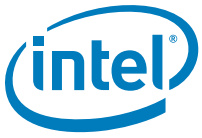
9.3.2 B-Unit Copy of I-Unit BAR (B_CR_ISPMMADR_LO_0_3_0_PCI)—Offset 10h

This register contains the lower 32 bits of I-Unit BAR, defined similarly to GTTMMADR.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V	**Memory Base Address (MBA):** ISPMMADR[38:24] is {ISPMMADR_HI[6:0],ISPMMADR_LO[31:24]}. These bits are set by the OS and correspond to address signals [38:24]. 16MB is the size of the ISPMMADR.
23:4	0h RO	**Address Mask (ADM):** Hardwired to zeros to indicate at least 16MB address range.
3	0h RO	**Prefetch Memory Enable (PREFMEM):** Hardwired to 0 to prevent prefetching.
2:1	2h RO	**Memory Base Address Type (MEMTYP):** • 00: To indicate 32 bit base address • 01: Reserved • 10: To indicate 64 bit base address • 11: Reserved
0	0h RO	**Memory or IO Space (MIOS):** Hardwired to zero, to indicate memory space.

9.3.3 B-Unit Copy of I-Unit BAR (B_CR_ISPMMADR_HI_0_3_0_PCI)—Offset 14h

This register contains the upper 32 bits of I-Unit BAR, defined similarly to GTTMMADR.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RESERVED_0):** Reserved. Must be set to 0 since addressing above 512GB is not supported.
6:0	0h RW/V	**Memory Base Address (MBA):** Upper bits of ISPMMADR[38:24].

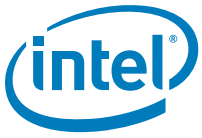
9.3.4 B-Unit Copy of Device 3 Control Register (B_CR_DEVICECTL_0_3_0_PCI)—Offset 78h

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 3 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/V	**Initiate Function Level Reset (INITIATE_FLR):** A write of 1b initiates Function Level Reset to the Function. The value read by software from this bit is always 0b. B-Unit uses only this bit for Dev3 FLR. The rest of the bits in this register are ignored by the B-Unit.
14:12	0h RO	**Max Read Request Size (MAX_READ_REQUEST_SIZE):** Functions that do not generate Read Requests larger than 128 bytes and Functions that do not generate Read Requests on their own behalf are permitted to implement this field as Read Only (RO) with a value of 000b.
11	0h RO	**Enable No Snoop (ENABLE_NO_SNOOP):** This bit is permitted to be hardwired to 0b if a Function would never set the 'No Snoop' attribute in transactions it initiates. The graphics device never generates a PCI Express TLP.
10	0h RO	**Aux Power PM Enable (AUX_PM_ENABLE):** Functions that do not implement this capability hardwire this bit to 0b.
9	0h RO	**Phantom Functions Enable (PHANTOM_FUNCTIONS_ENABLE):** Functions that do not implement this capability hardwire this bit to 0b.
8	0h RO	**Extended Tag Field Enable (EXTENDED_TAG_ENABLE):** Functions that do not implement this capability hardwire this bit to 0b.
7:5	0h RO	**Max Payload Size (MAX_PAYLOAD_SIZE):** Functions that support only the 128byte max payload size are permitted to hardwire this field to 000b.
4	0h RO	**Enable Relaxed Ordering (RO_ENABLE):** A Function is permitted to hardwire this bit to 0b if it never sets the Relaxed Ordering attribute in transactions it initiates as a Requester. The graphics device never generates a PCI Express TLP.
3	0h RO	**Unsupported Request Response Enable (UR_ENABLE):** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
2	0h RO	**Fatal Error Enable (FATAL_ERR_ENABLE):** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
1	0h RO	**Nonfatal Error Enable (NONFATAL_ERR_ENABLE):** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
0	0h RO	**Correctable Error Enable (CORRECTABLE_ERR_ENABLE):** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.



9.3.5 B-Unit Copy of PMCS for I-Unit Device 0/3/0 (B_CR_PMCS_0_3_0_PCI)—Offset D4h

This is the B-Unit copy of the Power Management Control/Status Register for I-Unit device 0/3/0.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 3 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved (RESERVED_1):** Reserved.
1:0	0h RW/V	**Power State (PWRSTAT):** This field indicates the current power state of the I-Unit, and can be used to set the I-Unit into a new power state. If software attempts to write an unsupported state to this field, the write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0, the I-Unit is optionally reset to initial values. • 00: D0 Default • 01: D1 Not Supported • 10: D2 Not Supported • 11: D3

9.4 Registers Summary

Table 9-4. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
80h	81h	B-Unit Copy of the I/O Decode Ranges Register for LPC (B_CR_IOD_LPC)—Offset 80h	0h
82h	83h	B-Unit Copy of the I/O Enables Register for LPC (B_CR_IOE_LPC)—Offset 82h	0h
84h	87h	B_LGIR1_LPC (B_CR_LGIR1_LPC)—Offset 84h	0h
88h	8Bh	B_LGIR2_LPC (B_CR_LGIR2_LPC)—Offset 88h	0h
8Ch	8Fh	B_LGIR3_LPC (B_CR_LGIR3_LPC)—Offset 8Ch	0h
90h	93h	B_LGIR4_LPC (B_CR_LGIR4_LPC)—Offset 90h	0h
98h	9Bh	B-Unit Copy of the LPC Generic Memory Range Register for LPC (B_CR_LGMR_LPC)—Offset 98h	0h
D8h	DBh	B-Unit Copy of the BIOS Decode Enable Register for LPC (B_CR_BDE_LPC)—Offset D8h	FFCFh

9.4.1 B-Unit Copy of the I/O Decode Ranges Register for LPC (B_CR_IOD_LPC)—Offset 80h

Affects B-Unit SAD for LPC regions.

Access Method

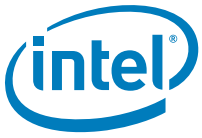
Type: CFG Register (Size: 16 bits)	**Device:** 31 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h RW/V	**FDD Range (FDD):** The following table describes which range to decode for the FDD Port. • 0 => 3F0h-3F5h, 3F7h (Primary) • 1 => 370h-375h, 377h (Secondary)
11:10	0h RO	Reserved.
9:8	0h RW/V	• Reserved
7	0h RO	Reserved.
6:4	0h RW/V	**ComB Range (CB):** The following table describes which range to decode for the ComB Port. • 000: 3F8h-3FFh (COM 1) • 001: 2F8h-2FFh (COM 2) • 010: 220h-227h • 011: 228h-22Fh • 100: 238h-23Fh • 101: 2E8h-2EFh (COM 4) • 110: 338h-33Fh • 111: 3E8h-3EFh (COM 3)
3	0h RO	Reserved.
2:0	0h RW/V	**ComA Range (CA):** The following table describes which range to decode for the ComA Port. • 000: 3F8h-3FFh (COM 1) • 001: 2F8h-2FFh (COM 2) • 010: 220h-227h • 011: 228h-22Fh • 100: 238h-23Fh • 101: 2E8h-2EFh (COM 4) • 110: 338h-33Fh • 111: 3E8h-3EFh (COM 3)

9.4.2 B-Unit Copy of the I/O Enables Register for LPC (B_CR_IOE_LPC)—Offset 82h

Affects B-Unit SAD for LPC regions.



Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 31 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	Reserved.
9	0h RW/V	**High Gameport Enable (HGE):** Enables decoding of the I/O locations 208h to 20Fh to LPC.
8	0h RW/V	**Low Gameport Enable (LGE):** Enables decoding of the I/O locations 200h to 207h to LPC.
7:4	0h RO	Reserved.
3	0h RW/V	**Floppy Drive Enable (FDE):** Enables decoding of the FDD range to LPC. Range is selected by LIOD.FDE.
2	0h RW/V	**Parallel Port Enable (PPE)**
1	0h RW/V	**Com Port B Enable (CBE):** Enables decoding of the ComB range to LPC. Range is selected LIOD.CB.
0	0h RW/V	**Com Port A Enable (CAE):** Enables decoding of the ComA range to LPC. Range is selected LIOD.CA.

9.4.3 B_LGIR1_LPC (B_CR_LGIR1_LPC)—Offset 84h

B-Unit copy of the LPC Generic I/O Range #1 register for LPC. Affects B-Unit SAD for LPC regions.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 31 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW/V	**Address [7:2] Mask (ADDR_MASK_7_2):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RO	Reserved.
15:2	0h RW/V	**Address [15:2] (ADDR_15_2):** DWord-aligned address. Note that SoC does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW/V	**LPC Decode Enable (EN):** When this bit is set to '1', then the range specified in this register is enabled for decoding to LPC.

9.4.4 B_LGIR2_LPC (B_CR_LGIR2_LPC)—Offset 88h

B-Unit copy of the LPC Generic I/O Range #2 register for LPC. Affects B-Unit SAD for LPC regions.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 31 **Function:** 0

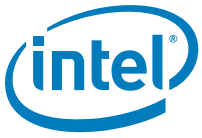
Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW/V	**Address [7:2] Mask (ADDR_MASK_7_2):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW/V	**Address [15:2] (ADDR_15_2):** DWord-aligned address. Note that SoC does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW/V	**LPC Decode Enable (EN):** When this bit is set to '1', then the range specified in this register is enabled for decoding to LPC.

9.4.5 B_LGIR3_LPC (B_CR_LGIR3_LPC)—Offset 8Ch

B-Unit copy of the LPC Generic I/O Range #3 register for LPC. Affects B-Unit SAD for LPC regions.

Access Method



Type: CFG Register (Size: 32 bits)	**Device:** 31 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW/V	**Address [7:2] Mask (ADDR_MASK_7_2):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW/V	**Address [15:2] (ADDR_15_2):** DWord-aligned address. Note that SoC does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW/V	**LPC Decode Enable (EN):** When this bit is set to '1', then the range specified in this register is enabled for decoding to LPC.

9.4.6 B_LGIR4_LPC (B_CR_LGIR4_LPC)—Offset 90h

B-Unit copy of the LPC Generic I/O Range #4 register for LPC. Affects B-Unit SAD for LPC regions.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 31 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW/V	**Address [7:2] Mask (ADDR_MASK_7_2):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW/V	**Address [15:2] (ADDR_15_2):** DWord-aligned address. Note that SoC does not provide decode down to the word or byte level.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RO	Reserved.
0	0h RW/V	**LPC Decode Enable (EN):** When this bit is set to '1', then the range specified in this register is enabled for decoding to LPC.

9.4.7 B-Unit Copy of the LPC Generic Memory Range Register for LPC (B_CR_LGMR_LPC)—Offset 98h

Affects B-Unit SAD for LPC regions.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 31 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/V	**Memory Address [31:16] (ADDR_31_16):** This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to LPC as standard LPC Memory Cycle if enabled.
15:1	0h RO	Reserved.
0	0h RW/V	**LPC Memory Range Decode Enable (EN):** When this bit is set to '1', then the range specified in this register is enabled for decoding to LPC.

9.4.8 B-Unit Copy of the BIOS Decode Enable Register for LPC (B_CR_BDE_LPC)—Offset D8h

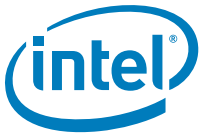
Affects B-Unit SAD for BIOS regions only when BIOS is resident in LPC.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 31 **Function:** 0

Default: FFCFh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RESERVED_0):** Reserved.
15	1h RO	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS ranges: FFF80000h-FFFFFFFFh and FFB80000h-FFBFFFFFh.



Bit Range	Default & Access	Field Name (ID): Description
14	1h RW/V	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS ranges: FFF00000h-FFF7FFFFh and FFB00000h-FFB7FFFFh.
13	1h RW/V	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS ranges: FFE80000h-FFEFFFFFh and FFA80000h-FFAFFFFFh.
12	1h RW/V	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS ranges: FFE00000h-FFE7FFFFh and FFA00000h-FFA7FFFFh.
11	1h RW/V	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS ranges: FFD80000h-FFDFFFFFh and FF980000h-FF9FFFFFh.
10	1h RW/V	**D0-D7 Enable (ED0):** Enables decoding of 512K of the following BIOS ranges: FFD00000h-FFD7FFFFh and FF900000h-FF97FFFFh.
9	1h RW/V	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS ranges: FFC80000h-FFCFFFFFh and FF880000h-FF8FFFFFh.
8	1h RW/V	**C0-C7 Enable (EC0):** Enables decoding of 512K of the following BIOS ranges: FFC00000h-FFC7FFFFh and FF800000h-FF87FFFFh.
7	1h RW/V	**Legacy F Segment Enable (LFE):** This enables the decoding of the legacy 64KB range at F0000h-FFFFFh.
6	1h RW/V	**Legacy E Segment Enable (LEE):** This enables the decoding of the legacy 64KB range at E0000h-EFFFFh.
5:4	0h RO	**Reserved (RESERVED_1):** Reserved.
3	1h RW/V	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS ranges: FF700000h-FF7FFFFFh and FF300000h-FF3FFFFFh.
2	1h RW/V	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS ranges: FF600000h-FF6FFFFFh and FF200000h-FF2FFFFFh.
1	1h RW/V	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS ranges: FF500000h-FF5FFFFFh and FF100000h-FF1FFFFFh.
0	1h RW/V	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS ranges: FF400000h-FF4FFFFFh and FF000000h-FF0FFFFFh.

9.5 Registers Summary

Table 9-5. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
50h	53h	B-Unit Copy of the TCO Base Address Register for Legacy SMBUS (B_CR_TCOBASE_SMBUS)—Offset 50h	0h
54h	57h	B-Unit Copy of the TCO Control Register for Legacy SMBUS (B_CR_TCOCTL_SMBUS)—Offset 54h	0h

9.5.1 B-Unit Copy of the TCO Base Address Register for Legacy SMBUS (B_CR_TCOBASE_SMBUS)—Offset 50h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 31 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:5	0h RW/V	**TCO Base Address (TCOBA):** Provides the 32 bytes of I/O space for TCO logic, mappable anywhere in the 64k I/O space on 32-byte boundaries.
4:0	0h RO	Reserved.

9.5.2 B-Unit Copy of the TCO Control Register for Legacy SMBUS (B_CR_TCOCTL_SMBUS)—Offset 54h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 31 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW/V	**TCO Base Enable (TCO_BASE_EN):** When set, decode of the I/O range pointed to by the TCO base register is enabled.
7:0	0h RO	Reserved.

9.6 Registers Summary

Table 9-6. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
D8h	DBh	B-Unit Copy of the BIOS Decode Enable register for SPI (B_CR_BDE_SPI)—Offset D8h	FFCFh

9.6.1 B-Unit Copy of the BIOS Decode Enable register for SPI (B_CR_BDE_SPI)—Offset D8h

Affects B-Unit SAD for BIOS regions, only when BIOS is resident in SPI.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 2

Default: FFCFh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RESERVED_0):** Reserved.
15	1h RO	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS ranges: FFF80000h-FFFFFFFFh and FFB80000h-FFBFFFFFh.
14	1h RW/V	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS ranges: FFF00000h-FFF7FFFFh and FFB00000h-FFB7FFFFh.
13	1h RW/V	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS ranges: FFE80000h-FFEFFFFFh and FFA80000h-FFAFFFFFh.
12	1h RW/V	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS ranges: FFE00000h-FFE7FFFFh and FFA00000h-FFA7FFFFh.
11	1h RW/V	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS ranges: FFD80000h-FFDFFFFFh and FF980000h-FF9FFFFFh.
10	1h RW/V	**D0-D7 Enable (ED0):** Enables decoding of 512K of the following BIOS ranges: FFD00000h-FFD7FFFFh and FF900000h-FF97FFFFh.
9	1h RW/V	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS ranges: FFC80000h-FFCFFFFFh and FF880000h-FF8FFFFFh.
8	1h RW/V	**C0-C7 Enable (EC0):** Enables decoding of 512K of the following BIOS ranges: FFC00000h-FFC7FFFFh and FF800000h-FF87FFFFh.
7	1h RW/V	**Legacy F Segment Enable (LFE):** This enables the decoding of the legacy 64KB range at F0000h-FFFFFh.
6	1h RW/V	**Legacy E Segment Enable (LEE):** This enables the decoding of the legacy 64KB range at E0000h-EFFFFh.
5:4	0h RO	**Reserved (RESERVED_1):** Reserved.
3	1h RW/V	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS ranges: FF700000h-FF7FFFFFh and FF300000h-FF3FFFFFh.
2	1h RW/V	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS ranges: FF600000h-FF6FFFFFh and FF200000h-FF2FFFFFh.
1	1h RW/V	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS ranges: FF500000h-FF5FFFFFh and FF100000h-FF1FFFFFh.
0	1h RW/V	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS ranges: FF400000h-FF4FFFFFh and FF000000h-FF0FFFFFh.

9.7 Registers Summary

Table 9-7. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	B-Unit Copy of IOBAR MMIO INDEX (B_CR_INDEX_0_2_0_IOBAR)—Offset 0h	0h

9.7.1 B-Unit Copy of IOBAR MMIO INDEX (B_CR_INDEX_0_2_0_IOBAR)—Offset 0h

Device 2 Function Level Reset must reset this register.

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved (RESERVED_0):** Reserved.
22:2	0h RW/V	**Register or GTT Offset (REGGTO):** This field selects any one of the DWORD registers within the MMIO register space of Device 2 if the target is MMIO Registers. This field selects a GTT offset if the target is the GTT.
1:0	0h RW/V	**Targeted Register Type (TARG):** • 00: MMIO Registers • 01: GTT • 1X: Reserved

9.8 Registers Summary

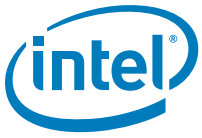
Table 9-8. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	0h	B-Unit Shadow of Legacy VGA Decode GR and MSR Bits (B_CR_VGADEC_0_2_0_VGABAR)—Offset 0h	0h

9.8.1 B-Unit Shadow of Legacy VGA Decode GR and MSR Bits (B_CR_VGADEC_0_2_0_VGABAR)—Offset 0h

Device 2 Function Level Reset must reset this entire register.

Access Method



Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	**Reserved (RESERVED_0):** Reserved.
4	0h RW/V	**Page Mode Enable (VGAGR10):** • 0: VGA mode • 1: Page mode
3:2	0h RW/V	**Select for VGA Memory Space (VGAGR6):** • 00: 0xA_0000-0xB_FFFF • 01: 0xA_0000-0xA_FFFF • 10: 0xB_0000-0xB_7FFF • 11: 0xB_0000-0xB_FFFF
1	0h RW/V	**VGA Memory Access Control (VGAMSR1):** Controls memory access, not IO. • 0: VGA memory access is disabled • 1: VGA memory access is enabled
0	0h RW/V	**IO Space Select (VGAMSR0):** Selects the IO space. • 0: 3Bx mode mono • 1: 3Dx mode color

9.9 Registers Summary

Table 9-9. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
64h	67h	B-Unit Copy of Default VTd BAR PMEN (B_CR_PMEN_REG_0_0_0_DEFVTDBAR)—Offset 64h	0h
68h	6Bh	B-Unit Copy of Default VTd BAR PLM Base Register (B_CR_PLMBASE_REG_0_0_0_DEFVTDBAR)—Offset 68h	0h
6Ch	6Fh	B-Unit Copy of Default VTd BAR PLM Limit Register (B_CR_PLMLIMIT_REG_0_0_0_DEFVTDBAR)—Offset 6Ch	0h
70h	77h	B-Unit Copy of Default VTd BAR PHM Base Register (B_CR_PHMBASE_REG_0_0_0_DEFVTDBAR)—Offset 70h	0h
78h	7Fh	B-Unit Copy of Default VTd BAR PHM Limit Register (B_CR_PHMLIMIT_REG_0_0_0_DEFVTDBAR)—Offset 78h	0h

9.9.1 B-Unit Copy of Default VTd BAR PMEN (B_CR_PMEN_REG_0_0_0_DEFVTDBAR)—Offset 64h

B-Unit copy of the Default VTd BAR PMEN register. Bit 31 is the only bit used for B-Unit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**EPM (EPM):** This field controls DMA accesses to the protected lowmemory and protected highmemory regions. • 0: Protected memory regions are disabled. • 1: Protected memory regions are enabled. Access control is implemented. IA accesses are always allowed access. NonIA accesses are allowed if request SAI matches the SAI of the Default VTd Engine. Requests blocked due to protected memory region violation are not recorded or reported as remapping faults. Hardware reports the status of the protected memory enable/disable operation through the PRS field in this register. Hardware implementations supporting DMA draining must drain any inflight translated DMA requests queued within the RootComplex before indicating the protected memory region as enabled through the PRS field.
30:1	0h RO	**Reserved (RESERVED_0):** Reserved.
0	0h RO	**PRS Unused (PRS):** Unused by the B-Unit. This field indicates the status of protected memory regions: • 0: Protected memory regions are disabled. • 1: Protected memory regions are enabled.

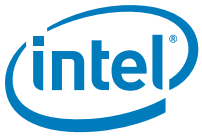
9.9.2 B-Unit Copy of Default VTd BAR PLM Base Register (B_CR_PLMBASE_REG_0_0_0_DEFVTDBAR)—Offset 68h

Register to set up the base address of DMA-protected low-memory region below 4GB. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled. This register is always treated as RO for implementations not supporting protected low memory region (PLMR field reported as Clear in the Capability register). The alignment of the protected low memory region base depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding the most significant bit position with 0 in the value read back from the register. Bits N:0 of this register are decoded by hardware as all 0s. Software must setup the protected low memory region below 4GB. Section 10.4.18 of the Intel Virtualization Technology for Directed I/O: Spec describes the Protected Low-Memory Limit register and hardware decoding of these registers. Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/V	**Protected Low Memory Base (PLMB):** This register specifies the base of the protected low-memory region in system memory.
19:0	0h RO	**Reserved (RESERVED_0):** Reserved.

9.9.3 B-Unit Copy of Default VTd BAR PLM Limit Register (B_CR_PLMLIMIT_REG_0_0_0_DEFVTDBAR)—Offset 6Ch

This register sets up the limit address of DMA-protected low-memory region below 4GB. This register must be set up before enabling protected memory through PMEN_REG, and it must not be updated when protected memory regions are enabled. This register is always treated as RO for implementations not supporting protected low memory region (PLMR field reported as Clear in the Capability register). The alignment of the protected low memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1's to this register, and then finding most significant zero bit position with 0 in the value read back from the register. Bits N:0 of the limit register are decoded by hardware as all 1s. The Protected low-memory base and limit registers function as follows: Programming the protected low-memory base and limit registers with the same value in bits 31:(N+1) specifies a protected low-memory region of size 2^(N+1) bytes. Programming the protected low-memory limit register with a value less than the protected low-memory base register disables the protected low-memory region. Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/V	**Protected Low Memory Limit (PLML):** This register specifies the last host physical address of the DMA protected low memory region in system memory.
19:0	0h RO	**Reserved (RESERVED_0):** Reserved.

9.9.4 B-Unit Copy of Default VTd BAR PHM Base Register (B_CR_PHMBASE_REG_0_0_0_DEFVTDBAR)—Offset 70h

This is the register to set up the base address of the DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled. This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as Clear in the Capability register). The alignment of the protected high memory region base depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1's to this register, and finding most significant zero bit position below host address width (HAW) in the value

read back from the register. Bits N:0 of this register are decoded by hardware as all 0s. Software may setup the protected high memory region either above or below 4GB. Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_1):** Reserved.
38:20	0h RW/V	**Protected High Memory Base (PHMB):** This register specifies the base of protected high memory region in system memory. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width.
19:0	0h RO	**Reserved (RESERVED_0):** Reserved.

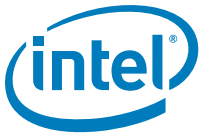
9.9.5 B-Unit Copy of Default VTd BAR PHM Limit Register (B_CR_PHMLIMIT_REG_0_0_0_DEFVTDBAR)—Offset 78h

Register to set up the limit address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled. This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as Clear in the Capability register). The alignment of the protected high memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine the value of N by writing all ones to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of the limit register are decoded by hardware as all ones. The protected high-memory base and limit registers function as follows: Programming the protected low-memory base and limit registers with the same value in bits HAW:(N+1) specifies a protected low-memory region of size 2^(N+1) bytes. Programming the protected high-memory limit register with a value less than the protected high-memory base register disables the protected high-memory region. Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved (RESERVED_1):** Reserved.
38:20	0h RW/V	**Protected High Memory Limit (PHML):** This register specifies the last host physical address of the DMA protected high memory region in system memory. Hardware ignores and does not implement bits 63:HAW where HAW is the host address width.
19:0	0h RO	**Reserved (RESERVED_0):** Reserved.

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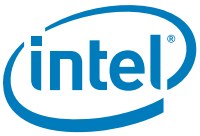


10 C-Unit

10.1 Registers Summary

Table 10-1. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID Register (DEVICE_ID_VENDOR_ID_0_0_0_PCI)—Offset 0h	5AF08086h
4h	7h	PCI Status and PCI Command Register (PCI_STATUS_COMMAND_0_0_0_PCI)—Offset 4h	7h
8h	Bh	PCI Revision ID and PCI Class Code Register (REVISION_ID_CLASS_CODE_0_0_0_PCI)—Offset 8h	6000000h
Ch	Fh	Master Latency Timer and Header Type Register (MASTER_LATENCY_TIME_0_0_0_PCI)—Offset Ch	800000h
2Ch	2Fh	PCI Subsystem Vendor ID and PCI Subsystem ID (SVID_SID_0_0_0_PCI)—Offset 2Ch	0h
34h	37h	Capability Register Pointer (CAPPTR_0_0_0_PCI)—Offset 34h	E0h
48h	4Bh	Memory Controller Hub Base Address Register (MCHBAR_LO_0_0_0_PCI)—Offset 48h	0h
4Ch	4Fh	Memory Controller Hub Base Address Register (MCHBAR_HI_0_0_0_PCI)—Offset 4Ch	0h
50h	53h	Graphics and Memory Controller Hub Graphics Control Register (GGC_0_0_0_PCI)—Offset 50h	0h
54h	57h	Device Enable Register (DEVEN_0_0_0_PCI)—Offset 54h	33h
58h	5Bh	Protected Audio Video Path Control (PAVPC_0_0_0_PCI)—Offset 58h	0h
60h	63h	PCI Express Enhanced Configuration Range Base Address Low (PCIEXBAR_LO_0_0_0_PCI)—Offset 60h	0h
64h	67h	PCI Express Enhanced Configuration Range Base Address High (PCIEXBAR_HI_0_0_0_PCI)—Offset 64h	0h
A8h	ABh	Top of Upper Usable DRAM Low (TOUUD_LO_0_0_0_PCI)—Offset A8h	0h
ACh	AFh	Top of Upper Usable DRAM High (TOUUD_HI_0_0_0_PCI)—Offset ACh	0h
B0h	B3h	Base of Data Stolen Memory (BDSM_0_0_0_PCI)—Offset B0h	0h
B4h	B7h	Base of Graphics Stolen Memory (BGSM_0_0_0_PCI)—Offset B4h	0h
B8h	BBh	Top Segment Memory Base (TSEGMB_0_0_0_PCI)—Offset B8h	100000h
BCh	BFh	Top of Lower Usable DRAM (TOLUD_0_0_0_PCI)—Offset BCh	100000h
DCh	DFh	Scratchpad (SKPD_0_0_0_PCI)—Offset DCh	0h
E0h	E3h	Capability ID0 Capability Control (CAPID0_CAPCTRL0_0_0_0_PCI)—Offset E0h	10C0009h
E4h	E7h	Capability ID0 A (CAPID0_A_0_0_0_PCI)—Offset E4h	0h
E8h	EBh	Capability ID0 B (CAPID0_B_0_0_0_PCI)—Offset E8h	0h
F8h	FBh	Design and Engineering Backup Register 0 (DEBUP0_0_0_0_PCI)—Offset F8h	0h
FCh	FFh	Design and Engineering Backup Register 1 (DEBUP1_0_0_0_PCI)—Offset FCh	0h
061Ch		I/O Buffer Control (IOBCTL)—Offset 061Ch	C000004h
0054h		Power Management Control And Status (PCS)—Offset 0054h	8h

Table 10-1. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1048h		LTRC_D013C_PCE—Offset 1048h	8080080h
0050h		PID_PC—Offset 0050h	C8436001h

10.1.1 Device ID and Vendor ID Register (DEVICE_ID_VENDOR_ID_0_0_0_PCI)—Offset 0h

This register uniquely identifies any PCI device.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 5AF08086h

Bit Range	Default & Access	Field Name (ID): Description
31:23	B5h RW/V	**Strap2 Portion of Device ID (DEVICE_ID_STRAP2):** The reset default value of this register is tied to the parameter DEVICE_ID_STRAP2. These bits can be rewritten from SETIDVALUE message 1st DW data byte2, byte3.
22:21	3h RO	**Strap1 Portion of Device ID (DEVICE_ID_STRAP1):** These bits are tied to a C-Unit parameter DEVICE_ID_STRAP1.
20:16	10h RO/V	**Fuse Backed Portion of Device ID (DEVICE_ID_FUSE):** These bits of Device ID are fuse backed.
15:0	8086h RO	**Vendor ID (VENDOR_ID):** Hardwired to Intel's Vendor ID value.

10.1.2 PCI Status and PCI Command Register (PCI_STATUS_COMMAND_0_0_0_PCI)—Offset 4h

PCI Status is used to record status information for PCI bus related events. PCI Command provides coarse control over a device's ability to generate and respond to PCI cycles.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 7h

Bit Range	Default & Access	Field Name (ID): Description
31:0	7h RO	**PCI Status and PCI Command (PCI_STATUS_AND_COMMAND):** Hardwired to 32'h00000007, allowing this device to respond to I/O space and Memory Space accesses. This device is also allowed to behave as a bus master.

10.1.3 PCI Revision ID and PCI Class Code Register (REVISION_ID_CLASS_CODE_0_0_0_PCI)—Offset 8h

Revision ID contains the revision number of the device. Class Code identifies the basic function of the device.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 6000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	600h RO	**Class Code 1 (CLASS_CODE1):** Hardwired 16'h0600, indicating this device is a Host Bridge.
15:8	0h RO	**Class Code 0 (CLASS_CODE0):** Hardwired to 8'h00, indicating this device is a Host Bridge.
7:0	0h RW/V	**Revision ID Strap (REVISION_ID_STRAP):** These bits can be rewritten from SETIDVALUE message 1st DW data byte 0.

10.1.4 Master Latency Timer and Header Type Register (MASTER_LATENCY_TIME_0_0_0_PCI)—Offset Ch

This register defines Latency Timer and layout of the device Configuration Space header.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RESERVED_1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23:16	80h RO	**Header Type (HEADER_TYPE):** This field identifies the layout of the second part of the predefined header (beginning at byte 10h in the Configuration Space) and also whether or not the device contains multiple functions. Hardwired to 8'h80, indicating this is a multi-function device.
15:8	0h RO	**Master Latency Timer (MASTER_LATENCY_TIMER):** This field specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. Hardwired to 1'b0.
7:0	0h RO	**Reserved (RESERVED_0):** Reserved.

10.1.5 PCI Subsystem Vendor ID and PCI Subsystem ID (SVID_SID_0_0_0_PCI)—Offset 2Ch

This register is used to uniquely identify the subsystem where the PCI device resides.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Subsystem ID (SUBSYSTEM_ID):** PCI Subsystem ID: This field should be programmed during BIOS initialization.
15:0	0h RW	**Subsystem Vendor ID (SUBSYSTEM_VENDOR_ID):** PCI Subsystem Vendor ID: This field should be programmed by BIOS during bootup to indicate the vendor of the system board.

10.1.6 Capability Register Pointer (CAPPTR_0_0_0_PCI)—Offset 34h

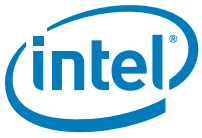
This register contains a pointer to the first Capability Register in a linked list.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: E0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RESERVED_0):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
7:0	E0h RO	**Base Address of First Capability Register (BASE_ADDR):** This pointer is an 8-bit address to an offset within this device's Configuration Space that holds the first Capability Register (CAPID0_CAPCTRL).

10.1.7 Memory Controller Hub Base Address Register (MCHBAR_LO_0_0_0_PCI)—Offset 48h

This register contains the lower 32bits of the MCHBAR base address.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Base Address of MCHBAR (BASE_ADDR):** Defines the base address of MCHBAR. MCHBAR[38:15] is {MCHBAR_HI[6:0],MCHBAR_LO[31:15]}. If incoming Request Address[38:15] matches MCHBAR[38:15] then the request hits and address in the MCHBAR range.
14:4	0h RO	**Base Address not Implemented (BASE_ADDR_NOT_IMPLEMENTED):** Hardwired to 0 to indicate size of BAR 32kB.
3:1	0h RO	**Reserved (RESERVED_0):** Reserved.
0	0h RW	**MCHBAR Enable (MCHBAREN):** • 0: MCHBAR is disabled and does not claim any memory • 1: MCHBAR memory mapped accesses are claimed and decoded appropriately

10.1.8 Memory Controller Hub Base Address Register (MCHBAR_HI_0_0_0_PCI)—Offset 4Ch

This register contains the upper 32bits of the MCHBAR base address.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RESERVED_0):** Reserved.
6:0	0h RW	**Base Address of MCHBAR (BASE_ADDR):** Defines the base address of the MCHBAR. If incoming Request Address[38:15] matches MCHBAR[38:15], then request hits an address in the MCHBAR range.

10.1.9 Graphics and Memory Controller Hub Graphics Control Register (GGC_0_0_0_PCI)—Offset 50h

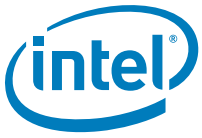
The GMCH Graphics Control register configures the memory preallocated to the internal graphics device.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RESERVED_1):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Graphics Memory Select (GMS):** This field is used to select the amount of Main Memory that is preallocated to support the Internal Graphics device in VGA nonlinear and Native linear modes. The BIOS ensures that memory is preallocated only when Internal graphics is enabled. This register is also Intel TXT lockable. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD bit 1 of this register is 0. • 00h:0MB • 01h:32MB • 02h:64MB • 03h:96MB • 04h:128MB • 05h:160MB • 06h:192MB • 07h:224MB • 08h:256MB • 09h:288MB • 0Ah:320MB • 0Bh:352MB • 0Ch:384MB • 0Dh:416MB • 0Eh:448MB • 0Fh:480MB • 10h:512MB • 20h:...1024MB... • 30h:...1536MB... • 3Fh:...2016MB • 40h-FFh:Illegal value
7:6	0h RW	**Size of Graphics Translation Table Memory (GGMS):** This field is used to select the amount of Main Memory that is preallocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is preallocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. • 0h: No Preallocated Memory • 1h: 2MB of Preallocated Memory • 2h: 4MB of Preallocated Memory • 3h: 8MB of Preallocated Memory
5:3	0h RO	**Reserved (RESERVED_0):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Versatile Acceleration Mode Enable (VAMEN):** Enables the use of the iGFX engines for Versatile Acceleration. • 1: iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. • 0: iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
1	0h RW/V	**IGD VGA Disable (IVD):** • 0: Enable. Device 2 IGD claims VGA memory and IO cycles the SubClass Code within Device 2 Class Code register is 00. • 1: Disable. Device 2 IGD does not claim VGA cycles Mem and IO and the Sub Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field bits 7:3 of this register preallocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse override CAPID0_A[IGD] set to 1h or via a register DEVEN[D2F0EN] set to 0h.
0	0h RW	**GGC Register Lock (GGCLCK):** This lock bit only impacts the Display copy of this register. In the C-Unit all register protection is implemented with SAI policy groups. This bit is maintained in the C-Unit for software observability. Display description: This bit locks all other writeable bits in this register.

10.1.10 Device Enable Register (DEVEN_0_0_0_PCI)—Offset 54h

The DEVEN register allows for enabling/disabling of PCI devices and functions that are within the CPU package.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 33h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved (RESERVED_1):** Reserved.
5	1h RW/V	**Device 3 Function 0 Enable (D3F0EN):** • 0: Bus 0 Device 3 Function 0 is disabled and hidden • 1: Bus 0 Device 3 Function 0 is enabled and visible This bit will be set to 0b and remain 0b if Device 3 capability is disabled.
4	1h RW/V	**Device 2 Function 0 Enable (D2F0EN):** • 0: Bus 0 Device 2 Function 0 is disabled and hidden • 1: Bus 0 Device 2 Function 0 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled.
3	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Reserved (RESERVED_0):** Reserved.
1	1h RW/V	**Device 0 Function 1 Enable (D0F1EN):** • 0: Bus 0 Device 0 Function 1 is disabled and hidden • 1: Bus 0 Device 0 Function 1 is enabled and visible This bit will be set to 0b and remain 0b if Device 0/0/1 capability is disabled.
0	1h RO	**Device 0 Function 0 Enable (D0F0EN):** Bus 0 Device 0 Function 0 may not be disabled, and is therefore hardwired to 1.

10.1.11 Protected Audio Video Path Control (PAVPC_0_0_0_PCI)—Offset 58h

This register contains the control bits for the Protected Audio Video Path.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Base of Protected Content Memory (PCMBASE):** Sizes supported in SoC: 1M, 2M, 4M, and 8M. Base value programmed from Top of Stolen Memory itself defines the size of the Write Only Protected Content Memory (WOPCM). Separate WOPCM size programming is redundant information and not required. Default 1M size programming. 4M recommended for SoC.
19:7	0h RO	**Reserved (RSVD2):** Reserved.
6	0h RW	**ASMF Enable (ASMFEN):** ASMF method enable • 0: Disabled (default) • 1: Enabled
5	0h RO	**Reserved (RSVD1):** Reserved.
4	0h RW	**Override Attack (OVTATTACK):** Override of Unsolicited Connection State Attack and Terminate. • 0: Disable Override. Attack Terminate allowed. • 1: Enable Override. Attack Terminate disallowed.
3	0h RW	**Heavy Mode Select (HVYMODSEL)**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**PAVP Register Lock (PAVPLCK):** This lock bit only impacts the Display copy of this register. In the C-Unit, all register protection is implemented with SAI policy groups. This bit is maintained in the C-Unit for software observability. Display description: This bit locks all writeable contents in this register when set, including itself. Only a hardware reset can unlock the register again. This lock bit needs to be set only if PAVP is enabled (bit 1 of this register is asserted.)
1	0h RW	**Protected Audio Video Path Enable (PAVPE):** • 0: PAVP functionality is disabled. • 1: PAVP functionality is enabled.
0	0h RW	**Protected Content Memory Enable (PCME):** This field enables Protected Content Memory within Graphics Stolen Memory. This memory is the same as the Write Only Protected Content Memory area whose size is defined by bit 5 of this register. This register is locked when PAVPLCK is set. • 0: Protected Content Memory is disabled and cannot be programmed in this manner when PAVP is enabled. • 1: Protected Content Memory is enabled and is the only programming option available when PAVP is enabled.

10.1.12 PCI Express Enhanced Configuration Range Base Address Low (PCIEXBAR_LO_0_0_0_PCI)—Offset 60h

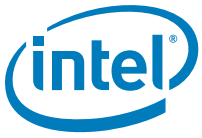
This register contains the lower 32bits of the base address of the PCI Express Enhanced Configuration region.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**PCI Express Base Address Register (PCIEXBAR):** PCIEXBAR[38:28] is {PCIEXBAR_HI[6:0],PCIEXBAR_LO[31:28]}. Describes bits [38:28] of the base address of the contiguous 256MB region for PCI Express Enhanced Configuration region. If bits [38:28] of the request address matches the PCIEXBAR[38:28] then the request targets the PCI Express Enhanced Configuration Space region. A posted memory operation from an IDI agent will be treated as a nonposted operation by the T-Unit and A-Unit.
27	0h RO	**Address Mask for 128MB region (ADMSK128):** Reserved. Unused by SoC since PCIEXBAR is a fixed 256MB region in SoCs.
26	0h RO	**Address Mask for 64MB region (ADMSK64):** Reserved. Unused by SoC since PCIEXBAR is a fixed 256MB region in SoCs.



Bit Range	Default & Access	Field Name (ID): Description
25:3	0h RO	**Reserved (RESERVED_0):** Reserved.
2:1	0h RO	**Length of the Region (LENGTH):** Reserved and set to 0, indicating a fixed 256 MB region.
0	0h RW	**PCIEXBAR Range Enable (PCIEXBAREN):** • 0: The PCIEXBAR range is disabled. Address may target DRAM or MMIO, depending on other address decode rules. • 1: The PCIEXBAR range is enabled. Incoming request address must be compared with PCIEXBAR to determine whether the request targets PCI Express Enhanced Configuration region.

10.1.13 PCI Express Enhanced Configuration Range Base Address High (PCIEXBAR_HI_0_0_0_PCI)—Offset 64h

This register contains the upper 32bits of the base address of the PCI Express Enhanced Configuration region.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RESERVED_0):** Reserved.
6:0	0h RW	**PCI Express Base Address Register (PCIEXBAR_HI):** PCIEXBAR[38:28] is {PCIEXBAR_HI[6:0],PCIEXBAR_LO[31:28]}. Describes bits [38:28] of the base address of the contiguous 256MB region for PCI Express Enhanced Configuration region. If bits [38:28] of the request address matches the PCIEXBAR[38:28] then the request targets the PCI Express Enhanced Configuration Space region. A posted memory operation from an IDI agent will be treated as a nonposted operation by the T-Unit and A-Unit.

10.1.14 Top of Upper Usable DRAM Low (TOUUD_LO_0_0_0_PCI)—Offset A8h

Defines the top of the upper usable DRAM range and start of the upper MMIO address range. Formerly defined in BMBOUND_HI. This register contains the lower 32 bits of TOUUD.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Top of Upper Usable DRAM (TOUUD):** TOUUD[38:20] is {TOUUD_HI[6:0],TOUUD_LO[31:20]}. Upper usable DRAM address range ends at the preceding byte. Upper MMIO Range starts at this address and extends up to the maximum system addressable memory range. Bits 38:20 are compared with bits 38:20 of the incoming request address to determine whether the request targets the upper usable DRAM range or upper MMIO range. If Request Address[38:20]>=TOUUD[38:20] and any bit in Request Address[38:32] is set, request is determined to target the upper MMIO range.
19:1	0h RO	**Reserved (RESERVED_0):** Reserved should return 0s on read.
0	0h RW	**TOUUD Register Lock (LOCK_RESERVED):** This lock bit only impacts the Display copy of this register. In the C-Unit, all register protection is implemented with SAI policy groups. This bit is maintained in the C-Unit for software observability. Display description: This bit will lock all writeable settings in this register, including itself (client definition).

10.1.15 Top of Upper Usable DRAM High (TOUUD_HI_0_0_0_PCI)—Offset ACh

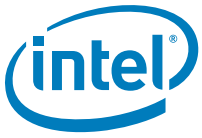
Defines the top of the upper usable DRAM range and start of the upper MMIO address range. Formerly defined in BMBOUND_HI. This register contains the upper 32 bits of TOUUD.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RESERVED_0):** Reserved.
6:0	0h RW	**Top of Upper Usable DRAM (TOUUD_HI):** TOUUD[38:20] is {TOUUD_HI[6:0],TOUUD_LO[31:20]}. Upper usable DRAM address range ends at the preceding byte. Upper MMIO Range starts at this address and extends up to the maximum system addressable memory range. Bits 38:20 are compared with bits 38:20 of the incoming request address to determine whether the request targets the upper usable DRAM range or upper MMIO range. If Request Address[38:20]>=TOUUD[38:20] and any bit in Request Address[38:32] is set, request is determined to target the upper MMIO range.



10.1.16 Base of Data Stolen Memory (BDSM_0_0_0_PCI)—Offset B0h

Defines the Base of the Data Stolen Memory. In addition, the GSM range is defined to end at the preceding byte. See BGSM register.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Base of Data Stolen Memory (BDSM):** This register contains the base address of the Data Stolen Memory. The limit for the Data Stolen Memory is TOLUD-1. This range is not decoded by the system agent, but is a sub-region of BGSM decoded by the Integrated Graphics Device. Incoming Request Address[31:20] is compared against BDSM[31:20] and TOLUD[31:20] to determine if the address falls in the range. The comparison check is as follows: BDSM[31:20]<=Address[31:20] && Address[31:20]<TOLUD[31:20] and Address[38:32]==0.
19:1	0h RO	**Reserved (RESERVED_0):** Reserved.
0	0h RW	**BDSM Register Lock (LOCK):** This lock bit only impacts the Display copy of this register. In the C-Unit all register protection is implemented with SAI policy groups. This bit is maintained in the C-Unit for software observability. Display description: This bit will lock all writeable settings in this register, including itself.

10.1.17 Base of Graphics Stolen Memory (BGSM_0_0_0_PCI)—Offset B4h

Defines the Base of the Graphics Stolen Memory. In addition, the SMM range is defined to end at the preceding byte. See TSEGMB register.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Base of Graphics Stolen Memory (BGSM):** This register contains the base address of the Graphics Stolen Memory. The limit for the Graphics Stolen Memory is TOLUD-1. Incoming Request Address[31:20] is compared against BGSM[31:20] and TOLUD[31:20] to determine if the address falls in the range. The comparison check is as follows: BGSM[31:20]<=Address[31:20] && Address[31:20]<TOLUD[31:20] and Address[38:32]==0. The Integrated Graphics Device (IGD) further subdivides this range, however outside of the IGD the access protections are the same and the system is not aware of the further sub-division. These divisions include a Data segment and a PCM segment.
19:1	0h RO	**Reserved (RESERVED_0):** Reserved.
0	0h RW	**BGSM Register Lock (LOCK):** This lock bit only impacts the Display copy of this register. In the C-Unit, all register protection is implemented with SAI policy groups. This bit is maintained in the C-Unit for software observability. Display description: This bit will lock all writeable settings in this register, including itself.

10.1.18 Top Segment Memory Base (TSEGMB_0_0_0_PCI)—Offset B8h

TSEGMB defines the base of the SMM range, and the BGSM register defines the limit of the SMM range. Note: In prior SoCs, the base register was defined in SMMRRL register and the limit was defined in the SMMRRH register.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	1h RW	**Base address of Top Segment DRAM Memory (TSEGMB):** BIOS determines the base of TSEG memory, which must be at or below Graphics Base of GTT Stolen Memory BGSM. SMM range starts at this base and ends at BGSM1. Incoming Request Address [31:20] will be compared with TSEGMB[31:20] and BGSM[31:20] to determine if the request targets the SMM range. The comparison check is as follows: Address[31:20]>=TSEGMB[31:20] && Address[31:20]<BGSM[31:20] and Address[38:32]==0. If the check passes, the request targets the SMM range. If the protection for the range is enabled, then the request SAI is compared against allowed SAIs specified by BSMRRAC and BSMRWAC registers to determine if access is allowed.

Bit Range	Default & Access	Field Name (ID): Description
19:1	0h RO	**Reserved (RESERVED_0):** Reserved.
0	0h RW	**TSEGMB Register Lock (LOCK):** This lock bit only impacts the Display copy of this register. In the C-Unit, all register protection is implemented with SAI policy groups. This bit is maintained in the C-Unit for software observability. Display description: This bit will lock all writeable settings in this register, including itself.

10.1.19 Top of Lower Usable DRAM (TOLUD_0_0_0_PCI)—Offset BCh

This register defines the Top of Lower Usable DRAM range and start of the Lower MMIO Address range. Formerly defined in BMBOUND.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	1h RW	**Top of Lower Usable DRAM (TOLUD):** Defines the top of lower usable DRAM, which ends at the preceding byte. Lower MMIO Address range starts at this address and continues up to the 4GB Address 0xFFFF_FFFF. Bits 31:20 are compared with incoming request Address[31:20] to determine whether the request targets lower usable DRAM range or the lower MMIO range. If Request Address[31:20]>=TOLUD[31:20] and Request Address[38:32]==0 then the Request Address falls in the Lower MMIO Address range.
19:1	0h RO	**Reserved (RESERVED_0):** Reserved.
0	0h RW	**TOLUD register lock (LOCK):** Reserved. Lock is unused by C-Unit. Register overwrites are protected via SAI access control policy registers.

10.1.20 Scratchpad (SKPD_0_0_0_PCI)—Offset DCh

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Scratchpad (SKPD):** 1 DWORD of data storage.

10.1.21 Capability ID0 Capability Control (CAPID0_CAPCTRL0_0_0_0_PCI)—Offset E0h

Control bits in this register describe the attributes of CAPID0_A and CAPID0_B capability registers.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 10C0009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RESERVED_0):** Reserved.
27:24	1h RO	**Capability ID Version (CAPID_VER):** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	Ch RO	**Capability ID0 Structure Length (CAPIDLEN):** This field has the value 0Ch to indicate the structure length 12 bytes. This is the total size of this CAPCTRL and the CAPID0_A and CAPID0_B registers in the following bytes.
15:8	0h RO	**Next Capability Register Pointer (NEXT_CAP):** This field is hardwired to 00h, indicating the end of the capabilities linked list.
7:0	9h RO	**Capability ID (CAP_ID):** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

10.1.22 Capability ID0 A (CAPID0_A_0_0_0_PCI)—Offset E4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Spare bits[31:24] (SPARE31_24):** Reserved for future capabilities.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW/Fuse	**VTd Disable (VTDD):** • 0: Enable VTd • 1: Disable VTd
22	0h RW/Fuse	**Fuse Spare bit[22] (FUSE_SPARE22):** Fuse backed spare.
21	0h RW/Fuse	**Fuse Spare bit[21] (FUSE_SPARE21):** Fuse backed spare.
20	0h RW/Fuse	**Fuse Spare bit[20] (FUSE_SPARE20):** Fuse backed spare.
19	0h RW/Fuse	**Fuse Spare bit[19] (FUSE_SPARE19):** Fuse backed spare.
18	0h RW/Fuse	**Fuse Spare bit[18] (FUSE_SPARE18):** Fuse backed spare.
17	0h RW/Fuse	**Fuse Spare bit[17] (FUSE_SPARE17):** Fuse backed spare.
16	0h RW/Fuse	**Fuse Spare bit[16] (FUSE_SPARE16):** Fuse backed spare.
15	0h RW/Fuse	**Camarillo Device (DPTF) Disable (CDD):** • 0: DPTF (Camarillo) associated memory spaces are accessible. • 1: DPTF (Camarillo) associated memory and IO spaces are disabled. DEVEN_0_0_0_PCI field for DPTF cannot be set.
14	0h RW/Fuse	**Fuse Spare bit[14] (FUSE_SPARE14):** Fuse backed spare.
13	0h RW/Fuse	**Fuse Spare bit[13] (FUSE_SPARE13):** Fuse backed spare.
12	0h RW/Fuse	**Fuse Spare bit[12] (FUSE_SPARE12):** Fuse backed spare.
11	0h RW/Fuse	**Internal Graphics Disable (IGD):** • 0: There is a graphics engine within this CPU. Internal Graphics Device 2 is enabled, and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the CPU. All nonSMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2, IO registers within Device 2, and VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6, if PCI Express GFX attach is supported. A selected amount of Graphics Memory space is preallocated from the main memory, based on Graphics Mode Select GMS in the GGC Register. Graphics Memory is preallocated above TSEG Memory. • 1: There is no graphics engine within this CPU. Internal Graphics Device 2 and all of its memory and I/O functions are disabled. Configuration cycles targeted to Device 2 will be passed on to DMI. In addition, all clocks to internal graphics logic are turned off. All nonSMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6. DEVEN [4:3] Device 0 offset 54h have no meaning. Device 2 Functions 0 and 1 are disabled and hidden.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO	**Device ID Override Enable (DIDOE):** Controls if there is an override of Dev2 GFX device ID. • 0: Disable ability to override DID -- For production • 1: Enable ability to override DID -- For debug and samples only
9:8	0h RO	**Control Device ID Value (CDID):** Controls the value of Dev2 GFX device ID. Identifier assigned to the core/primary PCI device. The corresponding two bit capability ID programming is: • 00: Desktop • 01: Mobile • 10: Server • 11: Marketing Spare
7:0	0h RW	**Spare bits[7:0] (SPARE7_0):** Reserved for future capabilities

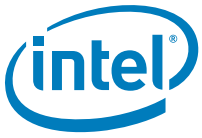
10.1.23 Capability ID0 B (CAPID0_B_0_0_0_PCI)—Offset E8h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/Fuse	**Imaging Unit Memory/IO Disable (IMGU_DIS):** • 0: Imaging Unit associated memory spaces are accessible. • 1: Imaging Unit associated memory and IO spaces are disabled. DEVEN_0_0_0_PCI field for Iunit cannot be set.
30	0h RW/Fuse	**Fuse Spare bit[30] (FUSE_SPARE_30):** Fuse backed spare.
29	0h RW/Fuse	**Fuse Spare bit[29] (FUSE_SPARE_29):** Fuse backed spares potentially to be used for PKGTYP encoding.
28	0h RW/Fuse	**Fuse Spare bit[28] (FUSE_SPARE_28):** Fuse backed spares potentially to be used for PKGTYP encoding.
27	0h RW/Fuse	**Fuse Spare bit[27] (FUSE_SPARE_27):** Fuse backed spares potentially to be used for PKGTYP encoding.
26	0h RW/Fuse	**Fuse Spare bit[26] (FUSE_SPARE_26):** Fuse backed spares potentially to be used for PKGTYP encoding.
25	0h RW/Fuse	**Fuse Spare bit[25] (FUSE_SPARE_25):** Fuse backed spares potentially to be used for PKGTYP encoding.
24	0h RW/Fuse	**Shared Virtual Memory Disable (SVMDIS):** • 0: Enable Shared Virtual Memory mode • 1: Disable Shared Virtual Memory mode



Bit Range	Default & Access	Field Name (ID): Description
23:0	0h RW	**Spare bits[23:0] (SPARE23_0):** Reserved for future capabilities.

10.1.24 Design and Engineering Backup Register 0 (DEBUP0_0_0_0_PCI)—Offset F8h

Reserved for future spare usage.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Spare bits[31:0] (SPARE_RW):** Spare RW bits for future usage.

10.1.25 Design and Engineering Backup Register 1 (DEBUP1_0_0_0_PCI)—Offset FCh

Reserved for future spare usage.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Spare bits[31:0] (SPARE_RW):** Spare RW bits for future usage.

10.1.26 I/O Buffer Control (IOBCTL)—Offset 061Ch

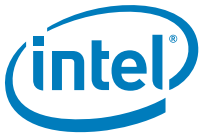
This register allows BIOS to control the I/O buffer configuration based on the motherboard configuration. Notes: 1. Bits 31:26 control the iDISPLAY Audio Link Buffers at the same time that 2. Bits 9:0 control HD-Audio and I2S/SSP Ports 0 and 1 buffers.

Access Method

Type: CR Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 2AC000004h

Range	Access Type	Default (reset)	Description
31:30	RW	0x0 (rst)	**IDSRCP (iDISPLAY Slew Rate Control P)** These bits control the pullup slew rate of the iDISPLAY Audio Link buffers. 00: P Slew Rate for iDISPLAY interface 01: Very slow P Slew Rate 10: Fast P Slew Rate 11: Slow P Slew Rate
29:28	RW	0x0 (rst)	**IDSRCN (iDISPLAY Slew Rate Control N)** These bits control the pulldown slew rate of the iDISPLAY Audio Link buffers. 00: N Slew Rate for iDISPLAY interface 01: Fast N Slew Rate 10: Slow N Slew Rate 11: Very Fast N Slew Rate
27:26	RW	0x3 (rst)	**IDHYS (iDISPLAY Hysteresis Control)** These bits control the hysteresis levels of the iDISPLAY Audio Link buffers. 00: No Hysteresis 01: >80mV (for GTL) 10: >0.1 VCC 11: >80mV (for iDISPLAY)
25:10	RO	0x0 (rst)	**RSVD1 (Reserved)** Reserved for future use
9:8	RW	0x0 (rst)	**OSEL (Ownership Select)** Indicates the ownership of the I/O buffer between Intel HD Audio link vs I2S0 / I2S port. 00: Intel HD-Audio link owns all the I/O buffers. 01: Intel HD-Audio link owns 4 of the I/O buffers for 1 HD-Audio codec connection, and I2S1 port owns 4 of the I/O buffers for 1 I2S codec connection. 10: Reserved. 11: I2S0 and I2S1 ports own all the I/O buffers. Note that the 01 setting is ONLY workable with the new type of Intel HD Audio codec known as Mobile HD Audio codec that does not making use of the reset pin.
7:6	RW	0x0 (rst)	**HDASRCP (HD-Audio Slew Rate Control P)** These bits control the pullup slew rate of the HD-Audio Link buffers. 00: P Slew Rate for HD-A interface 01: Slow P slew rate 10: Reserved 11: Reserved
5:4	RW	0x0 (rst)	**HDASRCN (HD-Audio Slew Rate Control N)** These bits control the pulldown slew rate of the HD-Audio Link buffers. 00: N Slew Rate for HD-A interface 01: Slow N slew rate 10: Reserved 11: Reserved



Range	Access Type	Default (reset)	Description
3:2	RW	0x1 (rst)	**HDAHYS (HD-Audio Hysteresis Control)** These bits control the hysteresis levels of the iDISPLAY Audio Link buffers. 00: No Hysteresis 01: HD-A at 1.8V or 3.3V 10: LPC at 3.3V 11: HD-A at 1.5V
1:1	RW	0x0 (rst)	**VSEL (Voltage Select)** When this bit is cleared to 0, the IO buffers will operate in 3.3V mode drive strength attribute. When this bit is set to 1, the IO buffers will operate in 1.8V mode drive strength attribute. The actual voltage of the IO buffer operation is still depending on the VCCPAZ power pin supplied voltage.
0:0	RO	0x0 (rst)	**RSVD0 (Reserved)** Reserved for future use

10.1.27 Power Management Control And Status (PCS)—Offset 0054h

This register is used to manage the PCI functions power management state as well as to enable/monitor PMEs. PMES and PMEE bits reside in Resume well, and reset by resume reset.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 8h

Range	Access Type	Default (reset)	Description
31:24	RO	0x0 (rst)	**DT (Data)** Does not apply. Hardwired to 0.
23:23	RO	0x0 (rst)	**BPCCE (Bus Power/Clock Control Enable)** Does not apply. Hardwired to 0.
22:22	RO	0x0 (rst)	**B23 (B2/B3 Support)** Does not apply. Hardwired to 0.
21:16	RO	0x0 (rst)	**RSVD3 (Reserved)** Reserved.
15:15	RW/1C/V	0x0 (rst)	**PMES (PME Status)** This bit is set when the Intel HD Audio controller would normally assert the PME# signal independent of the state of the PME bit. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
14:9	RO	0x0 (rst)	**RSVD2 (Reserved)** The Intel HD Audio subsystem does not implement the data register.

Range	Access Type	Default (reset)	Description
8:8	RW	0x0 (rst)	**PMEE (PME Enable)** When set, and if corresponding PMES is also set, the Intel HD Audio subsystem send PME to PMC. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
7:4	RO	0x0 (rst)	**RSVD1 (Reserved)** Reserved.
3:3	RW/L	0x1 (rst)	**NSR (No Soft Reset)** When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. Locked when FNCFG.BCLD = 1.
2:2	RO	0x0 (rst)	**RSVD0 (Reserved)** Reserved.
1:0	RW	0x0 (rst)	**PS (Power State)** This field is used both to determine the current power state of the Intel HD Audio subsystem and to set a new power state. The values are: • 00: D0 state • 1 1: D3HOT state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3HOT states, the Intel HD Audio subsystem's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the D3HOT state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

10.1.28 LTRC_D013C_PCE—Offset 1048h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 8080080h

Range	Access Type	Default (reset)	Description
31:30	RO	0x0 (rst)	**RSVD1_1 (Reserved)** Reserved.

Range	Access Type	Default (reset)	Description
29:29	RW	0x0 (rst)	**HAE (Hardware Autonomous Enable)** If set, then the IP may request a PG whenever it is idle. Note: If this bit is set, then bits[2:0] must be 000.
28:28	RO	0x0 (rst)	**RSVD0 (Reserved)** Reserved.
27:27	RW/L	0x1 (rst)	**SE (Sleep Enable)** If clear, then IP will never asset Sleep to the retention flops. If set, then IP may assert Sleep during PGing. Locked when DFx security policy is not in red unlock state.
26:26	RW	0x0 (rst)	**D3HE (D3-Hot Enable)** If set, then IP will PG when idle and the PMCSR[1:0] register in the IP = '11'.
25:25	RW	0x0 (rst)	**I3E (I3 Enable)** If set, then IP will PG when idle and the D0i3 register (D0i3C[2] = '1') is set. [p]Note: If bits [1:0] = #11#, then the IP would PG whenever either the D3 register or the D0i3 register is set.
24:24	RW	0x0 (rst)	**PMCRE (PMC Request Enable)** If set, then IP will PG when idle and the PMC requests power gating by asserting the pmc_(ip)_sw_pg_req_b signal.
23:20	RO	0x0 (rst)	**RSVD1 (Reserved)** Reserved.
19:19	RW/1C/V	0x1 (rst)	**RR (Restore Required)** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a '1'. This bit will be set on initial power up.
18:18	RW	0x0 (rst)	**I3 (D0i3)** SW sets this bit to '1' to move the IP into the D0i3 state. Writing this bit to ' 0' will return the IP to the fully active D0 state (D0i0).
17:17	RW	0x0 (rst)	**IR (Interrupt Request)** SW sets this bit to '1' to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
16:16	RO/V	0x0 (rst)	**CIP (Command-In-Progress)** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.
15:0	RO	0x0 (rst)	**RSVDP0 (Reserved)** Reserved.

10.1.29 PID_PC—Offset 0050h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: C8436001h

Range	Access Type	Default (reset)	Description
31:27	RW/L	0x19 (rst)	**PMES (PME_Support)** Indicates PME# can be generated from D3 and D0 states. Programmable by BIOS for the option to declare SUS well wake is supported or not: 19h (SUS well wake supported) or 09h (SUS well wake not supported). Locked when FNCFG.BCLD = 1.
26:26	RO	0x0 (rst)	**D2S (D2_Support)** The D2 state is not supported.
25:25	RO	0x0 (rst)	**D1S (D1_Support)** The D1 state is not supported.
24:22	RW/L	0x1 (rst)	**AC (Aux_Current)** Reports 55 mA maximum Suspend well current required when in the D3cold state. P rogrammable by BIOS for the option to declare SUS well wake is supported or not: 001b (SUS well wake supported) or 000b (SUS well wake not supported). Locke d when FNCFG.BCLD = 1.
21:21	RO	0x0 (rst)	**DSI (Device Specific Initialization)** Indicates that no device-specific initialization is required.
20:20	RO	0x0 (rst)	**RSVD (Reserved)** Reserved.
19:19	RO	0x0 (rst)	**PMEC (PME Clock)** Does not apply. Hardwired to 0.
18:16	RW/L	0x3 (rst)	**VS (Version)** Indicates support for Revision 1.2 of the PCI Power Management Specification. Programmable by BIOS to older revision if compatibility issue is found. Locked when FNCFG.BCLD = 1.
15:8	RW/L	0x60 (rst)	**NEXT (Next Capability)** Points to the next capability structure (MSI). Locked when FNCFG.BCLD = 1.
7:0	RO	0x1 (rst)	**CAP (Cap ID)** Indicates that this pointer is a PCI power management capability.

10.2 Registers Summary

Table 10-2. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
10h	13h	Thermal Management Base Address Register (TMBAR_LO_0_0_1_PCI)—Offset 10h	4h

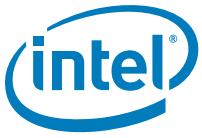


Table 10-2. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
14h	17h	Thermal Management Base Address Register (TMBAR_HI_0_0_1_PCI)—Offset 14h	0h

10.2.1 Thermal Management Base Address Register (TMBAR_LO_0_0_1_PCI)—Offset 10h

This is the base address for the Thermal Controller Memory Mapped space. There is no physical memory within this 32KB window that can be addressed. The 32KB reserved by this register does not alias to any PCI 2.2 compliant memory mapped space. All TMBAR space maps the access to this memory space towards MCHBAR space. For details of this BAR, refer to the MCHBAR specifications.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**TMMBA (TMMBA):** This field corresponds to bits 31 to 15 of the base address TMBAR address space. BIOS will program this register resulting in a base address for a 32KB block of contiguous memory address space. This register ensures that a naturally aligned 32KB space is allocated within total addressable memory space. The DPTF driver uses this base address to program all Thermal and Throttling control register set.'
14:4	0h RO	**Address Map (ADM):** Hardwired to 11'h000 to indicate at least 32KB address range.
3	0h RO	**Prefetch Memory (PM):** Hardwired to 1'b0 to prevent prefetching.
2:1	2h RO	**Memory Type (MT):** Hardwired to 2'b10 to indicate 64-bit address.
0	0h RO	**Memory or IO Space (MIOS):** Hardwired to 0 to indicate memory space.

10.2.2 Thermal Management Base Address Register (TMBAR_HI_0_0_1_PCI)—Offset 14h

This is the base address for the Thermal Controller Memory Mapped space. There is no physical memory within this 32KB window that can be addressed. The 32KB reserved by this register does not alias to any PCI 2.2 compliant memory mapped space. All TMBAR space maps the access to this memory space towards MCHBAR space. For details of this BAR, refer to the MCHBAR specifications.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Reserved RW (RSVDRW):** Must be set to 0 since addressing above 512GB is not supported.
6:0	0h RW	**TMMBA (TMMBA):** This field corresponds to bits 38 to 32 of the base address TMBAR address space. BIOS will program this register resulting in a base address for a 32KB block of contiguous memory address space. This register ensures that a naturally aligned 32KB space is allocated within total addressable memory space. The DPTF driver uses this base address to program all Thermal and Throttling control register set.

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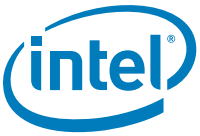


11 Imaging Controller

11.1 Registers Summary

Table 11-1. Summary of IUNIT_CFG Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	(VID_DID)—Offset 0h	A888086h
4h	7h	(PCICMD_PCISTS)—Offset 4h	100000h
8h	Bh	(RID_CC)—Offset 8h	4800000h
Ch	Fh	(CLS_MLT_HT_BIST)—Offset Ch	0h
10h	13h	(ISPMMADR_LOW)—Offset 10h	4h
14h	17h	(ISPMMADR_HIGH)—Offset 14h	0h
2Ch	2Fh	(SVID_SID)—Offset 2Ch	0h
34h	37h	(CAPPOINT)—Offset 34h	70h
3Ch	3Fh	(INTR)—Offset 3Ch	100h
70h	73h	(PCIECAPHDR_PCIECAP)—Offset 70h	92AC10h
74h	77h	(DEVICECAP)—Offset 74h	10008000h
78h	7Bh	(DEVICECTL_DEVICESTS)—Offset 78h	0h
ACh	AFh	(MSI_CAPID)—Offset ACh	80D005h
B0h	B3h	(MSI_ADDRESS_LO)—Offset B0h	0h
B4h	B7h	(MSI_ADDRESS_HI)—Offset B4h	0h
B8h	BBh	(MSI_DATA)—Offset B8h	0h
D0h	D3h	(PMCAP)—Offset D0h	30001h
D4h	D7h	(PMCS)—Offset D4h	8h
16Ch		"(SENSOR_FREQ_CTL)—Offset 16Ch"	0h
170h		"(SENSOR_CLK_CTL)—Offset 170h"	0h

11.1.1 (VID_DID)—Offset 0h

VID_DID - Vendor ID and Device ID Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: A888086h

Bit Range	Default & Access	Field Name (ID): Description
31:23	15h RO/V	**DIDH:** Device Identification Number High (DID_HIGH): Upper 9 bits of Device ID, corresponding to SOC ID. Set by SetIDValue

Bit Range	Default & Access	Field Name (ID): Description
22:18	2h RO	**DIDM:** Device Identification Number Mid (DID_MID): Middle 5 bits of Iunit Device ID Connected to straps at Iunit top level
17:16	0h RO/V	**DIDL:** Device Identification Number Low (DID_LOW): Lower 2 bits of Iunit Device ID. Connected to fuse isp_device_id
15:0	8086h RO	**VENDOR_ID:** Vendor Identification Number (VID): PCI standard identification for Intel.

11.1.2 (PCICMD_PCISTS)—Offset 4h

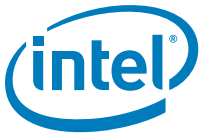
CMD_STS- Command and Status Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RO/V	**SERR_STS:** SERR status
29	0h RW/1C/V	**RMA:** Received Master Abort (MA): Set when IUNIT recieve UR
28	0h RW/1C/V	**RTA:** Received Target Abort (RTA): Set when IUNIT recieve CA
27	0h RW/1C/V	**STA:** Signaled Target Abort (STA): Set when IUNIT recieve P/NP transaction which is CA
26:21	0h RO	Reserved.
20	1h RO	**CAPLIST:** Capability List (CAP): Indicates that the CAPPOINT register at 34h provides an offset into PCI Configuration Space containing a pointer to the location of the first item in the list.
19	0h RO/V	**INTA_STATUS:** Interrupt Status (IS): Reflects the state of the interrupt in the camera device. Is set to 1 if IER and IIR are both set. Otherwise is set to 0.
18:11	0h RO	Reserved.
10	0h RW	**INTA_DISABLE:** Interrupt Disable (ID): When 1, blocks the sending of ASSERT_INTA and DEASSERT_INTA messages to the Intel Legacy Block (ILB). The interrupt status is not blocked from being reflected in PCICMDSTS.IS. When 0, permits the sending of ASSERT_INTA and DEASSERT_INTA messages to the ILB.
9	0h RW	**FastB2B**



Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**SERR_EN**
7	0h RO	Reserved.
6	0h RW	**Parity_Err**
5	0h RW	**VGA_Snp**
4	0h RW	**MWrInv**
3	0h RW	**SPECIAL_CYCLE**
2	0h RW	**BME:** Bus Master Enable (BME): Enables ISP to function as a PCI compliant master. When 0, blocks the sending of MSI interrupts. When 1, permits the sending of MSI interrupts.
1	0h RW	**MSE:** Memory Space Enable (MSE): When set, accesses to this device's memory space is enabled. When 1, the ISP will compare the incoming address on the IOSF bus with ISPMMADR_BAR(31:22). If there is a match and if the IOSF command is either a MEMRD or MEMWR, the ISP will select the command and direct it to internally addressed entity. When 0, the ISP will not claim MEMRD or MEMWR IOSF commands.
0	0h RW	**IOAE:** IO Space Enable - IUNIT doesn't expect to get IO commands.

11.1.3 (RID_CC)—Offset 8h

RID_CC - Revision ID and Class Code Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 4800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	4h RO	**BASECLASS_CODE:** Base-Class Code (BCC): 04h indicates a multimedia device
23:16	80h RO	**SUBCLASS_CODE:** Sub-Class Code: (SCC): 80h indicates a video device
15:8	0h RO	**PROGRAMMING_INTERFACE:** Programming Interface (PI): Default programming interface
7:0	0h RO/V	**REVISION_ID:** Revision ID (RID): The value in this field is set by the setIDValue message

11.1.4 (CLS_MLT_HT_BIST)—Offset Ch

CLS_MLT_HT_BIST - Cache Line Size, Master Latency Timer, Header Type and BIST Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**BIST:** Built In Self Test
23:16	0h RO	**HEADER_TYPE:** Header Type (HDR): Indicates a type 0 header format.
15:8	0h RO	**LATENCY_TIMER:** Latency Timer
7:0	0h RW	**CACHELINE_SIZE:** Cache Line Size: Value is ignored. This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no effect on any PCI Express device behavior.

11.1.5 (ISPMMADR_LOW)—Offset 10h

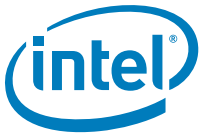
BAR_LOW - Low Part of Base Address Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**BASE_ADDR:** Base Address (BA): Set by the OS, these bits correspond to address signals (31:24). The ISP will compare the IOSF address (38:24) with {ISPMMADR_BAR_HI(6:0), ISPMMADR_BAR_LO(31:24)}. If there is a match, and PCICMDSTS(1) = MSE = 1 and the IOSF command is either a MEMRD or MEMWR, the ISP will select the command and direct it to internally addressed entity.
23:4	0h RO	**ADDR_MASK:** Address Mask: Hardwired to 0s to indicate at least 16MB address range
3	0h RO	**PREFETCHABLE:** Prefetchable Memory: Hardwired to 0 to prevent prefetching



Bit Range	Default & Access	Field Name (ID): Description
2:1	2h RO	**TYPE:** Memory Type - 2h indicates 64 bit wide addressing
0	0h RO	**MESSAGE_SPACE:** Message Space - 0h indicates memory space

11.1.6 (ISPMMADR_HIGH)—Offset 14h

BAR_HIGH - High Part of Base Address Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6:0	0h RW	**BASE_ADDR:** Base Address MSB

11.1.7 (SVID_SID)—Offset 2Ch

SVID_SID - Subsystem Vendor ID and Subsystem ID Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEM_ID:** Subsystem ID (SSID): Written by BIOS after reset, can be changed only after a reset cycle
15:0	0h RW/O	**SUBSYSTEM_VENDOR_ID:** Subsystem Vendor ID (SSVID):Written by BIOS after reset, can be changed only after a reset cycle

11.1.8 (CAPPOINT)—Offset 34h

CAPPTR - Capabilities Pointer Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 70h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	70h RO	**CAPABILITY_PTR:** Capabilities Pointer (CAP): CAPABILITIES_POINTER: This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the CAPID0 register at offset 70h

11.1.9 (INTR)—Offset 3Ch

INTR - Interrupt Properties Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MaxLat:** MaxLat
23:16	0h RO	**MinLat:** MinLat
15:8	1h RO	**INTERRUPT_PIN:** Interrupt Pin (IPIN): PCI Device 0/3/0 (IUNIT) is a single function device. If INTx is used, the PCI spec requires that it use INTA#. If INTx is used (FB_intx_supported fuse is 1), then this field is hard coded to 01h. If INTx is not used (FB_intx_supported fuse is 0), this field is hard coded to 00h. 1h indicates INTA
7:0	0h RW	**INTERRUPT_LINE:** Interrupt Line (ILIN): BIOS written value to communicate interrupt line routing information to the ISP device driver.

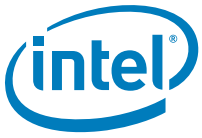
11.1.10 (PCIECAPHDR_PCIECAP)—Offset 70h

PCIE Capabilities Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 92AC10h



Bit Range	Default & Access	Field Name (ID): Description
31:16	92h RO	**PCIE_CAP:** PCIE_CAP: Bits 15:14: Reserved, 0 Bits 13:9: Interrupt Message Number (INTMSG): Since this device only supports one MSI vector, this field is hardwired to 0. Bit 8: Slot Implemented (SLOTIMP): Hardwired to 0 for any endpoint device. Bits 7:4: DevicePort Type: Indicates the specific type of this PCI Express function. 1001b indicates a Root Complex Integrated Endpoint Bits 3:0 Capability Version: Must be hardwired to 2h for Functions compliant to PCI Express 3.0 Base Specification.
15:8	ACh RO	**NEXT_PTR:** Next Capability Pointer: (PCIE_NEXT_CAP): Indicates the next item in the capabilities list or 00h if no other items exist in the linked list of capabilities.
7:0	10h RO	**CAPABILITY_ID:** Capability ID (PCIE_CAPID): Indicates the PCI Express Capability structure. This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure

11.1.11 (DEVICECAP)—Offset 74h

Capabilities Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 10008000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	10008000h RO	**DEVICECAP:** DEVICECAP: Bits 31:29: Reserved, 0 Bit 28: (FLRCAP): A value of 1b indicates the Function supports the optional Function Level Reset mechanism. Bits 27:26: Power Limit Scale: Not applicable , hardwired to 00b Bits 25:18: Power Limit Value: Not applicable , hardwired to 00b Bits 17:16: Reserved, 0. Bit 15: Role-base Error Reporting (RBER): When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1 Bits 14:12: Reserved, 0. Bits 11:9: Endpoint L1 Acceptable Latency: This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L1 state to the L0 state. Bits 8:6: Endpoint L0s Acceptable Latency: This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L0s state to the L0 state. Bit 5: Extended Tag Field Supported: This bit indicates the maximum supported size of the Tag field as a Requester. Bits 4:3: Phantom Functions Supported: This field indicates the support for use of unclaimed Function Numbers to extend the number of outstanding transactions for PCIe devices. Bits 2:0: Max_Payload_Size Supported: This field indicates the maximum payload size that the Function can support for TLPs. 000b represents 128 bytes, the minimum allowed value.

11.1.12 (DEVICECTL_DEVICESTS)—Offset 78h

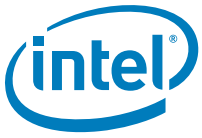
PCI Express Device Capabilities and Control Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RO/V	**DEVICESTS:** Transaction Pending bit: When Set, this bit indicates that the Function has issued Non-Posted Requests that have not been completed. A Function reports this bit is cleared only when all outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. This bit must also be cleared upon the completion of an FLR.
20	0h RO	**Relax_Ord_En:** AUX Power Detected: Not used, 0
19	0h RW/1C/V	**UR_Req_Det:** Unsupported Request Detected - set when IUNIT recieve P/NP transaction which is UR



Bit Range	Default & Access	Field Name (ID): Description
18:16	0h RO	**DEVICECTL_MISC_STS:** DEVICESTS Bits 2:0: Various error detected bits: The Root Complex Integrated Endpoint does not use the PCI Express error reporting mechanism. Always return 0.
15	0h RW	**INIT_FLR:** Initiate Function Level Reset: A write of 1b initiates Function Level Reset to the Function. The value read by software from this bit is always 0b.
14:0	0h RO	**DEVICECTL_MISC_CTRL:** DEVICECTL - Misc RO ctrl bits. the only bit set reflect Unsupported-Request-Reporting Enable

11.1.13 (MSI_CAPID)—Offset ACh

MSI_CAPID - MSI Capabilities and MSI Control Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 80D005h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**AC64:** 64-bit Address Capable (C64): PCIe devices must support 64b MSI addressing.
22:20	0h RW	**MME:** Multiple Message Enable (MME): This field is RW for software compatibility, but only a single message is ever generated.
19:17	0h RO	**MMC:** Multiple Message Capable (MMC)- 3'h0 indicates one outstanding message is supported
16	0h RW	**MSIEN:** MSI Enable (MSIE): If set, MSI is enabled. PCICMDSTS.BME must be set for an MSI to be generated. When 0, blocks the sending of a MSI interrupt. The interrupt status is not blocked from being reflected in the PCICMDSTS.IS bit. When 1, permits sending of a MSI interrupt.
15:8	D0h RO	**NEXT_PTR:** Next Capability Pointer (MSI_NEXT_CAP): This contains a pointer to the next item in the capabilities list which is the Power Management capability
7:0	5h RO	**CAPABILITY_ID:** MSI Capability (MSI_CAPID): Indicates an MSI capability.

11.1.14 (MSI_ADDRESS_LO)—Offset B0h

MSI Address Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**MSI_ADDR:** MSI Address: System specified message address, always DW aligned.
1:0	0h RO	Reserved.

11.1.15 (MSI_ADDRESS_HI)—Offset B4h

MSI Address Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6:0	0h RW	**MSI_ADDR:** MSI Address: Upper 32 bits of the system specified message address.

11.1.16 (MSI_DATA)—Offset B8h

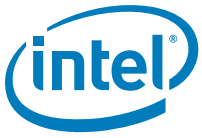
MSI Data Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**MSI_DATA:** MSI Data (MD): This 16-bit field is programmed by system software and is driven onto the lower word of data during the data phase of the MSI write transaction. When the ISP issues an MSI interrupt as a MEMWR on the IOSF, the write data corresponds to the value of this field.



11.1.17 (PMCAP)—Offset D0h

Power Management Capabilities

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 30001h

Bit Range	Default & Access	Field Name (ID): Description
31:16	3h RO	**PMCAP:** PM Capability: Bits 31:27: PME Support (PMES): The camera controller does not generate PME#. Bit 26: D2_SUPPORT (D2S): The D2 power management state is not supported. Bit 25: D1_SUPPORT (D1S): The D1 power management state is not supported. Bits 24:22: Reserved Bit 21: Device Specific Initialization (DSI): Hardwired to 0 to indicate that no special initialization of the camera controller is required before generic class device driver is to use it. Bits 20:19: Reserved Bits 18:16: Version (VS): Indicates compliance with revision 1.2 of the PCI Power Management Specification.
15:8	0h RO	**NEXT_PTR:** Next Capability Pointer (PM_NEXT_CAP): End of List
7:0	1h RO	**CAPABILITY_ID:** PM Capability ID (PM_CAPID): SIG defines this ID is 01h for power management

11.1.18 (PMCS)—Offset D4h

Power Management Control/Status

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 3 **Function:** 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/V	**PMES:** Power Management Event Status: Not used; No PME from D3cold. we put it as RW1C just to be complient w/ PCI spec
14:13	0h RO	**DS:** Data Scale: Not used
12:9	0h RO	**DSEL:** Data Select: Not used
8	0h RO	**PMEEN:** Power Management Event Enable

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3	1h RO	**NSR:** No Soft Reset (NSR): This read-only bit indicates that the device does not lose internal state on a D3hot to D0 transition. This means: The internal state is not reset on a D3 (D3hot actually) to D0 transition and no additional operating system intervention is required to preserve the state A transition from D3 to D0 will NOT cause the IP to return to D0 un-initialized. The Iunit+PUnit will restore the state of the IP configuration and MMIO registers .
2	0h RO	Reserved.
1:0	0h RW/V	**PS:** Power State (PS): : Power management is implemented by writing to control registers in the PUNIT. This field may be programmed by the software driver, but no action is taken based on writing to this field

11.1.19 (SENSOR_FREQ_CTL)—Offset 16Ch

Sets the Optional sensor frequency

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

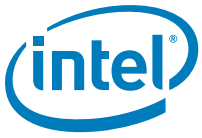
Default: 0h

Range	Access Type	Default (reset)	Description
31:31	RW	0x0 (rst)	**start** Start: When '1', the sensor
30:0	RW	0x0 (rst)	**freq_spec** Optional sensor frequency. For SoC can specify 6.75, 8, 19.2, 9.6, 14.4, 24, 26MHz.

11.1.20 (SENSOR_CLK_CTL)—Offset 170h

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Range	Access Type	Default (reset)	Description
7:7	RW	0x0 (rst)	**osc_clk3_sel** OSC_CLOCK_OUT3_Select: If 1, selects Opt sensor clk to drive OSC_CLK_OUT3; otherwise 24MHz clock drive to OSC_CLK_OUT3
6:6	RW	0x0 (rst)	**osc_clk3_en** OSC_CLOCK_OUT3_Enable: If 1, enables selected clock to drive OSC_CLK_OUT3
5:5	RW	0x0 (rst)	**osc_clk2_sel** OSC_CLOCK_OUT2_Select: If 1, selects Opt sensor clk to drive OSC_CLK_OUT2; otherwise 24MHz clock drive to OSC_CLK_OUT2
4:4	RW	0x0 (rst)	**osc_clk2_en** OSC_CLOCK_OUT2_Enable: If 1, enables selected clock to drive OSC_CLK_OUT2
3:3	RW	0x0 (rst)	**osc_clk1_sel** OSC_CLOCK_OUT1_Select: If 1, selects Opt sensor clk to drive OSC_CLK_OUT1; otherwise 24Hz clock drive to OSC_CLK_OUT1
2:2	RW	0x0 (rst)	**osc_clk1_en** OSC_CLOCK_OUT1_Enable: If 1, enables selected clock to drive OSC_CLK_OUT1
1:1	RW	0x0 (rst)	**osc_clk0_sel** OSC_CLOCK_OUT0_Select: If 1, selects Opt sensor clk to drive OSC_CLK_OUT0; otherwise 24MHz clock drive to OSC_CLK_OUT0
0:0	RW	0x0 (rst)	**osc_clk0_en** OSC_CLOCK_OUT0_Enable: If 1, enables selected clock to drive OSC_CLK_OUT0

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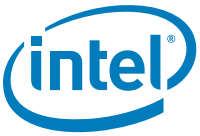


12 Audio Controller

12.1 Registers Summary

Table 12-1. Summary of HDAHC_CFGREG Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Vendor Identification (VID)—Offset 0h	8086h
2h	3h	Device ID (DID)—Offset 2h	8C20h
4h	5h	Command (CMD)—Offset 4h	0h
6h	7h	Status (STS)—Offset 6h	10h
8h	8h	Revision Identification (RID)—Offset 8h	0h
9h	9h	Programming Interface (PI)—Offset 9h	0h
Ah	Ah	Sub Class Code (SCC)—Offset Ah	3h
Bh	Bh	Base Class Code (BCC)—Offset Bh	4h
Ch	Ch	Cache Line Size (CLS)—Offset Ch	0h
Dh	Dh	Latency Timer (LT)—Offset Dh	0h
Eh	Eh	Header Type (HTYPE)—Offset Eh	0h
Fh	Fh	Built-in Self Test (BIST)—Offset Fh	0h
10h	13h	Intel HD Audio Base Lower Address (HDALBA)—Offset 10h	4h
14h	17h	Intel HD Audio Base Upper Address (HDAUBA)—Offset 14h	0h
18h	1Bh	Shadowed PCI Configuration Lower Base Address (SPCLBA)—Offset 18h	4h
1Ch	1Fh	Shadowed PCI Configuration Upper Base Address (SPCUBA)—Offset 1Ch	0h
20h	23h	Audio DSP Lower Base Address (ADSPLBA)—Offset 20h	4h
24h	27h	Audio DSP Upper Base Address (ADSPUBA)—Offset 24h	0h
2Ch	2Dh	Subsystem Vendor ID (SVID)—Offset 2Ch	0h
2Eh	2Fh	Subsystem ID (SID)—Offset 2Eh	0h
34h	34h	Capability Pointer (CAPPTR)—Offset 34h	50h
3Ch	3Ch	Interrupt Line (INTLN)—Offset 3Ch	0h
3Dh	3Dh	Interrupt Pin (INTPN)—Offset 3Dh	1h
43h	43h	Test Mode 1 register (TM1)—Offset 43h	0h
50h	51h	PCI Power Management Capability ID (PID)—Offset 50h	6001h
60h	61h	MSI Capability ID (MID)—Offset 60h	7005h
62h	63h	MSI Message Control (MMC)—Offset 62h	80h
64h	67h	MSI Message Lower Address (MMLA)—Offset 64h	0h
68h	6Bh	MSI Message Upper Address (MMUA)—Offset 68h	0h
6Ch	6Dh	MSI Message Data (MMD)—Offset 6Ch	0h
70h	71h	PCI Express Capability ID (PXID)—Offset 70h	10h
72h	73h	PCI Express Capabilities (PXC)—Offset 72h	91h
74h	77h	Device Capabilities (DEVCAP)—Offset 74h	10000000h
78h	79h	Device Control (DEVC)—Offset 78h	2800h

Table 12-1. Summary of HDAHC_CFGREG Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
7Ah	7Bh	Device Status (DEVS)—Offset 7Ah	10h
80h	83h	Vendor Specific Capability Identifiers (VSCID)—Offset 80h	F0146009h
84h	87h	Vendor Specific Extended Capability (VSECID)—Offset 84h	1400010h
8Ch	8Fh	Device Idle Pointer (DEVIDLEPTR)—Offset 8Ch	104A1h
90h	91h	Device Idle Power On Latency (DEVIDLEPOL)—Offset 90h	800h
100h	103h	Virtual Channel Enhanced Capability Header (VCCAP)—Offset 100h	0h
104h	107h	Port VC Capability Register 1 (PVCCAP1)—Offset 104h	1h
108h	10Bh	Port VC Capability Register 2 (PVCCAP2)—Offset 108h	0h
10Ch	10Dh	Port VC Control Register (PVCCTL)—Offset 10Ch	0h
10Eh	10Fh	Port VC Status Register (PVCSTS)—Offset 10Eh	0h
110h	113h	VC0 Resource Capability Register (VC0CAP)—Offset 110h	0h
114h	117h	VC0 Resource Control Register (VC0CTL)—Offset 114h	800000FFh
11Ah	11Bh	VC0 Resource Status Register (VC0STS)—Offset 11Ah	0h
11Ch	11Fh	VCi Resource Capability Register (VCiCAP)—Offset 11Ch	0h
120h	123h	VCi Resource Control Register (VCiCTL)—Offset 120h	0h
126h	127h	VCi Resource Status Register (VCiSTS)—Offset 126h	0h
130h	133h	Root Complex Link Declaration Enhanced (RCCAP)—Offset 130h	10005h
134h	137h	Element Self Description (ESD)—Offset 134h	F000100h
140h	143h	Link 1 Description (L1DESC)—Offset 140h	1h
148h	14Bh	Link 1 Lower Address (L1LADD)—Offset 148h	0h
14Ch	14Fh	Link 1 Upper Address (L1UADD)—Offset 14Ch	0h
0054h		Power Management Control And Status (PCS)—Offset 0054h	8h
0050h		PID_PC—Offset 0050h	C8436001h

12.1.1 Vendor Identification (VID)—Offset 0h

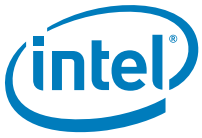
This register identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. FFFFh is an invalid value for Vendor ID.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 8086h

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Indicates that Intel is the vendor.



12.1.2 Device ID (DID)—Offset 2h

This register identifies the particular device. This identifier is allocated by the vendor. This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 8C20h

Bit Range	Default & Access	Field Name (ID): Description
15:0	8C20h RO/V	**Device ID (DID):** Indicates the device number assigned by the SIG. Bits(2:0) of the DID is controlled by fuse. IOSF Sideband Set ID Value message initializes bits 15:7 of this register value, whilst bits 6:0 of this register value are hard coded.

12.1.3 Command (CMD)—Offset 4h

This register provides coarse control over a device's ability to generate and respond to PCI cycles.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved (RSVD):** Read 0.
10	0h RW	**Interrupt Disable (ID):** Enables the device to assert an INTx#. When set, the Intel(r) HD Audio controller's INTx# signal will be de-asserted. When cleared, the INTx# signal may be asserted. Note that this bit does not affect the generation of MSIs.
9	0h RO	**Fast Back to Back Enable (FBE):** Not implemented. Hardwired to 0.
8	0h RW	**SERR Enable (SEN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
7	0h RO	**Wait Cycle Control (WCC):** Not implemented. Hardwired to 0.
6	0h RW	**Parity Error Response (PER):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
5	0h RO	**VGA Palette Snoop (VPS):** Not implemented. Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Memory Write and Invalidate Enable (MWI):** Not implemented. Hardwired to 0.
3	0h RO	**Special Cycle Enable (SCE):** Not implemented. Hardwired to 0.
2	0h RW	**Bus Master Enable (BME):** • 1: Enable • 0: Disable Controls standard PCI Express bus mastering capabilities for Memory and IO, reads and writes. Note that this also controls MSI generation since MSI are essentially Memory writes.
1	0h RW	**Memory Space Enable (MSE):** When set, enables memory space accesses to the Intel HD Audio controller.
0	0h RO	**I/O Space (IOS):** The Intel HD Audio controller does not implement IO Space, therefore this bit is hardwired to 0.

12.1.4 Status (STS)—Offset 6h

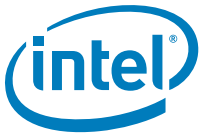
This register is used to record status information for PCI bus related events

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 10h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** Not implemented. Hardwired to 0.
14	0h RO	**SERR# Status (SERRS):** Not implemented. Hardwired to 0.
13	0h RW/1C/V	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, this bit is set. SW writes a 1 to this bit to clear it.
12	0h RW/1C/V	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, this bit is set. SW writes a 1 to this bit to clear it.
11	0h RO	**Signaled Target-Abort (STA):** Not implemented. Hardwired to 0.
10:9	0h RO	**DEVSEL# Timing Status (DEVT):** Does not apply. Hardwired to 0.
8	0h RO	**Master Data Parity Error (MDPE):** Not implemented. Hardwired to 0.
7	0h RO	**Fast Back to Back Capable (FBC):** Does not apply. Hardwired to 0.



Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RO	**66 MHz Capable (C66):** Does not apply. Hardwired to 0.
4	1h RO	**Capabilities List Exists (CLIST):** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	0h RO/V	**Interrupt Status (IS):** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register). Note that this bit is not set by an MSI.
2:0	0h RO	**Reserved (RSVD0):** Reserved.

12.1.5 Revision Identification (RID)—Offset 8h

This register specifies a device specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. This field should be viewed as a vendor defined extension to the Device ID. This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO/V	**Revision ID (RID):** Indicates the device specific revision identifier. IOSF Sideband Set ID Value message initializes this register value.

12.1.6 Programming Interface (PI)—Offset 9h

This register identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW/L	**Programming Interface (PI):** Value assigned to the Intel HD Audio subsystem. Locked when FNCFG.BCLD = 1.

12.1.7 Sub Class Code (SCC)—Offset Ah

This register identifies more specifically the function of the device This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 14 **Function:** 0

Default: 3h

Bit Range	Default & Access	Field Name (ID): Description
7:0	3h RW/L	**Sub Class Code (SCC):** This indicates the device is an Intel HD Audio audio device, in the context of a multimedia device. Locked when FNCFG.BCLD = 1.

12.1.8 Base Class Code (BCC)—Offset Bh

This register broadly classifies the type of function the device performs This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 14 **Function:** 0

Default: 4h

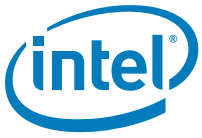
Bit Range	Default & Access	Field Name (ID): Description
7:0	4h RW/L	**Base Class Code (BCC):** This register indicates that the function implements a multimedia device. Locked when FNCFG.BCLD = 1.

12.1.9 Cache Line Size (CLS)—Offset Ch

This specifies the system cache line size in units of DWORDs.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 14 **Function:** 0



Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Cache Line Size (CLS):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the SoC.

12.1.10 Latency Timer (LT)—Offset Dh

This register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW/L	**Latency Timer (LT):** Doesn't apply to PCI Express. RO as 00h if PCI Express. If configured to appear as PCI device, maintain RW for Legacy PCI SW compliance. Locked when FNCFG.HDASPCID = 0.

12.1.11 Header Type (HTYPE)—Offset Eh

This register identifies the layout of the second part of the predefined header and also whether or not the device contains multiple functions.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/L	**Multi Function Device (MFD):** Value of 0 indicates a single function device. Value of 1 indicates a multi function device. Locked when FNCFG.BCLD = 1.
6:0	0h RO	**Header Type (HTYPE):** Implements Type 0 Configuration header.

12.1.12 Built-in Self Test (BIST)—Offset Fh

This optional register is used for control and status of BIST.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Built-in Self Test (BIST):** Not implemented in the Intel HD Audio subsystem. Hardwired to 00h.

Intel HD Audio Base Lower Address (HDALBA)—Offset 10h

This BAR creates a selected size of memory space to signify the base address (lower 32 bits) of the Intel HD Audio memory mapped configuration registers depending on implementation.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 4h

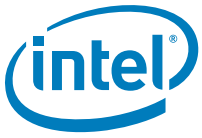
Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RW	**Lower Base Address (LBA):** Base address for the Intel HD Audio subsystem's memory mapped configuration registers. 16 Kbytes are requested by hardwiring bits 13:4 to 0.
13:4	0h RO	**Reserved (RSVD):** Reserved. Hardwired to 0.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

12.1.13 Intel HD Audio Base Upper Address (HDAUBA)—Offset 14h

This BAR creates a selected size of memory space to signify the base address (upper 32 bits) of the Intel HD Audio memory mapped configuration registers, depending on implementation.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0



Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Intel HD Audio Upper Base Address (UBA):** Upper 32 bits of the Base address for the Intel(r) HD Audio controller's memory mapped configuration registers.

12.1.14 Shadowed PCI Configuration Lower Base Address (SPCLBA)—Offset 18h

This BAR creates 4 Kbytes of memory space to signify the base address (lower 32 bits) of the shadowed PCI configuration when used as an ACPI device.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW/L	**Lower Base Address (LBA):** Base address for the PCI Configuration register shadowed to memory mapped. 4 KB is requested by hardwiring bits 11:4 to 0. Locked when PCICFGCTL0.SPCBAD = 1.
11:4	0h RO	**Reserved (RSVD):** Reserved. Hardwired to 0.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO/V	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

12.1.15 Shadowed PCI Configuration Upper Base Address (SPCUBA)—Offset 1Ch

This BAR creates 4 Kbytes of memory space to signify the base address (upper 32 bits) of the shadowed PCI configuration when used as an ACPI device.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Upper Base Address (UBA):** Upper 32 bits of the Base address for the PCI Configuration register shadowed to memory mapped. Locked when PCICFGCTL0.SPCBAD = 1.

12.1.16 Audio DSP Lower Base Address (ADSPLBA)—Offset 20h

This BAR creates a selected size of memory space to signify the base address (lower 32 bits) of the Audio DSP memory mapped configuration registers depending on implementation.
The number of LBA bits in this register is depending on the size of the memory window implemented, represented as x in the register table. The x value is determined by the parameter HDMBABC.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Lower Base Address (LBA):** Base address for the Audio DSP memory mapped configuration registers.
19:4	0h RO	**Reserved (RSVD):** Reserved. Hardwired to 0.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

12.1.17 Audio DSP Upper Base Address (ADSPUBA)—Offset 24h

This BAR creates a selected size of memory space to signify the base address (lower 32 bits) of the Audio DSP memory-mapped configuration registers, depending on implementation.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (UBA):** Upper 32 bits of the Base address for the Audio DSP memory mapped configuration registers.

12.1.18 Subsystem Vendor ID (SVID)—Offset 2Ch

This register should be implemented for any function that could be instantiated more than once in a given system, for example, a system with 2 audio subsystems, one down on the motherboard and the other plugged into a PCI expansion slot, should have the SVID register implemented. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one audio subsystem from the other(s).
Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SID to create one 32-bit write. This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/L	**Subsystem Vendor Identifier (SVID):** These RW bits have no functionality. Locked when FNCFG.BCLD = 1.

12.1.19 Subsystem ID (SID)—Offset 2Eh

This register should be implemented for any function that could be instantiated more than once in a given system, for example, a system with 2 audio subsystems, one down on the motherboard and the other plugged into a PCI expansion slot. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other(s). Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SVID to create one 32-bit write. This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/L	**Subsystem Identifier (SID):** These RW bits have no functionality. Locked when FNCFG.BCLD = 1.

12.1.20 Capability Pointer (CAPPTR)—Offset 34h

This optional register is used to point to a linked list of new capabilities implemented by this device.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 14 **Function:** 0

Default: 50h

Bit Range	Default & Access	Field Name (ID): Description
7:0	50h RO	**Capability Pointer (CAPPTR):** Indicates that the first capability pointer offset is offset 50h (Power Management Capability).

12.1.21 Interrupt Line (INTLN)—Offset 3Ch

The register is used to communicate interrupt line routing information. This register is not affected by FLR.
Implementation Notes: Due to legacy implementation of the INTLN field being implemented as reset by D3HOT to D0 Reset but not FLR and already work well with existing SW (despite FLR section in PCIe Specification does not have this register in the preservation list), this legacy implementation remains no change and documented here as reset by D3ONLY, which is a deviation from D3RST definition by excluding FLR.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (INTLN):** Hardware does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

12.1.22 Interrupt Pin (INTPN)—Offset 3Dh

This register tells which interrupt pin the device (or device function) uses. This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 14 **Function:** 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved (RSVD):** Reserved.
3:0	1h RW/L	**Interrupt Pin (INTPN):** Identifies the interrupt pin the function uses. • 0h: No interrupt pin • 1h: INTA • 2h: INTB • 3h: INTC • 4h: INTD • 5h Fh: reserved Locked when FNCFG.BCLD = 1.

12.1.23 Test Mode 1 register (TM1)—Offset 43h

This register provides some test mode policy for the functional operations.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Fast Reset (FRESET):** Fast Reset is a test mode operation used to reduce the wait time from the start of AZA_BCLK to AZA_RST# de-assertion. It is meant to be used to speed up simulations. • 0: 9 frames • 1: 1 frame This is also used to hasten the wait time required before DOCKAZRST# can be de-asserted after DockAttach bit has been set. Assertion of this bit causes the wait time to reduce from at least 2400 BitClks to 4 BitClks. Assertion of this bit reduces the frame wait time (in dock attach process) for codec enumeration from 32 to 4. Programmed before GCTL.CRSTB = 1.
6:0	0h RO	Reserved.

12.1.24 PCI Power Management Capability ID (PID)—Offset 50h

This register declares the power management capability structure.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 6001h

Bit Range	Default & Access	Field Name (ID): Description
15:8	60h RW/L	**Next Capability (NEXT):** Points to the next capability structure (MSI). Locked when FNCFG.BCLD = 1.
7:0	1h RO	**Cap ID (CAP):** Indicates that this pointer is a PCI power management capability.

12.1.25 MSI Capability ID (MID)—Offset 60h

This register declares the MSI capability structure. NEXT field is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 7005h

Bit Range	Default & Access	Field Name (ID): Description
15:8	70h RO/V	**Next Capability (NEXT):** Points to the PCI Express* capability structure. The value of this field depends on the FNCFG.HDASPCID bit. When FNCFG.HDASPCID is 0 , this field has a value of 70h where it points to the PCI Express capability structure. When FNCFG.HDASPCID bit is 1, this field has a value of 00h to indicate that this is the last capability structure in the list.
7:0	5h RO	**Cap ID (CAP):** Indicates that this pointer is a MSI capability.

12.1.26 MSI Message Control (MMC)—Offset 62h

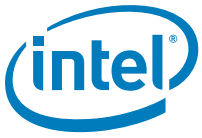
This register provides system software control over MSI.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**64b Address Capability (ADD64):** Indicates the ability to generate a 64-bit message address.
6:4	0h RO	**Multiple Message Enable (MME):** Normally this is a R/W register. However, since only 1 message is supported, these bits are hardwired to 000 = 1 message.
3:1	0h RO	**Multiple Message Capable (MMC):** Hardwired to 0 indicating request for 1 message.
0	0h RW	**MSI Enable (ME):** If set to 1 an MSI will be generated instead of an INTx#signal. If set to 0, an MSI may not be generated.

12.1.27 MSI Message Lower Address (MMLA)—Offset 64h

This register specifies the MSI message address (lower 32 bits).

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**MSI Message Lower Address (MMLA):** Lower Address used for MSI Message.
1:0	0h RO	**Reserved (RSVD):** Reserved.

12.1.28 MSI Message Upper Address (MMUA)—Offset 68h

This register specifies the MSI message address (Upper 32 bits).

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSI Message Upper Address (MMUA):** Upper 32 bits of address used for MSIMessage.

12.1.29 MSI Message Data (MMD)—Offset 6Ch

This register specifies the MSI message data.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**MSI Message Data (MMD):** Data used for MSI Message.

12.1.30 PCI Express Capability ID (PXID)—Offset 70h

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 10h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Next Capability (NEXT):** Indicates that this is the last capability structure inthe list.
7:0	10h RO	**Cap ID (CAP):** Indicates that this pointer is a PCI Express capability structure.

12.1.31 PCI Express Capabilities (PXC)—Offset 72h

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 91h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved (RSVD):** Reserved.
13:9	0h RO	**Interrupt Message Number (IMN):** Hardwired to 0.
8	0h RO	**Slot Implemented (SI):** Hardwired to 0.
7:4	9h RO	**Device/Port Type (DPT):** Indicates that this is a Root Complex IntegratedEndpoint Device.
3:0	1h RO	**Capability Version (CV):** Indicates version #1 PCI Express capability.

12.1.32 Device Capabilities (DEVCAP)—Offset 74h

This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 10000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD1):** Reserved.
28	1h RW/L	**Functional Level Reset (FLR):** A 1 indicates that the Intel HD Audio subsystem supports the Function Level Reset capability. Locked when FNCFG.BCLD = 1.
27:26	0h RO	**Captured Slot Power Limit Scale (SPLS):** Hardwired to 0.
25:18	0h RO	**Captured Slot Power Limit Value (SPLV):** Hardwired to 0.
17:15	0h RO	**Reserved (RSVD0):** Reserved.
14	0h RO	**Power Indicator Present (PIP):** Hardwired to 0.
13	0h RO	**Attention Indicator Present (AIP):** Hardwired to 0.
12	0h RO	**Attention Button Present (ABP):** Hardwired to 0.
11:9	0h RW/L	**Endpoint L1 Acceptable Latency (L1CAP):** This bit field is defined in the PCI Express spec as RO. At this time it is risky to assign a hardwired value to this bit field. Making it RW would cause a WHQL failure. By making it RW/L it will appear as RO to WHQL testing while allowing BIOS to write a value at boot that is determined by post silicon system testing. Locked when FNCFG.BCLD = 1.
8:6	0h RW/L	**Endpoint L0s Acceptable Latency (L0SCAP):** This bit field is defined in the PCI Express spec as RO. At this time it is risky to assign a hardwired value to this bit field. Making it RW would cause a WHQL failure. By making it RW/L it will appear as RO to WHQL testing while allowing BIOS to write a value at boot that is determined by post silicon system testing. Locked when FNCFG.BCLD = 1.
5	0h RO	**Extended Tag Field Support (ETCAP):** Indicates 5 bit tag supported.
4:3	0h RO	**Phantom Functions Supported (PFCAP):** Indicates phantom functions not supported.
2:0	0h RO	**Max Payload Size Supported (MPCAP):** Indicates 128B maximum payloadsize capability.

12.1.33 Device Control (DEVC)—Offset 78h

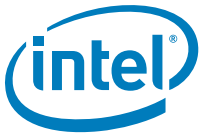
NSNPEN bit is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 2800h

Bit Range	Default & Access	Field Name (ID): Description
15	0h WO	**Initiate FLR (IF):** Used to initiate FLR transition. A write of 1 initiates FLR transition. Since hardware must not respond to any cycles until FLR completion, the read value by software from this bit is 0.
14:12	2h RW	**Max Read Request Size (MRRS):** This field sets the maximum Read Request size for the Function as a Requester. The Function must not generate Read Requests with size exceeding the set value. Defined encodings for this field are: • 000: 128 B • 001: 256 B • 010: 512 B • 011: 1024 B • 100: 2048 B • 101: 4096 B • 110 - 111: Reserved
11	1h RW	**Enable No Snoop (NSNPEN):** When set to 1 (or EM2.FNSNPEN = 1) the Intel HD Audio controller is permitted to set the No Snoop bit in the Requester Attributes of a bus master transaction. In this case VC0, VCp, or VC1 may be used for isochronous transfers. When set to 0 (and EM2.FNSNPEN = 0) the Intel HD Audio controller will not set the No Snoop bit. In the case isochronous transfers will not use VC1(VCi) even if it is enabled since VC1 is never snooped. Isochronous transfers will use either VCp or VC0. This bit is not affected by D3HOT to D0 reset or FLR.
10	0h RO	**Auxiliary (AUX) Power PM Enable (AUXPEN):** Hardwired to 0 indicating Intel HD Audio device does not draw AUX power.
9	0h RO	**Phantom Functions Enable (PFEN):** Hardwired to 0 disabling phantom functions.
8	0h RO	**Extended Tag Field Enable (ETEN):** Hardwired to 0 enabling 5-bit tag.
7:5	0h RO	**Max Payload Size (MAXPAY):** Hardwired to 000 indicating 128 B.
4	0h RO	**Enable Relaxed Ordering (ROEN):** Hardwired to 0 disabling relaxed ordering.



Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Unsupported Request Reporting Enable (URREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
2	0h RW	**Fatal Error Reporting Enable (FEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
1	0h RW	**Non-Fatal Error Reporting Enable (NFEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
0	0h RW	**Correctable Error Reporting Enable (CEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.

12.1.34 Device Status (DEVS)—Offset 7Ah

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 10h

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved (RSVD):** Reserved.
5	0h RO/V	**Transactions Pending (TXP):** A 1 indicates that the Intel HD Audio controller has issued Non-Posted requests which have not been completed. A 0 indicates that Completions for all Non-Posted Requests have been received.
4	1h RW/L	**AUX Power Detected (AUXDET):** Hardwired to 1 indicating the device is connected to Suspend power. Programmable by BIOS for the option to declare SUS well wake is supported or not: 1b (SUS well wake supported) or 0b (SUS well wake not supported). Locked when FNCFG.BCLD = 1.
3	0h RO	**Unsupported Request Detected (URDET):** Not implemented. Hardwired to 0.
2	0h RO	**Fatal Error Detected (FEDET):** Not implemented. Hardwired to 0.
1	0h RO	**Non-Fatal Error Detected (NFEDET):** Not implemented. Hardwired to 0.
0	0h RO	**Correctable Error Detected (CEDET):** Not implemented. Hardwired to 0.

12.1.35 Vendor Specific Capability Identifiers (VSCID)—Offset 80h

This register declares the vendor specific capability structure.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: F0146009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor-Specific Capability ID (VSID):** A value of Fh in this 4-bit field identifies this Vendor Specific Capability as an Extended Capability, which uses a VSEC 16-bit Extended Capability ID in the subsequent four bytes. This field allows software to differentiate this capability from other Vendor Specific capabilities.
27:24	0h RO	**Vendor Specific Capability Revision (VSREV):** For a VSID of Fh, this field is reserved 0h.
23:16	14h RO	**Vendor Specific Capability Length (VSLEN):** This field indicates the # of bytes of this Vendor Specific capability as required by the PCI spec inclusive of the CapID and Next Pointer.
15:8	60h RW/L	**Next Capability (NEXT):** Points to the next capability structure (MSI). Locked when FNCFG.BCLD = 1.
7:0	9h RO	**Cap ID (CAP):** Indicates that this pointer is a vendor specific capability.

12.1.36 Vendor Specific Extended Capability (VSECID)—Offset 84h

This register declares the vendor specific extended capability structure.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**Vendor Specific Extended Capability Length (VSECLEN):** This field indicates the # of bytes of this Vendor Specific capability inclusive of the 1st DW which includes the capability ID and Next pointer. For DevIdle, this is 14h.
19:16	0h RO	**Vendor Specific Extended Capability Revision (VSEREV):** For this revision of DevIdle, this field is 0h.
15:0	10h RO	**Vendor Specific Extended Capability ID (VSECID):** DevIdle has been assigned the Intel VSEC ID of 10h.

12.1.37 Device Idle Pointer (DEVIDLEPTR)—Offset 8Ch

This register specifies the location pointer to the DevIdle register in MMIO space.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 104A1h

Bit Range	Default & Access	Field Name (ID): Description
31:4	104Ah RO	**DevIdle MMIO Offset Location (DEVIDLELOC):** This register contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR.
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0s based BAR Number of the BAR which contains the location of the DevIdle MMIO register.
0	1h RO	**Valid (Valid):** Set to 1 to indicate that the function has implemented a DevIdle register as specified in the DevIdle that can be located using the DEVIDLELOC register and BARNUM.

12.1.38 Device Idle Power On Latency (DEVIDLEPOL)—Offset 90h

This register specifies the device idle power on latency.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved (RSVD0):** Reserved.
12:10	2h RW/L	**Power On Latency Scale (POLS):** Latency Scale multiplier. • 010: 1 us • 011: 32 us All other settings are reserved. The value of this register is multiplied with the Power On Latency Value (POLV) to provide the DevIdle power on exit latency multiplier scale from 1us to 32us. Locked when FNCFG.BCLD = 1.
9:0	0h RW/L	**Power On Latency Value (POLV):** Contains the 0#s based BAR Number of the BAR which contains the location of the DevIdle MMIO register.

12.1.39 Virtual Channel Enhanced Capability Header (VCCAP)—Offset 100h

This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/L	**Next Capability Offset (NXTCAP):** Points to the next capability header, which is the Root Complex Link Declaration Enhanced Capability Header. This register is RW/L to support removing the Root Complex Topology Capability from the PCI Express Extended Capability List. For systems which support the Root Complex Topology Capability Structure, boot BIOS should write a 130h to this register, otherwise boot BIOS should write a 000h to this register.
19:16	0h RW/L	**Capability Version (CV):** This register is RW/L to support removing the PCI Express Extended Capabilities from the Intel HD Audio subsystem. For systems which support the PCI Express Virtual Channel capability and the Root Complex Topology Capability Structure, boot BIOS should write a 1h to this register, otherwise boot BIOS should write a 0h to this register. Locked when FNCFG.BCLD = 1.
15:0	0h RW/L	**PCI Express Extended Capability ID (PCIEECID):** This register is RW/L to support removing the PCI Express Extended Capabilities from the Intel HD Audio subsysterm. For systems which support the PCI Express Virtual Channel capability and the Root Complex Topology Capability Structure, boot BIOS should write a 0002h to this register, otherwise boot BIOS should write a 0000h to this register. Locked when FNCFG.BCLD = 1.

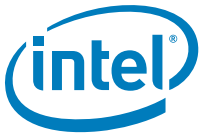
12.1.40 Port VC Capability Register 1 (PVCCAP1)—Offset 104h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved (RSVD2):** Reserved.
11:10	0h RO	**Port Arbitration Table Entry Size (PARBTBLES):** This is an endpoint device therefore this field is hardwired to 0 s.
9:8	0h RO	**Reference Clock (RC):** This is an endpoint device therefore this field is hardwired to 0 s.



Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved (RSVD1):** Reserved.
6:4	0h RO	**Low Priority Extended VC Count (LPVCCNT):** Indicates that only VC0 belongs to the low-priority VC group.
3	0h RO	**Reserved (RSVD0):** Reserved.
2:0	1h RO	**Extended VC Count (VCCNT):** Indicates that one extended VC (in addition to VC0) is supported by the Intel(r) HD Audio controller.

12.1.41 Port VC Capability Register 2 (PVCCAP2)—Offset 108h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**VC Arbitration Table Offset (VCARBTBL):** Hardwired to 0 indicating that a VC Arbitration Table is not present.
23:8	0h RO	**Reserved (RSVD):** Reserved.
7:0	0h RO	**VC Arbitration Capability (VCARBCAP):** Hardwired to 0 s. These bits are not applicable since the Intel HD Audio controller reports a 0 in the Low Priority Extended VC Count field.

12.1.42 Port VC Control Register (PVCCTL)—Offset 10Ch

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	**Reserved (RSVD):** Reserved.
3:1	0h RO	**VC Arbitration Select (VCARBSEL):** Hardwired to 0 s. Normally these bits are RW. But these bits are not applicable since the Intel HD Audio controller reports a 0 in the Low Priority Extended VC Count field.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**Load VC Arbitration Table (LVCARBTBL):** Hardwired to 0 since an arbitration table is not present.

12.1.43 Port VC Status Register (PVCSTS)—Offset 10Eh

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	**Reserved (RSVD):** Reserved.
0	0h RO	**VC Arbitration Table Status (VCARBTBLSTS):** Hardwired to 0 since the VC Arbitration Table is not present.

12.1.44 VC0 Resource Capability Register (VC0CAP)—Offset 110h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Port Arbitration Table Offset (PARBTBL):** Hardwired to 0 since this field is not valid for endpoint devices.
23	0h RO	**Reserved (RSVD1):** Reserved.
22:16	0h RO	**Maximum Time Slots (MTS):** Hardwired to 0 since this field is not valid for endpoint devices.
15	0h RO	**Reject Snoop Transactions (RST):** Hardwired to 0 since this field is not valid for endpoint devices.
14	0h RO	**Advanced Packet Switching (APS):** Hardwired to 0 since this field is not valid for endpoint devices.
13:8	0h RO	**Reserved (RSVD0):** Reserved.
7:0	0h RO	**Port Arbitration Capability (PARBCAP):** Hardwired to 0 since this field is not valid for endpoint devices.

12.1.45 VC0 Resource Control Register (VC0CTL)—Offset 114h

VC0MAP(7:1) field is not affected by FLR.
Implementation Notes: Due to legacy implementation of the VC0MAP field being implemented as reset by D3HOT to D0 Reset but not FLR and already work well with existing SW (and there is no clear definition in the PCI and PCIe Specification whether it should be reset by D3HOT to D0 Reset or not), this legacy implementation remains no change and documented here as reset by D3ONLY, which is a deviation from D3RST definition by excluding FLR.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 800000FFh

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**VC0 Enable (VC0EN):** Hardwired to 1 for VC0.
30:27	0h RO	**Reserved (RSVD2):** Reserved.
26:24	0h RO	**VC0 ID (VC0ID):** Hardwired to 0 since the first VC is always assigned as VC0.
23:20	0h RO	**Reserved (RSVD1):** Reserved.
19:17	0h RO	**Port Arbitration Select (PARBSEL):** Hardwired to 0 since this field is not valid for endpoint devices.
16	0h RO	**Load Port Arbitration Table (LPARBTBL):** Hardwired to 0 since this field is not valid for endpoint devices.
15:8	0h RO	**Reserved (RSVD0):** Reserved.
7:1	7Fh RW	**TC/VC0 Map (VC0MAP):** Bits (7:1) are implemented as R/W bits. This field is not used by the hardware, but it is RW to avoid confusing software.
0	1h RO	**TC/VC0 Map (VC0MAP_0):** Bit 0 is hardwired to 1 since TC0 is always mapped to VC0

12.1.46 VC0 Resource Status Register (VC0STS)—Offset 11Ah

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved (RSVD):** Reserved.
1	0h RO	**VC0 Negotiation Pending (VCNP):** This bit does not apply to the integrated Intel HD Audio device and is therefore hardwired to 0.
0	0h RO	**Port Arbitration Table Status (PARBTBLSTS):** Hardwired to 0 since this field is not valid for endpoint devices.

12.1.47 VCi Resource Capability Register (VCiCAP)—Offset 11Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Port Arbitration Table Offset (PARBTBL):** Hardwired to 0 since this field is not valid for endpoint devices.
23	0h RO	**Reserved (RSVD1):** Reserved.
22:16	0h RO	**Maximum Time Slots (MTS):** Hardwired to 0 since this field is not valid for endpoint devices.
15	0h RO	**Reject Snoop Transactions (RST):** Hardwired to 0 since this field is not valid for endpoint devices.
14	0h RO	**Advanced Packet Switching (APS):** Hardwired to 0 since this field is not valid for endpoint devices.
13:8	0h RO	**Reserved (RSVD0):** Reserved.
7:0	0h RO	**Port Arbitration Capability (PARBCAP):** Hardwired to 0 since this field is not valid for endpoint devices.

12.1.48 VCi Resource Control Register (VCiCTL)—Offset 120h

VCiEN bit and VCiID field are not affected by D3HOT to D0 Reset or FLR.
VCiM(7:1) field is not affected by FLR.
Implementation Notes: Due to legacy implementation of the VCiM field being implemented as reset by D3HOT to D0 Reset but not FLR and already work well with existing SW (and there is no clear definition in the PCI and PCIe Specification whether it should be reset by D3HOT to D0 Reset or not), this legacy implementation remains no change and documented here as reset by D3ONLY, which is a deviation from D3RST definition by excluding FLR.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VCi Enable (VCiEN):** When set to 1, VCi is enabled. This bit is not affected by D3HOT to D0 reset.
30:27	0h RO	**Reserved (RSVD2):** Reserved.
26:24	0h RW	**VCi ID (VCiID):** This fields assigns a VC ID to the VCi resource. This field is not used by the SoC hardware, but it is RW to avoid confusing software. These bits are not affected by D3HOT to D0 reset.
23:20	0h RO	**Reserved (RSVD1):** Reserved.
19:17	0h RO	**Port Arbitration Select (PARBSEL):** Hardwired to 0 since this field is not valid for endpoint devices.
16	0h RO	**Load Port Arbitration Table (LPARBTBL):** Hardwired to 0 since this field is not valid for endpoint devices.
15:8	0h RO	**Reserved (RSVD0):** Reserved.
7:1	0h RW	**TC/VCi Map (VCiM):** This field indicates the TCs that are mapped to the VCi resource. Bits (7:1) are implemented as RW bits. This field is not used by the hardware, but it is RW to avoid confusing software.
0	0h RO	**TC/VCi Map (VCiM_0):** This field indicates the TCs that are mapped to the VCi resource. Bit 0 is hardwired to 0 indicating it can not be mapped to VCi. This field is not used by the hardware.

12.1.49 VCi Resource Status Register (VCiSTS)—Offset 126h

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved (RSVD):** Reserved.
1	0h RO	**VCi Negotiation Pending (VCNP):** This bit does not apply to the integrated Intel HD Audio subsystem and is therefore hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**Port Arbitration Table Status (PARBTBLSTS):** Hardwired to 0 since this field is not valid for endpoint devices.

12.1.50 Root Complex Link Declaration Enhanced (RCCAP)—Offset 130h

Capability Header

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 10005h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Next Capability Offset (NXTCAP):** Indicates this is the last capability.
19:16	1h RO	**Capability Version (CV):** Indicates the version of the capability structure present
15:0	5h RO	**PCI Express Extended Capability ID (PCIEECID):** Indicates that this pointer is a PCI Express Extended Capability

12.1.51 Element Self Description (ESD)—Offset 134h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: F000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	Fh RO	**Port Number (PORT):** Intel HD Audio assigned as Port #15.
23:16	0h RW/L	**Component ID (COMPID):** Indicates the component ID assigned to this element by software. This is written once by platform BIOS and is locked until a platform reset. Locked when FNCFG.BCLD = 1.
15:8	1h RO	**Number of Link Entries (LNKENT):** The Intel HD Audio controller only connects to one device, the SOC egress port. Therefore this field reports a value of 1.
7:4	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RO	**Element Type (ELTYP):** The Intel HD Audio controller is an Integrated Root Complex Device. Therefore this field reports a value of 0h.

12.1.52 Link 1 Description (L1DESC)—Offset 140h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Target Port Number (TPORT):** The Intel HD Audio controller targets the SOC RCRB egress port, which is port #0.
23:16	0h RW/L	**Target Component ID (TCOMPID):** This field is programmed by platform BIOS to match the component ID of the SOC RCRB that is attached to this RCRB Locked when FNCFG.BCLD = 1.
15:2	0h RO	**Reserved (RSVD):** Reserved.
1	0h RO	**Link Type (LNKTYP):** Indicates Type 0.
0	1h RO	**Link Valid (LNKVLD):** Hardwired to 1.

12.1.53 Link 1 Lower Address (L1LADD)—Offset 148h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO/V	**Link 1 Lower Address (L1LADD):** Hardwired to match the RCBA register value in the PCI-LPC bridge.
13:0	0h RO	**Reserved (RSVD):** Reserved.

12.1.54 Link 1 Upper Address (L1UADD)—Offset 14Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 14 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link 1 Upper Address (L1UADD):** Hardwired to match the RCBA register value in the PCI-LPC bridge.

12.1.55 I/O Buffer Control (IOBCTL)—Offset 061Ch

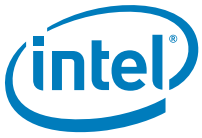
This register allows BIOS to control the I/O buffer configuration based on the motherboard configuration. Notes: 1. Bits 31:26 control the iDISPLAY Audio Link Buffers at the same time that 2. Bits 9:0 control HD-Audio and I2S/SSP Ports 0 and 1 buffers.

Access Method

Type: CR Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 2AC000004h

Range	Access Type	Default (reset)	Description
31:30	RW	0x0 (rst)	**IDSRCP (iDISPLAY Slew Rate Control P)** These bits control the pullup slew rate of the iDISPLAY Audio Link buffers. 00: P Slew Rate for iDISPLAY interface 01: Very slow P Slew Rate 10: Fast P Slew Rate 11: Slow P Slew Rate
29:28	RW	0x0 (rst)	**IDSRCN (iDISPLAY Slew Rate Control N)** These bits control the pulldown slew rate of the iDISPLAY Audio Link buffers. 00: N Slew Rate for iDISPLAY interface 01: Fast N Slew Rate 10: Slow N Slew Rate 11: Very Fast N Slew Rate
27:26	RW	0x3 (rst)	**IDHYS (iDISPLAY Hysteresis Control)** These bits control the hysteresis levels of the iDISPLAY Audio Link buffers. 00: No Hysteresis 01: >80mV (for GTL) 10: >0.1 VCC 11: >80mV (for iDISPLAY)
25:10	RO	0x0 (rst)	**RSVD1 (Reserved)** Reserved for future use



Range	Access Type	Default (reset)	Description
9:8	RW	0x0 (rst)	**OSEL (Ownership Select)** Indicates the ownership of the I/O buffer between Intel HD Audio link vs I2S0 / I2S port. 00: Intel HD-Audio link owns all the I/O buffers. 01: Intel HD-Audio link owns 4 of the I/O buffers for 1 HD-Audio codec connection, and I2S1 port owns 4 of the I/O buffers for 1 I2S codec connection. 10: Reserved. 11: I2S0 and I2S1 ports own all the I/O buffers. Note that the 01 setting is ONLY workable with the new type of Intel HD Audio codec known as Mobile HD Audio codec that does not making use of the reset pin.
7:6	RW	0x0 (rst)	**HDASRCP (HD-Audio Slew Rate Control P)** These bits control the pullup slew rate of the HD-Audio Link buffers. 00: P Slew Rate for HD-A interface 01: Slow P slew rate 10: Reserved 11: Reserved
5:4	RW	0x0 (rst)	**HDASRCN (HD-Audio Slew Rate Control N)** These bits control the pulldown slew rate of the HD-Audio Link buffers. 00: N Slew Rate for HD-A interface 01: Slow N slew rate 10: Reserved 11: Reserved
3:2	RW	0x1 (rst)	**HDAHYS (HD-Audio Hysteresis Control)** These bits control the hysteresis levels of the iDISPLAY Audio Link buffers. 00: No Hysteresis 01: HD-A at 1.8V or 3.3V 10: LPC at 3.3V 11: HD-A at 1.5V
1:1	RW	0x0 (rst)	**VSEL (Voltage Select)** When this bit is cleared to 0, the IO buffers will operate in 3.3V mode drive strength attribute. When this bit is set to 1, the IO buffers will operate in 1.8V mode drive strength attribute. The actual voltage of the IO buffer operation is still depending on the VCCPAZ power pin supplied voltage.
0:0	RO	0x0 (rst)	**RSVD0 (Reserved)** Reserved for future use

12.1.56 Power Management Control And Status (PCS)—Offset 0054h

This register is used to manage the PCI functions power management state as well as to enable/monitor PMEs. PMES and PMEE bits reside in Resume well, and reset by resume reset.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 8h

Range	Access Type	Default (reset)	Description
31:24	RO	0x0 (rst)	**DT (Data)** Does not apply. Hardwired to 0.
23:23	RO	0x0 (rst)	**BPCCE (Bus Power/Clock Control Enable)** Does not apply. Hardwired to 0.
22:22	RO	0x0 (rst)	**B23 (B2/B3 Support)** Does not apply. Hardwired to 0.
21:16	RO	0x0 (rst)	**RSVD3 (Reserved)** Reserved.
15:15	RW/1C/V	0x0 (rst)	**PMES (PME Status)** This bit is set when the Intel HD Audio controller would normally assert the PME# signal independent of the state of the PME bit. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
14:9	RO	0x0 (rst)	**RSVD2 (Reserved)** The Intel HD Audio subsystem does not implement the data register.
8:8	RW	0x0 (rst)	**PMEE (PME Enable)** When set, and if corresponding PMES is also set, the Intel HD Audio subsystem send PME to PMC. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
7:4	RO	0x0 (rst)	**RSVD1 (Reserved)** Reserved.
3:3	RW/L	0x1 (rst)	**NSR (No Soft Reset)** When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. Locked when FNCFG.BCLD = 1.
2:2	RO	0x0 (rst)	**RSVD0 (Reserved)** Reserved.

Range	Access Type	Default (reset)	Description
1:0	RW	0x0 (rst)	**PS (Power State)** This field is used both to determine the current power state of the Intel HD Audio subsystem and to set a new power state. The values are: • 00: D0 state • 1 1: D3HOT state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3HOT states, the Intel HD Audio subsystem's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the D3HOT state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

12.1.57 LTRC_D013C_PCE—Offset 1048h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 8080080h

Range	Access Type	Default (reset)	Description
31:30	RO	0x0 (rst)	**RSVD1_1 (Reserved)** Reserved.
29:29	RW	0x0 (rst)	**HAE (Hardware Autonomous Enable)** If set, then the IP may request a PG whenever it is idle. Note: If this bit is set, then bits[2:0] must be 000.
28:28	RO	0x0 (rst)	**RSVD0 (Reserved)** Reserved.
27:27	RW/L	0x1 (rst)	**SE (Sleep Enable)** If clear, then IP will never asset Sleep to the retention flops. If set, then IP may assert Sleep during PGing. Locked when DFx security policy is not in red unlock state.
26:26	RW	0x0 (rst)	**D3HE (D3-Hot Enable)** If set, then IP will PG when idle and the PMCSR[1:0] register in the IP = '11'.
25:25	RW	0x0 (rst)	**I3E (I3 Enable)** If set, then IP will PG when idle and the D0i3 register (D0i3C[2] = '1') is set. [p]Note: If bits [1:0] = #11#, then the IP would PG whenever either the D3 register or the D0i3 register is set.
24:24	RW	0x0 (rst)	**PMCRE (PMC Request Enable)** If set, then IP will PG when idle and the PMC requests power gating by asserting the pmc_(ip)_sw_pg_req_b signal.
23:20	RO	0x0 (rst)	**RSVD1 (Reserved)** Reserved.
19:19	RW/1C/V	0x1 (rst)	**RR (Restore Required)** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a '1'. This bit will be set on initial power up.

Range	Access Type	Default (reset)	Description
18:18	RW	0x0 (rst)	**I3 (D0i3)** SW sets this bit to '1' to move the IP into the D0i3 state. Writing this bit to ' 0' will return the IP to the fully active D0 state (D0i0).
17:17	RW	0x0 (rst)	**IR (Interrupt Request)** SW sets this bit to '1' to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
16:16	RO/V	0x0 (rst)	**CIP (Command-In-Progress)** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.
15:0	RO	0x0 (rst)	**RSVDP0 (Reserved)** Reserved.

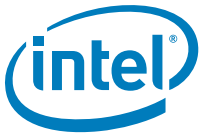
12.1.58 PID_PC—Offset 0050h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: C8436001h

Range	Access Type	Default (reset)	Description
31:27	RW/L	0x19 (rst)	**PMES (PME_Support)** Indicates PME# can be generated from D3 and D0 states. Programmable by BIOS for the option to declare SUS well wake is supported or not: 19h (SUS well wake supported) or 09h (SUS well wake not supported). Locked when FNCFG.BCLD = 1.
26:26	RO	0x0 (rst)	**D2S (D2_Support)** The D2 state is not supported.
25:25	RO	0x0 (rst)	**D1S (D1_Support)** The D1 state is not supported.
24:22	RW/L	0x1 (rst)	**AC (Aux_Current)** Reports 55 mA maximum Suspend well current required when in the D3cold state. P rogrammable by BIOS for the option to declare SUS well wake is supported or not: 001b (SUS well wake supported) or 000b (SUS well wake not supported). Locke d when FNCFG.BCLD = 1.
21:21	RO	0x0 (rst)	**DSI (Device Specific Initialization)** Indicates that no device-specific initialization is required.
20:20	RO	0x0 (rst)	**RSVD (Reserved)** Reserved.



Range	Access Type	Default (reset)	Description
19:19	RO	0x0 (rst)	**PMEC (PME Clock)** Does not apply. Hardwired to 0.
18:16	RW/L	0x3 (rst)	**VS (Version)** Indicates support for Revision 1.2 of the PCI Power Management Specification. Programmable by BIOS to older revision if compatibility issue is found. Locked when FNCFG.BCLD = 1.
15:8	RW/L	0x60 (rst)	**NEXT (Next Capability)** Points to the next capability structure (MSI). Locked when FNCFG.BCLD = 1.
7:0	RO	0x1 (rst)	**CAP (Cap ID)** Indicates that this pointer is a PCI power management capability.

12.2 Registers Summary

Table 12-2. Summary of HDAHC_MMREG Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Global Capabilities (GCAP)—Offset 0h	6701h
2h	2h	Minor Version (VMIN)—Offset 2h	0h
3h	3h	Major Version (VMAJ)—Offset 3h	1h
4h	5h	Output Payload Capability (OUTPAY)—Offset 4h	3Ch
6h	7h	Input Payload Capability (INPAY)—Offset 6h	1Dh
8h	Bh	Global Control (GCTL)—Offset 8h	0h
Ch	Dh	Wake Enable (WAKEEN)—Offset Ch	0h
Eh	Fh	Wake Status (WAKESTS)—Offset Eh	0h
10h	11h	Global Status (GSTS)—Offset 10h	0h
12h	13h	Global Capabilities 2 (GCAP2)—Offset 12h	1h
14h	15h	Linked List Capabilities Header (LLCH)—Offset 14h	C00h
18h	19h	Output Stream Payload Capability (OUTSTRMPAY)—Offset 18h	30h
1Ah	1Bh	Input Stream Payload Capability (INSTRMPAY)—Offset 1Ah	18h
20h	23h	Interrupt Control (INTCTL)—Offset 20h	0h
24h	27h	Interrupt Status (INTSTS)—Offset 24h	0h
30h	33h	Wall Clock Counter (WALCLK)—Offset 30h	0h
38h	3Bh	Stream Synchronization (SSYNC)—Offset 38h	0h
40h	43h	CORB Lower Base Address (CORBLBASE)—Offset 40h	0h
44h	47h	CORB Upper Base Address (CORBUBASE)—Offset 44h	0h
48h	49h	CORB Write Pointer (CORBWP)—Offset 48h	0h
4Ah	4Bh	CORB Read Pointer (CORBRP)—Offset 4Ah	0h
4Ch	4Ch	CORB Control (CORBCTL)—Offset 4Ch	0h
4Dh	4Dh	CORB Status (CORBSTS)—Offset 4Dh	0h
4Eh	4Eh	CORB Size (CORBSIZE)—Offset 4Eh	42h
50h	53h	RIRB Lower Base Address (RIRBLBASE)—Offset 50h	0h

Table 12-2. Summary of HDAHC_MMREG Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
54h	57h	RIRB Upper Base Address (RIRBUBASE)—Offset 54h	0h
58h	59h	RIRB Write Pointer (RIRBWP)—Offset 58h	0h
5Ah	5Bh	Response Interrupt Count (RINTCNT)—Offset 5Ah	0h
5Ch	5Ch	RIRB Control (RIRBCTL)—Offset 5Ch	0h
5Dh	5Dh	RIRB Status (RIRBSTS)—Offset 5Dh	0h
5Eh	5Eh	RIRB Size (RIRBSIZE)—Offset 5Eh	42h
68h	69h	Immediate Command Status (ICS)—Offset 68h	0h
70h	73h	DMA Position Lower Base Address (DPLBASE)—Offset 70h	0h
74h	77h	DMA Position Upper Base Address (DPUBASE)—Offset 74h	0h
80h	83h	Input/Output Stream Descriptor x Control (ISD0CTL)—Offset 80h	40000h
83h	83h	Input/Output Stream Descriptor x Status (ISD0STS)—Offset 83h	0h
84h	87h	Input/Output Stream Descriptor x Link Position in Buffer (ISD0LPIB)—Offset 84h	0h
88h	8Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD0CBL)—Offset 88h	0h
8Ch	8Dh	Input/Output Stream Descriptor x Last Valid Index (ISD0LVI)—Offset 8Ch	0h
8Eh	8Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD0FIFOW)—Offset 8Eh	4h
90h	91h	Input/Output Stream Descriptor x FIFO Size (ISD0FIFOS)—Offset 90h	0h
92h	93h	Input/Output Stream Descriptor x Format (ISD0FMT)—Offset 92h	0h
94h	95h	Input/Output Stream Descriptor x FIFO Limit (ISD0FIFOL)—Offset 94h	0h
98h	9Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD0BDLPLBA)—Offset 98h	0h
9Ch	9Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD0BDLPUBA)—Offset 9Ch	0h
A0h	A3h	Input/Output Stream Descriptor x Control (ISD1CTL)—Offset A0h	40000h
A3h	A3h	Input/Output Stream Descriptor x Status (ISD1STS)—Offset A3h	0h
A4h	A7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD1LPIB)—Offset A4h	0h
A8h	ABh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD1CBL)—Offset A8h	0h
ACh	ADh	Input/Output Stream Descriptor x Last Valid Index (ISD1LVI)—Offset ACh	0h
AEh	AFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD1FIFOW)—Offset AEh	4h
B0h	B1h	Input/Output Stream Descriptor x FIFO Size (ISD1FIFOS)—Offset B0h	0h
B2h	B3h	Input/Output Stream Descriptor x Format (ISD1FMT)—Offset B2h	0h
B4h	B5h	Input/Output Stream Descriptor x FIFO Limit (ISD1FIFOL)—Offset B4h	0h
B8h	BBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD1BDLPLBA)—Offset B8h	0h
BCh	BFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD1BDLPUBA)—Offset BCh	0h
C0h	C3h	Input/Output Stream Descriptor x Control (ISD2CTL)—Offset C0h	40000h
C3h	C3h	Input/Output Stream Descriptor x Status (ISD2STS)—Offset C3h	0h

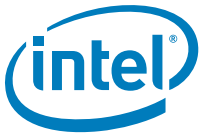


Table 12-2. Summary of HDAHC_MMREG Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C4h	C7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD2LPIB)—Offset C4h	0h
C8h	CBh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD2CBL)—Offset C8h	0h
CCh	CDh	Input/Output Stream Descriptor x Last Valid Index (ISD2LVI)—Offset CCh	0h
CEh	CFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD2FIFOW)—Offset CEh	4h
D0h	D1h	Input/Output Stream Descriptor x FIFO Size (ISD2FIFOS)—Offset D0h	0h
D2h	D3h	Input/Output Stream Descriptor x Format (ISD2FMT)—Offset D2h	0h
D4h	D5h	Input/Output Stream Descriptor x FIFO Limit (ISD2FIFOL)—Offset D4h	0h
D8h	DBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD2BDLPLBA)—Offset D8h	0h
DCh	DFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD2BDLPUBA)—Offset DCh	0h
E0h	E3h	Input/Output Stream Descriptor x Control (ISD3CTL)—Offset E0h	40000h
E3h	E3h	Input/Output Stream Descriptor x Status (ISD3STS)—Offset E3h	0h
E4h	E7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD3LPIB)—Offset E4h	0h
E8h	EBh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD3CBL)—Offset E8h	0h
ECh	EDh	Input/Output Stream Descriptor x Last Valid Index (ISD3LVI)—Offset ECh	0h
EEh	EFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD3FIFOW)—Offset EEh	4h
F0h	F1h	Input/Output Stream Descriptor x FIFO Size (ISD3FIFOS)—Offset F0h	0h
F2h	F3h	Input/Output Stream Descriptor x Format (ISD3FMT)—Offset F2h	0h
F4h	F5h	Input/Output Stream Descriptor x FIFO Limit (ISD3FIFOL)—Offset F4h	0h
F8h	FBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD3BDLPLBA)—Offset F8h	0h
FCh	FFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD3BDLPUBA)—Offset FCh	0h
100h	103h	Input/Output Stream Descriptor x Control (ISD4CTL)—Offset 100h	40000h
103h	103h	Input/Output Stream Descriptor x Status (ISD4STS)—Offset 103h	0h
104h	107h	Input/Output Stream Descriptor x Link Position in Buffer (ISD4LPIB)—Offset 104h	0h
108h	10Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD4CBL)—Offset 108h	0h
10Ch	10Dh	Input/Output Stream Descriptor x Last Valid Index (ISD4LVI)—Offset 10Ch	0h
10Eh	10Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD4FIFOW)—Offset 10Eh	4h
110h	111h	Input/Output Stream Descriptor x FIFO Size (ISD4FIFOS)—Offset 110h	0h
112h	113h	Input/Output Stream Descriptor x Format (ISD4FMT)—Offset 112h	0h
114h	115h	Input/Output Stream Descriptor x FIFO Limit (ISD4FIFOL)—Offset 114h	0h
118h	11Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD4BDLPLBA)—Offset 118h	0h

Table 12-2. Summary of HDAHC_MMREG Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
11Ch	11Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD4BDLPUBA)—Offset 11Ch	0h
120h	123h	Input/Output Stream Descriptor x Control (ISD5CTL)—Offset 120h	40000h
123h	123h	Input/Output Stream Descriptor x Status (ISD5STS)—Offset 123h	0h
124h	127h	Input/Output Stream Descriptor x Link Position in Buffer (ISD5LPIB)—Offset 124h	0h
128h	12Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD5CBL)—Offset 128h	0h
12Ch	12Dh	Input/Output Stream Descriptor x Last Valid Index (ISD5LVI)—Offset 12Ch	0h
12Eh	12Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD5FIFOW)—Offset 12Eh	4h
130h	131h	Input/Output Stream Descriptor x FIFO Size (ISD5FIFOS)—Offset 130h	0h
132h	133h	Input/Output Stream Descriptor x Format (ISD5FMT)—Offset 132h	0h
134h	135h	Input/Output Stream Descriptor x FIFO Limit (ISD5FIFOL)—Offset 134h	0h
138h	13Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD5BDLPLBA)—Offset 138h	0h
13Ch	13Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD5BDLPUBA)—Offset 13Ch	0h
140h	143h	Input/Output Stream Descriptor x Control (ISD6CTL)—Offset 140h	40000h
143h	143h	Input/Output Stream Descriptor x Status (ISD6STS)—Offset 143h	0h
144h	147h	Input/Output Stream Descriptor x Link Position in Buffer (ISD6LPIB)—Offset 144h	0h
148h	14Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD6CBL)—Offset 148h	0h
14Ch	14Dh	Input/Output Stream Descriptor x Last Valid Index (ISD6LVI)—Offset 14Ch	0h
14Eh	14Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD6FIFOW)—Offset 14Eh	4h
150h	151h	Input/Output Stream Descriptor x FIFO Size (ISD6FIFOS)—Offset 150h	0h
152h	153h	Input/Output Stream Descriptor x Format (ISD6FMT)—Offset 152h	0h
154h	155h	Input/Output Stream Descriptor x FIFO Limit (ISD6FIFOL)—Offset 154h	0h
158h	15Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD6BDLPLBA)—Offset 158h	0h
15Ch	15Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD6BDLPUBA)—Offset 15Ch	0h
160h	163h	Input/Output Stream Descriptor x Control (OSD0CTL)—Offset 160h	40000h
163h	163h	Input/Output Stream Descriptor x Status (OSD0STS)—Offset 163h	0h
164h	167h	Input/Output Stream Descriptor x Link Position in Buffer (OSD0LPIB)—Offset 164h	0h
168h	16Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD0CBL)—Offset 168h	0h
16Ch	16Dh	Input/Output Stream Descriptor x Last Valid Index (OSD0LVI)—Offset 16Ch	0h
16Eh	16Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD0FIFOW)—Offset 16Eh	4h
170h	171h	Input/Output Stream Descriptor x FIFO Size (OSD0FIFOS)—Offset 170h	0h

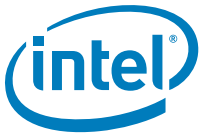


Table 12-2. Summary of HDAHC_MMREG Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
172h	173h	Input/Output Stream Descriptor x Format (OSD0FMT)—Offset 172h	0h
174h	175h	Input/Output Stream Descriptor x FIFO Limit (OSD0FIFOL)—Offset 174h	0h
178h	17Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD0BDLPLBA)—Offset 178h	0h
17Ch	17Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD0BDLPUBA)—Offset 17Ch	0h
180h	183h	Input/Output Stream Descriptor x Control (OSD1CTL)—Offset 180h	40000h
183h	183h	Input/Output Stream Descriptor x Status (OSD1STS)—Offset 183h	0h
184h	187h	Input/Output Stream Descriptor x Link Position in Buffer (OSD1LPIB)—Offset 184h	0h
188h	18Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD1CBL)—Offset 188h	0h
18Ch	18Dh	Input/Output Stream Descriptor x Last Valid Index (OSD1LVI)—Offset 18Ch	0h
18Eh	18Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD1FIFOW)—Offset 18Eh	4h
190h	191h	Input/Output Stream Descriptor x FIFO Size (OSD1FIFOS)—Offset 190h	0h
192h	193h	Input/Output Stream Descriptor x Format (OSD1FMT)—Offset 192h	0h
194h	195h	Input/Output Stream Descriptor x FIFO Limit (OSD1FIFOL)—Offset 194h	0h
198h	19Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD1BDLPLBA)—Offset 198h	0h
19Ch	19Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD1BDLPUBA)—Offset 19Ch	0h
1A0h	1A3h	Input/Output Stream Descriptor x Control (OSD2CTL)—Offset 1A0h	40000h
1A3h	1A3h	Input/Output Stream Descriptor x Status (OSD2STS)—Offset 1A3h	0h
1A4h	1A7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD2LPIB)—Offset 1A4h	0h
1A8h	1ABh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD2CBL)—Offset 1A8h	0h
1ACh	1ADh	Input/Output Stream Descriptor x Last Valid Index (OSD2LVI)—Offset 1ACh	0h
1AEh	1AFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD2FIFOW)—Offset 1AEh	4h
1B0h	1B1h	Input/Output Stream Descriptor x FIFO Size (OSD2FIFOS)—Offset 1B0h	0h
1B2h	1B3h	Input/Output Stream Descriptor x Format (OSD2FMT)—Offset 1B2h	0h
1B4h	1B5h	Input/Output Stream Descriptor x FIFO Limit (OSD2FIFOL)—Offset 1B4h	0h
1B8h	1BBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD2BDLPLBA)—Offset 1B8h	0h
1BCh	1BFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD2BDLPUBA)—Offset 1BCh	0h
1C0h	1C3h	Input/Output Stream Descriptor x Control (OSD3CTL)—Offset 1C0h	40000h
1C3h	1C3h	Input/Output Stream Descriptor x Status (OSD3STS)—Offset 1C3h	0h
1C4h	1C7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD3LPIB)—Offset 1C4h	0h
1C8h	1CBh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD3CBL)—Offset 1C8h	0h

Table 12-2. Summary of HDAHC_MMREG Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1CCh	1CDh	Input/Output Stream Descriptor x Last Valid Index (OSD3LVI)—Offset 1CCh	0h
1CEh	1CFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD3FIFOW)—Offset 1CEh	4h
1D0h	1D1h	Input/Output Stream Descriptor x FIFO Size (OSD3FIFOS)—Offset 1D0h	0h
1D2h	1D3h	Input/Output Stream Descriptor x Format (OSD3FMT)—Offset 1D2h	0h
1D4h	1D5h	Input/Output Stream Descriptor x FIFO Limit (OSD3FIFOL)—Offset 1D4h	0h
1D8h	1DBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD3BDLPLBA)—Offset 1D8h	0h
1DCh	1DFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD3BDLPUBA)—Offset 1DCh	0h
1E0h	1E3h	Input/Output Stream Descriptor x Control (OSD4CTL)—Offset 1E0h	40000h
1E3h	1E3h	Input/Output Stream Descriptor x Status (OSD4STS)—Offset 1E3h	0h
1E4h	1E7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD4LPIB)—Offset 1E4h	0h
1E8h	1EBh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD4CBL)—Offset 1E8h	0h
1ECh	1EDh	Input/Output Stream Descriptor x Last Valid Index (OSD4LVI)—Offset 1ECh	0h
1EEh	1EFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD4FIFOW)—Offset 1EEh	4h
1F0h	1F1h	Input/Output Stream Descriptor x FIFO Size (OSD4FIFOS)—Offset 1F0h	0h
1F2h	1F3h	Input/Output Stream Descriptor x Format (OSD4FMT)—Offset 1F2h	0h
1F4h	1F5h	Input/Output Stream Descriptor x FIFO Limit (OSD4FIFOL)—Offset 1F4h	0h
1F8h	1FBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD4BDLPLBA)—Offset 1F8h	0h
1FCh	1FFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD4BDLPUBA)—Offset 1FCh	0h
200h	203h	Input/Output Stream Descriptor x Control (OSD5CTL)—Offset 200h	40000h
203h	203h	Input/Output Stream Descriptor x Status (OSD5STS)—Offset 203h	0h
204h	207h	Input/Output Stream Descriptor x Link Position in Buffer (OSD5LPIB)—Offset 204h	0h
208h	20Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD5CBL)—Offset 208h	0h
20Ch	20Dh	Input/Output Stream Descriptor x Last Valid Index (OSD5LVI)—Offset 20Ch	0h
20Eh	20Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD5FIFOW)—Offset 20Eh	4h
210h	211h	Input/Output Stream Descriptor x FIFO Size (OSD5FIFOS)—Offset 210h	0h
212h	213h	Input/Output Stream Descriptor x Format (OSD5FMT)—Offset 212h	0h
214h	215h	Input/Output Stream Descriptor x FIFO Limit (OSD5FIFOL)—Offset 214h	0h
218h	21Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD5BDLPLBA)—Offset 218h	0h
21Ch	21Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD5BDLPUBA)—Offset 21Ch	0h
500h	503h	Global Time Synchronization Capability Header (GTSCH)—Offset 500h	11F00h

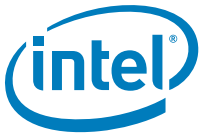


Table 12-2. Summary of HDAHC_MMREG Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
504h	507h	Global Time Synchronization Capability Declaration (GTSCD)—Offset 504h	0h
50Ch	50Fh	Global Time Synchronization Controller Adjust Control (GTSCTLAC)—Offset 50Ch	0h
520h	523h	Global Time Synchronization Capture Control (GTSCC0)—Offset 520h	0h
524h	527h	Wall Frame Counter Captured (WALFCC0)—Offset 524h	0h
528h	52Bh	Time Stamp Counter Captured Lower (TSCCL0)—Offset 528h	0h
52Ch	52Fh	Time Stamp Counter Captured Upper (TSCCU0)—Offset 52Ch	0h
534h	537h	Linear Link Position Frame Offset Captured (LLPFOC0)—Offset 534h	0h
538h	53Bh	Linear Link Position Captured Lower (LLPCL0)—Offset 538h	0h
53Ch	53Fh	Linear Link Position Captured Upper (LLPCU0)—Offset 53Ch	0h
540h	543h	Global Time Synchronization Capture Control (GTSCC1)—Offset 540h	0h
544h	547h	Wall Frame Counter Captured (WALFCC1)—Offset 544h	0h
548h	54Bh	Time Stamp Counter Captured Lower (TSCCL1)—Offset 548h	0h
54Ch	54Fh	Time Stamp Counter Captured Upper (TSCCU1)—Offset 54Ch	0h
554h	557h	Linear Link Position Frame Offset Captured (LLPFOC1)—Offset 554h	0h
558h	55Bh	Linear Link Position Captured Lower (LLPCL1)—Offset 558h	0h
55Ch	55Fh	Linear Link Position Captured Upper (LLPCU1)—Offset 55Ch	0h
700h	703h	Software Position Based FIFO Capability Header (SPBFCH)—Offset 700h	40000h
704h	707h	Software Position Based FIFO Control (SPBFCTL)—Offset 704h	0h
708h	70Bh	Input/Output Stream Descriptor x Software Position in Buffer (ISD0SPIB)—Offset 708h	0h
70Ch	70Fh	Input/Output Stream Descriptor x Max FIFO Size (ISD0MAXFIFOS)—Offset 70Ch	0h
710h	713h	Input/Output Stream Descriptor x Software Position in Buffer (ISD1SPIB)—Offset 710h	0h
714h	717h	Input/Output Stream Descriptor x Max FIFO Size (ISD1MAXFIFOS)—Offset 714h	0h
718h	71Bh	Input/Output Stream Descriptor x Software Position in Buffer (ISD2SPIB)—Offset 718h	0h
71Ch	71Fh	Input/Output Stream Descriptor x Max FIFO Size (ISD2MAXFIFOS)—Offset 71Ch	0h
720h	723h	Input/Output Stream Descriptor x Software Position in Buffer (ISD3SPIB)—Offset 720h	0h
724h	727h	Input/Output Stream Descriptor x Max FIFO Size (ISD3MAXFIFOS)—Offset 724h	0h
728h	72Bh	Input/Output Stream Descriptor x Software Position in Buffer (ISD4SPIB)—Offset 728h	0h
72Ch	72Fh	Input/Output Stream Descriptor x Max FIFO Size (ISD4MAXFIFOS)—Offset 72Ch	0h
730h	733h	Input/Output Stream Descriptor x Software Position in Buffer (ISD5SPIB)—Offset 730h	0h
734h	737h	Input/Output Stream Descriptor x Max FIFO Size (ISD5MAXFIFOS)—Offset 734h	0h
738h	73Bh	Input/Output Stream Descriptor x Software Position in Buffer (ISD6SPIB)—Offset 738h	0h

Table 12-2. Summary of HDAHC_MMREG Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
73Ch	73Fh	Input/Output Stream Descriptor x Max FIFO Size (ISD6MAXFIFOS)—Offset 73Ch	0h
740h	743h	Input/Output Stream Descriptor x Software Position in Buffer (OSD0SPIB)—Offset 740h	0h
744h	747h	Input/Output Stream Descriptor x Max FIFO Size (OSD0MAXFIFOS)—Offset 744h	0h
748h	74Bh	Input/Output Stream Descriptor x Software Position in Buffer (OSD1SPIB)—Offset 748h	0h
74Ch	74Fh	Input/Output Stream Descriptor x Max FIFO Size (OSD1MAXFIFOS)—Offset 74Ch	0h
750h	753h	Input/Output Stream Descriptor x Software Position in Buffer (OSD2SPIB)—Offset 750h	0h
754h	757h	Input/Output Stream Descriptor x Max FIFO Size (OSD2MAXFIFOS)—Offset 754h	0h
758h	75Bh	Input/Output Stream Descriptor x Software Position in Buffer (OSD3SPIB)—Offset 758h	0h
75Ch	75Fh	Input/Output Stream Descriptor x Max FIFO Size (OSD3MAXFIFOS)—Offset 75Ch	0h
760h	763h	Input/Output Stream Descriptor x Software Position in Buffer (OSD4SPIB)—Offset 760h	0h
764h	767h	Input/Output Stream Descriptor x Max FIFO Size (OSD4MAXFIFOS)—Offset 764h	0h
768h	76Bh	Input/Output Stream Descriptor x Software Position in Buffer (OSD5SPIB)—Offset 768h	0h
76Ch	76Fh	Input/Output Stream Descriptor x Max FIFO Size (OSD5MAXFIFOS)—Offset 76Ch	0h
800h	803h	Processing Pipe Capability Header (PPCH)—Offset 800h	30500h
804h	807h	Processing Pipe Control (PPCTL)—Offset 804h	0h
808h	80Bh	Processing Pipe Status (PPSTS)—Offset 808h	0h
810h	813h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC0LLPL)—Offset 810h	0h
814h	817h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC0LLPU)—Offset 814h	0h
818h	81Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC0LDPL)—Offset 818h	0h
81Ch	81Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC0LDPU)—Offset 81Ch	0h
820h	823h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC1LLPL)—Offset 820h	0h
824h	827h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC1LLPU)—Offset 824h	0h
828h	82Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC1LDPL)—Offset 828h	0h
82Ch	82Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC1LDPU)—Offset 82Ch	0h
830h	833h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC2LLPL)—Offset 830h	0h
834h	837h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC2LLPU)—Offset 834h	0h

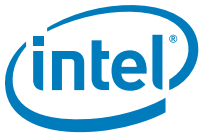


Table 12-2. Summary of HDAHC_MMREG Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
838h	83Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC2LDPL)—Offset 838h	0h
83Ch	83Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC2LDPU)—Offset 83Ch	0h
840h	843h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC3LLPL)—Offset 840h	0h
844h	847h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC3LLPU)—Offset 844h	0h
848h	84Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC3LDPL)—Offset 848h	0h
84Ch	84Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC3LDPU)—Offset 84Ch	0h
850h	853h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC4LLPL)—Offset 850h	0h
854h	857h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC4LLPU)—Offset 854h	0h
858h	85Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC4LDPL)—Offset 858h	0h
85Ch	85Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC4LDPU)—Offset 85Ch	0h
860h	863h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC5LLPL)—Offset 860h	0h
864h	867h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC5LLPU)—Offset 864h	0h
868h	86Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC5LDPL)—Offset 868h	0h
86Ch	86Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC5LDPU)—Offset 86Ch	0h
870h	873h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC6LLPL)—Offset 870h	0h
874h	877h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC6LLPU)—Offset 874h	0h
878h	87Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC6LDPL)—Offset 878h	0h
87Ch	87Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC6LDPU)—Offset 87Ch	0h
880h	883h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC0LLPL)—Offset 880h	0h
884h	887h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC0LLPU)—Offset 884h	0h
888h	88Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC0LDPL)—Offset 888h	0h
88Ch	88Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC0LDPU)—Offset 88Ch	0h
890h	893h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC1LLPL)—Offset 890h	0h
894h	897h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC1LLPU)—Offset 894h	0h
898h	89Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC1LDPL)—Offset 898h	0h

Table 12-2. Summary of HDAHC_MMREG Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
89Ch	89Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC1LDPU)—Offset 89Ch	0h
8A0h	8A3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC2LLPL)—Offset 8A0h	0h
8A4h	8A7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC2LLPU)—Offset 8A4h	0h
8A8h	8ABh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC2LDPL)—Offset 8A8h	0h
8ACh	8AFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC2LDPU)—Offset 8ACh	0h
8B0h	8B3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC3LLPL)—Offset 8B0h	0h
8B4h	8B7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC3LLPU)—Offset 8B4h	0h
8B8h	8BBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC3LDPL)—Offset 8B8h	0h
8BCh	8BFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC3LDPU)—Offset 8BCh	0h
8C0h	8C3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC4LLPL)—Offset 8C0h	0h
8C4h	8C7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC4LLPU)—Offset 8C4h	0h
8C8h	8CBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC4LDPL)—Offset 8C8h	0h
8CCh	8CFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC4LDPU)—Offset 8CCh	0h
8D0h	8D3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC5LLPL)—Offset 8D0h	0h
8D4h	8D7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC5LLPU)—Offset 8D4h	0h
8D8h	8DBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC5LDPL)—Offset 8D8h	0h
8DCh	8DFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC5LDPU)—Offset 8DCh	0h
8E0h	8E3h	Input/Output Processing Pipe's Link Connection x Control (IPPLC0CTL)—Offset 8E0h	0h
8E4h	8E5h	Input/Output Processing Pipe's Link Connection x Format (IPPLC0FMT)—Offset 8E4h	0h
8E8h	8EBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC0LLPL)—Offset 8E8h	0h
8ECh	8EFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC0LLPU)—Offset 8ECh	0h
8F0h	8F3h	Input/Output Processing Pipe's Link Connection x Control (IPPLC1CTL)—Offset 8F0h	0h
8F4h	8F5h	Input/Output Processing Pipe's Link Connection x Format (IPPLC1FMT)—Offset 8F4h	0h
8F8h	8FBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC1LLPL)—Offset 8F8h	0h
8FCh	8FFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC1LLPU)—Offset 8FCh	0h

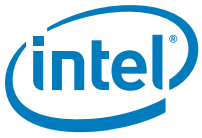


Table 12-2. Summary of HDAHC_MMREG Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
900h	903h	Input/Output Processing Pipe's Link Connection x Control (IPPLC2CTL)—Offset 900h	0h
904h	905h	Input/Output Processing Pipe's Link Connection x Format (IPPLC2FMT)—Offset 904h	0h
908h	90Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC2LLPL)—Offset 908h	0h
90Ch	90Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC2LLPU)—Offset 90Ch	0h
910h	913h	Input/Output Processing Pipe's Link Connection x Control (IPPLC3CTL)—Offset 910h	0h
914h	915h	Input/Output Processing Pipe's Link Connection x Format (IPPLC3FMT)—Offset 914h	0h
918h	91Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC3LLPL)—Offset 918h	0h
91Ch	91Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC3LLPU)—Offset 91Ch	0h
920h	923h	Input/Output Processing Pipe's Link Connection x Control (IPPLC4CTL)—Offset 920h	0h
924h	925h	Input/Output Processing Pipe's Link Connection x Format (IPPLC4FMT)—Offset 924h	0h
928h	92Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC4LLPL)—Offset 928h	0h
92Ch	92Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC4LLPU)—Offset 92Ch	0h
930h	933h	Input/Output Processing Pipe's Link Connection x Control (IPPLC5CTL)—Offset 930h	0h
934h	935h	Input/Output Processing Pipe's Link Connection x Format (IPPLC5FMT)—Offset 934h	0h
938h	93Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC5LLPL)—Offset 938h	0h
93Ch	93Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC5LLPU)—Offset 93Ch	0h
940h	943h	Input/Output Processing Pipe's Link Connection x Control (IPPLC6CTL)—Offset 940h	0h
944h	945h	Input/Output Processing Pipe's Link Connection x Format (IPPLC6FMT)—Offset 944h	0h
948h	94Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC6LLPL)—Offset 948h	0h
94Ch	94Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC6LLPU)—Offset 94Ch	0h
950h	953h	Input/Output Processing Pipe's Link Connection x Control (OPPLC0CTL)—Offset 950h	0h
954h	955h	Input/Output Processing Pipe's Link Connection x Format (OPPLC0FMT)—Offset 954h	0h
958h	95Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC0LLPL)—Offset 958h	0h
95Ch	95Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC0LLPU)—Offset 95Ch	0h
960h	963h	Input/Output Processing Pipe's Link Connection x Control (OPPLC1CTL)—Offset 960h	0h

Table 12-2. Summary of HDAHC_MMREG Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
964h	965h	Input/Output Processing Pipe's Link Connection x Format (OPPLC1FMT)—Offset 964h	0h
968h	96Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC1LLPL)—Offset 968h	0h
96Ch	96Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC1LLPU)—Offset 96Ch	0h
970h	973h	Input/Output Processing Pipe's Link Connection x Control (OPPLC2CTL)—Offset 970h	0h
974h	975h	Input/Output Processing Pipe's Link Connection x Format (OPPLC2FMT)—Offset 974h	0h
978h	97Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC2LLPL)—Offset 978h	0h
97Ch	97Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC2LLPU)—Offset 97Ch	0h
980h	983h	Input/Output Processing Pipe's Link Connection x Control (OPPLC3CTL)—Offset 980h	0h
984h	985h	Input/Output Processing Pipe's Link Connection x Format (OPPLC3FMT)—Offset 984h	0h
988h	98Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC3LLPL)—Offset 988h	0h
98Ch	98Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC3LLPU)—Offset 98Ch	0h
990h	993h	Input/Output Processing Pipe's Link Connection x Control (OPPLC4CTL)—Offset 990h	0h
994h	995h	Input/Output Processing Pipe's Link Connection x Format (OPPLC4FMT)—Offset 994h	0h
998h	99Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC4LLPL)—Offset 998h	0h
99Ch	99Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC4LLPU)—Offset 99Ch	0h
9A0h	9A3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC5CTL)—Offset 9A0h	0h
9A4h	9A5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC5FMT)—Offset 9A4h	0h
9A8h	9ABh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC5LLPL)—Offset 9A8h	0h
9ACh	9AFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC5LLPU)—Offset 9ACh	0h
C00h	C03h	Multiple Links Capability Header (MLCH)—Offset C00h	20800h
C04h	C07h	Multiple Links Capability Declaration (MLCD)—Offset C04h	1h
C40h	C43h	Link x Capabilities (LCAP0)—Offset C40h	7h
C44h	C47h	Link x Control (LCTL0)—Offset C44h	10002h
C48h	C4Bh	Link x Output Stream ID Mapping Valid (LOSIDV0)—Offset C48h	FFFEh
C4Ch	C4Fh	Link x SDI Identifier (LSDIID0)—Offset C4Ch	3h
C50h	C50h	Link x Per Stream Output Overhead (LPSOO0)—Offset C50h	0h
C52h	C52h	Link x Per Stream Input Overhead (LPSIO0)—Offset C52h	0h
C58h	C5Bh	Link x Wall Frame Counter (LWALFC0)—Offset C58h	0h
C60h	C61h	Link x Output Payload Capability (LOUTPAY6M0)—Offset C60h	0h

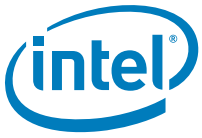


Table 12-2. Summary of HDAHC_MMREG Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C62h	C63h	Link x Output Payload Capability (LOUTPAY12M0)—Offset C62h	0h
C64h	C65h	Link x Output Payload Capability (LOUTPAY24M0)—Offset C64h	0h
C66h	C67h	Link x Output Payload Capability (LOUTPAY48M0)—Offset C66h	0h
C68h	C69h	Link x Output Payload Capability (LOUTPAY96M0)—Offset C68h	0h
C6Ah	C6Bh	Link x Output Payload Capability (LOUTPAY192M0)—Offset C6Ah	0h
C70h	C71h	Link x Input Payload Capability (LINPAY6M0)—Offset C70h	0h
C72h	C73h	Link x Input Payload Capability (LINPAY12M0)—Offset C72h	0h
C74h	C75h	Link x Input Payload Capability (LINPAY24M0)—Offset C74h	0h
C76h	C77h	Link x Input Payload Capability (LINPAY48M0)—Offset C76h	0h
C78h	C79h	Link x Input Payload Capability (LINPAY96M0)—Offset C78h	0h
C7Ah	C7Bh	Link x Input Payload Capability (LINPAY192M0)—Offset C7Ah	0h
C80h	C83h	Link x Capabilities (LCAP1)—Offset C80h	1Fh
C84h	C87h	Link x Control (LCTL1)—Offset C84h	10004h
C88h	C8Bh	Link x Output Stream ID Mapping Valid (LOSIDV1)—Offset C88h	FFFEh
C8Ch	C8Fh	Link x SDI Identifier (LSDIID1)—Offset C8Ch	4h
C90h	C90h	Link x Per Stream Output Overhead (LPSOO1)—Offset C90h	0h
C92h	C92h	Link x Per Stream Input Overhead (LPSIO1)—Offset C92h	0h
C98h	C9Bh	Link x Wall Frame Counter (LWALFC1)—Offset C98h	0h
CA0h	CA1h	Link x Output Payload Capability (LOUTPAY6M1)—Offset CA0h	0h
CA2h	CA3h	Link x Output Payload Capability (LOUTPAY12M1)—Offset CA2h	0h
CA4h	CA5h	Link x Output Payload Capability (LOUTPAY24M1)—Offset CA4h	0h
CA6h	CA7h	Link x Output Payload Capability (LOUTPAY48M1)—Offset CA6h	0h
CA8h	CA9h	Link x Output Payload Capability (LOUTPAY96M1)—Offset CA8h	0h
CAAh	CABh	Link x Output Payload Capability (LOUTPAY192M1)—Offset CAAh	0h
CB0h	CB1h	Link x Input Payload Capability (LINPAY6M1)—Offset CB0h	0h
CB2h	CB3h	Link x Input Payload Capability (LINPAY12M1)—Offset CB2h	0h
CB4h	CB5h	Link x Input Payload Capability (LINPAY24M1)—Offset CB4h	0h
CB6h	CB7h	Link x Input Payload Capability (LINPAY48M1)—Offset CB6h	0h
CB8h	CB9h	Link x Input Payload Capability (LINPAY96M1)—Offset CB8h	0h
CBAh	CBBh	Link x Input Payload Capability (LINPAY192M1)—Offset CBAh	0h
1F00h	1F03h	DMA Resume Capability Header (DRSMCH)—Offset 1F00h	50700h
1F04h	1F07h	DMA Resume Control (DRSMCTL)—Offset 1F04h	0h
1F08h	1F0Bh	DMA Position in Buffer Resume (ISD0DPIBR)—Offset 1F08h	0h
1F10h	1F13h	DMA Position in Buffer Resume (ISD1DPIBR)—Offset 1F10h	0h
1F18h	1F1Bh	DMA Position in Buffer Resume (ISD2DPIBR)—Offset 1F18h	0h
1F20h	1F23h	DMA Position in Buffer Resume (ISD3DPIBR)—Offset 1F20h	0h
1F28h	1F2Bh	DMA Position in Buffer Resume (ISD4DPIBR)—Offset 1F28h	0h
1F30h	1F33h	DMA Position in Buffer Resume (ISD5DPIBR)—Offset 1F30h	0h
1F38h	1F3Bh	DMA Position in Buffer Resume (ISD6DPIBR)—Offset 1F38h	0h
1F40h	1F43h	DMA Position in Buffer Resume (OSD0DPIBR)—Offset 1F40h	0h

Table 12-2. Summary of HDAHC_MMREG Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1F48h	1F4Bh	DMA Position in Buffer Resume (OSD1DPIBR)—Offset 1F48h	0h
1F50h	1F53h	DMA Position in Buffer Resume (OSD2DPIBR)—Offset 1F50h	0h
1F58h	1F5Bh	DMA Position in Buffer Resume (OSD3DPIBR)—Offset 1F58h	0h
1F60h	1F63h	DMA Position in Buffer Resume (OSD4DPIBR)—Offset 1F60h	0h
1F68h	1F6Bh	DMA Position in Buffer Resume (OSD5DPIBR)—Offset 1F68h	0h
2030h	2033h	Wall Clock Alias (WLCLKA)—Offset 2030h	0h
2084h	2087h	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD0LPIBA)—Offset 2084h	0h
20A4h	20A7h	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD1LPIBA)—Offset 20A4h	0h
20C4h	20C7h	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD2LPIBA)—Offset 20C4h	0h
20E4h	20E7h	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD3LPIBA)—Offset 20E4h	0h
2104h	2107h	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD4LPIBA)—Offset 2104h	0h
2124h	2127h	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD5LPIBA)—Offset 2124h	0h
2144h	2147h	Input Stream Descriptor 0 Link Position in Buffer Alias (ISD6LPIBA)—Offset 2144h	0h
2164h	2167h	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD0LPIBA)—Offset 2164h	0h
2184h	2187h	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD1LPIBA)—Offset 2184h	0h
21A4h	21A7h	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD2LPIBA)—Offset 21A4h	0h
21C4h	21C7h	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD3LPIBA)—Offset 21C4h	0h
21E4h	21E7h	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD4LPIBA)—Offset 21E4h	0h
2204h	2207h	Input Stream Descriptor 0 Link Position in Buffer Alias (OSD5LPIBA)—Offset 2204h	0h

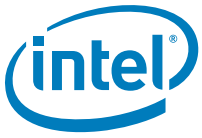
12.2.1 Global Capabilities (GCAP)—Offset 0h

This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 6701h



Bit Range	Default & Access	Field Name (ID): Description
15:12	6h RW/L	**Number of Output Streams Supported (OSS):** 0100b indicates that the Intel HD Audio controller supports four output streams. Reset value is hardcoded to parameter HSTOSC. Locked when FNCFG.BCLD = 1.
11:8	7h RW/L	**Number of Input Streams Supported (ISS):** 0100b indicates that the Intel HD Audio controller supports four input streams. Reset value is hardcoded to parameter HSTISC. Locked when FNCFG.BCLD = 1.
7:3	0h RO	**Number of Bidirectional Streams Supported (BSS):** 00000b indicates that the Intel HD Audio controller supports 0 bidirectional streams.
2:1	0h RW/L	**Number of Serial Data Out Signals (NSDO):** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. For the case in which multiple link segments are supported, this field indicates the number of SDOs for link 0. Locked when FNCFG.BCLD = 1.
0	1h RW/L	**64 Bit Address Supported (ADD64OK):** A 1 indicates that the Intel HD Audio controller supports 64 bit addressing for BDL addresses, data buffer addresses, and command buffer addresses. Locked when FNCFG.BCLD = 1.

12.2.2 Minor Version (VMIN)—Offset 2h

Register to indicate minor version of Intel HD Audio specification.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Minor Version (VMIN):** Indicates the Intel HD Audio controller supports minor revision number 00h of the Intel HD Audio specification.

12.2.3 Major Version (VMAJ)—Offset 3h

Register to indicate major version of Intel HD Audio specification

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
7:0	1h RO	**Major Version (VMAJ):** Indicates the Intel HD Audio controller supports major revision number 1 of the Intel HD Audio specification.

12.2.4 Output Payload Capability (OUTPAY)—Offset 4h

This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 3Ch

Bit Range	Default & Access	Field Name (ID): Description
15:0	3Ch RW/L	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 words in total. 40 bits are used for command and control, leaving 60 words available for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Note: In the event that multiple links are supported (GCAP2.LCOUNT) 0), the payload advertised will be the lowest common denominator offered by the default clock frequency on each link. Locked when FNCFG.BCLD = 1.

12.2.5 Input Payload Capability (INPAY)—Offset 6h

This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 1Dh

Bit Range	Default & Access	Field Name (ID): Description
15:0	1Dh RW/L	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link. This does not include bandwidth used for response. This measurement is in 16-bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz provides 500 bits per frame, or 31.25 words in total. 36 bits are used for response, leaving 29 words for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDI lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Note: In the event that multiple links are supported (GCAP2.LCOUNT) 0), the payload advertised will be the lowest common denominator offered by the default clock frequency on each link. Locked when FNCFG.BCLD = 1.

12.2.6 Global Control (GCTL)—Offset 8h

CRSTB bit is not affected by controller reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved (RSVD1):** Reserved.
8	0h RW	**Accept Unsolicited Response Enable (UNSOL):** If UNSOL is a 1, Unsolicited Responses from the codecs are accepted by the controller and placed into the Response Input Ring Buffer. If UNSOL is a 0, unsolicited responses are not accepted, and dropped on the floor.
7:2	0h RO	**Reserved (RSVD2):** Reserved.
1	0h RW/1S/V	**Flush Control (FCNTRL):** Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller, hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer bit 0 need not be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be 0). When the flush is initiated, the controller will flush pipelines to memory to guarantee that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFOs is not critical.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Controller Reset# (CRSTB):** Writing a 0 to this bit causes the Intel HD Audio controller to be reset. All state machines, FIFO's and non-suspend well memory mapped configuration registers (except ECAP, and not PCI Configuration Registers) in the controller will be reset. The Intel HD Audio link RESET# signal will be asserted and all other link signals will be driven to their "reset" values. After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify that the controller is in reset. Writing a 1 to this bit causes the controller to exit its reset state and deassert the Intel HD Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum Intel HD Audio link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. The CRST# bit defaults to a 0 after hardware reset, therefore software needs to write a 1 to this bit to begin operation. Note that the CORB/RIRB RUN bits and all Stream RUN bits must be verified cleared to zero before CRST# is written to 0 (asserted) in order to assure a clean re-start. When setting or clearing CRST#, software must ensure that minimum link timing requirements (minimum RESET# assertion time, etc.) are met. When CRST# is 0 indicating that the controller is in reset, writes to all Intel HD Audio memory mapped registers are ignored as if the device is not present. The only exception is the Global Control register containing the CRST# bit itself. The Global Control register is write-able as a DWord, Word, or Byte even when CRST# is 0 if the byte enable for the byte containing the CRST# bit (Byte Enable 0) is active. If Byte Enable 0 is not active, writes to the Global Control register will be ignored when CRST# is 0. When CRST# is 0, reads to Intel HD Audio memory mapped registers will return their default value except for registers that are not reset with PLTRST# or on a D3hot to D0 transition.

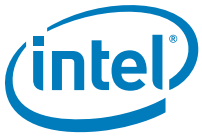
12.2.7 Wake Enable (WAKEEN)—Offset Ch

This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by resume reset.
The number of WAKEEN bits in this register is depending on the total number of codec address implemented, represented as x in the register table.
The x value is determined by the parameter CADC.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved (RSVD1):** Reserved.
1:0	0h RW	**SDIN Wake Enable Flags (WAKEEN):** Bits which control which SDI signal(s) may generate a wake event. A 1 bit in the bit mask indicates that the associated SDIN signal is enabled to generate a wake. These bits are cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

12.2.8 Wake Status (WAKESTS)—Offset Eh

This register resides in Primary well (always on), and reset by resume reset.
The number of WAKESTS bits in this register is depending on the total number of codec address implemented, represented as x in the register table. The x value is determined by the parameter CADC.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved (RSVD1):** Reserved.
1:0	0h RW/1C/V	**SDIN State Change Status Flags (WAKESTS):** Flag bits that indicate which SDI signal(s) received a State Change event. The bits are cleared by writing 1's to them. These bits are cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

12.2.9 Global Status (GSTS)—Offset 10h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved (RSVD1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW/1C/V	**Flush Status (FSTS):** This bit is set to a 1 by the hardware to indicate that the flush cycle initiated when the FCNTRL bit was set has completed. Software must write a 1to clear this bit before the next time FCNTRL is set.
0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.10 Global Capabilities 2 (GCAP2)—Offset 12h

This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/L	**Dynamic FIFO Limit Change Dapability (DFIFOLCC):** Indicates whether the energy efficient audio FIFOLC operation is static or dynamic. • 0: Static. FIFOLC bit only has effect before RUN bit is set for the first time. • 1: Dynamic. FIFOLC bit has effect before RUN bit is set for the first time, as well as after that. Locked when FNCFG.BCLD = 1.
0	1h RW/V/L	**Energy Efficient Audio Capability (EEAC):** Indicates whether the energy efficient audio with deeper buffering is supported or not. • 0: Not supported. FIFOL register and FIFOLC bit behave as RO. • 1: Supported. FIFOL register and FIFOLC bit behave as RW. Locked when FNCFG.BCLD = 1 or FUSVAL.CPPMD = 1.

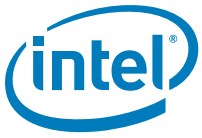
12.2.11 Linked List Capabilities Header (LLCH)—Offset 14h

This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: C00h



Bit Range	Default & Access	Field Name (ID): Description
15:0	C00h RW/L	**First Capability Pointer (PTR):** This field contains the offset to the first capability structure of the linked list capabilities, or 0000h if no linked list capabilities exist. Point to Multiple Links Capability. Locked when FNCFG.BCLD = 1.

12.2.12 Output Stream Payload Capability (OUTSTRMPAY)—Offset 18h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 30h

Bit Range	Default & Access	Field Name (ID): Description
15:0	30h RO	**Output Stream Payload Capability (OUTSTRMPAY):** Indicates maximum number of words per frame for any single output stream. This measurement is in 16 bit word quantities per 48 kHz frame. 48 Words (96B) is the maximum supported, therefore a value of 30h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Output Stream Descriptor register. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload

12.2.13 Input Stream Payload Capability (INSTRMPAY)—Offset 1Ah

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 18h

Bit Range	Default & Access	Field Name (ID): Description
15:0	18h RO	**Input Stream Payload Capability (INSTRMPAY):** Indicates maximum number of words per frame for any single input stream. This measurement is in 16-bit word quantities per 48 kHz frame. 24 Words (48B) is the maximum supported, therefore a value of 18h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Input Stream Descriptor register. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload

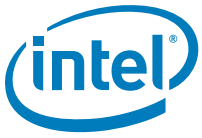
12.2.14 Interrupt Control (INTCTL)—Offset 20h

The Interrupt Status and Control register provides a central point for controlling and monitoring interrupt generation. The SIE (Stream Interrupt Enable) register controls the interrupt mask for each individual Input or Output Stream. Setting a 1 in the appropriate bit allows the particular interrupt source to generate a processor interrupt. The SIS (Stream Interrupt Status) register indicates the current interrupt status of each interrupt source. A 1 indicates that an interrupt is being requested. Note that the state of these bits is independent of the SIE bits; even if the corresponding bit is set to a 0 in the Stream Interrupt Enable register to disable processor interrupt generation, the Status bit may still be set to indicate that stream is requesting service. This can be used by polling software to determine which Streams need attention without incurring system interrupts.
The CIE (Controller Interrupt Enable) and CIS (Controller Interrupt Status) control and indicate the status of the general controller interrupt. General controller interrupt sources are to a Response Interrupt, a Response Buffer Overrun, and State Change events. Note that the CIS is independent of the CIE bit; even if the CIE bit is set to a 0 to disable processor interrupt generation, the CIS bit may still be set to indicate that stream is requesting service.
The GIE (Global Interrupt Enable) and GIS (Global Interrupt Status) control and indicate the status of all hardware interrupt sources in the Intel HD Audio controller. If GIS bit is a 1, a processor interrupt is currently being requested. If GIE is a 1, a processor interrupt may be requested; if GIE is a 0, then no processor interrupt may be requested. Note that the GIS is independent of the GIE bit; even if the GIE bit is set to a 0 to disable processor interrupt generation, the GIS bit may still be set to indicate that stream is requesting service.
GIE and CIE bits are not affected by controller reset.
The number of SIE bits in this register is depending on the total number of stream DMA implemented, represented as x in the register table. The x value is determined by the sum of parameter HSTISC and HSTOSC.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Global Interrupt Enable (GIE):** Global bit to enable device interrupt generation. When set to 1 the Intel HD Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI Configuration Space.
30	0h RW	**Controller Interrupt Enable (CIE):** Enables the general interrupt for controller functions. When set to 1 (and GIE is enabled), the controller generates an interrupt when the CIS bit gets set.
29:13	0h RO	**Reserved (RSVD1):** Reserved.
12:0	0h RW	**Stream Interrupt Enable (SIE):** When set to 1 the individual Streams are enabled to generate an interrupt when the corresponding stream status bits get set. A stream interrupt will be caused as a result of a buffer with IOC=1 in the BDL entry being completed, or as a result of a FIFO error (underrun or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set.

12.2.15 Interrupt Status (INTSTS)—Offset 24h

GIS and CIS bits are not affected by controller reset.
The number of SIS bits in this register is depending on the total number of stream DMA implemented, represented as x in the register table. The x value is determined by the sum of parameter HSTISC and HSTOSC.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Global Interrupt Status (GIS):** This bit is an OR of all of the interrupt status bits in this register and PPSTS register.
30	0h RW/V	**Controller Interrupt Status (CIS):** Status of general controller interrupt. A 1 indicates that an interrupt condition occurred due to a Response Interrupt, a Response Buffer Overrun Interrupt, CORB Memory Error Interrupt, or a SDIN State Change event. The exact cause can be determined by interrogating other registers. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the stated interrupt status bits for this register.

Bit Range	Default & Access	Field Name (ID): Description
29:13	0h RO	**Reserved (RSVD1):** Reserved.
12:0	0h RW/V	**Stream Interrupt Status (SIS):** A 1 indicates that an interrupt condition occurred on the corresponding Stream. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of an individual stream s interrupt status bits. The streams are numbered and the SIS bits assigned sequentially, based on their order in the register set.

12.2.16 Wall Clock Counter (WALCLK)—Offset 30h

The 32-bit monotonic counter provides a 'wall clock' that can be used by system software to synchronize independent audio controllers. The counter must be implemented.

Access Method

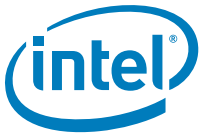
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Wall Clock Counter (WALCLK):** 32-bit counter that is incremented on each link BCLK period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition for this counter is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed, and reports the link 0 wall clock value.

12.2.17 Stream Synchronization (SSYNC)—Offset 38h

To synchronize two or more streams the corresponding SSYNC bits for the streams to be synchronized should be set to 1 before the 'RUN' bit for each stream is set.
The RUN bit for the corresponding stream must be set to 1 (and FIFORDY=1) prior to that stream's SSYNC bit being written to 0. To start multiple streams synchronously, the stream sync bits for those streams should be written to 0 at the same time. For all SSYNC bits on output engines that transition from 1 to 0 on the same write, the formatter will deliver a sample over the link in the same 48kHz frame. For all SSYNC bits on input engines that transition from 1 to 0 on the same write, the formatter will take stream data off the link and place it in the FIFO.
If synchronization is not desired, the stream synchronization bits may be left 0, and the



stream will simply begin running normally when the stream's 'RUN' bit is set.
In addition to platform reset, FLR, and controller reset, the register is also reset by stream reset.
The number of SSYNC bits in this register is depending on the total number of stream DMA implemented, represented as x in the register table. The x value is determined by the sum of parameter HSTISC and HSTOSC.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved (RSVD1):** Reserved.
12:0	0h RW	**Stream Synchronization Bits (SSYNC):** The Stream Synchronization bits, when set to 1, block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor, bit 0 corresponds to the first Stream Descriptor, etc. To synchronously start a set of DMA engines, the bits in the SSYNC register are first set to a 1. The RUN bits for the associated Stream Descriptors are then set to a 1 to start the DMA engines. When all streams are ready (FIFORDY=1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop streams, first the bits are set in the SSYNC register, and then the individual RUN bits in the Stream Descriptors are cleared by software. The streams are numbered and the SSYNC bits assigned sequentially, based on their order in the register set.

12.2.18 CORB Lower Base Address (CORBLBASE)—Offset 40h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**CORB Lower Base Address (CORBLBASE):** Lower address of the Command Output Ring Buffer, allowing the CORB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

Bit Range	Default & Access	Field Name (ID): Description
6:0	0h RO	**CORB Lower Base Unimplemented Bits (RSVD):** Hardwired to 0. This requires the CORB to be allocated with 128-byte granularity to allow for cache line fetch optimizations.

12.2.19 CORB Upper Base Address (CORBUBASE)—Offset 44h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**CORB Upper Base Address (CORBUBASE):** Upper 32 bits of address of the Command Output Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.ADD64OK = 0.

12.2.20 CORB Write Pointer (CORBWP)—Offset 48h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

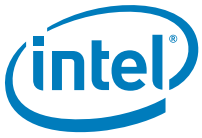
Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**CORB Write Pointer (CORBWP):** Software writes the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the Read Pointer matches the Write Pointer. Supports 256 CORB entries (256 x 4B=1KB). This field may be written while the DMA engine is running.

12.2.21 CORB Read Pointer (CORBRP)—Offset 4Ah

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/V	**CORB Read Pointer Reset (CORBRPRST):** Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual pre-fetched commands in the CORB hardware buffer within the Intel Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.
14:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RO/V	**CORB Read Pointer (CORBRP):** Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports 256 CORB entries (256 x 4B=1KB). This field may be read while the DMA engine is running.

12.2.22 CORB Control (CORBCTL)—Offset 4Ch

Length: 1 byte.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/V	**Enable CORB DMA Engine (CORBRUN):** • 0: DMA Stop • 1: DMA Run After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0h RW	**CORB Memory Error Interrupt Enable (CMEIE):** If this bit is set (and GIE and CIE are enabled), the controller will generate an interrupt if the MEI status bit is set.

12.2.23 CORB Status (CORBSTS)—Offset 4Dh

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RW/1C/V	**CORB Memory Error Indication (CMEI):** If this status bit is set, the controller has detected an error in the pathway between the controller and memory. This may be an ECC bit error or any other type of detectable data error which renders the command data fetched invalid. Software can clear this bit by writing a 1 to it. However, this type of error leaves the audio subsystem in an unviable state and typically requires CRST#.

12.2.24 CORB Size (CORBSIZE)—Offset 4Eh

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 42h

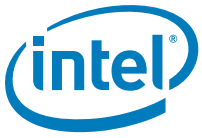
Bit Range	Default & Access	Field Name (ID): Description
7:4	4h RO	**CORB Size Capability (CORBSZCAP):** 0100b indicates that the ICH9 only supports a CORB size of 256 CORB entries (1024B).
3:2	0h RO	**Reserved (RSVD1):** Reserved.
1:0	2h RO	**CORB Size (CORBSIZE):** Hardwired to 10b which sets the CORB size to 256 entries (1024B).

12.2.25 RIRB Lower Base Address (RIRBLBASE)—Offset 50h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**RIRB Lower Base Address (RIRBLBASE):** Lower address of the Response Input Ring Buffer, allowing the RIRB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	0h RO	**RIRB Lower Base Unimplemented Bits (RSVD):** Hardwired to 0 to force 128-byte buffer alignment for cache line fetch optimizations.

12.2.26 RIRB Upper Base Address (RIRBUBASE)—Offset 54h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**RIRB Upper Base Address (RIRBUBASE):** Upper 32 bits of address of the Command Output Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

12.2.27 RIRB Write Pointer (RIRBWP)—Offset 58h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h WO	**RIRB Write Pointer Reset (RIRBWPRST):** Software writes a 1 to this bit to reset the RIRB Write Pointer to 0's. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit will always be read as 0.
14:8	0h RO	**Reserved (RSVD1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO/V	**RIRB Write Pointer (RIRBWP):** Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 Dword RIRB entry units (since each RIRB entry is 2 Dwords long). Supports up to 256 RIRB entries (256 x 8B=2KB). This field may be read while the DMA engine is running.

12.2.28 Response Interrupt Count (RINTCNT)—Offset 5Ah

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**N Response Interrupt Count (RINTCNT):** • 0000_0001b: 1 Response sent to RIRB • ... • 1111_1111b: 255 Responses sent to RIRB • 0000_0000b: 256 Responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note that each Response occupies 2 Dwords in the RIRB. This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one codec responds in one frame, then the count is increased by the number of responses received in the frame.

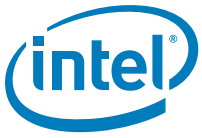
12.2.29 RIRB Control (RIRBCTL)—Offset 5Ch

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved (RSVD1):** Reserved.
2	0h RW	**Response Overrun Interrupt Control (RIRBOIC):** If this bit is set (and GIE and CIE are enabled), the hardware will generate an interrupt when the Response Overrun Interrupt Status bit is set.



Bit Range	Default & Access	Field Name (ID): Description
1	0h RW/V	**RIRB DMA Enable (RIRBRUN):** • 0: DMA Stop • 1: DMA Run After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0h RW	**Response Interrupt Control (RINTCTL):** • 0: Disable Interrupt. • 1: Generate an interrupt (if GIE and CIE are enabled) after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI_x inputs (whichever occurs first). The N counter is reset when the interrupt is generated.

12.2.30 RIRB Status (RIRBSTS)—Offset 5Dh

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved (RSVD1):** Reserved.
2	0h RW/1C/V	**Response Overrun Interrupt Status (RIRBOIS):** Hardware sets this bit to a 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs, the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.
1	0h RO	**Reserved (RSVD2):** Reserved.
0	0h RW/1C/V	**Response Interrupt (RINTFL):** Hardware sets this bit to a 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI(x) inputs (whichever occurs first). Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.

12.2.31 RIRB Size (RIRBSIZE)—Offset 5Eh

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 42h

Bit Range	Default & Access	Field Name (ID): Description
7:4	4h RO	**RIRB Size Capability (RIRBSZCAP):** 0100b indicates that the SoC only supports a RIRB size of 256 RIRB entries (2048B).
3:2	0h RO	**Reserved (RSVD1):** Reserved.
1:0	2h RO	**RIRB Size (RIRBSIZE):** Hard wired to 10b which sets the RIRB size to 256 entries (2048B).

12.2.32 Immediate Command Status (ICS)—Offset 68h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/1C/V	**Immediate Result Valid (IRV):** This bit is set to a 1 by hardware when a new response is latched into the IR register. This is a status flag indicating that software may read the response from the Immediate Response register. Software must clear this bit (by writing a one to it) before issuing a new command so that the software may determine when a new response has arrived.
0	0h RW/V	**Immediate Command Busy (ICB):** When this bit as read as a 0 it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from a 0 to a 1 (via software writing a 1), the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response register, the controller hardware sets the IRV flag and clears the ICB bit back to 0. SW may write this bit to a 0 if the bit fails to return to 0 after a reasonable timeout period. Note that an Immediate Command must not be issued while the CORB/RIRB mechanism is operating, otherwise the responses conflict. This must be enforced by software.

12.2.33 DMA Position Lower Base Address (DPLBASE)—Offset 70h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**DMA Position Lower Base Address (DPLBASE):** Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control, and must be programmed with a valid value before the FLCNRTL bit is set.
6:1	0h RO	**DMA Position Lower Base Unimplemented Bits (RSVD):** Hardwired to 0 to force 128 byte buffer alignment for cache line write optimizations.
0	0h RW	**DMA Position Buffer Enable (DPBE):** When this bit is set to a '1', the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically (typically once/frame). Software can use this value to know what data in memory is valid data. The controller must guarantee that the values in the DMA Position Buffer that the software can read represent positions in the stream for which valid data exists in the Stream's DMA buffer. This has particular relevance in systems which support isochronous transfer, the stream positions in the software-visible memory buffer must represent stream data which has reached the Global Observation point.

12.2.34 DMA Position Upper Base Address (DPUBASE)—Offset 74h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**DMA Position Upper Base Address (DPUBASE):** Upper 32 bits of address of the DMA Position Buffer Base Address. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.ADD64OK = 0.

12.2.35 Input/Output Stream Descriptor x Control (ISD0CTL)—Offset 80h

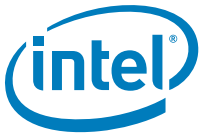
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000=Reserved (Indicates Unused) • 0001=Stream 1 • ... • 1110=Stream 14 • 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.



Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.36 Input/Output Stream Descriptor x Status (ISD0STS)—Offset 83h

Register for Input/Output Stream Descriptor x Status.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved (RSVD1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved (RSVD2):** Reserved.

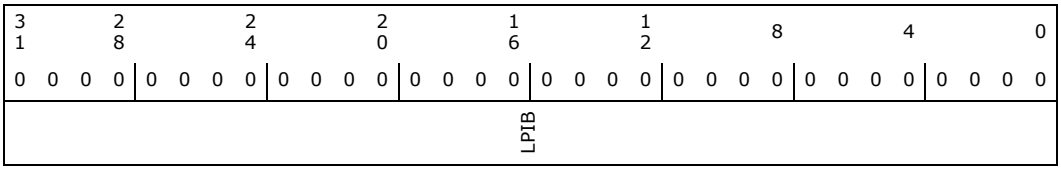
12.2.37 Input/Output Stream Descriptor x Link Position in Buffer (ISD0LPIB)—Offset 84h

Register for Input/Output Stream Descriptor x Link Position in Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.38 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD0CBL)—Offset 88h

Register for Input/Output Stream Descriptor x Cyclic Buffer Length.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

12.2.39 Input/Output Stream Descriptor x Last Valid Index (ISD0LVI)—Offset 8Ch

Register for Input/Output Stream Descriptor x Last Valid Index.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

12.2.40 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD0FIFOW)—Offset 8Eh

Register for Input/Output Stream Descriptor x FIFO Eviction Watermark.

Access Method

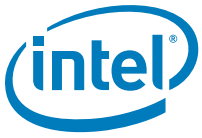
Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved (RSVD1):** Reserved.
2:0	4h RO/V	**FIFO Watermark (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The SoC HD Audio controller hard wired the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description • 000-011 Reserved • 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. • 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. • 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

12.2.41 Input/Output Stream Descriptor x FIFO Size (ISD0FIFOS)—Offset 90h

Register for Input/Output Stream Descriptor x FIFO Size.



Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

12.2.42 Input/Output Stream Descriptor x Format (ISD0FMT)—Offset 92h

Register for Input/Output Stream Descriptor x Format.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000: Divide by 1 (48 kHz, 44.1 kHz) • 001: Divide by 2 (24 kHz, 22.05 kHz) • 010: Divide by 3 (16 kHz, 32 kHz) • 011: Divide by 4 (11.025 kHz) • 100: Divide by 5 (9.6 kHz) • 101: Divide by 6 (8 kHz) • 110: Divide by 7 • 111: Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

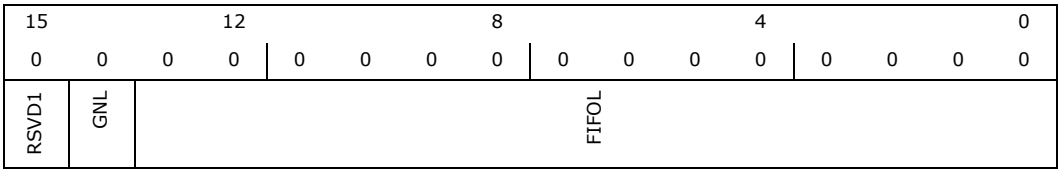
12.2.43 Input/Output Stream Descriptor x FIFO Limit (ISD0FIFOL)—Offset 94h

Register for Input/Output Stream Descriptor x FIFO Limit.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. • 0: 125 us • 1: 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. • 0 = Disabled (FIFOS is the limit) • 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

12.2.44 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD0BDLPLBA)—Offset 98h

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RO	Reserved.

12.2.45 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD0BDLPUBA)—Offset 9Ch

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

12.2.46 Input/Output Stream Descriptor x Control (ISD1CTL)—Offset A0h

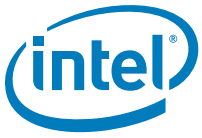
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.



Bit Range	Default & Access	Field Name (ID): Description
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000=Reserved (Indicates Unused) • 0001=Stream 1 • ... • 1110=Stream 14 • 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.47 Input/Output Stream Descriptor x Status (ISD1STS)—Offset A3h

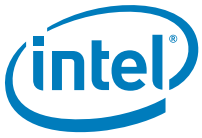
Register for Input/Output Stream Descriptor x Status.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved (RSVD1):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.48 Input/Output Stream Descriptor x Link Position in Buffer (ISD1LPIB)—Offset A4h

Register for Input/Output Stream Descriptor x Link Position in Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.49 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD1CBL)—Offset A8h

Register for Input/Output Stream Descriptor x Cyclic Buffer Length.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

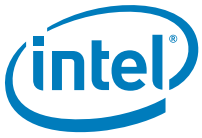
12.2.50 Input/Output Stream Descriptor x Last Valid Index (ISD1LVI)—Offset ACh

Register for Input/Output Stream Descriptor x Last Valid Index.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

12.2.51 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD1FIFOW)—Offset AEh

Register for Input/Output Stream Descriptor x FIFO Eviction Watermark.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved (RSVD1):** Reserved.
2:0	4h RO/V	**FIFO Watermark (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The SoC HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description • 000-011 Reserved • 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. • 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. • 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

12.2.52 Input/Output Stream Descriptor x FIFO Size (ISD1FIFOS)—Offset B0h

Register for Input/Output Stream Descriptor x FIFO Size.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

12.2.53 Input/Output Stream Descriptor x Format (ISD1FMT)—Offset B2h

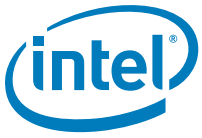
Register for Input/Output Stream Descriptor x Format.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz



Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000: Divide by 1 (48 kHz, 44.1 kHz) • 001: Divide by 2 (24 kHz, 22.05 kHz) • 010: Divide by 3 (16 kHz, 32 kHz) • 011: Divide by 4 (11.025 kHz) • 100: Divide by 5 (9.6 kHz) • 101: Divide by 6 (8 kHz) • 110: Divide by 7 • 111: Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.54 Input/Output Stream Descriptor x FIFO Limit (ISD1FIFOL)—Offset B4h

Register for Input/Output Stream Descriptor x FIFO Limit.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. • 0: 125 us • 1: 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. • 0 = Disabled (FIFOS is the limit) • 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

12.2.55 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD1BDLPLBA)—Offset B8h

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RO	Reserved.

12.2.56 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD1BDLPUBA)—Offset BCh

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

12.2.57 Input/Output Stream Descriptor x Control (ISD2CTL)—Offset C0h

SRST bit is not affected by stream reset.

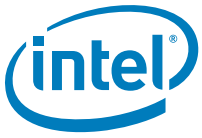
Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000=Reserved (Indicates Unused) • 0001=Stream 1 • ... • 1110=Stream 14 • 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.



Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.58 Input/Output Stream Descriptor x Status (ISD2STS)—Offset C3h

Register for Input/Output Stream Descriptor x Status.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.59 Input/Output Stream Descriptor x Link Position in Buffer (ISD2LPIB)—Offset C4h

Register for Input/Output Stream Descriptor x Link Position in Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.60 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD2CBL)—Offset C8h

Register for Input/Output Stream Descriptor x Cyclic Buffer Length.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

12.2.61 Input/Output Stream Descriptor x Last Valid Index (ISD2LVI)—Offset CCh

Register for Input/Output Stream Descriptor x Last Valid Index.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

12.2.62 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD2FIFOW)—Offset CEh

Register for Input/Output Stream Descriptor x FIFO Eviction Watermark.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved (RSVD1):** Reserved.
2:0	4h RO/V	**FIFO Watermark (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The SoC HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description • 000-011 Reserved • 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. • 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. • 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

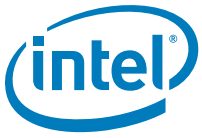
12.2.63 Input/Output Stream Descriptor x FIFO Size (ISD2FIFOS)—Offset D0h

Register for Input/Output Stream Descriptor x FIFO Size.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

12.2.64 Input/Output Stream Descriptor x Format (ISD2FMT)—Offset D2h

Register for Input/Output Stream Descriptor x Format.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz

Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000: Divide by 1 (48 kHz, 44.1 kHz) • 001: Divide by 2 (24 kHz, 22.05 kHz) • 010: Divide by 3 (16 kHz, 32 kHz) • 011: Divide by 4 (11.025 kHz) • 100: Divide by 5 (9.6 kHz) • 101: Divide by 6 (8 kHz) • 110: Divide by 7 • 111: Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.65 Input/Output Stream Descriptor x FIFO Limit (ISD2FIFOL)—Offset D4h

Register for Input/Output Stream Descriptor x FIFO Limit.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. • 0: 125 us • 1: 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. • 0 = Disabled (FIFOS is the limit) • 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

12.2.66 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD2BDLPLBA)—Offset D8h

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RO	Reserved.

12.2.67 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD2BDLPUBA)—Offset DCh

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

12.2.68 Input/Output Stream Descriptor x Control (ISD3CTL)—Offset E0h

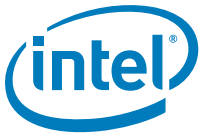
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000=Reserved (Indicates Unused) • 0001=Stream 1 • ... • 1110=Stream 14 • 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.



Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.69 Input/Output Stream Descriptor x Status (ISD3STS)—Offset E3h

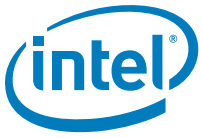
Register for Input/Output Stream Descriptor x Status.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.



Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.70 Input/Output Stream Descriptor x Link Position in Buffer (ISD3LPIB)—Offset E4h

Register for Input/Output Stream Descriptor x Link Position in Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.71 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD3CBL)—Offset E8h

Register for Input/Output Stream Descriptor x Cyclic Buffer Length.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

12.2.72 Input/Output Stream Descriptor x Last Valid Index (ISD3LVI)—Offset ECh

Register for Input/Output Stream Descriptor x Last Valid Index.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

12.2.73 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD3FIFOW)—Offset EEh

Register for Input/Output Stream Descriptor x FIFO Eviction Watermark.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved (RSVD1):** Reserved.
2:0	4h RO/V	**FIFO Watermark (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The SoC HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description • 000-011 Reserved • 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. • 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. • 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

12.2.74 Input/Output Stream Descriptor x FIFO Size (ISD3FIFOS)—Offset F0h

Register for Input/Output Stream Descriptor x FIFO Size.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

12.2.75 Input/Output Stream Descriptor x Format (ISD3FMT)—Offset F2h

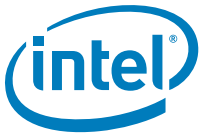
Register for Input/Output Stream Descriptor x Format.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz



Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000: Divide by 1 (48 kHz, 44.1 kHz) • 001: Divide by 2 (24 kHz, 22.05 kHz) • 010: Divide by 3 (16 kHz, 32 kHz) • 011: Divide by 4 (11.025 kHz) • 100: Divide by 5 (9.6 kHz) • 101: Divide by 6 (8 kHz) • 110: Divide by 7 • 111: Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.76 Input/Output Stream Descriptor x FIFO Limit (ISD3FIFOL)—Offset F4h

Register for Input/Output Stream Descriptor x FIFO Limit.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. • 0: 125 us • 1: 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. • 0 = Disabled (FIFOS is the limit) • 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

12.2.77 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD3BDLPLBA)—Offset F8h

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RO	Reserved.

12.2.78 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD3BDLPUBA)—Offset FCh

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

12.2.79 Input/Output Stream Descriptor x Control (ISD4CTL)—Offset 100h

SRST bit is not affected by stream reset.

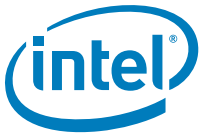
Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000=Reserved (Indicates Unused) • 0001=Stream 1 • ... • 1110=Stream 14 • 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.



Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.80 Input/Output Stream Descriptor x Status (ISD4STS)—Offset 103h

Register for Input/Output Stream Descriptor x Status.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.81 Input/Output Stream Descriptor x Link Position in Buffer (ISD4LPIB)—Offset 104h

Register for Input/Output Stream Descriptor x Link Position in Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.82 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD4CBL)—Offset 108h

Register for Input/Output Stream Descriptor x Cyclic Buffer Length.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

12.2.83 Input/Output Stream Descriptor x Last Valid Index (ISD4LVI)—Offset 10Ch

Register for Input/Output Stream Descriptor x Last Valid Index.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

12.2.84 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD4FIFOW)—Offset 10Eh

Register for Input/Output Stream Descriptor x FIFO Eviction Watermark.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved (RSVD1):** Reserved.
2:0	4h RO/V	**FIFO Watermark (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The SoC HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description • 000-011 Reserved • 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. • 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. • 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

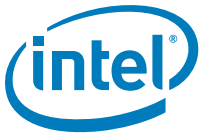
12.2.85 Input/Output Stream Descriptor x FIFO Size (ISD4FIFOS)—Offset 110h

Register for Input/Output Stream Descriptor x FIFO Size.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

12.2.86 Input/Output Stream Descriptor x Format (ISD4FMT)—Offset 112h

Register for Input/Output Stream Descriptor x Format.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz

Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000: Divide by 1 (48 kHz, 44.1 kHz) • 001: Divide by 2 (24 kHz, 22.05 kHz) • 010: Divide by 3 (16 kHz, 32 kHz) • 011: Divide by 4 (11.025 kHz) • 100: Divide by 5 (9.6 kHz) • 101: Divide by 6 (8 kHz) • 110: Divide by 7 • 111: Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.87 Input/Output Stream Descriptor x FIFO Limit (ISD4FIFOL)—Offset 114h

Register for Input/Output Stream Descriptor x FIFO Limit.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. • 0: 125 us • 1: 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. • 0 = Disabled (FIFOS is the limit) • 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

12.2.88 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD4BDLPLBA)—Offset 118h

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RO	Reserved.

12.2.89 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD4BDLPUBA)—Offset 11Ch

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

12.2.90 Input/Output Stream Descriptor x Control (ISD5CTL)—Offset 120h

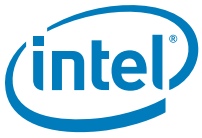
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000=Reserved (Indicates Unused) • 0001=Stream 1 • ... • 1110=Stream 14 • 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.



Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.91 Input/Output Stream Descriptor x Status (ISD5STS)—Offset 123h

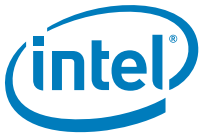
Register for Input/Output Stream Descriptor x Status.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.



Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.92 Input/Output Stream Descriptor x Link Position in Buffer (ISD5LPIB)—Offset 124h

Register for Input/Output Stream Descriptor x Link Position in Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.93 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD5CBL)—Offset 128h

Register for Input/Output Stream Descriptor x Cyclic Buffer Length.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

12.2.94 Input/Output Stream Descriptor x Last Valid Index (ISD5LVI)—Offset 12Ch

Register for Input/Output Stream Descriptor x Last Valid Index.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

12.2.95 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD5FIFOW)—Offset 12Eh

Register for Input/Output Stream Descriptor x FIFO Eviction Watermark.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved (RSVD1):** Reserved.
2:0	4h RO/V	**FIFO Watermark (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The SoC HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description • 000-011 Reserved • 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. • 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. • 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

12.2.96 Input/Output Stream Descriptor x FIFO Size (ISD5FIFOS)—Offset 130h

Register for Input/Output Stream Descriptor x FIFO Size.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

12.2.97 Input/Output Stream Descriptor x Format (ISD5FMT)—Offset 132h

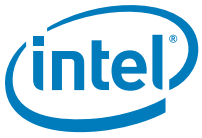
Register for Input/Output Stream Descriptor x Format.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz



Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000: Divide by 1 (48 kHz, 44.1 kHz) • 001: Divide by 2 (24 kHz, 22.05 kHz) • 010: Divide by 3 (16 kHz, 32 kHz) • 011: Divide by 4 (11.025 kHz) • 100: Divide by 5 (9.6 kHz) • 101: Divide by 6 (8 kHz) • 110: Divide by 7 • 111: Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.98 Input/Output Stream Descriptor x FIFO Limit (ISD5FIFOL)—Offset 134h

Register for Input/Output Stream Descriptor x FIFO Limit.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. • 0: 125 us • 1: 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. • 0 = Disabled (FIFOS is the limit) • 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

12.2.99 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD5BDLPLBA)—Offset 138h

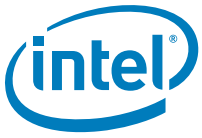
Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RO	Reserved.



12.2.100 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD5BDLPUBA)—Offset 13Ch

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

12.2.101 Input/Output Stream Descriptor x Control (ISD6CTL)—Offset 140h

SRST bit is not affected by stream reset.

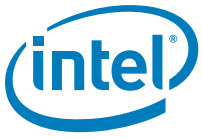
Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000=Reserved (Indicates Unused) • 0001=Stream 1 • ... • 1110=Stream 14 • 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.



Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.102 Input/Output Stream Descriptor x Status (ISD6STS)—Offset 143h

Register for Input/Output Stream Descriptor x Status.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.103 Input/Output Stream Descriptor x Link Position in Buffer (ISD6LPIB)—Offset 144h

Register for Input/Output Stream Descriptor x Link Position in Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.104 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD6CBL)—Offset 148h

Register for Input/Output Stream Descriptor x Cyclic Buffer Length.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

12.2.105 Input/Output Stream Descriptor x Last Valid Index (ISD6LVI)—Offset 14Ch

Register for Input/Output Stream Descriptor x Last Valid Index.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

12.2.106 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD6FIFOW)—Offset 14Eh

Register for Input/Output Stream Descriptor x FIFO Eviction Watermark.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved (RSVD1):** Reserved.
2:0	4h RO/V	**FIFO Watermark (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The SoC HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description • 000-011 Reserved • 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. • 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. • 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

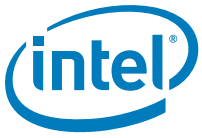
12.2.107 Input/Output Stream Descriptor x FIFO Size (ISD6FIFOS)—Offset 150h

Register for Input/Output Stream Descriptor x FIFO Size.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

12.2.108 Input/Output Stream Descriptor x Format (ISD6FMT)—Offset 152h

Register for Input/Output Stream Descriptor x Format.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz

Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000: Divide by 1 (48 kHz, 44.1 kHz) • 001: Divide by 2 (24 kHz, 22.05 kHz) • 010: Divide by 3 (16 kHz, 32 kHz) • 011: Divide by 4 (11.025 kHz) • 100: Divide by 5 (9.6 kHz) • 101: Divide by 6 (8 kHz) • 110: Divide by 7 • 111: Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.109 Input/Output Stream Descriptor x FIFO Limit (ISD6FIFOL)—Offset 154h

Register for Input/Output Stream Descriptor x FIFO Limit.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. • 0: 125 us • 1: 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. • 0 = Disabled (FIFOS is the limit) • 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

12.2.110 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD6BDLPLBA)—Offset 158h

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RO	Reserved.

12.2.111 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD6BDLPUBA)—Offset 15Ch

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

12.2.112 Input/Output Stream Descriptor x Control (OSD0CTL)—Offset 160h

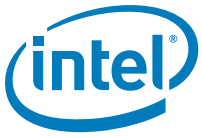
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000=Reserved (Indicates Unused) • 0001=Stream 1 • ... • 1110=Stream 14 • 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.



Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.113 Input/Output Stream Descriptor x Status (OSD0STS)—Offset 163h

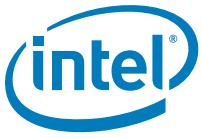
Register for Input/Output Stream Descriptor x Status.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.



Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.114 Input/Output Stream Descriptor x Link Position in Buffer (OSD0LPIB)—Offset 164h

Register for Input/Output Stream Descriptor x Link Position in Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.115 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD0CBL)—Offset 168h

Register for Input/Output Stream Descriptor x Cyclic Buffer Length.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

12.2.116 Input/Output Stream Descriptor x Last Valid Index (OSD0LVI)—Offset 16Ch

Register for Input/Output Stream Descriptor x Last Valid Index.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

12.2.117 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD0FIFOW)—Offset 16Eh

Register for Input/Output Stream Descriptor x FIFO Eviction Watermark.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved (RSVD1):** Reserved.
2:0	4h RO/V	**FIFO Watermark (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The SoC HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description • 000-011 Reserved • 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. • 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. • 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

12.2.118 Input/Output Stream Descriptor x FIFO Size (OSD0FIFOS)—Offset 170h

Register for Input/Output Stream Descriptor x FIFO Size.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

12.2.119 Input/Output Stream Descriptor x Format (OSD0FMT)—Offset 172h

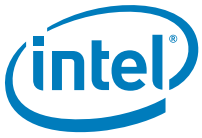
Register for Input/Output Stream Descriptor x Format.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz



Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000: Divide by 1 (48 kHz, 44.1 kHz) • 001: Divide by 2 (24 kHz, 22.05 kHz) • 010: Divide by 3 (16 kHz, 32 kHz) • 011: Divide by 4 (11.025 kHz) • 100: Divide by 5 (9.6 kHz) • 101: Divide by 6 (8 kHz) • 110: Divide by 7 • 111: Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.120 Input/Output Stream Descriptor x FIFO Limit (OSD0FIFOL)—Offset 174h

Register for Input/Output Stream Descriptor x FIFO Limit.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. • 0: 125 us • 1: 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. • 0 = Disabled (FIFOS is the limit) • 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

12.2.121 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD0BDLPLBA)—Offset 178h

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RO	Reserved.

12.2.122 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD0BDLPUBA)—Offset 17Ch

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

12.2.123 Input/Output Stream Descriptor x Control (OSD1CTL)—Offset 180h

SRST bit is not affected by stream reset.

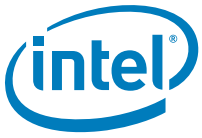
Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000=Reserved (Indicates Unused) • 0001=Stream 1 • ... • 1110=Stream 14 • 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.



Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.124 Input/Output Stream Descriptor x Status (OSD1STS)—Offset 183h

Register for Input/Output Stream Descriptor x Status.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.125 Input/Output Stream Descriptor x Link Position in Buffer (OSD1LPIB)—Offset 184h

Register for Input/Output Stream Descriptor x Link Position in Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.126 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD1CBL)—Offset 188h

Register for Input/Output Stream Descriptor x Cyclic Buffer Length.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

12.2.127 Input/Output Stream Descriptor x Last Valid Index (OSD1LVI)—Offset 18Ch

Register for Input/Output Stream Descriptor x Last Valid Index.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

12.2.128 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD1FIFOW)—Offset 18Eh

Register for Input/Output Stream Descriptor x FIFO Eviction Watermark.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved (RSVD1):** Reserved.
2:0	4h RO/V	**FIFO Watermark (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The SoC HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description • 000-011 Reserved • 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. • 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. • 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

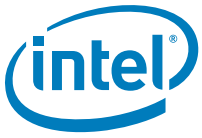
12.2.129 Input/Output Stream Descriptor x FIFO Size (OSD1FIFOS)—Offset 190h

Register for Input/Output Stream Descriptor x FIFO Size.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

12.2.130 Input/Output Stream Descriptor x Format (OSD1FMT)—Offset 192h

Register for Input/Output Stream Descriptor x Format.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz

Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000: Divide by 1 (48 kHz, 44.1 kHz) • 001: Divide by 2 (24 kHz, 22.05 kHz) • 010: Divide by 3 (16 kHz, 32 kHz) • 011: Divide by 4 (11.025 kHz) • 100: Divide by 5 (9.6 kHz) • 101: Divide by 6 (8 kHz) • 110: Divide by 7 • 111: Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.131 Input/Output Stream Descriptor x FIFO Limit (OSD1FIFOL)—Offset 194h

Register for Input/Output Stream Descriptor x FIFO Limit.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. • 0: 125 us • 1: 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. • 0 = Disabled (FIFOS is the limit) • 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

12.2.132 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD1BDLPLBA)—Offset 198h

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RO	Reserved.

12.2.133 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD1BDLPUBA)—Offset 19Ch

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

12.2.134 Input/Output Stream Descriptor x Control (OSD2CTL)—Offset 1A0h

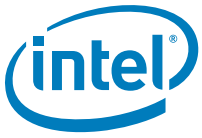
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000=Reserved (Indicates Unused) • 0001=Stream 1 • ... • 1110=Stream 14 • 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.



Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.135 Input/Output Stream Descriptor x Status (OSD2STS)—Offset 1A3h

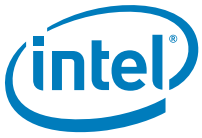
Register for Input/Output Stream Descriptor x Status.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.



Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.136 Input/Output Stream Descriptor x Link Position in Buffer (OSD2LPIB)—Offset 1A4h

Register for Input/Output Stream Descriptor x Link Position in Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.137 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD2CBL)—Offset 1A8h

Register for Input/Output Stream Descriptor x Cyclic Buffer Length.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

12.2.138 Input/Output Stream Descriptor x Last Valid Index (OSD2LVI)—Offset 1ACh

Register for Input/Output Stream Descriptor x Last Valid Index.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

12.2.139 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD2FIFOW)—Offset 1AEh

Register for Input/Output Stream Descriptor x FIFO Eviction Watermark.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved (RSVD1):** Reserved.
2:0	4h RO/V	**FIFO Watermark (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The SoC HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description • 000-011 Reserved • 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. • 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. • 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

12.2.140 Input/Output Stream Descriptor x FIFO Size (OSD2FIFOS)—Offset 1B0h

Register for Input/Output Stream Descriptor x FIFO Size.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

12.2.141 Input/Output Stream Descriptor x Format (OSD2FMT)—Offset 1B2h

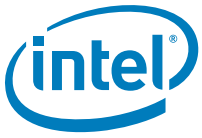
Register for Input/Output Stream Descriptor x Format.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz



Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000: Divide by 1 (48 kHz, 44.1 kHz) • 001: Divide by 2 (24 kHz, 22.05 kHz) • 010: Divide by 3 (16 kHz, 32 kHz) • 011: Divide by 4 (11.025 kHz) • 100: Divide by 5 (9.6 kHz) • 101: Divide by 6 (8 kHz) • 110: Divide by 7 • 111: Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.142 Input/Output Stream Descriptor x FIFO Limit (OSD2FIFOL)—Offset 1B4h

Register for Input/Output Stream Descriptor x FIFO Limit.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. • 0: 125 us • 1: 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. • 0 = Disabled (FIFOS is the limit) • 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

12.2.143 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD2BDLPLBA)—Offset 1B8h

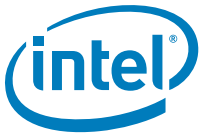
Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RO	Reserved.



12.2.144 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD2BDLPUBA)—Offset 1BCh

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

12.2.145 Input/Output Stream Descriptor x Control (OSD3CTL)—Offset 1C0h

SRST bit is not affected by stream reset.

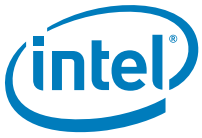
Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000=Reserved (Indicates Unused) • 0001=Stream 1 • ... • 1110=Stream 14 • 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.



Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.146 Input/Output Stream Descriptor x Status (OSD3STS)—Offset 1C3h

Register for Input/Output Stream Descriptor x Status.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.147 Input/Output Stream Descriptor x Link Position in Buffer (OSD3LPIB)—Offset 1C4h

Register for Input/Output Stream Descriptor x Link Position in Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.148 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD3CBL)—Offset 1C8h

Register for Input/Output Stream Descriptor x Cyclic Buffer Length.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

12.2.149 Input/Output Stream Descriptor x Last Valid Index (OSD3LVI)—Offset 1CCh

Register for Input/Output Stream Descriptor x Last Valid Index.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

12.2.150 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD3FIFOW)—Offset 1CEh

Register for Input/Output Stream Descriptor x FIFO Eviction Watermark.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved (RSVD1):** Reserved.
2:0	4h RO/V	**FIFO Watermark (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The SoC HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description • 000-011 Reserved • 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. • 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. • 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

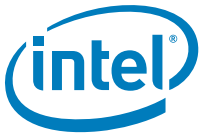
12.2.151 Input/Output Stream Descriptor x FIFO Size (OSD3FIFOS)—Offset 1D0h

Register for Input/Output Stream Descriptor x FIFO Size.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

12.2.152 Input/Output Stream Descriptor x Format (OSD3FMT)—Offset 1D2h

Register for Input/Output Stream Descriptor x Format.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz

Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000: Divide by 1 (48 kHz, 44.1 kHz) • 001: Divide by 2 (24 kHz, 22.05 kHz) • 010: Divide by 3 (16 kHz, 32 kHz) • 011: Divide by 4 (11.025 kHz) • 100: Divide by 5 (9.6 kHz) • 101: Divide by 6 (8 kHz) • 110: Divide by 7 • 111: Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.153 Input/Output Stream Descriptor x FIFO Limit (OSD3FIFOL)—Offset 1D4h

Register for Input/Output Stream Descriptor x FIFO Limit.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. • 0: 125 us • 1: 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. • 0 = Disabled (FIFOS is the limit) • 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

12.2.154 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD3BDLPLBA)—Offset 1D8h

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RO	Reserved.

12.2.155 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD3BDLPUBA)—Offset 1DCh

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

12.2.156 Input/Output Stream Descriptor x Control (OSD4CTL)—Offset 1E0h

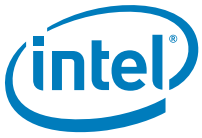
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000=Reserved (Indicates Unused) • 0001=Stream 1 • ... • 1110=Stream 14 • 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.



Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.157 Input/Output Stream Descriptor x Status (OSD4STS)—Offset 1E3h

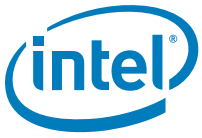
Register for Input/Output Stream Descriptor x Status.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.



Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.158 Input/Output Stream Descriptor x Link Position in Buffer (OSD4LPIB)—Offset 1E4h

Register for Input/Output Stream Descriptor x Link Position in Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.159 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD4CBL)—Offset 1E8h

Register for Input/Output Stream Descriptor x Cyclic Buffer Length.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

12.2.160 Input/Output Stream Descriptor x Last Valid Index (OSD4LVI)—Offset 1ECh

Register for Input/Output Stream Descriptor x Last Valid Index.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

12.2.161 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD4FIFOW)—Offset 1EEh

Register for Input/Output Stream Descriptor x FIFO Eviction Watermark.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved (RSVD1):** Reserved.
2:0	4h RO/V	**FIFO Watermark (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The SoC HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description • 000-011 Reserved • 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. • 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. • 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

12.2.162 Input/Output Stream Descriptor x FIFO Size (OSD4FIFOS)—Offset 1F0h

Register for Input/Output Stream Descriptor x FIFO Size.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

12.2.163 Input/Output Stream Descriptor x Format (OSD4FMT)—Offset 1F2h

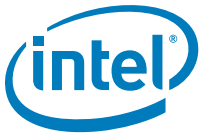
Register for Input/Output Stream Descriptor x Format.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz



Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000: Divide by 1 (48 kHz, 44.1 kHz) • 001: Divide by 2 (24 kHz, 22.05 kHz) • 010: Divide by 3 (16 kHz, 32 kHz) • 011: Divide by 4 (11.025 kHz) • 100: Divide by 5 (9.6 kHz) • 101: Divide by 6 (8 kHz) • 110: Divide by 7 • 111: Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.164 Input/Output Stream Descriptor x FIFO Limit (OSD4FIFOL)—Offset 1F4h

Register for Input/Output Stream Descriptor x FIFO Limit.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. • 0: 125 us • 1: 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. • 0 = Disabled (FIFOS is the limit) • 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

12.2.165 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD4BDLPLBA)—Offset 1F8h

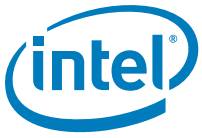
Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RO	Reserved.



12.2.166 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD4BDLPUBA)—Offset 1FCh

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

12.2.167 Input/Output Stream Descriptor x Control (OSD5CTL)—Offset 200h

SRST bit is not affected by stream reset.

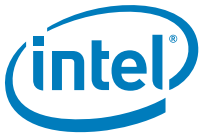
Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000=Reserved (Indicates Unused) • 0001=Stream 1 • ... • 1110=Stream 14 • 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.



Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.168 Input/Output Stream Descriptor x Status (OSD5STS)—Offset 203h

Register for Input/Output Stream Descriptor x Status.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.169 Input/Output Stream Descriptor x Link Position in Buffer (OSD5LPIB)—Offset 204h

Register for Input/Output Stream Descriptor x Link Position in Buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.170 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD5CBL)—Offset 208h

Register for Input/Output Stream Descriptor x Cyclic Buffer Length.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

12.2.171 Input/Output Stream Descriptor x Last Valid Index (OSD5LVI)—Offset 20Ch

Register for Input/Output Stream Descriptor x Last Valid Index.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD1):** Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'.

12.2.172 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD5FIFOW)—Offset 20Eh

Register for Input/Output Stream Descriptor x FIFO Eviction Watermark.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved (RSVD1):** Reserved.
2:0	4h RO/V	**FIFO Watermark (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The SoC HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description • 000-011 Reserved • 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. • 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. • 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

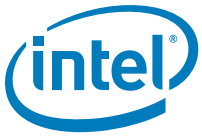
12.2.173 Input/Output Stream Descriptor x FIFO Size (OSD5FIFOS)—Offset 210h

Register for Input/Output Stream Descriptor x FIFO Size.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

12.2.174 Input/Output Stream Descriptor x Format (OSD5FMT)—Offset 212h

Register for Input/Output Stream Descriptor x Format.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz

Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000: Divide by 1 (48 kHz, 44.1 kHz) • 001: Divide by 2 (24 kHz, 22.05 kHz) • 010: Divide by 3 (16 kHz, 32 kHz) • 011: Divide by 4 (11.025 kHz) • 100: Divide by 5 (9.6 kHz) • 101: Divide by 6 (8 kHz) • 110: Divide by 7 • 111: Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.175 Input/Output Stream Descriptor x FIFO Limit (OSD5FIFOL)—Offset 214h

Register for Input/Output Stream Descriptor x FIFO Limit.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. • 0: 125 us • 1: 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. • 0 = Disabled (FIFOS is the limit) • 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

12.2.176 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD5BDLPLBA)—Offset 218h

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	**Reserved (RSVD1):** Reserved.
0	0h RO	Reserved.

12.2.177 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD5BDLPUBA)—Offset 21Ch

Register for Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

12.2.178 Global Time Synchronization Capability Header (GTSCH)—Offset 500h

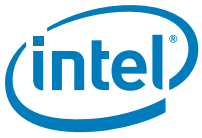
This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 11F00h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.
27:16	1h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.
15:0	1F00h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to DMA resume capability. Locked when FNCFG.BCLD = 1.



12.2.179 Global Time Synchronization Capability Declaration (GTSCD)—Offset 504h

This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved (RSVD1):** Reserved.
2	0h RW/L	**Controller Based Synchronization Adjust Supported (CTLSAS):** When set, it indicates that the controller based synchronization adjustment is supported. By adjusting the global link clock which is used as reference clock for the codecs DAC / ADC, the codec will indirectly changing the rate of all its active streams. Locked when FNCFG.BCLD = 1.
1:0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.180 Global Time Synchronization Controller Adjust Control (GTSCTLAC)—Offset 50Ch

This register controls the fractional divider feature of the Audio PLL.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD1):** Reserved.
17	0h RW/L	**Strobe (STB):** SW set to 1 enables the Audio PLL latching in the EN bit and VAL field into the PLL CKT and reflect the new fractional divider state. SW must clear this bit to 0 after at least 200 ns to complete the strobe pulse sequence. For each strobing of a new fractional divider value, SW should wait for fractional divider settling time to reflect the new ppm value before initiating the next strobing of another new fractional divider value. Locked when GTSCD.CTLSAS = 0.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/L	**Enable (EN):** When set, it allows the fractional divider of the Audio PLL to operate, per the fractional value specified in VAL field. The value needs to be latched into the Audio PLL by pulsing the STB bit. Locked when GTSCD.CTLSAS = 0.
15	0h RW/L	**Direction (DIR):** Indicates the direction of the ppm shift adjustment. • 0: Positive direction. • 1: Negative direction. Locked when GTSCD.CTLSAS = 0.
14:0	0h RW/L	**Value (VAL):** Indicates the value of the fractional divider if enabled. Locked when GTSCD.CTLSAS = 0.

12.2.181 Global Time Synchronization Capture Control (GTSCC0)—Offset 520h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Time Stamp Counter Capture Done (TSCCD):** This bit is set when a valid TSC value has been captured: WALFCC, TSCCL, TSCCU, LLPFOC, LLPCL, and LLPCH contain valid data. The Intel HD Audio driver software must acknowledge the completion by writing 1 to clear this bit.
30	0h RW	**Time Stamp Counter Capture Done Interrupt Enable (TSCCDIE):** If set to 1, TSCCD bit can pass through to cause an interrupt status reported in INTSTS.CIS bit, and cause an interrupt to CPU if INTCTL.CIE = 1 and INTCTL.GIE = 1.
29:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/1S/V	**Time Stamp Counter Capture Initiate (TSCCI):** Write to 1 to initiate Global Time Synchronization capture for measuring TSC offset to local wall frame info. Cleared to 0 by hardware when the process is completed.
4:0	0h RW	**Capture DMA Select (CDMAS):** To select which DMA's LLPL, and LLPU value to be captured together with the TSC value. Bit 4 = 1 for ODMA, 0 for IDMA. Bit 3:0 indicates the respective DMA engine index. Programmed before TSCCI = 1.

12.2.182 Wall Frame Counter Captured (WALFCC0)—Offset 524h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO/V	**Frame Number (FN):** Indicates the 23-bit frame number captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.
8:0	0h RO/V	**Clock in Frame (CIF):** Indicates the 9-bit clock in frame value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

12.2.183 Time Stamp Counter Captured Lower (TSCCL0)—Offset 528h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Counter Captured Lower (CCL):** Indicates the lower 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

12.2.184 Time Stamp Counter Captured Upper (TSCCU0)—Offset 52Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Counter Captured Upper (CCU):** Indicates the upper 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

12.2.185 Linear Link Position Frame Offset Captured (LLPFOC0)—Offset 534h

This register is to report additional accuracy details for captures made in between of two updates of LLP values, in number of 48 KHz HD Audio frames of the corresponding link. Audio streams with 44.1 KHz base rate and non zero divider FMT value will skip frames periodically on the Intel HD Audio link and Intel iDisplay Audio link in order to normalize its sampling rate to the 48 KHz HD Audio frame rate; hence; the frame offset will be useful in these cases.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RO/V	**Frame Offset Captured (FOC):** When the LLPCL and LLPCU registers are updated, this field records the elapsed number of 48 KHz HD Audio frames since the last LLP value change. Valid and static when GTSCC.TSCCD = 1.

12.2.186 Linear Link Position Captured Lower (LLPCL0)—Offset 538h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Linear Link Position Captured Lower (LLPCL):** Indicates the lower 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCL value that is captured is the LLPL value at the previous HD Audio frame boundary, not the live LLPL register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

12.2.187 Linear Link Position Captured Upper (LLPCU0)—Offset 53Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Linear Link Position Captured Upper (LLPCU):** Indicates the upper 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCU value that is captured is the LLPU value at the previous HD Audio frame boundary, not the live LLPU register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

12.2.188 Global Time Synchronization Capture Control (GTSCC1)—Offset 540h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Time Stamp Counter Capture Done (TSCCD):** This bit is set when a valid TSC value has been captured: WALFCC, TSCCL, TSCCU, LLPFOC, LLPCL, and LLPCH contain valid data. The Intel HD Audio driver software must acknowledge the completion by writing 1 to clear this bit.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW	**Time Stamp Counter Capture Done Interrupt Enable (TSCCDIE):** If set to 1, TSCCD bit can pass through to cause an interrupt status reported in INTSTS.CIS bit, and cause an interrupt to CPU if INTCTL.CIE = 1 and INTCTL.GIE = 1.
29:6	0h RO	**Reserved (RSVD1):** Reserved.
5	0h RW/1S/V	**Time Stamp Counter Capture Initiate (TSCCI):** Write to 1 to initiate Global Time Synchronization capture for measuring TSC offset to local wall frame info. Cleared to 0 by hardware when the process is completed.
4:0	0h RW	**Capture DMA Select (CDMAS):** To select which DMA's LLPL, and LLPU value to be captured together with the TSC value. Bit 4 = 1 for ODMA, 0 for IDMA. Bit 3:0 indicates the respective DMA engine index. Programmed before TSCCI = 1.

12.2.189 Wall Frame Counter Captured (WALFCC1)—Offset 544h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

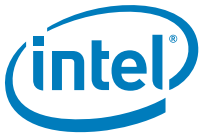
Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO/V	**Frame Number (FN):** Indicates the 23-bit frame number captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.
8:0	0h RO/V	**Clock in Frame (CIF):** Indicates the 9-bit clock in frame value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

12.2.190 Time Stamp Counter Captured Lower (TSCCL1)—Offset 548h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Counter Captured Lower (CCL):** Indicates the lower 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

12.2.191 Time Stamp Counter Captured Upper (TSCCU1)—Offset 54Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Counter Captured Upper (CCU):** Indicates the upper 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

12.2.192 Linear Link Position Frame Offset Captured (LLPFOC1)—Offset 554h

This register is to report additional accuracy details for captures made in between of two updates of LLP values, in number of 48 KHz HD Audio frames of the corresponding link. Audio streams with 44.1 KHz base rate and non zero divider FMT value will skip frames periodically on the Intel HD Audio link and Intel iDisplay Audio link in order to normalize its sampling rate to the 48 KHz HD Audio frame rate; hence; the frame offset will be useful in these cases.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RO/V	**Frame Offset Captured (FOC):** When the LLPCL and LLPCU registers are updated, this field records the elapsed number of 48 KHz HD Audio frames since the last LLP value change. Valid and static when GTSCC.TSCCD = 1.

12.2.193 Linear Link Position Captured Lower (LLPCL1)—Offset 558h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Linear Link Position Captured Lower (LLPCL):** Indicates the lower 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCL value that is captured is the LLPL value at the previous HD Audio frame boundary, not the live LLPL register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

12.2.194 Linear Link Position Captured Upper (LLPCU1)—Offset 55Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Linear Link Position Captured Upper (LLPCU):** Indicates the upper 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCU value that is captured is the LLPU value at the previous HD Audio frame boundary, not the live LLPU register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

12.2.195 Software Position Based FIFO Capability Header (SPBFCH)—Offset 700h

This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.
27:16	4h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.
15:0	0h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. This is the last capability in the linked list. Locked when FNCFG.BCLD = 1.

12.2.196 Software Position Based FIFO Control (SPBFCTL)—Offset 704h

The number of SPIBE bits in this register is depending on the total number of stream DMA implemented, represented as x in the register table.
The x value is determined by the parameter equation: HSTISC + HSTOSC.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved (RSVD1):** Reserved.
12:0	0h RW	**Software Position in Buffer Enable (SPIBE):** When set to 1, the SPIB register is the limit where the DMA will not access beyond the value programmed. When clear to 0, the SPIB register is ignored and DMA will operate in legacy mode with the minimum FIFO size. Note that it is possible for SW to set this SPIBE bit after the RUN bit is set as SW may only update the SPIB after it fill up a large portion of the ring buffer. However, once set, it must remain set until SRST take place.

12.2.197 Input/Output Stream Descriptor x Software Position in Buffer (ISD0SPIB)—Offset 708h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.198 Input/Output Stream Descriptor x Max FIFO Size (ISD0MAXFIFOS)—Offset 70Ch

Register for Input/Output Stream Descriptor x Max FIFO Size.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23:0	0h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allow through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

12.2.199 Input/Output Stream Descriptor x Software Position in Buffer (ISD1SPIB)—Offset 710h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.200 Input/Output Stream Descriptor x Max FIFO Size (ISD1MAXFIFOS)—Offset 714h

Register for Input/Output Stream Descriptor x Max FIFO Size.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23:0	0h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allow through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

12.2.201 Input/Output Stream Descriptor x Software Position in Buffer (ISD2SPIB)—Offset 718h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.202 Input/Output Stream Descriptor x Max FIFO Size (ISD2MAXFIFOS)—Offset 71Ch

Register for Input/Output Stream Descriptor x Max FIFO Size.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23:0	0h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allow through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

12.2.203 Input/Output Stream Descriptor x Software Position in Buffer (ISD3SPIB)—Offset 720h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.204 Input/Output Stream Descriptor x Max FIFO Size (ISD3MAXFIFOS)—Offset 724h

Register for Input/Output Stream Descriptor x Max FIFO Size.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23:0	0h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allow through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

12.2.205 Input/Output Stream Descriptor x Software Position in Buffer (ISD4SPIB)—Offset 728h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.206 Input/Output Stream Descriptor x Max FIFO Size (ISD4MAXFIFOS)—Offset 72Ch

Register for Input/Output Stream Descriptor x Max FIFO Size.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23:0	0h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allow through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

12.2.207 Input/Output Stream Descriptor x Software Position in Buffer (ISD5SPIB)—Offset 730h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.208 Input/Output Stream Descriptor x Max FIFO Size (ISD5MAXFIFOS)—Offset 734h

Register for Input/Output Stream Descriptor x Max FIFO Size.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23:0	0h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allow through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

12.2.209 Input/Output Stream Descriptor x Software Position in Buffer (ISD6SPIB)—Offset 738h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

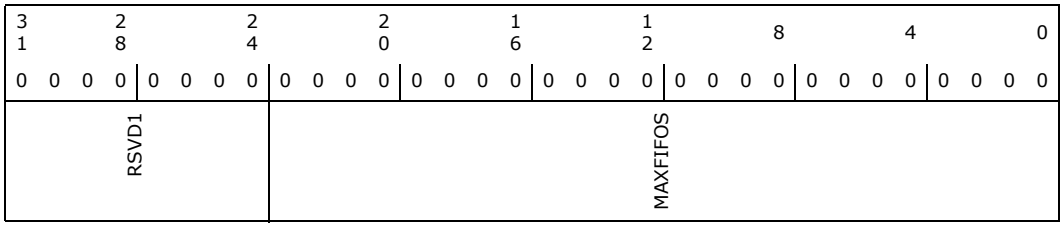
12.2.210 Input/Output Stream Descriptor x Max FIFO Size (ISD6MAXFIFOS)—Offset 73Ch

Register for Input/Output Stream Descriptor x Max FIFO Size.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23:0	0h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allow through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

12.2.211 Input/Output Stream Descriptor x Software Position in Buffer (OSD0SPIB)—Offset 740h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.212 Input/Output Stream Descriptor x Max FIFO Size (OSD0MAXFIFOS)—Offset 744h

Register for Input/Output Stream Descriptor x Max FIFO Size.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23:0	0h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allow through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

12.2.213 Input/Output Stream Descriptor x Software Position in Buffer (OSD1SPIB)—Offset 748h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.214 Input/Output Stream Descriptor x Max FIFO Size (OSD1MAXFIFOS)—Offset 74Ch

Register for Input/Output Stream Descriptor x Max FIFO Size.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23:0	0h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allow through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

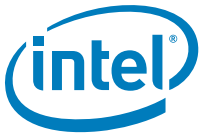
12.2.215 Input/Output Stream Descriptor x Software Position in Buffer (OSD2SPIB)—Offset 750h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.216 Input/Output Stream Descriptor x Max FIFO Size (OSD2MAXFIFOS)—Offset 754h

Register for Input/Output Stream Descriptor x Max FIFO Size.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23:0	0h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allow through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

12.2.217 Input/Output Stream Descriptor x Software Position in Buffer (OSD3SPIB)—Offset 758h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.218 Input/Output Stream Descriptor x Max FIFO Size (OSD3MAXFIFOS)—Offset 75Ch

Register for Input/Output Stream Descriptor x Max FIFO Size.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23:0	0h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allow through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

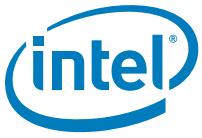
12.2.219 Input/Output Stream Descriptor x Software Position in Buffer (OSD4SPIB)—Offset 760h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.220 Input/Output Stream Descriptor x Max FIFO Size (OSD4MAXFIFOS)—Offset 764h

Register for Input/Output Stream Descriptor x Max FIFO Size.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23:0	0h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allow through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

12.2.221 Input/Output Stream Descriptor x Software Position in Buffer (OSD5SPIB)—Offset 768h

This register specifies the current SW read (for input stream) or write (for output stream) location in the SW ring buffer.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Software Position in Buffer (SPIB):** Indicates the number of bytes that SW has read from (for input stream) or write to (for output stream) the SW ring buffer. This register value should count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.222 Input/Output Stream Descriptor x Max FIFO Size (OSD5MAXFIFOS)—Offset 76Ch

Register for Input/Output Stream Descriptor x Max FIFO Size.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23:0	0h RO/V	**Max FIFO Size (MAXFIFOS):** Indicates the maximum FIFO size HW is able to buffer if SW allow through the use of SPIB register, hence reduce the interval of waking up the system to evict (for input) or fetch (for output) audio sample, achieving low power operation.

12.2.223 Processing Pipe Capability Header (PPCH)—Offset 800h

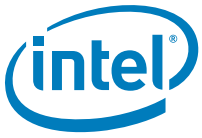
This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 30500h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.



Bit Range	Default & Access	Field Name (ID): Description
27:16	3h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.
15:0	500h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to Global Time Synchronization capability. Locked when FNCFG.BCLD = 1.

12.2.224 Processing Pipe Control (PPCTL)—Offset 804h

This register is not affected by stream reset.
Note that the PROCEN bit should only be modified when the corresponding host DMA and link DMA are idle, i.e. RUN bits are cleared, and the DMA contexts have been destroyed through SRST bits if it was previously activated.
Note that GPROCEN bit does not really enable or disable the Audio DSP operation, but mainly to workaround some legacy Intel HD Audio driver software such that if GPROCEN = 0, ADSPxBA (BAR2) is mapped to the Intel HD Audio memory mapped configuration registers, for complacency with some legacy SW implementation. If GPROCEN = 1, only then ADSPxBA (BAR2) is mapped to the actual Audio DSP memory mapped configuration registers.
The number of PROCEN bits in this register is depending on the total number of stream DMA implemented, represented as x in the register table.
The x value is determined by the parameter equation: HSTISC + HSTOSC.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Processing Interrupt Enable (PIE):** Enables the general interrupt for the Audio DSP function. When set to 1 (and GIE is enabled), the Audio DSP generates an interrupt when the PIS bit gets set.
30	0h RW	**Global Processing Enable (GPROCEN):** When set to 1, it indicates that the Audio DSP is enabled for operation.
29:13	0h RO	**Reserved (RSVD1):** Reserved.
12:0	0h RW	**Processing Enable (PROCEN):** When set to 1 the DMA engine associated with this stream will be enabled to route the audio stream to DSP audio pipes in the Audio DSP for processing. When cleared to 0 the DMA engine associated with this stream will be bypassing the Audio DSP and route the audio stream directly to the audio link.

12.2.225 Processing Pipe Status (PPSTS)—Offset 808h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Processing Interrupt Status (PIS):** Status of general interrupt for the Audio DSP function. A 1 indicates that an interrupt condition occurred in the Audio DSP function. The exact cause can be determined by interrogating the ADSPIS register. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the interrupt status bits in ADSPIS register.
30:0	0h RO	**Reserved (RSVD1):** Reserved.

12.2.226 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC0LLPL)—Offset 810h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.227 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC0LLPU)—Offset 814h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.228 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC0LDPL)—Offset 818h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.229 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC0LDPU)—Offset 81Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.230 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC1LLPL)—Offset 820h

r

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

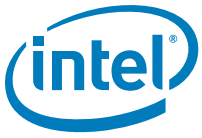
Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.231 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC1LLPU)—Offset 824h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.232 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC1LDPL)—Offset 828h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.233 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC1LDPU)—Offset 82Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.234 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC2LLPL)—Offset 830h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.235 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC2LLPU)—Offset 834h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.236 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC2LDPL)—Offset 838h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.237 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC2LDPU)—Offset 83Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.238 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC3LLPL)—Offset 840h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.239 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC3LLPU)—Offset 844h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.240 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC3LDPL)—Offset 848h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.241 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC3LDPU)—Offset 84Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.242 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC4LLPL)—Offset 850h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.243 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC4LLPU)—Offset 854h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

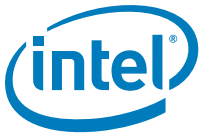
12.2.244 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC4LDPL)—Offset 858h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.



12.2.245 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC4LDPU)—Offset 85Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.246 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC5LLPL)—Offset 860h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.247 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC5LLPU)—Offset 864h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.248 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC5LDPL)—Offset 868h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.249 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC5LDPU)—Offset 86Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.250 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC6LLPL)—Offset 870h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.251 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC6LLPU)—Offset 874h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.252 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC6LDPL)—Offset 878h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.253 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC6LDPU)—Offset 87Ch

Access Method

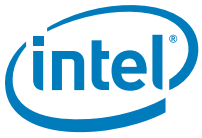
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.254 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC0LLPL)—Offset 880h

Access Method



Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.255 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC0LLPU)—Offset 884h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.256 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC0LDPL)—Offset 888h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.257 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC0LDPU)—Offset 88Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

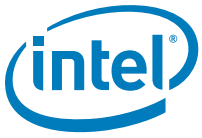
Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.258 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC1LLPL)—Offset 890h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.259 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC1LLPU)—Offset 894h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.260 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC1LDPL)—Offset 898h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.261 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC1LDPU)—Offset 89Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.262 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC2LLPL)—Offset 8A0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.263 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC2LLPU)—Offset 8A4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.264 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC2LDPL)—Offset 8A8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.265 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC2LDPU)—Offset 8ACh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.266 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC3LLPL)—Offset 8B0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.267 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC3LLPU)—Offset 8B4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.268 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC3LDPL)—Offset 8B8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.269 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC3LDPU)—Offset 8BCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.270 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC4LLPL)—Offset 8C0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.271 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC4LLPU)—Offset 8C4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.272 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC4LDPL)—Offset 8C8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.273 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC4LDPU)—Offset 8CCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.274 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC5LLPL)—Offset 8D0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.275 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC5LLPU)—Offset 8D4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.276 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC5LDPL)—Offset 8D8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.277 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC5LDPU)—Offset 8DCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the SoC backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.278 Input/Output Processing Pipe's Link Connection x Control (IPPLC0CTL)—Offset 8E0h

SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000: Reserved (Indicates Unused) • 0001: Stream 1 • ... • 1110: Stream 14 • 1111: Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.279 Input/Output Processing Pipe's Link Connection x Format (IPPLC0FMT)—Offset 8E4h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000=Divide by 1 (48 kHz, 44.1 kHz) • 001=Divide by 2 (24 kHz, 22.05 kHz) • 010=Divide by 3 (16 kHz, 32 kHz) • 011=Divide by 4 (11.025 kHz) • 100=Divide by 5 (9.6 kHz) • 101=Divide by 6 (8 kHz) • 110=Divide by 7 • 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.280 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC0LLPL)—Offset 8E8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.281 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC0LLPU)—Offset 8ECh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

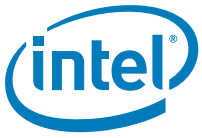
12.2.282 Input/Output Processing Pipe's Link Connection x Control (IPPLC1CTL)—Offset 8F0h

SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000: Reserved (Indicates Unused) • 0001: Stream 1 • ... • 1110: Stream 14 • 1111: Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

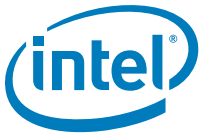
12.2.283 Input/Output Processing Pipe's Link Connection x Format (IPPLC1FMT)—Offset 8F4h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000=Divide by 1 (48 kHz, 44.1 kHz) • 001=Divide by 2 (24 kHz, 22.05 kHz) • 010=Divide by 3 (16 kHz, 32 kHz) • 011=Divide by 4 (11.025 kHz) • 100=Divide by 5 (9.6 kHz) • 101=Divide by 6 (8 kHz) • 110=Divide by 7 • 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16



12.2.284 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC1LLPL)—Offset 8F8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.285 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC1LLPU)—Offset 8FCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.286 Input/Output Processing Pipe's Link Connection x Control (IPPLC2CTL)—Offset 900h

SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

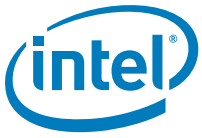
Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000: Reserved (Indicates Unused) • 0001: Stream 1 • ... • 1110: Stream 14 • 1111: Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.287 Input/Output Processing Pipe's Link Connection x Format (IPPLC2FMT)—Offset 904h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000=Divide by 1 (48 kHz, 44.1 kHz) • 001=Divide by 2 (24 kHz, 22.05 kHz) • 010=Divide by 3 (16 kHz, 32 kHz) • 011=Divide by 4 (11.025 kHz) • 100=Divide by 5 (9.6 kHz) • 101=Divide by 6 (8 kHz) • 110=Divide by 7 • 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.288 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC2LLPL)—Offset 908h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.289 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC2LLPU)—Offset 90Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

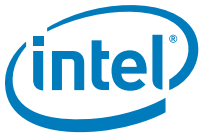
12.2.290 Input/Output Processing Pipe's Link Connection x Control (IPPLC3CTL)—Offset 910h

SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000: Reserved (Indicates Unused) • 0001: Stream 1 • ... • 1110: Stream 14 • 1111: Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

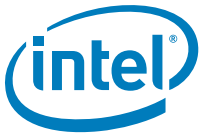
12.2.291 Input/Output Processing Pipe's Link Connection x Format (IPPLC3FMT)—Offset 914h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000=Divide by 1 (48 kHz, 44.1 kHz) • 001=Divide by 2 (24 kHz, 22.05 kHz) • 010=Divide by 3 (16 kHz, 32 kHz) • 011=Divide by 4 (11.025 kHz) • 100=Divide by 5 (9.6 kHz) • 101=Divide by 6 (8 kHz) • 110=Divide by 7 • 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16



12.2.292 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC3LLPL)—Offset 918h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.293 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC3LLPU)—Offset 91Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.294 Input/Output Processing Pipe's Link Connection x Control (IPPLC4CTL)—Offset 920h

SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000: Reserved (Indicates Unused) • 0001: Stream 1 • ... • 1110: Stream 14 • 1111: Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.295 Input/Output Processing Pipe's Link Connection x Format (IPPLC4FMT)—Offset 924h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000=Divide by 1 (48 kHz, 44.1 kHz) • 001=Divide by 2 (24 kHz, 22.05 kHz) • 010=Divide by 3 (16 kHz, 32 kHz) • 011=Divide by 4 (11.025 kHz) • 100=Divide by 5 (9.6 kHz) • 101=Divide by 6 (8 kHz) • 110=Divide by 7 • 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.296 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC4LLPL)—Offset 928h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.297 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC4LLPU)—Offset 92Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

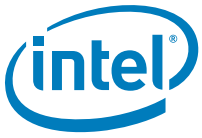
12.2.298 Input/Output Processing Pipe's Link Connection x Control (IPPLC5CTL)—Offset 930h

SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000: Reserved (Indicates Unused) • 0001: Stream 1 • ... • 1110: Stream 14 • 1111: Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

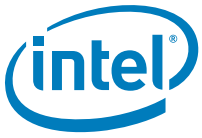
12.2.299 Input/Output Processing Pipe's Link Connection x Format (IPPLC5FMT)—Offset 934h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000=Divide by 1 (48 kHz, 44.1 kHz) • 001=Divide by 2 (24 kHz, 22.05 kHz) • 010=Divide by 3 (16 kHz, 32 kHz) • 011=Divide by 4 (11.025 kHz) • 100=Divide by 5 (9.6 kHz) • 101=Divide by 6 (8 kHz) • 110=Divide by 7 • 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16



12.2.300 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC5LLPL)—Offset 938h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.301 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC5LLPU)—Offset 93Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.302 Input/Output Processing Pipe's Link Connection x Control (IPPLC6CTL)—Offset 940h

SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

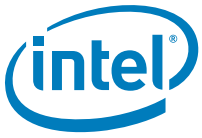
Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000: Reserved (Indicates Unused) • 0001: Stream 1 • ... • 1110: Stream 14 • 1111: Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.303 Input/Output Processing Pipe's Link Connection x Format (IPPLC6FMT)—Offset 944h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000=Divide by 1 (48 kHz, 44.1 kHz) • 001=Divide by 2 (24 kHz, 22.05 kHz) • 010=Divide by 3 (16 kHz, 32 kHz) • 011=Divide by 4 (11.025 kHz) • 100=Divide by 5 (9.6 kHz) • 101=Divide by 6 (8 kHz) • 110=Divide by 7 • 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.304 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC6LLPL)—Offset 948h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.305 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC6LLPU)—Offset 94Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

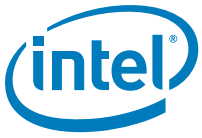
12.2.306 Input/Output Processing Pipe's Link Connection x Control (OPPLC0CTL)—Offset 950h

SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000: Reserved (Indicates Unused) • 0001: Stream 1 • ... • 1110: Stream 14 • 1111: Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

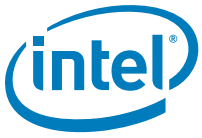
12.2.307 Input/Output Processing Pipe's Link Connection x Format (OPPLC0FMT)—Offset 954h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000=Divide by 1 (48 kHz, 44.1 kHz) • 001=Divide by 2 (24 kHz, 22.05 kHz) • 010=Divide by 3 (16 kHz, 32 kHz) • 011=Divide by 4 (11.025 kHz) • 100=Divide by 5 (9.6 kHz) • 101=Divide by 6 (8 kHz) • 110=Divide by 7 • 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16



12.2.308 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC0LLPL)—Offset 958h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.309 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC0LLPU)—Offset 95Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.310 Input/Output Processing Pipe's Link Connection x Control (OPPLC1CTL)—Offset 960h

SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

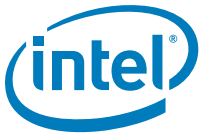
Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000: Reserved (Indicates Unused) • 0001: Stream 1 • ... • 1110: Stream 14 • 1111: Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.311 Input/Output Processing Pipe's Link Connection x Format (OPPLC1FMT)—Offset 964h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000=Divide by 1 (48 kHz, 44.1 kHz) • 001=Divide by 2 (24 kHz, 22.05 kHz) • 010=Divide by 3 (16 kHz, 32 kHz) • 011=Divide by 4 (11.025 kHz) • 100=Divide by 5 (9.6 kHz) • 101=Divide by 6 (8 kHz) • 110=Divide by 7 • 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.312 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC1LLPL)—Offset 968h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.313 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC1LLPU)—Offset 96Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

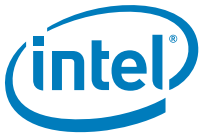
12.2.314 Input/Output Processing Pipe's Link Connection x Control (OPPLC2CTL)—Offset 970h

SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000: Reserved (Indicates Unused) • 0001: Stream 1 • ... • 1110: Stream 14 • 1111: Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.315 Input/Output Processing Pipe's Link Connection x Format (OPPLC2FMT)—Offset 974h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000=Divide by 1 (48 kHz, 44.1 kHz) • 001=Divide by 2 (24 kHz, 22.05 kHz) • 010=Divide by 3 (16 kHz, 32 kHz) • 011=Divide by 4 (11.025 kHz) • 100=Divide by 5 (9.6 kHz) • 101=Divide by 6 (8 kHz) • 110=Divide by 7 • 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.316 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC2LLPL)—Offset 978h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.317 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC2LLPU)—Offset 97Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.318 Input/Output Processing Pipe's Link Connection x Control (OPPLC3CTL)—Offset 980h

SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000: Reserved (Indicates Unused) • 0001: Stream 1 • ... • 1110: Stream 14 • 1111: Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.319 Input/Output Processing Pipe's Link Connection x Format (OPPLC3FMT)—Offset 984h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000=Divide by 1 (48 kHz, 44.1 kHz) • 001=Divide by 2 (24 kHz, 22.05 kHz) • 010=Divide by 3 (16 kHz, 32 kHz) • 011=Divide by 4 (11.025 kHz) • 100=Divide by 5 (9.6 kHz) • 101=Divide by 6 (8 kHz) • 110=Divide by 7 • 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.320 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC3LLPL)—Offset 988h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.321 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC3LLPU)—Offset 98Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

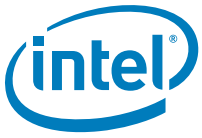
12.2.322 Input/Output Processing Pipe's Link Connection x Control (OPPLC4CTL)—Offset 990h

SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000: Reserved (Indicates Unused) • 0001: Stream 1 • ... • 1110: Stream 14 • 1111: Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

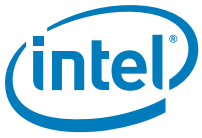
12.2.323 Input/Output Processing Pipe's Link Connection x Format (OPPLC4FMT)—Offset 994h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000=Divide by 1 (48 kHz, 44.1 kHz) • 001=Divide by 2 (24 kHz, 22.05 kHz) • 010=Divide by 3 (16 kHz, 32 kHz) • 011=Divide by 4 (11.025 kHz) • 100=Divide by 5 (9.6 kHz) • 101=Divide by 6 (8 kHz) • 110=Divide by 7 • 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16



12.2.324 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC4LLPL)—Offset 998h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.325 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC4LLPU)—Offset 99Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.326 Input/Output Processing Pipe's Link Connection x Control (OPPLC5CTL)—Offset 9A0h

SRST bit is not affected by stream reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. • 0000: Reserved (Indicates Unused) • 0001: Stream 1 • ... • 1110: Stream 14 • 1111: Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	**Reserved (RSVD1):** Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

12.2.327 Input/Output Processing Pipe's Link Connection x Format (OPPLC5FMT)—Offset 9A4h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD1):** Reserved.
14	0h RW	**Sample Base Rate (BASE):** • 0: 48 kHz • 1: 44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** • 000: 48 kHz/44.1 kHz or less • 001: x2 (96 kHz, 88.2 kHz, 32 kHz) • 010: x3 (144 kHz) • 011: x4 (192 kHz, 176.4 kHz) • 100-111: Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** • 000=Divide by 1 (48 kHz, 44.1 kHz) • 001=Divide by 2 (24 kHz, 22.05 kHz) • 010=Divide by 3 (16 kHz, 32 kHz) • 011=Divide by 4 (11.025 kHz) • 100=Divide by 5 (9.6 kHz) • 101=Divide by 6 (8 kHz) • 110=Divide by 7 • 111=Divide by 8 (6 kHz)
7	0h RO	**Reserved (RSVD2):** Reserved.
6:4	0h RW	**Bits per Sample (BITS):** • 000: 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. • 001: 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. • 010: 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 011: 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 100: 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. • 101-111: Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: • 0000: 1 • 0001: 2 • ... • 1111: 16

12.2.328 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC5LLPL)—Offset 9A8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

12.2.329 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC5LLPU)—Offset 9ACh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

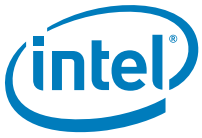
12.2.330 Multiple Links Capability Header (MLCH)—Offset C00h

This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 20800h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.
27:16	2h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.
15:0	800h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to Processing Pipe capability. Locked when FNCFG.BCLD = 1.

12.2.331 Multiple Links Capability Declaration (MLCD)—Offset C04h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD1):** Reserved.
3:0	1h RO	**Link Count (LCOUNT):** Indicates the number of links. Up to 15 links can be supported. A '0' indicates 1 link, and '1110' indicates 15 links. Note: '1111' is reserved. Note that this Link Count is the cumulative total number of links where the links can be heterogeneous. This field is hardcoded to parameter LNKC-1.

12.2.332 Link x Capabilities (LCAP0)—Offset C40h

This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 7h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Audio Link Type (ALT):** Indicates which Link Type this link belongs to. • 0001-1111: Reserved • 0000: Intel HD Audio Link Locked when FNCFG.BCLD = 1.
27:26	0h RO	**Reserved (RSVD1):** Reserved.
25:24	0h RW/L	**Number of Serial Data Out Signals (NSDO):** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. Locked when FNCFG.BCLD = 1.
23:6	0h RO	**Reserved (RSVD0):** Reserved.
5	0h RW/L	**192 MHz Supported (S192):** Indicates 192 MHz clock is supported. Locked when FNCFG.BCLD = 1.
4	0h RW/L	**96 MHz Supported (S96):** Indicates 96 MHz clock is supported. Locked when FNCFG.BCLD = 1.
3	0h RW/L	**48 MHz Supported (S48):** Indicates 48 MHz clock is supported. Locked when FNCFG.BCLD = 1.
2	1h RW/L	**24 MHz Supported (S24):** Indicates 24 MHz clock is supported. Locked when FNCFG.BCLD = 1.
1	1h RW/L	**12 MHz Supported (S12):** Indicates 12 MHz clock is supported. Locked when FNCFG.BCLD = 1.
0	1h RW/L	**6 MHz Supported (S6):** Indicates 6 MHz clock is supported. Locked when FNCFG.BCLD = 1.

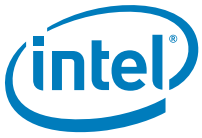
12.2.333 Link x Control (LCTL0)—Offset C44h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10002h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23	0h RO/V	**Current Power Active (CPA):** This value changes to the value set by SPA when the power of the link has reached that state. Software sets SPA, then monitors CPA to know when the link has changed state.
22:17	0h RO	**Reserved (RSVD2):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Set Power Active (SPA):** Software sets this bit to '1' to turn the link on (provided CRSTB = 1), and clears it to '0' when it wishes to turn the link off. When CPA matches the value of this bit, the achieved power state has been reached. Software is expected to wait for CPA to match SPA before it can program SPA again. Any deviation may result in undefined behaviour.
15:8	0h RO	**Reserved (RSVD3):** Reserved.
7:4	0h RO/V	**Current Clock Frequency (CCF):** Indicates the current clock frequency. When SCF is changed, and the link has moved to the new frequency, CCF shall take SCF value.
3:0	2h RW	**Set Clock Frequency (SCF):** Indicates the frequency that software wishes the link to run at. Changing this value to a value not supported by Link Capabilities shall result in indeterminate results. The possible encodings are: Encoding | Frequency • 0000: 6 MHz • 0001: 12 MHz • 0010: 24 MHz • 0011: 48 MHz • 0100: 96 MHz • 0101: Reserved for 192 MHz • 0110-1111: Reserved When the frequency changes, CCF shall change to SCF, indicating to software that the frequency change occurred. Software is expected to wait for CCF to match SCF, indicating that the frequency change occurred.

12.2.334 Link x Output Stream ID Mapping Valid (LOSIDV0)—Offset C48h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFEh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD1):** Reserved.
15	1h RW	**Output Stream ID of 15 is Valid for this Link (L1OSIDV15):** This link will claim / forward output cycles with Stream ID = 1111b.
14	1h RW	**Output Stream ID of 14 is Valid for this Link (L1OSIDV14):** This link will claim / forward output cycles with Stream ID = 1110b.

Bit Range	Default & Access	Field Name (ID): Description
13	1h RW	**Output Stream ID of 13 is Valid for this Link (L1OSIDV13):** This link will claim / forward output cycles with Stream ID = 1101b.
12	1h RW	**Output Stream ID of 12 is Valid for this Link (L1OSIDV12):** This link will claim / forward output cycles with Stream ID = 1100b.
11	1h RW	**Output Stream ID of 11 is Valid for this Link (L1OSIDV11):** This link will claim / forward output cycles with Stream ID = 1011b.
10	1h RW	**Output Stream ID of 10 is Valid for this Link (L1OSIDV10):** This link will claim / forward output cycles with Stream ID = 1010b.
9	1h RW	**Output Stream ID of 9 is Valid for this Link (L1OSIDV9):** This link will claim / forward output cycles with Stream ID = 1001b.
8	1h RW	**Output Stream ID of 8 is Valid for this Link (L1OSIDV8):** This link will claim / forward output cycles with Stream ID = 1000b.
7	1h RW	**Output Stream ID of 7 is Valid for this Link (L1OSIDV7):** This link will claim / forward output cycles with Stream ID = 0111b.
6	1h RW	**Output Stream ID of 6 is Valid for this Link (L1OSIDV6):** This link will claim / forward output cycles with Stream ID = 0110b.
5	1h RW	**Output Stream ID of 5 is Valid for this Link (L1OSIDV5):** This link will claim / forward output cycles with Stream ID = 0101b.
4	1h RW	**Output Stream ID of 4 is Valid for this Link (L1OSIDV4):** This link will claim / forward output cycles with Stream ID = 0100b.
3	1h RW	**Output Stream ID of 3 is Valid for this Link (L1OSIDV3):** This link will claim / forward output cycles with Stream ID = 0011b.
2	1h RW	**Output Stream ID of 2 is Valid for this Link (L1OSIDV2):** This link will claim / forward output cycles with Stream ID = 0010b.
1	1h RW	**Output Stream ID of 1 is Valid for this Link (L1OSIDV1):** This link will claim / forward output cycles with Stream ID = 0001b.
0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.335 Link x SDI Identifier (LSDIID0)—Offset C4Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD1):** Reserved.
15	0h RO	**Reserved (RSVD):** Reserved.
14	0h RO	**SDI 14 (SDIID14):** This link uses SDI 14. This bit is hardcoded per parameter LSDIID14 assignment.
13	0h RO	**SDI 13 (SDIID13):** This link uses SDI 13. This bit is hardcoded per parameter LSDIID13 assignment.
12	0h RO	**SDI 12 (SDIID12):** This link uses SDI 12. This bit is hardcoded per parameter LSDIID12 assignment.
11	0h RO	**SDI 11 (SDIID11):** This link uses SDI 11. This bit is hardcoded per parameter LSDIID11 assignment.
10	0h RO	**SDI 10 (SDIID10):** This link uses SDI 10. This bit is hardcoded per parameter LSDIID10 assignment.
9	0h RO	**SDI 9 (SDIID9):** This link uses SDI 9. This bit is hardcoded per parameter LSDIID9 assignment.
8	0h RO	**SDI 8 (SDIID8):** This link uses SDI 8. This bit is hardcoded per parameter LSDIID8 assignment.
7	0h RO	**SDI 7 (SDIID7):** This link uses SDI 7. This bit is hardcoded per parameter LSDIID7 assignment.
6	0h RO	**SDI 6 (SDIID6):** This link uses SDI 6. This bit is hardcoded per parameter LSDIID6 assignment.
5	0h RO	**SDI 5 (SDIID5):** This link uses SDI 5. This bit is hardcoded per parameter LSDIID5 assignment.
4	0h RO	**SDI 4 (SDIID4):** This link uses SDI 4. This bit is hardcoded per parameter LSDIID4 assignment.
3	0h RO	**SDI 3 (SDIID3):** This link uses SDI 3. This bit is hardcoded per parameter LSDIID3 assignment.
2	0h RO	**SDI 2 (SDIID2):** This link uses SDI 2. This bit is hardcoded per parameter LSDIID2 assignment.
1	1h RO	**SDI 1 (SDIID1):** This link uses SDI 1. This bit is hardcoded per parameter LSDIID1 assignment.
0	1h RO	**SDI 0 (SDIID0):** This link uses SDI 0. This bit is hardcoded per parameter LSDIID0 assignment.

12.2.336 Link x Per Stream Output Overhead (LPSOO0)—Offset C50h

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO/V	**Per Stream Output Overhead (PSOO):** Indicates the SDO Output Overhead on a per stream basis. This does not include bandwidth used for command and control. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LOUTPAY) - (NumOfStreams * LPSOO).

12.2.337 Link x Per Stream Input Overhead (LPSIO0)—Offset C52h

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO/V	**Per Stream Input Overhead (PSIO):** Indicates the SDI Input Overhead on a per stream basis. This does not include bandwidth used for response. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LINPAY) - (NumOfStreams * LPSIO).

12.2.338 Link x Wall Frame Counter (LWALFC0)—Offset C58h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO/V	**Frame Number (FN):** 23-bit counter that is incremented when CIF rolls over from 499 to 0. This counter will roll over to zero with a period of approximately 174 seconds.

Bit Range	Default & Access	Field Name (ID): Description
8:0	0h RO/V	**Clock in Frame (CIF):** 9-bit counter that is incremented on each link BCLK period and rolls over from 499 to 0. This counter will roll over to zero with a period of 48 KHz HD Audio frame. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed.

12.2.339 Link x Output Payload Capability (LOUTPAY6M0)—Offset C60h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] | Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] | Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.340 Link x Output Payload Capability (LOUTPAY12M0)—Offset C62h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] | Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] | Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.341 Link x Output Payload Capability (LOUTPAY24M0)—Offset C64h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] | Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] | Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.342 Link x Output Payload Capability (LOUTPAY48M0)—Offset C66h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] | Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] | Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.343 Link x Output Payload Capability (LOUTPAY96M0)—Offset C68h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] | Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] | Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.344 Link x Output Payload Capability (LOUTPAY192M0)—Offset C6Ah

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

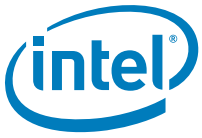
Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] | Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] | Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.345 Link x Input Payload Capability (LINPAY6M0)—Offset C70h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.346 Link x Input Payload Capability (LINPAY12M0)—Offset C72h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

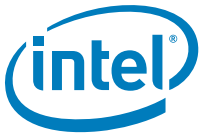
Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.347 Link x Input Payload Capability (LINPAY24M0)—Offset C74h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.348 Link x Input Payload Capability (LINPAY48M0)—Offset C76h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

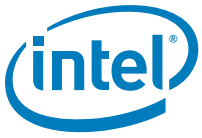
Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.349 Link x Input Payload Capability (LINPAY96M0)—Offset C78h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.350 Link x Input Payload Capability (LINPAY192M0)—Offset C7Ah

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.351 Link x Capabilities (LCAP1)—Offset C80h

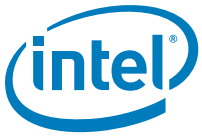
This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1Fh

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Audio Link Type (ALT):** Indicates which Link Type this link belongs to. • 0001-1111: Reserved • 0000: Intel HD Audio Link Locked when FNCFG.BCLD = 1.
27:26	0h RO	**Reserved (RSVD1):** Reserved.
25:24	0h RW/L	**Number of Serial Data Out Signals (NSDO):** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. Locked when FNCFG.BCLD = 1.
23:6	0h RO	**Reserved (RSVD0):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/L	**192 MHz Supported (S192):** Indicates 192 MHz clock is supported. Locked when FNCFG.BCLD = 1.
4	1h RW/L	**96 MHz Supported (S96):** Indicates 96 MHz clock is supported. Locked when FNCFG.BCLD = 1.
3	1h RW/L	**48 MHz Supported (S48):** Indicates 48 MHz clock is supported. Locked when FNCFG.BCLD = 1.
2	1h RW/L	**24 MHz Supported (S24):** Indicates 24 MHz clock is supported. Locked when FNCFG.BCLD = 1.
1	1h RW/L	**12 MHz Supported (S12):** Indicates 12 MHz clock is supported. Locked when FNCFG.BCLD = 1.
0	1h RW/L	**6 MHz Supported (S6):** Indicates 6 MHz clock is supported. Locked when FNCFG.BCLD = 1.

12.2.352 Link x Control (LCTL1)—Offset C84h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10004h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD1):** Reserved.
23	0h RO/V	**Current Power Active (CPA):** This value changes to the value set by SPA when the power of the link has reached that state. Software sets SPA, then monitors CPA to know when the link has changed state.
22:17	0h RO	**Reserved (RSVD2):** Reserved.
16	1h RW	**Set Power Active (SPA):** Software sets this bit to '1' to turn the link on (provided CRSTB = 1), and clears it to '0' when it wishes to turn the link off. When CPA matches the value of this bit, the achieved power state has been reached. Software is expected to wait for CPA to match SPA before it can program SPA again. Any deviation may result in undefined behaviour.
15:8	0h RO	**Reserved (RSVD3):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO/V	**Current Clock Frequency (CCF):** Indicates the current clock frequency. When SCF is changed, and the link has moved to the new frequency, CCF shall take SCF value.
3:0	4h RW	**Set Clock Frequency (SCF):** Indicates the frequency that software wishes the link to run at. Changing this value to a value not supported by Link Capabilities shall result in indeterminate results. The possible encodings are: Encoding | Frequency • 0000: 6 MHz • 0001: 12 MHz • 0010: 24 MHz • 0011: 48 MHz • 0100: 96 MHz • 0101: Reserved for 192 MHz • 0110-1111: Reserved When the frequency changes, CCF shall change to SCF, indicating to software that the frequency change occurred. Software is expected to wait for CCF to match SCF, indicating that the frequency change occurred.

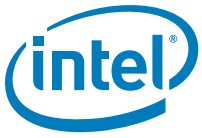
12.2.353 Link x Output Stream ID Mapping Valid (LOSIDV1)—Offset C88h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFEh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD1):** Reserved.
15	1h RW	**Output Stream ID of 15 is Valid for this Link (L1OSIDV15):** This link will claim / forward output cycles with Stream ID = 1111b.
14	1h RW	**Output Stream ID of 14 is Valid for this Link (L1OSIDV14):** This link will claim / forward output cycles with Stream ID = 1110b.
13	1h RW	**Output Stream ID of 13 is Valid for this Link (L1OSIDV13):** This link will claim / forward output cycles with Stream ID = 1101b.
12	1h RW	**Output Stream ID of 12 is Valid for this Link (L1OSIDV12):** This link will claim / forward output cycles with Stream ID = 1100b.
11	1h RW	**Output Stream ID of 11 is Valid for this Link (L1OSIDV11):** This link will claim / forward output cycles with Stream ID = 1011b.



Bit Range	Default & Access	Field Name (ID): Description
10	1h RW	**Output Stream ID of 10 is Valid for this Link (L1OSIDV10):** This link will claim / forward output cycles with Stream ID = 1010b.
9	1h RW	**Output Stream ID of 9 is Valid for this Link (L1OSIDV9):** This link will claim / forward output cycles with Stream ID = 1001b.
8	1h RW	**Output Stream ID of 8 is Valid for this Link (L1OSIDV8):** This link will claim / forward output cycles with Stream ID = 1000b.
7	1h RW	**Output Stream ID of 7 is Valid for this Link (L1OSIDV7):** This link will claim / forward output cycles with Stream ID = 0111b.
6	1h RW	**Output Stream ID of 6 is Valid for this Link (L1OSIDV6):** This link will claim / forward output cycles with Stream ID = 0110b.
5	1h RW	**Output Stream ID of 5 is Valid for this Link (L1OSIDV5):** This link will claim / forward output cycles with Stream ID = 0101b.
4	1h RW	**Output Stream ID of 4 is Valid for this Link (L1OSIDV4):** This link will claim / forward output cycles with Stream ID = 0100b.
3	1h RW	**Output Stream ID of 3 is Valid for this Link (L1OSIDV3):** This link will claim / forward output cycles with Stream ID = 0011b.
2	1h RW	**Output Stream ID of 2 is Valid for this Link (L1OSIDV2):** This link will claim / forward output cycles with Stream ID = 0010b.
1	1h RW	**Output Stream ID of 1 is Valid for this Link (L1OSIDV1):** This link will claim / forward output cycles with Stream ID = 0001b.
0	0h RO	**Reserved (RSVD2):** Reserved.

12.2.354 Link x SDI Identifier (LSDIID1)—Offset C8Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD1):** Reserved.

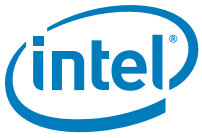
Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved (RSVD):** Reserved.
14	0h RO	**SDI 14 (SDIID14):** This link uses SDI 14. This bit is hardcoded per parameter LSDIID14 assignment.
13	0h RO	**SDI 13 (SDIID13):** This link uses SDI 13. This bit is hardcoded per parameter LSDIID13 assignment.
12	0h RO	**SDI 12 (SDIID12):** This link uses SDI 12. This bit is hardcoded per parameter LSDIID12 assignment.
11	0h RO	**SDI 11 (SDIID11):** This link uses SDI 11. This bit is hardcoded per parameter LSDIID11 assignment.
10	0h RO	**SDI 10 (SDIID10):** This link uses SDI 10. This bit is hardcoded per parameter LSDIID10 assignment.
9	0h RO	**SDI 9 (SDIID9):** This link uses SDI 9. This bit is hardcoded per parameter LSDIID9 assignment.
8	0h RO	**SDI 8 (SDIID8):** This link uses SDI 8. This bit is hardcoded per parameter LSDIID8 assignment.
7	0h RO	**SDI 7 (SDIID7):** This link uses SDI 7. This bit is hardcoded per parameter LSDIID7 assignment.
6	0h RO	**SDI 6 (SDIID6):** This link uses SDI 6. This bit is hardcoded per parameter LSDIID6 assignment.
5	0h RO	**SDI 5 (SDIID5):** This link uses SDI 5. This bit is hardcoded per parameter LSDIID5 assignment.
4	0h RO	**SDI 4 (SDIID4):** This link uses SDI 4. This bit is hardcoded per parameter LSDIID4 assignment.
3	0h RO	**SDI 3 (SDIID3):** This link uses SDI 3. This bit is hardcoded per parameter LSDIID3 assignment.
2	1h RO	**SDI 2 (SDIID2):** This link uses SDI 2. This bit is hardcoded per parameter LSDIID2 assignment.
1	0h RO	**SDI 1 (SDIID1):** This link uses SDI 1. This bit is hardcoded per parameter LSDIID1 assignment.
0	0h RO	**SDI 0 (SDIID0):** This link uses SDI 0. This bit is hardcoded per parameter LSDIID0 assignment.

12.2.355 Link x Per Stream Output Overhead (LPSOO1)—Offset C90h

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO/V	**Per Stream Output Overhead (PSOO):** Indicates the SDO Output Overhead on a per stream basis. This does not include bandwidth used for command and control. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LOUTPAY) - (NumOfStreams * LPSOO).

12.2.356 Link x Per Stream Input Overhead (LPSIO1)—Offset C92h

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO/V	**Per Stream Input Overhead (PSIO):** Indicates the SDI Input Overhead on a per stream basis. This does not include bandwidth used for response. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LINPAY) - (NumOfStreams * LPSIO).

12.2.357 Link x Wall Frame Counter (LWALFC1)—Offset C98h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO/V	**Frame Number (FN):** 23-bit counter that is incremented when CIF rolls over from 499 to 0. This counter will roll over to zero with a period of approximately 174 seconds.

Bit Range	Default & Access	Field Name (ID): Description
8:0	0h RO/V	**Clock in Frame (CIF):** 9-bit counter that is incremented on each link BCLK period and rolls over from 499 to 0. This counter will roll over to zero with a period of 48 KHz HD Audio frame. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed.

12.2.358 Link x Output Payload Capability (LOUTPAY6M1)—Offset CA0h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] | Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] | Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.359 Link x Output Payload Capability (LOUTPAY12M1)—Offset CA2h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] | Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] | Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.360 Link x Output Payload Capability (LOUTPAY24M1)—Offset CA4h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

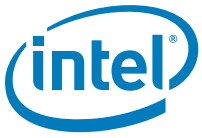
Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] | Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] | Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.361 Link x Output Payload Capability (LOUTPAY48M1)—Offset CA6h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] | Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] | Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.362 Link x Output Payload Capability (LOUTPAY96M1)—Offset CA8h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

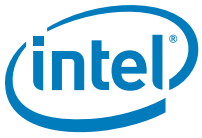
Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] | Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] | Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.363 Link x Output Payload Capability (LOUTPAY192M1)—Offset CAAh

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] | Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] | Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.364 Link x Input Payload Capability (LINPAY6M1)—Offset CB0h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

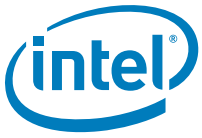
Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.365 Link x Input Payload Capability (LINPAY12M1)—Offset CB2h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.366 Link x Input Payload Capability (LINPAY24M1)—Offset CB4h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

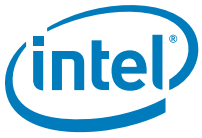
Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.367 Link x Input Payload Capability (LINPAY48M1)—Offset CB6h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.368 Link x Input Payload Capability (LINPAY96M1)—Offset CB8h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

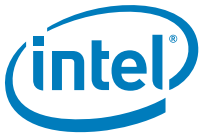
Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.369 Link x Input Payload Capability (LINPAY192M1)—Offset CBAh

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link at a given frequency. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. Reset value is dependent on the default clock frequency specified in parameter DEFLOUTPAY[x*96+95:x*96]. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. • 00h: 0 word • 01h: 1 word payload • ... • FFh: 255h word payload Offset | Frequency Encoding | Frequency • 40h+(40h*x) + 20h[15:0] | 6 MHz | 40h+(40h*x) + 28h[15:0] Reserved for 96 MHz • 40h+(40h*x) + 22h[15:0] | 12 MHz | 40h+(40h*x) + 2Ah[15:0] Reserved for 192 MHz • 40h+(40h*x) + 24h[15:0] | 24 MHz • 40h+(40h*x) + 26h[15:0] | Reserved for 48 MHz The audio bus driver queries this lookup register & LPSOO to derive the potential net output bandwidth before deciding whether to switch frequency.

12.2.370 DMA Resume Capability Header (DRSMCH)—Offset 1F00h

This register resides in Primary well (always on), or resides in Primary well (gated-controller) with state retention, and reset by platform reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 50700h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.
27:16	5h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.
15:0	700h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to SW position based FIFO capability. Locked when FNCFG.BCLD = 1.

12.2.371 DMA Resume Control (DRSMCTL)—Offset 1F04h

The number of RSM bits in this register is depending on the total number of stream DMA implemented, represented as x in the register table. The x value is determined by the parameter equation: HSTISC + HSTOSC.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved (RSVD1):** Reserved.
12:0	0h RW/1S/V	**Resume (RSM):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.

12.2.372 DMA Position in Buffer Resume (ISD0DPIBR)—Offset 1F08h

This register specifies the DPIB resume position.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

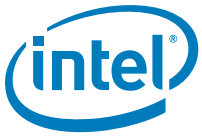
12.2.373 DMA Position in Buffer Resume (ISD1DPIBR)—Offset 1F10h

This register specifies the DPIB resume position.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

12.2.374 DMA Position in Buffer Resume (ISD2DPIBR)—Offset 1F18h

This register specifies the DPIB resume position.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

12.2.375 DMA Position in Buffer Resume (ISD3DPIBR)—Offset 1F20h

This register specifies the DPIB resume position.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

12.2.376 DMA Position in Buffer Resume (ISD4DPIBR)—Offset 1F28h

This register specifies the DPIB resume position.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

12.2.377 DMA Position in Buffer Resume (ISD5DPIBR)—Offset 1F30h

This register specifies the DPIB resume position.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

12.2.378 DMA Position in Buffer Resume (ISD6DPIBR)—Offset 1F38h

This register specifies the DPIB resume position.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

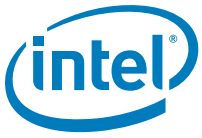
Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

12.2.379 DMA Position in Buffer Resume (OSD0DPIBR)—Offset 1F40h

This register specifies the DPIB resume position.

Access Method



Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

12.2.380 DMA Position in Buffer Resume (OSD1DPIBR)—Offset 1F48h

This register specifies the DPIB resume position.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

12.2.381 DMA Position in Buffer Resume (OSD2DPIBR)—Offset 1F50h

This register specifies the DPIB resume position.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

12.2.382 DMA Position in Buffer Resume (OSD3DPIBR)—Offset 1F58h

This register specifies the DPIB resume position.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

12.2.383 DMA Position in Buffer Resume (OSD4DPIBR)—Offset 1F60h

This register specifies the DPIB resume position.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

12.2.384 DMA Position in Buffer Resume (OSD5DPIBR)—Offset 1F68h

This register specifies the DPIB resume position.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DMA Position in Buffer Resume (DPIBR):** Indicates the DPIB resume position when DRSMCTL.RSM bit is set. Note that SW must program this register before setting the RUN bit.

12.2.385 Wall Clock Alias (WLCLKA)—Offset 2030h

This register is shadowed from the WALCLK register. Please refer to the corresponding section for register details.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Wall Clock Counter Alias (WALCLK):** This is an alias of the WALCK register. 32-bit counter that is incremented on each link BCLK period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition for this counter is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed, and reports the link 0 wall clock value.

12.2.386 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD0LPIBA)—Offset 2084h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Please refer to the corresponding section for register details.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.387 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD1LPIBA)—Offset 20A4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Please refer to the corresponding section for register details.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.388 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD2LPIBA)—Offset 20C4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Please refer to the corresponding section for register details.

Access Method

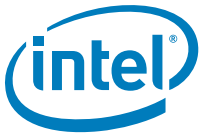
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.389 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD3LPIBA)—Offset 20E4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Please refer to the corresponding section for register details.



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.390 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD4LPIBA)—Offset 2104h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Please refer to the corresponding section for register details.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.391 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD5LPIBA)—Offset 2124h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Please refer to the corresponding section for register details.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.392 Input Stream Descriptor 0 Link Position in Buffer Alias (ISD6LPIBA)—Offset 2144h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Please refer to the corresponding section for register details.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

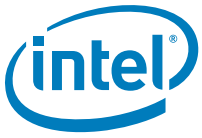
12.2.393 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD0LPIBA)—Offset 2164h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Please refer to the corresponding section for register details.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.394 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD1LPIBA)—Offset 2184h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Please refer to the corresponding section for register details.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.395 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD2LPIBA)—Offset 21A4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Please refer to the corresponding section for register details.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.396 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD3LPIBA)—Offset 21C4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Please refer to the corresponding section for register details.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.397 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD4LPIBA)—Offset 21E4h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Please refer to the corresponding section for register details.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

12.2.398 Input Stream Descriptor 0 Link Position in Buffer Alias (OSD5LPIBA)—Offset 2204h

These registers are shadowed from the (I/O)SD(x/y)LPIB registers. Please refer to the corresponding section for register details.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link Position in Buffer Alias (LPIB):** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds.

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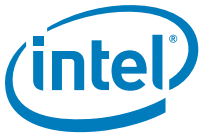


13 Power Management Controller (PMC)

13.1 Registers Summary

Table 13-1. Summary of ACPI CR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Power Management 1 Status and Enable (PM1_STS_EN)—Offset 0h	0h
4h	7h	Power Management 1 Control (PM1_CNT)—Offset 4h	0h
8h	Bh	Power Management 1 Timer (PM1_TMR)—Offset 8h	0h
20h	23h	General Purpose Event 0 Status (GPE0a_STS)—Offset 20h	0h
24h	27h	General Purpose Event 0 Status (GPE0b_STS)—Offset 24h	0h
28h	2Bh	General Purpose Event 0 Status (GPE0c_STS)—Offset 28h	0h
2Ch	2Fh	General Purpose Event 0 Status (GPE0d_STS)—Offset 2Ch	0h
30h	33h	General Purpose Event 0 Enables (GPE0a_EN)—Offset 30h	0h
34h	37h	General Purpose Event 0 Enable (GPE0b_EN)—Offset 34h	0h
38h	3Bh	General Purpose Event 0 Enable (GPE0c_EN)—Offset 38h	0h
3Ch	3Fh	General Purpose Event 0 Enable (GPE0d_EN)—Offset 3Ch	0h
40h	43h	SMI Control and Enable (SMI_EN)—Offset 40h	2h
44h	47h	SMI Status Register (SMI_STS)—Offset 44h	0h
4Ch	4Fh	Device Trap Status (DEVTRAP_STS)—Offset 4Ch	0h
50h	53h	General Purpose Event Control (GPE_CTRL)—Offset 50h	0h
60h	63h	TCO Reload Register (TCO_RLD)—Offset 60h	0h
64h	67h	TCO Timer Status (TCO_STS)—Offset 64h	0h
68h	6Bh	TCO Timer Control (TCO1_CNT)—Offset 68h	0h
70h	73h	TCO Timer Register (TCO_TMR)—Offset 70h	40000h
74h	77h	Advanced Power Management Status (APM_STS)—Offset 74h	0h
78h	7Bh	Advanced Power Management Control Port (APM_CNT)—Offset 78h	0h
7Ch	7Fh	Direct IRQ Enables (DIRECT_IRQ_EN)—Offset 7Ch	0h
200h	203h	"PCI Configuration Control 1 Register(PCICFGCTR1)—Offset 200h"	100h
204h	207h	"PCI Configuration Control 2 Register(PCICFGCTR2)—Offset 204h"	100h
208h	20Bh	"PCI Configuration Control 3 Register(PCICFGCTR3)—Offset 208h"	100h

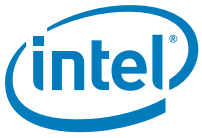
13.1.1 Power Management 1 Status and Enable (PM1_STS_EN)—Offset 0h

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (reserved4):** Reserved.
30	0h RW	**PCI Express Wake Disable (pciexp_wake_dis):** This bit is a scratchbit. The value written can be read back but there is not functionality behind the bit. Windows and Linux have confirmed that they dont use this bit but require it to save and return the written state. Historical reference only: This bit disables the inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register from waking the system. Modification of this bit has no impact on the value of the PCIEXP_WAKE_STS bit reset_type=Resume Well Reset#
29	0h RO	**Reserved**
28:27	0h RO	**Reserved (reserved5):** Reserved.
26	0h RW/V	**RTC Alarm Enable (rtc_en):** This is the RTC alarm enable bit. It works in conjunction with the SCI_EN bit: RTC_EN | SCI_EN | Effect when RTC_STS is set 0 | x | No SMI# or SCI. If system was in S1-S5, no wake even occurs. 1 | 0 | SMI#. If system was in S1-S5, then a wake event occurs before the SMI#. 1 | 1 | SCI. If system was in S1-S5, then a wake event occurs before the SCI. Note: To clarify, If rtc_en is set and and RTC_STS gets set during S0/S0ix and SCI/SMI will be sent depending on the state of SCI_EN and GBL_SMI_EN. In addition to being reset by SRTCRST_B assertion (on the removal of coin battery), PMC also clears this bit due to emergency shutdown events: - Power button override - CPU thermal trip. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
25	0h RO	**Reserved (reserved6):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
24	0h RW/V	**Power Button Enable (pwrbtn_en):** This bit is the power button enable. It works in conjunction with these bits: PWRBTN_EN | SCI_EN | Effect when PWRBTN_STS is set 0 | x | No SMI#, SCI or S0ix wake. 1 | 0 | SMI# and an S0ix wake. 1 | 1 | SCI and an S0ix wake. Note: PWRBTN_EN has no effect on the PWRBTN_STS bit being set by the assertion of the power button. The Power Button is always enabled as an SX Wake event. reset_type=Resume Well Reset#. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
23:22	0h RO	**Reserved (reserved7):** Reserved.
21	0h RW	**Global Enable (gbl_en):** The global enable bit. When both the GBL_EN and the GBL_STS are set, PMC generates an SCI. This field is reset on cold boot, cold reset, and warm reset, and Sx. On architectures that support a host partition reset this bit is reset on PMU_PLTRST_B. pltrst_b is the physical pin on the board. It's driven at the same time as host_prim_rst_b.
20:17	0h RO	**Reserved (reserved8):** Reserved.
16	0h RO	**Reserved**
15	0h RW/1C/V	**Wake Status (wak_sts):** This bit is set when the system is in one of the Sleep states (via the SLP_EN bit) and an enabled Wake event occurs. Upon setting this bit, the PMC will transition the system to the ON state. This bit can only be set by hardware and can only be cleared by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST_B. If a power failure occurs (such as removed batteries) without the SLP_EN bit set, the WAK_STS bit will not be set when the power returns if the AFTER_G3 bit is 0. If the AFTER_G3 bit is 1, then the WAK_STS bit will be set after waking from a power failure. If necessary, the BIOS can clear the WAK_STS bit in this case This is based on discussions with Microsoft. That behavior is not in the ACPI spec. According to ACPI spec 5.0 If the system does not support the S1 sleeping state, the WAK_STS bit can always return zero. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. On older SOCs this bit is reset on RSMRST_B

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**Reserved: PCI Express Wake Status (rsvd_pciexp_wake_sts):** Reference only: This bit is set by hardware to indicate that the system woke due to a PCI Express wakeup event. This event can be caused by the PCI Express WAKE# pins (PMU_WAKE_B, PCI_WAKE1_B, PCI_WAKE2_B, PCI_WAKE3_B) being active, or one or more of the PCI Express ports being in beacon state, or receipt of a PCI Express PME message at root port. This bit should only be set when one of these events causes the system to transition from a non-S0 system power state to the S0 system power state. This bit is set independent of the PCIEXP_WAKE_DIS bit. Software writes a 1 to clear this bit. If one of the WAKE# pins is still active during the write or one or more PCI Express ports is in the beacon state or PME message received indication is not cleared in the root port, then the bit will remain Power Management active (i.e. all inputs to this bit are level sensitive). Note: This bit does not itself cause a wake event or prevent entry to a sleeping state. Thus if the bit is 1 and the system is put into a sleeping state, the system will not automatically wake. reset_type = earlybootside_rst, (global_rst_b when arch available.)
13	0h RO	**Reserved: USB clockless Wake Status (rsvd_usb_clkless_sts):** Reference only: This bit is set by hardware to indicate that the system woke due to change in USB serial lines. This bit is set independent of the USB_CLKLESS_EN bit. Software writes a 1 to clear this bit. This field is reset on Global Reset.
12	0h RO	**Reserved (rsvd):** Reserved.
11	0h RW/1C/V	**Power Button Override (pwrbtnor_sts):** This bit is set any time a Power Button Override Event occurs (i.e. the power button is pressed for at least 4 consecutive seconds- These events cause an unconditional transition to the S5 state. The BIOS or SCI handler clears this bit by writing a 1 to it. This bit is not affected by hard resets via CF9h writes, and is not reset by RSMRST_B. Thus, this bit is preserved through power failures. Note that this bit is still asserted when the global SCI_EN is set to '1' then an SCI will be generated. reset_type=SRTCRST_B (on the removal of coin battery). This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
10	0h RW/1C/V	**RTC Status (rtc_sts):** This bit is set when the RTC generates an alarm (assertion of the IRQ8# signal), and is not affected by any other enable bit. See RTC_EN for the effect when RTC_STS goes active. This bit is only set by hardware and can only be reset by writing a one to this bit position. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. On older SOCs this bit is reset on RSMRST_B.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**Reserved (reserved1):** Reserved.
8	0h RW/1C/V	**Power Button Status (pwrbtn_sts):** This bit is set when the PMU_PWRBTN_B signal is asserted (low), independent of any other enable bit. See PWRBTN_EN for the effect when PWRBTN_STS goes active. PWRBTN_STS is always a wake event. This bit is only set by hardware and can be cleared by software writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST_B. If the PMU_PWRBTN_B signal is held low for more than 4 seconds, the PMC clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, the system transitions to the S5 state, and only PMU_PWRBTN_B is enabled as a wake event. If PWRBTN_STS bit is cleared by software while the PMU_PWRBTN_B pin is still held low, this will not cause the PWRBTN_STS bit to be set. The PMU_PWRBTN_B signal must go inactive and active again to set the PWRBTN_STS bit. Note that the CPU Thermal Trip and the Internal Thermal Sensors' Catastrophic Condition result in behavior matching the Power Button Override, which includes clearing this bit. reset_type=RSMRST_B. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. On older SOCs this bit is reset on RSMRST_B.
7:6	0h RO	**Reserved (reserved2):** Reserved.
5	0h RW/1C/V	**Global Status (gbl_sts):** This bit is set when an SCI is generated due to the BIOS wanting the attention of theSCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit. The SCI handler should then clear this bit by writing a 1 to it. This bit will not cause wake events or SMI#. This bit is not effected by SCI_EN. Note: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place. This field is reset on cold boot, cold reset, warm reset, global reset, and Sx. On architectures that support a host partition reset this bit is reset on PMU_PLTRST_B. pltrst_b is the physical pin on the board. It's driven at the same time as host_prim_rst_b.
4:1	0h RO	**Reserved (rserved3):** Reserved.
0	0h RO	**Reserved: Timer Overflow Status (rsvd_tmrof_sts):** Reference only: This is the timer overflow status bit. This bit gets set anytime bit 22 of the 24 bit timer goes low (bits are counted from 0 to 23). This will occur every 2.3435 seconds. See TMROF_EN for the effect when TMROF_STS goes active. Software clears this bit by writing a 1 to it. This field is reset on cold boot, cold reset, warm reset, global reset, and Sx. On architectures that support a host partition reset this bit is reset on PMU_PLTRST_B. pltrst_b is the physical pin on the board. It's driven at the same time as host_prim_rst_b.

13.1.2 Power Management 1 Control (PM1_CNT)—Offset 4h

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

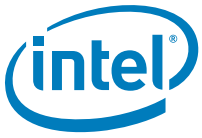
Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved (rsvd):** Reserved.
13	0h WO	**Sleep Enable (slp_en):** This is a write-only bit and reads to it always return a zero. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field.
12:10	0h RW/V	**Sleep Type (slp_typ):** This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. Bits | Mode | Typical Mapping 000 | ON | S0 001 | Reserved 010 | Reserved 011 | Reserved 100 | Reserved 101 | Suspend-To-RAM | S3 110 | Suspend-To-Disk | S4 111 | Soft Off | S5 This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
9:3	0h RO	**Reserved (reserved1):** Reserved.
2	0h WO	**Global RLS (gbl_rls):** This bit is used by the ACPI software to raise an event to the BIOS software. BIOS software has a corresponding enable and status bits to control its ability to receive ACPI events. This bit always reads as 0.
1	0h RW	**BM RLD (bm_rld):** This bit is treated as a scratch pad bit. Reset: cold boot, cold reset, warm reset, and Sx.
0	0h RW	**SCI Enable (sci_en):** Selects the SCI interrupt or the SMI# for various events. When this bit is 1, then the events will generate an SCI interrupt. When this bit is 0, these events will generate an SMI#. Reset: cold boot, cold reset, warm reset, and Sx.

13.1.3 Power Management 1 Timer (PM1_TMR)—Offset 8h

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**



Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (rsvd):** Reserved.
23:0	0h RO	**Reserved**

13.1.4 General Purpose Event 0 Status (GPE0a_STS)—Offset 20h

Note: This register is symmetrical to the General Purpose Event 0a Enable Register. Unless indicated otherwise below, if the corresponding _EN bit is set, then when the STS bit get set, the PMC will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the PMC will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set. This register should not be reset by CF9 write. reset_type=RSMRST_B
This register is reset on RSM_RST_N de-assertion. This register is not reset on cold reset, warm reset, and Sx.

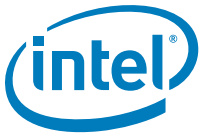
Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

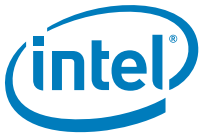
Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (rsvd31):** Reserved.
17	0h RW/1C/V	**SATA PME Status (sata_pme_sts):** This bit will be set to 1 by the PMC when SATA asserts its PME wire signal. Additionally, if the SATA_PME_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the SATA _PME_STS bit will generate an SCI (or SMI# if SCI_EN is not set but GLB_SMI_EN is). This bit is cleared by a software write of '1'. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/1C/V	**SMBUS Wake Status (smb_wak_sts):** This bit is set to 1 by the hardware to indicate that the wake event was caused by the SoC SMBus logic (SMBALERT# signal going active). Notes: 1. The SMBus controller will independently cause an SMI message so this bit does not need to do so (unlike the other bits in this register). 2. This bit is set by the SMBus slave command 01h (Wake/SMI#) even when the system is in the S0 state. Therefore, to avoid an instant wake on subsequent transitions to sleep states, software must clear this bit after each reception of the Wake/SMI# command or just prior to entering the sleep state. Note: This is a TCO Slave Write initiated function and not supported in the SoC. 3. The SMBALERT_STS bit (D31:F3:I/O Offset 00h:bit 5) should be cleared . This is not applicable to the SoC where the SMBUS alert wire is a no-connect. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
15	0h RW/1C/V	**GPIO Tier1 SCI Status (gpio_tier1_sci_sts):** This bit is a logical OR of sci_wake wires from tier 1 GPIO's. Additionally, if the GPIO_TIER1_SCI_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the GPIO_TIER1_SCI_STS bit will generate an SCI (or SMI# if SCI_EN is not set but GLB_SMI_EN is). This bit is cleared by a software write of '1'. If the GPIO_TIER1_SCI_EN is set this bit is a SX and S0ix wake source. There may be additional PMU wake mask bits for SX and SOix wakes. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
14	0h RW/1C/V	**AVS PME Status (avs_pme_sts):** This bit will be set to 1 by the PMC when AVS asserts its PME wire signal. Additionally, if the AVS_PME_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the AVS_PME_STS bit will generate an SCI (or SMI# if SCI_EN is not set but GLB_SMI_EN is). This bit is cleared by a software write of '1'. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
13	0h RW/1C/V	**USB XHCI PME Status (xhci_pme_sts):** This bit will be set to 1 by the PMC when USB XHCI asserts its PME wire signal. Additionally, if the XHCI_PME_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the XHCI_PME_STS bit will generate an SCI (or SMI# if SCI_EN is not set but GLB_SMI_EN is). This bit is cleared by a software write of '1'. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.



Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C/V	**USB XDCI PME Status (xdci_pme_sts):** This bit will be set to 1 by the PMC when USB XDCI asserts its PME wire signal. Additionally, if the XDCI_PME_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the XDCI_PME_STS bit will generate an SCI (or SMI# if SCI_EN is not set but GLB_SMI_EN is). This bit is cleared by a software write of '1'. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
11	0h RW/1C/V	**CSE PME Message Status (cse_pme_sts):** This bit will be set to 1 by the PMC when CSE sends Assert_PME message to PMC. Additionally, if the CSE_PME_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the CSE_PME_STS bit will generate an SCI (or SMI# if SCI_EN is not set but GLB_SMI_EN is). This bit is cleared by a software write of '1'. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
10	0h RW/1C/V	**Battery Low Status (batlow_sts):** This bit will be set to 1 by hardware when the PMU_BATLOW_B signal goes low. Software clears the bit by writing a 1 to the bit position. In Desktop Mode, this bit will be treated as Reserved. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
9	0h RW/1C/V	**PCIE GPE Message Status (pcie_gpe_sts):** This bit will be set to 1 by hardware to indicate that the PMC received an Assert_GPE message from one or more of the PCI-Express Ports. The GPE messages represents a PME event message from one or more of the PCI-Express Ports. Software attempts to clear this bit by writing a 1 to this bit position. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the level triggered SCI will remain active. Note that a race condition exists where the PCI Express device sends another PME message because the PCI Express device was not serviced within the time when it must resend the message. This may result in a spurious interrupt, and this is comprehended and approved by the PCI Express specification. The window for this race condition is approximately 95-105 milliseconds. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
8	0h RW/1C/V	**PCI Express Wake3 Status (pcie_wake3_sts):** This bit is set by hardware to indicate that the pci_wake3_b pin was asserted. Software writes a 1 to clear this bit. If pci_wake3_b pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C/V	**PCI Express Wake2 Status (pcie_wake2_sts):** This bit is set by hardware to indicate that the pci_wake2_b pin was asserted. Software writes a 1 to clear this bit. If pci_wake2_b pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
6	0h RW/1C/V	**PCI Express Wake1 Status (pcie_wake1_sts):** This bit is set by hardware to indicate that the pci_wake1_b pin was asserted. Software writes a 1 to clear this bit. If pci_wake1_b pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
5	0h RO	**Reserved (rsvd5):** Reserved.
4	0h RW/1C/V	**PUNIT SCI status (punit_sci_sts):** This bit will be set if the Power Management Unit requests SCI or and SMI if PUNIT_SCI_EN and !SCI_EN and GBL_SMI_EN is set. This bit is cleared by writing a 1 to this bit position. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
3	0h RW/1C/V	**PCI Express Wake0 Status (pcie_wake0_sts):** This bit is set by hardware to indicate that the pci_wake0_b pin was asserted. Software writes a 1 to clear this bit. If pci_wake0_b pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
2	0h RW/1C/V	**Software GPE Status (swgpe_sts):** The SWGPE_CTRL bit (bit 1 of GPE_CTRL reg) acts as a level input to this bit. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
1	0h RO	**Reserved (rsvd):** Reserved.
0	0h RW/1C/V	**PCIE SCI Message Status (pcie_sci_sts):** This bit will be set to 1 by the PMC when Pcie sends Assert_SCI message to PMC. Additionally, if the pcie_sci_en and sci_en bits are set, and the system is in an S0 state, then the setting of the pcie_sci_sts bit will generate an SCI (or SMI# if sci_en is not set but GLB_SMI_EN is). This bit is cleared by a software write of '1'. Note: TAG field of Assert_SCI message is ignored. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.



13.1.5 General Purpose Event 0 Status (GPE0b_STS)—Offset 24h

Note: This register is symmetrical to the General Purpose Event 0b Enable Register. Reads/writes to this register will result in the transaction being forwarded to the corresponding GPIO community based on the GPIO_GPE_CFG.gpe0_dw1 register configuration.

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**General Purpose Event 0 Status Dword 1 (gpe0b_sts):** Shadow of the general purpose event status from the corresponding GPIO community specified in GPIO_GPE_CFG.gpe0_dw1.

13.1.6 General Purpose Event 0 Status (GPE0c_STS)—Offset 28h

Note: This register is symmetrical to the General Purpose Event 0c Enable Register. Reads/writes to this register will result in the transaction being forwarded to the corresponding GPIO community based on the GPIO_GPE_CFG.gpe0_dw2 register configuration.

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**General Purpose Event 0 Status Dword 2 (gpe0c_sts):** Shadow of the general purpose event status from the corresponding GPIO community specified in GPIO_GPE_CFG.gpe0_dw2.

13.1.7 General Purpose Event 0 Status (GPE0d_STS)—Offset 2Ch

Note: This register is symmetrical to the General Purpose Event 0d Enable Register. Reads/writes to this register will result in the transaction being forwarded to the corresponding GPIO community based on the GPIO_GPE_CFG.gpe0_dw3 register configuration.

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**General Purpose Event 0 Status Dword 3 (gpe0d_sts):** Shadow of the general purpose event status from the corresponding GPIO community specified in GPIO_GPE_CFG.gpe0_dw3.

13.1.8 General Purpose Event 0 Enables (GPE0a_EN)—Offset 30h

Note: This register is symmetrical to the General Purpose Event 0a Status Register.reset_type=Resume Well Reset#.
This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.

Access Method

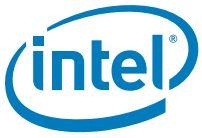
Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (rsvd31):** Reserved.
17	0h RW	**SATA PME Enable (sata_pme_en):** Enables the setting of the SATA_PME_STS bit to generate a wake event and/or an SCI or SMI#. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
16	0h RW/V	**SMBUS WAKE Enable (smb_wak_en):** Enables the setting of the SMB_WAK_STS bit to generate a wake event BUT NOT an SCI or SMI#. SMB_WAK is a special case in that it cannot cause an SCI or SMI. On platforms that support an on-die RTC well, this field is reset on SRTCRST_B, (on the removal of coin battery) Additionally on those platforms where this affects SX wake events the PMC must clear this field on powerbutton and CPU thermal trip. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/V	**GPIO Tier1 SCI Enable (gpio_tier1_sci_en):** Enables the setting of the GPIO_TIER1_SCI_STS bit to generate a wake event and/or an SCI or SMI#. On platforms that support an on-die RTC well, this field is reset on SRTCRST_B (on the removal of coin battery). Additionally on those platforms where this affects SX wake events the PMC must clear this field on powerbutton and CPU thermal trip. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
14	0h RW/V	**AVS PME Enable (avs_pme_en):** Enables the setting of the AVS PME STS bit to generate a wake event and/or an SCI or SMI#. On platforms that support an on-die RTC well, this field is reset on SRTCRST_B (on the removal of coin battery). Additionally on those platforms where this affects SX wake events the PMC must clear this field on powerbutton and CPU thermal trip. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
13	0h RW/V	**USB XHCI PME Enable (xhci_pme_en):** Enables the setting of the XHCI_PME_STS bit to generate a wake event and/or an SCI or SMI#. reset_type = SRTCRST_B - (on the removal of coin battery), Power button override, or CPU thermal trip, when arch available and relevant. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
12	0h RW/V	**USB XDCI PME Enable (xdci_pme_en):** Enables the setting of the XDCI_PME_STS bit to generate a wake event and/or an SCI or SMI#. reset_type = SRTCRST_B (on the removal of coin battery), Power button override, or CPU thermal trip, when arch available and relevant. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
11	0h RW	**CSE PME Message Enable (cse_pme_en):** Enables the setting of the CSE_PME_EN bit to generate a wake event and/or an SCI or SMI#.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/V	**Battery Low Enable (batlow_en):** This bit enables the PMU_BATLOW_B signal to cause an SMI# or SCI (depending on the SCI_EN bit) when it goes low.This bit does not prevent the PMU_BATLOW_B signal from inhibiting the wake event. On desktop platforms this pin should be tied high to ensure proper functionality. In addition to being reset by SRTCRST_B assertion, the PMC also clears this bit due to certain events: - Power button override. - CPU thermal trip reset_type=SRTCRST_B (on the removal of coin battery). This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
9	0h RW	**PCIE GPE Message Enable (pcie_gpe_en):** Enables the PMC to cause an SCI or SMI when the PCIE_GPE_STS bit is set. This is used to allow the PCI Express ports to cause an SCI or SMI due to pmc receiving an Assert_GPE from PCIE0 or PCIE1. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
8	0h RW/V	**PCI Express Wake3 Enable (pcie_wake3_en):** This bit, when set to 1, enables the PCIE_WAKE3_STS to to cause an SCI. On platforms that support an on-die RTC well, this field is reset on SRTCRST_B, (on the removal of coin battery). Additionally on those platforms where this affects SX wake events the PMC must clear this field on powerbutton and CPU thermal trip. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
7	0h RW/V	**PCI Express Wake2 Enable (pcie_wake2_en):** This bit, when set to 1, enables the PCIE_WAKE2_STS to to cause an SCI. On platforms that support an on-die RTC well, this field is reset on SRTCRST_B, (on the removal of coin battery). Additionally on those platforms where this affects SX wake events the PMC must clear this field on powerbutton and CPU thermal trip. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
6	0h RW/V	**PCI Express Wake1 Enable (pcie_wake1_en):** This bit, when set to 1, enables the PCIE_WAKE1_STS to to cause an SCI. On platforms that support an on-die RTC well, this field is reset on SRTCRST_B, (on the removal of coin battery). Additionally on those platforms where this affects SX wake events the PMC must clear this field on powerbutton and CPU thermal trip. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
5	0h RO	**Reserved (rsvd5):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**PUnit SCI Enable (punit_sci_en):** This bit enables the corresponding PUNIT_SCI_STS bit being set to cause an SCI and/or wake event.
3	0h RW/V	**PCI Express Wake0 Enable (pcie_wake0_en):** This bit, when set to 1, enables the PCIE_WAKE0_STS to to cause an SCI. On platforms that support an on-die RTC well, this field is reset on SRTCRST_B, (on the removal of coin battery). Additionally on those platforms where this affects SX wake events the PMC must clear this field on powerbutton and CPU thermal trip. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
2	0h RW	**Software GPE Enable (swgpe_en):** This bit, when set to 1, enables the SW GPE function. If SWGPE_CTRL is written to a 1, hardware will set SWGPE_STS (acts as a level input). If SWGPE_STS, SWGPE_EN, and SCI_EN are all 1's, an SCI will be generated. If SWGPE_STS = 1, SWGPE_EN = 1, SCI_EN = 0, and GBL_SMI_EN = 1 then an SMI# will be generated.
1	0h RO	**Reserved (rsvd):** Reserved.
0	0h RW	**PCIE SCI Message Enable (pcie_sci_en):** Enables the setting of the PCIE_SCI_EN bit to generate a wake event and/or an SCI or SMI#. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.

13.1.9 General Purpose Event 0 Enable (GPE0b_EN)—Offset 34h

Note: This register is symmetrical to the General Purpose Event 0b Status Register. Reads/writes to this register will result in the transaction being forwarded to the corresponding GPIO community based on the GPIO_GPE_CFG.gpe0_dw1 register configuration.

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**General Purpose Event 0 Enable Dword 1 (gpe0b_en):** Shadow of the general purpose event enable from the corresponding GPIO community specified in GPIO_GPE_CFG.gpe0_dw1.

13.1.10 General Purpose Event 0 Enable (GPE0c_EN)—Offset 38h

Note: This register is symmetrical to the General Purpose Event 0c Status Register. Reads/writes to this register will result in the transaction being forwarded to the corresponding GPIO community based on the GPIO_GPE_CFG.gpe0_dw2 register configuration.

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**General Purpose Event 0 Enable Dword 2 (gpe0c_en):** Shadow of the general purpose event enable from the corresponding GPIO community specified in GPIO_GPE_CFG.gpe0_dw2.

13.1.11 General Purpose Event 0 Enable (GPE0d_EN)—Offset 3Ch

Note: This register is symmetrical to the General Purpose Event 0d Status Register. Reads/writes to this register will result in the transaction being forwarded to the corresponding GPIO community based on the GPIO_GPE_CFG.gpe0_dw3 register configuration.

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

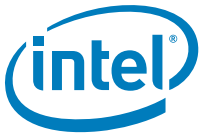
Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**General Purpose Event 0 Enable Dword 3 (gpe0d_en):** Shadow of the general purpose event enable from the corresponding GPIO community specified in GPIO_GPE_CFG.gpe0_dw3.

13.1.12 SMI Control and Enable (SMI_EN)—Offset 40h

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 2h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (rsvd):** Reserved.
27	0h RW	**OCP Fabric and CSE SMI Enable (ocp_smi_en):** Enables SMI logic to cause SMI if gbl_smi_en is set. This enables SMI logic for two sources: the PMC OCP fabric (via the PMC IOSF2OCP bridge) and CSE. This is reset on cold boot, cold reset, warm reset, and Sx.
26	0h RW	**SPI SMI Enable (spi_smi_en):** Enables SMI logic to cause SMI if gbl_smi_en is set.
25	0h RW	**SPI SSMI Enable (spi_ssmi_en):** Enables SMI logic to cause Sync SMI if gbl_smi_en is set.
24:22	0h RO	**Reserved (reserved24_22):** Reserved.
21	0h RW	**SCC2 SMI Enable (scc2_smi_en):** Enables SMI logic to cause SMI if gbl_smi_en is set.
20	0h RW	**PCIE SMI Enable (pcie_smi_en):** Enables SMI logic to cause SMI if gbl_smi_en is set. This is reset on cold boot, cold reset, warm reset, and Sx.
19	0h RW	**SCS SMI Enable (scs_smi_en):** Enables SMI logic to cause SMI if gbl_smi_en is set.
18	0h RW	**Host SMBUS SMI Enable (host_smbus_smi_en):** Enables SMI logic to cause SMI if gbl_smi_en is set.
17	0h RW	**XHCI SMI Enable (xhci_smi_en):** Enables SMI logic to cause SMI if gbl_smi_en is set.
16	0h RW	**SMBUS SMI Enable (smbus_smi_en):** Enables SMI logic to cause SMI if gbl_smi_en is set.
15	0h RW	**SERIRQ SMI Enable (serirq_smi_en):** Enables SMI logic to cause Sync SMI if gbl_smi_en is set.
14	0h RW	**Periodic Enable (periodic_en):** Setting this bit will cause the PMC to generate an SMI# when the PERIODIC_STS bit is set in the SMI_STS register.
13	0h RW/L	**TCO Enable (tco_en):** When set, enables the TCO logic to generate SMI#. When cleared, disables TCO logic generating an SMI#. Note: This bit cannot be written once the TCO_LOCK bit is set. This prevents unauthorized software from disabling the generation of TCO-based SMIs.
12	0h RW	**MCSMI Enable (mcsmi_en):** Software sets this bit to 1 to enables SoC to trap access to the microcontroller range (62h or 66h). A 'trapped' cycles will be claimed by SoC, but not forwarded to LPC. An SMI# will also be generated.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1S	**GPIO Unlock SSMI EN (gpio_unlock_ssmi_en):** Enables SSMI logic to cause SSMI if gbl_smi_en is set and parallel STS bit is set. Once written to '1', this bit can only be cleared by the reset condition for this bit. Reset on cold boot, cold reset, warm reset, and Sx. On architectures that support partitioned resets this bit is reset on the host reset (host_prim_rst_b).
10	0h RW	**GPIO SMI Enable (gpio_smi_en):** Enables SMI logic to cause SMI if gbl_smi_en is set.
9:8	0h RO	**Reserved (reserved5):** Reserved.
7	0h WO	**BIOS RLS (bios_rls):** Enables the generation of an SCI interrupt for ACPI software when a one is written to this bit position by BIOS software. This bit always reads a zero. Note: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place.
6	0h RW	**Software SMI Timer Enable (swsmi_tmr_en):** Software sets this bit to a 1 to start the Software SMI# Timer. When the timer expires (depending on the SWSMI_RATE_SEL bits), it will generate an SMI# and set the SWSMI_TMR_STS bit. The SWSMI_TMR_EN bit will remain at 1 until software sets it back to 0. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. The default for this bit is 0.
5	0h RW	**APMC Enable (apmc_en):** If set, this enables writes to the APM register to cause an SMI#.
4	0h RW	**SMI On Sleep Enable (smi_on_slp_en):** If this bit is set, the PMC will generate an SMI# when a write access attempts to set the SLP_EN bit (in the PM1_CNT register). Furthermore, the PMC will not put the system to a sleep state. This allows the SMI# handler work around chip-level bugs. It is expected that the SMI# handler will turn off the SMI_ON_SLP_EN bit before actually setting the SLP_EN bit.
3	0h RW	**Legacy USB Enable (legacy_usb_en):** Enables SMI logic to cause SMI if gbl_smi_en is set.
2	0h RW	**BIOS Enable (bios_en):** Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit. Note that if the BIOS_STS bit, which gets set when software writes a 1 to GBL_RLS bit, is already a 1 at the time that BIOS_EN becomes 1, an SMI# will be generated when BIOS_EN gets set.
1	1h RW/1S/V	**End of SMI (eos):** SMI handler sets this bit when it finishes handling the SMI. Setting this bit will force the PMC internal SMI request to zero for 1 clock.Thus if the internal SMI request is still asserted due to new SMI trigger and SMI_ACK was received for the previous SMI, a new SMI will be sent. Hardware clears this bit, SW/FW sets.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Global SMI Enable (gbl_smi_en):** When set, this bit enables the generation of SMIs in the system upon any enabled SMI event. If this bit is not set, no SMI# will be generated.Note: When the SMI_LOCK bit is set, this bit cannot be changed. On architectures that support a host partition reset this bit is reset on PMU_PLTRST_B. pltrst_b is the physical pin on the board. It's driven at the same time as host_prim_rst_b. The SoC does not have a host partition reset.

13.1.13 SMI Status Register (SMI_STS)—Offset 44h

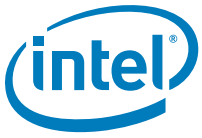
Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (rsvd):** Reserved.
27	0h RW/1C/V	**PMC OCP Fabric and CSE SMI Status (ocp_smi_sts):** This bit will be set if PMC OCP fabric (via PMC IOSF2OCP bridge) or CSE request an SMI#. Writing a '1' to this bit position clears this bit to '0'. This bit is overloaded to include CSE SMI in addition to PMC OCP fabric SMI in order to implement CSE SMI support with minimal hardware impact, due to the late addition of this support. Because this status bit is overloaded for multiple sources, the SMI handler must disambiguate between OCP and CSE sources. This can be done by: (1) Read ocp_smi_sts, store the result and clear ocp_smi_sts. (2) Read PMC OCP fabric and CSE status registers to determine if one or both of the sources requested an SMI. This is reset on cold boot, cold reset, warm reset, and Sx.
26	0h RW/1C/V	**SPI SMI Status (spi_smi_sts):** This bit will be set when the SPI logic is requesting an SMI#.
25	0h RW/1C/V	**SPI SSMI Status (spi_ssmi_sts):** This bit will be set when the SPI logic is requesting an Sync SMI#. The FW controlled ACPI_CTL.SPI_SSMI_CTRL bit acts as a rising edge input to this bit. SSMI is a FW flow in the SoC. Host clears this bit.
24:22	0h RO	**Reserved (reserved2):** Reserved.
21	0h RW/1C/V	**SCC2 SMI Status (scc2_smi_sts):** This bit will be set if SCC2 unit is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW/1C/V	**PCIE_SMI Status (pcie_smi_sts):** PCIE SMI event occurred. Set with Assert_SMI from PCIE0 or PCIE1. Writing a '1' to this bit position clears this bit to '0' SoC does not support Hot Plug Event. This is reset on cold boot, cold reset, warm reset, and Sx.
19	0h RW/1C/V	**SCS SMI Status (scs_smi_sts):** This bit will be set if SCS unit is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'.
18	0h RW/1C/V	**Host SMBUS SMI Status (host_smbus_smi_sts):** The PMC sets this bit to 1 to indicate that the SMI# was triggered when Host initiated SMBUS transaction encounters failure such as device error or bus collision or upon the completion of a valid transaction on the bus but with SMBUS SIP SMB_SMI_EN = 1. Further clarification of the cause of this SMI should be queried from SMBUS IPs HOST STATUS register. PMC sets this bit on receiving an SMI message with tag 0x1.
17	0h RW/1C/V	**USB XHCI SMI Status (xhci_smi_sts):** This bit will be set when the USB logic is requesting an SMI#.
16	0h RW/1C/V	**SMBUS SMI Status (smbus_smi_sts):** The PMC sets this bit to 1 to indicate that the SMI# was caused by: 1. The SMBUS Slave receiving a message that an SMI# should be caused. This implies that the PMC received an SMI message from SMBUS with tag 0x3. Note: This is a TCO Slave Write initiated function and not supported in the SoC. 2. The SMBALERT# signal goes active and the SMB_SMI_EN bit is set and the SMBALERT_DIS bit is cleared. This implies that the PMC received an SMI message from SMBUS with tag 0x2. 3. The SMBUS Slave receiving a HOST_NOTIFY message and the HOST_NOTIFY_INTREN and the SMB_SMI_EN bits are set. Where HOST_NOTIFY_INTREN is available via the SMBUS IP not in the PMC. This implies that the PMC received an SMI message from SMBUS with tag 0x2. 4. The SMBUS Slave receiving a SMI in S0 message. This implies that the PMC received an SMI message from SMBUS with tag 0x2. Note: This is a TCO Slave Write initiated function and not supported in the SoC This bit is sticky. It is cleared by writing a 1 to this bit position. Note that this bit is set from the 64 KHz clock domain used by the SMBUS. Software must wait at least 15.63 microseconds
15	0h RW/1C/V	**SERIRQ SMI Status (serirq_smi_sts):** 1: Indicates the SMI# was caused by the SERIRQ decoder. This implies that the PMC received an SMI message from LPC. 0: SMI# not caused by SERIRQ decoder. This bit will remain 1 until the software writes a 1 to this bit.
14	0h RW/1C/V	**Periodic Status (periodic_sts):** This bit will be set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit is also set, the PMC will generate an SMI#. This bit is cleared by writing a 1 to this bit position.



Bit Range	Default & Access	Field Name (ID): Description
13	0h RW/1C/V	**TCO Status (tco_sts):** Indicates SMI was caused by the TCO logic. This bit is cleared by writing a 1 to this bit position, Causes would be: 1. Century rollover from SMBUS. Not applicable in the SoC. This functionality comes from the RTC. 2. TCO_TMR 1st & 2nd expiration in PMC. 3. OS writes to TCO_DAT_IN register. Sent to PMC as a SMI message with tag 0x0 from SMBUS. 4. NMI occurred and mapped to SMI. Sent to PMC as a SMI message with not tag from ITSS. 5. INTRUDER# signal goes active. Wire to the PMC from SMBUS. 6. Illegal attempt to write to BIOS located in the FWH accessed over LPC. Sent to PMC as a SMI msg with tag 0x0 from SMBUS. 7. Changes of BC.WPD (Write Protect Disable) bit from 0 to 1. Sent to PMC as an SyncSMI message with tag 0x1 from LPC.
12	0h RW/1C/V	**Microcontroller SMI Status (mcsmi_sts):** This bit is set if there is an access to the power management microcontroller range (62h or 66h). If this bit is set, and the MCSMI_EN bit is also set, the SoC will generate an SMI#. This bit is set by hardware and cleared by software writing a 1 to its bit position. This bit will be set when the LPC logic is requesting an Sync SMI# with tag 0x0. The FW controlled ACPI_CTL.MCSMI_CTRL bit acts as a rising edge input to this bit. SSMI is a FW flow in the SoC.
11	0h RW/1C/V	**GPIO Unlock SSMI STS (gpio_unlock_ssmi_sts):** This bit will be set if the GIO registers lockdown logic is requested an SSMI. Writing a '1' to this bit position clears this bit to '0'.
10	0h RW/1C/V	**GPIO SMI STS (gpio_smi_sts):** This bit will be a 1 if any GPIO that is enabled to trigger SMI is asserted. GPIOs that are not routed to cause an SMI will have no effect on this bit.
9	0h RO	**Reserved**
8	0h RO	**Reserved**
7	0h RO	**Reserved (reserved4):** Reserved. No corresponding status bit to BIOS_RLS.
6	0h RW/1C/V	**Software SMI Timer Status (swsmi_tmr_sts):** This bit will be set to 1 by the hardware when the Software SMI# Timer expires. This bit will remain 1 until the software writes a 1 to this bit.
5	0h RW/1C/V	**Advanced Power Management Status (apm_sts):** SMI# was generated by a write access to the APM control register and if the APMC_EN bit is set. This bit is cleared by writing a one to its bit position. Reset on cold boot, cold reset, warm reset, and Sx. On architectures that support a partitioned resets this bit is reset on the host reset (host_prim_rst_b).
4	0h RW/1C/V	**SMI ON SLP EN Status (smi_on_slp_en_sts):** This bit will be set by the PMC when a write access attempts to set the SLP_EN bit. This bit is cleared by writing a 1 to this bit position.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**Legacy USB Status (legacy_usb_sts):** Logical OR of each of the SMI status bits in the USB Legacy Keybd Register in the LPC IP ANDed with the corresponding enable bits in the LPC IP. SMI_EN.LEGACY_USB_EN must be set for this bit to cuase and SMI. This bit is cleared by writing a 1 to this bit position. This bit will be set when the LPC logic is requesting an Sync SMI# with tag 0x2. The FW controlled ACPI_CTL.LEGACY_USB_CTRL bit acts as a rising edge input to this bit. SSMI is a FW flow in the SoC.
2	0h RW/1C/V	**BIOS Status (bios_sts):** This bit gets set by hardware when a 1 is written by software to the GBL_RLS bit. When both BIOS_EN and the BIOS_STS bit are set, an SMI# will be generated. The BIOS_STS bit is cleared when software writes a 1 to this bit position.
1:0	0h RO	**Reserved (reserved7):** Reserved.

13.1.14 Device Trap Status (DEVTRAP_STS)—Offset 4Ch

Each bit indicates if an access has occurred to the corresponding device's trap range or for bits 6:9 if the corresponding PCI interrupt is active. Write 1 to the same bit position to clear it. This register is used by APM power management software to see if there has been system activity. The periodic SMI# timer indicates if it is the right time to read the DEVTRAP_STS register.

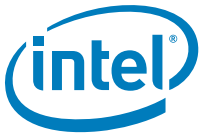
On architectures that support a host partition reset this register is reset on host_prim_rst_b. The SoC does not have a host partition reset.
This is reset on cold boot, cold reset, warm reset, and Sx.

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (rsvd16):** Reserved.
15:13	0h RO	**Reserved (rsvd15):** Reserved.
12	0h RW/1C/V	**Device Trap Status Bit 12 (d12_trp_sts):** KBC (60/64h)
11:6	0h RO	**Reserved (rsvd11):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C/V	**Device Trap Status Bit 5 (d5_trp_sts):** This will be set if any of the following are accessed (as determined by the I/O ranges in the LPC decoder (even if the LPC forwarding is not enabled): SP1, SP2, PP, FDC.
4:0	0h RO	**Reserved (rsvd4):** Reserved.

13.1.15 General Purpose Event Control (GPE_CTRL)—Offset 50h

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (rsvd):** Reserved.
17	0h RW	**Software General Purpose Event Control (swgpe_ctrl):** This bit allows software to control the assertion of SWGPE_STS bit. This bit is used by hardware as the level input signal for the SWGPE_STS bit in the GPE0a_STS register. When SWGPE_CTRL is 1, SWGPE_STS will be set to 1, and writes to SWGPE_STS with a value of 1 to clear SWGPE_STS will result in SWGPE_STS being set back to 1 by hardware. When SWGPE_CTRL is 0, writes to SWGPE_STS with a value of 1 will clear SWGPE_STS to 0. This is reset on cold boot, cold reset, warm reset, and Sx.
16:0	0h RO	**Reserved (reserved1):** Reserved.

13.1.16 TCO Reload Register (TCO_RLD)—Offset 60h

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved (rsvd):** Reserved.
9:0	0h RO/V	**TCO Timer Value (tco_val):** Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout.

13.1.17 TCO Timer Status (TCO_STS)—Offset 64h

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (reserved2):** Reserved.
17	0h RW/1C/V	**Second Timeout Status (second_to_sts):** PMC sets this bit to 1 to indicate that the TIMEOUT bit had been (or is currently) set and a second timeout occurred before the TCO_RLD register was written. If this bit is set and the NO_REBOOT config bit is 0, then the PMC will reboot the system after the second timeout. The reboot is done by interrupting the Arc and starting a reset flow based on the OS_POLICY. This bit is only cleared by writing a 1 to this bit or by a reset. On some prior platforms, this field is reset on RSMRST_B, a reset signal based on a RSMRST# pin that indicates the suspend/ resume voltages are stable. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
16:4	0h RO	**Reserved (reserved1):** Reserved.
3	0h RW/1C/V	**TCO Timeout (tco_timeout):** Bit set to 1 by PMC to indicate that the SMI was caused by TCO timer reaching 0. Reset: On cold boot, cold reset, warm reset, and Sx.
2:0	0h RO	**Reserved (rsvd):** Reserved.

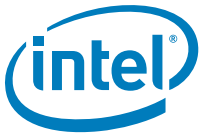
13.1.18 TCO Timer Control (TCO1_CNT)—Offset 68h

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (rsvd):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**OS Policy (os_policy):** OS-based software writes to these bits to select the policy that the BIOS will use after the platform resets due the WDT. The following convention is recommended for the BIOS and OS: 00: Boot normally 01: Shut down 10: Don't load OS. Hold in pre-boot state and use LAN to determine next step. 11: Reserved Reset on RSM_RST_N de-assertion only.
19:13	0h RO	**Reserved (reserved2):** Reserved.
12	0h RW/L	**TCO Lock (tco_lock):** When set to 1, this bit prevents writes from changing the TCO_EN bit (in offset 30h of Power Management I/O space). Once this bit is set to 1, it cannot be cleared by software writing a 0 to this bit location. Reset is required to change this bit from 1 to 0. This bit defaults to 0. On some prior platforms, this field is reset on cold reset. This is reset on cold boot, cold reset, warm reset, and Sx.
11	0h RW	**TCO Timer Halt (tco_tmr_halt):** 1: The TCO timer will halt. It will not count, and thus cannot reach a value that would cause an SMI# or to cause the SECOND_TO_STS bit to be set. This will also prevent rebooting. 0: The TCO timer is enabled to count. This is the default. This is reset on cold boot, cold reset, warm reset, and Sx.
10:0	0h RO	**Reserved (reserved1):** Reserved.

13.1.19 TCO Timer Register (TCO_TMR)—Offset 70h

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 40000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (reserved1):** Reserved.
25:16	4h RW	**TCO Timer Reload Value (tco_trld_val):** Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and thus allows timeouts ranging from 1.2 second to 613.8 seconds. Note: The timer has an error of +/- 1 tick (0.6s). The TCO Timer will only count down in the S0 and S0IX state.
15:0	0h RO	**Reserved (rsvd):** Reserved.

13.1.20 Advanced Power Management Status (APM_STS)—Offset 74h

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Advanced Power Management Status Port (apm_sts):** Used to pass data between the OS and the SMI handler. Basically, this is a scratch pad register and is not effected by any other register or function (other reset). Writes can come through ACPI register writes or from IO Port write to port 0xB3. On architectures that support a host partition reset this bit is reset on a host partition reset. This is reset on cold boot, cold reset, warm reset, and Sx.
23:0	0h RO	**Reserved (rsvd):** Reserved.

13.1.21 Advanced Power Management Control Port (APM_CNT)—Offset 78h

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (reserved0):** Reserved.
23:16	0h RW	**Advanced Power Management Control Port (apm_cnt):** Used to pass an APM command between the OS and the SMI handler. Writes to this bit field not only store data in the APMC register, but also generates an SMI# when the APMC_EN bit is set. Writes can come through ACPI register writes or from IO Port write to port 0xB2. On architectures that support a host partition reset this bit is reset on a host partition reset. This is reset on cold boot, cold reset, warm reset, and Sx.
15:0	0h RO	**Reserved (reserved1):** Reserved.

13.1.22 Direct IRQ Enables (DIRECT_IRQ_EN)—Offset 7Ch

This register is reset on cold boot, cold reset, warm reset, and Sx.

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved (reserved0):** Reserved.
9	0h RW	**Direct IRQ Enable for PMIC (pmic_en):** This bit enables generation of De/AssertIRQn message based on SVID's interrupt signal (which reflects PMIC's alert signal). The resulting De/AssertIRQn will have an IRQ vector, as programmed in the corresponding GCR.IRQ_SEL_0/1/2 field.
8	0h RW	**Direct IRQ Enable for XHCI (xhci_en):** This bit enables wake from S0ix and generation of De/AssertIRQn message based on XHCI's PME & D0i3 signals. The resulting De/AssertIRQn will have vector. as programmed in the corresponding GCR.IRQ_SEL_0/1 field.
7	0h RW	**Direct IRQ Enable for XDCI (xdci_en):** This bit enables wake from S0ix and generation of De/AssertIRQn message based on XDCI's PME & D0i3 signals. The resulting De/AssertIRQn will have vector. as programmed in the corresponding GCR.IRQ_SEL_0/1 field.
6	0h RW	**Reserved**
5	0h RW	**Direct IRQ Enable for SCC (sdcard_cd_en):** This bit enables wake from S0ix and generation of De/AssertIRQn message based on SCC's PME & D0i3 signals. The resulting De/AssertIRQn will have vector. as programmed in the corresponding GCR.IRQ_SEL_0/1 field.
4	0h RW	**Direct IRQ Enable for SCC (sdcard_d1_en):** This bit enables wake from S0ix and generation of De/AssertIRQn message based on SCC's PME & D0i3 signals. The resulting De/AssertIRQn will have vector. as programmed in the corresponding GCR.IRQ_SEL_0/1 field. Usage of this bit is not supported on the SoC because of the capabilities in the SCC IP.
3	0h RW	**Direct IRQ Enable for UART[3] (uart3_en):** This bit enables wake from S0ix and generation of De/AssertIRQn message based on UART's PME & D0i3 signals. The resulting De/AssertIRQn will have vector. as programmed in the corresponding GCR.IRQ_SEL_0/1 field.
2	0h RW	**Direct IRQ Enable for UART[2] (uart2_en):** This bit enables wake from S0ix and generation of De/AssertIRQn message based on UART's PME & D0i3 signals. The resulting De/AssertIRQn will have vector. as programmed in the corresponding GCR.IRQ_SEL_0/1 field.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Direct IRQ Enable for UART[1] (uart1_en):** This bit enables wake from S0ix and generation of De/AssertIRQn message based on UART's PME & D0i3 signals. The resulting De/AssertIRQn will have vector. as programmed in the corresponding GCR.IRQ_SEL_0/1 field.
0	0h RW	**Direct IRQ Enable for UART[0] (uart0_en):** This bit enables wake from S0ix and generation of De/AssertIRQn message based on UART's PME & D0i3 signals. The resulting De/AssertIRQn will have vector. as programmed in the corresponding GCR.IRQ_SEL_0/1 field.

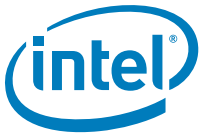
13.1.23 PCI Configuration Control 1 Register(PCICFGCTR1)—Offset 200h

Controls the PCI configuration space

Type: CFG Register (Size: 32 bits)	**Device:** **Function:**

Default: 100h

Range	Access Type	Default (reset)	Description
31:29	RO	0x0 (rst)	**Reserved0** Reserved
28:28	RW	0x0 (rst)	**DIS_PCI_IDLE_CAP1**
27:20	RW	0x0 (rst)	**PCI_IRQ1** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	RW	0x0 (rst)	**ACPI_IRQ1** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	RW	0x1 (rst)	**IPIN1** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7:7	RW	0x0 (rst)	**BAR1_DISABLE1** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	RW	0x0 (rst)	**PME_Support1** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1:1	RW	0x0 (rst)	**ACPI_INTR_EN1** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0:0	RW	0x0 (rst)	**PCI_CFG_DIS1** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported



13.1.24 PCI Configuration Control 2 Register(PCICFGCTR2)—Offset 204h

Controls the PCI configuration space

Type: CFG Register (Size: 32 bits)	**Device:** **Function:**

Default: 100h

Range	Access Type	Default (reset)	Description
31:29	RO	0x0 (rst)	**Reserved0** Reserved
28:28	RW	0x0 (rst)	**DIS_PCI_IDLE_CAP2**
27:20	RW	0x0 (rst)	**PCI_IRQ2** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	RW	0x0 (rst)	**ACPI_IRQ2** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	RW	0x1 (rst)	**IPIN2** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7:7	RW	0x0 (rst)	**BAR1_DISABLE2** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	RW	0x0 (rst)	**PME_Support2** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1:1	RW	0x0 (rst)	**ACPI_INTR_EN2** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0:0	RW	0x0 (rst)	**PCI_CFG_DIS2** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

13.1.25 PCI Configuration Control 3 Register(PCICFGCTR3)—Offset 208h

Controls the PCI configuration space

Type: CFG Register (Size: 32 bits)	**Device:** **Function:**

Default: 100h

Range	Access Type	Default (reset)	Description
31:29	RO	0x0 (rst)	**Reserved0** Reserved
28:28	RW	0x0 (rst)	**DIS_PCI_IDLE_CAP3**
27:20	RW	0x0 (rst)	**PCI_IRQ3** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	RW	0x0 (rst)	**ACPI_IRQ3** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	RW	0x1 (rst)	**IPIN3** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7:7	RW	0x0 (rst)	**BAR1_DISABLE3** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	RW	0x0 (rst)	**PME_Support3** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1:1	RW	0x0 (rst)	**ACPI_INTR_EN3** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0:0	RW	0x0 (rst)	**PCI_CFG_DIS3** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

13.2 Registers Summary

This space contains registers for use by the BIOS for configuring PMC behavior.

Table 13-2. Summary of GCR CR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1000h	1003h	Power and Reset Status (PRSTS)—Offset 1000h	0h
1008h	100Bh	PM CFG - Power Management Configuration (PMC_CFG)—Offset 1008h	0h
100Ch	100Fh	Power Management Configuration (PMC_CFG2)—Offset 100Ch	0h
1010h	1013h	SOC Power Management Status (SOC_PM_STS)—Offset 1010h	0h
1020h	1023h	General PM Configuration 1 (GEN_PMCON1)—Offset 1020h	4004h

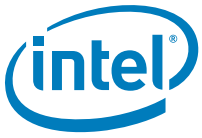


Table 13-2. Summary of GCR CR Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1024h	1027h	General PM Configuration 2 (GEN_PMCON2)—Offset 1024h	3800h
1028h	102Bh	General PM Configuration 3 (GEN_PMCON3)—Offset 1028h	0h
1030h	1033h	Configured Revision ID (CRID)—Offset 1030h	0h
1034h	1037h	Function Disable 0 (FUNC_DIS_0)—Offset 1034h	0h
1038h	103Bh	Function Disable 1 (FUNC_DIS_1)—Offset 1038h	0h
1048h	104Bh	Extended Test Mode Register (ETR)—Offset 1048h	18000h
1050h	1053h	GPIO Group to General Purpose Event Register Configuration (GPIO_GPE_CFG)—Offset 1050h	6300h
1064h	1067h	IRQ Select 0 (IRQ_SEL_0)—Offset 1064h	0h
1068h	106Bh	IRQ Select 1 (IRQ_SEL_1)—Offset 1068h	0h
106Ch	106Fh	IRQ Select 2 (IRQ_SEL_2)—Offset 106Ch	0h
1070h	1073h	Function ACPI Enumeration 0 (FUNC_ACPI_ENUM_0)—Offset 1070h	0h
1074h	1077h	Function ACPI Enumeration 1 (FUNC_ACPI_ENUM_1)—Offset 1074h	0h
1078h	107Bh	Fixed Deep S0Ix Counter Lower 32 Bits (TELEM_DEEP_S0IX_LO_HOST)—Offset 1078h	0h
107Ch	107Fh	Fixed Deep S0Ix Counter Upper 32 Bits (TELEM_DEEP_S0IX_HI_HOST)—Offset 107Ch	0h
1080h	1083h	Fixed Shallow S0Ix Counter Lower 32 Bits (TELEM_SHALLOW_S0IX_LO_HOST)—Offset 1080h	0h
1084h	1087h	Fixed Shallow S0Ix Counter Upper 32 Bits (TELEM_SHALLOW_S0IX_HI_HOST)—Offset 1084h	0h
1088h	108Bh	Reserved (TELEM_MISC_FIXED_LO_HOST)—Offset 1088h	0h
108Ch	108Fh	Reserved register for sharing data with software upper 32 bits (TELEM_MISC_FIXED_HI_HOST)—Offset 108Ch	0h
1090h	1093h	Scratchpad for sharing data between BIOS and PMC Firmware (BIOS_SCRATCHPAD)—Offset 1090h	0h
1094h	1097h	Display Hot Plug Detect Control (DISPLAY_HPD_CTL)—Offset 1094h	F0h
10C8h	10CBh	OBFF Control and Status (OBFF_CTL_STS)—Offset 10C8h	6450280Fh
10CCh	10CFh	Lock Register (LOCK)—Offset 10CCh	0h

13.2.1 Power and Reset Status (PRSTS)—Offset 1000h

Bits in this register only need to be valid for reading when the Main power well is up. However, since some of the events may initially be detected while the Main power well is down, they are marked as suspend well bits. All suspend well bits in this register are reset by global reset#.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	0h RO	**Reserved**
15	0h RO	**Reserved**
14:8	0h RO	**Reserved (reserved2):** Reserved.
7	0h RW/1C/V	**CSE Clear Reset Status (cse_cldrst_sts):** This bit will be set to '1' when the CSE FW triggers a reset. It will be cleared by a write of '1' by software. BIOS should read GEN_PMCON1 to determine what type of reset CSE requested. Reset by pwrgood.
6	0h RO	**Reserved**
5:0	0h RO	**Reserved (reserved1):** Reserved.

13.2.2 PM CFG - Power Management Configuration (PMC_CFG)—Offset 1008h

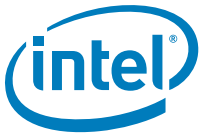
This register contains misc. fields used to configure the SOC's power management behavior.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

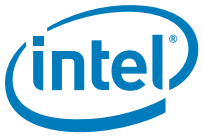
Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved (reserved4):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
19:18	0h RO	**Reserved (rsvd_slp_sus_min_asst_wdth):** SLP_SUS# Minimum Assertion Width. Reference only - This 2-bit value indicates the minimum assertion width of the SLP_SUS# signal to guarantee that the SUS Well power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 2'b00: 0 ms (i.e. stretching disabled - default) 2'b01: 500 ms 2'b10: 1 s 2'b11: 4 s This field is not writable when the SLP_Sx# Stretching Policy Lock Down bit is set. This field is ignored when exiting a G3 state if the Disable SLP_X Stretching After SUS Power Failure bit is set. Note that unlike with all other SLP_* pin stretching, this disable bit only impacts SLP_SUS# stretching during G3 exit rather than both G3 and DeepSx exit. SLP_SUS# stretching always applies to DeepSx regardless of the disable bit. Programming Note: For platforms that enable DeepSx, BIOS must program SLP_SUS# stretching to be greater than or equal to the largest stretching value on any other SLP_* pin (SLP_S3#, SLP_S4#, SLP_LAN#, or SLP_A#). This bit is only fully cleared by the RTEST# pin. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
17:16	0h RO	**Reserved (rsvd_slp_sus_a_asst_wdth):** SLP_A# Minimum Assertion Width. Reference only - This 2-bit value indicates the minimum assertion width of the SLP_A# signal to guarantee that the ASW power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 2'b00: 0 ms (i.e. stretching disabled - default) 2'b01: 4 s 2'b10: 98 ms 2'b11: 2 s This field is not writable when the SLP_Sx# Stretching Policy Lock Down bit is set. This field is ignored when exiting a G3 state if the Disable SLP_X Stretching After SUS Power Failure bit is set. This bit is only fully cleared by the RTEST# pin. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	**Reserved (reserved3):** Reserved.
9:8	0h RW/V/L	**Reset Power Cycle Duration (pwr_cyc_dur):** The value in this register determines the minimum time a platform will stay in reset (SLP_S3#, SLP_S4#, SLP_S5# asserted and also SLP_A# and SLP_LAN# asserted if applicable) during a host partition reset (if applicable) with power cycle or a global reset. The duration programmed in this register takes precedence over the applicable SLP_# stretch timers in these reset scenarios. Valid values are: 2'b11: 1-2 seconds 2'b10: 2-3 seconds 2'b01: 3-4 seconds 2'b00: 4-5 seconds (default) This field is not writable when the SLP_Sx# Stretching Policy Lock Down bit is set. Note that the duration programmed in this register should never be smaller than the stretch duration programmed in the following registers: GEN_PMCON_3.SLP_S3_MIN_ASST_WDTH GEN_PMCON_3.S4MAW PM_CFG.SLP_A_MIN_ASST_WDTH (if applicable) PM_CFG_SLP_LAN_MIN_ASST_WDTH (if applicable) This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well. These bits are fully cleared by RTCRST# assertion
7:6	0h RO	**Reserved (reserved2):** Reserved.
5	0h RO	**Reserved**
4	0h RW	**No Reboot (no_reboot):** FW will set this bit when TCO_NO_REBOOT SMIP is set.SW might also set this bit.When set, the TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout. Reset by: cold boot, cold reset, warm reset, and Sx.
3	0h RW	**S1/3/4/5 Entry Timeout Enable (sx_ent_to_en):** This policy bit determines whether the SOC will apply a timeout to the S3/S4/S5 entry flow. If this timeout is enabled and the entry flow appears to be hung, the SOC will trigger a global reset. Encodings: 0: Timeout Disabled (default) 1: Timeout Enabled On some prior platforms, this field is reset on RSMRST_B, a reset signal based on a RSMRST# pin that indicates the suspend/resume voltages are stable. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. Note: The active SMIP value to continue will override timeout bit for S4/S5 only.



Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RO	**Reserved (reserved1):** Reserved.

13.2.3 Power Management Configuration (PMC_CFG2)—Offset 100Ch

This register contains misc. fields used to configure the SOC's power management behavior.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Power Button Override Period (pwrbtn_ovr_per):** This field determines, while the power button remains asserted, how long the PMC will wait before initiating a global reset. Encoding: 3'b000: 4 seconds 3'b001: 6 seconds 3'b010: 8 seconds 3'b011: 10 seconds 3'b100: 12 seconds 3'b101: 14 seconds Others: Reserved This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.
28	0h RW/V/L	**Power Button Native Mode Disable (pwrbtn_dis):** When this bit is '0' (default), the PMC's power button logic will act upon the input value from the GPIO unit, as normal. When this bit is set to '1', the PMC must force its internal version of the power button pin to '1'. This will result in the PMC logic constantly seeing the pin as de-asserted. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
27:11	0h RO	**Reserved (reserved0):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/V	**Power Button Debounce Mode (pwrbtn_db_mode):** This bit controls when interrupts (SMI#, SCI) are generated in response to assertion of the PWRBTN# pin. This bit's values cause the following behavior: 0: The 16 ms debounce period applies to all usages of the PWRBTN# pin (legacy behavior). 1: When a falling edge occurs on the PWRBTN# pin, an interrupt is generated and the 16 ms debounce timer starts. Subsequent interrupts are masked while the debounce timer is running. Note: Power button override logic always samples the post-debounce version of the pin. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
9:0	0h RO	**Reserved (reserved1):** Reserved.

13.2.4 SOC Power Management Status (SOC_PM_STS)—Offset 1010h

This register contains misc. fields used to record events pertaining to SOC power management. Unless otherwise indicated, all RWC bits are cleared with a write of 1 by software.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

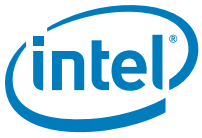
Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved (rsvd):** Reserved.
2	0h RO	**Reserved**
1	0h RO	**Reserved**
0	0h RO	**Reserved (reserved1):** Reserved.

13.2.5 General PM Configuration 1 (GEN_PMCON1)—Offset 1020h

Access Method

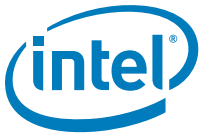
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4004h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (reserved6):** Reserved.
27	0h RW/1C/V	**Cold Boot Status (cold_boot_sts):** FW will populate this BIOS visible bit based on a COLD BOOT. This bit acts as notification to BIOS of the type of boot/reset. Reset by: cold boot, cold reset, warm reset, and Sx.
26	0h RW/1C/V	**Cold Reset Status (cold_reset_sts):** FW will populate this BIOS visible bit based on a COLD RESET. This bit acts as notification to BIOS of the type of boot/reset. Reset by: cold boot, cold reset, warm reset, and Sx.
25	0h RW/1C/V	**Warm Reset Status (warm_reset_sts):** FW will populate this BIOS visible bit based on a WARM RESET. This bit acts as notification to BIOS of the type of boot/reset. Reset by: cold boot, cold reset, warm reset, and Sx.
24	0h RW/1C/V	**Global Reset Status (global_reset_sts):** FW will populate this BIOS visible bit based on a GLOBAL RESET. This bit acts as notification to BIOS of the type of boot/reset. Reset by: cold boot, cold reset, warm reset, and Sx.
23	0h RW	**DRAM Initialization Scratchpad Bit (disb):** This bit does not effect hardware functionality in any way. It is provided as a scratchpad bit that is maintained through main power well resets and CF9h-initiated resets. BIOS is expected to set this bit prior to starting the DRAM initialization sequence and to clear this bit after completing the DRAM initialization sequence. BIOS can detect that a DRAM initialization sequence was interrupted by a reset by reading this bit during the boot sequence. If the bit is 1, then the DRAM initialization was interrupted. On some prior platforms, this field is reset on RSMRST_B, a reset signal based on a RSMRST# pin that indicates the suspend/resume voltages are stable. This field is reset on RSM_RST_N de-assertion that is based on the PMIC_PWRGOOD, , PCH_PWROK, or COREPWROK pin, depending on the platform config. This field is not reset on cold reset, warm reset, and Sx.
22	0h RO	**Reserved (reserved5):** Reserved.
21	0h RO	**Reserved**
20	0h RW/1C/V	**System Reset Status (srs):** This bit will be set based on an asserting edge of the PMU_RESETBUTTON_B pin (post 16 ms HW debounce if PMU_RESETBUTTON_B Debounce Disable SMIP is 0) BIOS is expected to read this bit and clear it if it is set. This bit is also reset by RSMRST_B and CF9h resets. reset_type=Resume Well Reset#. RSMRST_B is a reset signal based on a RSMRST# pin that indicates the suspend/resume voltages are stable. This reset would correspond to RSM_RST_N
19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C/V	**Minimum PMU SLP S4 B Assertion Width Violation Status (ms4v):** Hardware sets this bit when the PMU_SLP_S4_B assertion width is less than the time programmed in the PMU_SLP_S4_B Minimum Assertion Width field. The SOC begins the timer when PMU_SLP_S4_B pin is asserted during S4/S5 entry, or when the RSMRST_B input is deasserted during SUS well power-up. The status bit is cleared by software writing a 1 to the bit. Note that this bit is functional regardless of the value in the PMU_SLP_S4_B Assertion Stretch Enable and the Disable-SLP_X-Stretching-After-SUS-Power-Failure bits. This bit is reset by the assertion of the RSMRST_B pin, but can be set in some cases before the default value is readable. RSMRST_B is a reset signal based on a RSMRST# pin that indicates the suspend/resume voltages are stable. This reset would correspond to RSM_RST_N. Note: Relevant only for no PMIC mode.
17	0h RO	**Reserved (reserved4):** Reserved
16	0h RO	**Reserved**
15	0h RW/V	**PME B0 S5 Disable (pme_b0_s5_dis):** When set to '1', this bit blocks wake events from PME_B0_STS in S5, regardless of the state of PME_B0_EN. When cleared (default), wake events from PME_B0_STS are allowed in S5 if PME_B0_EN = '1'. Wakes from power states other than S5 are not affected by this policy bit. The SoC does not PME_B0_STS. It has a separate STS and EN for each source. Therefore this bit affects GPE0a_STS/EN bits for: XDCI, XHCI, and AVS. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well. This bit is only fully cleared by the SRTCRST_B pin (on the removal of coin battery).
14	1h RO	**Reserved**
13:10	0h RO	**Reserved (Reserved3):** Reserved
9	0h RO	**Reserved**
8	0h RO	**Reserved (Reserved2):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RW/V	**SWSMI Rate Select (swsmi_ratesel):** This 2-bit value indicates when the SWSMI timer will time out. Valid values are: 00 1.5 ms +/- 0.6 ms 01 16 ms +/- 4 ms 10 32 ms +/- 4 ms 11 64 ms +/- 4 ms reset_type = SRTCRST_B pin (removal of coin battery). This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
5:3	0h RO	**Reserved (reserved1):** Reserved.
2	1h RW/V	**RTC Power Status (rps):** Intel SOC will set this bit to 1 when RTEST_B indicates a weak or missing battery. The bit will remain set until the software clears it by writing a 0 back to this bit position. This bit is not cleared by any type of reset because a cleared shadowed value will be restored prior to this bit being visible. Note: Relevant only for no PMIC mode while SoC includes RTC well. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well.
1	0h RO	**Reserved (reserved0):** Reserved.
0	0h RW/V/L	**After G3 Enable (ag3e):** Determines what state to go to when power is reapplied after a power failure (G3 state). 0: System will return to an S0 state (boot) after power is re-applied. 1: System will return to the S5 state (except if it was in S4, in which case it will return to S4-like state). In the S5 state, the only enabled wake-up event is the Power Button or any enabled wake event that was preserved through the power failure. This bit is in the RTC well and is only cleared by SRTCRST_B assertion (on the removal of coin battery). Note: Relevant only for no PMIC mode. This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This field is shadowed in the PMC RTC Well

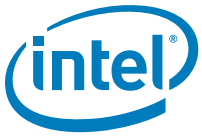
13.2.6 General PM Configuration 2 (GEN_PMCON2)—Offset 1024h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3800h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved (reserved1):** Reserved.
13:11	7h RW/L	**LPC Loopback Clock Control (lpc_lpb_clk_ctrl):** Delay for LPC loopback clock (to match board latency to and from the embedded controller. 000: RESERVED (This setting is not supported and may lead to inconsistent behavior on silicon) 001: 1.25 ns 010: 3.75 ns 011: 6.25 ns 100: 8.75 ns 101: 11.25 ns 110: 12.50 ns 111: 13.75 ns This field is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx. This register is locked by GCR.LOCK.lpc_lpb_clk_ctrl.
10	0h RO	**Reserved**
9	0h RO/V	**Power Button Level (pwrbtn_lvl):** This read-only bit indicates the current state of the PWRBTN# signal. 1: High 0: Low The value reflected in this bit is dependent upon PM_CFG1.PB_DB_MODE. The PB_DB_MODE bit's value causes the following behavior: 0: PWRBTN_LVL is taken from the debounced PWRBTN# pin value that is seen at the output of a 16 ms debouncer. 1: PWRBTN_LVL is taken from the raw PWRBTN# pin (before the debouncer).
8:5	0h RO	**Reserved (reserved3):** Reserved.
4	0h RW/L	**SMI Lock (smi_lock):** When this bit is set, writes to the GBL_SMI_EN bit will have no effect. Once the SMI_LOCK bit is set, writes of 0 to SMI_LOCK bit will have no effect (i.e. once set, this bit can only be cleared by reset). Reset: Reset on cold boot, cold reset, warm reset, Sx. In architectures that support partitioned resets, this bit reset on host partition reset. The SoC does not have a host partition reset.
3:2	0h RO	**Reserved (reserved4):** Reserved.
1:0	0h RW/L	**Period SMI Select (per_smi_sel):** Software sets these bits to control the rate at which the periodic SMI# is generated: 00: 64 seconds (default) 01 = 32 seconds 10 = 16 seconds 11 = 8 seconds Tolerance for the timer is +/- 1 second. Reset: Reset on cold boot, cold reset, warm reset, Sx.



13.2.7 General PM Configuration 3 (GEN_PMCON3)—Offset 1028h

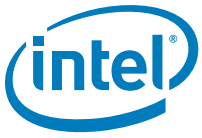
Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved (reserved1):** Reserved.
12	0h RO	**Reserved**
11:10	0h RW/L	**PMU SLP S3 B Minimum Assertion Width (slp_s3_min_asst_wdth):** Reference only: This 2-bit value indicates the minimum assertion width of the PMU_SLP_S3_B signal to guarantee that the Main power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00: 60 usec 01: 1 ms 10: 50 ms 11: 2 sec This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by the RSMRST_B pin. Note: Relevant only for no PMIC mode. RSMRST_B is a reset signal based on a RSMRST# pin that indicates the suspend/resume voltages are stable. This would correspond to RSM_RST_N based on the PMIC_PWRGOOD signal.
9:6	0h RO	**Reserved (reserved2):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW/V/L	**PMU SLP S4 B Minimum Assertion Width (s4maw):** This 2-bit value indicates the minimum assertion width of the PMU_SLP_S4_B signal to guarantee that the DRAMs have been safely power-cycled. This value may be modified per platform depending on DRAM types, power supply capacitance, etc. Valid values are: 11: 1 second 10: 2 seconds 01: 3 seconds 00: 4 seconds This value is used in two ways: If the PMU_SLP_S4_B assertion width is ever shorter than this time, a status bit is set for BIOS to read when S0 is entered. If enabled by bit 3 in this register, the hardware will prevent the PMU_SLP_S4_B signal from deasserting within this minimum time period after asserting. Note that the logic that measures this time is in the suspend power well. Therefore, when leaving a G3 state, the minimum time is measured from the deassertion of the internal suspend well reset (unless the Disable SLP_X Stretching After SUS Power Failure bit is set). This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. SRTCRST_B forces this field to the conservative default state (00b). Note: Relevant only for no PMIC mode. SRTCRST_B is a secure version of the RTC reset and is asserted only on the removal of coin battery. The SoC does not have an on-die RTC well. This field is shadowed in the PMC RTC Well



Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/V/L	**PMU SLP S4 B Assertion Stretch Enable (s4ase):** When set to 1, the PMU_SLP_S4_B pin will minimally assert for the time specified in bits 5:4 of this register. When 0, the reset flow still includes the SLP_S3_MIN_ASST_WDTH but no additional time is included for S4ASE. This bit is provided so that all DIMMs in the system can deterministically detect a power-cycle event for proper initialization. Note that there are behavioral changes that may be noticeable to the end-user when this bit is set. Resume times from S4 and S5 and power-up times from G3 may be delayed by several seconds. Cases in which this feature may not be desirable and therefore keeping the bit cleared are: A customer decides the user confusion due to the hardware delay is a bigger issue than the potential DRAM issue A customer decides the software status bit solution is adequate A different DRAM type is used or the platform provides an external solution to solve the power-cycling issue Validation regressions are impacted by the delay (especially after RSMRST_B deassertion) Avoid potential resume time WHQL violations This bit is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by SRTCRST_B. Note: Relevant only for no PMIC mode. SRTCRST_B is a secure version of the RTEST_B RTC reset and is asserted only on the removal of coin battery. The SoC does not have an on-die RTC well. This field is shadowed in the PMC RTC Well
2:0	0h RO	**Reserved (reserved3):** Reserved.

13.2.8 Configured Revision ID (CRID)—Offset 1030h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved (rsvd):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW/L	**RID Select (rid_sel):** Software writes this field to select the fuse sets reflected in PCI config space Revision ID. The decoding is: 00: Revision ID 01: CRID 0 10: CRID 1 11: CRID 2 This is reset on cold boot, cold reset, warm reset, and Sx. Reset: Reset on cold boot, cold reset, warm reset, Sx. In architectures that support partitioned resets, this bit reset on host partition reset. The SoC does not have a host partition reset. (setid multicast sends this out)

13.2.9 Function Disable 0 (FUNC_DIS_0)—Offset 1034h

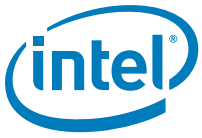
BIOS uses this register to disable specific function. PMC FW consults this register during reset to determine whether to bring an IP out of reset. These are only reset on RSM_RST_N de-assertion.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**RSVD**
30	0h RW/L	**SPI Disable (spi):** Set by BIOS to inform PMC SPI is disabled.
29	0h RW/L	**SSRAM Disable (ssram):** Set by BIOS to inform PMC SSRAM is disabled.
28	0h RW/L	**AVS Disable (avs):** Set by BIOS to inform PMC AVS is disabled.
27	0h RW/L	**CSE HECI1 Disable (cse_heci1):** Set by BIOS to inform PMC CSE_HECI1 is disabled. CSE_HECI1 is function 0 of a Multi-function device. If this function is disabled all functions of this device must be disabled.
26	0h RW/L	**CSE HECI2 Disable (cse_heci2):** Set by BIOS to inform PMC CSE_HECI2 is disabled.
25	0h RW/L	**CSE HECI3 Disable (cse_heci3):** Set by BIOS to inform PMC CSE_HECI3 is disabled.
24	0h RW/L	**ISH Disable (ish):** Set by BIOS to inform PMC ISH is disabled.
23	0h RW/L	**PCIE0P0 Disable (pcie0p0):** Set by BIOS to inform PMC PCIE0 port 0 is disabled.



Bit Range	Default & Access	Field Name (ID): Description
22	0h RW/L	**PCIE0P1 Disable (pcie0p1):** Set by BIOS to inform PMC PCIE0 port 1 is disabled.
21	0h RW/L	**LPSS I2C0 Disable (lpss_i2c0):** Set by BIOS to inform PMC LPSS_I2C0 is disabled. LPSS_I2C0 is function 0 of a Multi-function device. If this function is disabled all functions of this device must be disabled.
20	0h RW/L	**LPSS I2C1 Disable (lpss_i2c1):** Set by BIOS to inform PMC LPSS_I2C1 is disabled.
19	0h RW/L	**LPSS I2C2 Disable (lpss_i2c2):** Set by BIOS to inform PMC LPSS_I2C2 is disabled.
18	0h RW/L	**LPSS I2C3 Disable (lpss_i2c3):** Set by BIOS to inform PMC LPSS_I2C3 is disabled.
17	0h RW/L	**LPSS I2C4 Disable (lpss_i2c4):** Set by BIOS to inform PMC LPSS_I2C4 is disabled. LPSS_I2C4 is function 0 of a Multi-function device. If this function is disabled all functions of this device must be disabled.
16	0h RW/L	**LPSS I2C5 Disable (lpss_i2c5):** Set by BIOS to inform PMC LPSS_I2C5 is disabled.
15	0h RW/L	**LPSS I2C6 Disable (lpss_i2c6):** Set by BIOS to inform PMC LPSS_I2C6 is disabled.
14	0h RW/L	**LPSS I2C7 Disable (lpss_i2c7):** Set by BIOS to inform PMC LPSS_I2C7 is disabled.
13	0h RW/L	**LPSS UART0 Disable (lpss_uart0):** Set by BIOS to inform PMC LPSS_UART0 is disabled. LPSS_UART0 is function 0 of a Multi-function device. If this function is disabled all functions of this device must be disabled.
12	0h RW/L	**LPSS UART1 Disable (lpss_uart1):** Set by BIOS to inform PMC LPSS_UART1 is disabled.
11	0h RW/L	**LPSS UART2 Disable (lpss_uart2):** Set by BIOS to inform PMC LPSS_UART2 is disabled.
10	0h RW/L	**LPSS UART3 Disable (lpss_uart3):** Set by BIOS to inform PMC LPSS_UART3 is disabled.
9	0h RW/L	**LPSS SPI0 Disable (lpss_spi0):** Set by BIOS to inform PMC LPSS_SPI0 is disabled. LPSS_SPI0 is function 0 of a Multi-function device. If this function is disabled all functions of this device must be disabled.
8	0h RW/L	**LPSS SPI1 Disable (lpss_spi1):** Set by BIOS to inform PMC LPSS_SPI1 is disabled.
7	0h RW/L	**LPSS SPI2 Disable (lpss_spi2):** Set by BIOS to inform PMC LPSS_SPI2 is disabled.
6	0h RW/L	**PWM Disable (pwm):** Set by BIOS to inform PMC PWM is disabled.
5	0h RW/L	**SDCARD Disable (sdcard):** Set by BIOS to inform PMC SDCARD is disabled.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/L	**Reserved**
3	0h RW/L	**eMMC Disable (emmc):** Set by BIOS to inform PMC eMMC is disabled.
2	0h RW/L	**Rsvd**
1	0h RW/L	**xHCI Disable (xhci):** Set by BIOS to inform PMC xHCI is disabled. xHCI is function 0 of a Multi-function device. If this function is disabled all functions of this device must be disabled.
0	0h RW/L	**xDCI Disable (xdci):** Set by BIOS to inform PMC xDCI is disabled.

13.2.10 Function Disable 1 (FUNC_DIS_1)—Offset 1038h

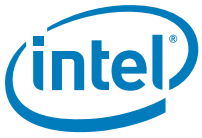
BIOS uses this register to disable specific function. PMC FW consults this register during reset to determine whether to bring an IP out of reset.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved (rsvd31):** Reserved.
9	0h RW/L	**SATA Disable (sata):** Set by BIOS to inform PMC SATA is disabled.
8:7	0h RO	**Reserved PCIE Disable (rsvd_pcie):** Reserved for PCIe expansion.
6	0h RW/L	**PCIE1 Port 3 Disable (pcie1p3):** Set by BIOS to inform PMC PCIE1 port 3 is disabled.
5	0h RW/L	**PCIE1 Port 2 Disable (pcie1p2):** Set by BIOS to inform PMC PCIE1 port 2 is disabled.
4	0h RW/L	**PCIE1 Port 1 Disable (pcie1p1):** Set by BIOS to inform PMC PCIE1 port 1 is disabled.
3	0h RW/L	**PCIE1 Port 0 Disable (pcie1p0):** Set by BIOS to inform PMC PCIE1 port 0 is disabled.
2	0h RW/L	**Rsvd**
1:0	0h RO	**Reserved (rsvd0):** Reserved.



13.2.11 Extended Test Mode Register (ETR)—Offset 1048h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 18000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**CF9h Lockdown (cf9lock):** When set, this will lock the CF9h-Global-Reset bit. When set, this register locks itself. On architectures that support partitioned resets, this bit is reset on a host partition reset. Reset: Reset on cold boot, cold reset, warm reset, Sx.
30:21	0h RO	**Reserved (reserved3):** Reserved.
20	0h RW/L	**CF9h Global Reset (cf9gr):** When this bit is set, a CF9h write of 6h or Eh will cause a Global Reset (of the Host partition where the designation is applicable). If this bit is cleared, a CF9h write of 6h or Eh will only reset the Host partition (Cold or Warm reset were no Host partition.) It is recommended that BIOS should set this bit early on in the boot sequence, and then clear it and set the CF9LOCK bit prior to loading the OS. When this bit is set, the hardware assumes that bit 18 (CF9h Without Resume Well Reset Enable) is cleared. This register is locked by the CF9 Lockdown (CF9LOCK) bit. On architectures that support resume well reset, this bit is resets on RSMRST_B. RSMRST_B is a reset signal based on a RSMRST# pin that indicates the suspend/resume voltages are stable. The SoC does not have a host partition reset or a resume well. Reset: Reset on cold boot, cold reset, warm reset, Sx.
19:18	0h RO	**Reserved (reserved2):** Reserved.
17:15	3h RW/L	**Max S0IX (max_s0ix):** Indicated the maximum S0i state SOC can go. 111: LTR/TNTE L6 threshold (S0i3) - Deepest S0ix state allowed 110: LTR/TNTE L6 threshold (S0i3) 101: LTR/TNTE L5 threshold 100: LTR/TNTE L4 threshold 011: LTR/TNTE L3 threshold 010: LTR/TNTE L2 threshold (Fastest Exit/Highest Pwr) 001: LTR/TNTE L1 threshold 000: No S0ix state allowed Reset Type: cold boot, cold reset, warm reset, and Sx.
14:0	0h RO	**Reserved (reserved1):** Reserved.

13.2.12 GPIO Group to General Purpose Event Register Configuration (GPIO_GPE_CFG)—Offset 1050h

Maps the ACPI GPE0[b-d] registers to GPIO groups. Each of gpe0_dw[1-3] is a lookup which maps a read/write to gpe0[b-d]_[en,sts] to a particular GPIO community and offset.

General purpose event enable register address mapping
15: 16'h130 (reserved)
14: 16'h130 (reserved)
13: 16'h130 (reserved)
12: 16'h130 (reserved)
11: 16'h138
10: 16'h134
09: 16'h130
08: 16'h138
07: 16'h134
06: 16'h130
05: 16'h138
04: 16'h134
03: 16'h130
02: 16'h138
01: 16'h134
00: 16'h130

General purpose event status register address mapping
15: 16'h120 (reserved)
14: 16'h120 (reserved)
13: 16'h120 (reserved)
12: 16'h120 (reserved)
11: 16'h128
10: 16'h124
09: 16'h120
08: 16'h128
07: 16'h124
06: 16'h120
05: 16'h128
04: 16'h124
03: 16'h120
02: 16'h128
01: 16'h124
00: 16'h120

GPIO Community PortID mapping
15: SB_PORTID_GPSW_CORE (reserved)
14: SB_PORTID_GPSW_CORE (reserved)
13: SB_PORTID_GPSW_CORE (reserved)
12: SB_PORTID_GPSW_CORE (reserved)
11: SB_PORTID_GPW_CORE
10: SB_PORTID_GPW_CORE
09: SB_PORTID_GPW_CORE
08: SB_PORTID_GPN_CORE
07: SB_PORTID_GPN_CORE
06: SB_PORTID_GPN_CORE

05: SB_PORTID_GPNW_CORE
04: SB_PORTID_GPNW_CORE
03: SB_PORTID_GPNW_CORE
02: SB_PORTID_GPSW_CORE
01: SB_PORTID_GPSW_CORE
00: SB_PORTID_GPSW_CORE

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6300h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (rsvd31):** Reserved.
15:12	6h RW	**GPIO Group to General Purpose Event Dword 3 (gpe0_dw3):** This register assigns a specific GPIO Group to the ACPI GPE0d (i.e. GPE0[127:96]). The value in this field determines which GPIO group is assigned to dword 3 (gpe0d).
11:8	3h RW	**GPIO Group to General Purpose Event Dword 2 (gpe0_dw2):** This register assigns a specific GPIO Group to the ACPI GPE0c (i.e. GPE0[95:64]). The value in this field determines which GPIO group is assigned to dword 2 (gpe0c).
7:4	0h RW	**GPIO Group to General Purpose Event Dword 1 (gpe0_dw1):** This register assigns a specific GPIO Group to the ACPI GPE0b (i.e. GPE0[63:32]). The value in this field determines which GPIO group is assigned to dword 1 (gpe0b).
3:0	0h RO	**Reserved (rsvd_gpe0_dw0):** GPIO Group to General Purpose Event Dword 0. This register assigns a specific GPIO Group to the ACPI GPE0a (i.e. GPE0[31:0]). The value in this field determines which GPIO group is assigned to dword 0 (gpe0a). This register is reserved / unused, because gpe0a is a local ACPI register.

13.2.13 IRQ Select 0 (IRQ_SEL_0)—Offset 1064h

ACPI uses these fields to fill the IRQ vector of the De/Assert_IRQn message for Direct IRQs. For the SoC, reset on cold boot, cold reset, warm reset, and Sx.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**IRQ Vector For UART 3 (dir_irq_sel_uart3)**
23:16	0h RW	**IRQ Vector For UART 2 (dir_irq_sel_uart2)**
15:8	0h RW	**IRQ Vector For UART 1 (dir_irq_sel_uart1)**
7:0	0h RW	**IRQ Vector For UART 0 (dir_irq_sel_uart0)**

13.2.14 IRQ Select 1 (IRQ_SEL_1)—Offset 1068h

ACPI uses these fields to fill the IRQ vector of the De/Assert_IRQn message for Direct IRQs. For the SoC, reset on cold boot, cold reset, warm reset, and Sx.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**IRQ Vector For XHCI (dir_irq_sel_xhci)**
23:16	0h RW	**IRQ Vector For XDCI (dir_irq_sel_xdci)**
15:8	0h RW	**IRQ Vector For SDCARD CD (dir_irq_sel_sdcard_cd)**
7:0	0h RW	**IRQ Vector For SDCARD D1 (dir_irq_sel_sdcard_d1)**

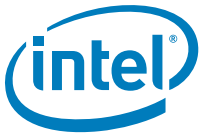
13.2.15 IRQ Select 2 (IRQ_SEL_2)—Offset 106Ch

ACPI uses these fields to fill the IRQ vector of the De/Assert_IRQn message for Direct IRQs. For the SoC, reset on cold boot, cold reset, warm reset, and Sx.
On architectures that support a partitioned resets this bit is reset on the host reset (host_prim_rst_b).

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**SCI IRQ Select (scis):** Specifies on which IRQ the SCI will internally appear. ACPI uses this field to fill the IRQ vector of the De/Assert_IRQn message for IOAPIC IRQ for PMIC interrupts. If not using the APIC, the SCI must be routed to IRQ[9-11], and that interrupt is not shareable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the SCI can also be mapped to IRQ20-23, and can be shared with other interrupts. This field fully defines the IRQ number to be sent. When the interrupt is mapped to APIC interrupts 9, 10 or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception.
23:16	0h RW	**PMIC Direct IRQ Select (dir_irq_sel_pmic):** ACPI uses this field to fill the IRQ vector of the De/Assert_IRQn message for IOAPIC IRQ for PMIC interrupts.
15:0	0h RO	**Reserved (rsvd):** Reserved.

13.2.16 Function ACPI Enumeration 0 (FUNC_ACPI_ENUM_0)—Offset 1070h

BIOS uses this register to enumerate ACPI functions. For the SoC, reset on cold boot, cold reset, warm reset, and Sx.

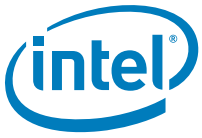
Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved Enable (rsvd31):** Reserved.
30	0h RW	**SPI Enable (spi):** If set by BIOS the named function is exposed to the OS via ACPI.
29	0h RW	**SSRAM Enable (ssram):** If set by BIOS the named function is exposed to the OS via ACPI.
28	0h RW	**AVS Enable (avs):** If set by BIOS the named function is exposed to the OS via ACPI.
27	0h RW	**CSE HECI1 Enable (cse_heci1):** If set by BIOS the named function is exposed to the OS via ACPI.
26	0h RW	**CSE HECI2 Enable (cse_heci2):** If set by BIOS the named function is exposed to the OS via ACPI.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW	**CSE HECI3 Enable (cse_heci3):** If set by BIOS the named function is exposed to the OS via ACPI.
24	0h RW	**ISH Enable (ish):** If set by BIOS the named function is exposed to the OS via ACPI.
23	0h RO	**Reserved (rsvd23):** Reserved.
22	0h RO	**Reserved (rsvd22):** Reserved.
21	0h RW	**LPSS I2C0 Enable (lpss_i2c0):** If set by BIOS the named function is exposed to the OS via ACPI.
20	0h RW	**LPSS I2C1 Enable (lpss_i2c1):** If set by BIOS the named function is exposed to the OS via ACPI.
19	0h RW	**LPSS I2C2 Enable (lpss_i2c2):** If set by BIOS the named function is exposed to the OS via ACPI.
18	0h RW	**LPSS I2C3 Enable (lpss_i2c3):** If set by BIOS the named function is exposed to the OS via ACPI.
17	0h RW	**LPSS I2C4 Enable (lpss_i2c4):** If set by BIOS the named function is exposed to the OS via ACPI.
16	0h RW	**LPSS I2C5 Enable (lpss_i2c5):** If set by BIOS the named function is exposed to the OS via ACPI.
15	0h RW	**LPSS I2C6 Enable (lpss_i2c6):** If set by BIOS the named function is exposed to the OS via ACPI.
14	0h RW	**LPSS I2C7 Enable (lpss_i2c7):** If set by BIOS the named function is exposed to the OS via ACPI.
13	0h RW	**LPSS UART0 Enable (lpss_uart0):** If set by BIOS the named function is exposed to the OS via ACPI.
12	0h RW	**LPSS UART1 Enable (lpss_uart1):** If set by BIOS the named function is exposed to the OS via ACPI.
11	0h RW	**LPSS UART2 Enable (lpss_uart2):** If set by BIOS the named function is exposed to the OS via ACPI.
10	0h RW	**LPSS UART3 Enable (lpss_uart3):** If set by BIOS the named function is exposed to the OS via ACPI.
9	0h RW	**LPSS SPI0 Enable (lpss_spi0):** If set by BIOS the named function is exposed to the OS via ACPI.
8	0h RW	**LPSS SPI1 Enable (lpss_spi1):** If set by BIOS the named function is exposed to the OS via ACPI.
7	0h RW	**LPSS SPI2 Enable (lpss_spi2):** If set by BIOS the named function is exposed to the OS via ACPI.
6	0h RW	**PWM Enable (pwm):** If set by BIOS the named function is exposed to the OS via ACPI.
5	0h RW	**SDCARD Enable (sdcard):** If set by BIOS the named function is exposed to the OS via ACPI.



Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Reserved**
3	0h RW	**eMMC Enable (emmc):** If set by BIOS the named function is exposed to the OS via ACPI.
2	0h RW	**RSVD**
1	0h RO	**Reserved (rsvd1):** Reserved.
0	0h RW	**xDCI Enable (xdci):** If set by BIOS the named function is exposed to the OS via ACPI.

13.2.17 Function ACPI Enumeration 1 (FUNC_ACPI_ENUM_1)—Offset 1074h

BIOS uses this register to enumerate ACPI functions. For the SoC, reset on cold boot, cold reset, warm reset, and Sx.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved (rsvd31):** Reserved.
2	0h RW	**Rsvd**
1	0h RW	**PMC PCI Enable (pmc_pci):** If set by BIOS the named function is exposed to the OS via ACPI.
0	0h RW	**P2SB Enable (p2sb):** If set by BIOS the named function is exposed to the OS via ACPI.

13.2.18 Fixed Deep S0Ix Counter Lower 32 Bits (TELEM_DEEP_S0IX_LO_HOST)—Offset 1078h

For the SoC, reset on cold boot, cold reset, warm reset, and Sx.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Fixed Deep S0Ix Counter (telem_deep_s0ix_lo_host)**

13.2.19 Fixed Deep S0Ix Counter Upper 32 Bits (TELEM_DEEP_S0IX_HI_HOST)—Offset 107Ch

For the SoC, reset on cold boot, cold reset, warm reset, and Sx.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Fixed Deep S0Ix Counter Upper 32 Bits (telem_deep_s0ix_hi_host)**

13.2.20 Fixed Shallow S0Ix Counter Lower 32 Bits (TELEM_SHALLOW_S0IX_LO_HOST)—Offset 1080h

For the SoC, reset on cold boot, cold reset, warm reset, and Sx.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Fixed Shallow S0Ix Counter (telem_shallow_s0ix_lo_host)**

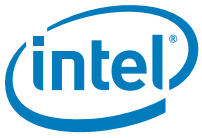
13.2.21 Fixed Shallow S0Ix Counter Upper 32 Bits (TELEM_SHALLOW_S0IX_HI_HOST)—Offset 1084h

For the SoC, reset on cold boot, cold reset, warm reset, and Sx.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Fixed Shallow S0Ix Counter (telem_shallow_s0ix_hi_host)**

13.2.22 Reserved (TELEM_MISC_FIXED_LO_HOST)—Offset 1088h

Register for sharing data with software lower 32 bits. For the SoC, reset on cold boot, cold reset, warm reset, and Sx.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Reserved (telem_misc_fixed_lo_host):** Reserved register for sharing data with software.

13.2.23 Reserved register for sharing data with software upper 32 bits (TELEM_MISC_FIXED_HI_HOST)—Offset 108Ch

For the SoC, reset on cold boot, cold reset, warm reset, and Sx.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Reserved (telem_misc_fixed_hi_host):** Reserved register for sharing data with software.

13.2.24 Scratchpad for sharing data between BIOS and PMC Firmware (BIOS_SCRATCHPAD)—Offset 1090h

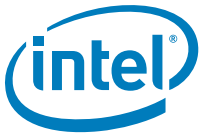
For the SoC, reset on cold boot, cold reset, warm reset, and Sx.
This register is reset on RSM_RST_N de-assertion. This field is not reset on cold reset, warm reset, and Sx.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Scratchpad 31 (scratchpad31):** This field is shadowed in the PMC RTC Well.
30	0h RW/V	**Scratchpad 30 (scratchpad30):** This field is shadowed in the PMC RTC Well.
29	0h RW/V	**Scratchpad 29 (scratchpad29):** This field is shadowed in the PMC RTC Well.
28	0h RW/V	**Scratchpad 28 (scratchpad28):** This field is shadowed in the PMC RTC Well.
27	0h RW	**Scratchpad 27 (scratchpad27)**
26	0h RW	**Scratchpad 26 (scratchpad26)**
25	0h RW	**Scratchpad 25 (scratchpad25)**
24	0h RW	**Scratchpad 24 (scratchpad24)**
23	0h RW	**Scratchpad 23 (scratchpad23)**
22	0h RW	**Scratchpad 22 (scratchpad22)**
21	0h RW	**Scratchpad 21 (scratchpad21)**
20	0h RW	**Scratchpad 20 (scratchpad20)**
19	0h RW	**Scratchpad 19 (scratchpad19)**
18	0h RW	**Scratchpad 18 (scratchpad18)**
17	0h RW	**Scratchpad 17 (scratchpad17)**
16	0h RW	**Scratchpad 16 (scratchpad16)**
15	0h RW	**Scratchpad 15 (scratchpad15)**
14	0h RW	**Scratchpad 14 (scratchpad14)**
13	0h RW	**Scratchpad 13 (scratchpad13)**
12	0h RW	**Scratchpad 12 (scratchpad12)**
11	0h RW	**Scratchpad 11 (scratchpad11)**
10	0h RW	**Scratchpad 10 (scratchpad10)**



Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Scratchpad 9 (scratchpad9)**
8	0h RW	**Scratchpad 8 (scratchpad8)**
7	0h RW	**Scratchpad 7 (scratchpad7)**
6	0h RW	**Scratchpad 6 (scratchpad6)**
5	0h RW	**Scratchpad 5 (scratchpad5)**
4	0h RW	**Scratchpad 4 (scratchpad4)**
3	0h RW	**Scratchpad 3 (scratchpad3)**
2	0h RW	**Scratchpad 2 (scratchpad2)**
1	0h RW	**S0IX Inhibit (s0ix_inhibit):** Used by PCIE ASL code
0	0h RW	**MOT Enable (mot_enable):** Indicates that MOT is enabled. When set to '1', PMC firmware will only switch ART to RTC after receiving the VnnOffPrepAck from pcode. This ensures proper time sync handling all the way until PCS is down.

13.2.25 Display Hot Plug Detect Control (DISPLAY_HPD_CTL)—Offset 1094h

Controls for PMC display hot plug detect logic. Hot plug detect is offloaded from display during S0ix, is used to gate S0ix entry, is an S0ix wake condition, and may result in notification to display controller. PMC implements a simplified hot plug detect, where the input is deglitched and edges are detected.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: F0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (rsvd):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RW	**Edge Rising (edge_rising):** Enable detection of rising edges. One bit per GPIO HPD wire. More than one GPIO can be enabled. One or both edges may be of interest, and the edge of interest may change based on polarity of GPIO HPD wire. edge_rising = 3'b001: ddi0 rising edges enabled edge_rising = 3'b010: ddi1 rising edges enabled ... edge_rising = 3'b111: ddi2, ddi1 and ddi0 rising edges enabled
12:10	0h RW	**Edge Falling (edge_falling):** Enable detection of falling edges. One bit per GPIO HPD wire. More than one GPIO can be enabled. One or both edges may be of interest, and the edge of interest may change based on polarity of GPIO HPD wire. edge_falling = 3'b001: ddi0 falling edges enabled edge_falling = 3'b010: ddi1 falling edges enabled ... edge_falling = 3'b111: ddi2, ddi1 and ddi0 falling edges enabled
9:5	7h RW	**Deglitch (deglitch):** Deglitch time, in 60 us steps. HPD logic will ignore any pulses shorter than the deglitch time. A transition which is held longer than the deglitch time will be considered an edge, and will result in an HPD event, which may prevent S0ix entry or wake from S0ix and notify display controller. All settings have an error of +/- 1 tick (60 us). 4'd0: 000 us (invalid configuration) 5'd1: 60 us (invalid configuration) 5'd2: 120 us ... 5'd7: 420 us (default) ... 5'd31: 1.86 ms
4:0	10h RW	**Recent Edge Detect (edge_det_rcnt):** Recent event time, in 10 ms steps. HPD logic will hold a wire asserted for a programmable period of time after an enabled edge has been detected, in order to prevent S0ix entry for this period of time. All settings have an error of +/- 1 tick (10 ms). Default: 160 ms Max: 310 ms

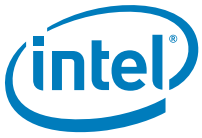
13.2.26 OBFF Control and Status (OBFF_CTL_STS)—Offset 10C8h

Through this register, BIOS controls the External OBFF feature through this register and, PMC indicates that it is currently processing an OBFF state change. The timing parameters for GPIO WAKE pin indication are also present in this register.
For the SoC, reset on cold boot, cold reset, warm reset, and Sx.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6450280Fh



Bit Range	Default & Access	Field Name (ID): Description
31:24	64h RW/L	**Tobff3 (Tobff3):** Minimum time between two consecutive state changes (to avoid misinterpretation of pattern). Programmable timer to control Tobff3. Timer counts 10 ns clock cycles. Tobff3(min) = 700 ns Default = 0x64 = 100 clocks = 1000 ns
23:16	50h RW/L	**Tobff2 (Tobff2):** Time between two falling WAKE# edges when signaling CPU Active. Programmable timer to control Tobff2. Timer counts 10 ns clock cycles. Tobff2(min) = 700 ns Tobff2(max) = 1000 ns Default = 0x50 = 80 clocks = 800 ns Note: Tobff2 must be programmed to a value at least 2x of Tobff1.
15:8	28h RW/L	**Tobff1 (Tobff1):** Minimum/Maximum WAKE# pulse width; applies to both active-inactive-active and inactive-active-inactive cases. Programmable timer to control Tobff1. Timer counts 10 ns clock cycles. Tobff1(min) = 300 ns Tobff1(max) = 500 ns Default = 0x28 = 40 clocks = 400 ns
7	0h RO/V	**PORT3 OBFF Status (PORT3_OBFF_STATUS):** OBFF Status: Indicates if PMC is currently processing an OBFF state change. ASL code will read this bit on RTD3 Entry to ensure no conflicts on WAKE# GPIO as part of RTD3 flows.
6	0h RO/V	**PORT2 OBFF Status (PORT2_OBFF_STATUS):** OBFF Status: Indicates if PMC is currently processing an OBFF state change. ASL code will read this bit on RTD3 Entry to ensure no conflicts on WAKE# GPIO as part of RTD3 flows.
5	0h RO/V	**PORT1 OBFF Status (PORT1_OBFF_STATUS):** OBFF Status: Indicates if PMC is currently processing an OBFF state change. ASL code will read this bit on RTD3 Entry to ensure no conflicts on WAKE# GPIO as part of RTD3 flows.
4	0h RO/V	**PORT0 OBFF Status (PORT0_OBFF_STATUS):** OBFF Status: Indicates if PMC is currently processing an OBFF state change. ASL code will read this bit on RTD3 Entry to ensure no conflicts on WAKE# GPIO as part of RTD3 flows.
3	1h RW/L	**PORT3 OBFF Disable (PORT3_OBFF_DISABLE):** OBFF Disable: When set, disables PMC from driving external OBFF signaling to the PCIe devices through the WAKE GPIO#.OBFF must only be driven to PCIe device when in D0. ASL code will provide this control by setting and clearing this bit on RTD3 Entry/ Exit FlowsIf set by BIOS the named function is exposed to the OS via ACPI

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/L	**PORT2 OBFF Disable (PORT2_OBFF_DISABLE):** OBFF Disable: When set, disables PMC from driving external OBFF signaling to the PCIe devices through the WAKE GPIO#.OBFF must only be driven to PCIe device when in D0. ASL code will provide this control by setting and clearing this bit on RTD3 Entry/ Exit FlowsIf set by BIOS the named function is exposed to the OS via ACPI
1	1h RW/L	**PORT1 OBFF Disable (PORT1_OBFF_DISABLE):** OBFF Disable: When set, disables PMC from driving external OBFF signaling to the PCIe devices through the WAKE GPIO#.OBFF must only be driven to PCIe device when in D0. ASL code will provide this control by setting and clearing this bit on RTD3 Entry/ Exit FlowsIf set by BIOS the named function is exposed to the OS via ACPI
0	1h RW/L	**PORT0 OBFF Disable (PORT0_OBFF_DISABLE):** OBFF Disable: When set, disables PMC from driving external OBFF signaling to the PCIe devices through the WAKE GPIO#.OBFF must only be driven to PCIe device when in D0. ASL code will provide this control by setting and clearing this bit on RTD3 Entry/ Exit FlowsIf set by BIOS the named function is exposed to the OS via ACPI

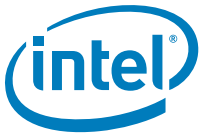
13.2.27 Lock Register (LOCK)—Offset 10CCh

Register | Field | Lock bit GEN_PMCON1 | PME_B0_S5_DIS | LOCK.Sx_WAKE]
GEN_PMCON1 | AG3E | LOCK.Sx_WAKE]
RSVD[GEN_PMCON2 | BIOS_PCI_EXP_EN | LOCK.PCIE]
GEN_PMCON2 | lpc_lpb_clk_ctrl | LOCK.lpc_lpb_clk_ctrl
GEN_PMCON3 | slp strch bits | LOCK.slpsx_str_pol_lock
PM_CFG | PWR_CYC_DUR | LOCK.slpsx_str_pol_lock
PM_CFG2 | pwrbtn_dis | LOCK.pwrbtn
IRQ_SEL_0 | all | LOCK.IRQ_SEL
IRQ_SEL_1 | all | LOCK.IRQ_SEL
IRQ_SEL_2 | all | LOCK.IRQ_SEL
CRID | all | LOCK.CRID
GEN_PMCON2 | PER_SMI_SEL | LOCK.PER_SMI
FUNC_DIS_0 | all | LOCK.FUNC_DIS
FUNC_DIS_1 | all | LOCK.FUNC_DIS
S0IX_WAKE_EN | all | LOCK.SOIX
ETR | MAX_S0IX | LOCK.SOIX
For the SoC, reset on cold boot, cold reset, warm reset, and Sx.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved (rsvd):** Reserved.
12	0h RW/L	**OBFF Lock (obff):** Locks GCR.OBFF_CTL_STS.Tobff1, Tobff2, Tobff3, PORT0_OBFF_DISABLE, PORT1_OBFF_DISABLE, PORT2_OBFF_DISABLE, PORT3_OBFF_DISABLE. This field is also self-locking.
11	0h RW/L	**Power Button Lock (pwrbtn):** Locks GCR.PMC_CFG2.pwrbtn_dis. This field is also self-locking.
10	0h RW/L	**LPC Loopback Clock Control Lock (lpc_lpb_clk_ctrl):** Locks GCR.GEN_PMCON2.lpc_lpb_clk_ctrl. This field is also self-locking.
9	0h RW/L	**ASLP Sx# Stretching Policy Lock-Down (slpsx_str_pol_lock):** When set to 1, this bit locks down the following fields: GEN_PMCON3.DIS_SLP_X_STRCH_SUSPF GEN_PMCON3.SLP_S3_MIN_ASST_WDTH GEN_PMCON3.S4MAW GEN_PMCON3.S4ASE PM_CFG.SLP_A_MIN_ASST_WDTH (if applicable) PM_CFG.SLP_LAN_MIN_ASST_WDTH (if applicable) PM_CFG.PWR_CYC_DUR Those bits become read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset. This lockdown bit is available in both desktop and mobile. Note: Relevant only for no PMIC mode.
8	0h RW/L	**IRQ Select Lock (irq_sel)**
7	0h RW/L	**CRID Lock (crid)**
6	0h RW/L	**SX Wake Lock (sx_wake)**
5	0h RO	**Reserved (rsvd_pcie):** Reserved: PCIE lock.
4	0h RW/L	**Periodic SMI Lock (per_smi)**
3	0h RW/L	**Func Dis Lock (func_dis)**
2	0h RW/L	**Reserved (s0ix):** Reserved.
1:0	0h RO	**Reserved (reserved1):** Reserved.

13.3 Registers Summary

IPC provides a general mechanism for interprocessor communication. IPC1 is used by the IA processor to send messages to the PMC.

Table 13-3. Summary of IPC Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	IPC Command (IPC_CMD)—Offset 0h	0h
4h	7h	IPC Status (IPC_STS)—Offset 4h	0h
8h	Bh	IPC Source Pointer (IPC_SPTR)—Offset 8h	0h
Ch	Fh	IPC Destination Pointer (IPC_DPTR)—Offset Ch	0h
80h	83h	IPC Write Buffer (IPC_WBUF0)—Offset 80h	0h
84h	87h	IPC Write Buffer (IPC_WBUF1)—Offset 84h	0h
88h	8Bh	IPC Write Buffer (IPC_WBUF2)—Offset 88h	0h
8Ch	8Fh	IPC Write Buffer (IPC_WBUF3)—Offset 8Ch	0h
90h	93h	IPC Read Buffer (IPC_RBUF0)—Offset 90h	0h
94h	97h	IPC Read Buffer (IPC_RBUF1)—Offset 94h	0h
98h	9Bh	IPC Read Buffer (IPC_RBUF2)—Offset 98h	0h
9Ch	9Fh	IPC Read Buffer (IPC_RBUF3)—Offset 9Ch	0h

13.3.1 IPC Command (IPC_CMD)—Offset 0h

The IPC CMD register is used for conveying the type of commands to the IPC block. This is a special kind of register and a write to this register always results in Interrupt to the ARC and Setting of the busy bit in the IPC_STS register. The setting of busy bit in the IPC_STS register results in blocking of all transaction from the IA host. The ARC FW is expected to read the IPC_CMD register, whenever interrupted, interpret it and follow the instructions as ordered by the IA host. The IA host may optionally prefer to be interrupted, when the command is complete by sending an MSI. When the ARC FW is done with the command, it is expected to update the IPC_STS register and clear the busy bit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Reserved (Reserved0):** Reserved.
23:16	0h RW	**Size (size):** Size of the transaction in bytes. This 8-bit field can potentially specify 256 Bytes, but the hardware based write_buffer and read_buffer are both only 16 bytes deep. So the size should not be greater than 16bytes for normal reads and normal write operation. However, larger sizes can be used for indirect operations.
15:12	0h RW	**Command ID (cmd_ID):** ID or Tag associated with this command. When the IPC command is completed, this value is copied in the IPC_STS register by the hardware.

Bit Range	Default & Access	Field Name (ID): Description
11:9	0h RW	**Reserved (rsvd):** Reserved.
8	0h RW	**MSI (msi):** Send an MSI once the command is executed.
7:0	0h RW	**Command (Command):** Following are defined commands: • 00h: Normal Write • 01h: Message Write • 02h: Indirect Read • 03h: Reserved • 04h: Read DMA • 05h: Indirect write • 06h: FFh - Reserved

13.3.2 IPC Status (IPC_STS)—Offset 4h

The IPC status register provides information related to the status of the IPC block and also some information related to the last executed command.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (rsvd):** Reserved.
23:16	0h RW/V	**Error Code (error_code):** If the err bit is set, this field may contain some error code. ARC FW is responsible for updating this value.
15:8	0h RO/V	**Initiator ID (Initiator_ID):** ID of the initiator, whose command was executed last. The initiator_ID information is available through the CONNID OCP. This bits are captured by the IPC hardware and placed in this field. This information could be used by the ARC FW to figure out the initiator for any particular IPC command and whether to service it or not. It may also be used for debug purpose, when the ARC FW is unable to service some IPC command and sets the error bit in the IPC_STC register.
7:4	0h RO/V	**Command ID (cmd_ID):** ID of the last command. The PMU Hardware copies this same field from the IPC_CMD register and places it in this reg.
3	0h RO/V	**Reserved (rsvd1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C/V	**IRQ (irq):** This bit is set when FW clears IPC_STS.Busy if IPC_CMD.msi is set.
1	0h RW/V	**Error (Error):** There was some error in executing the last command. This value is written by the ARC FW.
0	0h RW/V	**Busy (Busy):** IPC block is busy executing some command. When done, this bit would be unset. This bit is set, whenever the IPC hardware receives a new command on IPC_CMD register. ARC FW is responsible for unsetting this bit. For IPC2, the IPC hardware blocks any new transactions from cDMI, to the IPC block until this bit is cleared.

13.3.3 IPC Source Pointer (IPC_SPTR)—Offset 8h

This is a 32-bit register containing the address of the read transaction. The IPC Source Pointer Register is used by the IA host to perform indirect reads. The IA host would first write to this IPC_SPTR register and specify the read address location. Next, the IA host would issue an Indirect Read command on the IPC_CMD register. The ARC FW is responsible to decode this transaction and issue a read on the address specified by the IPC_SPTR register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Source Pointer (SPTR):** Read transaction source address.

13.3.4 IPC Destination Pointer (IPC_DPTR)—Offset Ch

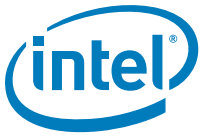
This register contains the destination address of indirect read or indirect write transaction. Please refer to IPC_CMD register for detailed usage of this register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Destination Pointer (DPTR):** Read or write transaction destination address.



13.3.5 IPC Write Buffer (IPC_WBUF0)—Offset 80h

The write buffer is 16 byte deep and is used by the IA host to write any data for ARC. This buffer is also used for writing Lincroft Msg and MsgD to system controller.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Write Buffer (WBUF)**

13.3.6 IPC Write Buffer (IPC_WBUF1)—Offset 84h

The write buffer is 16 byte deep and is used by the IA host to write any data for ARC. This buffer is also used for writing Lincroft Msg and MsgD to system controller.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Write Buffer (WBUF)**

13.3.7 IPC Write Buffer (IPC_WBUF2)—Offset 88h

The write buffer is 16 byte deep and is used by the IA host to write any data for ARC. This buffer is also used for writing Lincroft Msg and MsgD to system controller.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Write Buffer (WBUF)**

13.3.8 IPC Write Buffer (IPC_WBUF3)—Offset 8Ch

The write buffer is 16 byte deep and is used by the IA host to write any data for ARC. This buffer is also used for writing Lincroft Msg and MsgD to system controller.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Write Buffer (WBUF)**

13.3.9 IPC Read Buffer (IPC_RBUF0)—Offset 90h

This 16-byte deep read buffer is used by the IA host for gathering some data from the system controller. In the normal read mode, the IA host can ask the ARC to gather some information and store it in this IPC_RBUF buffer. Later on, the IA host can access this information.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Read Buffer (RBUF)**

13.3.10 IPC Read Buffer (IPC_RBUF1)—Offset 94h

This 16-byte deep read buffer is used by the IA host for gathering some data from the system controller. In the normal read mode, the IA host can ask the ARC to gather some information and store it in this IPC_RBUF buffer. Later on, the IA host can access this information.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Read Buffer (RBUF)**

13.3.11 IPC Read Buffer (IPC_RBUF2)—Offset 98h

This 16-byte deep read buffer is used by the IA host for gathering some data from the system controller. In the normal read mode, the IA host can ask the ARC to gather some information and store it in this IPC_RBUF buffer. Later on, the IA host can access this information.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Read Buffer (RBUF)**

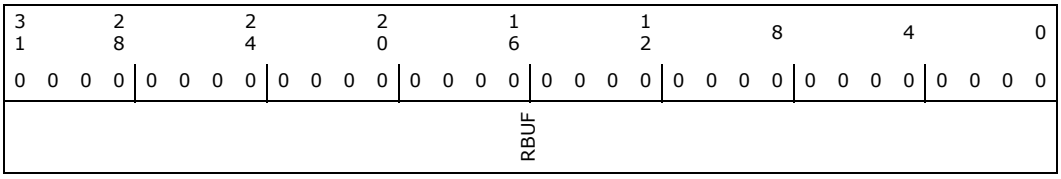
13.3.12 IPC Read Buffer (IPC_RBUF3)—Offset 9Ch

This 16-byte deep read buffer is used by the IA host for gathering some data from the system controller. In the normal read mode, the IA host can ask the ARC to gather some information and store it in this IPC_RBUF buffer. Later on, the IA host can access this information.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Read Buffer (RBUF)**

13.4 Registers Summary

Table 13-4. Summary of soc_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h	0h
4h	7h	STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h	0h
Ch	Fh	CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	0h
10h	13h	BAR -Base Address Register (BAR)—Offset 10h	0h
14h	17h	BAR -Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	BAR1 -Base Address Register1 (BAR1)—Offset 18h	0h
1Ch	1Fh	BAR1 -Base Address Register1 High (BAR1_HIGH)—Offset 1Ch	0h
20h	23h	(BAR2)—Offset 20h	0h
2Ch	2Fh	SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h	48030001h
84h	87h	PMECTRLSTATUS_type Power Management Control and status register (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI DEVICE IDLE CAPABILITY RECORD (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	DEVID VENDOR SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	D0I3_CONTROL_SW_LTR_MMIO_REG - SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	DEVICE_IDLE_POINTER_REG - Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	0h
A0h	A3h	D0I3_MAX_POW_LAT_PG_CONFIG - DEVICE PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	800h

13.4.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Device ID and Vendor ID provided by this register uniquely identifies the XXX Device

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V	**DEVICEID:** Device ID identifies the particular PCI device
15:0	0h RO/V	**VENDORID:** Vendor ID is a unique ID provided by the PCI SIG, which identifies the manufacturer of the device

13.4.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

Command register to programme interrupt disable , bus master enable, and Memory space enable. Status register to read the errors and aborts

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0:** Reserved 0
29	0h RW/1C/V	**RMA:** Received Master Abort
28	0h RW/1C/V	**RTA:** Received Target Abort
27:21	0h RO	**Reserved1:** Reserved
20	1h RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device
18:16	0h RO	**Reserved2:** Reserved
15:11	0h RO	**Reserved3:** Reserved
10	0h RW	**INTR_DISABLE:** Interrupt Disable
9	0h RO	**Reserved4:** Reserved
8	0h RW	**SERR_ENABLE:** SERR Enable , Not implemented
7:3	0h RO	**Reserved5:** Reserved
2	0h RW	**BME:** Bus Master Enable

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**MSE:** Memory Space Enable
0	0h RW/V	**IOSE:** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0. NOTE: This bit does not exist in the PMC IOSF2OCP bridge. It is shadowed in the PSF3 fabric. Using /V in AccessType so PMC cluster validation does not assume this bit will read back what was written.

13.4.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Revision ID register identifies revision of particular device and Class Code register is used to identify generic function of the device

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO/V	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface
7:0	0h RO/V	**RID:** Revision ID identifies the revision of particular PCI device.

13.4.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Cache Line size as RW with def 0, Latency timer RW with def 0, Header type with Type 0 configuration header and Reserved BIST register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**MULFNDEV:** Multi-Function Device
22:16	0h RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header
15:8	0h RO	**LATTIMER:** Latency Timer:. This register is implemented as R/W with default as 0
7:0	0h RW	**CACHELINE_SIZE:** Cacheline Size

13.4.5 BAR -Base Address Register (BAR)—Offset 10h

Base Address Register low [31:2] , type[2:1] in 32bit or 64bit addr range and memory space indicator [0]

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR:** Base Address Register Low, Base address of the OCP fabric memory space. Taken from Strap values as ones
11:4	0h RO	**SIZEINDICATOR:** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**TYPE:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range, If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE:** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

13.4.6 BAR -Base Address Register High (BAR_HIGH)—Offset 14h

Base Address Register High enabled if [2:1] of BAR_type_LOW is 10

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR_HIGH:** Base Address high - MSB

13.4.7 BAR1 -Base Address Register1 (BAR1)—Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K, type in [2:1] and memory space indicator in [0]

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR1:** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	0h RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0h RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0h RO	**TYPE1:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

13.4.8 BAR1 -Base Address Register1 High (BAR1_HIGH)—Offset 1Ch

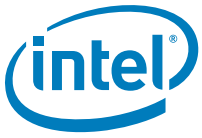
Base Address Register1 High enabled only if [2:1] of BAR1 register is 10

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR1_HIGH:** Base Address: Base address of the OCP fabric memory space. Taken from Strap values as ones



13.4.9 (BAR2)—Offset 20h

BAR -Base Address Register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**BASEADDR**
1	0h RO	**Reserved0**
0	0h RO	**MESSAGE_SPACE**

13.4.10 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID:** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0h RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

13.4.11 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address register is a RO indicates support for expansion ROMs

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE:** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

13.4.12 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Capabilities Pointer register indicates what the next capability is.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved0:** Reserved
7:0	80h RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is.

13.4.13 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

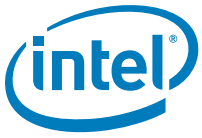
Interrupt line Register isn't used in Bridge directly, Interrupt Pin register reflects the IPIN value in private config space. Min_gnt register indicating the req of latency timers and max_lat register max latency

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT:** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**MIN_GNT:** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved0:** Reserved
11:8	1h RO	**INTPIN:** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**INTLINE:** Interrupt Line: It is used to communicate to software, the interrupt line to which the interrupt pin is connected

13.4.14 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

PowerManagement Capability ID register points to next capability structure and power mgmnt capability , with Power management capabilities register for PME support and version

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	9h RO	**PMESUPPORT:** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved0:** Reserved
18:16	3h RO	**VERSION:** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	0h RO	**NXTCAP:** Next Capability: Points to the next capability structure.
7:0	1h RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability

13.4.15 PMECTRLSTATUS_type Power Management Control and status register (PMECTRLSTATUS)—Offset 84h

power management control and status register to set and read PME status, PME enable, No Soft reset and power state

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**PMESTATUS:** PME Status
14:9	0h RO	**Reserved1:** Reserved
8	0h RW	**PMEENABLE:** PME Enable
7:4	0h RO	**Reserved2:** Reserved
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	**Reserved3:** Reserved
1:0	0h RW	**POWERSTATE:** Power State: This field is used both to determine the current power state and to set a new power state

13.4.16 PCI DEVICE IDLE CAPABILITY RECORD (PCIDEVIDLE_CAP_RECORD)—Offset 90h

PCI Device Vendor Specific Capability register defines Vendor specific Capability ID, revision , length , next capability and CAPID

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** Vendor Specific Capability ID
27:24	0h RO	**REVID:** Revision ID of capability structure
23:16	14h RO	**CAP_LENGTH:** Vendor Specific Capability Length
15:8	0h RO	**NEXT_CAP:** Next Capability
7:0	9h RO	**CAPID:** Capability ID

13.4.17 DEVID VENDOR SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)—Offset 94h

Extended Vendor capability register for VSEC Length, revision and ID

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH:** Vendor Specific Extended Capability Length
19:16	0h RO	**VSEC_REV:** Vendor specific Extended Capability revision
15:0	10h RO	**VSECID:** Vendor Specific Extended Capability ID

13.4.18 D0I3_CONTROL_SW_LTR_MMIO_REG - SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Software location pointer in MMIO space as an offset specified by BAR

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW_LAT_DWORD_OFFSET:** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW_LAT_BAR_NUM:** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW_LAT_VALID:** This value is reflected from the SW LTR valid strap at the top level

13.4.19 DEVICE_IDLE_POINTER_REG - Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location , BAR NUM and D0i3 Valid Strap

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**DWORD_OFFSET:** contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR
3:1	0h RO	**BAR_NUM:** Bar num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**VALID:** Valid: This value is reflected from the D0i3 valid strap at the top level.

13.4.20 D0I3_MAX_POW_LAT_PG_CONFIG - DEVICE PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

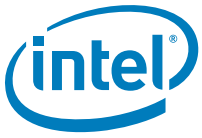
D0idle_Max_Power_On_Latency register set at boot and Power control enable register to enable communication with the PGCB block below the Bridge

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved0:** Reserved
21	0h RW	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved1:** Reserved
19	0h RW	**SLEEP_EN:** Sleep Enable
18	0h RW	**PGE:** DEVIDLE Enable (DEVIDLEN): If ?1?, then the function will power gate when idle and the DevIdle register (DevIdleC[2] = ?1?) is set.
17	0h RW	**I3_ENABLE:** D3-Hot Enable (D3HEN): If ?1?, then function will power gate when idle and the PMCSR[1:0] register in the function =?11? (D3).
16	0h RW	**PMCRE:** PMCRE: PMC Request Enable
15:13	0h RO	**Reserved2:** Reserved
12:10	2h RW/O	**POW_LAT_SCALE:** Power On Latency Scale
9:0	0h RW/O	**POW_LAT_VALUE:** Power On Latency value



13.5 Registers Summary

Table 13-5. Summary of soc_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h	A948086h
4h	7h	STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h	FF000000h
Ch	Fh	CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	0h
10h	13h	BAR -Base Address Register (BAR)—Offset 10h	0h
14h	17h	BAR -Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	BAR1 -Base Address Register1 (BAR1)—Offset 18h	0h
1Ch	1Fh	BAR1 -Base Address Register1 High (BAR1_HIGH)—Offset 1Ch	0h
20h	23h	(BAR2)—Offset 20h	0h
2Ch	2Fh	SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h	48030001h
84h	87h	PMECTRLSTATUS_type Power Management Control and status register (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI DEVICE IDLE CAPABILITY RECORD (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	DEVID VENDOR SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	D0I3_CONTROL_SW_LTR_MMIO_REG - SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	DEVICE_IDLE_POINTER_REG - Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	0h
A0h	A3h	D0I3_MAX_POW_LAT_PG_CONFIG - DEVICE PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	800h

13.5.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Device ID and Vendor ID provided by this register uniquely identifies the XXX Device

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: A948086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	A94h RO/V	**DEVICEID:** Device ID identifies the particular PCI device
15:0	8086h RO/V	**VENDORID:** Vendor ID is a unique ID provided by the PCI SIG, which identifies the manufacturer of the device

13.5.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

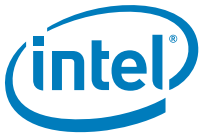
Command register to programme interrupt disable , bus master enable, and Memory space enable. Status register to read the errors and aborts

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0:** Reserved 0
29	0h RW/1C/V	**RMA:** Received Master Abort
28	0h RW/1C/V	**RTA:** Received Target Abort
27:21	0h RO	**Reserved1:** Reserved
20	1h RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device
18:16	0h RO	**Reserved2:** Reserved
15:11	0h RO	**Reserved3:** Reserved
10	0h RW	**INTR_DISABLE:** Interrupt Disable
9	0h RO	**Reserved4:** Reserved
8	0h RW	**SERR_ENABLE:** SERR Enable , Not implemented
7:3	0h RO	**Reserved5:** Reserved
2	0h RW	**BME:** Bus Master Enable



Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**MSE:** Memory Space Enable
0	0h RW/V	**IOSE:** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0. NOTE: This bit does not exist in the PMC IOSF2OCP bridge. It is shadowed in the PSF3 fabric. Using /V in AccessType so PMC cluster validation does not assume this bit will read back what was written.

13.5.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Revision ID register identifies revision of particular device and Class Code register is used to identify generic function of the device

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: FF000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	FF0000h RO/V	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface
7:0	0h RO/V	**RID:** Revision ID identifies the revision of particular PCI device.

13.5.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Cache Line size as RW with def 0, Latency timer RW with def 0, Header type with Type 0 configuration header and Reserved BIST register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**MULFNDEV:** Multi-Function Device
22:16	0h RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header
15:8	0h RO	**LATTIMER:** Latency Timer:. This register is implemented as R/W with default as 0
7:0	0h RW	**CACHELINE_SIZE:** Cacheline Size

13.5.5 BAR -Base Address Register (BAR)—Offset 10h

Base Address Register low [31:2] , type[2:1] in 32bit or 64bit addr range and memory space indicator [0]

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR:** Base Address Register Low, Base address of the OCP fabric memory space. Taken from Strap values as ones
11:4	0h RO	**SIZEINDICATOR:** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**TYPE:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range, If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE:** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

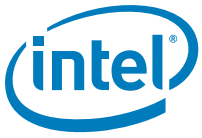
13.5.6 BAR -Base Address Register High (BAR_HIGH)—Offset 14h

Base Address Register High enabled if [2:1] of BAR_type_LOW is 10

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR_HIGH:** Base Address high - MSB

13.5.7 BAR1 -Base Address Register1 (BAR1)—Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K, type in [2:1] and memory space indicator in [0]

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR1:** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	0h RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0h RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0h RO	**TYPE1:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

13.5.8 BAR1 -Base Address Register1 High (BAR1_HIGH)—Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR1_HIGH:** Base Address: Base address of the OCP fabric memory space. Taken from Strap values as ones

13.5.9 (BAR2)—Offset 20h

BAR -Base Address Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**BASEADDR**
1	0h RO	**Reserved0**
0	0h RO	**MESSAGE_SPACE**

13.5.10 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 0h

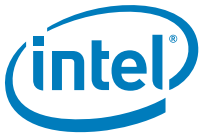
Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID:** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0h RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

13.5.11 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address register is a RO indicates support for expansion ROMs

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1



Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE:** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

13.5.12 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Capabilities Pointer register indicates what the next capability is.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved0:** Reserved
7:0	80h RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is.

13.5.13 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

Interrupt line Register isn't used in Bridge directly, Interrupt Pin register reflects the IPIN value in private config space. Min_gnt register indicating the req of latency timers and max_lat register max latency

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT:** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**MIN_GNT:** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved0:** Reserved
11:8	1h RO	**INTPIN:** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**INTLINE:** Interrupt Line: It is used to communicate to software, the interrupt line to which the interrupt pin is connected

13.5.14 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

PowerManagement Capability ID register points to next capability structure and power mgmnt capability , with Power management capabilities register for PME support and version

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	9h RO	**PMESUPPORT:** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved0:** Reserved
18:16	3h RO	**VERSION:** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	0h RO	**NXTCAP:** Next Capability: Points to the next capability structure.
7:0	1h RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability

13.5.15 PMECTRLSTATUS_type Power Management Control and status register (PMECTRLSTATUS)—Offset 84h

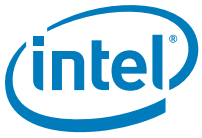
power management control and status register to set and read PME status, PME enable, No Soft reset and power state

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved0:** Reserved



Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**PMESTATUS:** PME Status
14:9	0h RO	**Reserved1:** Reserved
8	0h RW	**PMEENABLE:** PME Enable
7:4	0h RO	**Reserved2:** Reserved
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	**Reserved3:** Reserved
1:0	0h RW	**POWERSTATE:** Power State: This field is used both to determine the current power state and to set a new power state

13.5.16 PCI DEVICE IDLE CAPABILITY RECORD (PCIDEVIDLE_CAP_RECORD)—Offset 90h

PCI Device Vendor Specific Capability register defines Vendor specific Capability ID, revision , length , next capability and CAPID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** Vendor Specific Capability ID
27:24	0h RO	**REVID:** Revision ID of capability structure
23:16	14h RO	**CAP_LENGTH:** Vendor Specific Capability Length
15:8	0h RO	**NEXT_CAP:** Next Capability
7:0	9h RO	**CAPID:** Capability ID

13.5.17 DEVID VENDOR SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)—Offset 94h

Extended Vendor capability register for VSEC Length, revision and ID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH:** Vendor Specific Extended Capability Length
19:16	0h RO	**VSEC_REV:** Vendor specific Extended Capability revision
15:0	10h RO	**VSECID:** Vendor Specific Extended Capability ID

13.5.18 D0I3_CONTROL_SW_LTR_MMIO_REG - SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Software location pointer in MMIO space as an offset specified by BAR

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW_LAT_DWORD_OFFSET:** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW_LAT_BAR_NUM:** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW_LAT_VALID:** This value is reflected from the SW LTR valid strap at the top level

13.5.19 DEVICE_IDLE_POINTER_REG - Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location , BAR NUM and D0i3 Valid Strap

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**DWORD_OFFSET:** contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR
3:1	0h RO	**BAR_NUM:** Bar num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**VALID:** Valid: This value is reflected from the D0i3 valid strap at the top level.

13.5.20 D0I3_MAX_POW_LAT_PG_CONFIG - DEVICE PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

D0idle_Max_Power_On_Latency register set at boot and Power control enable register to enable communication with the PGCB block below the Bridge

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 1

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved0:** Reserved
21	0h RW	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved1:** Reserved
19	0h RW	**SLEEP_EN:** Sleep Enable
18	0h RW	**PGE:** DEVIDLE Enable (DEVIDLEN): If ?1?, then the function will power gate when idle and the DevIdle register (DevIdleC[2] = ?1?) is set.
17	0h RW	**I3_ENABLE:** D3-Hot Enable (D3HEN): If ?1?, then function will power gate when idle and the PMCSR[1:0] register in the function =?11? (D3).
16	0h RW	**PMCRE:** PMCRE: PMC Request Enable
15:13	0h RO	**Reserved2:** Reserved
12:10	2h RW/O	**POW_LAT_SCALE:** Power On Latency Scale
9:0	0h RW/O	**POW_LAT_VALUE:** Power On Latency value

13.6 Registers Summary

The Pulse Width Modulation block allows control of frequency and duty cycle of an output signal.

Table 13-6. Summary of Pulse Width Modulator Controller Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	PWM Control Register (PWMCTRL_0)—Offset 0h	400000h
100h	103h	PWM D0i3 Control Register (PWMD0i3C)—Offset 100h	8h
400h	403h	PWM Control Register (PWMCTRL_1)—Offset 400h	400000h
800h	803h	PWM Control Register (PWMCTRL_2)—Offset 800h	400000h
C00h	C03h	PWM Control Register (PWMCTRL_3)—Offset C00h	400000h

13.6.1 PWM Control Register (PWMCTRL_0)—Offset 0h

PWMCTRL controls the PWM and needs to be accessed in particular order to prevent any blips. Below is the recommended flow for programming the PWMCTRL registers. Initial Enable or First Activation:

- Program the Base Unit and On Time Divisor values.
- Set the Software Update Bit.
- Enable the PWM Output by setting PWM Enable.
- Repeat the above steps for the next PWM Module.

Dynamic update while PWM is Enabled:

- Program the Base Unit and On Time Divisor values.
- Set the Software Update Bit.
- Repeat the above steps for the next PWM module.

PWM output frequency = 19.2MHz * (Base_Unit / 256)

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 400000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable (ENABLE):** Enable PWM output.
30	0h RW/V	**Software Update (SW_UPDATE):** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the Base Unit (Integer or Fraction) On-time Divisor. The PWM module will apply the new settings at the end of the current cycle and clear this bit.

Bit Range	Default & Access	Field Name (ID): Description
29:22	1h RW	**Base Unit Integer (BASE_UNIT_INT):** Integer portion of Base Unit (Unsigned 8 integer bits and 14 fraction bits). Base_Unit = base_unit_int + (base_unit_frac / 16384)
21:8	0h RW	**Base Unit Frac (BASE_UNIT_FRAC):** Fractional portion of Base Unit (Unsigned 8 integer bits and 14 fraction bits). Base Unit = base_unit_int + (base_unit_frac / 16384)
7:0	0h RW	**On Time Divisor (ON_TIME_DIVISOR):** The On-time Divisor determines the PWM duty cycle. It is the number used to compare with the output of the base_unit counter.

13.6.2 PWM D0i3 Control Register (PWMD0i3C)—Offset 100h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (Rsvd):** Reserved.
3	1h RW/1C/V	**Restore Required (rr)**
2	0h RW	**D0i3 (i3)**
1	0h RO	**Interrupt Request (ir)**
0	0h RO/V	**Command in Progress (cip):** Set on a transition of i3.

13.6.3 PWM Control Register (PWMCTRL_1)—Offset 400h

PWMCTRL controls the PWM and needs to be accessed in particular order to prevent any blips. Below is the recommended flow for programming the PWMCTRL registers. Initial Enable or First Activation:

- Program the Base Unit and On Time Divisor values.
- Set the Software Update Bit.
- Enable the PWM Output by setting PWM Enable.
- Repeat the above steps for the next PWM Module.

Dynamic update while PWM is Enabled:

- Program the Base Unit and On Time Divisor values.
- Set the Software Update Bit.
- Repeat the above steps for the next PWM module.

PWM output frequency = 19.2MHz * (Base_Unit / 256p)

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 400000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable (ENABLE):** Enable PWM output.
30	0h RW/V	**Software Update (SW_UPDATE):** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the Base Unit (Integer or Fraction) On-time Divisor. The PWM module will apply the new settings at the end of the current cycle and clear this bit.
29:22	1h RW	**Base Unit Integer (BASE_UNIT_INT):** Integer portion of Base Unit (Unsigned 8 integer bits and 14 fraction bits). Base_Unit = base_unit_int + (base_unit_frac / 16384)
21:8	0h RW	**Base Unit Frac (BASE_UNIT_FRAC):** Fractional portion of Base Unit (Unsigned 8 integer bits and 14 fraction bits). Base Unit = base_unit_int + (base_unit_frac / 16384)
7:0	0h RW	**On Time Divisor (ON_TIME_DIVISOR):** The On-time Divisor determines the PWM duty cycle. It is the number used to compare with the output of the base_unit counter.

13.6.4 PWM Control Register (PWMCTRL_2)—Offset 800h

PWMCTRL controls the PWM and needs to be accessed in particular order to prevent any blips. Below is the recommended flow for programming the PWMCTRL registers. Initial Enable or First Activation:

- Program the Base Unit and On Time Divisor values.
- Set the Software Update Bit.
- Enable the PWM Output by setting PWM Enable.
- Repeat the above steps for the next PWM Module.

Dynamic update while PWM is Enabled:

- Program the Base Unit and On Time Divisor values.
- Set the Software Update Bit.
- Repeat the above steps for the next PWM module.

PWM output frequency = 19.2MHz * (Base_Unit / 2p56)

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 400000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable (ENABLE):** Enable PWM output.
30	0h RW/V	**Software Update (SW_UPDATE):** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the Base Unit (Integer or Fraction) On-time Divisor. The PWM module will apply the new settings at the end of the current cycle and clear this bit.
29:22	1h RW	**Base Unit Integer (BASE_UNIT_INT):** Integer portion of Base Unit (Unsigned 8 integer bits and 14 fraction bits). Base_Unit = base_unit_int + (base_unit_frac / 16384)
21:8	0h RW	**Base Unit Frac (BASE_UNIT_FRAC):** Fractional portion of Base Unit (Unsigned 8 integer bits and 14 fraction bits). Base Unit = base_unit_int + (base_unit_frac / 16384)
7:0	0h RW	**On Time Divisor (ON_TIME_DIVISOR):** The On-time Divisor determines the PWM duty cycle. It is the number used to compare with the output of the base_unit counter.

13.6.5 PWM Control Register (PWMCTRL_3)—Offset C00h

PWMCTRL controls the PWM and needs to be accessed in particular order to prevent any blips. Below is the recommended flow for programming the PWMCTRL registers. Initial Enable or First Activation:

- Program the Base Unit and On Time Divisor values.
- Set the Software Update Bit.
- Enable the PWM Output by setting PWM Enable.
- Repeat the above steps for the next PWM Module.

Dynamic update while PWM is Enabled:

- Program the Base Unit and On Time Divisor values.
- Set the Software Update Bit.
- Repeat the above steps for the next PWM module.

PWM output frequency = 19.2MHz * (Base_Unit /p 256)

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 400000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable (ENABLE):** Enable PWM output.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW/V	**Software Update (SW_UPDATE):** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the Base Unit (Integer or Fraction) On-time Divisor. The PWM module will apply the new settings at the end of the current cycle and clear this bit.
29:22	1h RW	**Base Unit Integer (BASE_UNIT_INT):** Integer portion of Base Unit (Unsigned 8 integer bits and 14 fraction bits). Base_Unit = base_unit_int + (base_unit_frac / 16384)
21:8	0h RW	**Base Unit Frac (BASE_UNIT_FRAC):** Fractional portion of Base Unit (Unsigned 8 integer bits and 14 fraction bits). Base Unit = base_unit_int + (base_unit_frac / 16384)
7:0	0h RW	**On Time Divisor (ON_TIME_DIVISOR):** The On-time Divisor determines the PWM duty cycle. It is the number used to compare with the output of the base_unit counter.

13.7 Registers Summary

Table 13-7. Summary of soc_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h	0h
4h	7h	STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h	0h
Ch	Fh	CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	0h
10h	13h	BAR -Base Address Register (BAR)—Offset 10h	0h
14h	17h	BAR -Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	BAR1 -Base Address Register1 (BAR1)—Offset 18h	0h
1Ch	1Fh	BAR1 -Base Address Register1 High (BAR1_HIGH)—Offset 1Ch	0h
20h	23h	(BAR2)—Offset 20h	0h
2Ch	2Fh	SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h	48030001h
84h	87h	PMECTRLSTATUS_type Power Management Control and status register (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI DEVICE IDLE CAPABILITY RECORD (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	DEVID VENDOR SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h

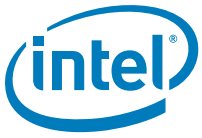


Table 13-7. Summary of soc_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
98h	9Bh	D0I3_CONTROL_SW_LTR_MMIO_REG - SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	DEVICE_IDLE_POINTER_REG - Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	0h
A0h	A3h	D0I3_MAX_POW_LAT_PG_CONFIG - DEVICE PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	800h

13.7.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Device ID and Vendor ID provided by this register uniquely identifies the XXX Device

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V	**DEVICEID:** Device ID identifies the particular PCI device
15:0	0h RO/V	**VENDORID:** Vendor ID is a unique ID provided by the PCI SIG, which identifies the manufacturer of the device

13.7.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

Command register to programme interrupt disable , bus master enable, and Memory space enable. Status register to read the errors and aborts

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0:** Reserved 0
29	0h RW/1C/V	**RMA:** Received Master Abort
28	0h RW/1C/V	**RTA:** Received Target Abort

Bit Range	Default & Access	Field Name (ID): Description
27:21	0h RO	**Reserved1:** Reserved
20	1h RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device
18:16	0h RO	**Reserved2:** Reserved
15:11	0h RO	**Reserved3:** Reserved
10	0h RW	**INTR_DISABLE:** Interrupt Disable
9	0h RO	**Reserved4:** Reserved
8	0h RW	**SERR_ENABLE:** SERR Enable , Not implemented
7:3	0h RO	**Reserved5:** Reserved
2	0h RW	**BME:** Bus Master Enable
1	0h RW	**MSE:** Memory Space Enable
0	0h RW/V	**IOSE:** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0. NOTE: This bit does not exist in the PMC IOSF2OCP bridge. It is shadowed in the PSF3 fabric. Using /V in AccessType so PMC cluster validation does not assume this bit will read back what was written.

13.7.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Revision ID register identifies revision of particular device and Class Code register is used to identify generic function of the device

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO/V	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO/V	**RID:** Revision ID identifies the revision of particular PCI device.

13.7.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Cache Line size as RW with def 0, Latency timer RW with def 0, Header type with Type 0 configuration header and Reserved BIST register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved0:** Reserved
23	0h RO	**MULFNDEV:** Multi-Function Device
22:16	0h RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header
15:8	0h RO	**LATTIMER:** Latency Timer:. This register is implemented as R/W with default as 0
7:0	0h RW	**CACHELINE_SIZE:** Cacheline Size

13.7.5 BAR -Base Address Register (BAR)—Offset 10h

Base Address Register low [31:2] , type[2:1] in 32bit or 64bit addr range and memory space indicator [0]

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR:** Base Address Register Low, Base address of the OCP fabric memory space. Taken from Strap values as ones
11:4	0h RO	**SIZEINDICATOR:** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**TYPE:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range, If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE:** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

13.7.6 BAR -Base Address Register High (BAR_HIGH)—Offset 14h

Base Address Register High enabled if [2:1] of BAR_type_LOW is 10

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR_HIGH:** Base Address high - MSB

13.7.7 BAR1 -Base Address Register1 (BAR1)—Offset 18h

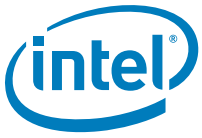
Base Address Register1 accesses to PCI configuration space and is always 4K, type in [2:1] and memory space indicator in [0]

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR1:** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	0h RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0h RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0h RO	**TYPE1:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range



Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

13.7.8 BAR1 -Base Address Register1 High (BAR1_HIGH)—Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR1_HIGH:** Base Address: Base address of the OCP fabric memory space. Taken from Strap values as ones

13.7.9 (BAR2)—Offset 20h

BAR -Base Address Register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**BASEADDR**
1	0h RO	**Reserved0**
0	0h RO	**MESSAGE_SPACE**

13.7.10 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID:** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0h RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

13.7.11 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address register is a RO indicates support for expansion ROMs

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE:** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

13.7.12 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

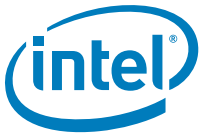
Capabilities Pointer register indicates what the next capability is

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved0:** Reserved
7:0	80h RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is.



13.7.13 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

Interrupt line Register is not used in Bridge directly, Interrupt Pin register reflects the IPIN value in private config space. Min_gnt register indicating the req of latency timers and max_lat register max latency.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT:** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**MIN_GNT:** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved0:** Reserved
11:8	1h RO	**INTPIN:** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0h RW	**INTLINE:** Interrupt Line: It is used to communicate to software, the interrupt line to which the interrupt pin is connected

13.7.14 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

PowerManagement Capability ID register points to next capability structure and power mgmnt capability , with Power management capabilities register for PME support and version

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	9h RO	**PMESUPPORT:** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved0:** Reserved
18:16	3h RO	**VERSION:** Indicates support for Revision 1.2 of the PCI Power Management Specification

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**NXTCAP:** Next Capability: Points to the next capability structure.
7:0	1h RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability

13.7.15 PMECTRLSTATUS_type Power Management Control and status register (PMECTRLSTATUS)—Offset 84h

power management control and status register to set and read PME status, PME enable, No Soft reset and power state

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved0:** Reserved
15	0h RW/1C/V	**PMESTATUS:** PME Status
14:9	0h RO	**Reserved1:** Reserved
8	0h RW	**PMEENABLE:** PME Enable
7:4	0h RO	**Reserved2:** Reserved
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	**Reserved3:** Reserved
1:0	0h RW	**POWERSTATE:** Power State: This field is used both to determine the current power state and to set a new power state

13.7.16 PCI DEVICE IDLE CAPABILITY RECORD (PCIDEVIDLE_CAP_RECORD)—Offset 90h

PCI Device Vendor Specific Capability register defines Vendor specific Capability ID, revision , length , next capability and CAPID

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** Vendor Specific Capability ID
27:24	0h RO	**REVID:** Revision ID of capability structure
23:16	14h RO	**CAP_LENGTH:** Vendor Specific Capability Length
15:8	0h RO	**NEXT_CAP:** Next Capability
7:0	9h RO	**CAPID:** Capability ID

13.7.17 DEVID VENDOR SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)—Offset 94h

Extended Vendor capability register for VSEC Length, revision and ID

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH:** Vendor Specific Extended Capability Length
19:16	0h RO	**VSEC_REV:** Vendor specific Extended Capability revision
15:0	10h RO	**VSECID:** Vendor Specific Extended Capability ID

13.7.18 D0I3_CONTROL_SW_LTR_MMIO_REG - SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Software location pointer in MMIO space as an offset specified by BAR

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW_LAT_DWORD_OFFSET:** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW_LAT_BAR_NUM:** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW_LAT_VALID:** This value is reflected from the SW LTR valid strap at the top level

13.7.19 DEVICE_IDLE_POINTER_REG - Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location , BAR NUM and D0i3 Valid Strap

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**DWORD_OFFSET:** contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR
3:1	0h RO	**BAR_NUM:** Bar num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**VALID:** Valid: This value is reflected from the D0i3 valid strap at the top level.

13.7.20 D0I3_MAX_POW_LAT_PG_CONFIG - DEVICE PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

D0idle_Max_Power_On_Latency register set at boot and Power control enable register to enable communication with the PGCB block below the Bridge

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved1:** Reserved
19	0h RW	**SLEEP_EN:** Sleep Enable
18	0h RW	**PGE:** DEVIDLE Enable (DEVIDLEN): If ?1?, then the function will power gate when idle and the DevIdle register (DevIdleC[2] = ?1?) is set.
17	0h RW	**I3_ENABLE:** D3-Hot Enable (D3HEN): If ?1?, then function will power gate when idle and the PMCSR[1:0] register in the function =?11? (D3).
16	0h RW	**PMCRE:** PMCRE: PMC Request Enable
15:13	0h RO	**Reserved2:** Reserved
12:10	2h RW/O	**POW_LAT_SCALE:** Power On Latency Scale
9:0	0h RW/O	**POW_LAT_VALUE:** Power On Latency value

13.8 Registers Summary

Table 13-8. Summary of soc_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h	AC88086h
4h	7h	STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h	C800000h
Ch	Fh	CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	0h
10h	13h	BAR -Base Address Register (BAR)—Offset 10h	0h
14h	17h	BAR -Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	BAR1 -Base Address Register1 (BAR1)—Offset 18h	0h
1Ch	1Fh	BAR1 -Base Address Register1 High (BAR1_HIGH)—Offset 1Ch	0h
20h	23h	(BAR2)—Offset 20h	0h
2Ch	2Fh	SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h	48030001h

Table 13-8. Summary of soc_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
84h	87h	PMECTRLSTATUS_type Power Management Control and status register (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI DEVICE IDLE CAPABILITY RECORD (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	DEVID VENDOR SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	D0I3_CONTROL_SW_LTR_MMIO_REG - SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	DEVICE_IDLE_POINTER_REG - Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	0h
A0h	A3h	D0I3_MAX_POW_LAT_PG_CONFIG - DEVICE PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	800h

13.8.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Device ID and Vendor ID provided by this register uniquely identifies the XXX Device

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: AC88086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	AC8h RO/V	**DEVICEID:** Device ID identifies the particular PCI device
15:0	8086h RO/V	**VENDORID:** Vendor ID is a unique ID provided by the PCI SIG, which identifies the manufacturer of the device

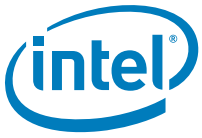
13.8.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

Command register to programme interrupt disable , bus master enable, and Memory space enable. Status register to read the errors and aborts

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0:** Reserved 0
29	0h RW/1C/V	**RMA:** Received Master Abort
28	0h RW/1C/V	**RTA:** Received Target Abort
27:21	0h RO	**Reserved1:** Reserved
20	1h RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device
18:16	0h RO	**Reserved2:** Reserved
15:11	0h RO	**Reserved3:** Reserved
10	0h RW	**INTR_DISABLE:** Interrupt Disable
9	0h RO	**Reserved4:** Reserved
8	0h RW	**SERR_ENABLE:** SERR Enable , Not implemented
7:3	0h RO	**Reserved5:** Reserved
2	0h RW	**BME:** Bus Master Enable
1	0h RW	**MSE:** Memory Space Enable
0	0h RW/V	**IOSE:** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0. NOTE: This bit does not exist in the PMC IOSF2OCP bridge. It is shadowed in the PSF3 fabric. Using /V in AccessType so PMC cluster validation does not assume this bit will read back what was written.

13.8.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Revision ID register identifies revision of particular device and Class Code register is used to identify generic function of the device

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: C800000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	C8000h RO/V	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface
7:0	0h RO/V	**RID:** Revision ID identifies the revision of particular PCI device.

13.8.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Cache Line size as RW with def 0, Latency timer RW with def 0, Header type with Type 0 configuration header and Reserved BIST register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved0:** Reserved
23	0h RO	**MULFNDEV:** Multi-Function Device
22:16	0h RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header
15:8	0h RO	**LATTIMER:** Latency Timer:. This register is implemented as R/W with default as 0
7:0	0h RW	**CACHELINE_SIZE:** Cacheline Size

13.8.5 BAR -Base Address Register (BAR)—Offset 10h

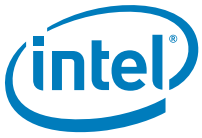
Base Address Register low [31:2] , type[2:1] in 32bit or 64bit addr range and memory space indicator [0]

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR:** Base Address Register Low, Base address of the OCP fabric memory space. Taken from Strap values as ones



Bit Range	Default & Access	Field Name (ID): Description
11:4	0h RO	**SIZEINDICATOR:** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**TYPE:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range, If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE:** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

13.8.6 BAR -Base Address Register High (BAR_HIGH)—Offset 14h

Base Address Register High enabled if [2:1] of BAR_type_LOW is 10

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR_HIGH:** Base Address high - MSB

13.8.7 BAR1 -Base Address Register1 (BAR1)—Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K, type in [2:1] and memory space indicator in [0]

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR1:** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	0h RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0h RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not prefetchable.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0h RO	**TYPE1:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

13.8.8 BAR1 -Base Address Register1 High (BAR1_HIGH)—Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR1_HIGH:** Base Address: Base address of the OCP fabric memory space. Taken from Strap values as ones

13.8.9 (BAR2)—Offset 20h

BAR -Base Address Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**BASEADDR**
1	0h RO	**Reserved0**
0	0h RO	**MESSAGE_SPACE**

13.8.10 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID:** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0h RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

13.8.11 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address register is a RO indicates support for expansion ROMs

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE:** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

13.8.12 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Capabilities Pointer register indicates what the next capability is

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved0:** Reserved
7:0	80h RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is.

13.8.13 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

Interrupt line Register isn't used in Bridge directly, Interrupt Pin register reflects the IPIN value in private config space. Min_gnt register indicating the req of latency timers and max_lat register max latency

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT:** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**MIN_GNT:** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved0:** Reserved
11:8	1h RO	**INTPIN:** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0h RW	**INTLINE:** Interrupt Line: It is used to communicate to software, the interrupt line to which the interrupt pin is connected

13.8.14 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

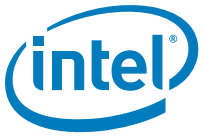
PowerManagement Capability ID register points to next capability structure and power mgmnt capability , with Power management capabilities register for PME support and version

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	9h RO	**PMESUPPORT:** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved0:** Reserved
18:16	3h RO	**VERSION:** Indicates support for Revision 1.2 of the PCI Power Management Specification



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**NXTCAP:** Next Capability: Points to the next capability structure.
7:0	1h RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability

13.8.15 PMECTRLSTATUS_type Power Management Control and status register (PMECTRLSTATUS)—Offset 84h

power management control and status register to set and read PME status, PME enable, No Soft reset and power state

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved0:** Reserved
15	0h RW/1C/V	**PMESTATUS:** PME Status
14:9	0h RO	**Reserved1:** Reserved
8	0h RW	**PMEENABLE:** PME Enable
7:4	0h RO	**Reserved2:** Reserved
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	**Reserved3:** Reserved
1:0	0h RW	**POWERSTATE:** Power State: This field is used both to determine the current power state and to set a new power state

13.8.16 PCI DEVICE IDLE CAPABILITY RECORD (PCIDEVIDLE_CAP_RECORD)—Offset 90h

PCI Device Vendor Specific Capability register defines Vendor specific Capability ID, revision , length , next capability and CAPID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** Vendor Specific Capability ID
27:24	0h RO	**REVID:** Revision ID of capability structure
23:16	14h RO	**CAP_LENGTH:** Vendor Specific Capability Length
15:8	0h RO	**NEXT_CAP:** Next Capability
7:0	9h RO	**CAPID:** Capability ID

13.8.17 DEVID VENDOR SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)—Offset 94h

Extended Vendor capability register for VSEC Length, revision and ID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH:** Vendor Specific Extended Capability Length
19:16	0h RO	**VSEC_REV:** Vendor specific Extended Capability revision
15:0	10h RO	**VSECID:** Vendor Specific Extended Capability ID

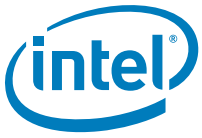
13.8.18 D0I3_CONTROL_SW_LTR_MMIO_REG - SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Software location pointer in MMIO space as an offset specified by BAR

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW_LAT_DWORD_OFFSET:** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW_LAT_BAR_NUM:** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW_LAT_VALID:** This value is reflected from the SW LTR valid strap at the top level

13.8.19 DEVICE_IDLE_POINTER_REG - Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location , BAR NUM and D0i3 Valid Strap

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**DWORD_OFFSET:** contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR
3:1	0h RO	**BAR_NUM:** Bar num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**VALID:** Valid: This value is reflected from the D0i3 valid strap at the top level.

13.8.20 D0I3_MAX_POW_LAT_PG_CONFIG - DEVICE PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

D0idle_Max_Power_On_Latency register set at boot and Power control enable register to enable communication with the PGCB block below the Bridge

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 26 **Function:** 0

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved1:** Reserved
19	0h RW	**SLEEP_EN:** Sleep Enable
18	0h RW	**PGE:** DEVIDLE Enable (DEVIDLEN): If ?1?, then the function will power gate when idle and the DevIdle register (DevIdleC[2] = ?1?) is set.
17	0h RW	**I3_ENABLE:** D3-Hot Enable (D3HEN): If ?1?, then function will power gate when idle and the PMCSR[1:0] register in the function =?11? (D3).
16	0h RW	**PMCRE:** PMCRE: PMC Request Enable
15:13	0h RO	**Reserved2:** Reserved
12:10	2h RW/O	**POW_LAT_SCALE:** Power On Latency Scale
9:0	0h RW/O	**POW_LAT_VALUE:** Power On Latency value

13.9 Registers Summary

Table 13-9. Summary of soc_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h	0h
4h	7h	STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h	0h
Ch	Fh	CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	0h
10h	13h	BAR -Base Address Register (BAR)—Offset 10h	0h
14h	17h	BAR -Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	BAR1 -Base Address Register1 (BAR1)—Offset 18h	0h
1Ch	1Fh	BAR1 -Base Address Register1 High (BAR1_HIGH)—Offset 1Ch	0h
20h	23h	(BAR2)—Offset 20h	0h
2Ch	2Fh	SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h	48030001h

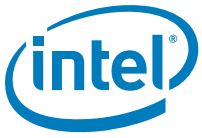


Table 13-9. Summary of soc_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
84h	87h	PMECTRLSTATUS_type Power Management Control and status register (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI DEVICE IDLE CAPABILITY RECORD (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	DEVID VENDOR SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	D0I3_CONTROL_SW_LTR_MMIO_REG - SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	DEVICE_IDLE_POINTER_REG - Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	0h
A0h	A3h	D0I3_MAX_POW_LAT_PG_CONFIG - DEVICE PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	800h

13.9.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Device ID and Vendor ID provided by this register uniquely identifies the XXX Device

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V	**DEVICEID:** Device ID identifies the particular PCI device
15:0	0h RO/V	**VENDORID:** Vendor ID is a unique ID provided by the PCI SIG, which identifies the manufacturer of the device

13.9.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

Command register to programme interrupt disable , bus master enable, and Memory space enable. Status register to read the errors and aborts

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0:** Reserved 0
29	0h RW/1C/V	**RMA:** Received Master Abort
28	0h RW/1C/V	**RTA:** Received Target Abort
27:21	0h RO	**Reserved1:** Reserved
20	1h RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device
18:16	0h RO	**Reserved2:** Reserved
15:11	0h RO	**Reserved3:** Reserved
10	0h RW	**INTR_DISABLE:** Interrupt Disable
9	0h RO	**Reserved4:** Reserved
8	0h RW	**SERR_ENABLE:** SERR Enable , Not implemented
7:3	0h RO	**Reserved5:** Reserved
2	0h RW	**BME:** Bus Master Enable
1	0h RW	**MSE:** Memory Space Enable
0	0h RW/V	**IOSE:** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0. NOTE: This bit does not exist in the PMC IOSF2OCP bridge. It is shadowed in the PSF3 fabric. Using /V in AccessType so PMC cluster validation does not assume this bit will read back what was written.

13.9.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Revision ID register identifies revision of particular device and Class Code register is used to identify generic function of the device

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO/V	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface
7:0	0h RO/V	**RID:** Revision ID identifies the revision of particular PCI device.

13.9.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Cache Line size as RW with def 0, Latency timer RW with def 0, Header type with Type 0 configuration header and Reserved BIST register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved0:** Reserved
23	0h RO	**MULFNDEV:** Multi-Function Device
22:16	0h RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header
15:8	0h RO	**LATTIMER:** Latency Timer:. This register is implemented as R/W with default as 0
7:0	0h RW	**CACHELINE_SIZE:** Cacheline Size

13.9.5 BAR -Base Address Register (BAR)—Offset 10h

Base Address Register low [31:2] , type[2:1] in 32bit or 64bit addr range and memory space indicator [0]

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR:** Base Address Register Low, Base address of the OCP fabric memory space. Taken from Strap values as ones

Bit Range	Default & Access	Field Name (ID): Description
11:4	0h RO	**SIZEINDICATOR:** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**TYPE:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range, If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE:** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

13.9.6 BAR -Base Address Register High (BAR_HIGH)—Offset 14h

Base Address Register High enabled if [2:1] of BAR_type_LOW is 10

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR_HIGH:** Base Address high - MSB

13.9.7 BAR1 -Base Address Register1 (BAR1)—Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K, type in [2:1] and memory space indicator in [0]

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR1:** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	0h RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0h RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not prefetchable.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0h RO	**TYPE1:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

13.9.8 BAR1 -Base Address Register1 High (BAR1_HIGH)—Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR1_HIGH:** Base Address: Base address of the OCP fabric memory space. Taken from Strap values as ones

13.9.9 (BAR2)—Offset 20h

BAR -Base Address Register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**BASEADDR**
1	0h RO	**Reserved0**
0	0h RO	**MESSAGE_SPACE**

13.9.10 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID:** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0h RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

13.9.11 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address register is a RO indicates support for expansion ROMs

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE:** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

13.9.12 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

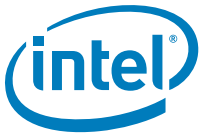
Capabilities Pointer register indicates what the next capability is

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved0:** Reserved
7:0	80h RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is.



13.9.13 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

Interrupt line Register isn't used in Bridge directly, Interrupt Pin register reflects the IPIN value in private config space. Min_gnt register indicating the req of latency timers and max_lat register max latency

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT:** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**MIN_GNT:** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved0:** Reserved
11:8	1h RO	**INTPIN:** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0h RW	**INTLINE:** Interrupt Line: It is used to communicate to software, the interrupt line to which the interrupt pin is connected

13.9.14 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

PowerManagement Capability ID register points to next capability structure and power mgmnt capability , with Power management capabilities register for PME support and version

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	9h RO	**PMESUPPORT:** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved0:** Reserved
18:16	3h RO	**VERSION:** Indicates support for Revision 1.2 of the PCI Power Management Specification

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**NXTCAP:** Next Capability: Points to the next capability structure.
7:0	1h RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability

13.9.15 PMECTRLSTATUS_type Power Management Control and status register (PMECTRLSTATUS)—Offset 84h

power management control and status register to set and read PME status, PME enable, No Soft reset and power state

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved0:** Reserved
15	0h RW/1C/V	**PMESTATUS:** PME Status
14:9	0h RO	**Reserved1:** Reserved
8	0h RW	**PMEENABLE:** PME Enable
7:4	0h RO	**Reserved2:** Reserved
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	**Reserved3:** Reserved
1:0	0h RW	**POWERSTATE:** Power State: This field is used both to determine the current power state and to set a new power state

13.9.16 PCI DEVICE IDLE CAPABILITY RECORD (PCIDEVIDLE_CAP_RECORD)—Offset 90h

PCI Device Vendor Specific Capability register defines Vendor specific Capability ID, revision , length , next capability and CAPID

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** Vendor Specific Capability ID
27:24	0h RO	**REVID:** Revision ID of capability structure
23:16	14h RO	**CAP_LENGTH:** Vendor Specific Capability Length
15:8	0h RO	**NEXT_CAP:** Next Capability
7:0	9h RO	**CAPID:** Capability ID

13.9.17 DEVID VENDOR SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)—Offset 94h

Extended Vendor capability register for VSEC Length, revision and ID

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH:** Vendor Specific Extended Capability Length
19:16	0h RO	**VSEC_REV:** Vendor specific Extended Capability revision
15:0	10h RO	**VSECID:** Vendor Specific Extended Capability ID

13.9.18 D0I3_CONTROL_SW_LTR_MMIO_REG - SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Software location pointer in MMIO space as an offset specified by BAR

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW_LAT_DWORD_OFFSET:** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW_LAT_BAR_NUM:** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW_LAT_VALID:** This value is reflected from the SW LTR valid strap at the top level

13.9.19 DEVICE_IDLE_POINTER_REG - Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location , BAR NUM and D0i3 Valid Strap

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**DWORD_OFFSET:** contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR
3:1	0h RO	**BAR_NUM:** Bar num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**VALID:** Valid: This value is reflected from the D0i3 valid strap at the top level.

13.9.20 D0I3_MAX_POW_LAT_PG_CONFIG - DEVICE PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

D0idle_Max_Power_On_Latency register set at boot and Power control enable register to enable communication with the PGCB block below the Bridge

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved1:** Reserved
19	0h RW	**SLEEP_EN:** Sleep Enable
18	0h RW	**PGE:** DEVIDLE Enable (DEVIDLEN): If ?1?, then the function will power gate when idle and the DevIdle register (DevIdleC[2] = ?1?) is set.
17	0h RW	**I3_ENABLE:** D3-Hot Enable (D3HEN): If ?1?, then function will power gate when idle and the PMCSR[1:0] register in the function =?11? (D3).
16	0h RW	**PMCRE:** PMCRE: PMC Request Enable
15:13	0h RO	**Reserved2:** Reserved
12:10	2h RW/O	**POW_LAT_SCALE:** Power On Latency Scale
9:0	0h RW/O	**POW_LAT_VALUE:** Power On Latency value

13.10 Registers Summary

Table 13-10. Summary of soc_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h	AEC8086h
4h	7h	STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h	5000000h
Ch	Fh	CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	0h
10h	13h	BAR -Base Address Register (BAR)—Offset 10h	0h
14h	17h	BAR -Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	BAR1 -Base Address Register1 (BAR1)—Offset 18h	0h
1Ch	1Fh	BAR1 -Base Address Register1 High (BAR1_HIGH)—Offset 1Ch	0h
20h	23h	(BAR2)—Offset 20h	0h
2Ch	2Fh	SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h	30001h

Table 13-10. Summary of soc_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
84h	87h	PMECTRLSTATUS_type Power Management Control and status register (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI DEVICE IDLE CAPABILITY RECORD (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	DEVID VENDOR SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	D0I3_CONTROL_SW_LTR_MMIO_REG - SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	DEVICE_IDLE_POINTER_REG - Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	0h
A0h	A3h	D0I3_MAX_POW_LAT_PG_CONFIG - DEVICE PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	800h

13.10.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Device ID and Vendor ID provided by this register uniquely identifies the XXX Device

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: AEC8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	AECh RO/V	**DEVICEID:** Device ID identifies the particular PCI device
15:0	8086h RO/V	**VENDORID:** Vendor ID is a unique ID provided by the PCI SIG, which identifies the manufacturer of the device

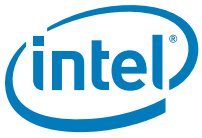
13.10.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

Command register to programme interrupt disable , bus master enable, and Memory space enable. Status register to read the errors and aborts

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0:** Reserved 0
29	0h RW/1C/V	**RMA:** Received Master Abort
28	0h RW/1C/V	**RTA:** Received Target Abort
27:21	0h RO	**Reserved1:** Reserved
20	1h RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device
18:16	0h RO	**Reserved2:** Reserved
15:11	0h RO	**Reserved3:** Reserved
10	0h RW	**INTR_DISABLE:** Interrupt Disable
9	0h RO	**Reserved4:** Reserved
8	0h RW	**SERR_ENABLE:** SERR Enable , Not implemented
7:3	0h RO	**Reserved5:** Reserved
2	0h RW	**BME:** Bus Master Enable
1	0h RW	**MSE:** Memory Space Enable
0	0h RW/V	**IOSE:** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0. NOTE: This bit does not exist in the PMC IOSF2OCP bridge. It is shadowed in the PSF3 fabric. Using /V in AccessType so PMC cluster validation does not assume this bit will read back what was written.

13.10.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Revision ID register identifies revision of particular device and Class Code register is used to identify generic function of the device

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 5000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	50000h RO/V	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface
7:0	0h RO/V	**RID:** Revision ID identifies the revision of particular PCI device.

13.10.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Cache Line size as RW with def 0, Latency timer RW with def 0, Header type with Type 0 configuration header and Reserved BIST register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved0:** Reserved
23	0h RO	**MULFNDEV:** Multi-Function Device
22:16	0h RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header
15:8	0h RO	**LATTIMER:** Latency Timer:. This register is implemented as R/W with default as 0
7:0	0h RW	**CACHELINE_SIZE:** Cacheline Size

13.10.5 BAR -Base Address Register (BAR)—Offset 10h

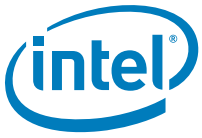
Base Address Register low [31:2] , type[2:1] in 32bit or 64bit addr range and memory space indicator [0]

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR:** Base Address Register Low, Base address of the OCP fabric memory space. Taken from Strap values as ones



Bit Range	Default & Access	Field Name (ID): Description
11:4	0h RO	**SIZEINDICATOR:** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**TYPE:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range, If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE:** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

13.10.6 BAR -Base Address Register High (BAR_HIGH)—Offset 14h

Base Address Register High enabled if [2:1] of BAR_type_LOW is 10

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR_HIGH:** Base Address high - MSB

13.10.7 BAR1 -Base Address Register1 (BAR1)—Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K, type in [2:1] and memory space indicator in [0]

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR1:** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	0h RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0h RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not prefetchable.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0h RO	**TYPE1:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

13.10.8 BAR1 -Base Address Register1 High (BAR1_HIGH)—Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR1_HIGH:** Base Address: Base address of the OCP fabric memory space. Taken from Strap values as ones

13.10.9 (BAR2)—Offset 20h

BAR -Base Address Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**BASEADDR**
1	0h RO	**Reserved0**
0	0h RO	**MESSAGE_SPACE**

13.10.10 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID:** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0h RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

13.10.11 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address register is a RO indicates support for expansion ROMs

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE:** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

13.10.12 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Capabilities Pointer register indicates what the next capability is

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved0:** Reserved
7:0	80h RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is.

13.10.13 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

Interrupt line Register isn't used in Bridge directly, Interrupt Pin register reflects the IPIN value in private config space. Min_gnt register indicating the req of latency timers and max_lat register max latency

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT:** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**MIN_GNT:** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved0:** Reserved
11:8	1h RO	**INTPIN:** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0h RW	**INTLINE:** Interrupt Line: It is used to communicate to software, the interrupt line to which the interrupt pin is connected

13.10.14 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

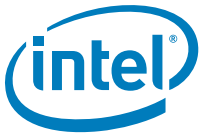
PowerManagement Capability ID register points to next capability structure and power mgmnt capability , with Power management capabilities register for PME support and version

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 30001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**PMESUPPORT:** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved0:** Reserved
18:16	3h RO	**VERSION:** Indicates support for Revision 1.2 of the PCI Power Management Specification



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**NXTCAP:** Next Capability: Points to the next capability structure.
7:0	1h RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability

13.10.15 PMECTRLSTATUS_type Power Management Control and status register (PMECTRLSTATUS)—Offset 84h

power management control and status register to set and read PME status, PME enable, No Soft reset and power state

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved0:** Reserved
15	0h RW/1C/V	**PMESTATUS:** PME Status
14:9	0h RO	**Reserved1:** Reserved
8	0h RW	**PMEENABLE:** PME Enable
7:4	0h RO	**Reserved2:** Reserved
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	**Reserved3:** Reserved
1:0	0h RW	**POWERSTATE:** Power State: This field is used both to determine the current power state and to set a new power state

13.10.16 PCI DEVICE IDLE CAPABILITY RECORD (PCIDEVIDLE_CAP_RECORD)—Offset 90h

PCI Device Vendor Specific Capability register defines Vendor specific Capability ID, revision , length , next capability and CAPID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** Vendor Specific Capability ID
27:24	0h RO	**REVID:** Revision ID of capability structure
23:16	14h RO	**CAP_LENGTH:** Vendor Specific Capability Length
15:8	0h RO	**NEXT_CAP:** Next Capability
7:0	9h RO	**CAPID:** Capability ID

13.10.17 DEVID VENDOR SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)—Offset 94h

Extended Vendor capability register for VSEC Length, revision and ID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH:** Vendor Specific Extended Capability Length
19:16	0h RO	**VSEC_REV:** Vendor specific Extended Capability revision
15:0	10h RO	**VSECID:** Vendor Specific Extended Capability ID

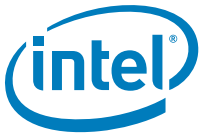
13.10.18 D0I3_CONTROL_SW_LTR_MMIO_REG - SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Software location pointer in MMIO space as an offset specified by BAR

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW_LAT_DWORD_OFFSET:** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW_LAT_BAR_NUM:** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW_LAT_VALID:** This value is reflected from the SW LTR valid strap at the top level

13.10.19 DEVICE_IDLE_POINTER_REG - Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location , BAR NUM and D0i3 Valid Strap

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**DWORD_OFFSET:** contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR
3:1	0h RO	**BAR_NUM:** Bar num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**VALID:** Valid: This value is reflected from the D0i3 valid strap at the top level.

13.10.20 D0I3_MAX_POW_LAT_PG_CONFIG - DEVICE PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

D0idle_Max_Power_On_Latency register set at boot and Power control enable register to enable communication with the PGCB block below the Bridge

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 13 **Function:** 3

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved1:** Reserved
19	0h RW	**SLEEP_EN:** Sleep Enable
18	0h RW	**PGE:** DEVIDLE Enable (DEVIDLEN): If ?1?, then the function will power gate when idle and the DevIdle register (DevIdleC[2] = ?1?) is set.
17	0h RW	**I3_ENABLE:** D3-Hot Enable (D3HEN): If ?1?, then function will power gate when idle and the PMCSR[1:0] register in the function =?11? (D3).
16	0h RW	**PMCRE:** PMCRE: PMC Request Enable
15:13	0h RO	**Reserved2:** Reserved
12:10	2h RW/O	**POW_LAT_SCALE:** Power On Latency Scale
9:0	0h RW/O	**POW_LAT_VALUE:** Power On Latency value

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14 Power Management Controller (P-Unit)

14.1 Registers Summary

Table 14-1. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
54h	57h	Device Enable Register (P_CR_DEVEN_0_0_0_PCI)—Offset 54h	33h
E4h	E7h	Capability ID0 A (P_CR_CAPID0_A_0_0_0_PCI)—Offset E4h	0h
E8h	EBh	Capability ID0 B (P_CR_CAPID0_B_0_0_0_PCI)—Offset E8h	0h

14.1.1 Device Enable Register (P_CR_DEVEN_0_0_0_PCI)—Offset 54h

The Device Enable register allows for enabling/disabling of PCI devices and functions that are within the CPU package.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 33h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**RESERVED_1 (RESERVED_1):** Reserved
5	1h RW/V	**Device 3 Function 0 Enable (Imaging) (D3F0EN):** 0 = Imaging Device 0/3/0 is disabled and hidden 1 = Imaging Device 0/3/0 is enabled and visible Software may write a 0b to this register to disable the imaging device. Writes to 1b are not allowed (i.e., the device may not be software enabled if hardware natively disables it)
4	1h RW/V	**Device 2 Function 0 Enable (Graphics/Display) (D2F0EN):** 0 = Graphics/Display Device 0/2/0 is disabled and hidden 1 = Graphics/Display Device 0/2/0 is enabled and visible Software may write a 0b to this register to disable the graphics / display device. Writes to 1b are not allowed (i.e., the device may not be software enabled if hardware natively disables it)

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	Reserved.
2	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
1	1h RW/V	**Device 0 Function 1 Enable (Thermal) (D0F1EN):** 0 = Thermal Device 0/0/1 is disabled and hidden 1 = Thermal Device 0/0/1 is enabled and visible Software may write a '0 to this register to disable the thermal device. Writes to '1 are not allowed (i.e., the device may not be software enabled if hardware natively disables it)
0	1h RO	**Device 0 Function 0 Enable (Memory / System Agent) (D0F0EN):** Device enable for MCHBAR device. This device not be disabled and is therefore hardwired to 1.

14.1.2 Capability ID0 A (P_CR_CAPID0_A_0_0_0_PCI)—Offset E4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V	**SPARE31_24 (SPARE31_24):** Reserved for future capabilities.
23	0h RW/V	**VTd Disable (VTDD):** 0 = Enable VTd 1 = Disable VTd
22	0h RW/V	**FUSE_SPARE22 (FUSE_SPARE22):** Fuse backed spare.
21	0h RW/V	**FUSE_SPARE21 (FUSE_SPARE21):** Fuse backed spare.
20	0h RW/V	**FUSE_SPARE20 (FUSE_SPARE20):** Fuse backed spare.
19	0h RW/V	**FUSE_SPARE19 (FUSE_SPARE19):** Fuse backed spare.
18	0h RW/V	**FUSE_SPARE18 (FUSE_SPARE18):** Fuse backed spare.
17	0h RW/V	**FUSE_SPARE17 (FUSE_SPARE17):** Fuse backed spare.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/V	**FUSE_SPARE16 (FUSE_SPARE16):** Fuse backed spare.
15	0h RW/V	**Thermal Device Disable (CDD):** 0 = Thermal associated memory spaces are accessible. 1 = Thermal associated memory and IO spaces are disabled. DEVEN_0_0_0_PCI field for DPTF cannot be set.
14	0h RW/V	**FUSE_SPARE14 (FUSE_SPARE14):** Fuse backed spare.
13	0h RW/V	**FUSE_SPARE13 (FUSE_SPARE13):** Fuse backed spare.
12	0h RW/V	**FUSE_SPARE12 (FUSE_SPARE12):** Fuse backed spare.
11	0h RW/V	**Internal Graphics and Display Disable (IGD):** 0 = There is a graphics engine within this CPU. Internal Graphics Device 2 is enabled, and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the CPU. All nonSMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2, IO registers within Device 2, and VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6, if PCI Express GFX attach is supported. A selected amount of Graphics Memory space is preallocated from the main memory, based on Graphics Mode Select GMS in the GGC Register. Graphics Memory is preallocated above TSEG Memory. 1 = There is no graphics engine within this CPU. Internal Graphics Device 2 and all of its memory and I/O functions are disabled. Configuration cycles targeted to Device 2 will be passed on to DMI. In addition, all clocks to internal graphics logic are turned off. All nonSMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6. DEVEN [4:3] Device 0 offset 54h have no meaning. Device 2 Functions 0 and 1 are disabled and hidden.
10	0h RO	**DIDOE (DIDOE):** Controls if there is an override of Dev2 (GFX) device ID. 0 = Disable ability to override DID - For production 1 = Enable ability to override DID - For debug and samples only

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RO	**CDID (CDID):** Controls the value of Dev2 (GFX) device ID. Identifier assigned to the core/primary PCI device.The corresponding two bit capability ID programming is: 00b = Desktop 01b = Mobile 10b = Server 11b = Marketing Spare
7:0	0h RW	**SPARE7_0 (SPARE7_0):** Reserved for future capabilities

14.1.3 Capability ID0 B (P_CR_CAPID0_B_0_0_0_PCI)—Offset E8h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**IMGU_DIS (IMGU_DIS):** 0: Imaging Unit associated memory spaces are accessible. 1: Imaging Unit associated memory and IO spaces are disabled. DEVEN_0_0_0_PCI field for I-unit can not be set.
30	0h RW/V	**FUSE_SPARE30 (FUSE_SPARE30):** Fuse backed spare.
29	0h RW/V	**FUSE_SPARE29 (FUSE_SPARE29):** Fuse backed spares, potentially to be used for PKGTYP encoding.
28	0h RW/V	**FUSE_SPARE28 (FUSE_SPARE28):** Fuse backed spares potentially to be used for PKGTYP encoding.
27	0h RW/V	**FUSE_SPARE27 (FUSE_SPARE27):** Fuse backed spares potentially to be used for PKGTYP encoding.
26	0h RW/V	**FUSE_SPARE26 (FUSE_SPARE26):** Fuse backed spares potentially to be used for PKGTYP encoding.
25	0h RW/V	**FUSE_SPARE25 (FUSE_SPARE25):** Fuse backed spares potentially to be used for PKGTYP encoding.
24	0h RW/V	**Shared Virtual Memory Disable (SVMDIS):** 0 = Enable Shared Virtual Memory mode 1 = Disable Shared Virtual Memory mode

Bit Range	Default & Access	Field Name (ID): Description
23:0	0h RW	**Spare (SPARE23_0):** Reserved for future capabilities.

14.2 Registers Summary

Table 14-2. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID Register (P_CR_DEVICE_ID_VENDOR_ID_0_0_1_PCI)—Offset 0h	A8C8086h
4h	7h	PCI_STATUS_COMMAND_0_0_1_PCI (P_CR_PCI_STATUS_COMMAND_0_0_1_PCI)—Offset 4h	900000h
8h	Bh	PCI Revision ID and PCI Class Code Register (P_CR_REVISION_ID_CLASS_CODE_0_0_1_PCI)—Offset 8h	11800000h
Ch	Fh	Master Latency Timer and Header Type Register (P_CR_MASTER_LATENCY_TIME_0_0_1_PCI)—Offset Ch	0h
10h	13h	Thermal Management Base Address Register (P_CR_TMBAR_LO_0_0_1_PCI)—Offset 10h	4h
14h	17h	Thermal Management Base Address Register (P_CR_TMBAR_HI_0_0_1_PCI)—Offset 14h	0h
2Ch	2Fh	PCI Subsystem Vendor ID and PCI Subsystem ID (P_CR_SVID_SID_0_0_1_PCI)—Offset 2Ch	0h
34h	37h	CAPPTR_0_0_1_PCI (P_CR_CAPPTR_0_0_1_PCI)—Offset 34h	D0h
3Ch	3Fh	Interrupt and Latency Configuration (P_CR_INTR_LAT_0_0_1_PCI)—Offset 3Ch	100h
54h	57h	Device Enable Register (P_CR_DEVEN_0_0_1_PCI)—Offset 54h	33h
88h	8Bh	SCISTS_0_0_1_PCI (P_CR_SCISTS_0_0_1_PCI)—Offset 88h	0h
CCh	CFh	SCI Command (P_CR_SCICMD_0_0_1_PCI)—Offset CCh	0h
D0h	D3h	Power Management Capabilities (P_CR_PMCAPID_0_0_1_PCI)—Offset D0h	3E001h
D4h	D7h	Power Management Control and Status (P_CR_PMCS_0_0_1_PCI)—Offset D4h	8h
DCh	DFh	Interrupt Status (P_CR_INTSTS_0_0_1_PCI)—Offset DCh	0h
E0h	E3h	Capability ID0 Capability Control (P_CR_CAPID0_CAPCTRL0_0_0_1_PCI)—Offset E0h	10C0009h
E4h	E7h	Capability ID0 A (P_CR_CAPID0_A_0_0_1_PCI)—Offset E4h	0h
E8h	EBh	Capability ID0 B (P_CR_CAPID0_B_0_0_1_PCI)—Offset E8h	0h

14.2.1 Device ID and Vendor ID Register (P_CR_DEVICE_ID_VENDOR_ID_0_0_1_PCI)—Offset 0h

This register uniquely identifies any PCI device.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: A8C8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	A8Ch RO/V	**Device ID (DEVICE_ID):** Identifier assigned to the SoC Thermal Management Controller.
15:0	8086h RO	**Vendor ID (VENDOR_ID):** Hardwired to Intel's Vendor ID value.

14.2.2 PCI_STATUS_COMMAND_0_0_1_PCI (P_CR_PCI_STATUS_COMMAND_0_0_1_PCI)—Offset 4h

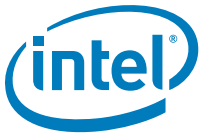
PCI Status is used to record status information for PCI bus related events, including the occurrence of a PCI compliant Master Abort (MA) and PCI compliant Target Abort (TA). PCISTS also indicates the DEVSEL# timing that has been set by the thermal device.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 900000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Detected Parity Error (DPE):** The Thermal device does not implement this bit and it is hardwired to a 0.
30	0h RO	**Signaled System Error (SSE):** This bit is hardwired to zero. The Thermal device never asserts SERR#, and therefore it has no need to implement this bit.
29	0h RO	**Received Master Abort (RURS):** The Thermal device does not implement this bit and it is hardwired to a 0.
28	0h RO	**Received Target Abort (RCAS):** The Thermal device does not implement this bit and it is hardwired to a 0.
27	0h RO	**Signaled Target Abort (STAS):** his bit is hardwired to 0. The Thermal device will not generate a Target Abort DMI completion packet or Special Cycle, and therefore it has no need to implement this bit.
26:25	0h RO	**DEVSEL Timing (DEVT):** These bits are hardwired to 0. Device 4 does not physically connect to PCI_A.
24	0h RO	**Master Data Parity Error (DPD):** This bit is hardwired to 0. PERR signaling and messaging are not implemented by the Thermal Device, and therefore it has no need to implement this bit.
23	1h RO	**Fast Back to Back Capable (FB2B_CAPABLE):** This bit is hardwired to 1. Device 4 does not physically connect to PCI_A, so this bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the Thermal device.



Bit Range	Default & Access	Field Name (ID): Description
22	0h RO	Reserved.
21	0h RO	**66MHz Capable (PCI66M):** The Thermal device does not implement this bit and it is hardwired to a 0.
20	1h RO	**Capabilities List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function. PCI Configuration Space containing a pointer to the location of the first item in the list.
19	0h RO/V	**Interrupt Status (IS):** Reflects the state of the INTA# signal at the input of the enable/disable circuit. This bit is set by HW to 1 when the INTA# is asserted and reset by HW to 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the 0.0.1.PCICMD register).
18:11	0h RO	Reserved.
10	0h RW	**INTx# Disable (INTDIS):** This bit, when set, disables the device from asserting INTx#, where 'x' is configured in the INTPIN register.
9	0h RO	**Fast Back to Back Enable (FB2B_ENABLE):** The Thermal device does not implement this bit and it is hardwired to a 0.
8	0h RO	**SERR# Enable (SERRE):** The Thermal device does not implement this bit and it is hardwired to a 0.
7	0h RO	**ADSTEP (ADSTEP):** The Thermal device does not implement this bit and it is hardwired to a 0.
6	0h RO	**Parity Error Enable (PERRE):** This bit is hardwired to 0. The Thermal device belongs to the category of devices that does not corrupt programs or data in system memory or hard drives. It therefore ignores any parity error that it detects and continues with normal operation.
5	0h RO	**VGA Snoop (VGASNOOP):** The Thermal device does not implement this bit and it is hardwired to a 0.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** This bit is hardwired to 0. The Thermal device will never issue memory write and invalidate commands, and therefore has no need to implement this bit.
3	0h RO	**Special Cycle Enable (SCE):** The Thermal device does not implement this bit and it is hardwired to a 0.
2	0h RW	**Bus Master Enable (BME):** The Thermal device is enabled to function as a PCI-compliant bus master when this bit is set. If it is not set, bus mastering is disabled.
1	0h RW	**Memory Access Enable (MAE):** The Thermal device will allow access to thermal registers when this bit is set. If it is not set, access to memory mapped thermal registers is disabled.
0	0h RO	**I/O Access Enable (IOAE):** The Thermal device does not implement this bit and it is hardwired to a 0.

14.2.3 PCI Revision ID and PCI Class Code Register (P_CR_REVISION_ID_CLASS_CODE_0_0_1_PCI)—Offset 8h

Revision ID contains the revision number of the device. Class Code identifies the basic function of the device.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 11800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	11h RO	**Base Class Code (BASE_CLASS_CODE):** This is an 8-bit value that indicates the base class code for the Thermal Controller. This code has the value 11h, indicating a device that is used for data acquisition and signal processing.
23:16	80h RO	**Sub-class Code (SUB_CLASS_CODE):** The code is 80h which indicates 'Other Data Acquisition and Signal Processing Controllers.'
15:8	0h RO	**Programming Interface (PI):** This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.
7:0	0h RO/V	**Revision ID (REVISION_ID):** Revision ID.

14.2.4 Master Latency Timer and Header Type Register (P_CR_MASTER_LATENCY_TIME_0_0_1_PCI)—Offset Ch

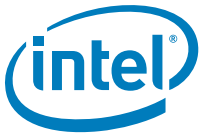
This register defines Latency Timer and layout of the device Configuration Space header.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**BIST Support (BS):** This bit is hardwired to zero. The Thermal device does not support BIST.
30:24	0h RO	Reserved.



Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RO	**Header Type (HDR):** This field always returns 0 to indicate that the Thermal device is a single function device with standard header layout.
15:8	0h RO	**Master Latency Timer (MLT):** This field is hardwired to 0. The Thermal device does not support perform bursts.
7:0	0h RO	**Cache Line Size (CLS):** This field is hardwired to 0. The Thermal Device as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

14.2.5 Thermal Management Base Address Register (P_CR_TMBAR_LO_0_0_1_PCI)—Offset 10h

This is the base address for the Thermal Controller Memory Mapped space. There is no physical memory within this 32KB window that can be addressed. The 32KB reserved by this register does not alias to any PCI 2.2 compliant memory mapped space. All TMBAR space maps the access to this memory space towards MCHBAR space. For details of this BAR, refer to the MCHBAR specifications.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Base Address of TMBAR (TMMBA):** This field corresponds to bits 31 to 15 of the base address TMBAR address space. BIOS will program this register resulting in a base address for a 32KB block of contiguous memory address space. This register ensures that a naturally aligned 32KB space is allocated within total addressable memory space. The DPTF driver uses this base address to program all Thermal and Throttling control register set.'
14:4	0h RO	**Address Map (ADM):** Hardwired to 0 to indicate at least 32KB address range.
3	0h RO	**Prefetch Memory (PM):** Hardwired to 0 to prevent prefetching.
2:1	2h RO	**Memory Type (MT):** Hardwired to '10 to indicate 64-bit address.
0	0h RO	**Memory or IO Space (MIOS):** Hardwired to 0 to indicate memory space.

14.2.6 Thermal Management Base Address Register (P_CR_TMBAR_HI_0_0_1_PCI)—Offset 14h

This is the base address for the Thermal Controller Memory Mapped space. There is no physical memory within this 32KB window that can be addressed. The 32KB reserved by this register does not alias to any PCI 2.2 compliant memory mapped space. All TMBAR space maps the access to this memory space towards MCHBAR space. For details of this BAR, refer to the MCHBAR specifications.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Reserved (RSVDRW):** Must be set to 0 since addressing above 512GB is not supported.
6:0	0h RW	**Base Address of TMBAR (TMMBA):** This field corresponds to bits 38 to 32 of the base address TMBAR address space. BIOS will program this register resulting in a base address for a 32KB block of contiguous memory address space. This register ensures that a naturally aligned 32KB space is allocated within total addressable memory space. The DPTF driver uses this base address to program all Thermal and Throttling control register set.

14.2.7 PCI Subsystem Vendor ID and PCI Subsystem ID (P_CR_SVID_SID_0_0_1_PCI)—Offset 2Ch

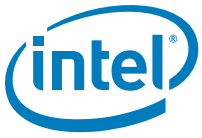
This register is used to uniquely identify the subsystem where the PCI device resides.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Subsystem ID (SUBSYSTEM_ID):** PCI Subsystem ID: This field should be programmed during BIOS initialization.
15:0	0h RW	**Subsystem Vendor ID (SUBSYSTEM_VENDOR_ID):** PCI Subsystem Vendor ID: This field should be programmed by BIOS during bootup to indicate the vendor of the system board.



14.2.8 CAPPTR_0_0_1_PCI (P_CR_CAPPTR_0_0_1_PCI)—Offset 34h

CAPPOINT provides the offset that is the pointer to the location of the first device capability in the capability list.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: D0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	D0h RO	**Base Address of First Capability Register (BASE_ADDR):** This pointer is an 8-bit address to an offset within this device's Configuration Space that holds the first Capability Register (CAPID0_CAPCTRL).

14.2.9 Interrupt and Latency Configuration (P_CR_INTR_LAT_0_0_1_PCI)—Offset 3Ch

This register is used for specifying how often the device needs to gain access to the PCI bus.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Maximum Latency Value (MLV):** These bits are hardwired to zero. The Thermal device has no specific requirements for how often it needs to access the PCI bus.
23:16	0h RO	**Minimum Grant Value (MGV):** These bits are hardwired to zero. The Thermal device does not burst as a PCI compliant master.
15:8	1h RW/L	**Interrupt Pin (INTPIN):** As a single function device, the Thermal device specifies INTA as its interrupt pin. 01h = INTA by default. BIOS may need to reconfigure this in order allow software to disambiguate multiple functions within MCHBAR. Recommended setting is 02h = INTB. This field is locked from future writes when the THERMAL_DEVICE_IRQ.LOCK

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (INTCON):** Used to communicate interrupt line routing information. BIOS Requirement: POST software writes the routing information into this register as it initializes and configures the system. The value indicates to which input of the system interrupt controller this device's interrupt pin is connected.

14.2.10 Device Enable Register (P_CR_DEVEN_0_0_1_PCI)—Offset 54h

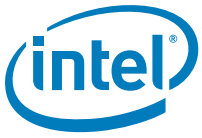
The Device Enable register allows for enabling/disabling of PCI devices and functions that are within the CPU package.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 33h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**RESERVED_1 (RESERVED_1):** Reserved
5	1h RW/V	**Device 3 Function 0 Enable (Imaging) (D3F0EN):** 0 = Imaging Device 0/3/0 is disabled and hidden 1 = Imaging Device 0/3/0 is enabled and visible Software may write a 0b to this register to disable the imaging device. Writes to 1b are not allowed (i.e., the device may not be software enabled if hardware natively disables it)
4	1h RW/V	**Device 2 Function 0 Enable (Graphics/Display) (D2F0EN):** 0 = Graphics/Display Device 0/2/0 is disabled and hidden 1 = Graphics/Display Device 0/2/0 is enabled and visible Software may write a 0b to this register to disable the graphics / display device. Writes to 1b are not allowed (i.e., the device may not be software enabled if hardware natively disables it)
3	0h RO	Reserved.
2	0h RO	**RESERVED_0 (RESERVED_0):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
1	1h RW/V	**Device 0 Function 1 Enable (Thermal) (D0F1EN):** 0 = Thermal Device 0/0/1 is disabled and hidden 1 = Thermal Device 0/0/1 is enabled and visible Software may write a '0 to this register to disable the thermal device. Writes to '1 are not allowed (i.e., the device may not be software enabled if hardware natively disables it)
0	1h RO	**Device 0 Function 0 Enable (Memory / System Agent) (D0F0EN):** Device enable for MCHBAR device. This device not be disabled and is therefore hardwired to 1.

14.2.11 SCISTS_0_0_1_PCI (P_CR_SCISTS_0_0_1_PCI)—Offset 88h

This register is used to report various error conditions via the SCI messaging mechanism. An SCI message is generated on a zero to one transition of any of these flags (if enabled by the SCICMD and PCICMD registers). This bit is set regardless of whether or not the SCI event is enabled and generated. After the event processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a 1 to it.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/1C/V	**CTED (CTED):** If set, indicates a thermal event was detected and SCI has optionally been generated. If this bit is already set, then an interrupt message will not be sent on a new event. ACPI software will write this bit to 1b to clear the event.

14.2.12 SCI Command (P_CR_SCICMD_0_0_1_PCI)—Offset CCh

This register enables various event conditions to generate an SCI event message. When an event log is observed, it will generate an SCI message when enabled by the SCICMD register.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW	**SCI Event Enable (SCICE):** 0 = SCI messaging in response to thermal events is disabled. 1 = Generate an SCI event message on detection of a hardware thermal event, as configured by software.
15:0	0h RO	Reserved.

14.2.13 Power Management Capabilities (P_CR_PMCAPID_0_0_1_PCI)—Offset D0h

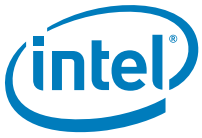
The Power Management Capabilities register is a 16-bit read-only register which provides information on the capabilities of the function related to power management. The information in this register is generally static and known at design time.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 3E001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**PME Support (PMES):** This field indicates the power states in which the thermal device may assert PME#. It is hardwired to 0 to indicate that the Thermal device does not support nor assert the PME# signal.
26	0h RO	**D2 (D2):** Hardwired to 0 to indicate that the D2 power management state is not supported.
25	0h RO	**D1 (D1):** Hardwired to 0 to indicate that the D1 power management state is not supported.
24:22	0h RO	Reserved.
21	0h RO	**Device Specific Initialization (DSI):** Indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. This bit is not used by some operating systems. Microsoft Windows and Windows NT, for instance, do not use this bit to determine whether to use D3. Instead, they use the driver's capabilities to determine this. 1b indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state.



Bit Range	Default & Access	Field Name (ID): Description
20	0h RO	**APS (APS):** The Thermal device does not implement this bit and it is hardwired to a 0.
19	0h RO	**PME# Capbility (PMEC):** Hardwired to 0 to indicate the thermal device does not support PME# generation.
18:16	3h RO	**Version (VER):** This device complies with revision 1.2 of the PCI Power Management Interface Specification.
15:8	E0h RO	**Next Capability Pointer (NCP):** This contains a pointer to next item in capabilities list. The next capability is E0h which is device 0 / func 0 capability mirror.
7:0	1h RO	**Capability ID (CID):** 01h indicates that this is a power management capability

14.2.14 Power Management Control and Status (P_CR_PMCS_0_0_1_PCI)—Offset D4h

The Data register is an optional, 8-bit read-only register that provides a mechanism for the function to report state dependent operating data such as power consumed or heat dissipation. Typically the data returned through the Data register is a static copy (look up table, for example) of the function's worst case 'DC characteristics' data sheet. This data, when made available to system software, could then be used to intelligently make decisions about power budgeting, cooling requirements, etc.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**DATA (DATA):** The data register, data scale and data select registers are not supported. Hardwired to zero.
23:16	0h RO	Reserved.
15	0h RO	**PME# Status (PMES):** This bit is set when the function would normally assert the PME# signal independent of the state of the PME_En bit. This bit is hardwired to 0b to indicate that PME# assertion from D3 (cold) is not supported.
14:13	0h RO	**Data Scale (DS):** The data register, data scale and data select registers are not supported
12:9	0h RO	**Data Select (DSEL):** The data register, data scale and data select registers are not supported
8	0h RO	**PME# Enable (PMEEN):** This bit is hardwired to 0b to indicate that PME# assertion from D3 (cold) is disabled.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NSR):** 1 = Devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration context is preserved. Upon transition from the D3hot to the D0 initialized state, no additional operating system intervention is required to preserve configuration Context beyond writing the PowerState bits. 0 = Devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full initialization sequence is needed to return the device to D0 initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	Reserved.
1:0	0h RW/V	**Power State (PS):** This field indicates the current power state of the thermal device and can be used to set the thermal device into a new power state. If software attempts to write an unsupported state to this field, the write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00b = D0 Default 01b = D1 Not Supported 10b = D2 Not Supported 11b = D3

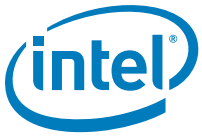
14.2.15 Interrupt Status (P_CR_INTSTS_0_0_1_PCI)—Offset DCh

This register is used to report interrupt pending event status. Upon event detection, if enabled, an interrupt message will be delivered to the IOAPIC. Upon processing that event, software may clear the event to enable future event signaling by writing a 1 to the INTSTAT bit in this register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/1C/V	**Interrupt Status (INTSTAT):** If set, indicates a thermal event was detected. If this bit is already set, then an interrupt message will not be sent upon detection of a new event.

14.2.16 Capability ID0 Capability Control (P_CR_CAPID0_CAPCTRL0_0_0_1_PCI)—Offset E0h

Control bits in this register describe the attributes of CAPID0_A and CAPID0_B capability registers.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 10C0009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:24	1h RO	**Capability ID Version (CAPID_VER):** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	Ch RO	**Capability ID0 Structure Length (CAPIDLEN):** This field has the value 0Ch to indicate the structure length 12 bytes. This is the total size of this CAPCTRL and the CAPID0_A and CAPID0_B registers in the following bytes.
15:8	0h RO	**Next Capability Register Pointer (NCP):** This field is hardwired to 00h, indicating the end of the capabilities linked list.
7:0	9h RO	**Capability ID (CAP_ID):** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

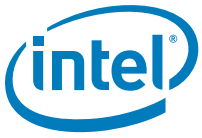
14.2.17 Capability ID0 A (P_CR_CAPID0_A_0_0_1_PCI)—Offset E4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V	**SPARE31_24 (SPARE31_24):** Reserved for future capabilities.
23	0h RW/V	**VTd Disable (VTDD):** 0 = Enable VTd 1 = Disable VTd
22	0h RW/V	**FUSE_SPARE22 (FUSE_SPARE22):** Fuse backed spare.
21	0h RW/V	**FUSE_SPARE21 (FUSE_SPARE21):** Fuse backed spare.
20	0h RW/V	**FUSE_SPARE20 (FUSE_SPARE20):** Fuse backed spare.
19	0h RW/V	**FUSE_SPARE19 (FUSE_SPARE19):** Fuse backed spare.
18	0h RW/V	**FUSE_SPARE18 (FUSE_SPARE18):** Fuse backed spare.
17	0h RW/V	**FUSE_SPARE17 (FUSE_SPARE17):** Fuse backed spare.
16	0h RW/V	**FUSE_SPARE16 (FUSE_SPARE16):** Fuse backed spare.
15	0h RW/V	**Thermal Device Disable (CDD):** 0 = Thermal associated memory spaces are accessible. 1 = Thermal associated memory and IO spaces are disabled. DEVEN_0_0_0_PCI field for DPTF cannot be set.
14	0h RW/V	**FUSE_SPARE14 (FUSE_SPARE14):** Fuse backed spare.
13	0h RW/V	**FUSE_SPARE13 (FUSE_SPARE13):** Fuse backed spare.
12	0h RW/V	**FUSE_SPARE12 (FUSE_SPARE12):** Fuse backed spare.



Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/V	**Internal Graphics and Display Disable (IGD):** 0 = There is a graphics engine within this CPU. Internal Graphics Device 2 is enabled, and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the CPU. All nonSMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2, IO registers within Device 2, and VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6, if PCI Express GFX attach is supported. A selected amount of Graphics Memory space is preallocated from the main memory, based on Graphics Mode Select GMS in the GGC Register. Graphics Memory is preallocated above TSEG Memory. 1 = There is no graphics engine within this CPU. Internal Graphics Device 2 and all of its memory and I/O functions are disabled. Configuration cycles targeted to Device 2 will be passed on to DMI. In addition, all clocks to internal graphics logic are turned off. All nonSMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Devices 1 and 6. DEVEN [4:3] Device 0 offset 54h have no meaning. Device 2 Functions 0 and 1 are disabled and hidden.
10	0h RO	**DIDOE (DIDOE):** Controls if there is an override of Dev2 (GFX) device ID. 0 = Disable ability to override DID - For production 1 = Enable ability to override DID - For debug and samples only
9:8	0h RO	**CDID (CDID):** Controls the value of Dev2 (GFX) device ID. Identifier assigned to the core/primary PCI device.The corresponding two bit capability ID programming is: 00b = Desktop 01b = Mobile 10b = Server 11b = Marketing Spare
7:0	0h RW	**SPARE7_0 (SPARE7_0):** Reserved for future capabilities

14.2.18 Capability ID0 B (P_CR_CAPID0_B_0_0_1_PCI)—Offset E8h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 0 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**IMGU_DIS (IMGU_DIS):** 0: Imaging Unit associated memory spaces are accessible. 1: Imaging Unit associated memory and IO spaces are disabled. DEVEN_0_0_0_PCI field for I-unit can not be set.
30	0h RW/V	**FUSE_SPARE30 (FUSE_SPARE30):** Fuse backed spare.
29	0h RW/V	**FUSE_SPARE29 (FUSE_SPARE29):** Fuse backed spares, potentially to be used for PKGTYP encoding.
28	0h RW/V	**FUSE_SPARE28 (FUSE_SPARE28):** Fuse backed spares potentially to be used for PKGTYP encoding.
27	0h RW/V	**FUSE_SPARE27 (FUSE_SPARE27):** Fuse backed spares potentially to be used for PKGTYP encoding.
26	0h RW/V	**FUSE_SPARE26 (FUSE_SPARE26):** Fuse backed spares potentially to be used for PKGTYP encoding.
25	0h RW/V	**FUSE_SPARE25 (FUSE_SPARE25):** Fuse backed spares potentially to be used for PKGTYP encoding.
24	0h RW/V	**Shared Virtual Memory Disable (SVMDIS):** 0 = Enable Shared Virtual Memory mode 1 = Disable Shared Virtual Memory mode
23:0	0h RW	**Spare (SPARE23_0):** Reserved for future capabilities.

14.3 Registers Summary

Table 14-3. Summary of pcs_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
805Ch	805Fh	THREAD_STATUS (P_CR_GT_THREAD_STATUS_0_2_0_GTTMMADR)—Offset 805Ch	7FF07h
8060h	8063h	CORE_STATUS (P_CR_GT_CORE_STATUS_0_2_0_GTTMMADR)—Offset 8060h	1100FF07h
8064h	8067h	GT_SLICE_INFO (P_CR_GT_SLICE_INFO_0_2_0_GTTMMADR)—Offset 8064h	0h
8068h	806Bh	GT Hardware P-state Control Request (P_CR_GT_HWP_REQ_0_2_0_GTTMMADR)—Offset 8068h	0h
8070h	8073h	GT_MEM_BOUND_COUNTER_0_2_0_GTTMMADR (P_CR_GT_MEM_BOUND_COUNTER_0_2_0_GTTMMADR)—Offset 8070h	0h
8074h	8077h	GT_SQ_OCCUPANCY_0_2_0_GTTMMADR (P_CR_GT_SQ_OCCUPANCY_0_2_0_GTTMMADR)—Offset 8074h	0h
8078h	807Bh	GT_RW_DRAM_0_2_0_GTTMMADR (P_CR_GT_RW_DRAM_0_2_0_GTTMMADR)—Offset 8078h	0h
807Ch	807Fh	GT_P_REQ (P_CR_GT_THREAD_P_REQ_0_2_0_GTTMMADR)—Offset 807Ch	0h

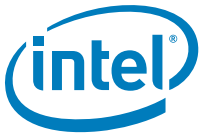


Table 14-3. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8080h	8087h	GT_ARAT_TTT (P_CR_GT_ARAT_TTT_0_2_0_GTTMMADR)—Offset 8080h	1FFFFFFFFFFFFFFFh
8088h	808Bh	GTC6_PREWAKE_TIMER_0_2_0_GTTMMADR (P_CR_GTC6_PREWAKE_TIMER_0_2_0_GTTMMADR)—Offset 8088h	0h
8090h	8093h	GT_DISP_PWRON_0_2_0_GTTMMADR (P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR)—Offset 8090h	0h
8108h	810Bh	GT_GFX_RC6_0_2_0_GTTMMADR (P_CR_GT_GFX_RC6_0_2_0_GTTMMADR)—Offset 8108h	0h
8124h	8127h	GTDRIVER_MAILBOX_INTERFACE_0_2_0_GTTMMADR (P_CR_GTDRIVER_MAILBOX_INTERFACE_0_2_0_GTTMMADR)—Offset 8124h	0h
8128h	812Bh	GTDRIVER_MAILBOX_DATA_LOW_0_2_0_GTTMMADR (P_CR_GTDRIVER_MAILBOX_DATA_LOW_0_2_0_GTTMMADR)—Offset 8128h	0h
812Ch	812Fh	GTDRIVER_MAILBOX_DATA_HIGH_0_2_0_GTTMMADR (P_CR_GTDRIVER_MAILBOX_DATA_HIGH_0_2_0_GTTMMADR)—Offset 812Ch	0h
8130h	8133h	P24C_PCODE_MAILBOX_INTERFACE_0_2_0_GTTMMADR (P_CR_P24C_PCODE_MAILBOX_INTERFACE_0_2_0_GTTMMADR)—Offset 8130h	0h
8134h	8137h	P24C_PCODE_MAILBOX_DATA_0_2_0_GTTMMADR (P_CR_P24C_PCODE_MAILBOX_DATA_0_2_0_GTTMMADR)—Offset 8134h	0h
8138h	813Bh	PCODE_P24C_MAILBOX_INTERFACE_0_2_0_GTTMMADR (P_CR_PCODE_P24C_MAILBOX_INTERFACE_0_2_0_GTTMMADR)—Offset 8138h	0h
813Ch	813Fh	PCODE_P24C_MAILBOX_DATA_0_2_0_GTTMMADR (P_CR_PCODE_P24C_MAILBOX_DATA_0_2_0_GTTMMADR)—Offset 813Ch	0h
8140h	8143h	GT_PM_CONFIG_0_2_0_GTTMMADR (P_CR_GT_PM_CONFIG_0_2_0_GTTMMADR)—Offset 8140h	0h
8150h	8153h	Graphics Interrupt Response Latency Tolerance (P_CR_GRAPHICS_INTERRUPT_RESPONSE_TIME_0_2_0_GTTMMADR)—Offset 8150h	0h
8160h	8163h	GTDRIVER_P2G_EVENTS_0_2_0_GTTMMADR (P_CR_GTDRIVER_P2G_EVENTS_0_2_0_GTTMMADR)—Offset 8160h	0h
8164h	8167h	GTDRIVER_G2P_EVENTS_0_2_0_GTTMMADR (P_CR_GTDRIVER_G2P_EVENTS_0_2_0_GTTMMADR)—Offset 8164h	0h
816Ch	816Fh	CORE_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_CORE_FREQUENCY_CAPABILITIES_0_2_0_GTTMMADR)—Offset 816Ch	0h
8170h	8173h	GRAPHICS_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_GRAPHICS_FREQUENCY_CAPABILITIES_0_2_0_GTTMMADR)—Offset 8170h	0h
8174h	8177h	SYSTEM_AGENT_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_SYSTEM_AGENT_FREQUENCY_CAPABILITIES_0_2_0_GTTMMADR)—Offset 8174h	0h
8178h	817Bh	Memory Frequency Status (P_CR_FAR_MEMORY_FREQUENCY_CAPABILITIES_0_2_0_GTTMMADR)—Offset 8178h	0h

Table 14-3. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8184h	8187h	GT_PERF_LIMIT_REASONS (P_CR_GT_PERF_LIMIT_REASONS_0_2_0_GTTMMADR)—Offset 8184h	0h
8190h	8197h	GTDRIVER_HWP_REQUEST_0_2_0_GTTMMADR (P_CR_GTDRIVER_HWP_REQUEST_0_2_0_GTTMMADR)—Offset 8190h	0h
8198h	819Bh	ISPDRIVER_PROCESSING_SYSTEM_FREQ_CAPABILITIES_0_0_0_MCHBAR (P_CR_PROCESSING_SYSTEM_FREQ_CAPABILITIES_0_2_0_GTTMMADR)—Offset 8198h	0h
819Ch	819Fh	GT_VIDEO_BUSYNESS_0_2_0_GTTMMADR (P_CR_GT_VIDEO_BUSYNESS_0_2_0_GTTMMADR)—Offset 819Ch	0h

14.3.1 THREAD_STATUS (P_CR_GT_THREAD_STATUS_0_2_0_GTTMMADR)—Offset 805Ch

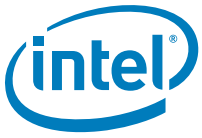
Per thread status register THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 7FF07h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**THREAD_ACTIVE (THREAD_ACTIVE):** Tied to same value as CORE_STATUS.CORE_ACTIVE, updated by PMA.
30	0h RO/V	**VOTE_REQUEST (VOTE_REQUEST):** This bit will be set on TC0TC1 and cleared on TC1ETC7.
29:19	0h RO	**RESERVED_2 (RESERVED_2):** reserved
18:16	7h RO/V	**THREAD_WISH_ALLOW (THREAD_WISH_ALLOW):** This field contains the allowed core C-state limit. It is read by Ucode on C-state entry to clip its wish_state request. Pcode updates this field (via IO_CORE_DEMOTED_C1) based on demotion algorithm and: fuse, DFX, SW limits in PKG_C_STATE_LIMIT_REQ, probe mode and patch load (via Ucode Mbox).
15:12	Fh RW	**THREAD_WISH_SUB_STATE (THREAD_WISH_SUB_STATE):** Ucode updates this field with the desired Thread CState SubState.
11:8	Fh RW	**THREAD_WISH_STATE (THREAD_WISH_STATE):** Ucode updates this field with the parameters of the MWAIT instruction.



Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**RESERVED_1 (RESERVED_1):** Reserved.
6:4	0h RW	**THREAD_TPD_STATE (THREAD_TPD_STATE):** Thread power down state
3	0h RO	**RESERVED_0 (RESERVED_0):** Reserved.
2:0	7h RW	**THREAD_STATE (THREAD_STATE):** Resolved thread_state updated by Ucode after it has completed entry/exit.

14.3.2 CORE_STATUS (P_CR_GT_CORE_STATUS_0_2_0_GTTMMADR)—Offset 8060h

Per core (including GT) status register.
Used by Ucode/GT and P-Unit/PMA HW to communicate core status to Pcode. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

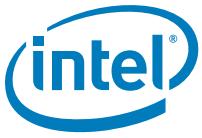
Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1100FF07h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**CORE_ACTIVE (CORE_ACTIVE):** Virtual signal indicating core is active. Value is updated by writes to RCSM_CORE_RESPONSE.CORE_ACTIVE from GT/GLM PMA. When set to '1', Pcode ignores value in CORE_STATE field and assumes C0, additionally P-Unit HW will delay fast path due to CORE_STATE field to non-C0 values until CORE_ACTIVE is '0'
30	0h RO/V	**WAKEUP_REQUEST (WAKEUP_REQUEST):** WAKEUP_REQUEST is set by interrupt wakes from T-Unit (via T2P_INT_WAKE) or Pcode via IO_PCODE_WAKEUP_REQUEST. WAKEUP_REQUEST is cleared by T-Unit (via T2P_INT_WAKE) when INT_READY vector is set. Fastpath (IO_FASTPATH_CORE_C) is set on WAKEUP_REQUEST, or when WAKEUP_REQUEST is '1' and CORE_IN_C3_C6 asserts.
29	0h RO	**RESERVED_3 (RESERVED_3):** Reserved
28	1h RO/V	**CORE_IN_C3_C6 (CORE_IN_C3_C6):** Virtual signal indicating core is in electrical (post RCSM flow) C3/C6. Value is updated by writes to RCSM_CORE_RESPONSE.CORE_IN_C3C6 from GT/GLM PMA. Must be asserted for WAKEUP_REQUEST to trigger fastpath.

Bit Range	Default & Access	Field Name (ID): Description
27	0h WO	**PROBE_MODE_DONE (PROBE_MODE_DONE):** Sent by Ucode to inform P-Unit that probe mode seqeunce is complete, used to clear pending probe mode request in P-Unit HW.
26	0h RW	**DISABLE_WAKEUP_REQ (DISABLE_WAKEUP_REQ):** Reserved.
25	0h RO/V	**S1_ACK (S1_ACK):** Reserved.
24	1h RW/V	**PM_BLOCK_REQ (PM_BLOCK_REQ):** Controls the status of the Interrupt Ready mask in the T-Unit. Set by Ucode before Piclet setup during C6 entry. On assertion of this bit P-Unit will send P2T_INT_CONTROL_ADDR.INT_READY_CLEAR to T-Unit. Any interrupts received after this point will cause T-Unit to send a interrupt wake request via T2P_INT_WAKE.SET_CORE_MASK Cleared by Ucode after Piclet replay during C6 exit. On deassertion of this bit, P-Unit will send P2T_INT_CONTROL_ADDR.INT_READY_SET to T-Unit. This will cause T-Unit to clear any pending interrupt wakes via T2P_INT_WAKE.CLEAR_CORE_MASK.
23	0h RO/V	**RFO_EN (RFO_EN):** For GT this bit indicates the status of read-for ownership (RFOs). If it is '1' RFOs are enabled and if it is '0' RFOs are disabled. This field only has meaning for the GT register instance. It is a dont care for the IA register instances.
22:16	0h RO	**RESERVED_2 (RESERVED_2):** Reserved
15:12	Fh RW	**CORE_WISH_SUB_STATE (CORE_WISH_SUB_STATE):** Ucode updates this field with the desired Core CState SubState.
11:8	Fh RW	**CORE_WISH_STATE (CORE_WISH_STATE):** Ucode updates this field with the parameters of the MWAIT instruction.
7	0h RO	**RESERVED_1 (RESERVED_1):** Reserved.
6:4	0h RW	**CORE_CPD_STATE (CORE_CPD_STATE):** Updated by Ucode on Core Power Down (CPD) exit or entry. CPD is used during GV Flows to quiesce core.
3	0h RO	**RESERVED_0 (RESERVED_0):** Reserved.
2:0	7h RW/V	**CORE_STATE (CORE_STATE):** Updated with the current core C-state, by Ucode on C6 entry/exit, at the end of the respective flow.



14.3.3 GT_SLICE_INFO (P_CR_GT_SLICE_INFO_0_2_0_GTTMMADR)—Offset 8064h

Status register describing GT slice state.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10	0h RO/V	**UNSLICESTAT (UNSLICESTAT):** Status of GT unslice power plane 0 = GT has unslice powered off 1 = GT has unslice powered on
9:3	0h RO	Reserved.
2:0	0h RO/V	**SLICESTAT (SLICESTAT):** Status of GT power planes. 000b = GT is powered off C6 or not yet booted 001b = GT has slice 0 powered 011b = GT has slices 0 and 1 powered 111b = GT has slices 0, 1 and 2 powered

14.3.4 GT Hardware P-state Control Request (P_CR_GT_HWP_REQ_0_2_0_GTTMMADR)—Offset 8068h

This register is used as an interface for the graphics driver to communicate hardware managed P-state control requests and/or hints specific to the graphics domain. These requests are used by silicon power management firmware to implement SOC and platform level power and thermal control algorithms.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Reserved3 (RSVD3):** This field is reserved for future use
23:16	0h RW	**Reserved2 (RSVD2):** This field is reserved for future use
15:8	0h RW	**Reserved1 (RSVD1):** This field is reserved for future use
7:0	0h RW	**Quality of Service P-state (QOS_RATIO):** GT Quality of Service P-state request. The GT driver programs this to define a desired performance floor. This floor is useful as a hint to power and thermal control algorithms to balance system resources appropriately in order to ensure a minimum graphics performance floor. Described in 16.67MHz reference clock units, e.g., a ratio of 24 results in a clock frequency of 400MHz.

14.3.5 GT_MEM_BOUND_COUNTER_0_2_0_GTTMMADR (P_CR_GT_MEM_BOUND_COUNTER_0_2_0_GTTMMADR)—Offset 8070h

GT memory bound counter. Holds the accumulated number of CS clks that GT has been waiting for memory grants.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**DATA (DATA):** Accumulated cycles GT has been waiting for memory grants.

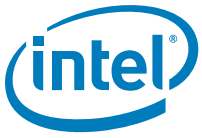
14.3.6 GT_SQ_OCCUPANCY_0_2_0_GTTMMADR (P_CR_GT_SQ_OCCUPANCY_0_2_0_GTTMMADR)—Offset 8074h

Accumulated GT super queue (SQ) occupancy. This is accumulated by GT and pushed to P-Unit from the GT PMA.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**DATA (DATA):** Accumulated SQ occupancy.

14.3.7 GT_RW_DRAM_0_2_0_GTTMMADR (P_CR_GT_RW_DRAM_0_2_0_GTTMMADR)—Offset 8078h

This register contains the the sum of the cycles GT has read or written DRAM. It contains a 32-bit accumulation of data sent via the Pushbus. Values exceeding 32 bits will wrap around.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**DATA (DATA):** RW GT cycles to DRAM

14.3.8 GT_P_REQ (P_CR_GT_THREAD_P_REQ_0_2_0_GTTMMADR)—Offset 807Ch

GT Pstate request. This register is written by driver/GT with the desired P-State request. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RW	**UNSLICE_RATIO (UNSLICE_RATIO):** UnSlice Ratio Multiple of 33.33MHz 2xclk 16 MHz 1xclk
22:14	0h RW	**SLICE_RATIO (SLICE_RATIO):** Slice Ratio Multiple of 33.33MHz 2xclk 16 MHz 1xclk
13:4	0h RO	**RESERVED_1 (RESERVED_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**SLICE_UNSLICE_POLICY (SLICE_UNSLICE_POLICY):** Specifies policy of slice and unslice ratios: 0x0 = Use unslice ratio for slice also ignore slice ratio field 0x1 = Maintain ratio between slice/unslice 0x2 = Attempt to throttle slice only maintain unslice ratio

14.3.9 GT_ARAT_TTT (P_CR_GT_ARAT_TTT_0_2_0_GTTMMADR)—Offset 8080h

Always Running APIC Timer 'Timer Target Time' (TTT) value. This is an absolute desired wakeup time. GT copies the local TTT to the P-Unit on RC6 entry. Pcode will wake GT via IO_PCODE_WAKEUP_REQUEST, such that the wake is finished when the URT reaches the value in this register.
To account for wake delay, Pcode will also take into account the prewake value that can be written via driver into GTC6_PREWAKE_TIMER_0_2_0_GTTMMADR.
If ARAT is invalid, GT will write all 1's (infinity).
GT writes this register via the MMIO alias GT_ARAT_TTT_0_2_0_GTTMMADR THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 1FFFFFFFFFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:61	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
60:0	1FFFFFFFFFFFFFFFh RW	**DATA (DATA):** The 61 bits of the TTT. GT will update this field with TTT value before entering RC6.

14.3.10 GTC6_PREWAKE_TIMER_0_2_0_GTTMMADR (P_CR_GTC6_PREWAKE_TIMER_0_2_0_GTTMMADR)—Offset 8088h

This register is used in conjuction with GT_ARAT_TTT. It contains the enable and value for a prewake offset that the GT driver can program to prewake GT from C6 with reference to its TTT.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
15	0h RW	**TMR_ENABLE (TMR_ENABLE):** Enable for the GT prewake, the driver sets this bit to 1 to enable the offset.
14:0	0h RW	**TMR_VALUE (TMR_VALUE):** Prewake timer value in microseconds, this will be subtracted from the GT_ARAT_TTT.

14.3.11 GT_DISP_PWRON_0_2_0_GTTMMADR (P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR)—Offset 8090h

Used by GT driver to control aspects of PHY power-on (MIPIO, eDP, DDI).

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**RESERVED_0 (RESERVED_0):** reserved
2	0h RW	**MIPIO_RST_CTRL (MIPIO_RST_CTRL):** MIPIO reset control. Driver clears on reset exit which deasserts side_rst to MIPI PHY and starts periodic RCOMPS from P-Unit. Driver sets on PHY disabling, which should occur prior to dev2 D3.
1	0h RW	**CH1_PWRREQ1P0_SUS (CH1_PWRREQ1P0_SUS):** GT Display eDP Power On. Written by GT driver to start eDP PHY initialization sequence.
0	0h RW	**CH0_PWRREQ1P0_SUS (CH0_PWRREQ1P0_SUS):** GT Display DDI Power On. Written by GT driver to start DDI PHY initialization sequence.

14.3.12 GT_GFX_RC6_0_2_0_GTTMMADR (P_CR_GT_GFX_RC6_0_2_0_GTTMMADR)—Offset 8108h

Wrapping counter containing the total GT RC6 residency time since boot.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**RC6 (RC6):** GT RC6 residency, value is specified in 833.33ns increments. Counter will wrap around.

14.3.13 GTDRIVER_MAILBOX_INTERFACE_0_2_0_GTTMMADR (P_CR_GTDRIVER_MAILBOX_INTERFACE_0_2_0_GTTMMADR)—Offset 8124h

Control and Status register for the GFXDRIVERtoPCODE mailbox. This mailbox is implemented as a means for the GT Driver running on the IA cores to tune parameters for specific GFX workloads. This register is used in conjunction with GTDRIVER_MAILBOX_DATA_{HIGH and LOW}. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**RUN_BUSY (RUN_BUSY):** SW may write to the two mailbox registers only when RUN_BUSY is clear(0). Setting RUN_BUSY to 1 will pend a Fast Path event to Pcode. After setting this bit SW will poll this bit until it is cleared. Alternatively PCODE can generate an interrupt to SW via GTDRIVER_P2G_EVENTS. PCODE will clear RUN_BUSY after updating the mailbox registers with the result and error code.
30:16	0h RO	Reserved.
15:8	0h RW/V	**PARAM1 (PARAM1):** This field is used to specify an additional parameter to extend the command when needed.
7:0	0h RW/V	**COMMAND (COMMAND):** This field contains the SW request command or the PCODE response code depending on the setting of RUN_BUSY.

14.3.14 GTDRIVER_MAILBOX_DATA_LOW_0_2_0_GTTMMADR (P_CR_GTDRIVER_MAILBOX_DATA_LOW_0_2_0_GTTMMADR)—Offset 8128h

Data register for lower 32b of data for the GTDRIVERtoPCODE mailbox. This mailbox is implemented as a means for the GTDriver running on the IA cores to tune parameters for specific GFX workloads. This register is used in conjunction with GTDRIVER_MAILBOX_INTERFACE. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**DATA (DATA):** This field contains the lower 32b of data associated with specific commands.

14.3.15 GTDRIVER_MAILBOX_DATA_HIGH_0_2_0_GTTMMADR (P_CR_GTDRIVER_MAILBOX_DATA_HIGH_0_2_0_GTTMMADR)—Offset 812Ch

Data register for upper 32b of data for the GFXDRIVERtoPCODE mailbox. This mailbox is implemented as a means for the GT Driver running on the IA cores to tune parameters for specific GFX workloads. This register is used in conjunction with GTDRIVER_MAILBOX_INTERFACE. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**DATA (DATA):** This field contains the upper 32b of data associated with specific commands.

14.3.16 P24C_PCODE_MAILBOX_INTERFACE_0_2_0_GTTMMADR (P_CR_P24C_PCODE_MAILBOX_INTERFACE_0_2_0_GTTMMADR)—Offset 8130h

Control and status register for the P24CtoPCODE mailbox. This mailbox is implemented as a way for the GT P24C to contact the P-unit and is accessible via MMIO. This register is used in conjunction with P24C_PCODE_MAILBOX_DATA. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**RUN_BUSY (RUN_BUSY):** Software may write to the mailbox registers only when RUN_BUSY is clear(0). Setting RUN_BUSY to 1 will pend a fastpath even to Pcode. After setting this bit software polls until it is cleared. Pcode clears the bit after updating the mailbox registers with the result and error code.
30:24	0h RO	Reserved.
23:16	0h RW/V	**PARAM2 (PARAM2):** This field is used to specify a second additional parameter to extend the command when needed.
15:8	0h RW/V	**PARAM1 (PARAM1):** This field is used to specify an additional parameter to extend the command when needed.
7:0	0h RW/V	**COMMAND (COMMAND):** This field contains the SW request command or the PCODE response code depending on the setting of RUN_BUSY.

14.3.17 P24C_PCODE_MAILBOX_DATA_0_2_0_GTTMMADR (P_CR_P24C_PCODE_MAILBOX_DATA_0_2_0_GTTMMADR)—Offset 8134h

Data register for the P24CtoPCODE mailbox. This register is used in conjunction with P24C_PCODE_MAILBOX_INTERFACE THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**DATA (DATA):** This field contains the data associated with specific commands.

14.3.18 PCODE_P24C_MAILBOX_INTERFACE_0_2_0_GTTMMADR (P_CR_PCODE_P24C_MAILBOX_INTERFACE_0_2_0_GTTMMADR)—Offset 8138h

Control and status register for the PCODEtoP24C mailbox. This mailbox is implemented as a way for pcode to sendi commands to the P24C GT microcontroller. This register is used in conjunction with PCODE_P24C_MAILBOX_DATA. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/0C/V	**RUN_BUSY (RUN_BUSY):** Pcode may write to the mailbox registers only when RUN_BUSY is clear(0). After setting RUN_BUSY to 1 PCode generates a PMLink command to shift in an uncore trap message to the GT P24C uC. GT P24C clears the RUN_BUSY bit after updating the mailbox registers with the result and error code. This clear of RUN_BUSY creates pends a fast path event to pcode.
30:24	0h RO	Reserved.
23:16	0h RW/V	**PARAM2 (PARAM2):** This field is used to specify a second additional parameter to extend the command when needed.
15:8	0h RW/V	**PARAM1 (PARAM1):** This field is used to specify an additional parameter to extend the command when needed.
7:0	0h RW/V	**COMMAND (COMMAND):** This field contains the PCODE request command or the GT P24C response code depending on the setting of RUN_BUSY. Command Encodings: 01h

14.3.19 PCODE_P24C_MAILBOX_DATA_0_2_0_GTTMMADR (P_CR_PCODE_P24C_MAILBOX_DATA_0_2_0_GTTMMADR)—Offset 813Ch

Data register for the PCODEtoP24C mailbox. This register is used in conjunction with PCODE_P24C_MAILBOX_INTERFACE. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**DATA (DATA):** This field contains the data associated with specific commands.

14.3.20 GT_PM_CONFIG_0_2_0_GTTMMADR (P_CR_GT_PM_CONFIG_0_2_0_GTTMMADR)—Offset 8140h

Interface for GT driver to configure power management.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**RESERVED_0 (RESERVED_0):** Reserved
0	0h RW	**DOORBELL_EN (DOORBELL_EN):** Set by driver to enable doorbell mode. This must be set after GT is in and held in RC0 (force-wake). This field must be cleared prior to dev2 D3.

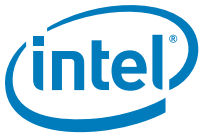
14.3.21 Graphics Interrupt Response Latency Tolerance (P_CR_GRAPHICS_INTERRUPT_RESPONSE_TIME_0_2_0_GTTMMADR)—Offset 8150h

This register is used by the graphics driver to communicate any interrupt latency tolerance (IRT/IRTL) requirements from the software. The P-unit is responsible for ensuring that the graphics worst-case interrupt response latency is always lower than what is programmed in this register.
Some components of worst-case exit latency for the graphics domain are outside the control of the P-unit, and therefore there is a physical floor below which the interrupt response tolerance may not be guaranteed. That floor is usually in the 100us range.
IRT is used only for S0i3 entry if Dev2 is not in D3. If Dev2 is in D3, its assumed latency tolerance is infinity.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**VALID (VALID):** This field qualifies the validity of the Value field in this register. If the valid bit is zero, then it is assumed that software has no constraints on wake latency (i.e., it supports infinity).
14:13	0h RO	Reserved.
12:10	0h RW	**Multiplier (MULTIPLIER):** This field indicates the unit of measurement that is defined for the Value field in this register. The units are 2^(5*multiplier) 000b = 1ns (2^0) 001b = 32ns (2^5) 010b = 1024ns (2^10) 011b = 32.768us (2^15) 100b = 1.048ms (2^20) 101b = 33.55ms (2^25)
9:0	0h RW	**VALUE (VALUE):** This scalar is multiplied by the multiplier field to calculate the net latency tolerance. Ex., with a MULTIPLIER of 2 and a VALUE of 20, the net latency tolerance is 20 * (2^10) = 20480ns or 20.48us

14.3.22 GTDRIVER_P2G_EVENTS_0_2_0_GTTMMADR (P_CR_GTDRIVER_P2G_EVENTS_0_2_0_GTTMMADR)—Offset 8160h

This extended capability allows PCODE to send an interrupt notification upon completion of a mailbox command received from the GTDRIVER. It is enabled via the GTDriver Mailbox. PCODE will set the appropriate bit in this register to 1 and will then write to 0.2.0.GTTMMADR.PIM[PCU_MBOXE]. The GFX Driver will clear the appropriate bit in this register by writing a 1 to the bit. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C/V	**EVENT7 (EVENT7):** Placeholder for Event
6	0h RW/1C/V	**EVENT6 (EVENT6):** Placeholder for Event
5	0h RW/1C/V	**EVENT5 (EVENT5):** Placeholder for Event
4	0h RW/1C/V	**EVENT4 (EVENT4):** Placeholder for Event
3	0h RW/1C/V	**EVENT3 (EVENT3):** Placeholder for Event
2	0h RW/1C/V	**EVENT2 (EVENT2):** Placeholder for Event
1	0h RW/1C/V	**EVENT1 (EVENT1):** Placeholder for Event
0	0h RW/1C/V	**EVENT0 (EVENT0):** This event indicates that the command previously sent by the GTDriver via the Mailbox mechanism is complete.

14.3.23 GTDRIVER_G2P_EVENTS_0_2_0_GTTMMADR (P_CR_GTDRIVER_G2P_EVENTS_0_2_0_GTTMMADR)—Offset 8164h

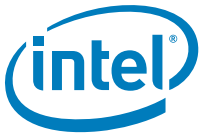
This extended capability allows the GTDriver to send a request to PCODE. The GTDriver will set the appropriate bit in this register to 1 when it wants to generate an event to PCODE. This will pend a Fast Path event to pcode. PCODE will clear the appropriate bit in this register after servicing the request. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW/1S/V	**EVENT7 (EVENT7):** Placeholder for Event
6	0h RW/1S/V	**EVENT6 (EVENT6):** Placeholder for Event
5	0h RW/1S/V	**EVENT5 (EVENT5):** Placeholder for Event
4	0h RW/1S/V	**EVENT4 (EVENT4):** Placeholder for Event



Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1S/V	**EVENT3 (EVENT3):** Placeholder for Event
2	0h RW/1S/V	**EVENT2 (EVENT2):** Placeholder for Event
1	0h RW/1S/V	**EVENT1 (EVENT1):** Placeholder for Event
0	0h RW/1S/V	**EVENT0 (EVENT0):** Placeholder for Event

14.3.24 CORE_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_CORE_FREQUENCY_CAPABILITIES_0_2_0_GTTMMADR)—Offset 816Ch

PUNIT_MMIO: Core Frequency Capabilities
This register describes the frequency capabilities of the IA cores. Units are 100MHz multiplied by the ratio.
Minimum and maximum ratio fields are initialized by pCode at reset. Last resolved ratio is updated upon changes to the processing system frequency. The efficient ratio is determined by firmware and may be updated dynamically depending on firmware support.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LAST_RESOLVED_FREQ (LAST_RESOLVED_FREQ):** Last resolved ratio for the IA cores. Units are 100MHz multiplied by the ratio. This value is updated dynamically whenever the IA core frequency changes.
23:16	0h RO/V	**MAX_SUPPORTED_FREQ (MAX_SUPPORTED_FREQ):** Maximum ratio for the IA cores. Units are 100MHz multiplied by the ratio.
15:8	0h RO/V	**EFFICIENT_FREQ (EFFICIENT_FREQ):** Firmware-calculated efficient ratio for the IA cores. Units are 100MHz multiplied by the ratio.
7:0	0h RO/V	**MIN_SUPPORTED_FREQ (MIN_SUPPORTED_FREQ):** Minimum supported ratio for the IA cores. Units are 100MHz multiplied by the ratio.

14.3.25 GRAPHICS_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_GRAPHICS_FREQUENCY_CAPABILITIES_0_2_0_GTTMMADR)—Offset 8170h

PUNIT_MMIO: Graphics Engine Frequency Capabilities
This register describes the frequency capabilities of the integrated graphics engine. Units are 50MHz multiplied by the ratio.
Minimum and maximum ratio fields are initialized by pCode at reset. Last resolved ratio is updated upon changes to the integrated graphics engine frequency. The efficient ratio is determined by firmware and may be updated dynamically depending on firmware support.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LAST_RESOLVED_FREQ (LAST_RESOLVED_FREQ):** Last resolved ratio for the integrated graphics engine. Units are 50MHz multiplied by the ratio. This value is updated dynamically whenever the graphics engine frequency changes.
23:16	0h RO/V	**MAX_SUPPORTED_FREQ (MAX_SUPPORTED_FREQ):** Maximum supported ratio for the integrated graphics engine. Units are 50MHz multiplied by the ratio.
15:8	0h RO/V	**EFFICIENT_FREQ (EFFICIENT_FREQ):** Firmware-calculated efficient ratio for the integrated graphics engine. Units are 50MHz multiplied by the ratio.
7:0	0h RO/V	**MIN_SUPPORTED_FREQ (MIN_SUPPORTED_FREQ):** Minimum supported ratio for the integrated graphics engine. Units are 50MHz multiplied by the ratio.

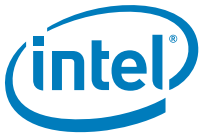
14.3.26 SYSTEM_AGENT_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_SYSTEM_AGENT_FREQUENCY_CAPABILITIES_0_2_0_GTTMMADR)—Offset 8174h

PUNIT_MMIO: System Agent Frequency Capabilities
This register describes the frequency capabilities of the System Agent. Units are 16.666MHz multiplied by the ratio.
Last resolved ratio is updated upon changes to the System Agent frequency.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LAST_RESOLVED_RATIO (LAST_RESOLVED_RATIO):** Last resolved System Agent ratio, in units of 16.666MHz.
23:16	0h RO/V	**RESERVED_2 (RESERVED_2):** Reserved
15:8	0h RO/V	**RESERVED_1 (RESERVED_1):** Reserved
7:0	0h RO/V	**RESERVED_0 (RESERVED_0):** Reserved

14.3.27 Memory Frequency Status (P_CR_FAR_MEMORY_FREQUENCY_CAPABILITIES_0_2_0_GTTMMADR)—Offset 8178h

This register reports out the LPDDR memory frequency. The actual capabilities of the SOC with respect to LPDDR frequency is described in the MEMSS_FREQUENCY_CAPABILITIES register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Last Resolved Memory Frequency (LAST_RESOLVED_RATIO):** This field reports out the LPDDR memory frequency in integer multiple of 133.33MHz. This register reflects what BIOS has programmed as the default LPDDR frequency in products that do not support run-time memory frequency control. For products supporting run-time memory frequency control, this field describes the last resolved frequency.
23:16	0h RO/V	**RESERVED_2 (RESERVED_2):** Reserved
15:8	0h RO/V	**RESERVED_1 (RESERVED_1):** Reserved
7:0	0h RO/V	**RESERVED_0 (RESERVED_0):** Reserved

14.3.28 GT_PERF_LIMIT_REASONS (P_CR_GT_PERF_LIMIT_REASONS_0_2_0_GTTMMADR)—Offset 8184h

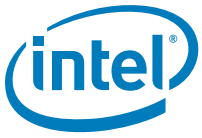
This register reports reasons for performance limitations on the integrated graphics engine. Status bits are an instantaneous indication of an active constraint. Log bits indicate that a constraint was enforced since the log bit was last cleared.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/0C/V	**QOS_LOG (QOS_LOG):** Logged indication that frequency was clamped below the software-defined quality-of-service floor. This bit is set by firmware, and is clearable by software.
30	0h RW/0C/V	**MAX_EFFICIENCY_FREQ_LOG (MAX_EFFICIENCY_FREQ_LOG):** Logged indication that frequency was clamped below the firmware-calculated maximum efficiency frequency. This bit is set by firmware, and is clearable by software.
29	0h RW/0C/V	**SPARE13_LOG (SPARE13_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
28	0h RW/0C/V	**EDP_LOG (EDP_LOG):** Logged indication that frequency was clamped due to the package-level Electrical Design Point constraint. This bit is set by firmware, and is clearable by software.
27	0h RW/0C/V	**SPARE11_LOG (SPARE11_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
26	0h RW/0C/V	**VR_THERMALERT_LOG (VR_THERMALERT_LOG):** Logged indication that frequency was clamped due to a voltage regulator thermal excursion. This bit is set by firmware, and is clearable by software.
25	0h RW/0C/V	**SPARE9_LOG (SPARE9_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
24	0h RW/0C/V	**SPARE8_LOG (SPARE8_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
23	0h RW/0C/V	**SPARE7_LOG (SPARE7_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
22	0h RW/0C/V	**SPARE6_LOG (SPARE6_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
21	0h RW/0C/V	**SPARE5_LOG (SPARE5_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
20	0h RW/0C/V	**SPARE4_LOG (SPARE4_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
19	0h RW/0C/V	**PL2_LOG (PL2_LOG):** Logged indication that frequency was clamped due to a package-level PL2 excursion. This bit is set by firmware, and is clearable by software.
18	0h RW/0C/V	**PL1_LOG (PL1_LOG):** Logged indication that frequency was clamped due to a package-level PL1 excursion. This bit is set by firmware, and is clearable by software.



Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/0C/V	**THERMAL_LOG (THERMAL_LOG):** Logged indication that frequency was clamped due to a thermal excursion. This bit is set by firmware, and is clearable by software.
16	0h RW/0C/V	**PROCHOT_LOG (PROCHOT_LOG):** Logged indication that frequency was clamped due to PROCHOT assertion. This bit is set by firmware, and is clearable by software.
15	0h RO/V	**QOS_STATUS (QOS_STATUS):** Frequency is limited below the operating system or driver Quality-of-Service floor.
14	0h RO/V	**MAX_EFFICIENCY_FREQ_STATUS (MAX_EFFICIENCY_FREQ_STATUS):** Frequency is limited below the maximum efficiency frequency.
13	0h RO/V	**SPARE13_STATUS (SPARE13_STATUS):** Frequency is limited due to ratio change transition attenuation (MCT, prevents frequent ratio changes due to core C-state entry/exit).
12	0h RO/V	**EDP_STATUS (EDP_STATUS):** Frequency is limited due to a package-level EDP constraint.
11	0h RO/V	**SPARE11_STATUS (SPARE11_STATUS):** Spare status bit.
10	0h RO/V	**VR_THERMALERT_STATUS (VR_THERMALERT_STATUS):** Frequency is limited due to a voltage regulator thermal excursion.
9	0h RO/V	**SPARE9_STATUS (SPARE9_STATUS):** Spare status bit.
8	0h RO/V	**SPARE8_STATUS (SPARE8_STATUS):** Spare status bit.
7	0h RO/V	**SPARE7_STATUS (SPARE7_STATUS):** Spare status bit.
6	0h RO/V	**SPARE6_STATUS (SPARE6_STATUS):** Spare status bit.
5	0h RO/V	**SPARE5_STATUS (SPARE5_STATUS):** Spare status bit.
4	0h RO/V	**SPARE4_STATUS (SPARE4_STATUS):** Spare status bit.
3	0h RO/V	**PL2_STATUS (PL2_STATUS):** Frequency is limited due to a package-level PL2 excursion.
2	0h RO/V	**PL1_STATUS (PL1_STATUS):** Frequency is limited due to a package-level PL1 excursion.
1	0h RO/V	**THERMAL_STATUS (THERMAL_STATUS):** Frequency is limited due to thermal excursion.
0	0h RO/V	**PROCHOT_STATUS (PROCHOT_STATUS):** Frequency is limited due to external PROCHOT assertion.

14.3.29 GTDRIVER_HWP_REQUEST_0_2_0_GTTMMADR (P_CR_GTDRIVER_HWP_REQUEST_0_2_0_GTTMMADR)—Offset 8190h

PUNIT_MMIO: GTDRIVER_HWP_REQUEST
This register allows the graphics driver to dictate the minimum and maximum performance of the IA cores. The driver may also change the behavior of any autonomous IA P-state controller, if supported by firmware. Non-zero values override default firmware behavior.

Access Method

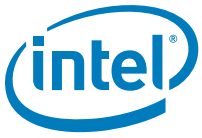
Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RW	**RESERVED_0 (RESERVED_0):** Reserved
41:32	0h RW	**ACTIVITY_WINDOW (ACTIVITY_WINDOW):** This field defines the time window over which the autonomous IA P-state controller (if supported) will manage IA core frequency. Units are microseconds.
31:24	0h RW	**AGGRESSIVENESS (AGGRESSIVENESS):** This field defines the performance/energy bias for the autonomous IA P-state controller, if supported.
23:16	0h RW	**MULTIPLIER (MULTIPLIER):** This field defines the IA frequency target: IA ratio = MULTIPLER * GT ratio. The format is U8.3.5 (e.g. 1.0 is 8h'20).
15:8	0h RW	**MAX_PERF (MAX_PERF):** Maximum IA core frequency allowed by the graphics driver. The field is defined as a ratio, multiply by 100MHz to convert to IA core frequency.
7:0	0h RW	**MIN_PERF (MIN_PERF):** Minimum IA core frequency allowed by the graphics driver. The field is defined as a ratio, multiply by 100MHz to convert to IA core frequency.

14.3.30 ISPDRIVER_PROCESSING_SYSTEM_FREQ_CAPABILITIES_0_0_0_MCHBAR (P_CR_PROCESSING_SYSTEM_FREQ_CAPABILITIES_0_2_0_GTTMMADR)—Offset 8198h

PUNIT_MMIO: Image Processing System Frequency Capabilities
This register describes the frequency capabilities of the image processing system. Units are 25MHz multiplied by the ratio.
Minimum and maximum ratio fields are initialized by pCode at reset. Last resolved ratio is updated upon changes to the processing system frequency. The efficient ratio is determined by firmware and may be updated dynamically depending on firmware support.



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LAST_RESOLVED_RATIO (LAST_RESOLVED_RATIO):** Last resolved ratio for the image processing system. Units are 25MHz multiplied by the ratio. This value is updated dynamically whenever the processing system frequency changes.
23:16	0h RO/V	**MAX_RATIO (MAX_RATIO):** Maximum ratio for the image processing system. Units are 25MHz multiplied by the ratio.
15:8	0h RO/V	**EFFICIENT_RATIO (EFFICIENT_RATIO):** Firmware-calculated efficient ratio for the image processing system. Units are 25MHz multiplied by the ratio.
7:0	0h RO/V	**MIN_RATIO (MIN_RATIO):** Minimum ratio for the image processing system. Units are 25MHz multiplied by the ratio.

14.3.31 GT_VIDEO_BUSYNESS_0_2_0_GTTMMADR (P_CR_GT_VIDEO_BUSYNESS_0_2_0_GTTMMADR)—Offset 819Ch

GT video busy counter. Holds the accumulated number of CS clks that GT video functions have been busy.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**DATA (DATA):** Accumulated cycles GT video functions have been busy.

14.4 Registers Summary

Table 14-4. Summary of pcs_regs_wrapper Registers

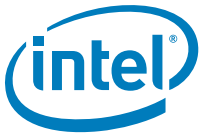
Offset Start	Offset End	Register Name (ID)—Offset	Default Value
7480h	7483h	ISPDRIVER_MAILBOX_INTERFACE_0_0_0_MCHBAR (P_CR_ISPDRIVER_MAILBOX_INTERFACE_0_0_0_MCHBAR)—Offset 7480h	0h

Table 14-4. Summary of pcs_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
7484h	7487h	ISPDRIVER_MAILBOX_DATA_LOW_0_0_0_MCHBAR (P_CR_ISPDRIVER_MAILBOX_DATA_LOW_0_0_0_MCHBAR)—Offset 7484h	0h
7488h	748Bh	ISPDRIVER_MAILBOX_DATA_HIGH_0_0_0_MCHBAR (P_CR_ISPDRIVER_MAILBOX_DATA_HIGH_0_0_0_MCHBAR)—Offset 7488h	0h
748Ch	748Fh	ISPDRIVER_P2I_EVENTS_0_0_0_MCHBAR (P_CR_ISPDRIVER_P2I_EVENTS_0_0_0_MCHBAR)—Offset 748Ch	0h
7490h	7493h	ISPDRIVER_I2P_EVENTS_0_0_0_MCHBAR (P_CR_ISPDRIVER_I2P_EVENTS_0_0_0_MCHBAR)—Offset 7490h	0h
7498h	749Bh	ISPDRIVER_PROCESSING_SYSTEM_FREQ_CAPABILITIES_0_0_0_MCHBAR (P_CR_ISPDRIVER_PROCESSING_SYSTEM_FREQ_CAPABILITIES_0_0_0_MCHBAR)—Offset 7498h	0h
74A0h	74A7h	ISPDRIVER_HWP_REQUEST_0_0_0_MCHBAR (P_CR_ISPDRIVER_HWP_REQUEST_0_0_0_MCHBAR)—Offset 74A0h	0h
74A8h	74ABh	ISPDRIVER_SPARE_RW_0_0_0_MCHBAR (P_CR_ISPDRIVER_SPARE_RW_0_0_0_MCHBAR)—Offset 74A8h	0h
74ACh	74AFh	ISPDRIVER_SPARE_RO_0_0_0_MCHBAR (P_CR_ISPDRIVER_SPARE_RO_0_0_0_MCHBAR)—Offset 74ACh	0h
74B0h	74B3h	CORE_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_ISPDRIVER_CORE_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 74B0h	0h
74B4h	74B7h	GRAPHICS_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_ISPDRIVER_GRAPHICS_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 74B4h	0h
74B8h	74BBh	SYSTEM_AGENT_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_ISPDRIVER_SYSTEM_AGENT_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 74B8h	0h
74BCh	74BFh	Memory Frequency Status (P_CR_ISPDRIVER_FAR_MEMORY_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 74BCh	0h
74CCh	74CFh	ISP_PERF_LIMIT_REASONS (P_CR_ISPDRIVER_ISP_PERF_LIMIT_REASONS_0_0_0_MCHBAR)—Offset 74CCh	0h
74D0h	74D3h	I-unit Processing System C0 Residency Counter (P_CR_ISPDRIVER_TELEM_IUNIT_C0_RESIDENCY_0_0_0_MCHBAR)—Offset 74D0h	0h
74D4h	74D7h	I-unit Processing System C0 Residency Counter (P_CR_ISPDRIVER_TELEM_IUNIT_FREQ_ACCUMULATOR_0_0_0_MCHBAR)—Offset 74D4h	0h

14.4.1 ISPDRIVER_MAILBOX_INTERFACE_0_0_0_MCHBAR (P_CR_ISPDRIVER_MAILBOX_INTERFACE_0_0_0_MCHBAR)—Offset 7480h

Control and Status register for the ISPDRIVERtoPCODE mailbox. This mailbox is implemented as a means for tuning parameters for specific ISP workloads. This register is used in conjunction with ISPDRIVER_MAILBOX_DATA. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**RUN_BUSY (RUN_BUSY):** SW may write to the mailbox registers only when RUN_BUSY is clear(0). Setting RUN_BUSY to 1 will pend a Fast Path event to pcode. After setting this bit SW will poll this bit until it is cleared. Alternatively PCODE can generate an interrupt to SW via ISPDRIVER_P2I_EVENTS. PCODE will clear RUN_BUSY after updating the mailbox registers with the result and error code.
30:29	0h RO	Reserved.
28:8	0h RW/V	**ADDR_CNTL (ADDR_CNTL):** This field is used to specify an additional parameters to extend the command when needed.
7:0	0h RW/V	**COMMAND (COMMAND):** This field contains the SW request command or the PCODE response code depending on the setting of RUN_BUSY.

14.4.2 ISPDRIVER_MAILBOX_DATA_LOW_0_0_0_MCHBAR (P_CR_ISPDRIVER_MAILBOX_DATA_LOW_0_0_0_MCHBAR)—Offset 7484h

Data register for lower 32b of data for the ISPDRIVERtoPCODE mailbox. This mailbox is implemented as a means for the ISPDriver running on the IA cores to tune parameters for specific ISP workloads. This register is used in conjunction with ISPDRIVER_MAILBOX_INTERFACE. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**DATA (DATA):** This field contains the data associated with specific commands.

14.4.3 ISPDRIVER_MAILBOX_DATA_HIGH_0_0_0_MCHBAR (P_CR_ISPDRIVER_MAILBOX_DATA_HIGH_0_0_0_MCHBAR)—Offset 7488h

Data register for upper 32b of data for the ISPDRIVERtoPCODE mailbox. This mailbox is implemented as a means for the ISPDriver running on the IA cores to tune parameters for specific ISP workloads. This register is used in conjunction with ISPDRIVER_MAILBOX_INTERFACE. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**DATA (DATA):** This field contains the data associated with specific commands.

14.4.4 ISPDRIVER_P2I_EVENTS_0_0_0_MCHBAR (P_CR_ISPDRIVER_P2I_EVENTS_0_0_0_MCHBAR)—Offset 748Ch

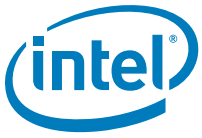
This extended capability allows PCODE to send an interrupt notification upon completion of a mailbox command. It is enabled via the ISP Driver Mailbox. PCODE will set the appropriate bit in this register to 1 and will then write to 0.3.0.ISPMMIOBAR.PIM[PCU_MBOX]. The ISP Driver will clear the appropriate bit in this register by writing a 1 to the bit. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW/1C/V	**EVENT7 (EVENT7):** Placeholder for Event
6	0h RW/1C/V	**EVENT6 (EVENT6):** Placeholder for Event
5	0h RW/1C/V	**EVENT5 (EVENT5):** Placeholder for Event



Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1C/V	**EVENT4 (EVENT4):** Placeholder for Event
3	0h RW/1C/V	**EVENT3 (EVENT3):** Placeholder for Event
2	0h RW/1C/V	**EVENT2 (EVENT2):** Placeholder for Event
1	0h RW/1C/V	**EVENT1 (EVENT1):** Placeholder for Event
0	0h RW/1C/V	**EVENT0 (EVENT0):** This event indicates that the command previously sent by the ISP Driver via the Mailbox mechanism is complete.

14.4.5 ISPDRIVER_I2P_EVENTS_0_0_0_MCHBAR (P_CR_ISPDRIVER_I2P_EVENTS_0_0_0_MCHBAR)—Offset 7490h

This extended capability allows the ISP Driver to send a request to PCODE. The ISP Driver will set the appropriate bit in this register to 1b when it wants to generate an event to PCODE. This will pend a Fast Path event to pcode. PCODE will clear the appropriate bit in this register after servicing the request. THIS REGISTER IS DUPLICATED IN THE PCU IO SPACE, XML CHANGES MUST BE MADE IN BOTH PLACES

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW/1S/V	**EVENT7 (EVENT7):** Placeholder for Event
6	0h RW/1S/V	**EVENT6 (EVENT6):** Placeholder for Event
5	0h RW/1S/V	**EVENT5 (EVENT5):** Placeholder for Event
4	0h RW/1S/V	**EVENT4 (EVENT4):** Placeholder for Event
3	0h RW/1S/V	**EVENT3 (EVENT3):** Placeholder for Event
2	0h RW/1S/V	**EVENT2 (EVENT2):** Placeholder for Event
1	0h RW/1S/V	**EVENT1 (EVENT1):** Placeholder for Event

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/1S/V	**EVENT0 (EVENT0):** Placeholder for Event

14.4.6 ISPDRIVER_PROCESSING_SYSTEM_FREQ_CAPABILITIES_0_0_0_MCHBAR (P_CR_ISPDRIVER_PROCESSING_SYSTEM_FREQ_CAPABILITIES_0_0_0_MCHBAR)—Offset 7498h

PUNIT_MMIO: Image Processing System Frequency Capabilities
This register describes the frequency capabilities of the image processing system. Units are 25MHz multiplied by the ratio.
Minimum and maximum ratio fields are initialized by pCode at reset. Last resolved ratio is updated upon changes to the processing system frequency. The efficient ratio is determined by firmware and may be updated dynamically depending on firmware support.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LAST_RESOLVED_RATIO (LAST_RESOLVED_RATIO):** Last resolved ratio for the image processing system. Units are 25MHz multiplied by the ratio. This value is updated dynamically whenever the processing system frequency changes.
23:16	0h RO/V	**MAX_RATIO (MAX_RATIO):** Maximum ratio for the image processing system. Units are 25MHz multiplied by the ratio.
15:8	0h RO/V	**EFFICIENT_RATIO (EFFICIENT_RATIO):** Firmware-calculated efficient ratio for the image processing system. Units are 25MHz multiplied by the ratio.
7:0	0h RO/V	**MIN_RATIO (MIN_RATIO):** Minimum ratio for the image processing system. Units are 25MHz multiplied by the ratio.

14.4.7 ISPDRIVER_HWP_REQUEST_0_0_0_MCHBAR (P_CR_ISPDRIVER_HWP_REQUEST_0_0_0_MCHBAR)—Offset 74A0h

PUNIT_MMIO: ISPDRIVER_HWP_REQUEST
This register allows the imaging unit driver to dictate the minimum and maximum performance of the IA cores. The driver may also change the behavior of any autonomous IA P-state controller, if supported by firmware. Non-zero values override default firmware behavior.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:42	0h RW	**RESERVED_0 (RESERVED_0):** Reserved
41:32	0h RW	**ACTIVITY_WINDOW (ACTIVITY_WINDOW):** This field defines the time window over which the autonomous IA P-state controller (if supported) will manage IA core frequency. Units are microseconds.
31:24	0h RW	**AGGRESSIVENESS (AGGRESSIVENESS):** This field defines the performance/energy bias for the autonomous IA P-state controller, if supported.
23:16	0h RW	**MULTIPLIER (MULTIPLIER):** This field defines the IA frequency target: IA ratio = MULTIPLER * processing system ratio. The format is U8.3.5 (e.g. 1.0 is 8h'20).
15:8	0h RW	**MAX_PERF (MAX_PERF):** Maximum IA core frequency allowed by the imaging unit driver. The field is defined as a ratio, multiply by 100MHz to convert to IA core frequency.
7:0	0h RW	**MIN_PERF (MIN_PERF):** Minimum IA core frequency allowed by the graphics driver. The field is defined as a ratio, multiply by 100MHz to convert to IA core frequency.

14.4.8 ISPDRIVER_SPARE_RW_0_0_0_MCHBAR (P_CR_ISPDRIVER_SPARE_RW_0_0_0_MCHBAR)—Offset 74A8h

Spare RW MMIO Register for IUNIT Driver.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SPARE_RW (SPARE_RW):** Spare RW MMIO space for I-Unit driver to Pcode/P-Unit interaction.

14.4.9 ISPDRIVER_SPARE_RO_0_0_0_MCHBAR (P_CR_ISPDRIVER_SPARE_RO_0_0_0_MCHBAR)—Offset 74ACh

Spare RO MMIO Register for IUNIT Driver.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SPARE_RO (SPARE_RO):** Spare RO MMIO space for I-Unit driver to Pcode/P-Unit interaction.

14.4.10 CORE_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_ISPDRIVER_CORE_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 74B0h

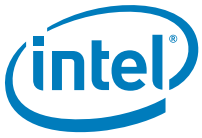
PUNIT_MMIO: Core Frequency Capabilities
This register describes the frequency capabilities of the IA cores. Units are 100MHz multiplied by the ratio.
Minimum and maximum ratio fields are initialized by pCode at reset. Last resolved ratio is updated upon changes to the processing system frequency. The efficient ratio is determined by firmware and may be updated dynamically depending on firmware support.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LAST_RESOLVED_FREQ (LAST_RESOLVED_FREQ):** Last resolved ratio for the IA cores. Units are 100MHz multiplied by the ratio. This value is updated dynamically whenever the IA core frequency changes.
23:16	0h RO/V	**MAX_SUPPORTED_FREQ (MAX_SUPPORTED_FREQ):** Maximum ratio for the IA cores. Units are 100MHz multiplied by the ratio.
15:8	0h RO/V	**EFFICIENT_FREQ (EFFICIENT_FREQ):** Firmware-calculated efficient ratio for the IA cores. Units are 100MHz multiplied by the ratio.
7:0	0h RO/V	**MIN_SUPPORTED_FREQ (MIN_SUPPORTED_FREQ):** Minimum supported ratio for the IA cores. Units are 100MHz multiplied by the ratio.



14.4.11 GRAPHICS_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_ISPDRIVER_GRAPHICS_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 74B4h

PUNIT_MMIO: Graphics Engine Frequency Capabilities
This register describes the frequency capabilities of the integrated graphics engine. Units are 50MHz multiplied by the ratio.
Minimum and maximum ratio fields are initialized by pCode at reset. Last resolved ratio is updated upon changes to the integrated graphics engine frequency. The efficient ratio is determined by firmware and may be updated dynamically depending on firmware support.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LAST_RESOLVED_FREQ (LAST_RESOLVED_FREQ):** Last resolved ratio for the integrated graphics engine. Units are 50MHz multiplied by the ratio. This value is updated dynamically whenever the graphics engine frequency changes.
23:16	0h RO/V	**MAX_SUPPORTED_FREQ (MAX_SUPPORTED_FREQ):** Maximum supported ratio for the integrated graphics engine. Units are 50MHz multiplied by the ratio.
15:8	0h RO/V	**EFFICIENT_FREQ (EFFICIENT_FREQ):** Firmware-calculated efficient ratio for the integrated graphics engine. Units are 50MHz multiplied by the ratio.
7:0	0h RO/V	**MIN_SUPPORTED_FREQ (MIN_SUPPORTED_FREQ):** Minimum supported ratio for the integrated graphics engine. Units are 50MHz multiplied by the ratio.

14.4.12 SYSTEM_AGENT_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR (P_CR_ISPDRIVER_SYSTEM_AGENT_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 74B8h

PUNIT_MMIO: System Agent Frequency Capabilities
This register describes the frequency capabilities of the System Agent. Units are 16.666MHz multiplied by the ratio.
Last resolved ratio is updated upon changes to the System Agent frequency.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LAST_RESOLVED_RATIO (LAST_RESOLVED_RATIO):** Last resolved System Agent ratio, in units of 16.666MHz.
23:16	0h RO/V	**RESERVED_2 (RESERVED_2):** Reserved
15:8	0h RO/V	**RESERVED_1 (RESERVED_1):** Reserved
7:0	0h RO/V	**RESERVED_0 (RESERVED_0):** Reserved

14.4.13 Memory Frequency Status (P_CR_ISPDRIVER_FAR_MEMORY_FREQUENCY_CAPABILITIES_0_0_0_MCHBAR)—Offset 74BCh

This register reports out the LPDDR memory frequency. The actual capabilities of the SOC with respect to LPDDR frequency is described in the MEMSS_FREQUENCY_CAPABILITIES register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Last Resolved Memory Frequency (LAST_RESOLVED_RATIO):** This field reports out the LPDDR memory frequency in integer multiple of 133.33MHz. This register reflects what BIOS has programmed as the default LPDDR frequency in products that do not support run-time memory frequency control. For products supporting run-time memory frequency control, this field describes the last resolved frequency.
23:16	0h RO/V	**RESERVED_2 (RESERVED_2):** Reserved
15:8	0h RO/V	**RESERVED_1 (RESERVED_1):** Reserved
7:0	0h RO/V	**RESERVED_0 (RESERVED_0):** Reserved

14.4.14 ISP_PERF_LIMIT_REASONS (P_CR_ISPDRIVER_ISP_PERF_LIMIT_REASONS_0_0_0_MCHBAR)—Offset 74CCh

This register reports reasons for performance limitations on the image processing system. Status bits are an instantaneous indication of an active constraint. Log bits indicate that a constraint was enforced since the log bit was last cleared.

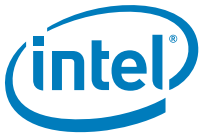
Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/0C/V	**QOS_LOG (QOS_LOG):** Logged indication that frequency was clamped below the software-defined quality-of-service floor. This bit is set by firmware, and is clearable by software.
30	0h RW/0C/V	**MAX_EFFICIENCY_FREQ_LOG (MAX_EFFICIENCY_FREQ_LOG):** Logged indication that frequency was clamped below the firmware-calculated maximum efficiency frequency. This bit is set by firmware, and is clearable by software.
29	0h RW/0C/V	**SPARE13_LOG (SPARE13_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
28	0h RW/0C/V	**EDP_LOG (EDP_LOG):** Logged indication that frequency was clamped due to the package-level Electrical Design Point constraint. This bit is set by firmware, and is clearable by software.
27	0h RW/0C/V	**SPARE11_LOG (SPARE11_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
26	0h RW/0C/V	**VR_THERMALERT_LOG (VR_THERMALERT_LOG):** Logged indication that frequency was clamped due to a voltage regulator thermal excursion. This bit is set by firmware, and is clearable by software.
25	0h RW/0C/V	**SPARE9_LOG (SPARE9_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
24	0h RW/0C/V	**SPARE8_LOG (SPARE8_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
23	0h RW/0C/V	**SPARE7_LOG (SPARE7_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
22	0h RW/0C/V	**SPARE6_LOG (SPARE6_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
21	0h RW/0C/V	**SPARE5_LOG (SPARE5_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
20	0h RW/0C/V	**SPARE4_LOG (SPARE4_LOG):** Spare log bit. This bit is set by firmware, and is clearable by software.
19	0h RW/0C/V	**PL2_LOG (PL2_LOG):** Logged indication that frequency was clamped due to a package-level PL2 excursion. This bit is set by firmware, and is clearable by software.
18	0h RW/0C/V	**PL1_LOG (PL1_LOG):** Logged indication that frequency was clamped due to a package-level PL1 excursion. This bit is set by firmware, and is clearable by software.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/0C/V	**THERMAL_LOG (THERMAL_LOG):** Logged indication that frequency was clamped due to a thermal excursion. This bit is set by firmware, and is clearable by software.
16	0h RW/0C/V	**PROCHOT_LOG (PROCHOT_LOG):** Logged indication that frequency was clamped due to PROCHOT assertion. This bit is set by firmware, and is clearable by software.
15	0h RO/V	**QOS_STATUS (QOS_STATUS):** Frequency is limited below the operating system or driver Quality-of-Service floor.
14	0h RO/V	**MAX_EFFICIENCY_FREQ_STATUS (MAX_EFFICIENCY_FREQ_STATUS):** Frequency is limited below the maximum efficiency frequency.
13	0h RO/V	**SPARE13_STATUS (SPARE13_STATUS):** Spare status bit.
12	0h RO/V	**EDP_STATUS (EDP_STATUS):** Frequency is limited due to a package-level EDP constraint.
11	0h RO/V	**SPARE11_STATUS (SPARE11_STATUS):** Spare status bit.
10	0h RO/V	**VR_THERMALERT_STATUS (VR_THERMALERT_STATUS):** Frequency is limited due to a voltage regulator thermal excursion.
9	0h RO/V	**SPARE9_STATUS (SPARE9_STATUS):** Spare status bit.
8	0h RO/V	**SPARE8_STATUS (SPARE8_STATUS):** Spare status bit.
7	0h RO/V	**SPARE7_STATUS (SPARE7_STATUS):** Spare status bit.
6	0h RO/V	**SPARE6_STATUS (SPARE6_STATUS):** Spare status bit.
5	0h RO/V	**SPARE5_STATUS (SPARE5_STATUS):** Spare status bit.
4	0h RO/V	**SPARE4_STATUS (SPARE4_STATUS):** Spare status bit.
3	0h RO/V	**PL2_STATUS (PL2_STATUS):** Frequency is limited due to a package-level PL2 excursion.
2	0h RO/V	**PL1_STATUS (PL1_STATUS):** Frequency is limited due to a package-level PL1 excursion.
1	0h RO/V	**THERMAL_STATUS (THERMAL_STATUS):** Frequency is limited due to thermal excursion.
0	0h RO/V	**PROCHOT_STATUS (PROCHOT_STATUS):** Frequency is limited due to external PROCHOT assertion.



14.4.15 I-unit Processing System C0 Residency Counter (P_CR_ISPDRIVER_TELEM_IUNIT_C0_RESIDENCY_0_0_0_MCHBAR)—Offset 74D0h

This counter measures time that I-unit processing system is active in the C0 state. This counter counts at the crystal clock frequency divided by 16. This counter may be used along with the I-unit Frequency Accumulator to calculate the average active clock ratio multiplier on the I-unit domain. **Average Active Frequency = Frequency Accumulator / C0 Residency**

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**C0 Residency (DATA):** This counter measures time that I-unit processing system is active in the C0 state. This counter counts at the crystal clock frequency divided by 16.

14.4.16 I-unit Processing System C0 Residency Counter (P_CR_ISPDRIVER_TELEM_IUNIT_FREQ_ACCUMULATOR_0_0_0_MCHBAR)—Offset 74D4h

This counter integrates the current clock ratio multiplier for the I-unit processing system domain at the same rate as the corresponding C0 residency counter. Its primary utility is in assessing the average active frequency of the domain **Average Active Frequency = Frequency Accumulator / C0 Residency**

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Clock Ratio Multiplier Accumulator (DATA):** This counter integrates the current clock ratio of the domain at the same rate as the corresponding C0 residency counter

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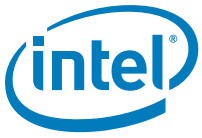


15 ITSS

15.1 Registers Summary

Table 15-1. Summary of 0_31_0_APIC MEM Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1h	4h	Version (VS)—Offset 1h	770020h
10h	17h	Redirection Table Entry 0 (RTE0)—Offset 10h	10000h
12h	19h	Redirection Table Entry 1 (RTE1)—Offset 12h	10000h
14h	1Bh	Redirection Table Entry 2 (RTE2)—Offset 14h	10000h
16h	1Dh	Redirection Table Entry 3 (RTE3)—Offset 16h	10000h
18h	1Fh	Redirection Table Entry 4 (RTE4)—Offset 18h	10000h
1Ah	21h	Redirection Table Entry 5 (RTE5)—Offset 1Ah	10000h
1Ch	23h	Redirection Table Entry 6 (RTE6)—Offset 1Ch	10000h
1Eh	25h	Redirection Table Entry 7 (RTE7)—Offset 1Eh	10000h
20h	27h	Redirection Table Entry 8 (RTE8)—Offset 20h	10000h
22h	29h	Redirection Table Entry 9 (RTE9)—Offset 22h	10000h
24h	2Bh	Redirection Table Entry 10 (RTE10)—Offset 24h	10000h
26h	2Dh	Redirection Table Entry 11 (RTE11)—Offset 26h	10000h
28h	2Fh	Redirection Table Entry 12 (RTE12)—Offset 28h	10000h
2Ah	31h	Redirection Table Entry 13 (RTE13)—Offset 2Ah	10000h
2Ch	33h	Redirection Table Entry 14 (RTE14)—Offset 2Ch	10000h
2Eh	35h	Redirection Table Entry 15 (RTE15)—Offset 2Eh	10000h
30h	37h	Redirection Table Entry 16 (RTE16)—Offset 30h	10000h
32h	39h	Redirection Table Entry 17 (RTE17)—Offset 32h	10000h
34h	3Bh	Redirection Table Entry 18 (RTE18)—Offset 34h	10000h
36h	3Dh	Redirection Table Entry 19 (RTE19)—Offset 36h	10000h
38h	3Fh	Redirection Table Entry 20 (RTE20)—Offset 38h	10000h
3Ah	41h	Redirection Table Entry 21 (RTE21)—Offset 3Ah	10000h
3Ch	43h	Redirection Table Entry 22 (RTE22)—Offset 3Ch	10000h
3Eh	45h	Redirection Table Entry 23 (RTE23)—Offset 3Eh	10000h
40h	47h	Redirection Table Entry 24 (RTE24)—Offset 40h	10000h
42h	49h	Redirection Table Entry 25 (RTE25)—Offset 42h	10000h
44h	4Bh	Redirection Table Entry 26 (RTE26)—Offset 44h	10000h
46h	4Dh	Redirection Table Entry 27 (RTE27)—Offset 46h	10000h
48h	4Fh	Redirection Table Entry 28 (RTE28)—Offset 48h	10000h
4Ah	51h	Redirection Table Entry 29 (RTE29)—Offset 4Ah	10000h
4Ch	53h	Redirection Table Entry 30 (RTE30)—Offset 4Ch	10000h
4Eh	55h	Redirection Table Entry 31 (RTE31)—Offset 4Eh	10000h
50h	57h	Redirection Table Entry 32 (RTE32)—Offset 50h	10000h

Table 15-1. Summary of 0_31_0_APIC MEM Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
52h	59h	Redirection Table Entry 33 (RTE33)—Offset 52h	10000h
54h	5Bh	Redirection Table Entry 34 (RTE34)—Offset 54h	10000h
56h	5Dh	Redirection Table Entry 35 (RTE35)—Offset 56h	10000h
58h	5Fh	Redirection Table Entry 36 (RTE36)—Offset 58h	10000h
5Ah	61h	Redirection Table Entry 37 (RTE37)—Offset 5Ah	10000h
5Ch	63h	Redirection Table Entry 38 (RTE38)—Offset 5Ch	10000h
5Eh	65h	Redirection Table Entry 39 (RTE39)—Offset 5Eh	10000h
60h	67h	Redirection Table Entry 40 (RTE40)—Offset 60h	10000h
62h	69h	Redirection Table Entry 41 (RTE41)—Offset 62h	10000h
64h	6Bh	Redirection Table Entry 42 (RTE42)—Offset 64h	10000h
66h	6Dh	Redirection Table Entry 43 (RTE43)—Offset 66h	10000h
68h	6Fh	Redirection Table Entry 44 (RTE44)—Offset 68h	10000h
6Ah	71h	Redirection Table Entry 45 (RTE45)—Offset 6Ah	10000h
6Ch	73h	Redirection Table Entry 46 (RTE46)—Offset 6Ch	10000h
6Eh	75h	Redirection Table Entry 47 (RTE47)—Offset 6Eh	10000h
70h	77h	Redirection Table Entry 48 (RTE48)—Offset 70h	10000h
72h	79h	Redirection Table Entry 49 (RTE49)—Offset 72h	10000h
74h	7Bh	Redirection Table Entry 50 (RTE50)—Offset 74h	10000h
76h	7Dh	Redirection Table Entry 51 (RTE51)—Offset 76h	10000h
78h	7Fh	Redirection Table Entry 52 (RTE52)—Offset 78h	10000h
7Ah	81h	Redirection Table Entry 53 (RTE53)—Offset 7Ah	10000h
7Ch	83h	Redirection Table Entry 54 (RTE54)—Offset 7Ch	10000h
7Eh	85h	Redirection Table Entry 55 (RTE55)—Offset 7Eh	10000h
80h	87h	Redirection Table Entry 56 (RTE56)—Offset 80h	10000h
82h	89h	Redirection Table Entry 57 (RTE57)—Offset 82h	10000h
84h	8Bh	Redirection Table Entry 58 (RTE58)—Offset 84h	10000h
86h	8Dh	Redirection Table Entry 59 (RTE59)—Offset 86h	10000h
88h	8Fh	Redirection Table Entry 60 (RTE60)—Offset 88h	10000h
8Ah	91h	Redirection Table Entry 61 (RTE61)—Offset 8Ah	10000h
8Ch	93h	Redirection Table Entry 62 (RTE62)—Offset 8Ch	10000h
8Eh	95h	Redirection Table Entry 63 (RTE63)—Offset 8Eh	10000h
90h	97h	Redirection Table Entry 64 (RTE64)—Offset 90h	10000h
92h	99h	Redirection Table Entry 65 (RTE65)—Offset 92h	10000h
94h	9Bh	Redirection Table Entry 66 (RTE66)—Offset 94h	10000h
96h	9Dh	Redirection Table Entry 67 (RTE67)—Offset 96h	10000h
98h	9Fh	Redirection Table Entry 68 (RTE68)—Offset 98h	10000h
9Ah	A1h	Redirection Table Entry 69 (RTE69)—Offset 9Ah	10000h
9Ch	A3h	Redirection Table Entry 70 (RTE70)—Offset 9Ch	10000h
9Eh	A5h	Redirection Table Entry 71 (RTE71)—Offset 9Eh	10000h
A0h	A7h	Redirection Table Entry 72 (RTE72)—Offset A0h	10000h

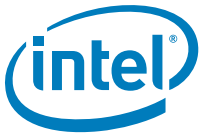


Table 15-1. Summary of 0_31_0_APIC MEM Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
A2h	A9h	Redirection Table Entry 73 (RTE73)—Offset A2h	10000h
A4h	ABh	Redirection Table Entry 74 (RTE74)—Offset A4h	10000h
A6h	ADh	Redirection Table Entry 75 (RTE75)—Offset A6h	10000h
A8h	AFh	Redirection Table Entry 76 (RTE76)—Offset A8h	10000h
AAh	B1h	Redirection Table Entry 77 (RTE77)—Offset AAh	10000h
ACh	B3h	Redirection Table Entry 78 (RTE78)—Offset ACh	10000h
AEh	B5h	Redirection Table Entry 79 (RTE79)—Offset AEh	10000h
B0h	B7h	Redirection Table Entry 80 (RTE80)—Offset B0h	10000h
B2h	B9h	Redirection Table Entry 81 (RTE81)—Offset B2h	10000h
B4h	BBh	Redirection Table Entry 82 (RTE82)—Offset B4h	10000h
B6h	BDh	Redirection Table Entry 83 (RTE83)—Offset B6h	10000h
B8h	BFh	Redirection Table Entry 84 (RTE84)—Offset B8h	10000h
BAh	C1h	Redirection Table Entry 85 (RTE85)—Offset BAh	10000h
BCh	C3h	Redirection Table Entry 86 (RTE86)—Offset BCh	10000h
BEh	C5h	Redirection Table Entry 87 (RTE87)—Offset BEh	10000h
C0h	C7h	Redirection Table Entry 88 (RTE88)—Offset C0h	10000h
C2h	C9h	Redirection Table Entry 89 (RTE89)—Offset C2h	10000h
C4h	CBh	Redirection Table Entry 90 (RTE90)—Offset C4h	10000h
C6h	CDh	Redirection Table Entry 91 (RTE91)—Offset C6h	10000h
C8h	CFh	Redirection Table Entry 92 (RTE92)—Offset C8h	10000h
CAh	D1h	Redirection Table Entry 93 (RTE93)—Offset CAh	10000h
CCh	D3h	Redirection Table Entry 94 (RTE94)—Offset CCh	10000h
CEh	D5h	Redirection Table Entry 95 (RTE95)—Offset CEh	10000h
D0h	D7h	Redirection Table Entry 96 (RTE96)—Offset D0h	10000h
D2h	D9h	Redirection Table Entry 97 (RTE97)—Offset D2h	10000h
D4h	DBh	Redirection Table Entry 98 (RTE98)—Offset D4h	10000h
D6h	DDh	Redirection Table Entry 99 (RTE99)—Offset D6h	10000h
D8h	DFh	Redirection Table Entry 100 (RTE100)—Offset D8h	10000h
DAh	E1h	Redirection Table Entry 101 (RTE101)—Offset DAh	10000h
DCh	E3h	Redirection Table Entry 102 (RTE102)—Offset DCh	10000h
DEh	E5h	Redirection Table Entry 103 (RTE103)—Offset DEh	10000h
E0h	E7h	Redirection Table Entry 104 (RTE104)—Offset E0h	10000h
E2h	E9h	Redirection Table Entry 105 (RTE105)—Offset E2h	10000h
E4h	EBh	Redirection Table Entry 106 (RTE106)—Offset E4h	10000h
E6h	EDh	Redirection Table Entry 107 (RTE107)—Offset E6h	10000h
E8h	EFh	Redirection Table Entry 108 (RTE108)—Offset E8h	10000h
EAh	F1h	Redirection Table Entry 109 (RTE109)—Offset EAh	10000h
ECh	F3h	Redirection Table Entry 110 (RTE110)—Offset ECh	10000h
EEh	F5h	Redirection Table Entry 111 (RTE111)—Offset EEh	10000h
F0h	F7h	Redirection Table Entry 112 (RTE112)—Offset F0h	10000h

Table 15-1. Summary of 0_31_0_APIC MEM Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
F2h	F9h	Redirection Table Entry 113 (RTE113)—Offset F2h	10000h
F4h	FBh	Redirection Table Entry 114 (RTE114)—Offset F4h	10000h
F6h	FDh	Redirection Table Entry 115 (RTE115)—Offset F6h	10000h
F8h	FFh	Redirection Table Entry 116 (RTE116)—Offset F8h	10000h
FAh	101h	Redirection Table Entry 117 (RTE117)—Offset FAh	10000h
FCh	103h	Redirection Table Entry 118 (RTE118)—Offset FCh	10000h
FEh	105h	Redirection Table Entry 119 (RTE119)—Offset FEh	10000h
3100h		PIRQA Routing Control (PARC)—Offset 3100h	80h
3101h		PIRQB Routing Control (PBRC)—Offset 3101h	80h
3102h		PIRQC Routing Control (PCRC)—Offset 3102h	80h
3103h		PIRQD Routing Control (PDRC)—Offset 3103h	80h
3104h		PIRQE Routing Control (PERC)—Offset 3104h	80h
3105h		PIRQF Routing Control (PFRC)—Offset 3105h	80h
3106h		PIRQG Routing Control (PGRC)—Offset 3106h	80h
3107h		PIRQH Routing Control (PHRC)—Offset 3107h	80h
3140h		PCI Interrupt Route 0 (PIR0)—Offset 3140h	3210h
3142h		PCI Interrupt Route 1 (PIR1)—Offset 3142h	3210h
3144h		PCI Interrupt Route 2 (PIR2)—Offset 3144h	3210h
3146h		PCI Interrupt Route 3(PIR3)—Offset 3146h	3210h
3148h		PCI Interrupt Route 4 (PIR4)—Offset 3148h	3210h
314Ah		PCI Interrupt Route 5 (PIR5)—Offset 314Ah	3210h
314Ch		PCI Interrupt Route 6 (PIR6)—Offset 314Ch	3210h
316Eh		PCI Interrupt Route 7 (PIR7)—Offset 314Eh	3210h
3150h		PCI Interrupt Route 8 (PIR8)—Offset 3150h	3210h
3152h		PCI Interrupt Route 9 (PIR9)—Offset 3152h	3210h
3154h		PCI Interrupt Route 10 (PIR10)—Offset 3154h	3210h
3156h		PCI Interrupt Route 11 (PIR11)—Offset 3156h	3210h
3158h		PCI Interrupt Route 12 (PIR12)—Offset 3158h	3210h
3200h		Interrupt Polarity Control 0 (IPC0)—Offset 3200h	FFh
3204h		Interrupt Polarity Control 1 (IPC1)—Offset 3204h	0h
3208h		Interrupt Polarity Control 2 (IPC2)—Offset 3208h	0h
320Ch		Interrupt Polarity Control 3 (IPC3)—Offset 320Ch	0h
3330h		ITSS Power Reduction Control (ITSSPRC)—Offset 3300h	0h
3334h		SIDE Clock Timing (SIDECT)—Offset 3304h	33h

15.1.1 Version (VS)—Offset 1h

*offset 01h - 01h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 770020h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved
23:16	77h RW/O	**Maximum Redirection Entries (MRE):** This is the entry number (0 being the lowest entry) of the highest entry in the redirection table. In PCH this field is defaulted to 17h to indicate 24 interrupts. This field is Read-Write-Once. BIOS must write to this field after PLTRST# to lockdown the value. This allows BIOS to utilize some of the entries for its own purpose and thus advertising fewer IOxAPIC Redirection Entries to OS. BIOS may to program this field up to 78h (maximum 120 entries) .
15	0h RO	**Pin Assertion Register Supported (PRQ):** Indicate that the IOxAPIC does not implement the Pin Assertion Register.
14:8	0h RO	**Reserved (RSVD_1):** Reserved
7:0	20h RO	**Version (VS):** Identifies the implementation version as IOxAPIC.

15.1.2 Redirection Table Entry 0 (RTE0)—Offset 10h

*offset 10h - 11h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.3 Redirection Table Entry 1 (RTE1)—Offset 12h

*offset 12h - 13h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.4 Redirection Table Entry 2 (RTE2)—Offset 14h

*offset 14h - 15h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC

Bit Range	Default & Access	Field Name (ID): Description
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

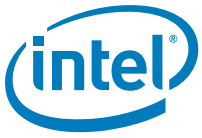
15.1.5 Redirection Table Entry 3 (RTE3)—Offset 16h

*offset 16h - 17h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h



Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.6 Redirection Table Entry 4 (RTE4)—Offset 18h

*offset 18h - 19h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.7 Redirection Table Entry 5 (RTE5)—Offset 1Ah

*offset 1Ah - 1Bh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.8 Redirection Table Entry 6 (RTE6)—Offset 1Ch

*offset 1Ch - 1Dh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.9 Redirection Table Entry 7 (RTE7)—Offset 1Eh

*offset 1Eh - 1Fh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.10 Redirection Table Entry 8 (RTE8)—Offset 20h

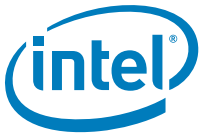
*offset 20h - 21h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.



Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.11 Redirection Table Entry 9 (RTE9)—Offset 22h

*offset 22h - 23h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.12 Redirection Table Entry 10 (RTE10)—Offset 24h

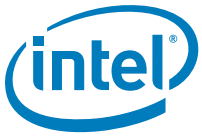
*offset 24h - 25h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.



Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.13 Redirection Table Entry 11 (RTE11)—Offset 26h

*offset 26h - 27h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.14 Redirection Table Entry 12 (RTE12)—Offset 28h

*offset 28h - 29h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC

Bit Range	Default & Access	Field Name (ID): Description
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.15 Redirection Table Entry 13 (RTE13)—Offset 2Ah

*offset 2Ah - 2Bh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.16 Redirection Table Entry 14 (RTE14)—Offset 2Ch

*offset 2Ch - 2Dh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.17 Redirection Table Entry 15 (RTE15)—Offset 2Eh

*offset 2Eh - 2Fh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.18 Redirection Table Entry 16 (RTE16)—Offset 30h

*offset 30h - 31h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.19 Redirection Table Entry 17 (RTE17)—Offset 32h

*offset 32h - 33h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.20 Redirection Table Entry 18 (RTE18)—Offset 34h

*offset 34h - 35h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.21 Redirection Table Entry 19 (RTE19)—Offset 36h

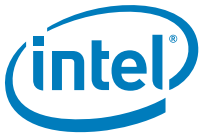
*offset 36h - 37h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.



Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.22 Redirection Table Entry 20 (RTE20)—Offset 38h

*offset 38h - 39h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.23 Redirection Table Entry 21 (RTE21)—Offset 3Ah

*offset 3Ah - 3Bh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.24 Redirection Table Entry 22 (RTE22)—Offset 3Ch

*offset 3Ch - 3Dh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC

Bit Range	Default & Access	Field Name (ID): Description
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

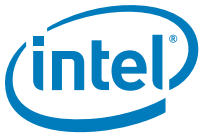
15.1.25 Redirection Table Entry 23 (RTE23)—Offset 3Eh

*offset 3Eh - 3Fh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h



Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.26 Redirection Table Entry 24 (RTE24)—Offset 40h

*offset 40h - 41h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

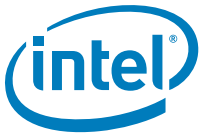
Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.27 Redirection Table Entry 25 (RTE25)—Offset 42h

*offset 42h - 43h

Access Method



Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.28 Redirection Table Entry 26 (RTE26)—Offset 44h

*offset 44h - 45h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.29 Redirection Table Entry 27 (RTE27)—Offset 46h

*offset 46h - 47h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.30 Redirection Table Entry 28 (RTE28)—Offset 48h

*offset 48h - 49h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.31 Redirection Table Entry 29 (RTE29)—Offset 4Ah

*offset 4Ah - 4Bh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.32 Redirection Table Entry 30 (RTE30)—Offset 4Ch

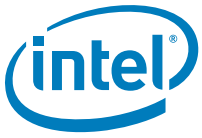
*offset 4Ch - 4Dh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.



Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.33 Redirection Table Entry 31 (RTE31)—Offset 4Eh

*offset 4Eh - EFh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.34 Redirection Table Entry 32 (RTE32)—Offset 50h

*offset 50h - 51h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC

Bit Range	Default & Access	Field Name (ID): Description
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.35 Redirection Table Entry 33 (RTE33)—Offset 52h

*offset 52h - 53h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.36 Redirection Table Entry 34 (RTE34)—Offset 54h

*offset 54h - 55h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.37 Redirection Table Entry 35 (RTE35)—Offset 56h

*offset 56h - 57h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.38 Redirection Table Entry 36 (RTE36)—Offset 58h

*offset 58h - 59h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.39 Redirection Table Entry 37 (RTE37)—Offset 5Ah

*offset 5Ah - 5Bh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.40 Redirection Table Entry 38 (RTE38)—Offset 5Ch

*offset 5Ch - 5Dh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.41 Redirection Table Entry 39 (RTE39)—Offset 5Eh

*offset 5Eh - 5Fh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.42 Redirection Table Entry 40 (RTE40)—Offset 60h

*offset 60h - 61h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.43 Redirection Table Entry 41 (RTE41)—Offset 62h

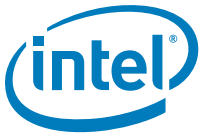
*offset 62h - 63h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.44 Redirection Table Entry 42 (RTE42)—Offset 64h

*offset 64h - 65h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC

Bit Range	Default & Access	Field Name (ID): Description
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.45 Redirection Table Entry 43 (RTE43)—Offset 66h

*offset 66h - 67h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.46 Redirection Table Entry 44 (RTE44)—Offset 68h

*offset 68h - 69h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.47 Redirection Table Entry 45 (RTE45)—Offset 6Ah

*offset 6Ah - 6Bh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.48 Redirection Table Entry 46 (RTE46)—Offset 6Ch

*offset 6Ch - 6Dh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.49 Redirection Table Entry 47 (RTE47)—Offset 6Eh

*offset 6Eh - 6Fh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.50 Redirection Table Entry 48 (RTE48)—Offset 70h

*offset 70h - 71h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.51 Redirection Table Entry 49 (RTE49)—Offset 72h

*offset 72h - 73h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.52 Redirection Table Entry 50 (RTE50)—Offset 74h

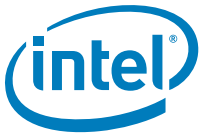
*offset 74h - 75h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.



Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.53 Redirection Table Entry 51 (RTE51)—Offset 76h

*offset 76h - 77h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.54 Redirection Table Entry 52 (RTE52)—Offset 78h

*offset 78h - 79h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC

Bit Range	Default & Access	Field Name (ID): Description
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.55 Redirection Table Entry 53 (RTE53)—Offset 7Ah

*offset 7Ah - 7Bh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.56 Redirection Table Entry 54 (RTE54)—Offset 7Ch

*offset 7Ch - 7Dh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.57 Redirection Table Entry 55 (RTE55)—Offset 7Eh

*offset 7Eh - 7Fh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.58 Redirection Table Entry 56 (RTE56)—Offset 80h

*offset 80h - 81h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.59 Redirection Table Entry 57 (RTE57)—Offset 82h

*offset 82h - 83h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.60 Redirection Table Entry 58 (RTE58)—Offset 84h

*offset 84h - 85h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.61 Redirection Table Entry 59 (RTE59)—Offset 86h

*offset 86h - 87h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.62 Redirection Table Entry 60 (RTE60)—Offset 88h

*offset 88h - 89h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.63 Redirection Table Entry 61 (RTE61)—Offset 8Ah

*offset 8Ah - 8Bh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.64 Redirection Table Entry 62 (RTE62)—Offset 8Ch

*offset 8Ch - 8Dh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC

Bit Range	Default & Access	Field Name (ID): Description
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.65 Redirection Table Entry 63 (RTE63)—Offset 8Eh

*offset 8Eh - 8Fh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.66 Redirection Table Entry 64 (RTE64)—Offset 90h

*offset 90h - 91h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.67 Redirection Table Entry 65 (RTE65)—Offset 92h

*offset 92h - 93h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.68 Redirection Table Entry 66 (RTE66)—Offset 94h

*offset 94h - 95h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.69 Redirection Table Entry 67 (RTE67)—Offset 96h

*offset 96h - 97h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.70 Redirection Table Entry 68 (RTE68)—Offset 98h

*offset 98h - 99h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.71 Redirection Table Entry 69 (RTE69)—Offset 9Ah

*offset 9Ah - 9Bh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.72 Redirection Table Entry 70 (RTE70)—Offset 9Ch

*offset 9Ch - 9Dh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.73 Redirection Table Entry 71 (RTE71)—Offset 9Eh

*offset 9Eh - 9Fh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.74 Redirection Table Entry 72 (RTE72)—Offset A0h

*offset A0h - A1h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC

Bit Range	Default & Access	Field Name (ID): Description
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.75 Redirection Table Entry 73 (RTE73)—Offset A2h

*offset A2h - A3h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.76 Redirection Table Entry 74 (RTE74)—Offset A4h

*offset A4h - A5h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.77 Redirection Table Entry 75 (RTE75)—Offset A6h

*offset A6h - A7h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.78 Redirection Table Entry 76 (RTE76)—Offset A8h

*offset A8h - A9h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.79 Redirection Table Entry 77 (RTE77)—Offset AAh

*offset AAh - ABh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.80 Redirection Table Entry 78 (RTE78)—Offset ACh

*offset ACh - ADh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.81 Redirection Table Entry 79 (RTE79)—Offset AEh

*offset AEh - AFh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.82 Redirection Table Entry 80 (RTE80)—Offset B0h

*offset B0h - B1h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.83 Redirection Table Entry 81 (RTE81)—Offset B2h

*offset B2h - B3h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.84 Redirection Table Entry 82 (RTE82)—Offset B4h

*offset B4h - B5h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC

Bit Range	Default & Access	Field Name (ID): Description
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.85 Redirection Table Entry 83 (RTE83)—Offset B6h

*offset B6h - B7h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.86 Redirection Table Entry 84 (RTE84)—Offset B8h

*offset B8h - B9h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.87 Redirection Table Entry 85 (RTE85)—Offset BAh

*offset BAh - BBh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.88 Redirection Table Entry 86 (RTE86)—Offset BCh

*offset BCh - BDh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.89 Redirection Table Entry 87 (RTE87)—Offset BEh

*offset BEh - BFh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.90 Redirection Table Entry 88 (RTE88)—Offset C0h

*offset C0h - C1h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.91 Redirection Table Entry 89 (RTE89)—Offset C2h

*offset C2h - C3h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.92 Redirection Table Entry 90 (RTE90)—Offset C4h

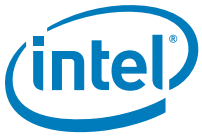
*offset C4h - C5h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.



Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.93 Redirection Table Entry 91 (RTE91)—Offset C6h

*offset C6h - C7h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.94 Redirection Table Entry 92 (RTE92)—Offset C8h

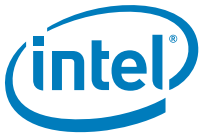
*offset C8h - C9h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC



Bit Range	Default & Access	Field Name (ID): Description
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.95 Redirection Table Entry 93 (RTE93)—Offset CAh

*offset CAh - CBh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.96 Redirection Table Entry 94 (RTE94)—Offset CCh

*offset CCh - CDh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.97 Redirection Table Entry 95 (RTE95)—Offset CEh

*offset CEh - CFh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.98 Redirection Table Entry 96 (RTE96)—Offset D0h

*offset D0h - D1h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.99 Redirection Table Entry 97 (RTE97)—Offset D2h

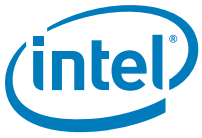
*offset D2h - D3h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.100 Redirection Table Entry 98 (RTE98)—Offset D4h

*offset D4h - D5h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.101 Redirection Table Entry 99 (RTE99)—Offset D6h

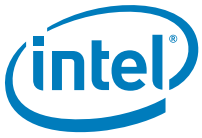
*offset D6h - D7h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.



Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.102 Redirection Table Entry 100 (RTE100)—Offset D8h

*offset D8h - D9h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.103 Redirection Table Entry 101 (RTE101)—Offset DAh

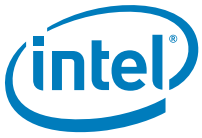
*offset DAh - DBh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.104 Redirection Table Entry 102 (RTE102)—Offset DCh

*offset DCh - DDh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC

Bit Range	Default & Access	Field Name (ID): Description
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

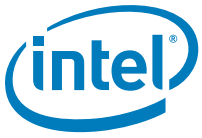
15.1.105 Redirection Table Entry 103 (RTE103)—Offset DEh

*offset DEh - DFh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h



Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.106 Redirection Table Entry 104 (RTE104)—Offset E0h

*offset E0h - E1h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.107 Redirection Table Entry 105 (RTE105)—Offset E2h

*offset E2h - E3h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.108 Redirection Table Entry 106 (RTE106)—Offset E4h

*offset E4h - E5h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.109 Redirection Table Entry 107 (RTE107)—Offset E6h

*offset E6h - E7h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.110 Redirection Table Entry 108 (RTE108)—Offset E8h

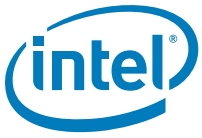
*offset E8h - E9h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.



Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.111 Redirection Table Entry 109 (RTE109)—Offset EAh

*offset EAh - EBh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.112 Redirection Table Entry 110 (RTE110)—Offset ECh

*offset ECh - EDh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.113 Redirection Table Entry 111 (RTE111)—Offset EEh

*offset EEh - EFh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.114 Redirection Table Entry 112 (RTE112)—Offset F0h

*offset F0h - F1h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC

Bit Range	Default & Access	Field Name (ID): Description
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.115 Redirection Table Entry 113 (RTE113)—Offset F2h

*offset F2h - F3h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.116 Redirection Table Entry 114 (RTE114)—Offset F4h

*offset F4h - F5h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.117 Redirection Table Entry 115 (RTE115)—Offset F6h

*offset F6h - F7h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.118 Redirection Table Entry 116 (RTE116)—Offset F8h

*offset F8h - F9h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.119 Redirection Table Entry 117 (RTE117)—Offset FAh

*offset FAh - FBh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.120 Redirection Table Entry 118 (RTE118)—Offset FCh

*offset FCh - FDh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.121 Redirection Table Entry 119 (RTE119)—Offset FEh

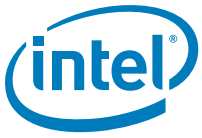
*offset FEh - FFh

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
47:17	0h RO	**Reserved (RSVD):** Reserved
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts - its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.



Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported (see Section 13.2.3 for details). 011 Reserved 100 NMI Not supported (see Section 13.2.3 for details). 101 INIT Not supported (see Section 13.2.3 for details). 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

15.1.122 PIRQA Routing Control (PARC)—Offset 3100h

PIRQA Routing Control Register

Access Method

Type: CR Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Range	Access Type	Default (reset)	Description
7:7	RW	0x1 (Core)	**REN (Interrupt Routing Enable)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
3:0	RW	0x0 (Core)	**IR (IRQ Routing)** Bits Mapping Bits Mapping 0000 Reserved 1000 Reserved 0001 Reserved 1001 IRQ9 0010 Reserved 1010 IRQ10 0011 IRQ3 1011 IRQ11 0100 IRQ4 1100 IRQ12 0101 IRQ5 1101 Reserved 0110 IRQ6 1110 IRQ14 0111 IRQ7 1111 IRQ15

15.1.123 PIRQB Routing Control (PBRC)—Offset 3101h

Routing for PIRQB#. Uses the same programming values as PARC.

Note that external PIRQB# is no longer supported.

Access Method

Type: CR Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Range	Access Type	Default (reset)	Description
7:7	RW	0x1 (Core)	**REN (Interrupt Routing Enable)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
3:0	RW	0x0 (Core)	**IR (IRQ Routing)** Bits Mapping Bits Mapping 0000 Reserved 1000 Reserved 0001 Reserved 1001 IRQ9 0010 Reserved 1010 IRQ10 0011 IRQ3 1011 IRQ11 0100 IRQ4 1100 IRQ12 0101 IRQ5 1101 Reserved 0110 IRQ6 1110 IRQ14 0111 IRQ7 1111 IRQ15

15.1.124 PIRQC Routing Control (PCRC)—Offset 3102h

Routing for PIRQC#. Uses the same programming values as PARC.

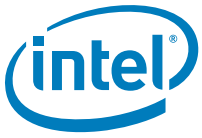
Note that external PIRQC# is no longer supported.

Access Method

Type: CR Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Range	Access Type	Default (reset)	Description
7:7	RW	0x1 (Core)	**REN (Interrupt Routing Enable)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.



Range	Access Type	Default (reset)	Description
6:4	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
3:0	RW	0x0 (Core)	**IR (IRQ Routing)** Bits Mapping Bits Mapping 0000 Reserved 1000 Reserved 0001 Reserved 1001 IRQ9 0010 Reserved 1010 IRQ10 0011 IRQ3 1011 IRQ11 0100 IRQ4 1100 IRQ12 0101 IRQ5 1101 Reserved 0110 IRQ6 1110 IRQ14 0111 IRQ7 1111 IRQ15

15.1.125 PIRQD Routing Control (PDRC)—Offset 3103h

Routing for PIRQD#. Uses the same programming values as PARC.

Note that external PIRQD# is no longer supported.

Access Method

Type: CR Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Range	Access Type	Default (reset)	Description
7:7	RW	0x1 (Core)	**REN (Interrupt Routing Enable)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
3:0	RW	0x0 (Core)	**IR (IRQ Routing)** Bits Mapping Bits Mapping 0000 Reserved 1000 Reserved 0001 Reserved 1001 IRQ9 0010 Reserved 1010 IRQ10 0011 IRQ3 1011 IRQ11 0100 IRQ4 1100 IRQ12 0101 IRQ5 1101 Reserved 0110 IRQ6 1110 IRQ14 0111 IRQ7 1111 IRQ15

15.1.126 PIRQE Routing Control (PERC)—Offset 3104h

Routing for PIRQE#. Uses the same programming values as PARC.

Note that external PIRQE# is no longer supported.

Access Method

Type: CR Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Range	Access Type	Default (reset)	Description
7:7	RW	0x1 (Core)	**REN (Interrupt Routing Enable)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
3:0	RW	0x0 (Core)	**IR (IRQ Routing)** Bits Mapping Bits Mapping 0000 Reserved 1000 Reserved 0001 Reserved 1001 IRQ9 0010 Reserved 1010 IRQ10 0011 IRQ3 1011 IRQ11 0100 IRQ4 1100 IRQ12 0101 IRQ5 1101 Reserved 0110 IRQ6 1110 IRQ14 0111 IRQ7 1111 IRQ15

15.1.127 PIRQF Routing Control (PFRC)—Offset 3105h

Routing for PIRQF#. Uses the same programming values as PARC.

Note that external PIRQF# is no longer supported.

Access Method

Type: CR Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Range	Access Type	Default (reset)	Description
7:7	RW	0x1 (Core)	**REN (Interrupt Routing Enable)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	RO	0x0 (Core)	**RSVD (Reserved)** Reserved

Range	Access Type	Default (reset)	Description
3:0	RW	0x0 (Core)	**IR (IRQ Routing)** Bits Mapping Bits Mapping 0000 Reserved 1000 Reserved 0001 Reserved 1001 IRQ9 0010 Reserved 1010 IRQ10 0011 IRQ3 1011 IRQ11 0100 IRQ4 1100 IRQ12 0101 IRQ5 1101 Reserved 0110 IRQ6 1110 IRQ14 0111 IRQ7 1111 IRQ15

15.1.128 PIRQG Routing Control (PGRC)—Offset 3106h

Routing for PIRQG#. Uses the same programming values as PARC.

Note that external PIRQG# is no longer supported.

Access Method

Type: CR Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Range	Access Type	Default (reset)	Description
7:7	RW	0x1 (Core)	**REN (Interrupt Routing Enable)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
3:0	RW	0x0 (Core)	**IR (IRQ Routing)** Bits Mapping Bits Mapping 0000 Reserved 1000 Reserved 0001 Reserved 1001 IRQ9 0010 Reserved 1010 IRQ10 0011 IRQ3 1011 IRQ11 0100 IRQ4 1100 IRQ12 0101 IRQ5 1101 Reserved 0110 IRQ6 1110 IRQ14 0111 IRQ7 1111 IRQ15

15.1.129 PIRQH Routing Control (PHRC)—Offset 3107h

Routing for PIRQH#. Uses the same programming values as PARC.

Note that external PIRQH# is no longer supported.

Access Method

Type: CR Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Range	Access Type	Default (reset)	Description
7:7	RW	0x1 (Core)	**REN (Interrupt Routing Enable)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
3:0	RW	0x0 (Core)	**IR (IRQ Routing)** Bits Mapping Bits Mapping 0000 Reserved 1000 Reserved 0001 Reserved 1001 IRQ9 0010 Reserved 1010 IRQ10 0011 IRQ3 1011 IRQ11 0100 IRQ4 1100 IRQ12 0101 IRQ5 1101 Reserved 0110 IRQ6 1110 IRQ14 0111 IRQ7 1111 IRQ15

15.1.130 PCI Interrupt Route 0 (PIR0)—Offset 3140h

PCI Interrupt Route 0 Register.

Access Method

Type: CR Register (Size: 16 bits)	**Device:** **Function:**

Default: 3210h

Range	Access Type	Default (reset)	Description
15:15	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
14:12	RW	0x3 (Core)	**IDR (Interrupt D Pin Route)** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#
11:11	RO	0x0 (Core)	**RSVD_1 (Reserved)** Reserved

Range	Access Type	Default (reset)	Description
10:8	RW	0x2 (Core)	**ICR (Interrupt C Pin Route)** See the IDR description. This field applies to INTC#
7:7	RO	0x0 (Core)	**RSVD_2 (Reserved)** Reserved
6:4	RW	0x1 (Core)	**IBR (Interrupt B Pin Route)** See the IDR description. This field applies to INTB#.
3:3	RO	0x0 (Core)	**RSVD_3 (Reserved)** Reserved
2:0	RW	0x0 (Core)	**IAR (Interrupt A Pin Route)** See the IDR description. This field applies to INTA#.

15.1.131 PCI Interrupt Route 1 (PIR1)—Offset 3142h

PCI Interrupt Route 1 Register.

Access Method

Type: CR Register (Size: 16 bits)	**Device:** **Function:**

Default: 3210h

Range	Access Type	Default (reset)	Description
15:15	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
14:12	RW	0x3 (Core)	**IDR (Interrupt D Pin Route)** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#
11:11	RO	0x0 (Core)	**RSVD_1 (Reserved)** Reserved
10:8	RW	0x2 (Core)	**ICR (Interrupt C Pin Route)** See the IDR description. This field applies to INTC#
7:7	RO	0x0 (Core)	**RSVD_2 (Reserved)** Reserved
6:4	RW	0x1 (Core)	**IBR (Interrupt B Pin Route)** See the IDR description. This field applies to INTB#.

Range	Access Type	Default (reset)	Description
3:3	RO	0x0 (Core)	**RSVD_3 (Reserved)** Reserved
2:0	RW	0x0 (Core)	**IAR (Interrupt A Pin Route)** See the IDR description. This field applies to INTA#.

15.1.132 PCI Interrupt Route 2 (PIR2)—Offset 3144h

PCI Interrupt Route 2 Register.

Access Method

Type: CR Register (Size: 16 bits)	**Device:** **Function:**

Default: 3210h

Range	Access Type	Default (reset)	Description
15:15	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
14:12	RW	0x3 (Core)	**IDR (Interrupt D Pin Route)** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#
11:11	RO	0x0 (Core)	**RSVD_1 (Reserved)** Reserved
10:8	RW	0x2 (Core)	**ICR (Interrupt C Pin Route)** See the IDR description. This field applies to INTC#
7:7	RO	0x0 (Core)	**RSVD_2 (Reserved)** Reserved
6:4	RW	0x1 (Core)	**IBR (Interrupt B Pin Route)** See the IDR description. This field applies to INTB#.
3:3	RO	0x0 (Core)	**RSVD_3 (Reserved)** Reserved
2:0	RW	0x0 (Core)	**IAR (Interrupt A Pin Route)** See the IDR description. This field applies to INTA#.

15.1.133 PCI Interrupt Route 3(PIR3)—Offset 3146h

PCI Interrupt Route 3 Register.

Access Method

Type: CR Register (Size: 16 bits)	**Device:** **Function:**

Default: 3210h

Range	Access Type	Default (reset)	Description
15:15	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
14:12	RW	0x3 (Core)	**IDR (Interrupt D Pin Route)** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#
11:11	RO	0x0 (Core)	**RSVD_1 (Reserved)** Reserved
10:8	RW	0x2 (Core)	**ICR (Interrupt C Pin Route)** See the IDR description. This field applies to INTC#
7:7	RO	0x0 (Core)	**RSVD_2 (Reserved)** Reserved
6:4	RW	0x1 (Core)	**IBR (Interrupt B Pin Route)** See the IDR description. This field applies to INTB#.
3:3	RO	0x0 (Core)	**RSVD_3 (Reserved)** Reserved
2:0	RW	0x0 (Core)	**IAR (Interrupt A Pin Route)** See the IDR description. This field applies to INTA#.

15.1.134 PCI Interrupt Route 4 (PIR4)—Offset 3148h

PCI Interrupt Route 4 Register.

Access Method

Type: CR Register (Size: 16 bits)	**Device:** **Function:**

Default: 3210h

Range	Access Type	Default (reset)	Description
15:15	RO	0x0 (Core)	**RSVD (Reserved)** Reserved

Range	Access Type	Default (reset)	Description
14:12	RW	0x3 (Core)	**IDR (Interrupt D Pin Route)** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#
11:11	RO	0x0 (Core)	**RSVD_1 (Reserved)** Reserved
10:8	RW	0x2 (Core)	**ICR (Interrupt C Pin Route)** See the IDR description. This field applies to INTC#
7:7	RO	0x0 (Core)	**RSVD_2 (Reserved)** Reserved
6:4	RW	0x1 (Core)	**IBR (Interrupt B Pin Route)** See the IDR description. This field applies to INTB#.
3:3	RO	0x0 (Core)	**RSVD_3 (Reserved)** Reserved
2:0	RW	0x0 (Core)	**IAR (Interrupt A Pin Route)** See the IDR description. This field applies to INTA#.

15.1.135 PCI Interrupt Route 5 (PIR5)—Offset 314Ah

PCI Interrupt Route 5 Register.

Access Method

Type: CR Register (Size: 16 bits)	**Device:** **Function:**

Default: 3210h

Range	Access Type	Default (reset)	Description
15:15	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
14:12	RW	0x3 (Core)	**IDR (Interrupt D Pin Route)** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#

Range	Access Type	Default (reset)	Description
11:11	RO	0x0 (Core)	**RSVD_1 (Reserved)** Reserved
10:8	RW	0x2 (Core)	**ICR (Interrupt C Pin Route)** See the IDR description. This field applies to INTC#
7:7	RO	0x0 (Core)	**RSVD_2 (Reserved)** Reserved
6:4	RW	0x1 (Core)	**IBR (Interrupt B Pin Route)** See the IDR description. This field applies to INTB#.
3:3	RO	0x0 (Core)	**RSVD_3 (Reserved)** Reserved
2:0	RW	0x0 (Core)	**IAR (Interrupt A Pin Route)** See the IDR description. This field applies to INTA#.

15.1.136 PCI Interrupt Route 6 (PIR6)—Offset 314Ch

PCI Interrupt Route 6 Register.

Access Method

Type: CR Register (Size: 16 bits)	**Device:** **Function:**

Default: 3210h

Range	Access Type	Default (reset)	Description
15:15	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
14:12	RW	0x3 (Core)	**IDR (Interrupt D Pin Route)** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#
11:11	RO	0x0 (Core)	**RSVD_1 (Reserved)** Reserved
10:8	RW	0x2 (Core)	**ICR (Interrupt C Pin Route)** See the IDR description. This field applies to INTC#
7:7	RO	0x0 (Core)	**RSVD_2 (Reserved)** Reserved

Range	Access Type	Default (reset)	Description
6:4	RW	0x1 (Core)	**IBR (Interrupt B Pin Route)** See the IDR description. This field applies to INTB#.
3:3	RO	0x0 (Core)	**RSVD_3 (Reserved)** Reserved
2:0	RW	0x0 (Core)	**IAR (Interrupt A Pin Route)** See the IDR description. This field applies to INTA#.

15.1.137 PCI Interrupt Route 7 (PIR7)—Offset 314Eh

PCI Interrupt Route 7 Register.

Access Method

Type: CR Register (Size: 16 bits)	**Device:** **Function:**

Default: 3210h

Range	Access Type	Default (reset)	Description
15:15	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
14:12	RW	0x3 (Core)	**IDR (Interrupt D Pin Route)** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#
11:11	RO	0x0 (Core)	**RSVD_1 (Reserved)** Reserved
10:8	RW	0x2 (Core)	**ICR (Interrupt C Pin Route)** See the IDR description. This field applies to INTC#
7:7	RO	0x0 (Core)	**RSVD_2 (Reserved)** Reserved
6:4	RW	0x1 (Core)	**IBR (Interrupt B Pin Route)** See the IDR description. This field applies to INTB#.
3:3	RO	0x0 (Core)	**RSVD_3 (Reserved)** Reserved
2:0	RW	0x0 (Core)	**IAR (Interrupt A Pin Route)** See the IDR description. This field applies to INTA#.

15.1.138 PCI Interrupt Route 8 (PIR8)—Offset 3150h

PCI Interrupt Route 8 Register.

Access Method

Type: CR Register (Size: 16 bits)	**Device:** **Function:**

Default: 3210h

Range	Access Type	Default (reset)	Description
15:15	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
14:12	RW	0x3 (Core)	**IDR (Interrupt D Pin Route)** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#
11:11	RO	0x0 (Core)	**RSVD_1 (Reserved)** Reserved
10:8	RW	0x2 (Core)	**ICR (Interrupt C Pin Route)** See the IDR description. This field applies to INTC#
7:7	RO	0x0 (Core)	**RSVD_2 (Reserved)** Reserved
6:4	RW	0x1 (Core)	**IBR (Interrupt B Pin Route)** See the IDR description. This field applies to INTB#.
3:3	RO	0x0 (Core)	**RSVD_3 (Reserved)** Reserved
2:0	RW	0x0 (Core)	**IAR (Interrupt A Pin Route)** See the IDR description. This field applies to INTA#.

15.1.139 PCI Interrupt Route 9 (PIR9)—Offset 3152h

PCI Interrupt Route 9 Register.

Access Method

Type: CR Register (Size: 16 bits)	**Device:** **Function:**

Default: 3210h

Range	Access Type	Default (reset)	Description
15:15	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
14:12	RW	0x3 (Core)	**IDR (Interrupt D Pin Route)** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#
11:11	RO	0x0 (Core)	**RSVD_1 (Reserved)** Reserved
10:8	RW	0x2 (Core)	**ICR (Interrupt C Pin Route)** See the IDR description. This field applies to INTC#
7:7	RO	0x0 (Core)	**RSVD_2 (Reserved)** Reserved
6:4	RW	0x1 (Core)	**IBR (Interrupt B Pin Route)** See the IDR description. This field applies to INTB#.
3:3	RO	0x0 (Core)	**RSVD_3 (Reserved)** Reserved
2:0	RW	0x0 (Core)	**IAR (Interrupt A Pin Route)** See the IDR description. This field applies to INTA#.

15.1.140 PCI Interrupt Route 10 (PIR10)—Offset 3154h

PCI Interrupt Route 10 Register.

Access Method

Type: CR Register (Size: 16 bits)	**Device:** **Function:**

Default: 3210h

Range	Access Type	Default (reset)	Description
15:15	RO	0x0 (Core)	**RSVD (Reserved)** Reserved

Range	Access Type	Default (reset)	Description
14:12	RW	0x3 (Core)	**IDR (Interrupt D Pin Route)** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#
11:11	RO	0x0 (Core)	**RSVD_1 (Reserved)** Reserved
10:8	RW	0x2 (Core)	**ICR (Interrupt C Pin Route)** See the IDR description. This field applies to INTC#
7:7	RO	0x0 (Core)	**RSVD_2 (Reserved)** Reserved
6:4	RW	0x1 (Core)	**IBR (Interrupt B Pin Route)** See the IDR description. This field applies to INTB#.
3:3	RO	0x0 (Core)	**RSVD_3 (Reserved)** Reserved
2:0	RW	0x0 (Core)	**IAR (Interrupt A Pin Route)** See the IDR description. This field applies to INTA#.

15.1.141 PCI Interrupt Route 11 (PIR11)—Offset 3156h

PCI Interrupt Route 11 Register.

Access Method

Type: CR Register (Size: 16 bits)	**Device:** **Function:**

Default: 3210h

Range	Access Type	Default (reset)	Description
15:15	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
14:12	RW	0x3 (Core)	**IDR (Interrupt D Pin Route)** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#

Range	Access Type	Default (reset)	Description
11:11	RO	0x0 (Core)	**RSVD_1 (Reserved)** Reserved
10:8	RW	0x2 (Core)	**ICR (Interrupt C Pin Route)** See the IDR description. This field applies to INTC#
7:7	RO	0x0 (Core)	**RSVD_2 (Reserved)** Reserved
6:4	RW	0x1 (Core)	**IBR (Interrupt B Pin Route)** See the IDR description. This field applies to INTB#.
3:3	RO	0x0 (Core)	**RSVD_3 (Reserved)** Reserved
2:0	RW	0x0 (Core)	**IAR (Interrupt A Pin Route)** See the IDR description. This field applies to INTA#.

15.1.142 PCI Interrupt Route 12 (PIR12)—Offset 3158h

PCI Interrupt Route 12 Register.

Access Method

Type: CR Register (Size: 16 bits)	**Device:** **Function:**

Default: 3210h

Range	Access Type	Default (reset)	Description
15:15	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
14:12	RW	0x3 (Core)	**IDR (Interrupt D Pin Route)** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#
11:11	RO	0x0 (Core)	**RSVD_1 (Reserved)** Reserved
10:8	RW	0x2 (Core)	**ICR (Interrupt C Pin Route)** See the IDR description. This field applies to INTC#
7:7	RO	0x0 (Core)	**RSVD_2 (Reserved)** Reserved

Range	Access Type	Default (reset)	Description
6:4	RW	0x1 (Core)	**IBR (Interrupt B Pin Route)** See the IDR description. This field applies to INTB#.
3:3	RO	0x0 (Core)	**RSVD_3 (Reserved)** Reserved
2:0	RW	0x0 (Core)	**IAR (Interrupt A Pin Route)** See the IDR description. This field applies to INTA#.

15.1.143 Interrupt Polarity Control 0 (IPC0)—Offset 3200h

Interrupt Polarity Control 0 Register.

Access Method

Type: CR Register (Size: 32 bits)	**Device:** **Function:**

Default: FFh

Range	Access Type	Default (reset)	Description
31:0	RW	0xFF0000 (Core)	**IPC0_IRQxAHPOLDIS (IRQ 31-0 Active High Polarity Disable)** IRQ 31-0 Active High Polarity Disable (IPC0.IRQxAHPOLDIS): When set to 1, the interrupt polarity associated with IRQ31 down to IRQ0 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

15.1.144 Interrupt Polarity Control 1 (IPC1)—Offset 3204h

Interrupt Polarity Control 1 Register.

Access Method

Type: CR Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Range	Access Type	Default (reset)	Description
31:0	RW	0xFF0000 (Core)	**IPC1_IRQAHPOLDIS (IRQ 63-32 Active High Polarity Disable)** IRQ 63-32 Active High Polarity Disable (IPC1.IRQAHPOLDIS): When set to 1, the interrupt polarity associated with IRQ63 down to IRQ32 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

15.1.145 Interrupt Polarity Control 2 (IPC2)—Offset 3208h

Interrupt Polarity Control 2 Register.

Access Method

Type: CR Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Range	Access Type	Default (reset)	Description
31:0	RW	0xFF0000 (Core)	**IPC2_IRQAHPOLDIS (IRQ 95-64 Active High Polarity Disable)** IRQ 95-64 Active High Polarity Disable (IPC2.IRQAHPOLDIS): When set to 1, the interrupt polarity associated with IRQ95 down to IRQ64 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

15.1.146 Interrupt Polarity Control 3 (IPC3)—Offset 320Ch

Interrupt Polarity Control 3 Register.

Access Method

Type: CR Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Range	Access Type	Default (reset)	Description
31:0	RW	0xFF0000 (Core)	**IPC3_IRQAHPOLDIS (IRQ 119-96 Active High Polarity Disable)** IRQ 119-96 Active High Polarity Disable (IPC3.IRQAHPOLDIS): When set to 1, the interrupt polarity associated with IRQ119 down to IRQ96 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

15.1.147 ITSS Power Reduction Control (ITSSPRC)—Offset 3300h

Power controls for the entire interrupt and timer subsystem.

Access Method

Type: CR Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Range	Access Type	Default (reset)	Description
31:5	RO	0x0 (Core)	**RSVD (Reserved)** Reserved
4:4	RW	0x0 (Core)	**PGCBDCGE (PGCB Dynamic Clock Gating Enable)** When set, the ITSS enables dynamic clock gating of the PGCB clock domain. BIOS is requested to program this field to 1.

Range	Access Type	Default (reset)	Description
3:3	RW	0x0 (Core)	**HPETDCGE (HPET Dynamic Clock Gating Enable)** When set, the HPET enables dynamic clock gating. BIOS is requested to program this field to 1.
2:2	RW	0x0 (Core)	**CGE8254 (8254 Static Clock Gating Enable)** When set, the 8254 timer is disabled statically. This bit shall be set by BIOS if the 8254 feature is not needed in the system or before BIOS hands off the system that supports C11. Normal operation of 8254 requires this bit to 0.
1:1	RW	0x0 (Core)	**SBDCGE (Sideband Dynamic Clock Gating Enable)** Setting this bit will enable all dynamic clock gating of the Sideband Clock domain. BIOS is requested to program this field to 1.
0:0	RW	0x0 (Core)	**PCIDCGE (PCI Dynamic Clock Gating Enable)** Setting this bit will enable dynamic clock gating for the ITSS Core Logic that uses PCI Clock. BIOS is requested to program this field to 1.

15.1.148 SIDE Clock Timing (SIDECT)—Offset 3304h

SIDE Clock Timing Register.

Access Method

Type: CR Register (Size: 16 bits)	**Device:** **Function:**

Default: 33h

Range	Access Type	Default (reset)	Description
15:7	RO	0x0 (Core)	**RSVD1 (Reserved)** Reserved
6:4	RW	0x3 (Core)	**CLKREQHO (Clock Request Hold-Off)** Defines the amount of idle time required between locking for power gate preparation and deassertion of the prim_clkreq signal. This field defines the exponent such that the actual delay = 2^ CLKREQHO. WARNING: This value should not be updated unless the Sideband Interface Clock Gating Enable (ITSSPRC.SBDCGE) control register bit is set to 0.
3:3	RO	0x0 (Core)	**RSVD2 (Reserved)** Reserved
2:0	RW	0x3 (Core)	**CLKGATEHO (Clock Gating Hold-Off)** Defines the amount of idle time required before local clock gating will be engaged (if enabled). This field defines the exponent such that the actual delay = 2^ CLGATEHO. WARNING: This value should not be updated unless the Sideband Interface Clock Gating Enable (ITSSPRC.SBDCGE) control register bit is set to 0.

15.2 Registers Summary

Table 15-2. Summary of 0_31_0_APIC MEM REG Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
FEC00000h	FEC00003h	Index Register (IDX)—Offset FEC00000h	0h
FEC00010h	FEC00013h	Window Register (WDW)—Offset FEC00010h	0h
FEC00040h	FEC00043h	EOI Register (EOI)—Offset FEC00040h	0h

15.2.1 Index Register (IDX)—Offset FEC00000h

This 8-bit register selects which indirect register appears in the window register to be manipulated by software. Software will program this register to select the desired APIC internal register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved.
7:0	0h RW	**Index Register (IDX):** Index Register for APIC

15.2.2 Window Register (WDW)—Offset FEC00010h

This 32-bit register specifies the data to be read or written to the register pointed to by the IDX register. This register can be accessed only in DW quantities. The registers are described in Section 13.2.1.2.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Window Register (WDW):** Window Register for APIC

15.2.3 EOI Register (EOI)—Offset FEC00040h

When a write is issued to this register, the IOxAPIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, RTE.RIRR for that entry will be cleared. If multiple entries have the same vector, each of those entries will have RTE.RIRR cleared. Only bits 7:0 are used. Bits 31:8 are ignored.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved.
7:0	0h WO	**EOI Register (EOI):** EOI Register.

15.3 Registers Summary

Table 15-3. Summary of 0_31_0_CPU IO Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
61h	61h	NMI Status and Control (NMI_STS_CNT)—Offset 61h	0h
70h	70h	NMI Enable (and Real Time Clock Index) (NMI_EN)—Offset 70h	80h
92h	92h	Init Register (PORT92)—Offset 92h	0h
CF9h	CF9h	Reset Control Register (RST_CNT)—Offset CF9h	0h

15.3.1 NMI Status and Control (NMI_STS_CNT)—Offset 61h

NMI Status and Control Register

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**SERR# NMI Source Status (SERR_NMI_STS):** This bit is set by any of the sources of the internal SERR on the PCH backbone, this includes SERR assertions forwarded from the secondary PCI bus, error from a PCIe port, Do_SERR or standard PCIe error message from DMI, or internal Bus 0 functions that generate SERR#. Bit 2 must be cleared in this register in order for this bit to be set. This interrupt source is enabled by setting bit 2 to 0. To reset the interrupt, set bit 2 to 1 and then set it to 0. This bit is read-only. When writing to port 61h, this bit must be 0.
6	0h RO	**IOCHK# NMI Source Status (IOCHK_NMI_STS):** This bit is set if an ISA agent (via SERIRQ) asserts IOCHK# and bit 3 is cleared in this register. This interrupt source is enabled by setting bit 3 to 0. To reset the interrupt, set bit 3 to 1 and then set it to 0. This bit is read-only. When writing to port 61h, this bit must be a 0.
5	0h RO	**Timer Counter 2 OUT Status (TMR2_OUT_STS):** This bit reflects the current state of the 8254 counter 2 output. Counter 2 must be programmed following any PCI reset for this bit to have a determinate value. When writing to port 61h, this bit must be a 0.
4	0h RO	**Reserved (RSVD):** Will return 0 when read. Writes to this bit will be ignored.
3	0h RW	**IOCHK# NMI Enable (IOCHK_NMI_EN):** When this bit is a 1, IOCHK# NMIs are disabled and cleared. When this bit is a 0, IOCHK# NMIs are enabled.
2	0h RW	**PCI SERR# Enable (PCI_SERR_EN):** When this bit is a 1, the SERR# NMIs are disabled and cleared. When this bit is a 0, SERR# NMIs are enabled.
1	0h RW	**Speaker Data Enable (SPKR_DAT_EN):** When this bit is a 0, the SPKR output is a 0. When this bit is a 1, the SPKR output is equivalent to the Counter 2 OUT signal value.
0	0h RW	**Timer Counter 2 Enable (TIM_CNT2_EN):** When this bit is a 0, Counter 2 counting is disabled. Counting is enabled when this bit is 1.

15.3.2 NMI Enable (and Real Time Clock Index) (NMI_EN)—Offset 70h

This register is write-only for normal operation. In Alt-Access mode, this register can be read to find the NMI Enable status and the RTC index value. *WO for normal operation, RW if Alternate access mode is enabled. Use RW because there is no equivalent register access attribute in RDL

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**NMI_EN# (NMI_EN):** When this bit is a 1, all NMI sources are disabled. When this bit is a 0, NMI sources are enabled.
6:0	0h RW	**Real Time Clock Index (Address) (RTC_INDX):** This data goes to the RTC to select which register or CMOS RAM address is being accessed.

15.3.3 Init Register (PORT92)—Offset 92h

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved (RSVD):** Reserved
0	0h RW	**INIT NOW (INIT_NOW):** When this bit transitions from a 0 to a 1, the PCH will force INIT# active for 16 PCI clocks.

15.3.4 Reset Control Register (RST_CNT)—Offset CF9h

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved (RSVD):** Reserved
3	0h RW	**Full Reset (FULL_RST):** When this bit is set to 1 and bit 1 is set to 1 (indicating Hard Reset, not Soft Reset), and the RST_CPU bit (bit 2) is written from 0 to 1, the PCH will do a full reset, including driving SLP_S3#, SLP_S4# and SLP_S5# active (low) for at least 3 (and no more than 5) seconds. When this bit is set, it also causes the full power cycle (SLP_S3/4/5# assertion) in response to SYSRESET#, PWROK#, and Watchdog timer reset sources.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Reset CPU (RST_CPU):** This bit will cause either a hard or soft reset to the CPU depending on the state of the SYS_RST bit (bit 1 in this same register). The software will cause the reset by setting bit 2 from a 0 to a 1.
1	0h RW	**System Reset (SYS_RST):** Ths bit determines the type of reset caused via RST_CPU (bit 2 of this register). If SYS_RST is 0 when RST_CPU goes from 0 to 1, then the PCH will force INIT# active for 16 PCI clocks. If SYS_RST is 1 when RST_CPU goes from 0 to 1, then the PCH will force PCI reset active for about 1 ms, however the SLP_S3#, SLP_S4# and SLP_S5# signals assertion is dependent on the value of the FULL_RST (bit3 of this register).
0	0h RO	**Reserved (RSVD_1):** Reserved

15.4 Registers Summary

Table 15-4. Summary of 0_31_0_HPET MEM SPT Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
FED000 00h	FED000 07h	General Capabilities and ID Register (GEN_CAP_ID)—Offset FED00000h	31ABA858086A701h
FED000 10h	FED000 17h	General Config Register (GEN_CFG)—Offset FED00010h	0h
FED000F 0h	FED000F 7h	Main Counter Value (MAIN_CNTR)—Offset FED000F0h	0h
FED001 00h	FED001 07h	Timer 0 Config and Capabilities (TMR0_CNF_CAP)—Offset FED00100h	F0000000008030h
FED001 08h	FED001 0Fh	Timer 0 Comparator Value (TMR0_CMP_VAL)—Offset FED00108h	FFFFFFFFFFFFFFFFh
FED001 10h	FED001 17h	Timer 0 FSB Interrupt Rout Register (TMR0_FSB_INT_ROUT)—Offset FED00110h	0h
FED001 20h	FED001 27h	Timer 1 Config and Capabilities (TMR1_CNF_CAP)—Offset FED00120h	F0000000008000h
FED001 28h	FED001 2Fh	Timer 1 Comparator Value (TMR1_CMP_VAL)—Offset FED00128h	FFFFFFFFh
FED001 30h	FED001 37h	Timer 1 FSB Interrupt Rout Register (TMR1_FSB_INT_ROUT)—Offset FED00130h	0h
FED001 40h	FED001 47h	Timer 2 Config and Capabilities (TMR2_CNF_CAP)—Offset FED00140h	F0080000008000h
FED001 48h	FED001 4Fh	Timer 2 Comparator Value (TMR2_CMP_VAL)—Offset FED00148h	FFFFFFFFh
FED001 50h	FED001 57h	Timer 2 FSB Interrupt Rout Register (TMR2_FSB_INT_ROUT)—Offset FED00150h	0h
FED001 60h	FED001 67h	Timer 3 Config and Capabilities (TMR3_CNF_CAP)—Offset FED00160h	F0100000008000h
FED001 68h	FED001 6Fh	Timer 3 Comparator Value (TMR3_CMP_VAL)—Offset FED00168h	FFFFFFFFh
FED001 70h	FED001 77h	Timer 3 FSB Interrupt Rout Register (TMR3_FSB_INT_ROUT)—Offset FED00170h	0h

FED000F0h	FED000F7h	Main Counter Value (MAIN_CNTR)—Offset FED000F0h	0h
FED00100h	FED00107h	Timer 0 Config and Capabilities (TMR0_CNF_CAP)—Offset FED00100h	F0000000008030h
FED00108h	FED0010Fh	Timer 0 Comparator Value (TMR0_CMP_VAL)—Offset FED00108h	FFFFFFFFFFFFFFFFh
FED00110h	FED00117h	Timer 0 FSB Interrupt Rout Register (TMR0_FSB_INT_ROUT)—Offset FED00110h	0h
FED00120h	FED00127h	Timer 1 Config and Capabilities (TMR1_CNF_CAP)—Offset FED00120h	F0000000008000h
FED00128h	FED0012Fh	Timer 1 Comparator Value (TMR1_CMP_VAL)—Offset FED00128h	FFFFFFFFh
FED00130h	FED00137h	Timer 1 FSB Interrupt Rout Register (TMR1_FSB_INT_ROUT)—Offset FED00130h	0h
FED00140h	FED00147h	Timer 2 Config and Capabilities (TMR2_CNF_CAP)—Offset FED00140h	F0080000008000h
FED00148h	FED0014Fh	Timer 2 Comparator Value (TMR2_CMP_VAL)—Offset FED00148h	FFFFFFFFh
FED00150h	FED00157h	Timer 2 FSB Interrupt Rout Register (TMR2_FSB_INT_ROUT)—Offset FED00150h	0h
FED00160h	FED00167h	Timer 3 Config and Capabilities (TMR3_CNF_CAP)—Offset FED00160h	F0100000008000h
FED00168h	FED0016Fh	Timer 3 Comparator Value (TMR3_CMP_VAL)—Offset FED00168h	FFFFFFFFh
FED00170h	FED00177h	Timer 3 FSB Interrupt Rout Register (TMR3_FSB_INT_ROUT)—Offset FED00170h	0h

15.4.1 General Capabilities and ID Register (GEN_CAP_ID)—Offset FED00000h

Software can read the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 000h or 004h. 64-bit accesses may only be done to 000h. Writes to this register will have no effect.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 31ABA858086A701h

Bit Range	Default & Access	Field Name (ID): Description
63:32	31ABA85h RO	**Main Counter Tick Period (COUNTER_CLK_PER_CAP):** This read-only field indicates the period at which the counter increments in femtoseconds (10^-15 seconds). The PCH HPET timers use a 24 MHz clock, which has a period of 41,666,667 femtoseconds. Therefore this register will always return 031ABA85h when read.
31:16	8086h RO	**Vendor ID (VENDOR_ID_CAP):** These bits will return 8086h when read to reflect Intel as the vendor.
15	1h RO	**Legacy Rout Capable (LEG_RT_CAP):** This bit will always be 1 when read,indicating support for the Legacy Interrupt Rout.
14	0h RO	**Reserved (RSV):** These bits will return 0 when read. Writes will have no effect.
13	1h RO	**Counter Size (COUNT_SIZE_CAP):** This bit will return 1 when read to indicate support for 64-bit counters allowing 64 or 32-bit mode operation.
12:8	7h RO	**Number of Timers (NUM_TIM_CAP):** This value in this field will be 07h to indicate support for 8 timers in the timer block.
7:0	1h RO	**Revision ID (REV_ID):** The value in this field will be 01h to indicate for revision 1.0 of the HPET specification.

15.4.2 General Config Register (GEN_CFG)—Offset FED00010h

Software can read the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 010h or 014h. 64-bit accesses may only be done to 010h.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:2	0h RO	**Reserved (RSV_63_2):** These bits will return 0 when read. Writes will have no effect.
1	0h RW	**Legacy Rout (LEG_RT_CNF):** If the LEG_RT_CNF bit is set, then the interrupts will be routed as follows: Timer 0 will be routed to IRQ0 in 8259 or IRQ2 in the I/O APIC Timer 1 will be routed to IRQ8 in 8259 or IRQ8 in the I/O APIC Timer 2-7 will be routed as per the routing in that timers config register. If the LEG_RT_CNF bit is set, the individual routing bits for timers 0 and 1 (APIC or FSB) will have no impact. Otherwise, if the LEG_RT_CNF bit is not set, the individual routing bits for each of the timers are used. This bit will default to 0. BIOS can set it to 1 to enable the legacy routing, or 0 to disable the legacy routing. When changing other bits in this register, this bit should be left unchanged. Otherwise, a spurious interrupt may occur.
0	0h RW	**Overall Enable (ENABLE_CNF):** This bit must be set to enable any of the timers to generate interrupts. If this bit is 0, then the main counter will halt (will not increment) and no interrupts will be caused by any of these timers. For level-triggered interrupts, if an interrupt is pending when the ENABLE_CNF bit is changed from 1 to 0, the interrupt status indications (in the various Txx_INT_STS bits) will not be cleared. Software must write to the Txx_INT_STS bits to clear the interrupts. Intel Specific: This bit will default to 0. BIOS can set it to 1 or 0.

15.4.3 Main Counter Value (MAIN_CNTR)—Offset FED000F0h

Software can read the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 0F0h or 0F4h. 64-bit accesses may only be done to 0F0h. Writes to this register should only be done while the counter is halted. Reads to this register return the current value of the main counter. If 32-bit software attempts to read a 64-bit counter, it should first halt the counter. Since this will delay the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode. Reads to this register are monotonic. No two consecutive reads will return the same value. The second of two reads will always return a larger value (unless the timer has rolled over to 0)

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW/V	**Counter Value (COUNTER_VAL):** Reads return the current value of the counter. Writes load the new value to the counter.

15.4.4 Timer 0 Config and Capabilities (TMR0_CNF_CAP)—Offset FED00100h

Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x0h or 1x4h. 64-bit accesses may only be done to 1x0h.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: F0000000008030h

Bit Range	Default & Access	Field Name (ID): Description
63:32	F00000h RO	**Timer 0 Interrupt Rout (TIMER0_INT_ROUT_CAP):** This 32-bit read-only field indicates to which interrupts in the 8259 or I/O (x) APIC this timers interrupt can be routed to. This is used in conjunction with the TIMERn_INT_ROUT_CNF field. Writes to this field will have no effect. Note: If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Each bit in this field corresponds to a particular interrupt. For example, if this timers interrupt can be mapped to interrupts 16, 18, 20, 22, or 24, then bits 16, 18, 20, 22, and 24 in this field will be set to 1. All other bits will be 0. Timer 0,1 : Bits 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. Timer 2 : Bits 11, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 11 is used, software should ensure IRQ 11 is not shared with any other devices to guarantee the proper operation of this timer. Timer 3 : Bits 12, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 12 is used, software should ensure IRQ 12 is not shared with any other devices to guarantee the proper operation of this timer. Timer 4-7: This field is always 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
31:16	0h RO	**Reserved (RSV_31_16):** These bits will return 0 when read. Writes will have no effect.
15	1h RO	**FSB Interrupt Delivery Capability (TIMER0_FSB_INT_DEL_CAP):** This bit is always read as 1, since the SoCSoC HPET implementation supports the direct FSB interrupt delivery.
14	0h RW	**Timer 0 FSB Interrupt Delivery Enable (TIMER0_FSB_EN_CNF):** When set, this will force the interrupts for Timer n to be delivered directly as FSB messages, rather than using the 8259 or I/O (x) APIC. In this case, the TIMERn_INT_ROUTE_CNF field in this register will be ignored and the TIMERn_FSB_ROUT register will be used instead. Timer 0, 1, 2, 3: This bit is a read/write bit. Timer 4, 5, 6, 7: This bit is always Read-Only 1 as interrupt from these timers can only be delivered via direct FSB interrupt messages.

Bit Range	Default & Access	Field Name (ID): Description
13:9	0h RW	**Interrupt Route (TIMER0_INT_ROUT_CNF):** This 5-bit field indicates the routing for the interrupt to the 8259 or I/O APIC. A maximum of 32 interrupts are supported. Software writes to this field to select which interrupt in the 8259 or I/O (x)APIC will be used for this timers interrupt. The default value for this register is 00h. If the Legacy Rout bit is set, then Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers. If the TIMERn_FSB_EN_CNF bit is set, then the interrupt will be delivered directly to the FSB, and this bit field has no effect. If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Software must not program any value other than 0-15 in this field. Software must ensure that the value is valid for a particular timer as indicated by the TIMERn_INT_ROUTE_CAP field for that timer. The PCH logic does not check the validity of the value written. For Timers 4-7, this field is always Read-Only 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
8	0h RW	**Timer 0 32-bit Mode (TIMER0_32_MODE_CNF):** Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if the software is not willing to halt the main counter to read or write a particular timer, and the software not capable of do an atomic 64-bit read to the timer. When TIMER0_32MODE_CNF is set to '1', the hardware counter will essentially be doing 32-bit operation on comparator match and rollovers. I.e. the upper 32-bit of the Timer 0 Comparator Value register is ignored. The upper 32-bit of the main counter is not involved in any roll over from lower 32-bit of the main counter and becomes all zero's. For timer 0, this bit will be read/write and default to 0. For timers 1-7, this bit will always read as 0 and writes will have no effect (since these seven timers are 32-bits).
7	0h RO	**Reserved (RSV_7):** This bit will return 0 when read. Writes will have no effect.
6	0h RO	**Timer 0 Value Set (TIMER0_VAL_SET_CNF):** Software uses this bit only for timers that have been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timers accumulator. Software does NOT have to write this bit back to 0 (it automatically clears). This bit will return 0 when read. Software should not write a 1 to this bit position if the timer is set to non-periodic mode. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1-7 as they do not support the periodic mode.
5	1h RO	**Timer 0 Size (TIMER0_SIZE_CAP):** Read-only Indicator of the timers size capability. 1: 64-bits 0: 32-bits. The value is 1 (64-bits) for timer 0, and 0 (32-bits) for timers 1-7.
4	1h RO	**Periodic Interrupt Capable (TIMER0_PER_INT_CAP):** If this read-only bit is 1, then the hardware supports a periodic mode for this timers interrupt. The value is 1 (periodic supported) for timer 0, and 0 (not supported) for timers 1-7.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Timer 0 Type (TIMER0_TYPE_CNF):** Setting this bit to 1 enables the timer to generate a periodic interrupt if it is capable of doing so. If the TIMERn_PER_INT_CAP bit is 0, then this bit will always return 0 when read and writes will have no impact. For timer 0, this bit will be read/write, with default of 0. For timers 1-7, this bit will be read-only, with a fixed value of 0.
2	0h RW	**Timer 0 Interrupt Enable (TIMER0_INT_ENB_CNF):** This bit must be set to 1 to enable timer n to cause an interrupt when it times out. If this bit is 0, the timer can still count and generate appropriate status bits, but will not cause an interrupt. Default value is 0.
1	0h RW	**Timer Interrupt Type (TIMER0_INT_TYPE_CNF):** Determines whether an edge or level interrupt will be used for this timer (when enabled). 0: Edge-triggered. If another interrupt occurs, another edge will be generated. 1: Level-triggered. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active. The default value is 0, edge-triggered. The interrupt type for any timer should be set before that timer generates any interrupts. If the interrupt type is changed dynamically, there will be some delay before the new type takes effect. That delay is not specified. Timer 0-3: This bit is a read/write bit as both edge and level triggered modes are supported. Timer 4-7: This bit is always Read-Only 0 as only edge-triggered mode is supported.
0	0h RO	**Reserved (RSV_0):** These bits will return 0 when read. Writes will have no effect.

15.4.5 Timer 0 Comparator Value (TMR0_CMP_VAL)—Offset FED00108h

Timer 0 Comparator Value Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: FFFFFFFFFFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:0	FFFFFFFFF FFFFFFFh RW/V	**Timer 0 Comparator Value (TMR0_CMP_VAL):** If the timer is configured to non-periodic mode, when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). The value in this register does not change based on the interrupt being generated. If the timer is configured to periodic mode (supported only for Timer 0), when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). When this time out occurs, the value in this register is increased by the value last written to the register. For example, in periodic mode if the value written to the register is 0000123h: 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h. 4. The value in this register will then be adjusted by the hardware to 00000369h As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h The default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer will have a default value of 00000000FFFFFFFFh. A 64-bit timer will have a default value of FFFFFFFFFFFFFFFFh. Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x8h or 1xCh. 64-bit accesses may only be done to 1x8h. Comparator value. Timer 0 is 64-bits wide. Timers 1-7 are 32-bits wide.

15.4.6 Timer 0 FSB Interrupt Rout Register (TMR0_FSB_INT_ROUT)—Offset FED00110h

Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x0h or 1x4h. 64-bit accesses may only be done to 1x0h.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:34	0h RW	**Timer 0 FSB Interrupt Address (TIMER0_FSB_INT_ADDR):** Software sets this 32-bit field to indicate the location that the FSB interrupt message should be written. Intel-Specific: This register is implemented for timer 0:7.
33:32	0h RO	**Reserved (RSV):** Bit(33:32) are read-only and hard-wired to 0.
31:0	0h RW	**Timer 0 FSB Interrupt Value (TIMER0_FSB_INT_VAL):** Software sets this 32-bit field to indicate that value that is written during the FSB interrupt message. Intel-Specific: This register is implemented for timer 0:7.

15.4.7 Timer 1 Config and Capabilities (TMR1_CNF_CAP)—Offset FED00120h

Timer 1 Config and Capabilities Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: F0000000008000h

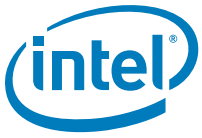
Bit Range	Default & Access	Field Name (ID): Description
63:32	F00000h RO	**Timer 1 Interrupt Rout (TIMER1_INT_ROUT_CAP):** This 32-bit read-only field indicates to which interrupts in the 8259 or I/O (x) APIC this timers interrupt can be routed to. This is used in conjunction with the TIMERn_INT_ROUT_CNF field. Writes to this field will have no effect. Note: If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Each bit in this field corresponds to a particular interrupt. For example, if this timers interrupt can be mapped to interrupts 16, 18, 20, 22, or 24, then bits 16, 18, 20, 22, and 24 in this field will be set to 1. All other bits will be 0. Timer 0,1 : Bits 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. Timer 2 : Bits 11, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 11 is used, software should ensure IRQ 11 is not shared with any other devices to guarantee the proper operation of this timer. Timer 3 : Bits 12, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 12 is used, software should ensure IRQ 12 is not shared with any other devices to guarantee the proper operation of this timer. Timer 4-7: This field is always 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
31:16	0h RO	**Reserved (RSV_31_16):** These bits will return 0 when read. Writes will have no effect.

Bit Range	Default & Access	Field Name (ID): Description
15	1h RO	**FSB Interrupt Delivery Capability (TIMER1_FSB_INT_DEL_CAP):** This bit is always read as 1, since the SoC HPET implementation supports the direct FSB interrupt delivery.
14	0h RW	**Timer 1 FSB Interrupt Delivery Enable (TIMER1_FSB_EN_CNF):** When set, this will force the interrupts for Timer n to be delivered directly as FSB messages, rather than using the 8259 or I/O (x) APIC. In this case, the TIMERn_INT_ROUTE_CNF field in this register will be ignored and the TIMERn_FSB_ROUT register will be used instead. Timer 0, 1, 2, 3: This bit is a read/write bit. Timer 4, 5, 6, 7: This bit is always Read-Only 1 as interrupt from these timers can only be delivered via direct FSB interrupt messages.
13:9	0h RW	**Interrupt Route (TIMER1_INT_ROUT_CNF):** This 5-bit field indicates the routing for the interrupt to the 8259 or I/O APIC. A maximum of 32 interrupts are supported. Software writes to this field to select which interrupt in the 8259 or I/O (x)APIC will be used for this timers interrupt. The default value for this register is 00h. If the Legacy Rout bit is set, then Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers. If the TIMERn_FSB_EN_CNF bit is set, then the interrupt will be delivered directly to the FSB, and this bit field has no effect. If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Software must not program any value other than 0-15 in this field. Software must ensure that the value is valid for a particular timer as indicated by the TIMERn_INT_ROUTE_CAP field for that timer. The PCH logic does not check the validity of the value written. For Timers 4-7, this field is always Read-Only 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
8	0h RO	**Timer 1 32-bit Mode (TIMER1_32_MODE_CNF):** Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if the software is not willing to halt the main counter to read or write a particular timer, and the software not capable of do an atomic 64-bit read to the timer. When TIMER0_32MODE_CNF is set to '1', the hardware counter will essentially be doing 32-bit operation on comparator match and rollovers. I.e. the upper 32-bit of the Timer 0 Comparator Value register is ignored. The upper 32-bit of the main counter is not involved in any roll over from lower 32-bit of the main counter and becomes all zero's. For timer 0, this bit will be read/write and default to 0. For timers 1-7, this bit will always read as 0 and writes will have no effect (since these seven timers are 32-bits).
7	0h RO	**Reserved (RSV_7):** This bit will return 0 when read. Writes will have no effect.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**Timer 1 Value Set (TIMER1_VAL_SET_CNF):** Software uses this bit only for timers that have been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timers accumulator. Software does NOT have to write this bit back to 0 (it automatically clears). This bit will return 0 when read. Software should not write a 1 to this bit position if the timer is set to non-periodic mode. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1-7 as they do not support the periodic mode.
5	0h RO	**Timer 1 Size (TIMER1_SIZE_CAP):** Read-only Indicator of the timers size capability. 1: 64-bits 0: 32-bits. The value is 1 (64-bits) for timer 0, and 0 (32-bits) for timers 1-7.
4	0h RO	**Periodic Interrupt Capable (TIMER1_PER_INT_CAP):** If this read-only bit is 1, then the hardware supports a periodic mode for this timers interrupt. The value is 1 (periodic supported) for timer 0, and 0 (not supported) for timers 1-7.
3	0h RO	**Timer 1 Type (TIMER1_TYPE_CNF):** Setting this bit to 1 enables the timer togenerate a periodic interrupt if it is capable of doing so. If the TIMERn_PER_INT_CAP bit is 0, then this bit will always return 0 when read and writes will have no impact. For timer 0, this bit will be read/write, with default of 0. For timers 1-7, this bit will be read-only, with a fixed value of 0.
2	0h RW	**Timer 1 Interrupt Enable (TIMER1_INT_ENB_CNF):** This bit must be set to 1 to enable timer n to cause an interrupt when it times out. If this bit is 0, the timer can still count and generate appropriate status bits, but will not cause an interrupt. Default value is 0.
1	0h RW	**Timer Interrupt Type (TIMER1_INT_TYPE_CNF):** Determines whether an edge or level interrupt will be used for this timer (when enabled). 0: Edge-triggered. If another interrupt occurs, another edge will be generated. 1: Level-triggered. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active. The default value is 0, edge-triggered. The interrupt type for any timer should be set before that timer generates any interrupts. If the interrupt type is changed dynamically, there will be some delay before the new type takes effect. That delay is not specified. Timer 0-3: This bit is a read/write bit as both edge and level triggered modes are supported. Timer 4-7: This bit is always Read-Only 0 as only edge-triggered mode is supported.
0	0h RO	**Reserved (RSV_0):** These bits will return 0 when read. Writes will have no effect.

15.4.8 Timer 1 Comparator Value (TMR1_CMP_VAL)—Offset FED00128h

Timer 1 Comparator Value Register



Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RO	**Reserved (RSV):** Reserved.
31:0	FFFFFFFFh RW	**Timer 1 Comparator Value (TMR1_CMP_VAL):** If the timer is configured to non-periodic mode, when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). The value in this register does not change based on the interrupt being generated. If the timer is configured to periodic mode (supported only for Timer 0), when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). When this time out occurs, the value in this register is increased by the value last written to the register. For example, in periodic mode if the value written to the register is 0000123h: 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h. 4. The value in this register will then be adjusted by the hardware to 00000369h As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h The default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer will have a default value of 00000000FFFFFFFFh. A 64-bit timer will have a default value of FFFFFFFFFFFFFFFFh. Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x8h or 1xCh. 64-bit accesses may only be done to 1x8h. Comparator value. Timer 0 is 64-bits wide. Timers 1-7 are 32-bits wide.

15.4.9 Timer 1 FSB Interrupt Rout Register (TMR1_FSB_INT_ROUT)—Offset FED00130h

Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x0h or 1x4h. 64-bit accesses may only be done to 1x0h.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:34	0h RW	**Timer 1 FSB Interrupt Address (TIMER1_FSB_INT_ADDR):** Software sets this 32-bit field to indicate the location that the FSB interrupt message should be written. Intel-Specific: This register is implemented for timer 0:7.
33:32	0h RO	**Reserved (RSV):** Bit(33:32) are read-only and hard-wired to 0.
31:0	0h RW	**Timer 1 FSB Interrupt Value (TIMER1_FSB_INT_VAL):** Software sets this 32-bit field to indicate that value that is written during the FSB interrupt message. Intel-Specific: This register is implemented for timer 0:7.

15.4.10 Timer 2 Config and Capabilities (TMR2_CNF_CAP)—Offset FED00140h

Timer 2 Config and Capabilities Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: F0080000008000h

Bit Range	Default & Access	Field Name (ID): Description
63:32	F00800h RO	**Timer 2 Interrupt Rout (TIMER2_INT_ROUT_CAP):** This 32-bit read-only field indicates to which interrupts in the 8259 or I/O (x) APIC this timers interrupt can be routed to. This is used in conjunction with the TIMERn_INT_ROUT_CNF field. Writes to this field will have no effect. Note: If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Each bit in this field corresponds to a particular interrupt. For example, if this timers interrupt can be mapped to interrupts 16, 18, 20, 22, or 24, then bits 16, 18, 20, 22, and 24 in this field will be set to 1. All other bits will be 0. Timer 0,1 : Bits 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. Timer 2 : Bits 11, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 11 is used, software should ensure IRQ 11 is not shared with any other devices to guarantee the proper operation of this timer. Timer 3 : Bits 12, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 12 is used, software should ensure IRQ 12 is not shared with any other devices to guarantee the proper operation of this timer. Timer 4-7: This field is always 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
31:16	0h RO	**Reserved (RSV_31_16):** These bits will return 0 when read. Writes will have no effect.
15	1h RO	**FSB Interrupt Delivery Capability (TIMER2_FSB_INT_DEL_CAP):** This bit is always read as 1, since the SoC HPET implementation supports the direct FSB interrupt delivery.
14	0h RW	**Timer 2 FSB Interrupt Delivery Enable (TIMER2_FSB_EN_CNF):** When set, this will force the interrupts for Timer n to be delivered directly as FSB messages, rather than using the 8259 or I/O (x) APIC. In this case, the TIMERn_INT_ROUTE_CNF field in this register will be ignored and the TIMERn_FSB_ROUT register will be used instead. Timer 0, 1, 2, 3: This bit is a read/write bit. Timer 4, 5, 6, 7: This bit is always Read-Only 1 as interrupt from these timers can only be delivered via direct FSB interrupt messages.

Bit Range	Default & Access	Field Name (ID): Description
13:9	0h RW	**Interrupt Route (TIMER2_INT_ROUT_CNF):** This 5-bit field indicates the routing for the interrupt to the 8259 or I/O APIC. A maximum of 32 interrupts are supported. Software writes to this field to select which interrupt in the 8259 or I/O (x)APIC will be used for this timers interrupt. The default value for this register is 00h. If the Legacy Rout bit is set, then Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers. If the TIMERn_FSB_EN_CNF bit is set, then the interrupt will be delivered directly to the FSB, and this bit field has no effect. If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Software must not program any value other than 0-15 in this field. Software must ensure that the value is valid for a particular timer as indicated by the TIMERn_INT_ROUTE_CAP field for that timer. The PCH logic does not check the validity of the value written. For Timers 4-7, this field is always Read-Only 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
8	0h RO	**Timer 2 32-bit Mode (TIMER2_32_MODE_CNF):** Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if the software is not willing to halt the main counter to read or write a particular timer, and the software not capable of do an atomic 64-bit read to the timer. When TIMER0_32MODE_CNF is set to '1', the hardware counter will essentially be doing 32-bit operation on comparator match and rollovers. I.e. the upper 32-bit of the Timer 0 Comparator Value register is ignored. The upper 32-bit of the main counter is not involved in any roll over from lower 32-bit of the main counter and becomes all zero's. For timer 0, this bit will be read/write and default to 0. For timers 1-7, this bit will always read as 0 and writes will have no effect (since these seven timers are 32-bits).
7	0h RO	**Reserved (RSV_7):** This bit will return 0 when read. Writes will have no effect.
6	0h RO	**Timer 2 Value Set (TIMER2_VAL_SET_CNF):** Software uses this bit only for timers that have been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timers accumulator. Software does NOT have to write this bit back to 0 (it automatically clears). This bit will return 0 when read. Software should not write a 1 to this bit position if the timer is set to non-periodic mode. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1-7 as they do not support the periodic mode.
5	0h RO	**Timer 2 Size (TIMER2_SIZE_CAP):** Read-only Indicator of the timers size capability. 1: 64-bits 0: 32-bits. The value is 1 (64-bits) for timer 0, and 0 (32-bits) for timers 1-7.
4	0h RO	**Periodic Interrupt Capable (TIMER2_PER_INT_CAP):** If this read-only bit is 1, then the hardware supports a periodic mode for this timers interrupt. The value is 1 (periodic supported) for timer 0, and 0 (not supported) for timers 1-7.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Timer 2 Type (TIMER2_TYPE_CNF):** Setting this bit to 1 enables the timer to generate a periodic interrupt if it is capable of doing so. If the TIMERn_PER_INT_CAP bit is 0, then this bit will always return 0 when read and writes will have no impact. For timer 0, this bit will be read/write, with default of 0. For timers 1-7, this bit will be read-only, with a fixed value of 0.
2	0h RW	**Timer 2 Interrupt Enable (TIMER2_INT_ENB_CNF):** This bit must be set to 1 to enable timer n to cause an interrupt when it times out. If this bit is 0, the timer can still count and generate appropriate status bits, but will not cause an interrupt. Default value is 0.
1	0h RW	**Timer Interrupt Type (TIMER2_INT_TYPE_CNF):** Determines whether an edge or level interrupt will be used for this timer (when enabled). 0: Edge-triggered. If another interrupt occurs, another edge will be generated. 1: Level-triggered. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active. The default value is 0, edge-triggered. The interrupt type for any timer should be set before that timer generates any interrupts. If the interrupt type is changed dynamically, there will be some delay before the new type takes effect. That delay is not specified. Timer 0-3: This bit is a read/write bit as both edge and level triggered modes are supported. Timer 4-7: This bit is always Read-Only 0 as only edge-triggered mode is supported.
0	0h RO	**Reserved (RSV_0):** These bits will return 0 when read. Writes will have no effect.

15.4.11 Timer 2 Comparator Value (TMR2_CMP_VAL)—Offset FED00148h

Timer 2 Comparator Value Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RO	**Reserved (RSV):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**Timer 2 Comparator Value (TMR2_CMP_VAL):** If the timer is configured to non-periodic mode, when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). The value in this register does not change based on the interrupt being generated. If the timer is configured to periodic mode (supported only for Timer 0), when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). When this time out occurs, the value in this register is increased by the value last written to the register. For example, in periodic mode if the value written to the register is 0000123h: 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h. 4. The value in this register will then be adjusted by the hardware to 00000369h As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h The default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer will have a default value of 00000000FFFFFFFFh. A 64-bit timer will have a default value of FFFFFFFFFFFFFFFFh. Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x8h or 1xCh. 64-bit accesses may only be done to 1x8h. Comparator value. Timer 0 is 64-bits wide. Timers 1-7 are 32-bits wide.

15.4.12 Timer 2 FSB Interrupt Rout Register (TMR2_FSB_INT_ROUT)—Offset FED00150h

Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x0h or 1x4h. 64-bit accesses may only be done to 1x0h.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:34	0h RW	**Timer 2 FSB Interrupt Address (TIMER2_FSB_INT_ADDR):** Software sets this 32-bit field to indicate the location that the FSB interrupt message should be written. Intel-Specific: This register is implemented for timer 0:7.
33:32	0h RO	**Reserved (RSV):** Bit(33:32) are read-only and hard-wired to 0.
31:0	0h RW	**Timer 2 FSB Interrupt Value (TIMER2_FSB_INT_VAL):** Software sets this 32-bit field to indicate that value that is written during the FSB interrupt message. Intel-Specific: This register is implemented for timer 0:7.

15.4.13 Timer 3 Config and Capabilities (TMR3_CNF_CAP)—Offset FED00160h

Timer 3 Config and Capabilities Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: F0100000008000h

Bit Range	Default & Access	Field Name (ID): Description
63:32	F01000h RO	**Timer 3 Interrupt Rout (TIMER3_INT_ROUT_CAP):** This 32-bit read-only field indicates to which interrupts in the 8259 or I/O (x) APIC this timers interrupt can be routed to. This is used in conjunction with the TIMERn_INT_ROUT_CNF field. Writes to this field will have no effect. Note: If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Each bit in this field corresponds to a particular interrupt. For example, if this timers interrupt can be mapped to interrupts 16, 18, 20, 22, or 24, then bits 16, 18, 20, 22, and 24 in this field will be set to 1. All other bits will be 0. Timer 0,1 : Bits 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. Timer 2 : Bits 11, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 11 is used, software should ensure IRQ 11 is not shared with any other devices to guarantee the proper operation of this timer. Timer 3 : Bits 12, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 12 is used, software should ensure IRQ 12 is not shared with any other devices to guarantee the proper operation of this timer. Timer 4-7: This field is always 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
31:16	0h RO	**Reserved (RSV_31_16):** These bits will return 0 when read. Writes will have no effect.

Bit Range	Default & Access	Field Name (ID): Description
15	1h RO	**FSB Interrupt Delivery Capability (TIMER3_FSB_INT_DEL_CAP):** This bit is always read as 1, since the SoC HPET implementation supports the direct FSB interrupt delivery.
14	0h RW	**Timer 3 FSB Interrupt Delivery Enable (TIMER3_FSB_EN_CNF):** When set, this will force the interrupts for Timer n to be delivered directly as FSB messages, rather than using the 8259 or I/O (x) APIC. In this case, the TIMERn_INT_ROUTE_CNF field in this register will be ignored and the TIMERn_FSB_ROUT register will be used instead. Timer 0, 1, 2, 3: This bit is a read/write bit. Timer 4, 5, 6, 7: This bit is always Read-Only 1 as interrupt from these timers can only be delivered via direct FSB interrupt messages.
13:9	0h RW	**Interrupt Route (TIMER3_INT_ROUT_CNF):** This 5-bit field indicates the routing for the interrupt to the 8259 or I/O APIC. A maximum of 32 interrupts are supported. Software writes to this field to select which interrupt in the 8259 or I/O (x)APIC will be used for this timers interrupt. The default value for this register is 00h. If the Legacy Rout bit is set, then Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers. If the TIMERn_FSB_EN_CNF bit is set, then the interrupt will be delivered directly to the FSB, and this bit field has no effect. If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Software must not program any value other than 0-15 in this field. Software must ensure that the value is valid for a particular timer as indicated by the TIMERn_INT_ROUTE_CAP field for that timer. The PCH logic does not check the validity of the value written. For Timers 4-7, this field is always Read-Only 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
8	0h RO	**Timer 3 32-bit Mode (TIMER3_32_MODE_CNF):** Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if the software is not willing to halt the main counter to read or write a particular timer, and the software not capable of do an atomic 64-bit read to the timer. When TIMER0_32MODE_CNF is set to '1', the hardware counter will essentially be doing 32-bit operation on comparator match and rollovers. I.e. the upper 32-bit of the Timer 0 Comparator Value register is ignored. The upper 32-bit of the main counter is not involved in any roll over from lower 32-bit of the main counter and becomes all zero's. For timer 0, this bit will be read/write and default to 0. For timers 1-7, this bit will always read as 0 and writes will have no effect (since these seven timers are 32-bits).
7	0h RO	**Reserved (RSV_7):** This bit will return 0 when read. Writes will have no effect.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**Timer 3 Value Set (TIMER3_VAL_SET_CNF):** Software uses this bit only for timers that have been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timers accumulator. Software does NOT have to write this bit back to 0 (it automatically clears). This bit will return 0 when read. Software should not write a 1 to this bit position if the timer is set to non-periodic mode. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1-7 as they do not support the periodic mode.
5	0h RO	**Timer 3 Size (TIMER3_SIZE_CAP):** Read-only Indicator of the timers size capability. 1: 64-bits 0: 32-bits. The value is 1 (64-bits) for timer 0, and 0 (32-bits) for timers 1-7.
4	0h RO	**Periodic Interrupt Capable (TIMER3_PER_INT_CAP):** If this read-only bit is 1, then the hardware supports a periodic mode for this timers interrupt. The value is 1 (periodic supported) for timer 0, and 0 (not supported) for timers 1-7.
3	0h RO	**Timer 3 Type (TIMER3_TYPE_CNF):** Setting this bit to 1 enables the timer to generate a periodic interrupt if it is capable of doing so. If the TIMERn_PER_INT_CAP bit is 0, then this bit will always return 0 when read and writes will have no impact. For timer 0, this bit will be read/write, with default of 0. For timers 1-7, this bit will be read-only, with a fixed value of 0.
2	0h RW	**Timer 3 Interrupt Enable (TIMER3_INT_ENB_CNF):** This bit must be set to 1 to enable timer n to cause an interrupt when it times out. If this bit is 0, the timer can still count and generate appropriate status bits, but will not cause an interrupt. Default value is 0.
1	0h RW	**Timer Interrupt Type (TIMER3_INT_TYPE_CNF):** Determines whether an edge or level interrupt will be used for this timer (when enabled). 0: Edge-triggered. If another interrupt occurs, another edge will be generated. 1: Level-triggered. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active. The default value is 0, edge-triggered. The interrupt type for any timer should be set before that timer generates any interrupts. If the interrupt type is changed dynamically, there will be some delay before the new type takes effect. That delay is not specified. Timer 0-3: This bit is a read/write bit as both edge and level triggered modes are supported. Timer 4-7: This bit is always Read-Only 0 as only edge-triggered mode is supported.
0	0h RO	**Reserved (RSV_0):** These bits will return 0 when read. Writes will have no effect.

15.4.14 Timer 3 Comparator Value (TMR3_CMP_VAL)—Offset FED00168h

Timer 3 Comparator Value Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RO	**Reserved (RSV):** Reserved.
31:0	FFFFFFFFh RW	**Timer 3 Comparator Value (TMR3_CMP_VAL):** If the timer is configured to non-periodic mode, when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). The value in this register does not change based on the interrupt being generated. If the timer is configured to periodic mode (supported only for Timer 0), when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). When this time out occurs, the value in this register is increased by the value last written to the register. For example, in periodic mode if the value written to the register is 0000123h: 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h. 4. The value in this register will then be adjusted by the hardware to 00000369h As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h The default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer will have a default value of 00000000FFFFFFFFh. A 64-bit timer will have a default value of FFFFFFFFFFFFFFFFh. Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x8h or 1xCh. 64-bit accesses may only be done to 1x8h. Comparator value. Timer 0 is 64-bits wide. Timers 1-7 are 32-bits wide.

15.4.15 Timer 3 FSB Interrupt Rout Register (TMR3_FSB_INT_ROUT)—Offset FED00170h

Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x0h or 1x4h. 64-bit accesses may only be done to 1x0h.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:34	0h RW	**Timer 3 FSB Interrupt Address (TIMER3_FSB_INT_ADDR):** Software sets this 32-bit field to indicate the location that the FSB interrupt message should be written. Intel-Specific: This register is implemented for timer 0:7.
33:32	0h RO	**Reserved (RSV):** Bit(33:32) are read-only and hard-wired to 0.
31:0	0h RW	**Timer 3 FSB Interrupt Value (TIMER3_FSB_INT_VAL):** Software sets this 32-bit field to indicate that value that is written during the FSB interrupt message. Intel-Specific: This register is implemented for timer 0:7.

15.4.16 Timer 4 Config and Capabilities (TMR4_CNF_CAP)—Offset FED00180h

Timer 4 Config and Capabilities Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C000h

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RO	**Timer 4 Interrupt Rout (TIMER4_INT_ROUT_CAP):** This 32-bit read-only field indicates to which interrupts in the 8259 or I/O (x) APIC this timers interrupt can be routed to. This is used in conjunction with the TIMERn_INT_ROUT_CNF field. Writes to this field will have no effect. Note: If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Each bit in this field corresponds to a particular interrupt. For example, if this timers interrupt can be mapped to interrupts 16, 18, 20, 22, or 24, then bits 16, 18, 20, 22, and 24 in this field will be set to 1. All other bits will be 0. Timer 0,1 : Bits 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. Timer 2 : Bits 11, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 11 is used, software should ensure IRQ 11 is not shared with any other devices to guarantee the proper operation of this timer. Timer 3 : Bits 12, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 12 is used, software should ensure IRQ 12 is not shared with any other devices to guarantee the proper operation of this timer. Timer 4-7: This field is always 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
31:16	0h RO	**Reserved (RSV_31_16):** These bits will return 0 when read. Writes will have no effect.
15	1h RO	**FSB Interrupt Delivery Capability (TIMER4_FSB_INT_DEL_CAP):** This bit is always read as 1, since the SoC HPET implementation supports the direct FSB interrupt delivery.
14	1h RO	**Timer 4 FSB Interrupt Delivery Enable (TIMER4_FSB_EN_CNF):** When set, this will force the interrupts for Timer n to be delivered directly as FSB messages, rather than using the 8259 or I/O (x) APIC. In this case, the TIMERn_INT_ROUTE_CNF field in this register will be ignored and the TIMERn_FSB_ROUT register will be used instead. Timer 0, 1, 2, 3: This bit is a read/write bit. Timer 4, 5, 6, 7: This bit is always Read-Only 1 as interrupt from these timers can only be delivered via direct FSB interrupt messages.

Bit Range	Default & Access	Field Name (ID): Description
13:9	0h RO	**Interrupt Route (TIMER4_INT_ROUT_CNF):** This 5-bit field indicates the routing for the interrupt to the 8259 or I/O APIC. A maximum of 32 interrupts are supported. Software writes to this field to select which interrupt in the 8259 or I/O (x)APIC will be used for this timers interrupt. The default value for this register is 00h. If the Legacy Rout bit is set, then Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers. If the TIMERn_FSB_EN_CNF bit is set, then the interrupt will be delivered directly to the FSB, and this bit field has no effect. If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Software must not program any value other than 0-15 in this field. Software must ensure that the value is valid for a particular timer as indicated by the TIMERn_INT_ROUTE_CAP field for that timer. The PCH logic does not check the validity of the value written. For Timers 4-7, this field is always Read-Only 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
8	0h RO	**Timer 4 32-bit Mode (TIMER4_32_MODE_CNF):** Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if the software is not willing to halt the main counter to read or write a particular timer, and the software not capable of do an atomic 64-bit read to the timer. When TIMER0_32MODE_CNF is set to '1', the hardware counter will essentially be doing 32-bit operation on comparator match and rollovers. I.e. the upper 32-bit of the Timer 0 Comparator Value register is ignored. The upper 32-bit of the main counter is not involved in any roll over from lower 32-bit of the main counter and becomes all zero's. For timer 0, this bit will be read/write and default to 0. For timers 1-7, this bit will always read as 0 and writes will have no effect (since these seven timers are 32-bits).
7	0h RO	**Reserved (RSV_7):** This bit will return 0 when read. Writes will have no effect.
6	0h RO	**Timer 4 Value Set (TIMER4_VAL_SET_CNF):** Software uses this bit only for timers that have been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timers accumulator. Software does NOT have to write this bit back to 0 (it automatically clears). This bit will return 0 when read. Software should not write a 1 to this bit position if the timer is set to non-periodic mode. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1-7 as they do not support the periodic mode.
5	0h RO	**Timer 4 Size (TIMER4_SIZE_CAP):** Read-only Indicator of the timers size capability. 1: 64-bits 0: 32-bits. The value is 1 (64-bits) for timer 0, and 0 (32-bits) for timers 1-7.
4	0h RO	**Periodic Interrupt Capable (TIMER4_PER_INT_CAP):** If this read-only bit is 1, then the hardware supports a periodic mode for this timers interrupt. The value is 1 (periodic supported) for timer 0, and 0 (not supported) for timers 1-7.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Timer 4 Type (TIMER4_TYPE_CNF):** Setting this bit to 1 enables the timer to generate a periodic interrupt if it is capable of doing so. If the TIMERn_PER_INT_CAP bit is 0, then this bit will always return 0 when read and writes will have no impact. For timer 0, this bit will be read/write, with default of 0. For timers 1-7, this bit will be read-only, with a fixed value of 0.
2	0h RW	**Timer 4 Interrupt Enable (TIMER4_INT_ENB_CNF):** This bit must be set to 1 to enable timer n to cause an interrupt when it times out. If this bit is 0, the timer can still count and generate appropriate status bits, but will not cause an interrupt. Default value is 0.
1	0h RO	**Timer Interrupt Type (TIMER4_INT_TYPE_CNF):** Determines whether an edge or level interrupt will be used for this timer (when enabled). 0: Edge-triggered. If another interrupt occurs, another edge will be generated. 1: Level-triggered. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active. The default value is 0, edge-triggered. The interrupt type for any timer should be set before that timer generates any interrupts. If the interrupt type is changed dynamically, there will be some delay before the new type takes effect. That delay is not specified. Timer 0-3: This bit is a read/write bit as both edge and level triggered modes are supported. Timer 4-7: This bit is always Read-Only 0 as only edge-triggered mode is supported.
0	0h RO	**Reserved (RSV_0):** These bits will return 0 when read. Writes will have no effect.

15.4.17 Timer 4 Comparator Value (TMR4_CMP_VAL)—Offset FED00188h

Timer 4 Comparator Value Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RO	**Reserved (RSV):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**Timer 4 Comparator Value (TMR4_CMP_VAL):** If the timer is configured to non-periodic mode, when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). The value in this register does not change based on the interrupt being generated. If the timer is configured to periodic mode (supported only for Timer 0), when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). When this time out occurs, the value in this register is increased by the value last written to the register. For example, in periodic mode if the value written to the register is 0000123h: 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h. 4. The value in this register will then be adjusted by the hardware to 00000369h As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h The default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer will have a default value of 00000000FFFFFFFFh. A 64-bit timer will have a default value of FFFFFFFFFFFFFFFFh. Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x8h or 1xCh. 64-bit accesses may only be done to 1x8h. Comparator value. Timer 0 is 64-bits wide. Timers 1-7 are 32-bits wide.

15.4.18 Timer 4 FSB Interrupt Rout Register (TMR4_FSB_INT_ROUT)—Offset FED00190h

Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x0h or 1x4h. 64-bit accesses may only be done to 1x0h.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:34	0h RW	**Timer 4 FSB Interrupt Address (TIMER4_FSB_INT_ADDR):** Software sets this 32-bit field to indicate the location that the FSB interrupt message should be written. Intel-Specific: This register is implemented for timer 0:7.
33:32	0h RO	**Reserved (RSV):** Bit(33:32) are read-only and hard-wired to 0.
31:0	0h RW	**Timer 4 FSB Interrupt Value (TIMER4_FSB_INT_VAL):** Software sets this 32-bit field to indicate that value that is written during the FSB interrupt message. Intel-Specific: This register is implemented for timer 0:7.

15.4.19 Timer 5 Config and Capabilities (TMR5_CNF_CAP)—Offset FED001A0h

Timer 5 Config and Capabilities Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C000h

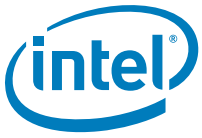
Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RO	**Timer 5 Interrupt Rout (TIMER5_INT_ROUT_CAP):** This 32-bit read-only field indicates to which interrupts in the 8259 or I/O (x) APIC this timers interrupt can be routed to. This is used in conjunction with the TIMERn_INT_ROUT_CNF field. Writes to this field will have no effect. Note: If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Each bit in this field corresponds to a particular interrupt. For example, if this timers interrupt can be mapped to interrupts 16, 18, 20, 22, or 24, then bits 16, 18, 20, 22, and 24 in this field will be set to 1. All other bits will be 0. Timer 0,1 : Bits 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. Timer 2 : Bits 11, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 11 is used, software should ensure IRQ 11 is not shared with any other devices to guarantee the proper operation of this timer. Timer 3 : Bits 12, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 12 is used, software should ensure IRQ 12 is not shared with any other devices to guarantee the proper operation of this timer. Timer 4-7: This field is always 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
31:16	0h RO	**Reserved (RSV_31_16):** These bits will return 0 when read. Writes will have no effect.

Bit Range	Default & Access	Field Name (ID): Description
15	1h RO	**FSB Interrupt Delivery Capability (TIMER5_FSB_INT_DEL_CAP):** This bit is always read as 1, since the SoC HPET implementation supports the direct FSB interrupt delivery.
14	1h RO	**Timer 5 FSB Interrupt Delivery Enable (TIMER5_FSB_EN_CNF):** When set, this will force the interrupts for Timer n to be delivered directly as FSB messages, rather than using the 8259 or I/O (x) APIC. In this case, the TIMERn_INT_ROUTE_CNF field in this register will be ignored and the TIMERn_FSB_ROUT register will be used instead. Timer 0, 1, 2, 3: This bit is a read/write bit. Timer 4, 5, 6, 7: This bit is always Read-Only 1 as interrupt from these timers can only be delivered via direct FSB interrupt messages.
13:9	0h RO	**Interrupt Route (TIMER5_INT_ROUT_CNF):** This 5-bit field indicates the routing for the interrupt to the 8259 or I/O APIC. A maximum of 32 interrupts are supported. Software writes to this field to select which interrupt in the 8259 or I/O (x)APIC will be used for this timers interrupt. The default value for this register is 00h. If the Legacy Rout bit is set, then Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers. If the TIMERn_FSB_EN_CNF bit is set, then the interrupt will be delivered directly to the FSB, and this bit field has no effect. If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Software must not program any value other than 0-15 in this field. Software must ensure that the value is valid for a particular timer as indicated by the TIMERn_INT_ROUTE_CAP field for that timer. The PCH logic does not check the validity of the value written. For Timers 4-7, this field is always Read-Only 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
8	0h RO	**Timer 5 32-bit Mode (TIMER5_32_MODE_CNF):** Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if the software is not willing to halt the main counter to read or write a particular timer, and the software not capable of do an atomic 64-bit read to the timer. When TIMER0_32MODE_CNF is set to '1', the hardware counter will essentially be doing 32-bit operation on comparator match and rollovers. I.e. the upper 32-bit of the Timer 0 Comparator Value register is ignored. The upper 32-bit of the main counter is not involved in any roll over from lower 32-bit of the main counter and becomes all zero's. For timer 0, this bit will be read/write and default to 0. For timers 1-7, this bit will always read as 0 and writes will have no effect (since these seven timers are 32-bits).
7	0h RO	**Reserved (RSV_7):** This bit will return 0 when read. Writes will have no effect.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**Timer 5 Value Set (TIMER5_VAL_SET_CNF):** Software uses this bit only for timers that have been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timers accumulator. Software does NOT have to write this bit back to 0 (it automatically clears). This bit will return 0 when read. Software should not write a 1 to this bit position if the timer is set to non-periodic mode. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1-7 as they do not support the periodic mode.
5	0h RO	**Timer 5 Size (TIMER5_SIZE_CAP):** Read-only Indicator of the timers size capability. 1: 64-bits 0: 32-bits. The value is 1 (64-bits) for timer 0, and 0 (32-bits) for timers 1-7.
4	0h RO	**Periodic Interrupt Capable (TIMER5_PER_INT_CAP):** If this read-only bit is 1, then the hardware supports a periodic mode for this timers interrupt. The value is 1 (periodic supported) for timer 0, and 0 (not supported) for timers 1-7.
3	0h RO	**Timer 5 Type (TIMER5_TYPE_CNF):** Setting this bit to 1 enables the timer to generate a periodic interrupt if it is capable of doing so. If the TIMERn_PER_INT_CAP bit is 0, then this bit will always return 0 when read and writes will have no impact. For timer 0, this bit will be read/write, with default of 0. For timers 1-7, this bit will be read-only, with a fixed value of 0.
2	0h RW	**Timer 5 Interrupt Enable (TIMER5_INT_ENB_CNF):** This bit must be set to 1 to enable timer n to cause an interrupt when it times out. If this bit is 0, the timer can still count and generate appropriate status bits, but will not cause an interrupt. Default value is 0.
1	0h RO	**Timer Interrupt Type (TIMER5_INT_TYPE_CNF):** Determines whether an edge or level interrupt will be used for this timer (when enabled). 0: Edge-triggered. If another interrupt occurs, another edge will be generated. 1: Level-triggered. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active. The default value is 0, edge-triggered. The interrupt type for any timer should be set before that timer generates any interrupts. If the interrupt type is changed dynamically, there will be some delay before the new type takes effect. That delay is not specified. Timer 0-3: This bit is a read/write bit as both edge and level triggered modes are supported. Timer 4-7: This bit is always Read-Only 0 as only edge-triggered mode is supported.
0	0h RO	**Reserved (RSV_0):** These bits will return 0 when read. Writes will have no effect.

15.4.20 Timer 5 Comparator Value (TMR5_CMP_VAL)—Offset FED001A8h

Timer 5 Comparator Value Register



Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RO	**Reserved (RSV):** Reserved.
31:0	FFFFFFFFh RW	**Timer 5 Comparator Value (TMR5_CMP_VAL):** If the timer is configured to non-periodic mode, when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). The value in this register does not change based on the interrupt being generated. If the timer is configured to periodic mode (supported only for Timer 0), when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). When this time out occurs, the value in this register is increased by the value last written to the register. For example, in periodic mode if the value written to the register is 0000123h: 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h. 4. The value in this register will then be adjusted by the hardware to 00000369h As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h The default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer will have a default value of 00000000FFFFFFFFh. A 64-bit timer will have a default value of FFFFFFFFFFFFFFFFh. Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x8h or 1xCh. 64-bit accesses may only be done to 1x8h. Comparator value. Timer 0 is 64-bits wide. Timers 1-7 are 32-bits wide.

15.4.21 Timer 5 FSB Interrupt Rout Register (TMR5_FSB_INT_ROUT)—Offset FED001B0h

Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x0h or 1x4h. 64-bit accesses may only be done to 1x0h.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:34	0h RW	**Timer 5 FSB Interrupt Address (TIMER5_FSB_INT_ADDR):** Software sets this 32-bit field to indicate the location that the FSB interrupt message should be written. Intel-Specific: This register is implemented for timer 0:7.
33:32	0h RO	**Reserved (RSV):** Bit(33:32) are read-only and hard-wired to 0.
31:0	0h RW	**Timer 5 FSB Interrupt Value (TIMER5_FSB_INT_VAL):** Software sets this 32-bit field to indicate that value that is written during the FSB interrupt message. Intel-Specific: This register is implemented for timer 0:7.

15.4.22 Timer 6 Config and Capabilities (TMR6_CNF_CAP)—Offset FED001C0h

Timer 6 Config and Capabilities Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C000h

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RO	**Timer 6 Interrupt Rout (TIMER6_INT_ROUT_CAP):** This 32-bit read-only field indicates to which interrupts in the 8259 or I/O (x) APIC this timers interrupt can be routed to. This is used in conjunction with the TIMERn_INT_ROUT_CNF field. Writes to this field will have no effect. Note: If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Each bit in this field corresponds to a particular interrupt. For example, if this timers interrupt can be mapped to interrupts 16, 18, 20, 22, or 24, then bits 16, 18, 20, 22, and 24 in this field will be set to 1. All other bits will be 0. Timer 0,1 : Bits 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. Timer 2 : Bits 11, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 11 is used, software should ensure IRQ 11 is not shared with any other devices to guarantee the proper operation of this timer. Timer 3 : Bits 12, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 12 is used, software should ensure IRQ 12 is not shared with any other devices to guarantee the proper operation of this timer. Timer 4-7: This field is always 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
31:16	0h RO	**Reserved (RSV_31_16):** These bits will return 0 when read. Writes will have no effect.
15	1h RO	**FSB Interrupt Delivery Capability (TIMER6_FSB_INT_DEL_CAP):** This bit is always read as 1, since the SoC HPET implementation supports the direct FSB interrupt delivery.
14	1h RO	**Timer 6 FSB Interrupt Delivery Enable (TIMER6_FSB_EN_CNF):** When set, this will force the interrupts for Timer n to be delivered directly as FSB messages, rather than using the 8259 or I/O (x) APIC. In this case, the TIMERn_INT_ROUTE_CNF field in this register will be ignored and the TIMERn_FSB_ROUT register will be used instead. Timer 0, 1, 2, 3: This bit is a read/write bit. Timer 4, 5, 6, 7: This bit is always Read-Only 1 as interrupt from these timers can only be delivered via direct FSB interrupt messages.

Bit Range	Default & Access	Field Name (ID): Description
13:9	0h RO	**Interrupt Route (TIMER6_INT_ROUT_CNF):** This 5-bit field indicates the routing for the interrupt to the 8259 or I/O APIC. A maximum of 32 interrupts are supported. Software writes to this field to select which interrupt in the 8259 or I/O (x)APIC will be used for this timers interrupt. The default value for this register is 00h. If the Legacy Rout bit is set, then Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers. If the TIMERn_FSB_EN_CNF bit is set, then the interrupt will be delivered directly to the FSB, and this bit field has no effect. If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Software must not program any value other than 0-15 in this field. Software must ensure that the value is valid for a particular timer as indicated by the TIMERn_INT_ROUTE_CAP field for that timer. The PCH logic does not check the validity of the value written. For Timers 4-7, this field is always Read-Only 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
8	0h RO	**Timer 6 32-bit Mode (TIMER6_32_MODE_CNF):** Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if the software is not willing to halt the main counter to read or write a particular timer, and the software not capable of do an atomic 64-bit read to the timer. When TIMER0_32MODE_CNF is set to '1', the hardware counter will essentially be doing 32-bit operation on comparator match and rollovers. I.e. the upper 32-bit of the Timer 0 Comparator Value register is ignored. The upper 32-bit of the main counter is not involved in any roll over from lower 32-bit of the main counter and becomes all zero's. For timer 0, this bit will be read/write and default to 0. For timers 1-7, this bit will always read as 0 and writes will have no effect (since these seven timers are 32-bits).
7	0h RO	**Reserved (RSV_7):** This bit will return 0 when read. Writes will have no effect.
6	0h RO	**Timer 6 Value Set (TIMER6_VAL_SET_CNF):** Software uses this bit only for timers that have been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timers accumulator. Software does NOT have to write this bit back to 0 (it automatically clears). This bit will return 0 when read. Software should not write a 1 to this bit position if the timer is set to non-periodic mode. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1-7 as they do not support the periodic mode.
5	0h RO	**Timer 6 Size (TIMER6_SIZE_CAP):** Read-only Indicator of the timers size capability. 1: 64-bits 0: 32-bits. The value is 1 (64-bits) for timer 0, and 0 (32-bits) for timers 1-7.
4	0h RO	**Periodic Interrupt Capable (TIMER6_PER_INT_CAP):** If this read-only bit is 1, then the hardware supports a periodic mode for this timers interrupt. The value is 1 (periodic supported) for timer 0, and 0 (not supported) for timers 1-7.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Timer 6 Type (TIMER6_TYPE_CNF):** Setting this bit to 1 enables the timer to generate a periodic interrupt if it is capable of doing so. If the TIMERn_PER_INT_CAP bit is 0, then this bit will always return 0 when read and writes will have no impact. For timer 0, this bit will be read/write, with default of 0. For timers 1-7, this bit will be read-only, with a fixed value of 0.
2	0h RW	**Timer 6 Interrupt Enable (TIMER6_INT_ENB_CNF):** This bit must be set to 1 to enable timer n to cause an interrupt when it times out. If this bit is 0, the timer can still count and generate appropriate status bits, but will not cause an interrupt. Default value is 0.
1	0h RO	**Timer Interrupt Type (TIMER6_INT_TYPE_CNF):** Determines whether an edge or level interrupt will be used for this timer (when enabled). 0: Edge-triggered. If another interrupt occurs, another edge will be generated. 1: Level-triggered. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active. The default value is 0, edge-triggered. The interrupt type for any timer should be set before that timer generates any interrupts. If the interrupt type is changed dynamically, there will be some delay before the new type takes effect. That delay is not specified. Timer 0-3: This bit is a read/write bit as both edge and level triggered modes are supported. Timer 4-7: This bit is always Read-Only 0 as only edge-triggered mode is supported.
0	0h RO	**Reserved (RSV_0):** These bits will return 0 when read. Writes will have no effect.

15.4.23 Timer 6 Comparator Value (TMR6_CMP_VAL)—Offset FED001C8h

Timer 6 Comparator Value Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RO	**Reserved (RSV):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**Timer 6 Comparator Value (TMR6_CMP_VAL):** If the timer is configured to non-periodic mode, when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). The value in this register does not change based on the interrupt being generated. If the timer is configured to periodic mode (supported only for Timer 0), when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). When this time out occurs, the value in this register is increased by the value last written to the register. For example, in periodic mode if the value written to the register is 0000123h: 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h. 4. The value in this register will then be adjusted by the hardware to 00000369h As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h The default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer will have a default value of 00000000FFFFFFFFh. A 64-bit timer will have a default value of FFFFFFFFFFFFFFFFh. Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x8h or 1xCh. 64-bit accesses may only be done to 1x8h. Comparator value. Timer 0 is 64-bits wide. Timers 1-7 are 32-bits wide.

15.4.24 Timer 6 FSB Interrupt Rout Register (TMR6_FSB_INT_ROUT)—Offset FED001D0h

Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x0h or 1x4h. 64-bit accesses may only be done to 1x0h.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:34	0h RW	**Timer 6 FSB Interrupt Address (TIMER6_FSB_INT_ADDR):** Software sets this 32-bit field to indicate the location that the FSB interrupt message should be written. Intel-Specific: This register is implemented for timer 0:7.
33:32	0h RO	**Reserved (RSV):** Bit(33:32) are read-only and hard-wired to 0.
31:0	0h RW	**Timer 6 FSB Interrupt Value (TIMER6_FSB_INT_VAL):** Software sets this 32-bit field to indicate that value that is written during the FSB interrupt message. Intel-Specific: This register is implemented for timer 0:7.

15.4.25 Timer 7 Config and Capabilities (TMR7_CNF_CAP)—Offset FED001E0h

Timer 7 config and Capabilities Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C000h

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RO	**Timer 7 Interrupt Rout (TIMER7_INT_ROUT_CAP):** This 32-bit read-only field indicates to which interrupts in the 8259 or I/O (x) APIC this timers interrupt can be routed to. This is used in conjunction with the TIMERn_INT_ROUT_CNF field. Writes to this field will have no effect. Note: If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Each bit in this field corresponds to a particular interrupt. For example, if this timers interrupt can be mapped to interrupts 16, 18, 20, 22, or 24, then bits 16, 18, 20, 22, and 24 in this field will be set to 1. All other bits will be 0. Timer 0,1 : Bits 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. Timer 2 : Bits 11, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 11 is used, software should ensure IRQ 11 is not shared with any other devices to guarantee the proper operation of this timer. Timer 3 : Bits 12, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 12 is used, software should ensure IRQ 12 is not shared with any other devices to guarantee the proper operation of this timer. Timer 4-7: This field is always 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
31:16	0h RO	**Reserved (RSV_31_16):** These bits will return 0 when read. Writes will have no effect.

Bit Range	Default & Access	Field Name (ID): Description
15	1h RO	**FSB Interrupt Delivery Capability (TIMER7_FSB_INT_DEL_CAP):** This bit is always read as 1, since the SoC HPET implementation supports the direct FSB interrupt delivery.
14	1h RO	**Timer 7 FSB Interrupt Delivery Enable (TIMER7_FSB_EN_CNF):** When set, this will force the interrupts for Timer n to be delivered directly as FSB messages, rather than using the 8259 or I/O (x) APIC. In this case, the TIMERn_INT_ROUTE_CNF field in this register will be ignored and the TIMERn_FSB_ROUT register will be used instead. Timer 0, 1, 2, 3: This bit is a read/write bit. Timer 4, 5, 6, 7: This bit is always Read-Only 1 as interrupt from these timers can only be delivered via direct FSB interrupt messages.
13:9	0h RO	**Interrupt Route (TIMER7_INT_ROUT_CNF):** This 5-bit field indicates the routing for the interrupt to the 8259 or I/O APIC. A maximum of 32 interrupts are supported. Software writes to this field to select which interrupt in the 8259 or I/O (x)APIC will be used for this timers interrupt. The default value for this register is 00h. If the Legacy Rout bit is set, then Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers. If the TIMERn_FSB_EN_CNF bit is set, then the interrupt will be delivered directly to the FSB, and this bit field has no effect. If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Software must not program any value other than 0-15 in this field. Software must ensure that the value is valid for a particular timer as indicated by the TIMERn_INT_ROUTE_CAP field for that timer. The PCH logic does not check the validity of the value written. For Timers 4-7, this field is always Read-Only 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
8	0h RO	**Timer 7 32-bit Mode (TIMER7_32_MODE_CNF):** Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if the software is not willing to halt the main counter to read or write a particular timer, and the software not capable of do an atomic 64-bit read to the timer. When TIMER0_32MODE_CNF is set to '1', the hardware counter will essentially be doing 32-bit operation on comparator match and rollovers. I.e. the upper 32-bit of the Timer 0 Comparator Value register is ignored. The upper 32-bit of the main counter is not involved in any roll over from lower 32-bit of the main counter and becomes all zero's. For timer 0, this bit will be read/write and default to 0. For timers 1-7, this bit will always read as 0 and writes will have no effect (since these seven timers are 32-bits).
7	0h RO	**Reserved (RSV_7):** This bit will return 0 when read. Writes will have no effect.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**Timer 7 Value Set (TIMER7_VAL_SET_CNF):** Software uses this bit only for timers that have been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timers accumulator. Software does NOT have to write this bit back to 0 (it automatically clears). Software should not write a 1 to this bit position if the timer is set to non-periodic mode. Intel Specific: This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1, 2, 3, 4, 5, 6, and 7.
5	0h RO	**Timer 7 Size (TIMER7_SIZE_CAP):** Read-only Indicator of the timers size capability. 1: 64-bits 0: 32-bits. The value is 1 (64-bits) for timer 0, and 0 (32-bits) for timers 1-7.
4	0h RO	**Periodic Interrupt Capable (TIMER7_PER_INT_CAP):** If this read-only bit is 1, then the hardware supports a periodic mode for this timers interrupt. The value is 1 (periodic supported) for timer 0, and 0 (not supported) for timers 1-7.
3	0h RO	**Timer 7 Type (TIMER7_TYPE_CNF):** Setting this bit to 1 enables the timer to generate a periodic interrupt if it is capable of doing so. If the TIMERn_PER_INT_CAP bit is 0, then this bit will always return 0 when read and writes will have no impact. For timer 0, this bit will be read/write, with default of 0. For timers 1-7, this bit will be read-only, with a fixed value of 0.
2	0h RW	**Timer 7 Interrupt Enable (TIMER7_INT_ENB_CNF):** This bit must be set to 1 to enable timer n to cause an interrupt when it times out. If this bit is 0, the timer can still count and generate appropriate status bits, but will not cause an interrupt. Default value is 0.
1	0h RO	**Timer Interrupt Type (TIMER7_INT_TYPE_CNF):** Determines whether an edge or level interrupt will be used for this timer (when enabled). 0: Edge-triggered. If another interrupt occurs, another edge will be generated. 1: Level-triggered. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active. The default value is 0, edge-triggered. The interrupt type for any timer should be set before that timer generates any interrupts. If the interrupt type is changed dynamically, there will be some delay before the new type takes effect. That delay is not specified. Timer 0-3: This bit is a read/write bit as both edge and level triggered modes are supported. Timer 4-7: This bit is always Read-Only 0 as only edge-triggered mode is supported.
0	0h RO	**Reserved (RSV_0):** These bits will return 0 when read. Writes will have no effect.

15.4.26 Timer 7 Comparator Value (TMR7_CMP_VAL)—Offset FED001E8h

Timer 7 Comparator Value Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RO	**Reserved (RSV):** Reserved.
31:0	FFFFFFFFh RW	**Timer 7 Comparator Value (TMR7_CMP_VAL):** If the timer is configured to non-periodic mode, when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). The value in this register does not change based on the interrupt being generated. If the timer is configured to periodic mode (supported only for Timer 0), when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). When this time out occurs, the value in this register is increased by the value last written to the register. For example, in periodic mode if the value written to the register is 0000123h: 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h. 4. The value in this register will then be adjusted by the hardware to 00000369h As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h The default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer will have a default value of 00000000FFFFFFFFh. A 64-bit timer will have a default value of FFFFFFFFFFFFFFFFh. Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x8h or 1xCh. 64-bit accesses may only be done to 1x8h. Comparator value. Timer 0 is 64-bits wide. Timers 1-7 are 32-bits wide.

15.4.27 Timer 7 FSB Interrupt Rout Register (TMR7_FSB_INT_ROUT)—Offset FED001F0h

Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x0h or 1x4h. 64-bit accesses may only be done to 1x0h.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:34	0h RW	**Timer 7 FSB Interrupt Address (TIMER7_FSB_INT_ADDR):** Software sets this 32-bit field to indicate the location that the FSB interrupt message should be written. Intel-Specific: This register is implemented for timer 0:7.
33:32	0h RO	**Reserved (RSV):** Bit(33:32) are read-only and hard-wired to 0.
31:0	0h RW	**Timer 7 FSB Interrupt Value (TIMER7_FSB_INT_VAL):** Software sets this 32-bit field to indicate that value that is written during the FSB interrupt message. Intel-Specific: This register is implemented for timer 0:7.

15.5 Registers Summary

Table 15-5. Summary of 0_31_0_INTR IO Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
20h	20h	Master Initialization Command Word 1 (MICW1)—Offset 20h	11h
20h	20h	Master Operational Control Word 2 (MOCW2)—Offset 20h	0h
20h	20h	Master Operational Control Word 3 (MOCW3)—Offset 20h	8h
21h	21h	Master Initialization Command Word 2 (MICW2)—Offset 21h	0h
21h	21h	Master Initialization Command Word 3 (MICW3)—Offset 21h	7h
21h	21h	Master Initialization Command Word 4 (MICW4)—Offset 21h	0h
21h	21h	Master Operational Control Word 1 (MOCW1)—Offset 21h	0h
A0h	A0h	Slave Operational Control Word 3 (SOCW3)—Offset A0h	8h
A0h	A0h	Slave Initialization Command Word 1 (SICW1)—Offset A0h	11h
A0h	A0h	Slave Operational Control Word 2 (SOCW2)—Offset A0h	0h
A1h	A1h	Slave Initialization Command Word 3 (SICW3)—Offset A1h	7h
A1h	A1h	Slave Initialization Command Word 4 (SICW4)—Offset A1h	0h
A1h	A1h	Slave Operational Control Word 1 (SOCW1)—Offset A1h	0h
A1h	A1h	Slave Initialization Command Word 2 (SICW2)—Offset A1h	0h
4D0h	4D0h	Master Edge/Level Control (ELCR1)—Offset 4D0h	0h
4D1h	4D1h	Slave Edge/Level Control (ELCR2)—Offset 4D1h	0h

15.5.1 Master Initialization Command Word 1 (MICW1)—Offset 20h

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:
1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.

3. The slave mode address is set to 7.
4. Special Mask Mode is cleared and Status Read is set to IRR.
Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 11h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h WO	**ICW/OCW select (ICW_OCW_SLT1):** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	1h WO	**ICW/OCW select (ICW_OCW_SLT2):** This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	0h WO	**Edge/Level Bank Select (LTIM):** Disabled. Replaced by the edge/level triggered control registers (ELCR).
2	0h WO	**ADI-IGNORED (ADI):** Ignored for PCH. Should be programmed to 0.
1	0h WO	**Single or Cascade (SNGL):** Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	1h WO	**ICW4 Write Required (IC4):** This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

15.5.2 Master Operational Control Word 2 (MOCW2)—Offset 20h

*address should be 20h
Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h WO	**Rotate and EOI Codes (REOI):** R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 Rotate in Auto EOI Mode (Clear) 001 Non-specific EOI command 010 No Operation 011 *Specific EOI Command 100 Rotate in Auto EOI Mode (Set) 101 Rotate on Non-Specific EOI Command 110 *Set Priority Command 111 *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	0h WO	**OCW2 Select (O2S):** When selecting OCW2, bits 4:3 = 00
2:0	0h WO	**Interrupt Level Select (L2, L1, L0) (ILSLT):** L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function, programming L2, L1 and L0 to 0 is sufficient in this case.

15.5.3 Master Operational Control Word 3 (MOCW3)—Offset 20h

*address should be 20h

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved (RSVD):** Must be 0.
6	0h WO	**Special Mask Mode (SMM):** If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
5	0h WO	**Enable Special Mask Mode (ESMM):** When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a "don't care".
4:3	1h WO	**OCW3 Select (O3S):** When selecting OCW3, bits 4:3 = 01

Bit Range	Default & Access	Field Name (ID): Description
2	0h WO	**Poll Mode Command (PMC):** When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	0h WO	**Register Read Command (RRC):** These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not affect the register read selection. Following ICW initialization, the default OCW3 port address read will be "read IRR". To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. Value Command 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

15.5.4 Master Initialization Command Word 2 (MICW2)—Offset 21h

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h WO	**Interrupt Vector Base Address (IVBA):** Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h WO	**Interrupt Request Level (IRL):** When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

15.5.5 Master Initialization Command Word 3 (MICW3)—Offset 21h

*address should be 21h

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 7h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h WO	**MICW3 [7:3] (MICW3_7_3):** These bits must be programmed to zero.
2	1h WO	**Cascaded Controller Connection (CCC):** This bit must always be programmed to a 1 to indicate the slave controller for interrupts 8 - 15 is cascaded on IRQ2.
1:0	3h WO	**MICW [1:0] (MICW3_1_0):** These bits must be programmed to zero.

15.5.6 Master Initialization Command Word 4 (MICW4)—Offset 21h

*address should be 21h

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h WO	**Reserved (RSVD):** Must be 0.
4	0h WO	**Special Fully Nested Mode (SFNM):** Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0h WO	**Buffered Mode (BUF):** Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0h WO	**Master/Slave in Buffered Mode (MSBM):** Not used. Should always be programmed to 0.
1	0h WO	**Automatic End of Interrupt (AEOI):** This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed. AEOI is discussed in Section 13.1.7.2
0	0h WO	**Microprocessor Mode (MM):** This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.1

15.5.7 Master Operational Control Word 1 (MOCW1)—Offset 21h

*address should be 21h

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Request Mask (IRM):** When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

15.5.8 Slave Operational Control Word 3 (SOCW3)—Offset A0h

*address should be A0h

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved (RSVD):** Must be 0.
6	0h WO	**Special Mask Mode (SMM):** If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
5	0h WO	**Enable Special Mask Mode (ESMM):** When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a "don't care".
4:3	1h WO	**OCW3 Select (O3S):** When selecting OCW3, bits 4:3 = 01
2	0h WO	**Poll Mode Command (PMC):** When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	0h WO	**Register Read Command (RRC):** These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not affect the register read selection. Following ICW initialization, the default OCW3 port address read will be "read IRR". To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. Value Command 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

15.5.9 Slave Initialization Command Word 1 (SICW1)—Offset A0h

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:
1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The slave mode address is set to 7.
4. Special Mask Mode is cleared and Status Read is set to IRR.

Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 11h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h WO	**ICW/OCW select (ICW_OCW_SLT1):** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	1h WO	**ICW/OCW select (ICW_OCW_SLT2):** This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	0h WO	**Edge/Level Bank Select (LTIM):** Disabled. Replaced by the edge/level triggered control registers (ELCR).
2	0h WO	**ADI-IGNORED (ADI):** Ignored for PCH. Should be programmed to 0.
1	0h WO	**Single or Cascade (SNGL):** Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	1h WO	**ICW4 Write Required (IC4):** This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

15.5.10 Slave Operational Control Word 2 (SOCW2)—Offset A0h

*address should be A0h
Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h WO	**Rotate and EOI Codes (REOI):** R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 Rotate in Auto EOI Mode (Clear) 001 Non-specific EOI command 010 No Operation 011 *Specific EOI Command 100 Rotate in Auto EOI Mode (Set) 101 Rotate on Non-Specific EOI Command 110 *Set Priority Command 111 *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	0h WO	**OCW2 Select (O2S):** When selecting OCW2, bits 4:3 = 00

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h WO	**Interrupt Level Select (L2, L1, L0) (ILSLT):** L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function, programming L2, L1 and L0 to 0 is sufficient in this case.

15.5.11 Slave Initialization Command Word 3 (SICW3)—Offset A1h

*address should be A1h

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 7h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h WO	**Reserved (RSVD):** Must be 0.
2:0	7h WO	**Slave Identification Code (SIC):** This field must be programmed to 02h to match the code broadcast by the master controller during the INTA# sequence.

15.5.12 Slave Initialization Command Word 4 (SICW4)—Offset A1h

*address should be A1h

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h WO	**Reserved (RSVD):** Must be 0.
4	0h WO	**Special Fully Nested Mode (SFNM):** Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0h WO	**Buffered Mode (BUF):** Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0h WO	**Master/Slave in Buffered Mode (MSBM):** Not used. Should always be programmed to 0.

Bit Range	Default & Access	Field Name (ID): Description
1	0h WO	**Automatic End of Interrupt (AEOI):** This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed. AEOI is discussed in Section 13.1.7.2
0	0h WO	**Microprocessor Mode (MM):** This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.1

15.5.13 Slave Operational Control Word 1 (SOCW1)—Offset A1h

*address should be A1h

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Request Mask (IRM):** When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

15.5.14 Slave Initialization Command Word 2 (SICW2)—Offset A1h

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h WO	**Interrupt Vector Base Address (IVBA):** Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h WO	**Interrupt Request Level (IRL):** When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

15.5.15 Master Edge/Level Control (ELCR1)—Offset 4D0h

Master Edge/Level Control Register

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RW	**Edge Level Control (ELC_7_3):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level.
2:0	0h RO	**Reserved (RSVD):** The cascade channel(IRQ2), heart beat timer (IRQ0), and keyboard controller (IRQ1), cannot be put into level mode

15.5.16 Slave Edge/Level Control (ELCR2)—Offset 4D1h

Slave Edge/Level Control Register

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RW	**Edge Level Control (ELC_15_14):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 7 applies to IRQ15, and bit 6 to IRQ14.
5	0h RW	**Edge Level Control (ELC_13):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. This bit applies to IRQ13.
4:1	0h RW	**Edge Level Control (ELC_12_9):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 4 applies to IRQ12, bit 3 to IRQ11, bit 2 to IRQ10, and bit 1 to IRQ9.
0	0h RO	**Reserved (RSVD):** The Real Time Clock (IRQ8#) cannot be programmed for level mode.

15.6 Registers Summary

Table 15-6. Summary of 0_31_0_LEG_8254_TIMER IO Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
40h	40h	Counter 0 - Interval Timer Status Byte Format Register (C0_ITSBFR)—Offset 40h	C4h
40h	40h	Counter 0 - Counter Access Ports Register (C0_CAPR)—Offset 40h	0h
42h	42h	Counter 2 - Interval Timer Status Byte Format Register (C2_ITSBFR)—Offset 42h	C4h
42h	42h	Counter 2 - Counter Access Ports Register (C2_CAPR)—Offset 42h	0h
43h	43h	Timer Control Word Register (TCW)—Offset 43h	0h
43h	43h	Read Back Command (RBC)—Offset 43h	C0h
43h	43h	Counter Latch Command (CLC)—Offset 43h	0h

15.6.1 Counter 0 - Interval Timer Status Byte Format Register (C0_ITSBFR)—Offset 40h

Each counter's status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0 and 42h for counter 2) returns the status byte. The status byte returns the following:

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: C4h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Counter OUT Pin State (COPS):** When this bit is a 1, the OUT pin of the counter is also a 1. When this bit is a 0, the OUT pin of the counter is also a 0.
6	1h RO	**Count Register Status (CRSTS):** This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode, but until the count is loaded into the counting element (CE), the count value will be incorrect. 0 Count has been transferred from CR to CE and is available for reading. 1 Null Count. Count has not been transferred from CR to CE and is not yet available for reading.
5:4	0h RO	**Read/Write Selection Status (RW_SLT_STS):** These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	2h RO	**Mode Selection Status (MD_SLT_STS):** These bits return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	0h RO	**Countdown Type Status (CDT_STS):** This bit reflects the current countdown type, ether 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

15.6.2 Counter 0 - Counter Access Ports Register (C0_CAPR)—Offset 40h

*Address should be 40h

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Counter Port (CP):** Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

15.6.3 Counter 2 - Interval Timer Status Byte Format Register (C2_ITSBFR)—Offset 42h

Each counter's status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0 and 42h for counter 2) returns the status byte. The status byte returns the following:

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: C4h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Counter OUT Pin State (COPS):** When this bit is a 1, the OUT pin of the counter is also a 1. When this bit is a 0, the OUT pin of the counter is also a 0.
6	1h RO	**Count Register Status (CRSTS):** This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode, but until the count is loaded into the counting element (CE), the count value will be incorrect. 0 Count has been transferred from CR to CE and is available for reading. 1 Null Count. Count has not been transferred from CR to CE and is not yet available for reading.
5:4	0h RO	**Read/Write Selection Status (RW_SLT_STS):** These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB

Bit Range	Default & Access	Field Name (ID): Description
3:1	2h RO	**Mode Selection Status (MD_SLT_STS):** These bits return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	0h RO	**Countdown Type Status (CDT_STS):** This bit reflects the current countdown type, ether 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

15.6.4 Counter 2 - Counter Access Ports Register (C2_CAPR)—Offset 42h

*Address should be 42h

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Counter Port (CP):** Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

15.6.5 Timer Control Word Register (TCW)—Offset 43h

This register is programmed prior to any counter being accessed to specify counter modes. Following reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state. There are two special commands that can be issued to the counters through this register, the Read Back Command and the Counter Latch Command. When these commands are chosen, several bits within this register are redefined.

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h WO	**Counter Select (CNT_SLT):** The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1 00 Counter 0 select 01 Reserved 10 Counter 2 select 11 Read Back Command
5:4	0h WO	**Read/Write Select: (RW_SLT):** These bits are the read/write control bits. The actual counter programming is done through the counter port (40h for counter 0 and 42h for counter 2) 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	0h WO	**Counter Mode Selection (CNT_MD_SLTN):** These bits select one of six possible modes of operation for the selected counter. 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	0h WO	**Binary/BCD Countdown Select (B_BCD_CNTDWN_SLT):** 0 Binary countdown is used. The largest possible binary count is 2^16 1 Binary coded decimal (BCD) count is used.The largest possible BCD count is 10^4

15.6.6 Read Back Command (RBC)—Offset 43h

*Address should be 43h
The Read Back Command is used to determine the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter or counters. Status and/or count may be latched in any or all of the counters by selecting the counter during the register write. The count and status remain latched until read, and further latch commands are ignored until the count is read.
Both count and status of the selected counters may be latched simultaneously by setting both bit 5 and bit 4 to 0. If both are latched, the first read operation from that counter returns the latched status. The next one or two reads, depending on whether the counter is programmed for one or two byte counts, returns the latched count. Subsequent reads return an unlatched count.

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: C0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	3h WO	**Read Back Command (RBC):** Must be 11 to select the Read Back Command
5	0h WO	**Latch Count of Selected Counters (LCSC):** 0 Current count value of the selected counters will be latched 1 Current count will not be latched
4	0h WO	**Latch Status of Selected Counters (LSSC):** 0 Status of the selected counters will be latched 1 Status will not be latched
3	0h WO	**Counter 2 Select (CNT_2_SLT):** When set to 1, Counter 2 count and/or status will be latched
2	0h WO	**Reserved (RSVD):** Reserved
1	0h WO	**Counter 0 Select (CNT_0_SLT):** When set to 1, Counter 0 count and/or status will be latched.
0	0h WO	**Reserved (RSVD_1):** Must be 0.

15.6.7 Counter Latch Command (CLC)—Offset 43h

*Address should be 43h
The Counter Latch Command latches the current count value. This command is used to insure that the count read from the counter is accurate. The count value is then read from each counter's count register through the Counter Ports Access Ports Register (40h for counter 0 and 42h for counter 2). The count must be read according to the programmed format, i.e. if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other (read, write, or programming operations for other counters may be inserted between the reads). If a counter is latched once and then latched again before the count is read, the second Counter Latch Command is ignored.

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h WO	**Counter Selection (CNT_SLT):** These bits select the counter for latching. If 11 is written, then the write is interpreted as a read back command. 00 = Counter 0 01 = Reserved 10 = Counter 2
5:4	0h WO	**Counter Latch Command (CLC):** Write 00 to select the Counter Latch Command.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h WO	**Reserved (RSVD):** Must be 0.

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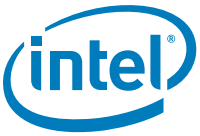


16 IOSF2OCP

16.1 Registers Summary

Table 16-1. Summary of map_iosf2ocp_pci_configreg Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h	22D88086h
4h	7h	STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h	6h
Ch	Fh	CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	0h
10h	13h	BAR -Base Address Register (BAR)—Offset 10h	4h
14h	17h	BAR -Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	BAR1 -Base Address Register1 (BAR1)—Offset 18h	4h
1Ch	1Fh	BAR1 -Base Address Register1 High (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch	0h
80h	83h	POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h	39001h
84h	87h	PMECTRLSTATUS_type Power Management Control and status register (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI DEVICE IDLE CAPABILITY RECORD (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	DEVID VENDOR SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	D0I3_CONTROL_SW_LTR_MMIO_REG - SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	DEVICE_IDLE_POINTER_REG - Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	6D01h
A0h	A3h	D0I3_MAX_POW_LAT_PG_CONFIG - DEVICE PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	0h

16.1.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Device ID and Vendor ID provided by this register uniquely identifies the XXX Device

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 22D88086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	22D8h RO	**DEVICEID:** Device ID identifies the particular PCI device
15:0	8086h RO	**VENDORID:** Vendor ID is a unique ID provided by the PCI SIG, which identifies the manufacturer of the device

16.1.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

Command register to programme interrupt disable , bus master enable, and Memory space enable. Status register to read the errors and aborts

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0:** Reserved 0
29	0h RW/1C	**RMA:** Received Master Abort
28	0h RW/1C	**RTA:** Received Target Abort
27:21	0h RO	**Reserved1:** Reserved
20	1h RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device
18:16	0h RO	**Reserved2:** Reserved
15:11	0h RO	**Reserved3:** Reserved
10	0h RW	**INTR_DISABLE:** Interrupt Disable
9	0h RO	**Reserved4:** Reserved
8	0h RW	**SERR_ENABLE:** SERR Enable , Not implemented

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved5:** Reserved
2	0h RW	**BME:** Bus Master Enable
1	0h RW	**MSE:** Memory Space Enable
0	0h RO	**Reserved6:** Reserved

16.1.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Revision ID register identifies revision of particular device and Class Code register is used to identify generic function of the device

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 6h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface
7:0	6h RO	**RID:** Revision ID identifies the revision of particular PCI device.

16.1.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Cache Line size as RW with def 0, Latency timer RW with def 0, Header type with Type 0 configuration header and Reserved BIST register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved0:** Reserved
23	0h RO	**MULFNDEV:** Multi-Function Device

Bit Range	Default & Access	Field Name (ID): Description
22:16	0h RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header
15:8	0h RO	**LATTIMER:** Latency Timer:. This register is implemented as R/W with default as 0
7:0	0h RW	**CACHELINE_SIZE:** Cacheline Size

16.1.5 BAR -Base Address Register (BAR)—Offset 10h

Base Address Register low [31:2] , type[2:1] in 32bit or 64bit addr range and memory space indicator [0]

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR:** Base Address Register Low, Base address of the OCP fabric memory space. Taken from Strap values as ones
11:4	0h RO	**SIZEINDICATOR:** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable
2:1	2h RO	**TYPE:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range, If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE:** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

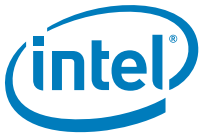
16.1.6 BAR -Base Address Register High (BAR_HIGH)—Offset 14h

Base Address Register High enabled if [2:1] of BAR_type_LOW is 10

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR_HIGH:** Base Address high - MSB

16.1.7 BAR1 -Base Address Register1 (BAR1)—Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K, type in [2:1] and memory space indicator in [0]

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR1:** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	0h RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0h RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	2h RO	**TYPE1:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

16.1.8 BAR1 -Base Address Register1 High (BAR1_HIGH)—Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR1_HIGH:** Base Address: Base address of the OCP fabric memory space. Taken from Strap values as ones

16.1.9 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID:** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0h RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

16.1.10 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address register is a RO indicates support for expansion ROMs

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE:** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

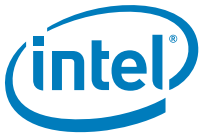
16.1.11 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Capabilities Pointer register indicates what the next capability is

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved0:** Reserved
7:0	80h RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is.

16.1.12 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

Interrupt line Register isn't used in Bridge directly, Interrupt Pin register reflects the IPIN value in private config space. Min_gnt register indicating the req of latency timers and max_lat register max latency

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT:** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**MIN_GNT:** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved0:** Reserved
11:8	0h RO	**INTPIN:** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0h RW	**INTLINE:** Interrupt Line: It is used to communicate to software, the interrupt line to which the interrupt pin is connected

16.1.13 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

PowerManagement Capability ID register points to next capability structure and power mgmnt capability , with Power management capabilities register for PME support and version

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 39001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**PMESUPPORT:** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved0:** Reserved
18:16	3h RO	**VERSION:** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**NXTCAP:** Next Capability: Points to the next capability structure.
7:0	1h RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability

16.1.14 PMECTRLSTATUS_type Power Management Control and status register (PMECTRLSTATUS)—Offset 84h

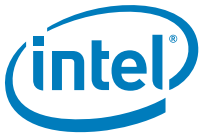
power management control and status register to set and read PME status, PME enable, No Soft reset and power state

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved0:** Reserved
15	0h RW/1C	**PMESTATUS:** PME Status
14:9	0h RO	**Reserved1:** Reserved
8	0h RW	**PMEENABLE:** PME Enable
7:4	0h RO	**Reserved2:** Reserved
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	**Reserved3:** Reserved
1:0	0h RW	**POWERSTATE:** Power State: This field is used both to determine the current power state and to set a new power state



16.1.15 PCI DEVICE IDLE CAPABILITY RECORD (PCIDEVIDLE_CAP_RECORD)—Offset 90h

PCI Device Vendor Specific Capability register defines Vendor specific Capability ID, revision , length , next capability and CAPID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** Vendor Specific Capability ID
27:24	0h RO	**REVID:** Revision ID of capability structure
23:16	14h RO	**CAP_LENGTH:** Vendor Specific Capability Length
15:8	0h RO	**NEXT_CAP:** Next Capability
7:0	9h RO	**CAPID:** Capability ID

16.1.16 DEVID VENDOR SPECIFIC REG (DEVID_VEND_SPECIFIC_REG)—Offset 94h

Extended Vendor capability register for VSEC Length, revision and ID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH:** Vendor Specific Extended Capability Length
19:16	0h RO	**VSEC_REV:** Vendor specific Extended Capability revision
15:0	10h RO	**VSECID:** Vendor Specific Extended Capability ID

16.1.17 D0I3_CONTROL_SW_LTR_MMIO_REG - SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Software location pointer in MMIO space as an offset specified by BAR

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW_LAT_DWORD_OFFSET:** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW_LAT_BAR_NUM:** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW_LAT_VALID:** This value is reflected from the SW LTR valid strap at the top level

16.1.18 DEVICE_IDLE_POINTER_REG - Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location , BAR NUM and D0i3 Valid Strap

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 6D01h

Bit Range	Default & Access	Field Name (ID): Description
31:4	6D0h RO	**DWORD_OFFSET:** contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR
3:1	0h RO	**BAR_NUM:** Bar num: Indicates that the D0i3 MMIO location is always at BAR0
0	1h RO	**VALID:** Valid: This value is reflected from the D0i3 valid strap at the top level.

16.1.19 D0I3_MAX_POW_LAT_PG_CONFIG - DEVICE PG CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

D0idle_Max_Power_On_Latency register set at boot and Power control enable register to enable communication with the PGCB block below the Bridge

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 17 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved0:** Reserved
21	0h RO	**HAE:** Hardware Autonomous Enable
20	0h RO	**Reserved1:** Reserved
19	0h RO	**SLEEP_EN:** Sleep Enable
18	0h RO	**PGE:** DEVIDLE Enable (DEVIDLEN): If ?1?, then the function will power gate when idle and the DevIdle register (DevIdleC[2] = ?1?) is set.
17	0h RO	**I3_ENABLE:** D3-Hot Enable (D3HEN): If ?1?, then function will power gate when idle and the PMCSR[1:0] register in the function =?11? (D3).
16	0h RO	**PMCRE:** PMCRE: PMC Request Enable
15:13	0h RO	**Reserved2:** Reserved
12:10	0h RW/O	**POW_LAT_SCALE:** Power On Latency Scale
9:0	0h RW/O	**POW_LAT_VALUE:** Power On Latency value

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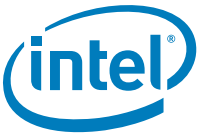


17 PCIe

17.1 Registers Summary

Table 17-1. Summary of pcie_cfg Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4h	7h	Device Command; Primary Status (CMD_PSTS)—Offset 4h	100000h
8h	Bh	Revision ID;Class Code (RID_CC)—Offset 8h	60400F0h
Ch	Fh	Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch	810000h
18h	1Bh	Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h	0h
1Ch	1Fh	I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch	0h
20h	23h	Memory Base and Limit (MBL)—Offset 20h	0h
24h	27h	Prefetchable Memory Base and Limit (PMBL)—Offset 24h	10001h
28h	2Bh	Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h	0h
2Ch	2Fh	Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch	0h
34h	37h	Capabilities List Pointer (CAPP)—Offset 34h	40h
3Ch	3Fh	Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch	0h
40h	43h	Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h	428010h
44h	47h	Device Capabilities (DCAP)—Offset 44h	8001h
48h	4Bh	Device Control; Device Status (DCTL_DSTS)—Offset 48h	100000h
4Ch	4Fh	Link Capabilities (LCAP)—Offset 4Ch	710C00h
50h	53h	Link Control; Link Status (LCTL_LSTS)—Offset 50h	10000h
54h	57h	Slot Capabilities (SLCAP)—Offset 54h	40060h
58h	5Bh	Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h	0h
5Ch	5Fh	Root Control (RCTL)—Offset 5Ch	0h
60h	63h	Root Status (RSTS)—Offset 60h	0h
64h	67h	Device Capabilities 2 (DCAP2)—Offset 64h	80837h
68h	6Bh	Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h	0h
6Ch	6Fh	Link Capabilities 2 (LCAP2)—Offset 6Ch	0h
70h	73h	Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h	0h
74h	77h	Slot Capabilities 2 (SLCAP2)—Offset 74h	0h
78h	7Bh	Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h	0h
80h	83h	Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h	9005h
88h	8Bh	Message Signaled Interrupt Message Data (MD)—Offset 88h	0h
90h	93h	Subsystem Vendor Capability (SVCAP)—Offset 90h	A00Dh
94h	97h	Subsystem Vendor IDs (SVID)—Offset 94h	0h
A0h	A3h	Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h	C8030001h
A4h	A7h	PCI Power Management Control And Status (PMCS)—Offset A4h	8h

Table 17-1. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
100h	103h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	0h
104h	107h	Uncorrectable Error Status (UES)—Offset 104h	0h
108h	10Bh	Uncorrectable Error Mask (UEM)—Offset 108h	0h
10Ch	10Fh	Uncorrectable Error Severity (UEV)—Offset 10Ch	60011h
110h	113h	Correctable Error Status (CES)—Offset 110h	0h
114h	117h	Correctable Error Mask (CEM)—Offset 114h	2000h
118h	11Bh	Advanced Error Capabilities and Control (AECC)—Offset 118h	0h
11Ch	11Fh	Header Log DW1 (HL_DW1)—Offset 11Ch	0h
120h	123h	Header Log DW2 (HL_DW2)—Offset 120h	0h
124h	127h	Header Log DW3 (HL_DW3)—Offset 124h	0h
128h	12Bh	Header Log DW4 (HL_DW4)—Offset 128h	0h
12Ch	12Fh	Root Error Command (REC)—Offset 12Ch	0h
134h	137h	Error Source Identification (ESID)—Offset 134h	0h
140h	143h	ACS Extended Capability Header (ACSECH)—Offset 140h	0h
144h	147h	ACS Capability Register (ACSCAPR)—Offset 144h	Fh
148h	14Bh	ACS Control Register (ACSCTLR)—Offset 148h	0h
150h	153h	PTM Extended Capability Header (PTMECH)—Offset 150h	0h
154h	157h	PTM Capability Register (PTMCAPR)—Offset 154h	400h
158h	15Bh	PTM Control Register (PTMCTLR)—Offset 158h	0h
200h	203h	L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h	0h
204h	207h	L1 Sub-States Capabilities (L1SCAP)—Offset 204h	28281Fh
208h	20Bh	L1 Sub-States Control 1 (L1SCTL1)—Offset 208h	0h
20Ch	20Fh	L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch	28h
220h	223h	Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h	0h
224h	227h	Link Control 3 (LCTL3)—Offset 224h	0h
228h	22Bh	Lane Error Status (LES)—Offset 228h	0h
22Ch	22Fh	Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch	7F7F7F7Fh
230h	233h	Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h	7F7F7F7Fh
300h	303h	PCI Express Replay Timer Policy 1 (PCIERTP1)—Offset 300h	A64F96h
304h	307h	PCI Express Replay Timer Policy 2 (PCIERTP2)—Offset 304h	1BC00B86h
328h	32Bh	PCI Express Status 1 (PCIESTS1)—Offset 328h	0h
32Ch	32Fh	PCI Express Status 2 (PCIESTS2)—Offset 32Ch	0h
330h	333h	PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h	2A000016h
334h	337h	PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h	4ABCB5BCh
390h	393h	PTM Propagation Delay (PTMPD)—Offset 390h	0h
394h	397h	PTM Lower Local Master Time (PTMLLMT)—Offset 394h	0h
398h	39Bh	PTM Upper Local Master Time (PTMULMT)—Offset 398h	0h
39Ch	39Fh	PTM Pipe Stage Delay Configuration 1 (PTMPSDC1)—Offset 39Ch	0h

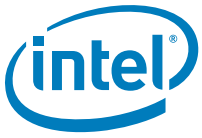


Table 17-1. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3A0h	3A3h	PTM Pipe Stage Delay Configuration 2 (PTMPSDC2)—Offset 3A0h	0h
3A4h	3A7h	PTM Pipe Stage Delay Configuration 3 (PTMPSDC3)—Offset 3A4h	0h
3A8h	3ABh	PTM Pipe Stage Delay Configuration 4 (PTMPSDC4)—Offset 3A8h	0h
3ACh	3AFh	PTM Pipe Stage Delay Configuration 5 (PTMPSDC5)—Offset 3ACh	0h
3B0h	3B3h	PTM Extended Config (PTMECFG)—Offset 3B0h	0h
3B4h	3B7h	PTM Lower T2 Time Stamp (PTMLT2TSTMP)—Offset 3B4h	0h
3B8h	3BBh	PTM Upper T2 Time Stamp (PTMUT2TSTMP)—Offset 3B8h	0h
414h	417h	Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h	0h
418h	41Bh	Thermal and Power Throttling (TNPT)—Offset 418h	930h
41Ch	41Fh	Dynamic Lane Switch (DYNLNSW)—Offset 41Ch	0h
428h	42Bh	Power Control Enable (PCE)—Offset 428h	9h
42Ch	42Fh	PGCB Control1 (PGCBCTL1)—Offset 42Ch	14155555h
430h	433h	PGCB Control2 (PGCBCTL2)—Offset 430h	54h
450h	453h	Equalization Configuration 1 (EQCFG1)—Offset 450h	3102h
454h	457h	Remote Transmitter Preset Coefficient List 1 (RTPCL1)—Offset 454h	0h
458h	45Bh	Remote Transmitter Preset Coefficient List 2 (RTPCL2)—Offset 458h	0h
45Ch	45Fh	Remote Transmitter Preset Coefficient List 3 (RTPCL3)—Offset 45Ch	0h
460h	463h	Remote Transmitter Preset Coefficient List 4 (RTPCL4)—Offset 460h	0h
464h	467h	Figure Of Merit Status (FOMS)—Offset 464h	0h
468h	46Bh	Hardware Autonomous Equalization Control (HAEQ)—Offset 468h	A0080E00h
470h	473h	Local Transmitter Coefficient Override 1 (LTCO1)—Offset 470h	0h
474h	477h	Local Transmitter Coefficient Override 2 (LTCO2)—Offset 474h	0h
478h	47Bh	GEN3 L0s Control (G3L0SCTL)—Offset 478h	C00281Eh
47Ch	47Fh	Equalization Configuration 2 (EQCFG2)—Offset 47Ch	A001h
480h	483h	Monitor Mux (MM)—Offset 480h	0h
500h	503h	Lane0 P0 and P1 Preset-Coefficient Mapping (L0P0P1PCM)—Offset 500h	0h
504h	507h	Lane0 P1, P2 and P3 Preset-Coefficient Mapping (L0P1P2P3PCM)—Offset 504h	0h
508h	50Bh	Lane0 P3 and P4 Preset-Coefficient Mapping (L0P3P4PCM)—Offset 508h	0h
50Ch	50Fh	Lane0 P5 and P6 Preset-Coefficient Mapping (L0P5P6PCM)—Offset 50Ch	0h
510h	513h	Lane0 P6, P7 and P8 Preset-Coefficient Mapping (L0P6P7P8PCM)—Offset 510h	0h
514h	517h	Lane0 P8 and P9 Preset-Coefficient Mapping (L0P8P9PCM)—Offset 514h	0h
518h	51Bh	Lane0 P10 Preset-Coefficient Mapping (L0P10PCM)—Offset 518h	0h
51Ch	51Fh	Lane0 LF and FS (L0LFFS)—Offset 51Ch	0h
520h	523h	Lane1 P0 and P1 Preset-Coefficient Mapping (L1P0P1PCM)—Offset 520h	0h
524h	527h	Lane1 P1, P2 and P3 Preset-Coefficient Mapping (L1P1P2P3PCM)—Offset 524h	0h
528h	52Bh	Lane1 P3 and P4 Preset-Coefficient Mapping (L1P3P4PCM)—Offset 528h	0h
52Ch	52Fh	Lane1 P5 and P6 Preset-Coefficient Mapping (L1P5P6PCM)—Offset 52Ch	0h
530h	533h	Lane1 P6, P7 and P8 Preset-Coefficient Mapping (L1P6P7P8PCM)—Offset 530h	0h

Table 17-1. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
534h	537h	Lane1 P8 and P9 Preset-Coefficient Mapping (L1P8P9PCM)—Offset 534h	0h
538h	53Bh	Lane1 P10 Preset-Coefficient Mapping (L1P10PCM)—Offset 538h	0h
53Ch	53Fh	Lane1 LF and FS (L1LFFS)—Offset 53Ch	0h
540h	543h	Lane2 P0 and P1 Preset-Coefficient Mapping (L2P0P1PCM)—Offset 540h	0h
544h	547h	Lane2 P1, P2 and P3 Preset-Coefficient Mapping (L2P1P2P3PCM)—Offset 544h	0h
548h	54Bh	Lane2 P3 and P4 Preset-Coefficient Mapping (L2P3P4PCM)—Offset 548h	0h
54Ch	54Fh	Lane2 P5 and P6 Preset-Coefficient Mapping (L2P5P6PCM)—Offset 54Ch	0h
550h	553h	Lane2 P6, P7 and P8 Preset-Coefficient Mapping (L2P6P7P8PCM)—Offset 550h	0h
554h	557h	Lane2 P8 and P9 Preset-Coefficient Mapping (L2P8P9PCM)—Offset 554h	0h
558h	55Bh	Lane2 P10 Preset-Coefficient Mapping (L2P10PCM)—Offset 558h	0h
55Ch	55Fh	Lane2 LF and FS (L2LFFS)—Offset 55Ch	0h
560h	563h	Lane3 P0 and P1 Preset-Coefficient Mapping (L3P0P1PCM)—Offset 560h	0h
564h	567h	Lane3 P1, P2 and P3 Preset-Coefficient Mapping (L3P1P2P3PCM)—Offset 564h	0h
568h	56Bh	Lane3 P3 and P4 Preset-Coefficient Mapping (L3P3P4PCM)—Offset 568h	0h
56Ch	56Fh	Lane3 P5 and P6 Preset-Coefficient Mapping (L3P5P6PCM)—Offset 56Ch	0h
570h	573h	Lane3 P6, P7 and P8 Preset-Coefficient Mapping (L3P6P7P8PCM)—Offset 570h	0h
574h	577h	Lane3 P8 and P9 Preset-Coefficient Mapping (L3P8P9PCM)—Offset 574h	0h
578h	57Bh	Lane3 P10 Preset-Coefficient Mapping (L3P10PCM)—Offset 578h	0h
57Ch	57Fh	Lane3 LF and FS (L3LFFS)—Offset 57Ch	0h
1010h		PCLKD_L1TREF_CFG—Offset 1010h	0h

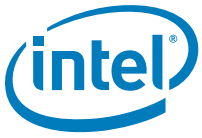
17.1.1 Device Command; Primary Status (CMD_PSPCLKD_L1TREF_CFG—Offset 1010hTS)—Offset 4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**DPE - Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if CMD.PERE is not set.
30	0h RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic.



Bit Range	Default & Access	Field Name (ID): Description
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
26:25	0h RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved per PCI-Express spec
24	0h RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and CMD.PERE is set.
23	0h RO	**Primary Fast Back to Back Capable (PFBC):** Reserved per PCI-Express spec.
22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Primary 66 MHz Capable (PC66):** Reserved per PCI-Express spec.
20	1h RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list.
19	0h RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID.
18:16	0h RO	**Reserved (RSVD_1):** Reserved
15:11	0h RO	**Reserved (RSVD_2):** Reserved
10	0h RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec.
8	0h RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec.
6	0h RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** Reserved per PCI-Express spec.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec.
3	0h RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec.
2	0h RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0h RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0h RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone..

17.1.2 Revision ID;Class Code (RID_CC)—Offset 8h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 60400F0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	6h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	4h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO/V	**Programming Interface (PI):** The value reported in this register is a function of the Decode Control.Subtractive Decode Enable (SDE) register. SDE Value reported in this register 0: 00h 1: 01h
7:0	F0h RO/V	**Revision ID (RID):** Indicates the revision of the bridge.

17.1.3 Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 810000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved
23	1h RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device.
22:16	1h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h.
15:11	0h RO	**Latency Count (CT):** Reserved per PCI-Express spec
10:8	0h RO	**Reserved (RSVD_1):** Reserved
7:0	0h RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec

17.1.4 Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V2	**Secodary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	0h RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.
15:8	0h RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port.
7:0	0h RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

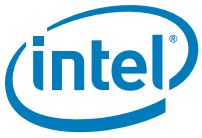
17.1.5 I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
30	0h RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with 'Unsupported Request' status from the device.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with 'Completion Abort' status from the device.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with 'Completion Abort' status to the device.
26:25	0h RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.



Bit Range	Default & Access	Field Name (ID): Description
23	0h RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec
20:16	0h RO	**Reserved (RSVD_1):** Reserved
15:12	0h RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing.

17.1.6 Memory Base and Limit (MBL)—Offset 20h

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is MB [gt]= AD[lb]31:20[rb] [lt]= ML.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	0h RO	**Reserved (RSVD):** Reserved
15:4	0h RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RO	**Reserved (RSVD_1):** Reserved

17.1.7 Prefetchable Memory Base and Limit (PMBL)—Offset 24h

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB [gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 10001h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing.
15:4	0h RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	1h RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing.

17.1.8 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

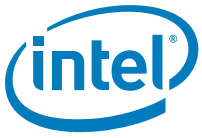
Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.



17.1.9 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

17.1.10 Capabilities List Pointer (CAPP)—Offset 34h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 40h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved
7:0	40h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) OffsetCapability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI) 90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List OffsetCapability Next Pointer 100h Advanced Error Reporting 000h

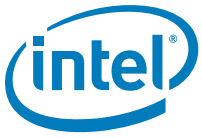
17.1.11 Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD):** Reserved
27	0h RW/V2	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
26	0h RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set.
25	0h RW/V2	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
24	0h RW/V2	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
23	0h RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec.
22	0h RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port.
21	0h RW/V2	**Master Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
20	0h RW	**VGA 16-Bit Decode (V16):** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.
19	0h RW	**VGA Enable (VE):** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h 3BBh and 3C0h 3DFh, and all aliases of bits 15:10 in any combination of 1's



Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
17	0h RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
16	0h RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.
15:8	0h RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG register in chipset config space: Port Bits[lb]15:12[rb] Bits[lb]11:08[rb] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP 4 0h STRPFUSECFG.P4IP 5 0h STRPFUSECFG.P5IP 6 0h STRPFUSECFG.P6IP 7 0h STRPFUSECFG.P7IP 8 0h STRPFUSECFG.P8IP The value that is programmed into STRPFUSECFG.PxIP is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above.
7:0	0h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

17.1.12 Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 428010h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved
30	0h RO	**Reserved (RSVD_1):** Reserved. This register at one time was for TCS Routing but that was later removed from the PCIe 2.0 spec
29:25	0h RO	**Interrupt Message Number (IMN):** The root port does not have multiple MSI interrupt numbers.
24	0h RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
23:20	4h RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port
19:16	2h RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 specification which incorporates the Register Expansion ECN.
15:8	80h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h RO	**Capability ID (CID):** Indicates this is a PCI Express capability

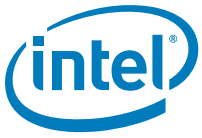
17.1.13 Device Capabilities (DCAP)—Offset 44h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 8001h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD):** Reserved
28	0h RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports
27:26	0h RO	**Captured Slot Power Limit Scale (CSPS):** Not supported
25:18	0h RO	**Captured Slot Power Limit Value (CSPV):** Not supported
17:16	0h RO	**Reserved (RSVD_1):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
15	1h RO	**Role Based Error Reporting (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.
14	0h RO	**Reserved (RSVD_2):** Reserved. On previous version of the specification this was Power Indicator Present (PIP)
13	0h RO	**Reserved (RSVD_3):** Reserved. On previous version of the specification this was Attention Indicator Present (AIP)
12	0h RO	**Reserved (RSVD_4):** Reserved. On previous version of the specification this was Attention Button Present (ABP)
11:9	0h RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports.
8:6	0h RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port.
5	0h RO	**Extended Tag Field Supported (ETFS):** The root port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	0h RO	**Phantom Functions Supported (PFS):** No phantom functions supported
2:0	1h RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Only Max Payload Size of up to 256B is supported. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface.

17.1.14 Device Control; Device Status (DCTL_DSTS)—Offset 48h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
20	1h RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup
19	0h RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
18	0h RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp
17	0h RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout
16	0h RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout.
15	0h RO	**Reserved (RSVD_1):** Reserved
14:12	0h RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface.
11	0h RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.
10	0h RW/P	**Aux Power PM Enable (APME):** The OS will set this bit to '1' if the device connected has detected aux power.
9	0h RO	**Phantom Functions Enable (PFE):** Not supported
8	0h RO	**Extended Tag Field Enable (ETFE):** Not supported

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RW	**Max Payload Size (MPS):** The root port only supports up to 256B max payload. Programming this field to any values other than 128B or 256B max payload size will result in aliasing to 128B max payload size. If the DCAP.MPS indicates 128B max payload size support, programming this field to any values other than 128B will result in aliasing to 128B max payload size. Programming this field to any values greater than DCAP.MPS will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME.
4	0h RO	**Enable Relaxed Ordering (ERO):** Not supported
3	0h RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0h RW	**Fatal Error Reporting Enable (FEE):** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0h RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0h RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

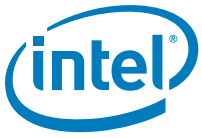
17.1.15 Link Capabilities (LCAP)—Offset 4Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 710C00h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h
23	0h RO	**Reserved (RSVD):** Reserved
22	1h RW/O	**ASPM Optionality Compliance (ASPMOC):** ASPM Optionality Compliance(ASPMOC): This bit must be set to 1b for PCIe 3.0 compliant port. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests.
21	1h RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1h RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0h RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the root port does not support Surprise Down Error Reporting
18	0h RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism.
17:15	2h RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b Less than 1 us 001b 1 us to less than 2 us 010b 2 us to less than 4 us 011b 4 us to less than 8 us 100b 8 us to less than 16 us 101b 16 us to less than 32 us 110b 32 us to 64 us 111b More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency.



Bit Range	Default & Access	Field Name (ID): Description
14:12	0h RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL
11:10	3h RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 No ASPM Supported 01 L0s Supported 10 L1 Supported 11 L0s and L1 supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is '01'. Otherwise, the default of this field is '11'. If STRPFUSECFG.ASPMDIS is 1, BIOS writing '11' to this field will have the same effect as writing '01'. '01' will be reflected on this register when read and the register will turn to Read-Only once written once.
9:4	0h RO/V	**Maximum Link Width (MLW):** For the root ports, several values can be taken, based upon the value of the chipset configuration register field RPC.PC1 for ports 1-4: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RO/V	**Max Link Speeds (MLS):** Indicates the supported link speeds of the Root Port. 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5GT/s Link speeds supported This register reports a value of 0001b if the Root Port Gen2 Disable Fuse is set or the MPC.PCIEGEN2DIS bit is set, else this register reports a value of 0010b. Max Link Speeds (MLS): This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. This register reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through Fuse or MPC.PCIESD register. This register reports a value of 0010b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through Fuse or MPC.PCIESD register.

17.1.16 Link Control; Link Status (LCTL_LSTS)—Offset 50h

Access Method

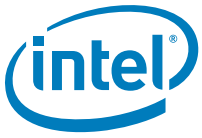
Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
29	0h RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.
28	0h RO/V	**Slot Clock Configuration (SCC):** In normal mode, root port uses the same reference clock as on the platform and does not generate its own clock. Note: The default of this register bit is dependent on the 'PCIe Non-Common Clock With SSC Mode Enable Strap'. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'.
27	0h RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
26	0h RO	**Reserved (RSVD):** Reserved. Previously this was defined as Link Training Error (LTE) but support for this bit was removed from subsequent versions of the PCI Express specification.
25:20	0h RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained.

Bit Range	Default & Access	Field Name (ID): Description
19:16	1h RO/V	**Current Link Speed (CLS):** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link This field indicates the negotiated Link speed of the given link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. The value of this field is undefined if the link is not up.
15:12	0h RO	**Reserved (RSVD_1):** Reserved
11	0h RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.
10	0h RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.
9	0h RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. Note: When operating as PCI Express, this bit defines the value of the Link Upconfigure Capability in TS2 Ordered Sets.
8	0h RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on Root Ports.
7	0h RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. Note: This functionality is not applicable for Mobile Express.
6	0h RW	**Common Clock Configuration (CCC):** When set, indicates that the root port and device are operating with a distributed common reference clock.



Bit Range	Default & Access	Field Name (ID): Description
5	0h WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0h RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state.
3	0h RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0h RO	**Reserved (RSVD_2):** Reserved
1:0	0h RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see '00' as an output from this register. BIOS reading this register should always return the correct value.

17.1.17 Slot Capabilities (SLCAP)—Offset 54h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 40060h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/O	**Physical Slot Number (PSN__31_24):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
23:19	0h RW/O	**Physical Slot Number (PSN__23_19):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.

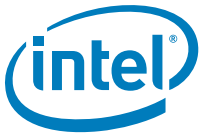
Bit Range	Default & Access	Field Name (ID): Description
18	1h RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0h RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented.
16:15	0h RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:8	0h RW/O	**Slot Power Limit Value (SLV__14_8):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
7	0h RW/O	**Slot Power Limit Value (SLV__7_7):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1h RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported.
5	1h RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification.
4	0h RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot.
3	0h RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot.
2	0h RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present
1	0h RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot
0	0h RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot.

17.1.18 Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved (RSVD):** Reserved
24	0h RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
23	0h RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock.
22	0h RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'.
21	0h RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented.
20	0h RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller..
19	0h RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the SLSTS.PDS bit changes state.
18	0h RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented.
17	0h RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented.
16	0h RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button
15:13	0h RO	**Reserved (RSVD_1):** Reserved
12	0h RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed
11	0h RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock.
10	0h RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug.
9:8	0h RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller..
7:6	0h RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller..
5	0h RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0h RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller..

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state.
2	0h RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller..
1	0h RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller...
0	0h RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller..

17.1.19 Root Control (RCTL)—Offset 5Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:4	0h RO	**Reserved (RSVD_1):** Reserved
3	0h RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set).
2	0h RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0h RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0h RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

17.1.20 Root Status (RSTS)—Offset 60h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17	0h RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. Root ports have a one deep PME pending queue.
16	0h RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0h RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

17.1.21 Device Capabilities 2 (DCAP2)—Offset 64h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 80837h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved (RSVD):** Reserved
19:18	2h RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported.
17:12	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/ disable the root port from declaring support for the LTR capability.
10:6	0h RO	**Reserved (RSVD_2):** Reserved
5	1h RO	**ARI Forwarding Supported (AFS):** ARI Forwarding Supported (AFS): Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. Note: This bit is not made RWO to simplify implementation, since there is a requirement that the ARI Forwarding Enable bit must be hardwired to 0b if ARI Forwarding Supported bit is 0b. It is low risk to keep this risk 1b.
4	1h RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	7h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C 0111b Ranges A, B [amp] C [lt]-- This is what PCH supports 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved.

17.1.22 Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15	0h RO	**Reserved (RSVD_1):** Reserved
14:13	0h RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** 00b Disable OBFF mechanism. 01b Enable OBFF mechanism using Message signaling (Variation A). 10b Enable OBFF mechanism using Message signaling (Variation B). 11b Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect.
12:11	0h RO	**Reserved (RSVD_2):** Reserved
10	0h RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:6	0h RO	**Reserved (RSVD_3):** Reserved
5	0h RW	**ARI Forwarding Enable (AFE):** ARI Forwarding Enable (AFE): When set, the Downstream Port disables its traditional Device Number field being 0b enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port.
4	0h RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The root port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 us to 100 us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either when this value was changed or when each request was issued.

17.1.23 Link Capabilities 2 (LCAP2)—Offset 6Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved (RSVD):** Reserved
22:16	0h RO	**Lower SKP OS Reception Supported Speeds Vector (LSOSRSS):** Lower SKP OS Reception Supported Speeds Vector(LSOSRSS): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
15:9	0h RO	**Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV):** Lower SKP OS Generation Supported Speeds Vector(LSOSGSSV): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
8	0h RO	**Crosslink Supported (CS):** Crosslink Supported (CS): No support for Crosslink.
7:1	0h RO/V	**Supported Link Speeds Vector (SLSV):** Supported Link Speeds Vector (SLSV): This field indicates the supported Link speed of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. Bit definitions within this field are: Bit 0: 2.5 GT/s. Bit 1: 5.0 GT/s. Bit 2: 8.0 GT/s. Bits 6:3: Reserved. This register reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through Fuse or MPC.PCIESD register. This register reports a value of 0011b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through Fuse or MPC.PCIESD register.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**Reserved (RSVD_1):** Reserved

17.1.24 Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h

Access Method

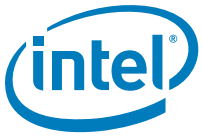
Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/1C/V/P	**Link Equalization Request (LER):** Link Equalization Request (LER): This bit is set by hardware to request the Link equalization process to be performed on the Link. Register Attribute: Dynamic.
20	0h RO/V/P	**Equalization Phase 3 Successful (EQP3S):** Equalization Phase 3 Successful (EQP3S): When set to 1, this bit indicates that Phase 3 of the Transmitter Equalization procedure has successfully completed.
19	0h RO/V/P	**Equalization Phase 2 Successful (EQP2S):** Equalization Phase 2 Successful (EQP2S): When set to 1, this bit indicates that Phase 2 of the Transmitter Equalization procedure has successfully completed.
18	0h RO/V/P	**Equalization Phase 1 Successful (EQP1S):** Equalization Phase 1 Successful (EQP1S): When set to 1, this bit indicates that Phase 1 of the Transmitter Equalization procedure has successfully completed.
17	0h RO/V/P	**Equalization Complete (EqC):** Equalization Complete (EC): When set to 1, this bit indicates that the Transmitter Equalization procedure has completed
16	0h RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/P	**Compliance Preset/De-emphasis (CD):** For 8.0 GT/s Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b -3.5 dB 0000b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. The default value of this field is 0000b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value.
11	0h RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only.
10	0h RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.

Bit Range	Default & Access	Field Name (ID): Description
9:7	0h RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate. Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0h RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5	0h RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds.



Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value.
3:0	0h RW/V/P	**Target Link Speed (TLS):** Target Link Speed (TLS): This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. If a value is written to this field that does not correspond to a supported speed, as indicated by the Supported Link Speeds Vector, the result is undefined. The default value of this field is GEN1. Note: This register field could be used by REUT software to limit the link speed to 2.5 GT/s or 5 GT/s data rate.

17.1.25 Slot Capabilities 2 (SLCAP2)—Offset 74h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved (RSVD):** Reserved

17.1.26 Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:0	0h RO	**Reserved (RSVD_1):** Reserved

17.1.27 Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 9005h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved
23	0h RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
22:20	0h RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
19:17	0h RO	**Multiple Message Capable (MMC):** Only one message is required.
16	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.

Bit Range	Default & Access	Field Name (ID): Description
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	5h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

17.1.28 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction.

17.1.29 Subsystem Vendor Capability (SVCAP)—Offset 90h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: A00Dh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

17.1.30 Subsystem Vendor IDs (SVID)—Offset 94h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

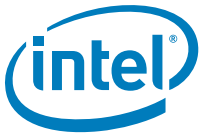
17.1.31 Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: C8030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	19h RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Microsoft operating systems to enable PME# in devices connected behind this root port.
26	0h RO	**D2_Support (D2S):** The D2 state is not supported.
25	0h RO	**D1_Support (D1S):** The D1 state is not supported.
24:22	0h RO	**Aux_Current (AC):** Reports 0mA (self-powered), as use of this controller does not add to suspect well power consumption.
21	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
20	0h RO	**Reserved (RSVD):** Reserved
19	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
18:16	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	1h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

17.1.32 PCI Power Management Control And Status (PMCS)—Offset A4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Data (DTA):** Reserved
23	0h RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification
22	0h RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification.
21:16	0h RO	**Reserved (RSVD):** Reserved
15	0h RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0h RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Microsoft operating systems to enable PME# on devices connected to this root port.
7:4	0h RO	**Reserved (RSVD_1):** Reserved
3	1h RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved (RSVD_2):** Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 D0 state 11 D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

17.1.33 Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h

Size:32 bits
The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list.
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

17.1.34 Uncorrectable Error Status (UES)—Offset 104h

This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/1C/V/P	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0h RW/1C/V/P	**Completor Abort Status (CA):** Indicates a completer abort was received

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Not supported.
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RO	**Training Error Status (TE):** Not supported.

17.1.35 Uncorrectable Error Mask (UEM)—Offset 108h

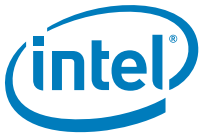
When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/P	**ACS Violation Mask (AVM):** Reserved. Access Control Services are not supported
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.



Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0h RW/P	**Completor Abort Mask (CM):** Mask for completer abort.
14	0h RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.
13	0h RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RO	**Training Error Mask (TE):** Not supported.

17.1.36 Uncorrectable Error Severity (UEV)—Offset 10Ch

This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 60011h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/P	**ACS Violation Severity (AVS):** Severity for ACS violation.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	1h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.

Bit Range	Default & Access	Field Name (ID): Description
17	1h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0h RW/P	**Completor Abort Severity (CA):** Severity for completer abort.
14	0h RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	1h RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation..

17.1.37 Correctable Error Status (CES)—Offset 110h

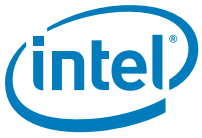
This register is only reset by a loss of core power

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved (RSVD):** Reserved
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	**Reserved (RSVD_1):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

17.1.38 Correctable Error Mask (CEM)—Offset 114h

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved (RSVD):** Reserved
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	**Reserved (RSVD_1):** Reserved
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.

Bit Range	Default & Access	Field Name (ID): Description
5:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

17.1.39 Advanced Error Capabilities and Control (AECC)—Offset 118h

This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved (RSVD):** Reserved
8	0h RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0h RO	**ECRC Check Capable (ECC):** ECRC is not supported.
6	0h RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0h RO	**ECRC Generation Capabile (EGC):** ECRC is not supported.
4:0	0h RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

17.1.40 Header Log DW1 (HL_DW1)—Offset 11Ch

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**1st dWord of TLP (DW1):** Byte0 [amp][amp] Byte1 [amp][amp] Byte2 [amp][amp] Byte3

17.1.41 Header Log DW2 (HL_DW2)—Offset 120h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**2nd dWord of TLP (DW2):** Byte4 [amp][amp] Byte5 [amp][amp] Byte6 [amp][amp] Byte7

17.1.42 Header Log DW3 (HL_DW3)—Offset 124h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**3rd dWord of TLP (DW3):** Byte8 [amp][amp] Byte9 [amp][amp] Byte10 [amp][amp] Byte11

17.1.43 Header Log DW4 (HL_DW4)—Offset 128h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**4th dWord of TLP (DW4):** Byte12 [amp][amp] Byte13 [amp][amp] Byte14 [amp][amp] Byte15

17.1.44 Root Error Command (REC)—Offset 12Ch

This register allows errors to generate interrupts.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved (RSVD):** Reserved
2	0h RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0h RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0h RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

17.1.45 Error Source Identification (ESID)—Offset 134h

Size:32 bits
Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set.
15:0	0h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set.

17.1.46 ACS Extended Capability Header (ACSECH)—Offset 140h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support ACS Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support ACS Extended Capability, BIOS should write a 000Dh to this register else it should write 0.

17.1.47 ACS Capability Register (ACSCAPR)—Offset 144h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: Fh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD_1):** Reserved for Egress Control Vector Size. This field is not applicable since ACS P2P Egress Control is not supported.
7	0h RO	**Reserved (RSVD_2):** Reserved
6	0h RO	**ACS Direct Translated P2P (T):** ACS Direct Translated P2P (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control (E):** ACS P2P Egress Control (E): ACS P2P Egress Control is not supported.
4	0h RO	**ACS Upstream Forwarding (U):** ACS Upstream Forwarding (U): ACS Upstream Forwarding is not supported.
3	1h RW/O	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Required for all Functions that support ACS P2P Request Redirect; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Completion Redirect.
2	1h RW/O	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Required for Root Ports that support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports; required for multi-function device Functions that support peer-to-peer traffic with other Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Request Redirect.
1	1h RW/O	**ACS Translation Blocking (B):** ACS Translation Blocking (B): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Translation Blocking.
0	1h RW/O	**ACS Source Validation (V):** ACS Source Validation (V): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Source Validation.

17.1.48 ACS Control Register (ACSCTLR)—Offset 148h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RSVD):** Reserved,
6	0h RO	**ACS Direct Translated P2P Enable (T):** ACS Direct Translated P2P Enable (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control Enable (E):** ACS P2P Egress Control Enable (E): ACS P2P Egress Control is not supported.
4	0h RO	**ACS Upstream Forwarding Enable (U):** ACS Upstream Forwarding Enable (U): ACS Upstream Forwarding is not supported.
3	0h RW	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Determines when the component redirects peer-to-peer Completions upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear.
2	0h RW	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Determines when the component redirects peer-to-peer memory Requests targeting another peer port upstream. I/O, Configuration, VDM Messages and Completions are never affected by ACS P2P Request Redirect.
1	0h RW	**ACS Translation Blocking (B):** ACS Translation Blocking (B): When set, the component blocks all upstream Memory Requests whose Address Translation (AT) field is not set to the default value. I/O, Configuration, Completions and Messages are never affected by ACS Translation Blocking.
0	0h RW	**ACS Source Validation (V):** ACS Source Validation (V): When set, the component validates the Bus Number from the Requester ID of upstream Requests against the secondary / subordinate Bus Numbers. I/O, Configuration and Completions are never affected by ACS Source Validation.

17.1.49 PTM Extended Capability Header (PTMECH)—Offset 150h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support PTM Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support PTM Extended Capability, BIOS should write a 001Fh to this register else it should write 0.

17.1.50 PTM Capability Register (PTMCAPR)—Offset 154h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 400h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved,
15:8	4h RW/O	**Local Clock Granularity (LCG):** Local Clock Granularity(LCG): 0000 0000b - Time Source does not implement a local clock. It simply propagates timing information obtained from further Upstream in the PTM Hierarchy when responding to PTM Request messages. 0000 0001b - 1111 1110b: Indicates the period of this Time Sources local clock in ns. 1111 1111b: Indicates the period of this Time Sources local clock is greater than 254 ns. If the PTM Root Select bit is Set, this local clock is used to provide PTM Master Time. Otherwise, the Time Source uses this local clock to locally track PTM Master Time received from further Upstream within a PTM Hierarchy.
7:3	0h RO	**Reserved (RSVD_1):** Reserved,
2	0h RW/O	**PTM Root Capable (PTMRC):** PTM Root Capable(PTMRC): Root Ports must set this bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW/O	**PTM Responder Capable (PTMRSPC):** PTM Responder Capable(PTMRSPC): Root Ports are permitted to set this bit to 1b to indicate that they implement the PTM Responder role.
0	0h RO	**PTM Requester Capable (PTMREQC):** PTM Requester Capable(PTMREQC): PTM Requester Role is not supported by Root Port.

17.1.51 PTM Control Register (PTMCTLR)—Offset 158h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:8	0h RO	**Effective Granularity (EG):** Effective Granularity(EG): Root Port does not support PTM Requester role.
7:2	0h RO	**Reserved (RSVD_1):** Reserved.
1	0h RW	**Root Select (RS):** Root Select(RS): When Set, if the PTM Enable bit is also Set, this Time Source is the PTM Root. Within each PTM Hierarchy, it is recommended that system software select only the furthest Upstream Time Source to be the PTM Root.
0	0h RW	**PTM Enable (PTME):** PTM Enable(PTME): When Set, this Function is permitted to participate in the PTM mechanism according to its selected role. Software must not have the PTM Enable bit Set in the PTM Control register on a Function associated with an Upstream Port unless the associated Downstream Port on the Link already has the PTM Enable bit Set in its associated PTM Control register. Register Attribute: Static.

17.1.52 L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h

Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 1h
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 001Eh. .

17.1.53 L1 Sub-States Capabilities (L1SCAP)—Offset 204h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 28281Fh

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
23:19	5h RW/O	**Port Tpower_on Value (PTV):** Along with the Port T_POWER_ON Scale Field in the L1 Substates Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF.
18	0h RO	**Reserved (RSVD_1):** Reserved.
17:16	0h RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Substates Capabilities register. '00b': 2 us '01b': 10 us '10b': 100 us '11b': Reserved Required for all Ports that support L1.OFF.
15:8	28h RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF.
7:5	0h RO	**Reserved (RSVD_2):** Reserved
4	1h RW/O	**L1 PM Substates Supported (L1PSS):** When Set this bit indicates that this Port supports L1 PM Substates. For compatibility with possible future extensions, software must not enable L1 PM Substates unless this bit is set. This RWO field must be programmed prior to enabling ASPM.
3	1h RW/O	**ASPM L1.1 Substates Supported (AL11S):** When set, this bit indicates that this port supports L1 substates for ASPM L1.SNOOZ. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
2	1h RW/O	**ASPM L1.2 Supported (AL12S):** When set, this bit indicates that ASPM_L1.OFF is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
1	1h RW/O	**PCI-PM L1.1 Supported (PPL11S):** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

Bit Range	Default & Access	Field Name (ID): Description
0	1h RW/O	**PCI-PM L1.2 Supported (PPL12S):** When set, this bit indicates that L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

17.1.54 L1 Sub-States Control 1 (L1SCTL1)—Offset 208h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**L1.2 LTR Threshold Latency ScaleValue (L12LTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe root port. The value in this field, together with L12LTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L12LTRSTLV times 1 ns 001: L12LTRSTLV times 32 ns 010: L12LTRSTLV times 1024 ns 011: L12LTRSTLV times 32768 ns 100: L12LTRSTLV times 1048576 ns 101: L12LTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
28:26	0h RO	**Reserved (RSVD):** Reserved
25:16	0h RW	**L1.2 LTR Threshold Latency Value (L12OFFLTRTLV):** This field contains the L1.2 LTR Threshold Latency Value for this particular PCIe root port. The value in this field, together with L12LTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
15:8	0h RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time the PCIe root port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved (RSVD_1):** Reserved
3	0h RW	**ASPM L1.1 Enabled (AL11E):** When set, this bit indicates that ASPM L1.SNOOZ substates are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic
2	0h RW	**ASPM L1.2 Enable (AL12E):** When set, this bit indicates that ASPM L1.OFF substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic
1	0h RW	**PCI-PM L1.SNOOZ Enable (PPL11E):** When set, this bit indicates that PCI-PM L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
0	0h RW	**PCI-PM L1.2 Enabled (PPL12E):** When set, this bit indicates that PCI-PM L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.

17.1.55 L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 28h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:3	5h RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# is sampled asserts in L1.OFF state. Tpower_on value is calculated by multiplying the value in this field by the value in the TPOS field. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
2	0h RO	**Reserved (RSVD_1):** Reserved
1:0	0h RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. '00b': 2 us '01b': 10 us '10b': 100us '11b': Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static

17.1.56 Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h

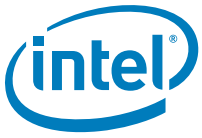
Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.



Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEECID):** PCI Express Extended Capability ID (PCIEECID): This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 0019h to this register else it should write 0.

17.1.57 Link Control 3 (LCTL3)—Offset 224h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:9	0h RO	**Enable Lower SKP OS Generation Vector (ELSOSGV):** Enable Lower SKP OS Generation Vector(ELSOSGV): When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is Set in this field and the corresponding bit in the Lower SKP OS Generation Supported Speeds Vector is not set.
8:2	0h RO	**Reserved (RSVD_1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Link Equalization Request Interrupt Enable (LERIE):** Link Equalization Request Interrupt Enable (LERIE): When set, this bit enables the generation of an interrupt to indicate that the Link Equalization Request bit has been set.
0	0h RW	**Perform Equalization (PE):** Perform Equalization (PE): When this bit is 1b and Link Retrain bit is set with the Target Link Speed field set to 8 GT/s, the Downstream Port must perform Link Equalization. This bit is cleared by Root Port upon entry to Link Equalization

17.1.58 Lane Error Status (LES)—Offset 228h

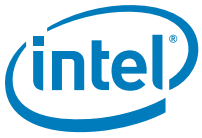
The Lane number is the default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD):** Reserved
3	0h RW/1C/V/P	**Lane 3 Error Status (L3ES):** Lane 3 Error Status (L3ES): Lane 3 detected a Lane-based error.
2	0h RW/1C/V/P	**Lane 2 Error Status (L2ES):** Lane 2 Error Status (L2ES): Lane 2 detected a Lane-based error.
1	0h RW/1C/V/P	**Lane 1 Error Status (L1ES):** Lane 1 Error Status (L1ES): Lane 1 detected a Lane-based error.
0	0h RW/1C/V/P	**Lane 0 Error Status (L0ES):** Lane 0 Error Status (L0ES): Lane 0 detected a Lane-based error.



17.1.59 Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 7F7F7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved.
30:28	7h RW	**Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH):** Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 1 Transmitter Preset (UPL1TP):** Upstream Port Lane 1 Transmitter Preset (UPL1TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	**Reserved (RSVD_1):** Reserved.
22:20	7h RW	**Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH):** Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 1 Transmitter Preset (DPL1TP):** Downstream Port Lane 1 Transmitter Preset (DPL1TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved (RSVD_2):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
14:12	7h RW	**Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH):** Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 0 Transmitter Preset (UPL0TP):** Upstream Port Lane 0 Transmitter Preset (UPL0TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	**Reserved (RSVD_3):** Reserved.
6:4	7h RW	**Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH):** Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 0 Transmitter Preset (DPL0TP):** Downstream Port Lane 0 Transmitter Preset (DPL0TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

17.1.60 Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 7F7F7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
30:28	7h RW	**Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH):** Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 3 Transmitter Preset (UPL3TP):** Upstream Port Lane 3 Transmitter Preset (UPL3TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	**Reserved (RSVD_1):** Reserved
22:20	7h RW	**Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH):** Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 3 Transmitter Preset (DPL3TP):** Downstream Port Lane 3 Transmitter Preset (DPL3TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved (RSVD_2):** Reserved
14:12	7h RW	**Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH):** Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 2 Transmitter Preset (UPL2TP):** Upstream Port Lane 2 Transmitter Preset (UPL2TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	**Reserved (RSVD_3):** Reserved
6:4	7h RW	**Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH):** Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
3:0	Fh RW	**Downstream Port Lane 2 Transmitter Preset (DPL2TP):** Downstream Port Lane 2 Transmitter Preset (DPL2TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

17.1.61 PCI Express Replay Timer Policy 1 (PCIERTP1)—Offset 300h

The Replay Timer controlled by the Replay Timeout field is started when the Retry Buffer is empty and a TLP is placed into it or an Ack/Nak DLLP is received and there are still non-acknowledged packets within the Retry Buffer. The counter continues to count until the next valid Ack DLLP or a NAK DLLP that acknowledges unacknowledged TLPs is received, or it reaches the timeout value specified by this register. When a valid Ack/Nak DLLP is received, the timer is reset to zero and restarted if there are still non-acknowledged packets within the Retry Buffer. Otherwise if the Retry Buffer is empty, the counter is just reset to zero. If the timer reaches the timeout value, the non-acknowledged packets within the Retry Buffer will be replayed.
The default for this register is dependant on the MAX_PAYLOAD_SIZE , the NEGOTIATED_WIDTH, and the NEGOTIATED_SPEED.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: A64F96h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved,
23:20	Ah RW	**Gen 2 x1 (G2X1):** Gen 2 x1 (G2X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 7) * 64 link clocks. For PCIE Gen 2 speed and x1 width For Mobile Express HS-Gear 3 speed and x1 width.

Bit Range	Default & Access	Field Name (ID): Description
19:16	6h RW	**Gen 2 x2 (G2X2):** Gen 2 x2 (G2X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 4) * 64 link clocks. For PCIe Gen 2 speed and x2 width. For Mobile Express HS-Gear 3 speed and x2 width.
15:12	4h RW	**Gen 2 x4 (G2X4):** Gen 2 x4 (G2X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 2 speed and x4 width. For Mobile Express HS-Gear 3 speed and x4 width.
11:8	Fh RW	**Gen 1 x1 (G1X1):** Gen 1 x1 (G1X1): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 10) * 64 link clocks. For 512B MPS: (nnn + 17) * 64 link clocks. For PCIe Gen 1 speed and x1 width. For Mobile Express HS-Gear 2 speed and x1 width.
7:4	9h RW	**Gen 1 x2 (G1X2):** Gen 1 x2 (G1X2): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For PCIe Gen 1 speed and x2 width. For Mobile Express HS-Gear 2 speed and x2 width.

Bit Range	Default & Access	Field Name (ID): Description
3:0	6h RW	**Gen 1 x4 (G1X4):** Gen 1 x4 (G1X4): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/ Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 1 speed and x4 width. For Mobile Express HS-Gear 2 speed and x4 width.

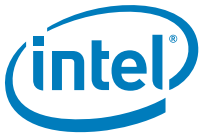
17.1.62 PCI Express Replay Timer Policy 2 (PCIERTP2)—Offset 304h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 1BC00B86h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Lane 0 Lane Number (L0LN):** Lane 0 Lane Number(L0LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 0 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
29:28	1h RW	**Lane 1 Lane Number (L1LN):** Lane 1 Lane Number(L1LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 1 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.



Bit Range	Default & Access	Field Name (ID): Description
27:26	2h RW	**Lane 2 Lane Number (L2LN):** Lane 2 Lane Number(L2LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 2 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
25:24	3h RW	**Lane 3 Lane Number (L3LN):** Lane 3 Lane Number(L3LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 3 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
23	1h RW	**Loopback Master EQ TS1 Enable (LMEQTS1E):** Loopback Master EQ TS1 Enable(LMEQTS1E): When set, the Loopback Master will use EQ TS1 Ordered Sets to direct the Loopback Slave into Loopback from Configuration.Linkwidth.Start. The Preset field of the EQ TS1 Ordered Sets will be specified by Upstream Port Lane X Transmitter Preset and Upstream Port Lane X Receiver Preset Hint fields in the Lane Equalization Control registers.
22	1h RW	**Loopback Master EQ Change Enable (LMEQCE):** Loopback Master EQ Change Enable(LMEQCE): This field is applicable to the case where Loopback is entered from Recovery state. When set, the Loopback Master will set the EC field of the GEN3 TS1 Ordered Sets to the appropriate value based on the ports direction(10b or 11b) to direct the Loopback Slave into Loopback from Recovery state. The Preset field of the GEN3 TS1 Ordered Sets will be specified by Upstream Port Lane X Transmitter Preset and Upstream Port Lane X Receiver Preset Hint fields in the Lane Equalization Control registers.
21:12	0h RO	**Reserved (RSVD):** Reserved
11:8	Bh RW	**Gen 3 x1 (G3X1):** Gen 3 x1 (G3X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For Gen 3 speed and x1 width

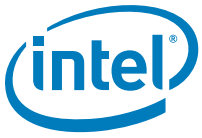
Bit Range	Default & Access	Field Name (ID): Description
7:4	8h RW	**Gen 3 x2 (G3X2):** Gen 3 x2 (G3X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For Gen 3 speed and x2 width
3:0	6h RW	**Gen 3 x4 (G3X4):** Gen 3 x4 (G3X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 1) * 64 link clocks. For 512B MPS: (nnn + 2) * 64 link clocks. For Gen 3 speed and x4 width

17.1.63 PCI Express Status 1 (PCIESTS1)—Offset 328h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LTSM State (LTSMSTATE):** Indicates the LTSM present state. Hex LTSSM States 00 DETIDLE 01 DETRDY 02 DETIDLEP1TOP2 03 DETRDYP2TOP1 04 DETRDYINP1 05 DETRDYINP1EXE 06 DETP2POLLSTART 07 DETP1POLLSTART 08 DETP2TOP0 09 DETP1TOP0 0A ECPCMPRETRAIN 0B ECPCMFAILP0TOP2 0C DETP0TOP2 0D PMODECHANGE 0E ECPCMPCIE 0F ECPCMUSB3 10 DET2POLLINP0 11 POLLINGACTIVE 12 POLLINGCOMPLIANCEMARGINCNT 13 POLLINGCOMPLIANCE 14 POLLINGCOMPLIANCESPEEDUP 15 POLLINGCOMPLIANCESPEEDDN 16 POLLINGCOMPLIANCESPEEDTXEIDLE 17 POLLINGCOMPLIANCESPEEDRXEIDLE 18 POLLINGCOMPLIANCESPEED 19 POLLINGCOMPLIANCESPEEDDONE 1A POLLINGCOMPLIANCEEXIT 1B POLLINGCONFIGURATION 1C POLLINGTXEIDLE 1D POLLINGEND 1E POLLINGENDWAIT 1F LINKWIDTHSTART 20 LINKWIDTHACCEPT 21 LANENUMWAIT 22 LANENUMACCEPT 23 LANEDESKEW 24 CONFIGCOMPLETE 25 CONFIGIDLE 26 LWNEXITRECOVERY 27 CONFIGLPBKENTRY 28 CONFIGLPBKLWSTART 29 CONFIGLPBKSPEEDTXEIDLE 2A CONFIGLPBKSPEEDSTART 2B CONFIGLPBKSPEEDRXEIDLE 2C CONFIGLPBKSPEED 2D CONFIGLPBKREUTSKIP 2E CONFIGLPBKREUT 2F CONFIGLPBKEXITM 30 CONFIGLPBKTXEIDLE

Bit Range	Default & Access	Field Name (ID): Description
		31 LWNEXIT 32 LWNLNK2DETECT 33 L0 34 TXL0SRXL0 35 RXL0STXL0 36 TXL0SRXL0S 37 L1TXEIDLE 38 L1RCVEIDLE 39 L1PREENTRY 3A L1ENTRY 3B L1IDLE 3C L1IDLEGEN2WAIT 3D L1EXIT 3E L2TXEIDLE 3F L2RCVEIDLE 40 L2IDLEWAIT 41 L2IDLERDY 42 L2IDLE 43 LOOPBACKENTRY 44 LPBKACTIVEMTXSKP 45 LPBKACTIVEMSKPDSKW 46 LOOPBACKACTIVEM 47 LPBKSLAVESPEEDTXEIDLE 48 LPBKSLAVESPEEDRXEIDLE 49 LPBKSLAVESPEED 4A LOOPBACKACTIVES 4B LOOPBACKCMMSKP 4C LOOPBACKCMM 4D LOOPBACKEXITM 4E LOOPBACKEXITS 4F LOOPBACKEXITL0 50 LOOPBACKLNK2DETECT 51 LOOPBACK2DETECT 52 DISTX16TS1DIS 53 DISTXEIDLE 54 DISWAITSTART 55 DISWAITGNT 56 DISWAIT4TXMARGIN 57 DISWAIT 58 DIS2DETECT 59 HOTRESETTS1 5A HOTRESETDONE 5B HOTRESETEIDLE 5C RECOVERYRCVRWAIT 5D RECOVERYRCVRMARGINCNT 5E RECOVERYRCVRLOCK 5F RECOVERYDESKEW 60 RECOVERYRCVRCFG 61 RECOVERYSPEED 62 RECOVERYSPEEDTXEIDLE 63 RECOVERYSPEEDRXEIDLE

Bit Range	Default & Access	Field Name (ID): Description
		64 RECOVERYSPEEDREADY 65 RECOVERYIDLE 66 RECOVERYEXITDETECT 67 RECOVERYLNK2DETECT 68 RECOVERYEXITLPBK 69 RECOVERYEXITL0 6A RECOVERYEXITDIS 6B RECOVERYEXITRST ***Note:*** This register field could be used by REUT software to monitor the link LTSSM substates.
23	0h RO	**Reserved (RSVD):** Reserved.
22:19	0h RO/V	**Link Status (LNKSTAT):** During Link initialization the Link will always traverse this list of state from the top (0000) to the bottom of the list (0111). One or more power management states may be skipped, but the direction of list traversal will remain the same. 0000 Link Down 0001 : Link Retrain 0011 : L1 0100 : L2 0101 : L3 0111 : L0 (Link Up) 1000 : L0s (Transmit [amp] Receive) 1001 : L0s (Transmit only) 1010 : L0s (Receive only) All others reserved
18:17	0h RO/V	**Replay Number (REPLAYNUM):** Number of times the Retry Buffer has been replayed since the last Link initialization / re-training. When the Data Link Layer has replayed the contents of the Retry Buffer four times a Link re-training will be initiated which will reset this value back to zero.
16	0h RO/V	**Data Link Layer Retry (DLLRETRY):** Indicates when the Data Link Layer has received a corrupted TLP or has detected a dropped packet and is currently waiting for the remote agent to re-transmit the corrupted/dropped packet. The value of Next Receive Sequence Number will be the sequence number associated with the corrupted packet.
15:12	0h RO/V	**Lane Status (LANESTAT):** Indicates which lanes are trained. A '1' indicates that the corresponding lane is trained (i.e. bit 0 = '1' means lane 0 is trained).
11:0	0h RO/V	**Next Transmitted Sequence Number (NXTTXSEQNUM):** This is the sequence number to be applied to and pre-pended to the next outgoing TLP.

17.1.64 PCI Express Status 2 (PCIESTS2)—Offset 32Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**PCIe Port 3 Non-Common Clock With SSC Mode Enable Strap (P3PNCCWSSCMES):** '0': PCIe port 3 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 3 is enabled to operate in non-common clock mode with SSC enabled.
30	0h RO/V	**PCIe Port 2 Non-Common Clock With SSC Mode Enable Strap (P2PNCCWSSCMES):** '0': PCIe port 2 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 2 is enabled to operate in non-common clock mode with SSC enabled.
29	0h RO/V	**PCIe Port 1 Non-Common Clock With SSC Mode Enable Strap (P1PNCCWSSCMES):** '0': PCIe port 1 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 1 is enabled to operate in non-common clock mode with SSC enabled.
28	0h RO/V	**PCIe Port 0 Non-Common Clock With SSC Mode Enable Strap (P0PNCCWSSCMES):** '0': PCIe port 0 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 0 is enabled to operate in non-common clock mode with SSC enabled.
27:16	0h RO/V	**Next Receive Sequence Number (NXTRCVSEQ):** This is the sequence number associated with the TLP that is expected to be received next.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/1C/V	**Cause of Last Recovery Event (CLRE):** Cause of Last Recovery Event (CLRE): This field logs the cause of the entry to Recovery from L0. Only the first cause of Recovery is captured, until the register is cleared. Encoding Recovery Event 0000 No Recovery. 0001 Recovery entry triggered by remote device. 0010 Link Layer initiated Link Retrain due to error. 0011 De-skew buffer full. 0100 L0s exit time-out. 0101 Elastic Buffer overrun/underrun. 0110 Triggered by speed change. 0111 Link upconfiguration/downconfiguration. 1000 L0 Electrical Idle Inference. 1001 Any of the Link Retrain, CMM Start, Hot Reset, Link Disable, REUT Loopback Master or REUT Forced Loopback Master bit set. 1010 Received EIOS for RXL0s entry when ASPM L0s is disabled. 1011 Entry to Recovery from RXL0s due to PME timeout. Others Reserved.
11:0	0h RO/V	**Last Acknowledged Sequence Number (LASTACKSEQNUM):** This is the sequence number associated with the last acknowledged TLP.

17.1.65 PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h

Note that selecting a lane number that does not exist for a port may result in undefined behavior.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 2A000016h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**GEN3 Intel CMM Scrambler Bypass (G3ICMMSB):** GEN3 Intel CMM Scrambler Bypass(G3ICMMSB): When set, the Intel CMM pattern will bypass scrambling in GEN3. This bit does not impact non Intel CMM pattern. The TSx and SOS prior to Intel CMM will still be scrambled normally. Note: This bit must be set prior to enabling Intel CMM, by setting the PCIECMMPC.START. Note: When operating in Mobile Express mode, this field is not applicable.
30	0h RO	**Reserved (RSVD):** Reserved
29	1h RW	**CMM Symbol[3] Select (SYM3SEL):** 0: selects CMM Symbol [lb]3[rb] to a control character 1: selects CMM Symbol [lb]3[rb] as a data character
28	0h RW	**CMM Symbol[2] Select (SYM2SEL):** 0: selects CMM Symbol [lb]2[rb] to a control character 1: selects CMM Symbol [lb]2[rb] as a data character
27	1h RW	**CMM Symbol[1] Select (SYM1SEL):** 0: selects CMM Symbol [lb]1[rb] to a control character 1: selects CMM Symbol [lb]1[rb] as a data character
26	0h RW	**CMM Symbol[0] Select (SYM0SEL):** 0: selects CMM Symbol [lb]0[rb] to a control character 1: selects CMM Symbol [lb]0[rb] as a data character
25:24	2h RW	**CMM Sync Header (CMMSH):** CMM Sync Header(CMMSH): Specifies the Sync Header for the Intel CMM pattern specified in PCIECMMSB. Note: Due to implementation limitation, only a value of 10b is supported. All the other values are not supported.
23:22	0h RO/V	**CMM Error Lane Number (ERRLANENUM):** This field contains the lane number of the failing lane. Only valid when CMM Error Detected is 1.
21:16	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO/V	**CMM Invert (INVERT):** Indicates which lanes are inverted 000: No inversion 001: Lanes 0 010: Lanes 1 011: Lanes 2 100: Lanes 3 This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated)
12:10	0h RO/V	**CMM Symbol Error Number Invert (SYMERRNUMINV):** Indicates which register number miscompared on the failing lane, if the failing lane was an inverted lane. Only valid when CMM Error Detected is 1. 000: CMM Data D0 001: CMM Data D0 010: CMM Data D0 011: CMM Data D1 100: CMM Data D2 101: CMM Data D3 110: CMM Data D0 111: CMM Data D0
9:8	0h RO/V	**CMM Symbol Error Number (SYMERRNUM):** Indicates which register number miscompared on the failing lane, if the failing lane was not inverted. Only valid when CMM Error Detected is 1. 00: CMM Data 0 01: CMM Data 1 10: CMM Data 2 11: CMM Data 3
7	0h RW/1C/V	**CMM Error Detected (ERRDET):** 1: An error was detected 0: No error detected Note: This bit will be shadowed to an observability pin that can be used for IRQ generation.
6:5	0h RW	**Select Lane Number to be inverted for CMM (SLNINVCMM):** Select Lane Number to be inverted for CMM
4	1h RW	**CMM AutoInvert (AUTOINVERT):** 1: CMM autosequences through the inversion 0: CMM does not sequence inversion
3	0h RO/V	**CMM Status (STAT):** This bit is set when the CMM Start bit is set and cleared when the CMM mode has been entered successfully. 0: Compliance Measurement Mode is not active or CMM mode has been entered successfully. 1: Set as a result of CMM Start bit being set.
2	1h RW	**CMM Invert Enable (INVEN):** 1: Enables the Inversion of the lane 0: Lane not inverted
1	1h RW	**Reserved (RSVD_2):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/L	**CMM Start (START):** 1: Start CMM 0: Stop CMM

17.1.66 PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 4ABCB5BCh

Bit Range	Default & Access	Field Name (ID): Description
31:24	4Ah RW	**CMM Data [3] (DATA3):** This character contains CMM Data [lb]3[rb] that will be transmitted on the link.
23:16	BCh RW	**CMM Data [2] (DATA2):** This character contains CMM Data [lb]2[rb] that will be transmitted on the link.
15:8	B5h RW	**CMM Data [1] (DATA1):** This character contains CMM Data [lb]1[rb] that will be transmitted on the link.
7:0	BCh RW	**CMM Data [0] (DATA0):** This character contains CMM Data [lb]0[rb] that will be transmitted on the link.

17.1.67 PTM Propagation Delay (PTMPD)—Offset 390h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Propagation Delay Value (CPTMPDV):** Current PTM Propagation Delay Value(CPTMPDV): This field reports the current PTM Propagation Delay value captured from the last successful PTM dialog.

17.1.68 PTM Lower Local Master Time (PTMLLMT)—Offset 394h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Lower Local Master Time Value (CPTMLLMTV):** Current PTM Lower Local Master Time Value(CPTMLLMTV): This field reports the lower fields bits 31:0 of the Local TSC time value.

17.1.69 PTM Upper Local Master Time (PTMULMT)—Offset 398h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Upper Local Master Time Value (CPTMULMTV):** Current PTM Upper Local Master Time Value(CPTMULMTV): This field reports the upper fields bits 63:32 of the Local TSC time value.

17.1.70 PTM Pipe Stage Delay Configuration 1 (PTMPSDC1)—Offset 39Ch

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN1 X2 RX Pipe Stage Delay (G1X2RPSD):** GEN1 X2 RX Pipe Stage Delay(G1X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN1 X2 TX Pipe Stage Delay (G1X2TPSD):** GEN1 X2 TX Pipe Stage Delay(G1X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN1 X1 RX Pipe Stage Delay (G1X1RPSD):** GEN1 X1 RX Pipe Stage Delay(G1X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN1 X1 TX Pipe Stage Delay (G1X1TPSD):** GEN1 X1 TX Pipe Stage Delay(G1X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.1.71 PTM Pipe Stage Delay Configuration 2 (PTMPSDC2)—Offset 3A0h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN2 X1 RX Pipe Stage Delay (G2X1RPSD):** GEN2 X1 RX Pipe Stage Delay(G2X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN2 X1 TX Pipe Stage Delay (G2X1TPSD):** GEN2 X1 TX Pipe Stage Delay(G2X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN1 X4 RX Pipe Stage Delay (G1X4RPSD):** GEN1 X4 RX Pipe Stage Delay(G1X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN1 X4 TX Pipe Stage Delay (G1X4TPSD):** GEN1 X4 TX Pipe Stage Delay(G1X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.1.72 PTM Pipe Stage Delay Configuration 3 (PTMPSDC3)—Offset 3A4h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN2 X4 RX Pipe Stage Delay (G2X4RPSD):** GEN2 X4 RX Pipe Stage Delay(G2X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN2 X4 TX Pipe Stage Delay (G2X4TPSD):** GEN2 X4 TX Pipe Stage Delay(G2X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN2 X2 RX Pipe Stage Delay (G2X2RPSD):** GEN2 X2 RX Pipe Stage Delay(G2X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN2 X2 TX Pipe Stage Delay (G2X2TPSD):** GEN2 X2 TX Pipe Stage Delay(G2X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.1.73 PTM Pipe Stage Delay Configuration 4 (PTMPSDC4)—Offset 3A8h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN3 X2 RX Pipe Stage Delay (G3X2RPSD):** GEN3 X2 RX Pipe Stage Delay(G3X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN3 X2 TX Pipe Stage Delay (G3X2TPSD):** GEN3 X2 TX Pipe Stage Delay(G3X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN3 X1 RX Pipe Stage Delay (G3X1RPSD):** GEN3 X1 RX Pipe Stage Delay(G3X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN3 X1 TX Pipe Stage Delay (G3X1TPSD):** GEN3 X1 TX Pipe Stage Delay(G3X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.1.74 PTM Pipe Stage Delay Configuration 5 (PTMPSDC5)—Offset 3ACh

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:8	0h RW	**GEN3 X4 RX Pipe Stage Delay (G3X4RPSD):** GEN3 X4 RX Pipe Stage Delay(G3X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN3 X4 TX Pipe Stage Delay (G3X4TPSD):** GEN3 X4 TX Pipe Stage Delay(G3X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.1.75 PTM Extended Config (PTMECFG)—Offset 3B0h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20:18	0h RW	**Periodic Local TSC Link Fetch Frequency (PLTLFF):** Periodic Local TSC Link Fetch Frequency (PLTLFF): When this register is programmed to a non-zero values, the Local TSC Link Clock would perform a periodic fetch to obtain the latest TSC from the Local TSC XTAL Clock domain. This mechanism would ensure the Root Port Local TSC Link is always synchronized with the actual TSC as Link Clock domain is able to drift due to SSC. 000: Disable this feature. 001: Always pull without waiting for expiration. 010: Every 8 clocks 011: Every 16 clocks 100: Every 32 clocks 101: Every 64 clocks 110: Every 128 clocks 111: Every 256 clocks This register is only available in Port 1. Note: Software is expected to program this register prior to setting PTM Enable.
17:15	0h RW/1C/V	**Global Time Fetch Retry Counter (GTFRC):** Global Time Fetch Retry Counter. This register is incremented when the Root Port detected a retry on each Global Time Fetch on IOSF Sideband. The Root Port would increment the value of this register whenever ARU re-sends a LocalSync message. If more than 7 Retries are detected during the Global Time Fetch, Root Port would keep the value of this register to 111 (max) value. Software is expected to write 111 to this register to clear the entire field to 0. Note: For each x4 instance, only the value from Port 1 is used.
14:13	0h RW/1C/V	**Global Time Fetch Fail Counter (GTFFC):** Global Time Fetch Fail Counter. This register is incremented when the Root Port detected a fail on each Global Time Fetch on IOSF Sideband. The Root Port would increment the value of this register whenever ARU sends a SyncComp with the Fail status. If more than 3 failures are detected in the Global Time Fetch, Root Port would keep the value of this register to 111 (max) value. Software is expected to write 11 to this register to clear the entire field to 0. Note: For each x4 instance, only the value from Port 1 is used.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Global Time Fetch Status Pending Completion (GTFSPC):** Global Time Fetch Status Pending Completion. This register is set to 1 by the Root Port when it is in progress of fetching the Global Time from ARU. Note: For each x4 instance, only the value from Port 1 is used.
11:9	0h RW	**Periodic Global Time Stamp Counter Fetch Frequency (PGTSCFF):** Periodic Global Time Stamp Counter Fetch Frequency (PGTSCFF) : This field determine the frequency the Root Port would autonomously fetch the Global Time Stamp Counter. 00: 10us 01: 100us 10: 500us 10: 1ms Software is expected to program this bit first before programming the PGTSCFE register. Attribute: Dynamic Note: For each x4 instance, only the value from Port 1 is used.
8	0h RW	**Periodic Global Time Stamp Counter Fetch Enable (PGTSCFE):** Periodic Global Time Stamp Counter Fetch Enable (PGTSCFE) : When this bit set, the Controller will re-fetch the Global Time from the Always Running Unit (ARU). Once Fetch is completed, the Controller would update all the Local TSC with the newly fetch Global Time. If any PTM dialog is initiated while the re-fetch occurred, the Controller would use the existing Local TSC timers. Hardware would clear this bit upon completed fetching the Global Time. Attribute : Dynamic Note: For each x4 instance, only the value from Port 1 is used.
7	0h RW	**Trigger Global Time Stamp Counter Fetch Enable (TGTSCFE):** Trigger Global Time Stamp Counter Fetch Enable (TGTSCFE) : When this bit set, the Controller will re-fetch the Global Time from the Always Running Unit (ARU). Once Fetch is completed, the Controller would update all the Local TSC with the newly fetch Global Time. If any PTM dialog is initiated while the re-fetch occurred, the Controller would use the existing Local TSC timers. Hardware would clear this bit upon completed fetching the Global Time. Software can only set this register if PGTSCFE is not set. Attribute : Dynamic Note: For each x4 instance, only the value from Port 1 is used.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**PTM Request Periodic ACK Enable (PTMRPAE):** PTM Request Periodic ACK Enable (PTMRPAE) : When this register is set to 1, whenever a valid PTM request TLP is received, the Link Layer would transmit multiple ACK DLLPs corresponding to the PTM Request message. The number of ACK DLLP that the Link Layer would transmit is based on the PTMRNOPAD register. Attribute : Static Note: For each x4 instance, only the value from Port 1 is used.
5:4	0h RW	**PTM Request Number Of Periodic ACK DLLP (PTMRNOPAD):** PTM Request Number Of Periodic ACK DLLP (PTMRNOPAD) : When PTMRPAE is enable, whenever a valid PTM Request message is received, the Link Layer would transmit multiple ACK DLLP corresponding to the receiving of the PTM Request message. This register define the number of DLLP ACK will be transmitted as high priority. 00 - TX 1 DLLP ACK 01 - TX 2 DLLP ACK 10 - TX 3 DLLP ACK 11 - TX 4 DLLP ACK Attribute : Static Note: For each x4 instance, only the value from Port 1 is used.
3:0	0h RW	**IOSF Max Allowed Delay programming (IOSFMADP):** IOSF Max Allowed Delay programming (IOSFMADP): bits Status 0000 Bound Range Low 0001 Bound Range 2 1000 Bound Range Max others reserved

17.1.76 PTM Lower T2 Time Stamp (PTMLT2TSTMP)—Offset 3B4h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Latest Captured Lower T2 TimeStamp (LCLT2TS):** Latest Captured Lower T2 TimeStamp (LCLT2TS). This field shows the latest lower 32-bit of T2 TimeStamp captured by the Root Port in TSC Clock Domain when the Root Port received a valid PTM Request message. The renewable T2 TimeStamp due to a duplicate PTM Request would also be reflected in this field.

17.1.77 PTM Upper T2 Time Stamp (PTMUT2TSTMP)—Offset 3B8h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Latest Captured Upper T2 TimeStamp (LCUT2TS):** Latest Captured Upper T2 TimeStamp (LCUT2TS). This field shows the latest upper 32-bit of T2 TimeStamp captured by the Root Port in TSC Clock Domain when the Root Port received a valid PTM Request message. The renewable T2 TimeStamp due to a duplicate PTM Request would also be reflected in this field.

17.1.78 Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**mod-PHY Power Gating Disable Fuse (mPHYPGD):** 0: mod-PHY power gating is enabled. 1: mod-PHY power gating is disabled. Note: Prior to fuse pull, the default of this bit is specified in the 'Reset' column of this field. The default value will reflect the fuse value once fuse pull is done.
30:0	0h RO	**Reserved (RSVD):** Reserved

17.1.79 Thermal and Power Throttling (TNPT)—Offset 418h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 930h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Throttle Period (TP):** Throttle Period (TP): If any of the TNPT.DRXLTE or TNPT.DTXLTE bit is '1, this field defines the duration in milliseconds that defines the Throttling Window. When TNPT.TTG is set to 0, the effective Throttling Period is: 00h: 1 ms 01h: 2 ms : : FFh: 256 ms Note: The Throttle Period will have an uncertainty of +/-1 ms. When TNPT.TTG is set to 1, the effective Throttling Period is: 00h: 100 us 01h: 200 us : : FFh: 25.6 ms Note: The Throttle Period will have an uncertainty of +/-100 us. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling. Note: If TNPT.TT is programmed to a value bigger than TNPT.TP, the hardware behavior is undefined.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RW	**Throttle Time (TT):** Throttle Time (TT): If any of the TNPT.DRXLTE or TNPT.DTXLTE bit is '1, this field defines the period of the Throttling Zone within the Throttling Window specified by TNPT.TP. The value specified in this field will be multiplied by the respective multiplier in TNPT.TSLxM fields depending on the throttling severity indication received together with the Throttling State change indication. When TNPT.TTG is set to 0, the effective Throttle Time is: 00h: 1 ms 01h: 2 ms : 3Fh: 64 ms Others: Alias to 3Fh. Note: The Throttle Period will have an uncertainty of +/-1 ms. When TNPT.TTG is set to 1, the effective Throttle Time is: 00h: 100 us 01h: 200 us : 3Fh: 6.4 ms Note: The Throttle Period will have an uncertainty of +/-100 us. Note: If the reserved encoding is programmed to this field, hardware will behave the same as if the field is programmed to 3Fh. Note: Since the design is using a 1 ms tick for this timer, the Throttle Time will have an uncertainty of +/-1 ms. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling. Note: If TNPT.TT is programmed to a value bigger than TNPT.TP, the hardware behavior is undefined.
15:12	0h RO	**Reserved (RSVD):** Reserved
11:10	2h RW	**Throttling Severity Level 3 Multiplier (TSL3M):** Throttling Severity Level 3 Multiplier (TSL3M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: Always throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.

Bit Range	Default & Access	Field Name (ID): Description
9:8	1h RW	**Throttling Severity Level 2 Multiplier (TSL2M):** Throttling Severity Level 2 Multiplier (TSL2M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: Always throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.
7:6	0h RW	**Throttling Severity Level 1 Multiplier (TSL1M):** Throttling Severity Level 1 Multiplier (TSL1M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: No throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the link throttling
5:4	3h RW	**Throttling Severity Level 0 Multiplier (TSL0M):** Throttling Severity Level 0 Multiplier (TSL0M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: No throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.
3	0h RO	**Reserved (RSVD_1):** Reserved
2	0h RW	**Throttling Timer Granuality (TTG):** Throttling Timer Granuality (TTG): This register determines the granuality of the Thermal Throttling timers. This provides a smaller granuality

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Dynamic RX Link Throttling Enable (DRXLTE):** Dynamic RX Link Throttling Enable (DRXLTE): '0b: Dynamic Link RX Throttling mechanism is disabled. '1b: Dynamic Link RX Throttling mechanism is enabled. PCIe Root Port will induce the link to enter RXL0s. The duty cycle of the throttling window is configurable based on the throttling severity. Note: This field can only be set if the remote component supports TXL0s.
0	0h RW	**Dynamic TX Link Throttling Enable (DTXLTE):** Dynamic TX Link Throttling Enable (DTXLTE): '0b: Dynamic Link TX Throttling mechanism is disabled. '1b: Dynamic Link TX Throttling mechanism is enabled. PCIe Root Port will induce the link to enter TXL0s. The duty cycle of the throttling window is configurable based on the throttling severity. Note: This field can only be set if the remote component supports TXL0s.

17.1.80 Dynamic Lane Switch (DYNLNSW)—Offset 41Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved (RSVD):** Reserved.
0	0h RW	**Hardware Re-Do Preset to Coefficient Mapping Query After Lane Switching (HWRP2CM):** Hardware Re-Do Preset to Coefficient Mapping Query After Lane Switching (HWRP2CM): When this bit is set, the PCIe-SIP Controller would query the Preset to Coefficient mapping through the PIPE GetLocalPresetCoefficients and LocalTxCoefficientsValid interface whenever the Lane Switch ownership has transitioned to PCIe (from another Controller). Note that if this bit is set while the HPCMQE bit is set, the PCIe-SIP Controller would only perform the query once. Unlike the HPCMQE bit, the PCIe-SIP Controller would not clear this bit after completing the query over the PIPE interface. Register Attribute: Static.

17.1.81 Power Control Enable (PCE)—Offset 428h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 9h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved (RSVD):** Reserved for Force Isolate and Reset Together. This bit is not used. The timing between isolate and reset can be controller through PGCBCTL register.
5	0h RW	**Hardware Autonomous Enable (HAE):** Hardware Autonomous Enable (HAE): If set, and the corresponding per-LTSSM state power gating enable bit is also set, then controller power gating will be done when the controller is idle and the controller power gating condition is met in that particular LTSSM state. Refer to PCIEPMECTL2 register for the per-LTSSM state power gating enable bit. If either this bit. is not set or the corresponding per-LTSSM state power gating enable bit is not set, then controller power gating will not be done in that LTSSM state. Note: For each x4 instance, only the value from Port 0 is used. NOTE: If this bit is set, then bits[lb]2:0[rb] must be '000.
4	0h RO	**Reserved (RSVD_1):** Reserved for Force Isolate and Reset Together. This bit is not used. The timing between isolate and reset can be controller through PGCBCTL register.
3	1h RW/L	**Sleep Enable (SE):** Sleep Enable (SE): If clear, Sleep indication to the retention flops will never assert. If set, Sleep indication will be assert to the retention flops as part of the hardware autonomous controller power gating entry flow.
2	0h RO	**Reserved (RSVD_2):** Reserved for D3-Hot Enable. Not supported. RTD3 is supported instead.
1	0h RO	**Reserved (RSVD_3):** Reserved for D0i3 Enable. No support for D0i3.
0	1h RW	**PMC Request Enable (PMCRE):** PMC Request Enable (PMCRE): When set, the controller will only power gate when pmc_[lt]ip[gt]_sw_pg_req_b = '0 and hardware autonomous controller power gating conditions are met. When clear, controller will power gate immediately when the hardware autonomous controller power gating conditions are met regardless of the state of pmc_[lt]ip[gt]_sw_pg_req_b.

17.1.82 PGCB Control1 (PGCBCTL1)—Offset 42Ch

This register specifies the minimum number of delay clocks the PGCB should wait between various states.
Note: For each x4 instance, only the value from Port 0 is used.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 14155555h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved for cfg_trsvd0. Not applicable since frc_clk_srst_en is tied to '0.
29:28	1h RW	**cfg_trstup2frcclks (trstup2frcclks):** cfg_trstup2frcclks(cfg_trstup2frcclks): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
27:26	1h RW	**cfg_tclksonack_cp (tclksonack_cp):** cfg_tclksonack_cp(cfg_tclksonack_cp): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
25:24	0h RO	**Reserved (RSVD_1):** Reserved for cfg_tclksoffack_srst. Not applicable since frc_clk_srst_en is tied to 0.
23:22	0h RO	**Reserved (RSVD_2):** Reserved for cfg_tclksonack_srst. Not applicable since frc_clk_srst_en is tied to 0.
21:20	1h RW	**cfg_tpokup (tpokup):** cfg_tpokup(cfg_tpokup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
19:18	1h RW	**cfg_tpokdown (tpokdown):** cfg_tpokdown(cfg_tpokdown): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
17:16	1h RW	**cfg_tlatchdis (tlatchdis):** cfg_tlatchdis(cfg_tlatchdis): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
15:14	1h RW	**cfg_tsleepinactiv (tsleepinactiv):** cfg_tsleepinactiv(cfg_tsleepinactiv): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
13:12	1h RW	**cfg_tinaccrstup (tinaccrstup):** cfg_tinaccrstup(cfg_tinaccrstup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
11:10	1h RW	**cfg_taccrstup (taccrstup):** cfg_taccrstup(cfg_taccrstup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
9:8	1h RW	**cfg_tlatchen (tlatchen):** cfg_tlatchen(cfg_tlatchen): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
7:6	1h RW	**cfg_tdeisolate (tdeisolate):** cfg_tdeisolate(cfg_tdeisolate): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
5:4	1h RW	**cfg_trstdown (trstdown):** cfg_trstdown(cfg_trstdown): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
3:2	1h RW	**cfg_tisolate (tisolate):** cfg_tisolate(cfg_tisolate): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
1:0	1h RW	**cfg_tsleepact (tsleepact):** cfg_tsleepact(cfg_tsleepact): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

17.1.83 PGCB Control2 (PGCBCTL2)—Offset 430h

This register specifies the minimum number of delay clocks the PGCB should wait between various states.
Note: For each x4 instance, only the value from Port 0 is used.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 54h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved.
7:6	1h RW	**cfg_trsvd4 (trsvd4):** cfg_trsvd4(cfg_trsvd4): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
5:4	1h RW	**cfg_trsvd3 (trsvd3):** cfg_trsvd3(cfg_trsvd3): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
3:2	1h RW	**cfg_trsvd2 (trsvd2):** cfg_trsvd2(cfg_trsvd2): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	**Reserved (RSVD_1):** Reserved for cfg_trsvd1. Not applicable since frc_clk_srst_en is tied to 0.

17.1.84 Equalization Configuration 1 (EQCFG1)—Offset 450h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 3102h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Recovery Entry Count (REC):** Recovery Entry Count (REC): This field indicates the value of the Recovery Entry Counter. This is a 1-based counter. Software must read this register multiple times. The value is valid only if the same value is read out on both of the reads.
23	0h RW	**Recovery Entry and Idle Framing Error Count Enable (REIFECE):** Recovery Entry and Idle Framing Error Count Enable (REIFECE): This bit, when set by software turns on the Recovery Entry Counter and the per-lane Idle Framing Error Counter. The counters are reset when this bit is cleared. This bit is expected to be used by the Software Preset/Coefficient Search tool but is not precluded to be used for other debug purpose. The value of the Recovery Entry Count can be read through EQCFG1.REC field. The value of the Idle Framing Error Count can be read through the Monitor Mux register.
22	0h RW	**Quiesce Guarantee (QG):** Quiesce Guarantee (QG): When set, the Quiesce Guarantee bit in the transmitted TS2 Ordered Set will be set in Recovery.RcvrCfg. When clear, the Quiesce Guarantee bit in the transmitted TS2 Ordered Set will be clear. In all other states, the Quiesce Guarantee bit is Reserved.
21	0h RW	**Link Equalization Request SMI Enable (LERSMIE):** Link Equalization Request SMI Enable (LERSMIE): When set, this bit enables the generation of an SMI to indicate that the Link Equalization Request bit has been set. This mode is meant for survivability purpose such that BIOS can be invoked to address the Re-Equalization request.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Reset EIEOS Interval Count (REIC):** Reset EIEOS Interval Count(REIC): When set, allows the root port to restrict the device from sending EIEOS until after 65536 TS1 Ordered Sets have been transmitted in Phase 3 of the Link Equalization, in the window when the receiver is evaluating the remote transmitter settings..
19	0h RW	**Link Equalization Bypass (LEB):** Link Equalization Bypass (LEB): When set, the root port will never initiate entry to Recovery.Equalization state. This includes never send EQ TS2 in Recovery.RcvrCfg that could cause the device to set start_equalization_w_preset variable. Note: This bit only affects the initial autonomous transition to Link Equalization state when equalization_done_8GT_data_rate = 0. This bit does not affect the software-direction to re-perform Link Equalization.
18	0h RW	**Link Equalization Phase 2 and 3 Bypass (LEP23B):** Link Equalization Phase 2 and 3 Bypass(LEP23B): When set, bypasses the Phase 2 and Phase 3 of Link Equalization. Once Phase 1 is completed, Root Port transitions from Phase 1 directly to Recovery.RcvrLock.
17	0h RW	**Link Equalization 3 Bypass (LEP3B):** Link Equalization 3 Bypass(LEP3B): When set, bypasses the Phase 3 of Link Equalization. Once Phase 2 is completed, Root Port transitions from Phase 2 directly to Recovery.RcvrLock.
16	0h RW	**Remote Transmit Link Equalization Preset/Coefficient Evaluation Bypass (RTLEPCEB):** Remote Transmit Link Equalization Preset/Coefficient Evaluation Bypass (RTLEPCEB): When set, this bit disables the Hardware Autonomous Preset/ Coefficient Search mechanism to search for the best Preset or Coefficient by traversing the Preset or Coefficient List and checking the receiver eye width margin for each of the settings. Instead, the Preset/Coefficient values used by the remote Transmitter will be accepted and the Link Equalization phase will be completed after one round of receiver link training, excluding margining. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Remote Transmitter Preset Coefficient Override Enable (RTPCOE):** Remote Transmitter Preset Coefficient Override Enable (RTPCOE): When set, this bit disables the hardware mechanism to search for the best Preset or Coefficient by traversing the Preset or Coefficient List and checking the receiver eye width margin for each of the settings. Instead, the Preset or Coefficient values specified by the override fields are used. If RTPCL1.PCM = 1, the Preset Override values for each lanes is derived from the following register fields: Lane 0: RTPCL1.RTPRECL0PL0. Lane 1: RTPCL1.RTPOSTCL0PL1. Lane 2: RTPCL1.RTPRECL1PL2. Lane 3: RTPCL1.RTPOSTCL1PL3. If RTPCL1.PCM = 0, the Coefficient Override values for each lanes is derived from the following register fields: Lane 0: RTPCL1.RTPRECL0PL0 and RTPCL1.RTPOSTCL0PL1. Lane 1: RTPCL1.RTPRECL1PL2 and RTPCL1.RTPOSTCL1PL3. Lane 2: RTPCL1.RTPRECL2PL4 and RTPCL2.RTPOSTCL2PL5. Lane 3: RTPCL2.RTPRECL3PL6 and RTPCL2.RTPOSTCL3PL7. BIOS must ensure that the corresponding RTPCL* registers above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
14	0h RW	**Link Equalization Request SCI Enable (LERSCIE):** Link Equalization Request SCI Enable (LERSCIE): When set, this bit enables the generation of an SCI to indicate that the Link Equalization Request bit has been set. This mode is meant for survivability purpose such that SCI handler can be invoked to address the Re-Equalization request.

Bit Range	Default & Access	Field Name (ID): Description
13	1h RW/1S/V	**Hardware Preset to Coefficient Mapping Query Enable (HPCMQE):** Hardware Preset to Coefficient Mapping Query Enable(HPCMQE): When set, the controller will query the Preset to Coefficient mapping through the PIPE GetLocalPresetCoefficients and LocalTxCoefficientsValid interface whenever this bit transitions from 0 to 1. The default of this register bit is 1, indicating that the Preset to Coefficient mapping query will be done on the PIPE interface once coming out of reset. Controller will then update the Preset-Coefficient Mapping registers with the corresponding Coefficient, for each Preset. Controller will also update the LFFS Local LF and Local FS field with the local PHY LF and FS values. Hardware will clear this bit when the Preset to Coefficient mapping query over the PIPE interface is completed. If the Hardware Preset to Coefficient Mapping mechanism is never enabled, the value of the Preset to Coefficient mapping configured by BIOS through the Preset-Coefficient Mapping registers will be used instead of querying through the PIPE interface. Note: BIOS should check to ensure that this field is cleared before enabling Controller Power Gating or mod-PHY Power Gating.
12	1h RO/V	**Hardware Autonomous Equalization Done (HAED):** Hardware Autonomous Equalization Done(HAED): This bit will be cleared when Hardware Autonomous Preset/Coefficient Search starts and will be set when Hardware Autonomous Preset/Coefficient Search is done. This bit is polled by software to ensure that the Hardware Autonomous Preset/Coefficient Search is done before proceeding with the next software sequencing. Some of the Hardware Autonomous Preset/ Coefficient search algorithm may involve the hardware initiating multiple speed change to allow multiple iterations of Link Equalization to be done with different Preset/Coefficient lists. This bit will remain cleared until the iterations are done.

Bit Range	Default & Access	Field Name (ID): Description
11:8	1h RW	**Receiver Wait Time For New Equalization Value Evaluation (RWTNEVE):** Receiver Wait Time For New Equalization Value Evaluation (RWTNEVE): For Downstream Port: This field specifies the amount of time the receiver will wait after entering Phase 3 and sending the new Preset or Coefficient values through the TS1 Ordered Sets before validating the Block Alignment and eventually evaluate the incoming ordered sets (RXEqEval on the PIPE interface asserts). For Upstream Port: This field specifies the amount of time the receiver will wait after entering Phase 2 and sending the new Preset or Coefficient values through the TS1 Ordered Sets before validating the Block Alignment and eventually evaluate the incoming ordered sets (RXEqEval on the PIPE interface asserts). For both Upstream and Downstream Port, this field also specifies the amount of time the receiver will wait after entering Phase 1 before instructing the receiver to adapt to the incoming ordered sets. For Loopback Master: This field specifies the amount of time the receiver will wait after instructing the Loopback Slave to apply a specific Preset through EQ TS1. 0h: 500 ns. 1h: 1 us. 2h: 2 us. 3h: 3 us. 4h: 4 us. : : Fh:15 us.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**EQ TS2 in Recovery.ReceiverConfig Enable (EQTS2IRRC):** EQ TS2 in Recovery.ReceiverConfig Enable(EQTS2IRRC): When set, enables the transmitter to send EQ TS2 in Recovery.RcvrCfg state even when equalization_done_8GT_data_rate variable is 1b, provided that the Downstream Port advertised 8.0 GT/s data rate support in Recovery.RcvrLock, and 8.0 GT/s data rate support has been advertised in the Configuration.Complete or Recovery.RcvrCfg substates by the Upstream Port since exiting the Detect state, and eight consecutive TS1 or TS2 Ordered Sets were received on any configured Lane prior to entry to this substate with speed_change bit set to 1b. When clear, the transmitter can only send EQ TS2 if equalization_done_8GT_data_rate variable is 0b and the Downstream Port advertised 8.0 GT/s data rate support in Recovery.RcvrLock, and 8.0 GT/s data rate support has been advertised in the Configuration.Complete or Recovery.RcvrCfg substates by the Upstream Port since exiting the Detect state, and eight consecutive TS1 or TS2 Ordered Sets were received on any configured Lane prior to entry to this substate with speed_change bit set to 1b. When this bit is used, hardware must ensure that the start_equalization_w_preset variable are in the correct state to ensure that the components on both sides of the link are never out of sync.
6:4	0h RO	**Reserved (RSVD):** Reserved
3	0h RW	**Link EQ Phase 1 Transmit Coefficient Settling Policy (LEQP1TCSP):** Link EQ Phase 1 Transmit Coefficient Settling Policy(LEQP1TCSP): When operating in GEN3 data rate and there is a software/hardware request to re-perform Link Equalization through the Recovery.RcvrLock to Recovery.Equalization arc, PCIe spec requires that the downstream port transmitter switch to the setting specified by the Downstream Port Lane X Transmitter Preset registers in Phase 1. This switching is happening while the downstream port is still actively transmitting TS1 and the upstream port is only required to sample 2 TS1 to determine the next sub-state to transition to. Since the new coefficient setting can take up to 256 ns to settle, the 2 TS1 sampled by the upstream port may be incorrect causing the two LTSSM to be out of sync. When this bit is set, the RP will continue to send EIEOS until the local transmitter setting has settled (specified by PHYCTL2.TXCFGCHGWAIT) before sending TS1 as required in Recovery.Equalization Phase 1. When this bit is clear, the RP will send TS1 with EC = 01 in Recovery.Equalization Phase 1 even though the transmitter setting is still settling.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Multi-Fragment Linear and Nine-Tile List Enable (MFLNTL):** Multi-Fragment Linear and Nine-Tile List Enable(MFLNTL): When set in Hardware Autonomous Linear Preset/Coefficient Search mode, the full Preset/Coefficient List will be traversed in multiple fragments, where each fragments is done in separate entry to Recovery. This is used in the case where a longer dwelling time is required for a particular Preset/Coefficient (configured through EQCFG2.PCET). Subsequent Preset/Coefficient entries within the list that could not be covered within that Recovery session will be covered in subsequent re-entries into Recovery. When set in Hardware Autonomous Nine-Tiles Search mode, the 9-tiles list that could not be covered within that Recovery session will be covered in subsequent re-entries into Recovery.
1	1h RW	**Transmitter Use Preset Policy (TUPP):** Transmitter Use Preset Policy(TUPP): This field applies to the Link Equalization Phase where the local transmitter setting is being adjusted. When set, the transmitted TS1 Use Preset bit will be set if the remote device requests the local transmitter to apply specific Preset(instead of Coefficient). When clear, the Use Preset bit will not be set in this case. Note: This bit must be set before changing speed to GEN3 data rate.
0	0h RW	**Receiver Use Preset Policy (RUPP):** Receiver Use Preset Policy(RUPP): This field applies to the Link Equalization Phase where the remote transmitter setting is being adjusted. When set, the received TS1 Use Preset bit will be checked. When clear, the Use Preset bit in the received TS1 will be ignored. Note: This bit must be set before changing speed to GEN3 data rate.

17.1.85 Remote Transmitter Preset Coefficient List 1 (RTPCL1)—Offset 454h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Preset/Coefficient Mode (PCM):** Preset/Coefficient Mode (PCM): This bit defines whether the Preset List or Coefficient List should be sent to the remote TX to adjust the remote TX setting. For Downstream Port, this is used in Phase 3 of the Link Equalization. For Upstream Port, this is used in Phase 2 of the Link Equalization. The list of coefficient or preset is configurable through the Remote Transmitter Preset Coefficient List [lb]1:4[rb] registers. When this bit is set, Coefficient Mode is enabled and the Remote Transmitter Preset Coefficient List [lb]1:4[rb] registers contain the Coefficient List. When this bit is clear, Preset Mode is enabled and the Remote Transmitter Preset Coefficient List [lb]1:3[rb] registers contain the Preset List.
30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 2/Preset List 4 (RTPRECL2PL4):** Remote Transmitter Pre-Cursor Coefficient List 2/Preset List 4 (RTPRECL2PL4): For Downstream Port: This field defines the pre-cursor coefficient List 2 or Preset List 4 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 2 or Preset List 4 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Remote Transmitter Post-Cursor Coefficient List 1/Preset List 3 (RTPOSTCL1PL3):** Remote Transmitter Post-Cursor Coefficient List 1/Preset List 3 (RTPOSTCL1PL3): For Downstream Port: This field defines the post-cursor coefficient List 1 or Preset List 3 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 1 or Preset List 3 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
17:12	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 1/Preset List 2 (RTPRECL1PL2):** Remote Transmitter Pre-Cursor Coefficient List 1/Preset List 2 (RTPRECL1PL2): For Downstream Port: This field defines the pre-cursor coefficient List 1 or Preset List 2 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 1 or Preset List 2 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Remote Transmitter Post-Cursor Coefficient List 0/Preset List 1 (RTPOSTCL0PL1):** Remote Transmitter Post-Cursor Coefficient List 0/Preset List 1 (RTPOSTCL0PL1): For Downstream Port: This field defines the post-cursor coefficient List 0 or Preset List 1 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 0 or Preset List 1 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
5:0	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 0/Preset List 0 (RTPRECL0PL0):** Remote Transmitter Pre-Cursor Coefficient List 0/Preset List 0 (RTPRECL0PL0): For Downstream Port: This field defines the pre-cursor coefficient List 0 or Preset List 0 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 0 or Preset List 0 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.1.86 Remote Transmitter Preset Coefficient List 2 (RTPCL2)—Offset 458h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Remote Transmitter Post-Cursor Coefficient List 4/Preset List 9 (RTPOSTCL4PL9):** Remote Transmitter Post-Cursor Coefficient List 4/Preset List 9(RTPOSTCL4PL9): For Downstream Port: This field defines the post-cursor coefficient List 4 or Preset List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 4 or Preset List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 4/Preset List 8 (RTPRECL4PL8):** Remote Transmitter Pre-Cursor Coefficient List 4/Preset List 8 (RTPRECL4PL8): For Downstream Port: This field defines the pre-cursor coefficient List 4 or Preset List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 4 or Preset List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Post-Cursor Coefficient List 3/Preset List 7 (RTPOSTCL3PL7):** Remote Transmitter Post-Cursor Coefficient List 3/Preset List 7 (RTPOSTCL3PL7): For Downstream Port: This field defines the post-cursor coefficient List 3 or Preset List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 3 or Preset List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 3/Preset List 6 (RTPRECL3PL6):** Remote Transmitter Pre-Cursor Coefficient List 3/Preset List 6 (RTPRECL3PL6): For Downstream Port: This field defines the pre-cursor coefficient List 3 or Preset List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 3 or Preset List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Post-Cursor Coefficient List 2/Preset List 5 (RTPOSTCL2PL5):** Remote Transmitter Post-Cursor Coefficient List 2/Preset List 5 (RTPOSTCL2PL5): For Downstream Port: This field defines the post-cursor coefficient List 2 or Preset List 5 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 2 or Preset List 5 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.1.87 Remote Transmitter Preset Coefficient List 3 (RTPCL3)—Offset 45Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 7 (RTPRECL7):** Remote Transmitter Pre-Cursor Coefficient List 7 (RTPRECL7): For Downstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Post-Cursor Coefficient List 6 (RTPOSTCL6):** Remote Transmitter Post-Cursor Coefficient List 6 (RTPOSTCL6): For Downstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 6 (RTPRECL6):** Remote Transmitter Pre-Cursor Coefficient List 6 (RTPRECL6): For Downstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Post-Cursor Coefficient List 5 (RTPOSTCL5):** Remote Transmitter Post-Cursor Coefficient List 5 (RTPOSTCL5): For Downstream Port: This field defines the pre-cursor coefficient List 5 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 5 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 5/Preset List 10 (RTPRECL5PL10):** Remote Transmitter Pre-Cursor Coefficient List 5/Preset List 10 (RTPRECL5PL10): For Downstream Port: This field defines the pre-cursor coefficient List 5 or Preset List 10 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 5 or Preset List 10 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.1.88 Remote Transmitter Preset Coefficient List 4 (RTPCL4)—Offset 460h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Remote Transmitter Post-Cursor Coefficient List 9 (RTPOSTCL9):** Remote Transmitter Post-Cursor Coefficient List 9 (RTPOSTCL9): For Downstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 9 (RTPRECL9):** Remote Transmitter Pre-Cursor Coefficient List 9 (RTPRECL9): For Downstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Post-Cursor Coefficient List 8 (RTPOSTCL8):** Remote Transmitter Post-Cursor Coefficient List 8 (RTPOSTCL8): For Downstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 8 (RTPRECL8):** Remote Transmitter Pre-Cursor Coefficient List 8 (RTPRECL8): For Downstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Post-Cursor Coefficient List 7 (RTPOSTCL7):** Remote Transmitter Post-Cursor Coefficient List 7 (RTPOSTCL7): For Downstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.1.89 Figure Of Merit Status (FOMS)—Offset 464h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved
30:29	0h RW	**Index (I):** Index (I): The FOMV field will reflect the Figure of Merit Scoreboard value for the index specified by this field. List N below refers to the Figure of Merit values captured in the scoreboard corresponding to the Preset or Coefficient List N. 00b: Index 0 =[gt] {List 2, List 1, List 0}. 01b: Index 1 =[gt] {List 5, List 4, List 3}. 10b: Index 2 =[gt] {List 8, List 7, List 6}. 11b: Index 3 =[gt] {Rsvd, List 10, List 9}.

Bit Range	Default & Access	Field Name (ID): Description
28:24	0h RW	**Lane Number (LN):** Lane Number (LN): The FOMV field will reflect the Figure of Merit Scoreboard value for the lane specified by this field. 00000b: Lane 0. 00001b: Lane 1. 00010b: Lane 2. 00011b: Lane 3. Others: Reserved.
23:0	0h RO/V	**Figure of Merit Scoreboard Value (FOMSV):** Figure of Merit Scoreboard Value (FOMSV): This field will reflect the Figure of Merit Scoreboard entries referenced by the Lane Number and Index field in this register. For example, when Index == 00b, this field will reflect the Figure of Merit values for Lane specified in Lane Number field and the encoding of this field is as shown below: 23:16: Figure of Merit for Preset/Coefficient List 2. 15:8 : Figure of Merit for Preset/Coefficient List 1. 7:0 : Figure of Merit for Preset/Coefficient List 0. If the Receiver Eye Width margining completes with error, the value of Figure of Merit should reflect 0x00.

17.1.90 Hardware Autonomous Equalization Control (HAEQ)—Offset 468h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: A0080E00h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Ah RW	**Hardware Autonomous Preset/Coefficient Count Per-Iteration (HAPCCPI):** Hardware Autonomous Preset/Coefficient Count Per-Iteration(HAPCCPI): This field defines the number of Preset/Coefficient to be traversed for every iteration of Recovery Equalization. For the Linear Mode, EQCFG2.HAPCSB specifies the total number of Presets/Coefficients to be checked in total while this field specifies the number of Presets/Coefficients to be checked per-iteration of Recovery Equalization. Hardware will enter Recovery Equalization and check the number of Presets/Coefficients specified by this field. Once that is done, hardware will exit Recovery Equalization and trigger another entry to Recovery Equalization to check another set of Presets/Coefficients. This goes on until the total number of Presets/Coefficients are checked. For Nine-Tiles Mode, EQCFG2.NTIC specifies the number of 9-tiles iterations, which indirectly specifies the total number of Presets/ Coefficients to be checked in total. Similar to Linear Mode, this field specifies the number of Presets/Coefficients to be checked per-iteration of Recovery Equalization. 0h: 1 Preset/Coefficient per-iteration. 1h: 2 Preset/Coefficient per-iteration. 2h: 3 Preset/Coefficient per-iteration. ... 9h: 10 Preset/Coefficient per-iteration. Ah: 11 Preset/Coefficient per-iteration. Others: Reserved.
27:20	0h RW	**FOM Error Mask (FOMEM):** FOM Error Mask(FOMEM): The FOM error counter will be masked(thus ignoring the FOM error) for all the FOM values prior to the FOM value specified in this field. If this field is programmed to 00h, this mechanism is disabled. This bit must be configured before training to GEN3 data rate.

Bit Range	Default & Access	Field Name (ID): Description
19	1h RW	**MAC FOM Control (MACFOMC):** MAC FOM Control(MACFOMC): When set, MAC controls the advancement of the FOM values completely while in the Link Equalization mode. For downstream port, this is done in Phase 3 and for upstream port, this is done in Phase 2 of the Link Equalization. The dwelling time for each of the FOM values are programmed through the remaining fields of this register. When enabled, the hardware will start in Speeding Mode, where it will instruct the PHY to increment the FOM value after the Speeding Latency specified by HAEQ.SL field. Once the FOM value matches HAEQ.SFOMFM, the hardware switches from Speeding Mode to Dwelling Mode. In Dwelling mode, the MAC will instruct PHY to increment the FOM value after the Dwelling Latency specified by HAEQ.DL field. This is done until the link equalization phase is completed. When cleared, PHY controls the advancement of the FOM values completely, during the Link Equalization mode. This bit must be configured before training to GEN3 data rate.
18:16	0h RW	**Speeding Latency (SL):** Speeding Latency(SL): Specifies the residency time for a particular FOM value in Speeding Mode. 000b: 192 ns. 001b: 256 ns. 010b: 512 ns. 011b: 1 us. 100b: 2 us. 101b: 4 us. 110b: 8 us. 111b: 16 us. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.
15:8	Eh RW	**Dwelling Latency (DL):** Dwelling Latency(DL): Specifies the residency time for a particular FOM value in Dwelling Mode. 00h: 2 us. 01h: 4 us. 02h: 6 us. ... FFh: 512 us. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Starting FOM For Margining (SFOMFM):** Starting FOM For Margining(SFOMFM): Define the FOM where MAC switches from Speeding Mode to Dwelling Mode after hitting the programmed FOM value in Hardware Autonomous Preset/Coefficient mode. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.

17.1.91 Local Transmitter Coefficient Override 1 (LTCO1)—Offset 470h

Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane bits are not used.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD):** Reserved
25	0h RW	**Lane 1 Transmitter Coefficient Override Enable (L1TCOE):** Lane 1 Transmitter Coefficient Override Enable (L1TCOE): When set, the transmitter coefficient override values LTPCO1.L1TPRECO and LTPCO1.L1TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO1.L1TPRECO and LTPCO1.L1TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Lane 0 Transmitter Coefficient Override Enable (L0TCOE):** Lane 0 Transmitter Coefficient Override Enable (L0TCOE): When set, the transmitter coefficient override values LTPCO1.L0TPRECO and LTPCO1.L0TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO1.L0TPRECO and LTPCO1.L0TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
23:18	0h RW	**Lane 1 Transmitter Post-Cursor Coefficient Override (L1TPOSTCO):** Lane 1 Transmitter Post-Cursor Coefficient Override (L1TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L1TCOE = 1.
17:12	0h RW	**Lane 1 Transmitter Pre-Cursor Coefficient Override (L1TPRECO):** Lane 1 Transmitter Pre-Cursor Coefficient Override (L1TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L1TCOE = 1.
11:6	0h RW	**Lane 0 Transmitter Post-Cursor Coefficient Override (L0TPOSTCO):** Lane 0 Transmitter Post-Cursor Coefficient Override (L0TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L0TCOE = 1.
5:0	0h RW	**Lane 0 Transmitter Pre-Cursor Coefficient Override (L0TPRECO):** Lane 0 Transmitter Pre-Cursor Coefficient Override (L0TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L0TCOE = 1.

17.1.92 Local Transmitter Coefficient Override 2 (LTCO2)—Offset 474h

Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane bits are not used.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD):** Reserved
25	0h RW	**Lane 3 Transmitter Coefficient Override Enable (L3TCOE):** Lane 3 Transmitter Coefficient Override Enable (L3TCOE): When set, the transmitter coefficient override values LTPCO2.L3TPRECO and LTPCO2.L3TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO2.L3TPRECO and LTPCO2.L3TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
24	0h RW	**Lane 2 Transmitter Coefficient Override Enable (L2TCOE):** Lane 2 Transmitter Coefficient Override Enable (L2TCOE): When set, the transmitter coefficient override values LTPCO2.L2TPRECO and LTPCO2.L2TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO2.L2TPRECO and LTPCO2.L2TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Lane 3 Transmitter Post-Cursor Coefficient Override (L3TPOSTCO):** Lane 3 Transmitter Post-Cursor Coefficient Override (L3TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L3TCOE = 1.
17:12	0h RW	**Lane 3 Transmitter Pre-Cursor Coefficient Override (L3TPRECO):** Lane 3 Transmitter Pre-Cursor Coefficient Override (L3TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L3TCOE = 1
11:6	0h RW	**Lane 2 Transmitter Post-Cursor Coefficient Override (L2TPOSTCO):** Lane 2 Transmitter Post-Cursor Coefficient Override (L2TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L2TCOE = 1.
5:0	0h RW	**Lane 2 Transmitter Pre-Cursor Coefficient Override (L2TPRECO):** Lane 2 Transmitter Pre-Cursor Coefficient Override (L2TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L2TCOE = 1.

17.1.93 GEN3 L0s Control (G3L0SCTL)—Offset 478h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: C00281Eh

Bit Range	Default & Access	Field Name (ID): Description
31:24	Ch RW	**Gen3 Active State L0s Preparation Latency (G3ASL0SPL):** Gen3 Active State L0s Preparation Latency (G3ASL0SPL) Determines how long the Link layer has to indicate IDLE before the link initialization and control logic enters L0s 00: 0 clocks (enter immediately) 01: 1 clock ... FF: 255 clocks The value of this register is only used if the Gen3 L0s Entry Idle Control register is set to [quote]11[/quote] and operating in Gen3 mode.
23:22	0h RW	**Gen3 L0s Entry Idle Control (G3L0SIC):** Gen3 L0s Entry Idle Control (G3L0SIC): 00 : Allow entry into L0s after the link has been idle for a period of time equal to of the received N_FTS total entry time (1/4 * N_FTS * 16) 01 : Allow entry into L0s after the link has been idle for for a period of time equal to of the received N_FTS total entry time (1/2 * N_FTS * 16) 10 : Allow entry after the link has been idle for for a period of time equal to the received N_FTS total entry time (N_FTS * 16) 11: Allow entry into L0s after the link has been idle for a period specified in the Gen3 Active State L0s Preparation Latency register. This register is only applied when operating in Gen3 mode.
21:16	0h RO	**Reserved (RSVD):** Reserved
15:8	28h RW	**Gen3 Unique Clock N_FTS (G3UCNFTS):** Gen3 Unique Clock N_FTS (G3UCNFTS): Number of Fast Training Sequence ordered sets required to be transmitted for a root port Receiver to exit L0s in a unique (non-common) clock configuration (LCTL.CCC=0) when operating in Gen3 mode. The N_FTS value is sent in TS1 and TS2 training sets during link training. 00: 0 FTS sets 01: 1 FTS set ... FF: 255 FTS sets Note: When operating in Mobile Express mode, the output of this field is not used to determine the number of FTS to be sent on TXL0s exit. Mobile Express does not support Fast Training Sequence. Instead, SYNC is used to achieve bit lock. However, the output of this field is still used in L0s Entry Idle Control registers to determine the L0s Entry Idle latency.

Bit Range	Default & Access	Field Name (ID): Description
7:0	1Eh RW	**Gen3 Common Clock N_FTS (G3CCNFTS):** Gen3 Common Clock N_FTS (G3CCNFTS): Number of Fast Training Sequence ordered sets required to be transmitted for a root port Receiver to exit L0s in a common clock configuration (LCTL.CCC=1) when operating in Gen3 mode. The N_FTS value is sent in TS1 and TS2 training sets during link training. 00: 0 FTS sets 01: 1 FTS set ... FF: 255 FTS sets Note: When operating in Mobile Express mode, the output of this field is not used to determine the number of FTS to be sent on TXL0s exit. Mobile Express does not support Fast Training Sequence. Instead, SYNC is used to achieve bit lock. However, the output of this field is still used in L0s Entry Idle Control registers to determine the L0s Entry Idle latency.

17.1.94 Equalization Configuration 2 (EQCFG2)—Offset 47Ch

Size:32 bits
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: A001h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Nine-Tiles Iteration Count (NTIC):** Nine-Tiles Iteration Count(NTIC): This field specifies the number of iterations to perform the 9-tiles search. Each iteration involves evaluating the neighboring 9-tiles for the best Preset/Coefficient margin and then use the Preset/Coefficient as the centerpoint to identify and evaluate the next 9-tiles. 00h: 1 iteration. 01h: 2 iterations. 02h: 3 iterations. ... FFh: 256 iterations.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**Equalization Margining Disable (EMD):** Equalization Margining Disable(EMD):When set, the Root Port will not request the PHY to perform Receiver Margining by asserting RxEqEval on each Preset/ Coefficient list traversed. This allows the receiver to still measure the Bit Error Count without margining. When cleared, the Root Port will request the PHY to perform Receiver Margining by asserting RxEqEval. This field is only valid when operating in Hardware Autonomous Preset/Coefficient Search mode. The Preset/Coefficient list will still be traversed to the end.
22:20	0h RW	**Nine-Tiles Step Size (NTSS):** Nine-Tiles Step Size(NTSS): This field specifies the step size used to identify the surrounding 9-tiles to be used for margining. 000b: 1 step. 001b: 2 steps. 010b: 3 steps. 011b: 4 steps. 100b: 5 steps. 101b: 6 steps. 110b: 7 steps. 111b: 8 steps. Each of the steps is measured in terms of incrementing of decrementing the coefficient values.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW	**Preset/Coefficient Evaluation Timeout (PCET):** Preset/ Coefficient Evaluation Timeout(PCET): This field specifies the evaluation timeout for a single Preset/Coefficient in the List when operating in Hardware Autonomous Preset/Coefficient Search mode. By spec, the evaluation phase must be completed before the 24 ms timeout. To support 12 Presets (11 Presets + 1 final good Preset), each Preset will have up to 2 ms for evaluation. This field allows the 2 ms timer to be programmable. This is useful if the EQCFG2.HAPCSB limits the Preset/Coefficient List to smaller than 12 such that each Preset/Coefficient could be evaluated for a time longer than 2 ms. 0h: 2 ms. 1h: 2.5 ms. 2h: 3 ms. 3h: 3.5 ms. 4h: 4 ms. 5h: 4.5 ms. 6h: 5 ms. 7h: 6 ms. 8h: 7 ms. 9h: 8 ms. Ah: 9 ms. Bh:10 ms. Ch:11 ms. Dh:21 ms. Eh:22 ms. Fh:23 ms.
15:12	Ah RW	**Hardware Autonomous Preset/Coefficient Search Bound (HAPCSB):** Hardware Autonomous Preset/Coefficient Search Bound(HAPCSB): This field defines the number of Preset/ Coefficient List to be traversed, out of 11 for Presets or out of 10 for Coefficients. The Preset/Coefficient list will be traversed from List 0 to the value specified by this field in incremental order. This field allows equalization to be done with smaller set of Preset/ Coefficient list and each of the Preset/Coefficient list could be run for a longer time. 0h: Preset/Coefficient List 0 only. 1h: Preset/Coefficient List 0 - 1. 2h: Preset/Coefficient List 0 - 2. : : 9h: Preset/Coefficient List 0 - 9. Ah: Preset List 0 - 10/Coefficient List 0-9. Others: Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Nine-Tiles Equalization Mechanism Enable (NTEME):** Nine-Tiles Equalization Mechanism Enable(NTEME): When set, the Nine-Tiles Equalization Mechanism is enabled when running in Hardware Autonomous Preset/Coefficient Search Mode.
10	0h RW	**Mid-Point Equalization Mechanism Enable (MPEME):** Mid-Point Equalization Mechanism Enable(MPEME): When set, the Mid-Point Equalization Mechanism is enabled when running in Hardware Autonomous Preset/Coefficient Search Mode.
9:8	0h RW	**Receiver Eye Width Margin Error Threshold Multiplier (REWMETM):** Receiver Eye Width Margin Error Threshold Multiplier (REWMETM): This field specifies the multiplier to be used with REWMET field. 00b: Multiply REWMET by 1 (effectively no multiplier). 01b: Multiply REWMET by 10. 10b: Multiply REWMET by 100. 11b: Multiply REWMET by 1000.
7:0	1h RW	**Receiver Eye Width Margin Error Threshold (REWMET):** Receiver Eye Width Margin Error Threshold (REWMET): This field specifies the count threshold which upon exceeded, will cause controller to terminate the current iteration of Receiver Eye Width Margining and move on to the next preset or coefficient in the list. The value specified in this field will need to be multiplied with the multiplier specified in REWMETM field to get the final threshold values. 00h: Terminate on 1 x REWMETM errors. 01h: Terminate on 2 x REWMETM errors. 02h: Terminate on 4 x REWMETM errors. 03h: Terminate on 6 x REWMETM errors. : : FEh: Terminate on 508 x REWMETM errors. FFh: Never terminate. Rely on PHY to terminate the margining.

17.1.95 Monitor Mux (MM)—Offset 480h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO/V	**Monitor Signal State (MSST):** Monitor Signal State(MSST): The internal signal groupings selected by MM.MSS field is reflected in this field. The intention of this monitor signal is provide software a capability to monitor some of the GEN3 related parameters accumulated by the controller through the Link Equalization that are too costly to be mapped to dedicated registers. Implementation MUST NEVER expose any security related information through this Monitor Mux.
7:0	0h RW	**Monitor Signal Select (MSS):** Monitor Signal Select(MSS): This field is essentially the mux select for the Monitor Signal mux. Setting this field allows different monitor signals to be muxed out and readable by software through the MM.MSST field.

17.1.96 Lane0 P0 and P1 Preset-Coefficient Mapping (L0P0P1PCM)—Offset 500h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.97 Lane0 P1, P2 and P3 Preset-Coefficient Mapping (L0P1P2P3PCM)—Offset 504h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.98 Lane0 P3 and P4 Preset-Coefficient Mapping (L0P3P4PCM)—Offset 508h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.99 Lane0 P5 and P6 Preset-Coefficient Mapping (L0P5P6PCM)—Offset 50Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.100 Lane0 P6, P7 and P8 Preset-Coefficient Mapping (L0P6P7P8PCM)—Offset 510h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.101 Lane0 P8 and P9 Preset-Coefficient Mapping (L0P8P9PCM)—Offset 514h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

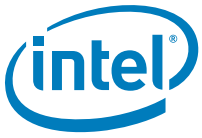
Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.102 Lane0 P10 Preset-Coefficient Mapping (L0P10PCM)—Offset 518h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.



Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.103 Lane0 LF and FS (L0LFFS)—Offset 51Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.104 Lane1 P0 and P1 Preset-Coefficient Mapping (L1P0P1PCM)—Offset 520h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.105 Lane1 P1, P2 and P3 Preset-Coefficient Mapping (L1P1P2P3PCM)—Offset 524h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.106 Lane1 P3 and P4 Preset-Coefficient Mapping (L1P3P4PCM)—Offset 528h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.107 Lane1 P5 and P6 Preset-Coefficient Mapping (L1P5P6PCM)—Offset 52Ch

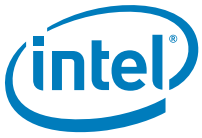
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



17.1.108 Lane1 P6, P7 and P8 Preset-Coefficient Mapping (L1P6P7P8PCM)—Offset 530h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.109 Lane1 P8 and P9 Preset-Coefficient Mapping (L1P8P9PCM)—Offset 534h

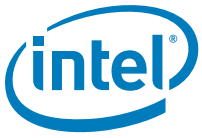
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.110 Lane1 P10 Preset-Coefficient Mapping (L1P10PCM)—Offset 538h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.111 Lane1 LF and FS (L1LFFS)—Offset 53Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.112 Lane2 P0 and P1 Preset-Coefficient Mapping (L2P0P1PCM)—Offset 540h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.113 Lane2 P1, P2 and P3 Preset-Coefficient Mapping (L2P1P2P3PCM)—Offset 544h

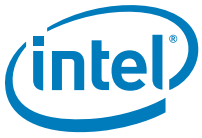
This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.114 Lane2 P3 and P4 Preset-Coefficient Mapping (L2P3P4PCM)—Offset 548h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.115 Lane2 P5 and P6 Preset-Coefficient Mapping (L2P5P6PCM)—Offset 54Ch

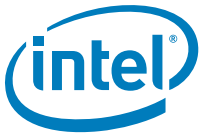
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.116 Lane2 P6, P7 and P8 Preset-Coefficient Mapping (L2P6P7P8PCM)—Offset 550h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.117 Lane2 P8 and P9 Preset-Coefficient Mapping (L2P8P9PCM)—Offset 554h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.118 Lane2 P10 Preset-Coefficient Mapping (L2P10PCM)—Offset 558h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.119 Lane2 LF and FS (L2LFFS)—Offset 55Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.120 Lane3 P0 and P1 Preset-Coefficient Mapping (L3P0P1PCM)—Offset 560h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.121 Lane3 P1, P2 and P3 Preset-Coefficient Mapping (L3P1P2P3PCM)—Offset 564h

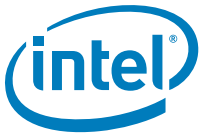
This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.122 Lane3 P3 and P4 Preset-Coefficient Mapping (L3P3P4PCM)—Offset 568h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.123 Lane3 P5 and P6 Preset-Coefficient Mapping (L3P5P6PCM)—Offset 56Ch

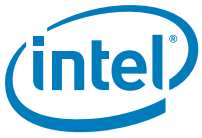
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.124 Lane3 P6, P7 and P8 Preset-Coefficient Mapping (L3P6P7P8PCM)—Offset 570h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.125 Lane3 P8 and P9 Preset-Coefficient Mapping (L3P8P9PCM)—Offset 574h

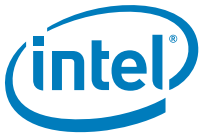
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.126 Lane3 P10 Preset-Coefficient Mapping (L3P10PCM)—Offset 578h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.127 Lane3 LF and FS (L3LFFS)—Offset 57Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.128 Lane3 LF and FS (L3LFFS)—Offset 57Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.1.129 PCLKD_L1TREF_CFG—Offset 1010h

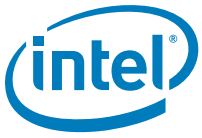
CR delay timer count for L1 tref.

Access Method

Type: CR Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Range	Access Type	Default (reset)	Description
31:16	RW	0x0 (rst)	**RESERVED (RESERVED)**



Range	Access Type	Default (reset)	Description
15:12	RW	0x0 (rst)	**TclkReqSRC3 (TclkReqSRC3)** Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC3 ungated (TclkreqSRC3): Minimum elapsed time from the Effective Mapped CLKREQ# signal assertion to the corresponding PCIe SRC Clock being allowed to toggle. This minimum time of CLKOUT_SRCn[P/N] staying gated at low voltage allows for the PCIe device's voltage rail to ramp to safe level on the exit from L1Off state before being driven with clock from the PCH. 0000: 0us minimum elapsed time from Effective Mapped CLKREQ# assertion to corresponding CLKOUT_SRCn ungated Default This setting is for PCIe device that does not support L1Off. This setting must also be used when corresponding CLKOUT_SRCn is configured for non-PCIe clock use, i.e. as MEX reference clock, etc. 0001: 5us minimum elapsed time ... 0010: 10us minimum elapsed time ... 0011: 15us minimum elapsed time ... 0100: 20us minimum elapsed time ... 0101: 25us minimum elapsed time ... 0110: 30us minimum elapsed time ... 0111: 35us minimum elapsed time ... 1000: 40us minimum elapsed time ... 1001: 45us minimum elapsed time ... 1010: 50us minimum elapsed time ... 1011: 60us minimum elapsed time ... 1100: 70us minimum elapsed time ... 1101: 80us minimum elapsed time ... 1110: 90us minimum elapsed time ... 1111: 100us minimum elapsed time .
11:8	RW	0x0 (rst)	**TclkReqSRC2 (TclkReqSRC2)** Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC2 ungated (TclkreqSRC2): Minimum elapsed time from the Effective Mapped CLKREQ# signal assertion to the corresponding PCIe SRC Clock being allowed to toggle. This minimum time of CLKOUT_SRCn[P/N] staying gated at low voltage allows for the PCIe device's voltage rail to ramp to safe level on the exit from L1Off state before being driven with clock from the PCH. 0000: 0us minimum elapsed time from Effective Mapped CLKREQ# assertion to corresponding CLKOUT_SRCn ungated Default This setting is for PCIe device that does not support L1Off. This setting must also be used when corresponding CLKOUT_SRCn is configured for non-PCIe clock use, i.e. as MEX reference clock, etc. 0001: 5us minimum elapsed time ... 0010: 10us minimum elapsed time ... 0011: 15us minimum elapsed time ... 0100: 20us minimum elapsed time ... 0101: 25us minimum elapsed time ... 0110: 30us minimum elapsed time ... 0111: 35us minimum elapsed time ... 1000: 40us minimum elapsed time ... 1001: 45us minimum elapsed time ... 1010: 50us minimum elapsed time ... 1011: 60us minimum elapsed time ... 1100: 70us minimum elapsed time ... 1101: 80us minimum elapsed time ... 1110: 90us minimum elapsed time ... 1111: 100us minimum elapsed time .

Range	Access Type	Default (reset)	Description
7:4	RW	0x0 (rst)	**TclkReqSRC1 (TclkReqSRC1)** Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC1 ungated (TclkreqSRC1): Minimum elapsed time from the Effective Mapped CLKREQ# signal assertion to the corresponding PCIe SRC Clock being allowed to toggle. This minimum time of CLKOUT_SRCn[P/N] staying gated at low voltage allows for the PCIe device's voltage rail to ramp to safe level on the exit from L1Off state before being driven with clock from the PCH. 0000: 0us minimum elapsed time from Effective Mapped CLKREQ# assertion to corresponding CLKOUT_SRCn ungated Default This setting is for PCIe device that does not support L1Off. This setting must also be used when corresponding CLKOUT_SRCn is configured for non-PCIe clock use, i.e. as MEX reference clock, etc. 0001: 5us minimum elapsed time ... 0010: 10us minimum elapsed time ... 0011: 15us minimum elapsed time ... 0100: 20us minimum elapsed time ... 0101: 25us minimum elapsed time ... 0110: 30us minimum elapsed time ... 0111: 35us minimum elapsed time ... 1000: 40us minimum elapsed time ... 1001: 45us minimum elapsed time ... 1010: 50us minimum elapsed time ... 1011: 60us minimum elapsed time ... 1100: 70us minimum elapsed time ... 1101: 80us minimum elapsed time ... 1110: 90us minimum elapsed time ... 1111: 100us minimum elapsed time .
3:0	RW	0x0 (rst)	**TclkReqSRC0 (TclkReqSRC0)** Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC0 ungated (TclkreqSRC0): Minimum elapsed time from the Effective Mapped CLKREQ# signal assertion to the corresponding PCIe SRC Clock being allowed to toggle. This minimum time of CLKOUT_SRCn[P/N] staying gated at low voltage allows for the PCIe device's voltage rail to ramp to safe level on the exit from L1Off state before being driven with clock from the PCH. 0000: 0us minimum elapsed time from Effective Mapped CLKREQ# assertion to corresponding CLKOUT_SRCn ungated Default This setting is for PCIe device that does not support L1Off. This setting must also be used when corresponding CLKOUT_SRCn is configured for non-PCIe clock use, i.e. as MEX reference clock, etc. 0001: 5us minimum elapsed time ... 0010: 10us minimum elapsed time ... 0011: 15us minimum elapsed time ... 0100: 20us minimum elapsed time ... 0101: 25us minimum elapsed time ... 0110: 30us minimum elapsed time ... 0111: 35us minimum elapsed time ... 1000: 40us minimum elapsed time ... 1001: 45us minimum elapsed time ... 1010: 50us minimum elapsed time ... 1011: 60us minimum elapsed time ... 1100: 70us minimum elapsed time ... 1101: 80us minimum elapsed time ... 1110: 90us minimum elapsed time ... 1111: 100us minimum elapsed time .

17.2 Registers Summary

Table 17-2. Summary of pcie_cfg Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4h	7h	Device Command; Primary Status (CMD_PSTS)—Offset 4h	100000h
8h	Bh	Revision ID;Class Code (RID_CC)—Offset 8h	60400F0h

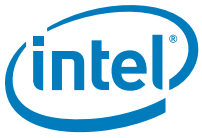


Table 17-2. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
Ch	Fh	Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch	810000h
18h	1Bh	Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h	0h
1Ch	1Fh	I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch	0h
20h	23h	Memory Base and Limit (MBL)—Offset 20h	0h
24h	27h	Prefetchable Memory Base and Limit (PMBL)—Offset 24h	10001h
28h	2Bh	Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h	0h
2Ch	2Fh	Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch	0h
34h	37h	Capabilities List Pointer (CAPP)—Offset 34h	40h
3Ch	3Fh	Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch	0h
40h	43h	Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h	428010h
44h	47h	Device Capabilities (DCAP)—Offset 44h	8001h
48h	4Bh	Device Control; Device Status (DCTL_DSTS)—Offset 48h	100000h
4Ch	4Fh	Link Capabilities (LCAP)—Offset 4Ch	710C00h
50h	53h	Link Control; Link Status (LCTL_LSTS)—Offset 50h	10000h
54h	57h	Slot Capabilities (SLCAP)—Offset 54h	40060h
58h	5Bh	Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h	0h
5Ch	5Fh	Root Control (RCTL)—Offset 5Ch	0h
60h	63h	Root Status (RSTS)—Offset 60h	0h
64h	67h	Device Capabilities 2 (DCAP2)—Offset 64h	80837h
68h	6Bh	Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h	0h
6Ch	6Fh	Link Capabilities 2 (LCAP2)—Offset 6Ch	0h
70h	73h	Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h	0h
74h	77h	Slot Capabilities 2 (SLCAP2)—Offset 74h	0h
78h	7Bh	Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h	0h
80h	83h	Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h	9005h
88h	8Bh	Message Signaled Interrupt Message Data (MD)—Offset 88h	0h
90h	93h	Subsystem Vendor Capability (SVCAP)—Offset 90h	A00Dh
94h	97h	Subsystem Vendor IDs (SVID)—Offset 94h	0h
A0h	A3h	Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h	C8030001h
A4h	A7h	PCI Power Management Control And Status (PMCS)—Offset A4h	8h
100h	103h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	0h
104h	107h	Uncorrectable Error Status (UES)—Offset 104h	0h
108h	10Bh	Uncorrectable Error Mask (UEM)—Offset 108h	0h
10Ch	10Fh	Uncorrectable Error Severity (UEV)—Offset 10Ch	60011h
110h	113h	Correctable Error Status (CES)—Offset 110h	0h
114h	117h	Correctable Error Mask (CEM)—Offset 114h	2000h
118h	11Bh	Advanced Error Capabilities and Control (AECC)—Offset 118h	0h
11Ch	11Fh	Header Log DW1 (HL_DW1)—Offset 11Ch	0h

Table 17-2. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
120h	123h	Header Log DW2 (HL_DW2)—Offset 120h	0h
124h	127h	Header Log DW3 (HL_DW3)—Offset 124h	0h
128h	12Bh	Header Log DW4 (HL_DW4)—Offset 128h	0h
12Ch	12Fh	Root Error Command (REC)—Offset 12Ch	0h
134h	137h	Error Source Identification (ESID)—Offset 134h	0h
140h	143h	ACS Extended Capability Header (ACSECH)—Offset 140h	0h
144h	147h	ACS Capability Register (ACSCAPR)—Offset 144h	Fh
148h	14Bh	ACS Control Register (ACSCTLR)—Offset 148h	0h
150h	153h	PTM Extended Capability Header (PTMECH)—Offset 150h	0h
154h	157h	PTM Capability Register (PTMCAPR)—Offset 154h	400h
158h	15Bh	PTM Control Register (PTMCTLR)—Offset 158h	0h
200h	203h	L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h	0h
204h	207h	L1 Sub-States Capabilities (L1SCAP)—Offset 204h	28281Fh
208h	20Bh	L1 Sub-States Control 1 (L1SCTL1)—Offset 208h	0h
20Ch	20Fh	L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch	28h
220h	223h	Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h	0h
224h	227h	Link Control 3 (LCTL3)—Offset 224h	0h
228h	22Bh	Lane Error Status (LES)—Offset 228h	0h
22Ch	22Fh	Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch	7F7F7F7Fh
230h	233h	Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h	7F7F7F7Fh
300h	303h	PCI Express Replay Timer Policy 1 (PCIERTP1)—Offset 300h	A64F96h
304h	307h	PCI Express Replay Timer Policy 2 (PCIERTP2)—Offset 304h	1BC00B86h
328h	32Bh	PCI Express Status 1 (PCIESTS1)—Offset 328h	0h
32Ch	32Fh	PCI Express Status 2 (PCIESTS2)—Offset 32Ch	0h
330h	333h	PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h	2A000016h
334h	337h	PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h	4ABCB5BCh
390h	393h	PTM Propagation Delay (PTMPD)—Offset 390h	0h
394h	397h	PTM Lower Local Master Time (PTMLLMT)—Offset 394h	0h
398h	39Bh	PTM Upper Local Master Time (PTMULMT)—Offset 398h	0h
39Ch	39Fh	PTM Pipe Stage Delay Configuration 1 (PTMPSDC1)—Offset 39Ch	0h
3A0h	3A3h	PTM Pipe Stage Delay Configuration 2 (PTMPSDC2)—Offset 3A0h	0h
3A4h	3A7h	PTM Pipe Stage Delay Configuration 3 (PTMPSDC3)—Offset 3A4h	0h
3A8h	3ABh	PTM Pipe Stage Delay Configuration 4 (PTMPSDC4)—Offset 3A8h	0h
3ACh	3AFh	PTM Pipe Stage Delay Configuration 5 (PTMPSDC5)—Offset 3ACh	0h
3B0h	3B3h	PTM Extended Config (PTMECFG)—Offset 3B0h	0h
3B4h	3B7h	PTM Lower T2 Time Stamp (PTMLT2TSTMP)—Offset 3B4h	0h
3B8h	3BBh	PTM Upper T2 Time Stamp (PTMUT2TSTMP)—Offset 3B8h	0h
414h	417h	Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h	0h

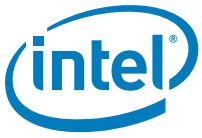


Table 17-2. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
418h	41Bh	Thermal and Power Throttling (TNPT)—Offset 418h	930h
41Ch	41Fh	Dynamic Lane Switch (DYNLNSW)—Offset 41Ch	0h
428h	42Bh	Power Control Enable (PCE)—Offset 428h	9h
42Ch	42Fh	PGCB Control1 (PGCBCTL1)—Offset 42Ch	14155555h
430h	433h	PGCB Control2 (PGCBCTL2)—Offset 430h	54h
450h	453h	Equalization Configuration 1 (EQCFG1)—Offset 450h	3102h
454h	457h	Remote Transmitter Preset Coefficient List 1 (RTPCL1)—Offset 454h	0h
458h	45Bh	Remote Transmitter Preset Coefficient List 2 (RTPCL2)—Offset 458h	0h
45Ch	45Fh	Remote Transmitter Preset Coefficient List 3 (RTPCL3)—Offset 45Ch	0h
460h	463h	Remote Transmitter Preset Coefficient List 4 (RTPCL4)—Offset 460h	0h
464h	467h	Figure Of Merit Status (FOMS)—Offset 464h	0h
468h	46Bh	Hardware Autonomous Equalization Control (HAEQ)—Offset 468h	A0080E00h
470h	473h	Local Transmitter Coefficient Override 1 (LTCO1)—Offset 470h	0h
474h	477h	Local Transmitter Coefficient Override 2 (LTCO2)—Offset 474h	0h
478h	47Bh	GEN3 L0s Control (G3L0SCTL)—Offset 478h	C00281Eh
47Ch	47Fh	Equalization Configuration 2 (EQCFG2)—Offset 47Ch	A001h
480h	483h	Monitor Mux (MM)—Offset 480h	0h
500h	503h	Lane0 P0 and P1 Preset-Coefficient Mapping (L0P0P1PCM)—Offset 500h	0h
504h	507h	Lane0 P1, P2 and P3 Preset-Coefficient Mapping (L0P1P2P3PCM)—Offset 504h	0h
508h	50Bh	Lane0 P3 and P4 Preset-Coefficient Mapping (L0P3P4PCM)—Offset 508h	0h
50Ch	50Fh	Lane0 P5 and P6 Preset-Coefficient Mapping (L0P5P6PCM)—Offset 50Ch	0h
510h	513h	Lane0 P6, P7 and P8 Preset-Coefficient Mapping (L0P6P7P8PCM)—Offset 510h	0h
514h	517h	Lane0 P8 and P9 Preset-Coefficient Mapping (L0P8P9PCM)—Offset 514h	0h
518h	51Bh	Lane0 P10 Preset-Coefficient Mapping (L0P10PCM)—Offset 518h	0h
51Ch	51Fh	Lane0 LF and FS (L0LFFS)—Offset 51Ch	0h
520h	523h	Lane1 P0 and P1 Preset-Coefficient Mapping (L1P0P1PCM)—Offset 520h	0h
524h	527h	Lane1 P1, P2 and P3 Preset-Coefficient Mapping (L1P1P2P3PCM)—Offset 524h	0h
528h	52Bh	Lane1 P3 and P4 Preset-Coefficient Mapping (L1P3P4PCM)—Offset 528h	0h
52Ch	52Fh	Lane1 P5 and P6 Preset-Coefficient Mapping (L1P5P6PCM)—Offset 52Ch	0h
530h	533h	Lane1 P6, P7 and P8 Preset-Coefficient Mapping (L1P6P7P8PCM)—Offset 530h	0h
534h	537h	Lane1 P8 and P9 Preset-Coefficient Mapping (L1P8P9PCM)—Offset 534h	0h
538h	53Bh	Lane1 P10 Preset-Coefficient Mapping (L1P10PCM)—Offset 538h	0h
53Ch	53Fh	Lane1 LF and FS (L1LFFS)—Offset 53Ch	0h
540h	543h	Lane2 P0 and P1 Preset-Coefficient Mapping (L2P0P1PCM)—Offset 540h	0h
544h	547h	Lane2 P1, P2 and P3 Preset-Coefficient Mapping (L2P1P2P3PCM)—Offset 544h	0h
548h	54Bh	Lane2 P3 and P4 Preset-Coefficient Mapping (L2P3P4PCM)—Offset 548h	0h
54Ch	54Fh	Lane2 P5 and P6 Preset-Coefficient Mapping (L2P5P6PCM)—Offset 54Ch	0h

Table 17-2. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
550h	553h	Lane2 P6, P7 and P8 Preset-Coefficient Mapping (L2P6P7P8PCM)—Offset 550h	0h
554h	557h	Lane2 P8 and P9 Preset-Coefficient Mapping (L2P8P9PCM)—Offset 554h	0h
558h	55Bh	Lane2 P10 Preset-Coefficient Mapping (L2P10PCM)—Offset 558h	0h
55Ch	55Fh	Lane2 LF and FS (L2LFFS)—Offset 55Ch	0h
560h	563h	Lane3 P0 and P1 Preset-Coefficient Mapping (L3P0P1PCM)—Offset 560h	0h
564h	567h	Lane3 P1, P2 and P3 Preset-Coefficient Mapping (L3P1P2P3PCM)—Offset 564h	0h
568h	56Bh	Lane3 P3 and P4 Preset-Coefficient Mapping (L3P3P4PCM)—Offset 568h	0h
56Ch	56Fh	Lane3 P5 and P6 Preset-Coefficient Mapping (L3P5P6PCM)—Offset 56Ch	0h
570h	573h	Lane3 P6, P7 and P8 Preset-Coefficient Mapping (L3P6P7P8PCM)—Offset 570h	0h
574h	577h	Lane3 P8 and P9 Preset-Coefficient Mapping (L3P8P9PCM)—Offset 574h	0h
578h	57Bh	Lane3 P10 Preset-Coefficient Mapping (L3P10PCM)—Offset 578h	0h
57Ch	57Fh	Lane3 LF and FS (L3LFFS)—Offset 57Ch	0h

17.2.1 Device Command; Primary Status (CMD_PSTS)—Offset 4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**DPE - Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if CMD.PERE is not set.
30	0h RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
26:25	0h RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved per PCI-Express spec
24	0h RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and CMD.PERE is set.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**Primary Fast Back to Back Capable (PFBC):** Reserved per PCI-Express spec.
22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Primary 66 MHz Capable (PC66):** Reserved per PCI-Express spec.
20	1h RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list.
19	0h RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID.
18:16	0h RO	**Reserved (RSVD_1):** Reserved
15:11	0h RO	**Reserved (RSVD_2):** Reserved
10	0h RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec.
8	0h RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0h RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec.
6	0h RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** Reserved per PCI-Express spec.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec.
3	0h RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0h RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0h RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone..

17.2.2 Revision ID;Class Code (RID_CC)—Offset 8h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 60400F0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	6h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	4h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h.
15:8	0h RO/V	**Programming Interface (PI):** The value reported in this register is a function of the Decode Control.Subtractive Decode Enable (SDE) register. SDE Value reported in this register 0: 00h 1: 01h
7:0	F0h RO/V	**Revision ID (RID):** Indicates the revision of the bridge.

17.2.3 Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 810000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved
23	1h RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device.
22:16	1h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h.
15:11	0h RO	**Latency Count (CT):** Reserved per PCI-Express spec
10:8	0h RO	**Reserved (RSVD_1):** Reserved
7:0	0h RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec

17.2.4 Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V2	**Secodary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	0h RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.
15:8	0h RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port.
7:0	0h RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

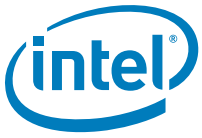
17.2.5 I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
30	0h RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with 'Unsupported Request' status from the device.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with 'Completion Abort' status from the device.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with 'Completion Abort' status to the device.
26:25	0h RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.
23	0h RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec
20:16	0h RO	**Reserved (RSVD_1):** Reserved
15:12	0h RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing.



17.2.6 Memory Base and Limit (MBL)—Offset 20h

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is MB [gt]= AD[lb]31:20[rb] [lt]= ML.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	0h RO	**Reserved (RSVD):** Reserved
15:4	0h RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	0h RO	**Reserved (RSVD_1):** Reserved

17.2.7 Prefetchable Memory Base and Limit (PMBL)—Offset 24h

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB [gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 10001h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing.
15:4	0h RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.

Bit Range	Default & Access	Field Name (ID): Description
3:0	1h RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing.

17.2.8 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.

17.2.9 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

17.2.10 Capabilities List Pointer (CAPP)—Offset 34h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 40h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved
7:0	40h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) OffsetCapability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI) 90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List OffsetCapability Next Pointer 100h Advanced Error Reporting 000h

17.2.11 Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch

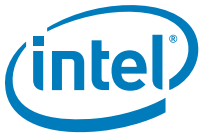
Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD):** Reserved
27	0h RW/V2	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
26	0h RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set.
25	0h RW/V2	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW/V2	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
23	0h RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec.
22	0h RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port.
21	0h RW/V2	**Master Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
20	0h RW	**VGA 16-Bit Decode (V16):** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.
19	0h RW	**VGA Enable (VE):** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h 3BBh and 3C0h 3DFh, and all aliases of bits 15:10 in any combination of 1's
18	0h RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
17	0h RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
16	0h RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG register in chipset config space: Port Bits[lb]15:12[rb] Bits[lb]11:08[rb] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP 4 0h STRPFUSECFG.P4IP 5 0h STRPFUSECFG.P5IP 6 0h STRPFUSECFG.P6IP 7 0h STRPFUSECFG.P7IP 8 0h STRPFUSECFG.P8IP The value that is programmed into STRPFUSECFG.PxIP is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above.
7:0	0h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

17.2.12 Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 428010h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved
30	0h RO	**Reserved (RSVD_1):** Reserved. This register at one time was for TCS Routing but that was later removed from the PCIe 2.0 spec
29:25	0h RO	**Interrupt Message Number (IMN):** The root port does not have multiple MSI interrupt numbers.
24	0h RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
23:20	4h RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port

Bit Range	Default & Access	Field Name (ID): Description
19:16	2h RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 specification which incorporates the Register Expansion ECN.
15:8	80h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h RO	**Capability ID (CID):** Indicates this is a PCI Express capability

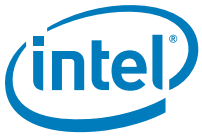
17.2.13 Device Capabilities (DCAP)—Offset 44h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 8001h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD):** Reserved
28	0h RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports
27:26	0h RO	**Captured Slot Power Limit Scale (CSPS):** Not supported
25:18	0h RO	**Captured Slot Power Limit Value (CSPV):** Not supported
17:16	0h RO	**Reserved (RSVD_1):** Reserved
15	1h RO	**Role Based Error Reporting (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.
14	0h RO	**Reserved (RSVD_2):** Reserved. On previous version of the specification this was Power Indicator Present (PIP)
13	0h RO	**Reserved (RSVD_3):** Reserved. On previous version of the specification this was Attention Indicator Present (AIP)



Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**Reserved (RSVD_4):** Reserved. On previous version of the specification this was Attention Button Present (ABP)
11:9	0h RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports.
8:6	0h RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port.
5	0h RO	**Extended Tag Field Supported (ETFS):** The root port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	0h RO	**Phantom Functions Supported (PFS):** No phantom functions supported
2:0	1h RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Only Max Payload Size of up to 256B is supported. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface.

17.2.14 Device Control; Device Status (DCTL_DSTS)—Offset 48h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
20	1h RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
18	0h RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp
17	0h RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout
16	0h RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout.
15	0h RO	**Reserved (RSVD_1):** Reserved
14:12	0h RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface.
11	0h RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.
10	0h RW/P	**Aux Power PM Enable (APME):** The OS will set this bit to '1' if the device connected has detected aux power.
9	0h RO	**Phantom Functions Enable (PFE):** Not supported
8	0h RO	**Extended Tag Field Enable (ETFE):** Not supported
7:5	0h RW	**Max Payload Size (MPS):** The root port only supports up to 256B max payload. Programming this field to any values other than 128B or 256B max payload size will result in aliasing to 128B max payload size. If the DCAP.MPS indicates 128B max payload size support, programming this field to any values other than 128B will result in aliasing to 128B max payload size. Programming this field to any values greater than DCAP.MPS will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME.
4	0h RO	**Enable Relaxed Ordering (ERO):** Not supported

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0h RW	**Fatal Error Reporting Enable (FEE):** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0h RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0h RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

17.2.15 Link Capabilities (LCAP)—Offset 4Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 710C00h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h
23	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
22	1h RW/O	**ASPM Optionality Compliance (ASPMOC):** ASPM Optionality Compliance (ASPMOC): This bit must be set to 1b for PCIe 3.0 compliant port. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests.
21	1h RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1h RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0h RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the root port does not support Surprise Down Error Reporting
18	0h RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism.
17:15	2h RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b Less than 1 us 001b 1 us to less than 2 us 010b 2 us to less than 4 us 011b 4 us to less than 8 us 100b 8 us to less than 16 us 101b 16 us to less than 32 us 110b 32 us to 64 us 111b More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency.
14:12	0h RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL

Bit Range	Default & Access	Field Name (ID): Description
11:10	3h RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 No ASPM Supported 01 L0s Supported 10 L1 Supported 11 L0s and L1 supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is '01'. Otherwise, the default of this field is '11'. If STRPFUSECFG.ASPMDIS is 1, BIOS writing '11' to this field will have the same effect as writing '01'. '01' will be reflected on this register when read and the register will turn to Read-Only once written once.
9:4	0h RO/V	**Maximum Link Width (MLW):** For the root ports, several values can be taken, based upon the value of the chipset configuration register field RPC.PC1 for ports 1-4: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RO/V	**Max Link Speeds (MLS):** Indicates the supported link speeds of the Root Port. 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5GT/s Link speeds supported This register reports a value of 0001b if the Root Port Gen2 Disable Fuse is set or the MPC.PCIEGEN2DIS bit is set, else this register reports a value of 0010b. Max Link Speeds (MLS): This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. This register reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through Fuse or MPC.PCIESD register. This register reports a value of 0010b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through Fuse or MPC.PCIESD register.

17.2.16 Link Control; Link Status (LCTL_LSTS)—Offset 50h

Access Method

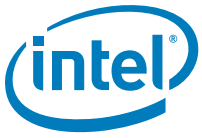
Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
29	0h RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.
28	0h RO/V	**Slot Clock Configuration (SCC):** In normal mode, root port uses the same reference clock as on the platform and does not generate its own clock. Note: The default of this register bit is dependent on the 'PCIe Non-Common Clock With SSC Mode Enable Strap'. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'.
27	0h RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
26	0h RO	**Reserved (RSVD):** Reserved. Previously this was defined as Link Training Error (LTE) but support for this bit was removed from subsequent versions of the PCI Express specification.
25:20	0h RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained.

Bit Range	Default & Access	Field Name (ID): Description
19:16	1h RO/V	**Current Link Speed (CLS):** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link This field indicates the negotiated Link speed of the given link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. The value of this field is undefined if the link is not up.
15:12	0h RO	**Reserved (RSVD_1):** Reserved
11	0h RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.
10	0h RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.
9	0h RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. Note: When operating as PCI Express, this bit defines the value of the Link Upconfigure Capability in TS2 Ordered Sets.
8	0h RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on Root Ports.
7	0h RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. Note: This functionality is not applicable for Mobile Express.
6	0h RW	**Common Clock Configuration (CCC):** When set, indicates that the root port and device are operating with a distributed common reference clock.



Bit Range	Default & Access	Field Name (ID): Description
5	0h WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0h RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state.
3	0h RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0h RO	**Reserved (RSVD_2):** Reserved
1:0	0h RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see '00' as an output from this register. BIOS reading this register should always return the correct value.

17.2.17 Slot Capabilities (SLCAP)—Offset 54h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 40060h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/O	**Physical Slot Number (PSN__31_24):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
23:19	0h RW/O	**Physical Slot Number (PSN__23_19):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.

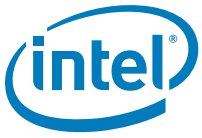
Bit Range	Default & Access	Field Name (ID): Description
18	1h RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0h RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented.
16:15	0h RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:8	0h RW/O	**Slot Power Limit Value (SLV__14_8):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
7	0h RW/O	**Slot Power Limit Value (SLV__7_7):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1h RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported.
5	1h RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification.
4	0h RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot.
3	0h RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot.
2	0h RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present
1	0h RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot
0	0h RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot.

17.2.18 Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved (RSVD):** Reserved
24	0h RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
23	0h RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock.
22	0h RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'.
21	0h RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented.
20	0h RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller..
19	0h RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the SLSTS.PDS bit changes state.
18	0h RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented.
17	0h RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented.
16	0h RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button
15:13	0h RO	**Reserved (RSVD_1):** Reserved
12	0h RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed
11	0h RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock.
10	0h RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug.
9:8	0h RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller..
7:6	0h RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller..
5	0h RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0h RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller..

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state.
2	0h RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller..
1	0h RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller...
0	0h RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller..

17.2.19 Root Control (RCTL)—Offset 5Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:4	0h RO	**Reserved (RSVD_1):** Reserved
3	0h RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set).
2	0h RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0h RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0h RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

17.2.20 Root Status (RSTS)—Offset 60h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17	0h RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. Root ports have a one deep PME pending queue.
16	0h RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0h RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

17.2.21 Device Capabilities 2 (DCAP2)—Offset 64h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 80837h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved (RSVD):** Reserved
19:18	2h RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported.
17:12	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/ disable the root port from declaring support for the LTR capability.
10:6	0h RO	**Reserved (RSVD_2):** Reserved
5	1h RO	**ARI Forwarding Supported (AFS):** ARI Forwarding Supported (AFS): Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. Note: This bit is not made RWO to simplify implementation, since there is a requirement that the ARI Forwarding Enable bit must be hardwired to 0b if ARI Forwarding Supported bit is 0b. It is low risk to keep this risk 1b.
4	1h RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	7h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C 0111b Ranges A, B [amp] C [lt]-- This is what PCH supports 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved.

17.2.22 Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15	0h RO	**Reserved (RSVD_1):** Reserved
14:13	0h RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** 00b Disable OBFF mechanism. 01b Enable OBFF mechanism using Message signaling (Variation A). 10b Enable OBFF mechanism using Message signaling (Variation B). 11b Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect.
12:11	0h RO	**Reserved (RSVD_2):** Reserved
10	0h RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:6	0h RO	**Reserved (RSVD_3):** Reserved
5	0h RW	**ARI Forwarding Enable (AFE):** ARI Forwarding Enable (AFE): When set, the Downstream Port disables its traditional Device Number field being 0b enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port.
4	0h RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The root port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 us to 100 us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either when this value was changed or when each request was issued.

17.2.23 Link Capabilities 2 (LCAP2)—Offset 6Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved (RSVD):** Reserved
22:16	0h RO	**Lower SKP OS Reception Supported Speeds Vector (LSOSRSS):** Lower SKP OS Reception Supported Speeds Vector(LSOSRSS): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
15:9	0h RO	**Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV):** Lower SKP OS Generation Supported Speeds Vector(LSOSGSSV): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
8	0h RO	**Crosslink Supported (CS):** Crosslink Supported (CS): No support for Crosslink.
7:1	0h RO/V	**Supported Link Speeds Vector (SLSV):** Supported Link Speeds Vector (SLSV): This field indicates the supported Link speed of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. Bit definitions within this field are: Bit 0: 2.5 GT/s. Bit 1: 5.0 GT/s. Bit 2: 8.0 GT/s. Bits 6:3: Reserved. This register reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through Fuse or MPC.PCIESD register. This register reports a value of 0011b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through Fuse or MPC.PCIESD register.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**Reserved (RSVD_1):** Reserved

17.2.24 Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h

Access Method

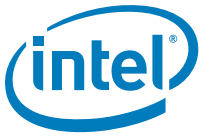
Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/1C/V/P	**Link Equalization Request (LER):** Link Equalization Request (LER): This bit is set by hardware to request the Link equalization process to be performed on the Link. Register Attribute: Dynamic.
20	0h RO/V/P	**Equalization Phase 3 Successful (EQP3S):** Equalization Phase 3 Successful (EQP3S): When set to 1, this bit indicates that Phase 3 of the Transmitter Equalization procedure has successfully completed.
19	0h RO/V/P	**Equalization Phase 2 Successful (EQP2S):** Equalization Phase 2 Successful (EQP2S): When set to 1, this bit indicates that Phase 2 of the Transmitter Equalization procedure has successfully completed.
18	0h RO/V/P	**Equalization Phase 1 Successful (EQP1S):** Equalization Phase 1 Successful (EQP1S): When set to 1, this bit indicates that Phase 1 of the Transmitter Equalization procedure has successfully completed.
17	0h RO/V/P	**Equalization Complete (EqC):** Equalization Complete (EC): When set to 1, this bit indicates that the Transmitter Equalization procedure has completed
16	0h RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/P	**Compliance Preset/De-emphasis (CD):** For 8.0 GT/s Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b -3.5 dB 0000b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. The default value of this field is 0000b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value.
11	0h RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only.
10	0h RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.

Bit Range	Default & Access	Field Name (ID): Description
9:7	0h RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0h RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5	0h RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds.



Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value.
3:0	0h RW/V/P	**Target Link Speed (TLS):** Target Link Speed (TLS): This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. If a value is written to this field that does not correspond to a supported speed, as indicated by the Supported Link Speeds Vector, the result is undefined. The default value of this field is GEN1. Note: This register field could be used by REUT software to limit the link speed to 2.5 GT/s or 5 GT/s data rate.

17.2.25 Slot Capabilities 2 (SLCAP2)—Offset 74h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved (RSVD):** Reserved

17.2.26 Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:0	0h RO	**Reserved (RSVD_1):** Reserved

17.2.27 Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 9005h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved
23	0h RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
22:20	0h RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
19:17	0h RO	**Multiple Message Capable (MMC):** Only one message is required.
16	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.

Bit Range	Default & Access	Field Name (ID): Description
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	5h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

17.2.28 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction.

17.2.29 Subsystem Vendor Capability (SVCAP)—Offset 90h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: A00Dh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

17.2.30 Subsystem Vendor IDs (SVID)—Offset 94h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

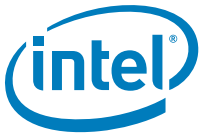
17.2.31 Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: C8030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	19h RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Microsoft operating systems to enable PME# in devices connected behind this root port.
26	0h RO	**D2_Support (D2S):** The D2 state is not supported.
25	0h RO	**D1_Support (D1S):** The D1 state is not supported.
24:22	0h RO	**Aux_Current (AC):** Reports 0mA (self-powered), as use of this controller does not add to suspect well power consumption.
21	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
20	0h RO	**Reserved (RSVD):** Reserved
19	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
18:16	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	1h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

17.2.32 PCI Power Management Control And Status (PMCS)—Offset A4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Data (DTA):** Reserved
23	0h RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification
22	0h RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification.
21:16	0h RO	**Reserved (RSVD):** Reserved
15	0h RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0h RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Microsoft operating systems to enable PME# on devices connected to this root port.
7:4	0h RO	**Reserved (RSVD_1):** Reserved
3	1h RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved (RSVD_2):** Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 D0 state 11 D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

17.2.33 Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h

Size:32 bits
The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list.
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

17.2.34 Uncorrectable Error Status (UES)—Offset 104h

This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/1C/V/P	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0h RW/1C/V/P	**Completor Abort Status (CA):** Indicates a completer abort was received

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Not supported.
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RO	**Training Error Status (TE):** Not supported.

17.2.35 Uncorrectable Error Mask (UEM)—Offset 108h

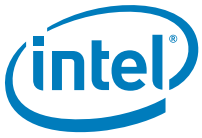
When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/P	**ACS Violation Mask (AVM):** Reserved. Access Control Services are not supported
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.



Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0h RW/P	**Completor Abort Mask (CM):** Mask for completer abort.
14	0h RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.
13	0h RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RO	**Training Error Mask (TE):** Not supported.

17.2.36 Uncorrectable Error Severity (UEV)—Offset 10Ch

This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 60011h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/P	**ACS Violation Severity (AVS):** Severity for ACS violation.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	1h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.

Bit Range	Default & Access	Field Name (ID): Description
17	1h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0h RW/P	**Completor Abort Severity (CA):** Severity for completer abort.
14	0h RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	1h RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation..

17.2.37 Correctable Error Status (CES)—Offset 110h

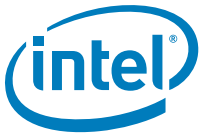
This register is only reset by a loss of core power

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved (RSVD):** Reserved
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	**Reserved (RSVD_1):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

17.2.38 Correctable Error Mask (CEM)—Offset 114h

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved (RSVD):** Reserved
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	**Reserved (RSVD_1):** Reserved
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.

Bit Range	Default & Access	Field Name (ID): Description
5:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

17.2.39 Advanced Error Capabilities and Control (AECC)—Offset 118h

This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved (RSVD):** Reserved
8	0h RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0h RO	**ECRC Check Capable (ECC):** ECRC is not supported.
6	0h RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0h RO	**ECRC Generation Capabile (EGC):** ECRC is not supported.
4:0	0h RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

17.2.40 Header Log DW1 (HL_DW1)—Offset 11Ch

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**1st dWord of TLP (DW1):** Byte0 [amp][amp] Byte1 [amp][amp] Byte2 [amp][amp] Byte3

17.2.41 Header Log DW2 (HL_DW2)—Offset 120h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**2nd dWord of TLP (DW2):** Byte4 [amp][amp] Byte5 [amp][amp] Byte6 [amp][amp] Byte7

17.2.42 Header Log DW3 (HL_DW3)—Offset 124h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**3rd dWord of TLP (DW3):** Byte8 [amp][amp] Byte9 [amp][amp] Byte10 [amp][amp] Byte11

17.2.43 Header Log DW4 (HL_DW4)—Offset 128h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**4th dWord of TLP (DW4):** Byte12 [amp][amp] Byte13 [amp][amp] Byte14 [amp][amp] Byte15

17.2.44 Root Error Command (REC)—Offset 12Ch

This register allows errors to generate interrupts.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved (RSVD):** Reserved
2	0h RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0h RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0h RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

17.2.45 Error Source Identification (ESID)—Offset 134h

Size:32 bits
Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set.
15:0	0h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set.

17.2.46 ACS Extended Capability Header (ACSECH)—Offset 140h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support ACS Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support ACS Extended Capability, BIOS should write a 000Dh to this register else it should write 0.

17.2.47 ACS Capability Register (ACSCAPR)—Offset 144h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: Fh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD_1):** Reserved for Egress Control Vector Size. This field is not applicable since ACS P2P Egress Control is not supported.
7	0h RO	**Reserved (RSVD_2):** Reserved
6	0h RO	**ACS Direct Translated P2P (T):** ACS Direct Translated P2P (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control (E):** ACS P2P Egress Control (E): ACS P2P Egress Control is not supported.
4	0h RO	**ACS Upstream Forwarding (U):** ACS Upstream Forwarding (U): ACS Upstream Forwarding is not supported.
3	1h RW/O	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Required for all Functions that support ACS P2P Request Redirect; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Completion Redirect.
2	1h RW/O	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Required for Root Ports that support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports; required for multi-function device Functions that support peer-to-peer traffic with other Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Request Redirect.
1	1h RW/O	**ACS Translation Blocking (B):** ACS Translation Blocking (B): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Translation Blocking.
0	1h RW/O	**ACS Source Validation (V):** ACS Source Validation (V): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Source Validation.

17.2.48 ACS Control Register (ACSCTLR)—Offset 148h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RSVD):** Reserved,
6	0h RO	**ACS Direct Translated P2P Enable (T):** ACS Direct Translated P2P Enable (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control Enable (E):** ACS P2P Egress Control Enable (E): ACS P2P Egress Control is not supported.
4	0h RO	**ACS Upstream Forwarding Enable (U):** ACS Upstream Forwarding Enable (U): ACS Upstream Forwarding is not supported.
3	0h RW	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Determines when the component redirects peer-to-peer Completions upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear.
2	0h RW	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Determines when the component redirects peer-to-peer memory Requests targeting another peer port upstream. I/O, Configuration, VDM Messages and Completions are never affected by ACS P2P Request Redirect.
1	0h RW	**ACS Translation Blocking (B):** ACS Translation Blocking (B): When set, the component blocks all upstream Memory Requests whose Address Translation (AT) field is not set to the default value. I/O, Configuration, Completions and Messages are never affected by ACS Translation Blocking.
0	0h RW	**ACS Source Validation (V):** ACS Source Validation (V): When set, the component validates the Bus Number from the Requester ID of upstream Requests against the secondary / subordinate Bus Numbers. I/O, Configuration and Completions are never affected by ACS Source Validation.

17.2.49 PTM Extended Capability Header (PTMECH)—Offset 150h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support PTM Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support PTM Extended Capability, BIOS should write a 001Fh to this register else it should write 0.

17.2.50 PTM Capability Register (PTMCAPR)—Offset 154h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 400h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved,
15:8	4h RW/O	**Local Clock Granularity (LCG):** Local Clock Granularity(LCG): 0000 0000b - Time Source does not implement a local clock. It simply propagates timing information obtained from further Upstream in the PTM Hierarchy when responding to PTM Request messages. 0000 0001b - 1111 1110b: Indicates the period of this Time Sources local clock in ns. 1111 1111b: Indicates the period of this Time Sources local clock is greater than 254 ns. If the PTM Root Select bit is Set, this local clock is used to provide PTM Master Time. Otherwise, the Time Source uses this local clock to locally track PTM Master Time received from further Upstream within a PTM Hierarchy.
7:3	0h RO	**Reserved (RSVD_1):** Reserved,
2	0h RW/O	**PTM Root Capable (PTMRC):** PTM Root Capable(PTMRC): Root Ports must set this bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW/O	**PTM Responder Capable (PTMRSPC):** PTM Responder Capable(PTMRSPC): Root Ports are permitted to set this bit to 1b to indicate that they implement the PTM Responder role.
0	0h RO	**PTM Requester Capable (PTMREQC):** PTM Requester Capable(PTMREQC): PTM Requester Role is not supported by Root Port.

17.2.51 PTM Control Register (PTMCTLR)—Offset 158h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:8	0h RO	**Effective Granularity (EG):** Effective Granularity(EG): Root Port does not support PTM Requester role.
7:2	0h RO	**Reserved (RSVD_1):** Reserved.
1	0h RW	**Root Select (RS):** Root Select(RS): When Set, if the PTM Enable bit is also Set, this Time Source is the PTM Root. Within each PTM Hierarchy, it is recommended that system software select only the furthest Upstream Time Source to be the PTM Root.
0	0h RW	**PTM Enable (PTME):** PTM Enable(PTME): When Set, this Function is permitted to participate in the PTM mechanism according to its selected role. Software must not have the PTM Enable bit Set in the PTM Control register on a Function associated with an Upstream Port unless the associated Downstream Port on the Link already has the PTM Enable bit Set in its associated PTM Control register. Register Attribute: Static.

17.2.52 L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h

Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 1h
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 001Eh. .

17.2.53 L1 Sub-States Capabilities (L1SCAP)—Offset 204h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 28281Fh

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
23:19	5h RW/O	**Port Tpower_on Value (PTV):** Along with the Port T_POWER_ON Scale Field in the L1 Substates Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF.
18	0h RO	**Reserved (RSVD_1):** Reserved.
17:16	0h RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Substates Capabilities register. '00b': 2 us '01b': 10 us '10b': 100 us '11b': Reserved Required for all Ports that support L1.OFF.
15:8	28h RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF.
7:5	0h RO	**Reserved (RSVD_2):** Reserved
4	1h RW/O	**L1 PM Substates Supported (L1PSS):** When Set this bit indicates that this Port supports L1 PM Substates. For compatibility with possible future extensions, software must not enable L1 PM Substates unless this bit is set. This RWO field must be programmed prior to enabling ASPM.
3	1h RW/O	**ASPM L1.1 Substates Supported (AL11S):** When set, this bit indicates that this port supports L1 substates for ASPM L1.SNOOZ. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
2	1h RW/O	**ASPM L1.2 Supported (AL12S):** When set, this bit indicates that ASPM_L1.OFF is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
1	1h RW/O	**PCI-PM L1.1 Supported (PPL11S):** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

Bit Range	Default & Access	Field Name (ID): Description
0	1h RW/O	**PCI-PM L1.2 Supported (PPL12S):** When set, this bit indicates that L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

17.2.54 L1 Sub-States Control 1 (L1SCTL1)—Offset 208h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**L1.2 LTR Threshold Latency ScaleValue (L12LTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe root port. The value in this field, together with L12LTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L12LTRSTLV times 1 ns 001: L12LTRSTLV times 32 ns 010: L12LTRSTLV times 1024 ns 011: L12LTRSTLV times 32768 ns 100: L12LTRSTLV times 1048576 ns 101: L12LTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
28:26	0h RO	**Reserved (RSVD):** Reserved
25:16	0h RW	**L1.2 LTR Threshold Latency Value (L12OFFLTRTLV):** This field contains the L1.2 LTR Threshold Latency Value for this particular PCIe root port. The value in this field, together with L12LTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
15:8	0h RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time the PCIe root port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved (RSVD_1):** Reserved
3	0h RW	**ASPM L1.1 Enabled (AL11E):** When set, this bit indicates that ASPM L1.SNOOZ substates are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic
2	0h RW	**ASPM L1.2 Enable (AL12E):** When set, this bit indicates that ASPM L1.OFF substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic
1	0h RW	**PCI-PM L1.SNOOZ Enable (PPL11E):** When set, this bit indicates that PCI-PM L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
0	0h RW	**PCI-PM L1.2 Enabled (PPL12E):** When set, this bit indicates that PCI-PM L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.

17.2.55 L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 28h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:3	5h RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# is sampled asserts in L1.OFF state. Tpower_on value is calculated by multiplying the value in this field by the value in the TPOS field. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
2	0h RO	**Reserved (RSVD_1):** Reserved
1:0	0h RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. '00b': 2 us '01b': 10 us '10b': 100us '11b': Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static

17.2.56 Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h

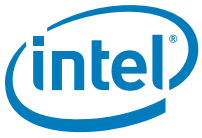
Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.



Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEECID):** PCI Express Extended Capability ID (PCIEECID): This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 0019h to this register else it should write 0.

17.2.57 Link Control 3 (LCTL3)—Offset 224h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:9	0h RO	**Enable Lower SKP OS Generation Vector (ELSOSGV):** Enable Lower SKP OS Generation Vector(ELSOSGV): When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is Set in this field and the corresponding bit in the Lower SKP OS Generation Supported Speeds Vector is not set.
8:2	0h RO	**Reserved (RSVD_1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Link Equalization Request Interrupt Enable (LERIE):** Link Equalization Request Interrupt Enable (LERIE): When set, this bit enables the generation of an interrupt to indicate that the Link Equalization Request bit has been set.
0	0h RW	**Perform Equalization (PE):** Perform Equalization (PE): When this bit is 1b and Link Retrain bit is set with the Target Link Speed field set to 8 GT/s, the Downstream Port must perform Link Equalization. This bit is cleared by Root Port upon entry to Link Equalization

17.2.58 Lane Error Status (LES)—Offset 228h

The Lane number is the default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD):** Reserved
3	0h RW/1C/V/P	**Lane 3 Error Status (L3ES):** Lane 3 Error Status (L3ES): Lane 3 detected a Lane-based error.
2	0h RW/1C/V/P	**Lane 2 Error Status (L2ES):** Lane 2 Error Status (L2ES): Lane 2 detected a Lane-based error.
1	0h RW/1C/V/P	**Lane 1 Error Status (L1ES):** Lane 1 Error Status (L1ES): Lane 1 detected a Lane-based error.
0	0h RW/1C/V/P	**Lane 0 Error Status (L0ES):** Lane 0 Error Status (L0ES): Lane 0 detected a Lane-based error.

17.2.59 Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 7F7F7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved.
30:28	7h RW	**Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH):** Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 1 Transmitter Preset (UPL1TP):** Upstream Port Lane 1 Transmitter Preset (UPL1TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	**Reserved (RSVD_1):** Reserved.
22:20	7h RW	**Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH):** Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 1 Transmitter Preset (DPL1TP):** Downstream Port Lane 1 Transmitter Preset (DPL1TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved (RSVD_2):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
14:12	7h RW	**Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH):** Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 0 Transmitter Preset (UPL0TP):** Upstream Port Lane 0 Transmitter Preset (UPL0TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	**Reserved (RSVD_3):** Reserved.
6:4	7h RW	**Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH):** Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 0 Transmitter Preset (DPL0TP):** Downstream Port Lane 0 Transmitter Preset (DPL0TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

17.2.60 Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 7F7F7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
30:28	7h RW	**Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH):** Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 3 Transmitter Preset (UPL3TP):** Upstream Port Lane 3 Transmitter Preset (UPL3TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	**Reserved (RSVD_1):** Reserved
22:20	7h RW	**Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH):** Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 3 Transmitter Preset (DPL3TP):** Downstream Port Lane 3 Transmitter Preset (DPL3TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved (RSVD_2):** Reserved
14:12	7h RW	**Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH):** Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 2 Transmitter Preset (UPL2TP):** Upstream Port Lane 2 Transmitter Preset (UPL2TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	**Reserved (RSVD_3):** Reserved
6:4	7h RW	**Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH):** Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
3:0	Fh RW	**Downstream Port Lane 2 Transmitter Preset (DPL2TP):** Downstream Port Lane 2 Transmitter Preset (DPL2TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

17.2.61 PCI Express Replay Timer Policy 1 (PCIERTP1)—Offset 300h

The Replay Timer controlled by the Replay Timeout field is started when the Retry Buffer is empty and a TLP is placed into it or an Ack/Nak DLLP is received and there are still non-acknowledged packets within the Retry Buffer. The counter continues to count until the next valid Ack DLLP or a NAK DLLP that acknowledges unacknowledged TLPs is received, or it reaches the timeout value specified by this register. When a valid Ack/Nak DLLP is received, the timer is reset to zero and restarted if there are still non-acknowledged packets within the Retry Buffer. Otherwise if the Retry Buffer is empty, the counter is just reset to zero. If the timer reaches the timeout value, the non-acknowledged packets within the Retry Buffer will be replayed.
The default for this register is dependant on the MAX_PAYLOAD_SIZE , the NEGOTIATED_WIDTH, and the NEGOTIATED_SPEED.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: A64F96h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved,
23:20	Ah RW	**Gen 2 x1 (G2X1):** Gen 2 x1 (G2X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 7) * 64 link clocks. For PCIE Gen 2 speed and x1 width For Mobile Express HS-Gear 3 speed and x1 width.

Bit Range	Default & Access	Field Name (ID): Description
19:16	6h RW	**Gen 2 x2 (G2X2):** Gen 2 x2 (G2X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 4) * 64 link clocks. For PCIe Gen 2 speed and x2 width. For Mobile Express HS-Gear 3 speed and x2 width.
15:12	4h RW	**Gen 2 x4 (G2X4):** Gen 2 x4 (G2X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 2 speed and x4 width. For Mobile Express HS-Gear 3 speed and x4 width.
11:8	Fh RW	**Gen 1 x1 (G1X1):** Gen 1 x1 (G1X1): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 10) * 64 link clocks. For 512B MPS: (nnn + 17) * 64 link clocks. For PCIe Gen 1 speed and x1 width. For Mobile Express HS-Gear 2 speed and x1 width.
7:4	9h RW	**Gen 1 x2 (G1X2):** Gen 1 x2 (G1X2): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For PCIe Gen 1 speed and x2 width. For Mobile Express HS-Gear 2 speed and x2 width.

Bit Range	Default & Access	Field Name (ID): Description
3:0	6h RW	**Gen 1 x4 (G1X4):** Gen 1 x4 (G1X4): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/ Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 1 speed and x4 width. For Mobile Express HS-Gear 2 speed and x4 width.

17.2.62 PCI Express Replay Timer Policy 2 (PCIERTP2)—Offset 304h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 1BC00B86h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Lane 0 Lane Number (L0LN):** Lane 0 Lane Number(L0LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 0 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
29:28	1h RW	**Lane 1 Lane Number (L1LN):** Lane 1 Lane Number(L1LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 1 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.

Bit Range	Default & Access	Field Name (ID): Description
27:26	2h RW	**Lane 2 Lane Number (L2LN):** Lane 2 Lane Number(L2LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 2 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
25:24	3h RW	**Lane 3 Lane Number (L3LN):** Lane 3 Lane Number(L3LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 3 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
23	1h RW	**Loopback Master EQ TS1 Enable (LMEQTS1E):** Loopback Master EQ TS1 Enable(LMEQTS1E): When set, the Loopback Master will use EQ TS1 Ordered Sets to direct the Loopback Slave into Loopback from Configuration.Linkwidth.Start. The Preset field of the EQ TS1 Ordered Sets will be specified by Upstream Port Lane X Transmitter Preset and Upstream Port Lane X Receiver Preset Hint fields in the Lane Equalization Control registers.
22	1h RW	**Loopback Master EQ Change Enable (LMEQCE):** Loopback Master EQ Change Enable(LMEQCE): This field is applicable to the case where Loopback is entered from Recovery state. When set, the Loopback Master will set the EC field of the GEN3 TS1 Ordered Sets to the appropriate value based on the ports direction(10b or 11b) to direct the Loopback Slave into Loopback from Recovery state. The Preset field of the GEN3 TS1 Ordered Sets will be specified by Upstream Port Lane X Transmitter Preset and Upstream Port Lane X Receiver Preset Hint fields in the Lane Equalization Control registers.
21:12	0h RO	**Reserved (RSVD):** Reserved
11:8	Bh RW	**Gen 3 x1 (G3X1):** Gen 3 x1 (G3X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For Gen 3 speed and x1 width

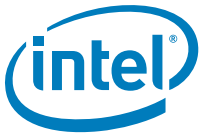
Bit Range	Default & Access	Field Name (ID): Description
7:4	8h RW	**Gen 3 x2 (G3X2):** Gen 3 x2 (G3X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For Gen 3 speed and x2 width
3:0	6h RW	**Gen 3 x4 (G3X4):** Gen 3 x4 (G3X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 1) * 64 link clocks. For 512B MPS: (nnn + 2) * 64 link clocks. For Gen 3 speed and x4 width

17.2.63 PCI Express Status 1 (PCIESTS1)—Offset 328h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LTSM State (LTSMSTATE):** Indicates the LTSM present state. Hex LTSSM States 00DETIDLE 01DETRDY 02DETIDLEP1TOP2 03DETRDYP2TOP1 04DETRDYINP1 05DETRDYINP1EXE 06DETP2POLLSTART 07DETP1POLLSTART 08DETP2TOP0 09DETP1TOP0 0AECPCMPRETRAIN 0BECPCMFAILP0TOP2 0CDETP0TOP2 0DPMODECHANGE 0EECPCMPCIE 0FECPCMUSB3 10DET2POLLINP0 11POLLINGACTIVE 12POLLINGCOMPLIANCEMARGINCNT 13POLLINGCOMPLIANCE 14POLLINGCOMPLIANCESPEEDUP 15POLLINGCOMPLIANCESPEEDDN 16POLLINGCOMPLIANCESPEEDTXEIDLE 17POLLINGCOMPLIANCESPEEDRXEIDLE 18POLLINGCOMPLIANCESPEED 19POLLINGCOMPLIANCESPEEDDONE 1APOLLINGCOMPLIANCEEXIT 1BPOLLINGCONFIGURATION 1CPOLLINGTXEIDLE 1DPOLLINGEND 1EPOLLINGENDWAIT 1FLINKWIDTHSTART 20LINKWIDTHACCEPT 21LANENUMWAIT 22LANENUMACCEPT 23LANEDESKEW 24CONFIGCOMPLETE 25CONFIGIDLE 26LWNEXITRECOVERY 27CONFIGLPBKENTRY 28CONFIGLPBKLWSTART 29CONFIGLPBKSPEEDTXEIDLE 2ACONFIGLPBKSPEEDSTART 2BCONFIGLPBKSPEEDRXEIDLE 2CCONFIGLPBKSPEED 2DCONFIGLPBKREUTSKIP 2ECONFIGLPBKREUT 2FCONFIGLPBKEXITM 30CONFIGLPBKTXEIDLE

Bit Range	Default & Access	Field Name (ID): Description
		31LWNEXIT 32LWNLNK2DETECT 33L0 34TXL0SRXL0 35RXL0STXL0 36TXL0SRXL0S 37L1TXEIDLE 38L1RCVEIDLE 39L1PREENTRY 3AL1ENTRY 3BL1IDLE 3CL1IDLEGEN2WAIT 3DL1EXIT 3EL2TXEIDLE 3FL2RCVEIDLE 40L2IDLEWAIT 41L2IDLERDY 42L2IDLE 43LOOPBACKENTRY 44LPBKACTIVEMTXSKP 45LPBKACTIVEMSKPDSKW 46LOOPBACKACTIVEM 47LPBKSLAVESPEEDTXEIDLE 48LPBKSLAVESPEEDRXEIDLE 49LPBKSLAVESPEED 4ALOOPBACKACTIVES 4BLOOPBACKCMMSKP 4CLOOPBACKCMM 4DLOOPBACKEXITM 4ELOOPBACKEXITS 4FLOOPBACKEXITL0 50LOOPBACKLNK2DETECT 51LOOPBACK2DETECT 52DISTX16TS1DIS 53DISTXEIDLE 54DISWAITSTART 55DISWAITGNT 56DISWAIT4TXMARGIN 57DISWAIT 58DIS2DETECT 59HOTRESETTS1 5AHOTRESETDONE 5BHOTRESETEIDLE 5CRECOVERYRCVRWAIT 5DRECOVERYRCVRMARGINCNT 5ERECOVERYRCVRLOCK 5FRECOVERYDESKEW 60RECOVERYRCVRCFG 61RECOVERYSPEED 62RECOVERYSPEEDTXEIDLE 63RECOVERYSPEEDRXEIDLE

Bit Range	Default & Access	Field Name (ID): Description
		64RECOVERYSPEEDREADY 65RECOVERYIDLE 66RECOVERYEXITDETECT 67RECOVERYLNK2DETECT 68RECOVERYEXITLPBK 69RECOVERYEXITL0 6ARECOVERYEXITDIS 6BRECOVERYEXITRST Note: This register field could be used by REUT software to monitor the link LTSSM substates.
23	0h RO	**Reserved (RSVD):** Reserved.
22:19	0h RO/V	**Link Status (LNKSTAT):** During Link initialization the Link will always traverse this list of state from the top (0000) to the bottom of the list (0111). One or more power management states may be skipped, but the direction of list traversal will remain the same. 0000 Link Down 0001 : Link Retrain 0011 : L1 0100 : L2 0101 : L3 0111 : L0 (Link Up) 1000 : L0s (Transmit [amp] Receive) 1001 : L0s (Transmit only) 1010 : L0s (Receive only) All others reserved
18:17	0h RO/V	**Replay Number (REPLAYNUM):** Number of times the Retry Buffer has been replayed since the last Link initialization / re-training. When the Data Link Layer has replayed the contents of the Retry Buffer four times a Link re-training will be initiated which will reset this value back to zero.
16	0h RO/V	**Data Link Layer Retry (DLLRETRY):** Indicates when the Data Link Layer has received a corrupted TLP or has detected a dropped packet and is currently waiting for the remote agent to re-transmit the corrupted/dropped packet. The value of Next Receive Sequence Number will be the sequence number associated with the corrupted packet.
15:12	0h RO/V	**Lane Status (LANESTAT):** Indicates which lanes are trained. A '1' indicates that the corresponding lane is trained (i.e. bit 0 = '1' means lane 0 is trained).
11:0	0h RO/V	**Next Transmitted Sequence Number (NXTTXSEQNUM):** This is the sequence number to be applied to and pre-pended to the next outgoing TLP.

17.2.64 PCI Express Status 2 (PCIESTS2)—Offset 32Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**PCIe Port 3 Non-Common Clock With SSC Mode Enable Strap (P3PNCCWSSCMES):** '0': PCIe port 3 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 3 is enabled to operate in non-common clock mode with SSC enabled.
30	0h RO/V	**PCIe Port 2 Non-Common Clock With SSC Mode Enable Strap (P2PNCCWSSCMES):** '0': PCIe port 2 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 2 is enabled to operate in non-common clock mode with SSC enabled.
29	0h RO/V	**PCIe Port 1 Non-Common Clock With SSC Mode Enable Strap (P1PNCCWSSCMES):** '0': PCIe port 1 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 1 is enabled to operate in non-common clock mode with SSC enabled.
28	0h RO/V	**PCIe Port 0 Non-Common Clock With SSC Mode Enable Strap (P0PNCCWSSCMES):** '0': PCIe port 0 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 0 is enabled to operate in non-common clock mode with SSC enabled.
27:16	0h RO/V	**Next Receive Sequence Number (NXTRCVSEQ):** This is the sequence number associated with the TLP that is expected to be received next.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/1C/V	**Cause of Last Recovery Event (CLRE):** Cause of Last Recovery Event (CLRE): This field logs the cause of the entry to Recovery from L0. Only the first cause of Recovery is captured, until the register is cleared. Encoding Recovery Event 0000 No Recovery. 0001 Recovery entry triggered by remote device. 0010 Link Layer initiated Link Retrain due to error. 0011 De-skew buffer full. 0100 L0s exit time-out. 0101 Elastic Buffer overrun/underrun. 0110 Triggered by speed change. 0111 Link upconfiguration/downconfiguration. 1000 L0 Electrical Idle Inference. 1001 Any of the Link Retrain, CMM Start, Hot Reset, Link Disable, REUT Loopback Master or REUT Forced Loopback Master bit set. 1010 Received EIOS for RXL0s entry when ASPM L0s is disabled. 1011 Entry to Recovery from RXL0s due to PME timeout. Others Reserved.
11:0	0h RO/V	**Last Acknowledged Sequence Number (LASTACKSEQNUM):** This is the sequence number associated with the last acknowledged TLP.

17.2.65 PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h

Note that selecting a lane number that does not exist for a port may result in undefined behavior.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 2A000016h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**GEN3 Intel CMM Scrambler Bypass (G3ICMMSB):** GEN3 Intel CMM Scrambler Bypass(G3ICMMSB): When set, the Intel CMM pattern will bypass scrambling in GEN3. This bit does not impact non Intel CMM pattern. The TSx and SOS prior to Intel CMM will still be scrambled normally. Note: This bit must be set prior to enabling Intel CMM, by setting the PCIECMMPC.START. Note: When operating in Mobile Express mode, this field is not applicable.
30	0h RO	**Reserved (RSVD):** Reserved
29	1h RW	**CMM Symbol[3] Select (SYM3SEL):** 0: selects CMM Symbol [lb]3[rb] to a control character 1: selects CMM Symbol [lb]3[rb] as a data character
28	0h RW	**CMM Symbol[2] Select (SYM2SEL):** 0: selects CMM Symbol [lb]2[rb] to a control character 1: selects CMM Symbol [lb]2[rb] as a data character
27	1h RW	**CMM Symbol[1] Select (SYM1SEL):** 0: selects CMM Symbol [lb]1[rb] to a control character 1: selects CMM Symbol [lb]1[rb] as a data character
26	0h RW	**CMM Symbol[0] Select (SYM0SEL):** 0: selects CMM Symbol [lb]0[rb] to a control character 1: selects CMM Symbol [lb]0[rb] as a data character
25:24	2h RW	**CMM Sync Header (CMMSH):** CMM Sync Header(CMMSH): Specifies the Sync Header for the Intel CMM pattern specified in PCIECMMSB. Note: Due to implementation limitation, only a value of 10b is supported. All the other values are not supported.
23:22	0h RO/V	**CMM Error Lane Number (ERRLANENUM):** This field contains the lane number of the failing lane. Only valid when CMM Error Detected is 1.
21:16	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO/V	**CMM Invert (INVERT):** Indicates which lanes are inverted 000: No inversion 001: Lanes 0 010: Lanes 1 011: Lanes 2 100: Lanes 3 This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated)
12:10	0h RO/V	**CMM Symbol Error Number Invert (SYMERRNUMINV):** Indicates which register number miscompared on the failing lane, if the failing lane was an inverted lane. Only valid when CMM Error Detected is 1. 000: CMM Data D0 001: CMM Data D0 010: CMM Data D0 011: CMM Data D1 100: CMM Data D2 101: CMM Data D3 110: CMM Data D0 111: CMM Data D0
9:8	0h RO/V	**CMM Symbol Error Number (SYMERRNUM):** Indicates which register number miscompared on the failing lane, if the failing lane was not inverted. Only valid when CMM Error Detected is 1. 00: CMM Data 0 01: CMM Data 1 10: CMM Data 2 11: CMM Data 3
7	0h RW/1C/V	**CMM Error Detected (ERRDET):** 1: An error was detected 0: No error detected Note: This bit will be shadowed to an observability pin that can be used for IRQ generation.
6:5	0h RW	**Select Lane Number to be inverted for CMM (SLNINVCMM):** Select Lane Number to be inverted for CMM
4	1h RW	**CMM AutoInvert (AUTOINVERT):** 1: CMM autosequences through the inversion 0: CMM does not sequence inversion
3	0h RO/V	**CMM Status (STAT):** This bit is set when the CMM Start bit is set and cleared when the CMM mode has been entered successfully. 0: Compliance Measurement Mode is not active or CMM mode has been entered successfully. 1: Set as a result of CMM Start bit being set.
2	1h RW	**CMM Invert Enable (INVEN):** 1: Enables the Inversion of the lane 0: Lane not inverted
1	1h RW	**Reserved (RSVD_2):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/L	**CMM Start (START):** 1: Start CMM 0: Stop CMM

17.2.66 PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 4ABCB5BCh

Bit Range	Default & Access	Field Name (ID): Description
31:24	4Ah RW	**CMM Data [3] (DATA3):** This character contains CMM Data [lb]3[rb] that will be transmitted on the link.
23:16	BCh RW	**CMM Data [2] (DATA2):** This character contains CMM Data [lb]2[rb] that will be transmitted on the link.
15:8	B5h RW	**CMM Data [1] (DATA1):** This character contains CMM Data [lb]1[rb] that will be transmitted on the link.
7:0	BCh RW	**CMM Data [0] (DATA0):** This character contains CMM Data [lb]0[rb] that will be transmitted on the link.

17.2.67 PTM Propagation Delay (PTMPD)—Offset 390h

Size:32 bits

Access Method

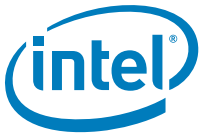
Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Propagation Delay Value (CPTMPDV):** Current PTM Propagation Delay Value(CPTMPDV): This field reports the current PTM Propagation Delay value captured from the last successful PTM dialog.

17.2.68 PTM Lower Local Master Time (PTMLLMT)—Offset 394h

Size:32 bits



Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Lower Local Master Time Value (CPTMLLMTV):** Current PTM Lower Local Master Time Value(CPTMLLMTV): This field reports the lower fields bits 31:0 of the Local TSC time value.

17.2.69 PTM Upper Local Master Time (PTMULMT)—Offset 398h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Upper Local Master Time Value (CPTMULMTV):** Current PTM Upper Local Master Time Value(CPTMULMTV): This field reports the upper fields bits 63:32 of the Local TSC time value.

17.2.70 PTM Pipe Stage Delay Configuration 1 (PTMPSDC1)—Offset 39Ch

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN1 X2 RX Pipe Stage Delay (G1X2RPSD):** GEN1 X2 RX Pipe Stage Delay(G1X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN1 X2 TX Pipe Stage Delay (G1X2TPSD):** GEN1 X2 TX Pipe Stage Delay(G1X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN1 X1 RX Pipe Stage Delay (G1X1RPSD):** GEN1 X1 RX Pipe Stage Delay(G1X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN1 X1 TX Pipe Stage Delay (G1X1TPSD):** GEN1 X1 TX Pipe Stage Delay(G1X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.2.71 PTM Pipe Stage Delay Configuration 2 (PTMPSDC2)—Offset 3A0h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN2 X1 RX Pipe Stage Delay (G2X1RPSD):** GEN2 X1 RX Pipe Stage Delay(G2X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN2 X1 TX Pipe Stage Delay (G2X1TPSD):** GEN2 X1 TX Pipe Stage Delay(G2X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN1 X4 RX Pipe Stage Delay (G1X4RPSD):** GEN1 X4 RX Pipe Stage Delay(G1X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN1 X4 TX Pipe Stage Delay (G1X4TPSD):** GEN1 X4 TX Pipe Stage Delay(G1X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.2.72 PTM Pipe Stage Delay Configuration 3 (PTMPSDC3)—Offset 3A4h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN2 X4 RX Pipe Stage Delay (G2X4RPSD):** GEN2 X4 RX Pipe Stage Delay(G2X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN2 X4 TX Pipe Stage Delay (G2X4TPSD):** GEN2 X4 TX Pipe Stage Delay(G2X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN2 X2 RX Pipe Stage Delay (G2X2RPSD):** GEN2 X2 RX Pipe Stage Delay(G2X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN2 X2 TX Pipe Stage Delay (G2X2TPSD):** GEN2 X2 TX Pipe Stage Delay(G2X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.2.73 PTM Pipe Stage Delay Configuration 4 (PTMPSDC4)—Offset 3A8h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN3 X2 RX Pipe Stage Delay (G3X2RPSD):** GEN3 X2 RX Pipe Stage Delay(G3X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN3 X2 TX Pipe Stage Delay (G3X2TPSD):** GEN3 X2 TX Pipe Stage Delay(G3X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN3 X1 RX Pipe Stage Delay (G3X1RPSD):** GEN3 X1 RX Pipe Stage Delay(G3X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN3 X1 TX Pipe Stage Delay (G3X1TPSD):** GEN3 X1 TX Pipe Stage Delay(G3X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.2.74 PTM Pipe Stage Delay Configuration 5 (PTMPSDC5)—Offset 3ACh

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:8	0h RW	**GEN3 X4 RX Pipe Stage Delay (G3X4RPSD):** GEN3 X4 RX Pipe Stage Delay(G3X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN3 X4 TX Pipe Stage Delay (G3X4TPSD):** GEN3 X4 TX Pipe Stage Delay(G3X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.2.75 PTM Extended Config (PTMECFG)—Offset 3B0h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20:18	0h RW	**Periodic Local TSC Link Fetch Frequency (PLTLFF):** Periodic Local TSC Link Fetch Frequency (PLTLFF): When this register is programmed to a non-zero values, the Local TSC Link Clock would perform a periodic fetch to obtain the latest TSC from the Local TSC XTAL Clock domain. This mechanism would ensure the Root Port Local TSC Link is always synchronized with the actual TSC as Link Clock domain is able to drift due to SSC. 000: Disable this feature. 001: Always pull without waiting for expiration. 010: Every 8 clocks 011: Every 16 clocks 100: Every 32 clocks 101: Every 64 clocks 110: Every 128 clocks 111: Every 256 clocks This register is only available in Port 1. Note: Software is expected to program this register prior to setting PTM Enable.
17:15	0h RW/1C/V	**Global Time Fetch Retry Counter (GTFRC):** Global Time Fetch Retry Counter. This register is incremented when the Root Port detected a retry on each Global Time Fetch on IOSF Sideband. The Root Port would increment the value of this register whenever ARU re-sends a LocalSync message. If more than 7 Retries are detected during the Global Time Fetch, Root Port would keep the value of this register to 111 (max) value. Software is expected to write 111 to this register to clear the entire field to 0. Note: For each x4 instance, only the value from Port 1 is used.
14:13	0h RW/1C/V	**Global Time Fetch Fail Counter (GTFFC):** Global Time Fetch Fail Counter. This register is incremented when the Root Port detected a fail on each Global Time Fetch on IOSF Sideband. The Root Port would increment the value of this register whenever ARU sends a SyncComp with the Fail status. If more than 3 failures are detected in the Global Time Fetch, Root Port would keep the value of this register to 111 (max) value. Software is expected to write 11 to this register to clear the entire field to 0. Note: For each x4 instance, only the value from Port 1 is used.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Global Time Fetch Status Pending Completion (GTFSPC):** Global Time Fetch Status Pending Completion. This register is set to 1 by the Root Port when it is in progress of fetching the Global Time from ARU. Note: For each x4 instance, only the value from Port 1 is used.
11:9	0h RW	**Periodic Global Time Stamp Counter Fetch Frequency (PGTSCFF):** Periodic Global Time Stamp Counter Fetch Frequency (PGTSCFF) : This field determine the frequency the Root Port would autonomously fetch the Global Time Stamp Counter. 00: 10us 01: 100us 10: 500us 10: 1ms Software is expected to program this bit first before programming the PGTSCFE register. Attribute: Dynamic Note: For each x4 instance, only the value from Port 1 is used.
8	0h RW	**Periodic Global Time Stamp Counter Fetch Enable (PGTSCFE):** Periodic Global Time Stamp Counter Fetch Enable (PGTSCFE) : When this bit set, the Controller will re-fetch the Global Time from the Always Running Unit (ARU). Once Fetch is completed, the Controller would update all the Local TSC with the newly fetch Global Time. If any PTM dialog is initiated while the re-fetch occurred, the Controller would use the existing Local TSC timers. Hardware would clear this bit upon completed fetching the Global Time. Attribute : Dynamic Note: For each x4 instance, only the value from Port 1 is used.
7	0h RW	**Trigger Global Time Stamp Counter Fetch Enable (TGTSCFE):** Trigger Global Time Stamp Counter Fetch Enable (TGTSCFE) : When this bit set, the Controller will re-fetch the Global Time from the Always Running Unit (ARU). Once Fetch is completed, the Controller would update all the Local TSC with the newly fetch Global Time. If any PTM dialog is initiated while the re-fetch occurred, the Controller would use the existing Local TSC timers. Hardware would clear this bit upon completed fetching the Global Time. Software can only set this register if PGTSCFE is not set. Attribute : Dynamic Note: For each x4 instance, only the value from Port 1 is used.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**PTM Request Periodic ACK Enable (PTMRPAE):** PTM Request Periodic ACK Enable (PTMRPAE) : When this register is set to 1, whenever a valid PTM request TLP is received, the Link Layer would transmit multiple ACK DLLPs corresponding to the PTM Request message. The number of ACK DLLP that the Link Layer would transmit is based on the PTMRNOPAD register. Attribute : Static Note: For each x4 instance, only the value from Port 1 is used.
5:4	0h RW	**PTM Request Number Of Periodic ACK DLLP (PTMRNOPAD):** PTM Request Number Of Periodic ACK DLLP (PTMRNOPAD) : When PTMRPAE is enable, whenever a valid PTM Request message is received, the Link Layer would transmit multiple ACK DLLP corresponding to the receiving of the PTM Request message. This register define the number of DLLP ACK will be transmitted as high priority. 00 - TX 1 DLLP ACK 01 - TX 2 DLLP ACK 10 - TX 3 DLLP ACK 11 - TX 4 DLLP ACK Attribute : Static Note: For each x4 instance, only the value from Port 1 is used.
3:0	0h RW	**IOSF Max Allowed Delay programming (IOSFMADP):** IOSF Max Allowed Delay programming (IOSFMADP): bits Status 0000 Bound Range Low 0001 Bound Range 2 1000 Bound Range Max others reserved

17.2.76 PTM Lower T2 Time Stamp (PTMLT2TSTMP)—Offset 3B4h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Latest Captured Lower T2 TimeStamp (LCLT2TS):** Latest Captured Lower T2 TimeStamp (LCLT2TS). This field shows the latest lower 32-bit of T2 TimeStamp captured by the Root Port in TSC Clock Domain when the Root Port received a valid PTM Request message. The renewable T2 TimeStamp due to a duplicate PTM Request would also be reflected in this field.

17.2.77 PTM Upper T2 Time Stamp (PTMUT2TSTMP)—Offset 3B8h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Latest Captured Upper T2 TimeStamp (LCUT2TS):** Latest Captured Upper T2 TimeStamp (LCUT2TS). This field shows the latest upper 32-bit of T2 TimeStamp captured by the Root Port in TSC Clock Domain when the Root Port received a valid PTM Request message. The renewable T2 TimeStamp due to a duplicate PTM Request would also be reflected in this field.

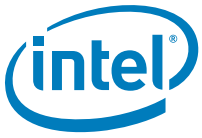
17.2.78 Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**mod-PHY Power Gating Disable Fuse (mPHYPGD):** 0: mod-PHY power gating is enabled. 1: mod-PHY power gating is disabled. Note: Prior to fuse pull, the default of this bit is specified in the 'Reset' column of this field. The default value will reflect the fuse value once fuse pull is done.
30:0	0h RO	**Reserved (RSVD):** Reserved



17.2.79 Thermal and Power Throttling (TNPT)—Offset 418h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 930h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Throttle Period (TP):** Throttle Period (TP): If any of the TNPT.DRXLTE or TNPT.DTXLTE bit is '1, this field defines the duration in milliseconds that defines the Throttling Window. When TNPT.TTG is set to 0, the effective Throttling Period is: 00h: 1 ms 01h: 2 ms : : FFh: 256 ms Note: The Throttle Period will have an uncertainty of +/-1 ms. When TNPT.TTG is set to 1, the effective Throttling Period is: 00h: 100 us 01h: 200 us : : FFh: 25.6 ms Note: The Throttle Period will have an uncertainty of +/-100 us. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling. Note: If TNPT.TT is programmed to a value bigger than TNPT.TP, the hardware behavior is undefined.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RW	**Throttle Time (TT):** Throttle Time (TT): If any of the TNPT.DRXLTE or TNPT.DTXLTE bit is '1, this field defines the period of the Throttling Zone within the Throttling Window specified by TNPT.TP. The value specified in this field will be multiplied by the respective multiplier in TNPT.TSLxM fields depending on the throttling severity indication received together with the Throttling State change indication. When TNPT.TTG is set to 0, the effective Throttle Time is: 00h: 1 ms 01h: 2 ms : 3Fh: 64 ms Others: Alias to 3Fh. Note: The Throttle Period will have an uncertainty of +/-1 ms. When TNPT.TTG is set to 1, the effective Throttle Time is: 00h: 100 us 01h: 200 us : 3Fh: 6.4 ms Note: The Throttle Period will have an uncertainty of +/-100 us. Note: If the reserved encoding is programmed to this field, hardware will behave the same as if the field is programmed to 3Fh. Note: Since the design is using a 1 ms tick for this timer, the Throttle Time will have an uncertainty of +/-1 ms. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling. Note: If TNPT.TT is programmed to a value bigger than TNPT.TP, the hardware behavior is undefined.
15:12	0h RO	**Reserved (RSVD):** Reserved
11:10	2h RW	**Throttling Severity Level 3 Multiplier (TSL3M):** Throttling Severity Level 3 Multiplier (TSL3M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: Always throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.

Bit Range	Default & Access	Field Name (ID): Description
9:8	1h RW	**Throttling Severity Level 2 Multiplier (TSL2M):** Throttling Severity Level 2 Multiplier (TSL2M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: Always throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.
7:6	0h RW	**Throttling Severity Level 1 Multiplier (TSL1M):** Throttling Severity Level 1 Multiplier (TSL1M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: No throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the link throttling
5:4	3h RW	**Throttling Severity Level 0 Multiplier (TSL0M):** Throttling Severity Level 0 Multiplier (TSL0M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: No throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.
3	0h RO	**Reserved (RSVD_1):** Reserved
2	0h RW	**Throttling Timer Granuality (TTG):** Throttling Timer Granuality (TTG): This register determines the granuality of the Thermal Throttling timers. This provides a smaller granuality

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Dynamic RX Link Throttling Enable (DRXLTE):** Dynamic RX Link Throttling Enable (DRXLTE): '0b: Dynamic Link RX Throttling mechanism is disabled. '1b: Dynamic Link RX Throttling mechanism is enabled. PCIe Root Port will induce the link to enter RXL0s. The duty cycle of the throttling window is configurable based on the throttling severity. Note: This field can only be set if the remote component supports TXL0s.
0	0h RW	**Dynamic TX Link Throttling Enable (DTXLTE):** Dynamic TX Link Throttling Enable (DTXLTE): '0b: Dynamic Link TX Throttling mechanism is disabled. '1b: Dynamic Link TX Throttling mechanism is enabled. PCIe Root Port will induce the link to enter TXL0s. The duty cycle of the throttling window is configurable based on the throttling severity. Note: This field can only be set if the remote component supports TXL0s.

17.2.80 Dynamic Lane Switch (DYNLNSW)—Offset 41Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved (RSVD):** Reserved.
0	0h RW	**Hardware Re-Do Preset to Coefficient Mapping Query After Lane Switching (HWRP2CM):** Hardware Re-Do Preset to Coefficient Mapping Query After Lane Switching (HWRP2CM): When this bit is set, the PCIe-SIP Controller would query the Preset to Coefficient mapping through the PIPE GetLocalPresetCoefficients and LocalTxCoefficientsValid interface whenever the Lane Switch ownership has transitioned to PCIe (from another Controller). Note that if this bit is set while the HPCMQE bit is set, the PCIe-SIP Controller would only perform the query once. Unlike the HPCMQE bit, the PCIe-SIP Controller would not clear this bit after completing the query over the PIPE interface. Register Attribute: Static.

17.2.81 Power Control Enable (PCE)—Offset 428h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 9h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved (RSVD):** Reserved for Force Isolate and Reset Together. This bit is not used. The timing between isolate and reset can be controller through PGCBCTL register.
5	0h RW	**Hardware Autonomous Enable (HAE):** Hardware Autonomous Enable (HAE): If set, and the corresponding per-LTSSM state power gating enable bit is also set, then controller power gating will be done when the controller is idle and the controller power gating condition is met in that particular LTSSM state. Refer to PCIEPMECTL2 register for the per-LTSSM state power gating enable bit. If either this bit. is not set or the corresponding per-LTSSM state power gating enable bit is not set, then controller power gating will not be done in that LTSSM state. Note: For each x4 instance, only the value from Port 0 is used. NOTE: If this bit is set, then bits[lb]2:0[rb] must be '000.
4	0h RO	**Reserved (RSVD_1):** Reserved for Force Isolate and Reset Together. This bit is not used. The timing between isolate and reset can be controller through PGCBCTL register.
3	1h RW/L	**Sleep Enable (SE):** Sleep Enable (SE): If clear, Sleep indication to the retention flops will never assert. If set, Sleep indication will be assert to the retention flops as part of the hardware autonomous controller power gating entry flow.
2	0h RO	**Reserved (RSVD_2):** Reserved for D3-Hot Enable. Not supported. RTD3 is supported instead.
1	0h RO	**Reserved (RSVD_3):** Reserved for D0i3 Enable. No support for D0i3.
0	1h RW	**PMC Request Enable (PMCRE):** PMC Request Enable (PMCRE): When set, the controller will only power gate when pmc_[lt]ip[gt]_sw_pg_req_b = '0 and hardware autonomous controller power gating conditions are met. When clear, controller will power gate immediately when the hardware autonomous controller power gating conditions are met regardless of the state of pmc_[lt]ip[gt]_sw_pg_req_b.

17.2.82 PGCB Control1 (PGCBCTL1)—Offset 42Ch

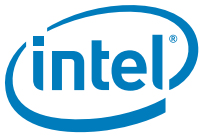
This register specifies the minimum number of delay clocks the PGCB should wait between various states.
Note: For each x4 instance, only the value from Port 0 is used.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 14155555h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved for cfg_trsvd0. Not applicable since frc_clk_srst_en is tied to '0.
29:28	1h RW	**cfg_trstup2frcclks (trstup2frcclks):** cfg_trstup2frcclks(cfg_trstup2frcclks): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
27:26	1h RW	**cfg_tclksonack_cp (tclksonack_cp):** cfg_tclksonack_cp(cfg_tclksonack_cp): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
25:24	0h RO	**Reserved (RSVD_1):** Reserved for cfg_tclksoffack_srst. Not applicable since frc_clk_srst_en is tied to 0.
23:22	0h RO	**Reserved (RSVD_2):** Reserved for cfg_tclksonack_srst. Not applicable since frc_clk_srst_en is tied to 0.
21:20	1h RW	**cfg_tpokup (tpokup):** cfg_tpokup(cfg_tpokup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
19:18	1h RW	**cfg_tpokdown (tpokdown):** cfg_tpokdown(cfg_tpokdown): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks



Bit Range	Default & Access	Field Name (ID): Description
17:16	1h RW	**cfg_tlatchdis (tlatchdis):** cfg_tlatchdis(cfg_tlatchdis): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
15:14	1h RW	**cfg_tsleepinactiv (tsleepinactiv):** cfg_tsleepinactiv(cfg_tsleepinactiv): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
13:12	1h RW	**cfg_tinaccrstup (tinaccrstup):** cfg_tinaccrstup(cfg_tinaccrstup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
11:10	1h RW	**cfg_taccrstup (taccrstup):** cfg_taccrstup(cfg_taccrstup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
9:8	1h RW	**cfg_tlatchen (tlatchen):** cfg_tlatchen(cfg_tlatchen): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
7:6	1h RW	**cfg_tdeisolate (tdeisolate):** cfg_tdeisolate(cfg_tdeisolate): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
5:4	1h RW	**cfg_trstdown (trstdown):** cfg_trstdown(cfg_trstdown): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
3:2	1h RW	**cfg_tisolate (tisolate):** cfg_tisolate(cfg_tisolate): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
1:0	1h RW	**cfg_tsleepact (tsleepact):** cfg_tsleepact(cfg_tsleepact): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

17.2.83 PGCB Control2 (PGCBCTL2)—Offset 430h

This register specifies the minimum number of delay clocks the PGCB should wait between various states.
Note: For each x4 instance, only the value from Port 0 is used.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 54h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved.
7:6	1h RW	**cfg_trsvd4 (trsvd4):** cfg_trsvd4(cfg_trsvd4): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
5:4	1h RW	**cfg_trsvd3 (trsvd3):** cfg_trsvd3(cfg_trsvd3): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
3:2	1h RW	**cfg_trsvd2 (trsvd2):** cfg_trsvd2(cfg_trsvd2): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	**Reserved (RSVD_1):** Reserved for cfg_trsvd1. Not applicable since frc_clk_srst_en is tied to 0.

17.2.84 Equalization Configuration 1 (EQCFG1)—Offset 450h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 3102h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Recovery Entry Count (REC):** Recovery Entry Count (REC): This field indicates the value of the Recovery Entry Counter. This is a 1-based counter. Software must read this register multiple times. The value is valid only if the same value is read out on both of the reads.
23	0h RW	**Recovery Entry and Idle Framing Error Count Enable (REIFECE):** Recovery Entry and Idle Framing Error Count Enable (REIFECE): This bit, when set by software turns on the Recovery Entry Counter and the per-lane Idle Framing Error Counter. The counters are reset when this bit is cleared. This bit is expected to be used by the Software Preset/Coefficient Search tool but is not precluded to be used for other debug purpose. The value of the Recovery Entry Count can be read through EQCFG1.REC field. The value of the Idle Framing Error Count can be read through the Monitor Mux register.
22	0h RW	**Quiesce Guarantee (QG):** Quiesce Guarantee (QG): When set, the Quiesce Guarantee bit in the transmitted TS2 Ordered Set will be set in Recovery.RcvrCfg. When clear, the Quiesce Guarantee bit in the transmitted TS2 Ordered Set will be clear. In all other states, the Quiesce Guarantee bit is Reserved.
21	0h RW	**Link Equalization Request SMI Enable (LERSMIE):** Link Equalization Request SMI Enable (LERSMIE): When set, this bit enables the generation of an SMI to indicate that the Link Equalization Request bit has been set. This mode is meant for survivability purpose such that BIOS can be invoked to address the Re-Equalization request.

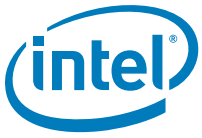
Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Reset EIEOS Interval Count (REIC):** Reset EIEOS Interval Count(REIC): When set, allows the root port to restrict the device from sending EIEOS until after 65536 TS1 Ordered Sets have been transmitted in Phase 3 of the Link Equalization, in the window when the receiver is evaluating the remote transmitter settings..
19	0h RW	**Link Equalization Bypass (LEB):** Link Equalization Bypass (LEB): When set, the root port will never initiate entry to Recovery.Equalization state. This includes never send EQ TS2 in Recovery.RcvrCfg that could cause the device to set start_equalization_w_preset variable. Note: This bit only affects the initial autonomous transition to Link Equalization state when equalization_done_8GT_data_rate = 0. This bit does not affect the software-direction to re-perform Link Equalization.
18	0h RW	**Link Equalization Phase 2 and 3 Bypass (LEP23B):** Link Equalization Phase 2 and 3 Bypass(LEP23B): When set, bypasses the Phase 2 and Phase 3 of Link Equalization. Once Phase 1 is completed, Root Port transitions from Phase 1 directly to Recovery.RcvrLock.
17	0h RW	**Link Equalization 3 Bypass (LEP3B):** Link Equalization 3 Bypass(LEP3B): When set, bypasses the Phase 3 of Link Equalization. Once Phase 2 is completed, Root Port transitions from Phase 2 directly to Recovery.RcvrLock.
16	0h RW	**Remote Transmit Link Equalization Preset/Coefficient Evaluation Bypass (RTLEPCEB):** Remote Transmit Link Equalization Preset/Coefficient Evaluation Bypass (RTLEPCEB): When set, this bit disables the Hardware Autonomous Preset/ Coefficient Search mechanism to search for the best Preset or Coefficient by traversing the Preset or Coefficient List and checking the receiver eye width margin for each of the settings. Instead, the Preset/Coefficient values used by the remote Transmitter will be accepted and the Link Equalization phase will be completed after one round of receiver link training, excluding margining. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Remote Transmitter Preset Coefficient Override Enable (RTPCOE):** Remote Transmitter Preset Coefficient Override Enable (RTPCOE): When set, this bit disables the hardware mechanism to search for the best Preset or Coefficient by traversing the Preset or Coefficient List and checking the receiver eye width margin for each of the settings. Instead, the Preset or Coefficient values specified by the override fields are used. If RTPCL1.PCM = 1, the Preset Override values for each lanes is derived from the following register fields: Lane 0: RTPCL1.RTPRECL0PL0. Lane 1: RTPCL1.RTPOSTCL0PL1. Lane 2: RTPCL1.RTPRECL1PL2. Lane 3: RTPCL1.RTPOSTCL1PL3. If RTPCL1.PCM = 0, the Coefficient Override values for each lanes is derived from the following register fields: Lane 0: RTPCL1.RTPRECL0PL0 and RTPCL1.RTPOSTCL0PL1. Lane 1: RTPCL1.RTPRECL1PL2 and RTPCL1.RTPOSTCL1PL3. Lane 2: RTPCL1.RTPRECL2PL4 and RTPCL2.RTPOSTCL2PL5. Lane 3: RTPCL2.RTPRECL3PL6 and RTPCL2.RTPOSTCL3PL7. BIOS must ensure that the corresponding RTPCL* registers above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
14	0h RW	**Link Equalization Request SCI Enable (LERSCIE):** Link Equalization Request SCI Enable (LERSCIE): When set, this bit enables the generation of an SCI to indicate that the Link Equalization Request bit has been set. This mode is meant for survivability purpose such that SCI handler can be invoked to address the Re-Equalization request.

Bit Range	Default & Access	Field Name (ID): Description
13	1h RW/1S/V	**Hardware Preset to Coefficient Mapping Query Enable (HPCMQE):** Hardware Preset to Coefficient Mapping Query Enable(HPCMQE): When set, the controller will query the Preset to Coefficient mapping through the PIPE GetLocalPresetCoefficients and LocalTxCoefficientsValid interface whenever this bit transitions from 0 to 1. The default of this register bit is 1, indicating that the Preset to Coefficient mapping query will be done on the PIPE interface once coming out of reset. Controller will then update the Preset-Coefficient Mapping registers with the corresponding Coefficient, for each Preset. Controller will also update the LFFS Local LF and Local FS field with the local PHY LF and FS values. Hardware will clear this bit when the Preset to Coefficient mapping query over the PIPE interface is completed. If the Hardware Preset to Coefficient Mapping mechanism is never enabled, the value of the Preset to Coefficient mapping configured by BIOS through the Preset-Coefficient Mapping registers will be used instead of querying through the PIPE interface. Note: BIOS should check to ensure that this field is cleared before enabling Controller Power Gating or mod-PHY Power Gating.
12	1h RO/V	**Hardware Autonomous Equalization Done (HAED):** Hardware Autonomous Equalization Done(HAED): This bit will be cleared when Hardware Autonomous Preset/Coefficient Search starts and will be set when Hardware Autonomous Preset/Coefficient Search is done. This bit is polled by software to ensure that the Hardware Autonomous Preset/Coefficient Search is done before proceeding with the next software sequencing. Some of the Hardware Autonomous Preset/ Coefficient search algorithm may involve the hardware initiating multiple speed change to allow multiple iterations of Link Equalization to be done with different Preset/Coefficient lists. This bit will remain cleared until the iterations are done.

Bit Range	Default & Access	Field Name (ID): Description
11:8	1h RW	**Receiver Wait Time For New Equalization Value Evaluation (RWTNEVE):** Receiver Wait Time For New Equalization Value Evaluation (RWTNEVE): For Downstream Port: This field specifies the amount of time the receiver will wait after entering Phase 3 and sending the new Preset or Coefficient values through the TS1 Ordered Sets before validating the Block Alignment and eventually evaluate the incoming ordered sets (RXEqEval on the PIPE interface asserts). For Upstream Port: This field specifies the amount of time the receiver will wait after entering Phase 2 and sending the new Preset or Coefficient values through the TS1 Ordered Sets before validating the Block Alignment and eventually evaluate the incoming ordered sets (RXEqEval on the PIPE interface asserts). For both Upstream and Downstream Port, this field also specifies the amount of time the receiver will wait after entering Phase 1 before instructing the receiver to adapt to the incoming ordered sets. For Loopback Master: This field specifies the amount of time the receiver will wait after instructing the Loopback Slave to apply a specific Preset through EQ TS1. 0h: 500 ns. 1h: 1 us. 2h: 2 us. 3h: 3 us. 4h: 4 us. : : Fh:15 us.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**EQ TS2 in Recovery.ReceiverConfig Enable (EQTS2IRRC):** EQ TS2 in Recovery.ReceiverConfig Enable(EQTS2IRRC): When set, enables the transmitter to send EQ TS2 in Recovery.RcvrCfg state even when equalization_done_8GT_data_rate variable is 1b, provided that the Downstream Port advertised 8.0 GT/s data rate support in Recovery.RcvrLock, and 8.0 GT/s data rate support has been advertised in the Configuration.Complete or Recovery.RcvrCfg substates by the Upstream Port since exiting the Detect state, and eight consecutive TS1 or TS2 Ordered Sets were received on any configured Lane prior to entry to this substate with speed_change bit set to 1b. When clear, the transmitter can only send EQ TS2 if equalization_done_8GT_data_rate variable is 0b and the Downstream Port advertised 8.0 GT/s data rate support in Recovery.RcvrLock, and 8.0 GT/s data rate support has been advertised in the Configuration.Complete or Recovery.RcvrCfg substates by the Upstream Port since exiting the Detect state, and eight consecutive TS1 or TS2 Ordered Sets were received on any configured Lane prior to entry to this substate with speed_change bit set to 1b. When this bit is used, hardware must ensure that the start_equalization_w_preset variable are in the correct state to ensure that the components on both sides of the link are never out of sync.
6:4	0h RO	**Reserved (RSVD):** Reserved
3	0h RW	**Link EQ Phase 1 Transmit Coefficient Settling Policy (LEQP1TCSP):** Link EQ Phase 1 Transmit Coefficient Settling Policy(LEQP1TCSP): When operating in GEN3 data rate and there is a software/hardware request to re-perform Link Equalization through the Recovery.RcvrLock to Recovery.Equalization arc, PCIe spec requires that the downstream port transmitter switch to the setting specified by the Downstream Port Lane X Transmitter Preset registers in Phase 1. This switching is happening while the downstream port is still actively transmitting TS1 and the upstream port is only required to sample 2 TS1 to determine the next sub-state to transition to. Since the new coefficient setting can take up to 256 ns to settle, the 2 TS1 sampled by the upstream port may be incorrect causing the two LTSSM to be out of sync. When this bit is set, the RP will continue to send EIEOS until the local transmitter setting has settled (specified by PHYCTL2.TXCFGCHGWAIT) before sending TS1 as required in Recovery.Equalization Phase 1. When this bit is clear, the RP will send TS1 with EC = 01 in Recovery.Equalization Phase 1 even though the transmitter setting is still settling.



Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Multi-Fragment Linear and Nine-Tile List Enable (MFLNTL):** Multi-Fragment Linear and Nine-Tile List Enable(MFLNTL): When set in Hardware Autonomous Linear Preset/Coefficient Search mode, the full Preset/Coefficient List will be traversed in multiple fragments, where each fragments is done in separate entry to Recovery. This is used in the case where a longer dwelling time is required for a particular Preset/Coefficient (configured through EQCFG2.PCET). Subsequent Preset/Coefficient entries within the list that could not be covered within that Recovery session will be covered in subsequent re-entries into Recovery. When set in Hardware Autonomous Nine-Tiles Search mode, the 9-tiles list that could not be covered within that Recovery session will be covered in subsequent re-entries into Recovery.
1	1h RW	**Transmitter Use Preset Policy (TUPP):** Transmitter Use Preset Policy(TUPP): This field applies to the Link Equalization Phase where the local transmitter setting is being adjusted. When set, the transmitted TS1 Use Preset bit will be set if the remote device requests the local transmitter to apply specific Preset(instead of Coefficient). When clear, the Use Preset bit will not be set in this case. Note: This bit must be set before changing speed to GEN3 data rate.
0	0h RW	**Receiver Use Preset Policy (RUPP):** Receiver Use Preset Policy(RUPP): This field applies to the Link Equalization Phase where the remote transmitter setting is being adjusted. When set, the received TS1 Use Preset bit will be checked. When clear, the Use Preset bit in the received TS1 will be ignored. Note: This bit must be set before changing speed to GEN3 data rate.

17.2.85 Remote Transmitter Preset Coefficient List 1 (RTPCL1)—Offset 454h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Preset/Coefficient Mode (PCM):** Preset/Coefficient Mode (PCM): This bit defines whether the Preset List or Coefficient List should be sent to the remote TX to adjust the remote TX setting. For Downstream Port, this is used in Phase 3 of the Link Equalization. For Upstream Port, this is used in Phase 2 of the Link Equalization. The list of coefficient or preset is configurable through the Remote Transmitter Preset Coefficient List [lb]1:4[rb] registers. When this bit is set, Coefficient Mode is enabled and the Remote Transmitter Preset Coefficient List [lb]1:4[rb] registers contain the Coefficient List. When this bit is clear, Preset Mode is enabled and the Remote Transmitter Preset Coefficient List [lb]1:3[rb] registers contain the Preset List.
30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 2/Preset List 4 (RTPRECL2PL4):** Remote Transmitter Pre-Cursor Coefficient List 2/Preset List 4 (RTPRECL2PL4): For Downstream Port: This field defines the pre-cursor coefficient List 2 or Preset List 4 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 2 or Preset List 4 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Remote Transmitter Post-Cursor Coefficient List 1/Preset List 3 (RTPOSTCL1PL3):** Remote Transmitter Post-Cursor Coefficient List 1/Preset List 3 (RTPOSTCL1PL3): For Downstream Port: This field defines the post-cursor coefficient List 1 or Preset List 3 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 1 or Preset List 3 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
17:12	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 1/Preset List 2 (RTPRECL1PL2):** Remote Transmitter Pre-Cursor Coefficient List 1/Preset List 2 (RTPRECL1PL2): For Downstream Port: This field defines the pre-cursor coefficient List 1 or Preset List 2 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 1 or Preset List 2 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Remote Transmitter Post-Cursor Coefficient List 0/Preset List 1 (RTPOSTCL0PL1):** Remote Transmitter Post-Cursor Coefficient List 0/Preset List 1 (RTPOSTCL0PL1): For Downstream Port: This field defines the post-cursor coefficient List 0 or Preset List 1 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 0 or Preset List 1 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
5:0	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 0/Preset List 0 (RTPRECL0PL0):** Remote Transmitter Pre-Cursor Coefficient List 0/Preset List 0 (RTPRECL0PL0): For Downstream Port: This field defines the pre-cursor coefficient List 0 or Preset List 0 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 0 or Preset List 0 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.2.86 Remote Transmitter Preset Coefficient List 2 (RTPCL2)—Offset 458h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Remote Transmitter Post-Cursor Coefficient List 4/Preset List 9 (RTPOSTCL4PL9):** Remote Transmitter Post-Cursor Coefficient List 4/Preset List 9(RTPOSTCL4PL9): For Downstream Port: This field defines the post-cursor coefficient List 4 or Preset List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 4 or Preset List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 4/Preset List 8 (RTPRECL4PL8):** Remote Transmitter Pre-Cursor Coefficient List 4/Preset List 8 (RTPRECL4PL8): For Downstream Port: This field defines the pre-cursor coefficient List 4 or Preset List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 4 or Preset List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Post-Cursor Coefficient List 3/Preset List 7 (RTPOSTCL3PL7):** Remote Transmitter Post-Cursor Coefficient List 3/Preset List 7 (RTPOSTCL3PL7): For Downstream Port: This field defines the post-cursor coefficient List 3 or Preset List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 3 or Preset List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 3/Preset List 6 (RTPRECL3PL6):** Remote Transmitter Pre-Cursor Coefficient List 3/Preset List 6 (RTPRECL3PL6): For Downstream Port: This field defines the pre-cursor coefficient List 3 or Preset List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 3 or Preset List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Post-Cursor Coefficient List 2/Preset List 5 (RTPOSTCL2PL5):** Remote Transmitter Post-Cursor Coefficient List 2/Preset List 5 (RTPOSTCL2PL5): For Downstream Port: This field defines the post-cursor coefficient List 2 or Preset List 5 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 2 or Preset List 5 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.2.87 Remote Transmitter Preset Coefficient List 3 (RTPCL3)—Offset 45Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 7 (RTPRECL7):** Remote Transmitter Pre-Cursor Coefficient List 7 (RTPRECL7): For Downstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Post-Cursor Coefficient List 6 (RTPOSTCL6):** Remote Transmitter Post-Cursor Coefficient List 6 (RTPOSTCL6): For Downstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 6 (RTPRECL6):** Remote Transmitter Pre-Cursor Coefficient List 6 (RTPRECL6): For Downstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Post-Cursor Coefficient List 5 (RTPOSTCL5):** Remote Transmitter Post-Cursor Coefficient List 5 (RTPOSTCL5): For Downstream Port: This field defines the pre-cursor coefficient List 5 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 5 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 5/Preset List 10 (RTPRECL5PL10):** Remote Transmitter Pre-Cursor Coefficient List 5/Preset List 10 (RTPRECL5PL10): For Downstream Port: This field defines the pre-cursor coefficient List 5 or Preset List 10 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 5 or Preset List 10 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.2.88 Remote Transmitter Preset Coefficient List 4 (RTPCL4)—Offset 460h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Remote Transmitter Post-Cursor Coefficient List 9 (RTPOSTCL9):** Remote Transmitter Post-Cursor Coefficient List 9 (RTPOSTCL9): For Downstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 9 (RTPRECL9):** Remote Transmitter Pre-Cursor Coefficient List 9 (RTPRECL9): For Downstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Post-Cursor Coefficient List 8 (RTPOSTCL8):** Remote Transmitter Post-Cursor Coefficient List 8 (RTPOSTCL8): For Downstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 8 (RTPRECL8):** Remote Transmitter Pre-Cursor Coefficient List 8 (RTPRECL8): For Downstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Post-Cursor Coefficient List 7 (RTPOSTCL7):** Remote Transmitter Post-Cursor Coefficient List 7 (RTPOSTCL7): For Downstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.2.89 Figure Of Merit Status (FOMS)—Offset 464h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved
30:29	0h RW	**Index (I):** Index (I): The FOMV field will reflect the Figure of Merit Scoreboard value for the index specified by this field. List N below refers to the Figure of Merit values captured in the scoreboard corresponding to the Preset or Coefficient List N. 00b: Index 0 =[gt] {List 2, List 1, List 0}. 01b: Index 1 =[gt] {List 5, List 4, List 3}. 10b: Index 2 =[gt] {List 8, List 7, List 6}. 11b: Index 3 =[gt] {Rsvd, List 10, List 9}.

Bit Range	Default & Access	Field Name (ID): Description
28:24	0h RW	**Lane Number (LN):** Lane Number (LN): The FOMV field will reflect the Figure of Merit Scoreboard value for the lane specified by this field. 00000b: Lane 0. 00001b: Lane 1. 00010b: Lane 2. 00011b: Lane 3. Others: Reserved.
23:0	0h RO/V	**Figure of Merit Scoreboard Value (FOMSV):** Figure of Merit Scoreboard Value (FOMSV): This field will reflect the Figure of Merit Scoreboard entries referenced by the Lane Number and Index field in this register. For example, when Index == 00b, this field will reflect the Figure of Merit values for Lane specified in Lane Number field and the encoding of this field is as shown below: 23:16: Figure of Merit for Preset/Coefficient List 2. 15:8 : Figure of Merit for Preset/Coefficient List 1. 7:0 : Figure of Merit for Preset/Coefficient List 0. If the Receiver Eye Width margining completes with error, the value of Figure of Merit should reflect 0x00.

17.2.90 Hardware Autonomous Equalization Control (HAEQ)—Offset 468h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: A0080E00h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Ah RW	**Hardware Autonomous Preset/Coefficient Count Per-Iteration (HAPCCPI):** Hardware Autonomous Preset/Coefficient Count Per-Iteration(HAPCCPI): This field defines the number of Preset/Coefficient to be traversed for every iteration of Recovery Equalization. For the Linear Mode, EQCFG2.HAPCSB specifies the total number of Presets/Coefficients to be checked in total while this field specifies the number of Presets/Coefficients to be checked per-iteration of Recovery Equalization. Hardware will enter Recovery Equalization and check the number of Presets/Coefficients specified by this field. Once that is done, hardware will exit Recovery Equalization and trigger another entry to Recovery Equalization to check another set of Presets/Coefficients. This goes on until the total number of Presets/Coefficients are checked. For Nine-Tiles Mode, EQCFG2.NTIC specifies the number of 9-tiles iterations, which indirectly specifies the total number of Presets/ Coefficients to be checked in total. Similar to Linear Mode, this field specifies the number of Presets/Coefficients to be checked per-iteration of Recovery Equalization. 0h: 1 Preset/Coefficient per-iteration. 1h: 2 Preset/Coefficient per-iteration. 2h: 3 Preset/Coefficient per-iteration. ... 9h: 10 Preset/Coefficient per-iteration. Ah: 11 Preset/Coefficient per-iteration. Others: Reserved.
27:20	0h RW	**FOM Error Mask (FOMEM):** FOM Error Mask(FOMEM): The FOM error counter will be masked(thus ignoring the FOM error) for all the FOM values prior to the FOM value specified in this field. If this field is programmed to 00h, this mechanism is disabled. This bit must be configured before training to GEN3 data rate.

Bit Range	Default & Access	Field Name (ID): Description
19	1h RW	**MAC FOM Control (MACFOMC):** MAC FOM Control(MACFOMC): When set, MAC controls the advancement of the FOM values completely while in the Link Equalization mode. For downstream port, this is done in Phase 3 and for upstream port, this is done in Phase 2 of the Link Equalization. The dwelling time for each of the FOM values are programmed through the remaining fields of this register. When enabled, the hardware will start in Speeding Mode, where it will instruct the PHY to increment the FOM value after the Speeding Latency specified by HAEQ.SL field. Once the FOM value matches HAEQ.SFOMFM, the hardware switches from Speeding Mode to Dwelling Mode. In Dwelling mode, the MAC will instruct PHY to increment the FOM value after the Dwelling Latency specified by HAEQ.DL field. This is done until the link equalization phase is completed. When cleared, PHY controls the advancement of the FOM values completely, during the Link Equalization mode. This bit must be configured before training to GEN3 data rate.
18:16	0h RW	**Speeding Latency (SL):** Speeding Latency(SL): Specifies the residency time for a particular FOM value in Speeding Mode. 000b: 192 ns. 001b: 256 ns. 010b: 512 ns. 011b: 1 us. 100b: 2 us. 101b: 4 us. 110b: 8 us. 111b: 16 us. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.
15:8	Eh RW	**Dwelling Latency (DL):** Dwelling Latency(DL): Specifies the residency time for a particular FOM value in Dwelling Mode. 00h: 2 us. 01h: 4 us. 02h: 6 us. ... FFh: 512 us. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Starting FOM For Margining (SFOMFM):** Starting FOM For Margining(SFOMFM): Define the FOM where MAC switches from Speeding Mode to Dwelling Mode after hitting the programmed FOM value in Hardware Autonomous Preset/Coefficient mode. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.

17.2.91 Local Transmitter Coefficient Override 1 (LTCO1)—Offset 470h

Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane bits are not used.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD):** Reserved
25	0h RW	**Lane 1 Transmitter Coefficient Override Enable (L1TCOE):** Lane 1 Transmitter Coefficient Override Enable (L1TCOE): When set, the transmitter coefficient override values LTPCO1.L1TPRECO and LTPCO1.L1TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO1.L1TPRECO and LTPCO1.L1TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Lane 0 Transmitter Coefficient Override Enable (L0TCOE):** Lane 0 Transmitter Coefficient Override Enable (L0TCOE): When set, the transmitter coefficient override values LTPCO1.L0TPRECO and LTPCO1.L0TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO1.L0TPRECO and LTPCO1.L0TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
23:18	0h RW	**Lane 1 Transmitter Post-Cursor Coefficient Override (L1TPOSTCO):** Lane 1 Transmitter Post-Cursor Coefficient Override (L1TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L1TCOE = 1.
17:12	0h RW	**Lane 1 Transmitter Pre-Cursor Coefficient Override (L1TPRECO):** Lane 1 Transmitter Pre-Cursor Coefficient Override (L1TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L1TCOE = 1.
11:6	0h RW	**Lane 0 Transmitter Post-Cursor Coefficient Override (L0TPOSTCO):** Lane 0 Transmitter Post-Cursor Coefficient Override (L0TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L0TCOE = 1.
5:0	0h RW	**Lane 0 Transmitter Pre-Cursor Coefficient Override (L0TPRECO):** Lane 0 Transmitter Pre-Cursor Coefficient Override (L0TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L0TCOE = 1.

17.2.92 Local Transmitter Coefficient Override 2 (LTCO2)—Offset 474h

Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane bits are not used.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD):** Reserved
25	0h RW	**Lane 3 Transmitter Coefficient Override Enable (L3TCOE):** Lane 3 Transmitter Coefficient Override Enable (L3TCOE): When set, the transmitter coefficient override values LTPCO2.L3TPRECO and LTPCO2.L3TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO2.L3TPRECO and LTPCO2.L3TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
24	0h RW	**Lane 2 Transmitter Coefficient Override Enable (L2TCOE):** Lane 2 Transmitter Coefficient Override Enable (L2TCOE): When set, the transmitter coefficient override values LTPCO2.L2TPRECO and LTPCO2.L2TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO2.L2TPRECO and LTPCO2.L2TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Lane 3 Transmitter Post-Cursor Coefficient Override (L3TPOSTCO):** Lane 3 Transmitter Post-Cursor Coefficient Override (L3TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L3TCOE = 1.
17:12	0h RW	**Lane 3 Transmitter Pre-Cursor Coefficient Override (L3TPRECO):** Lane 3 Transmitter Pre-Cursor Coefficient Override (L3TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L3TCOE = 1
11:6	0h RW	**Lane 2 Transmitter Post-Cursor Coefficient Override (L2TPOSTCO):** Lane 2 Transmitter Post-Cursor Coefficient Override (L2TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L2TCOE = 1.
5:0	0h RW	**Lane 2 Transmitter Pre-Cursor Coefficient Override (L2TPRECO):** Lane 2 Transmitter Pre-Cursor Coefficient Override (L2TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L2TCOE = 1.

17.2.93 GEN3 L0s Control (G3L0SCTL)—Offset 478h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: C00281Eh

Bit Range	Default & Access	Field Name (ID): Description
31:24	Ch RW	**Gen3 Active State L0s Preparation Latency (G3ASL0SPL):** Gen3 Active State L0s Preparation Latency (G3ASL0SPL) Determines how long the Link layer has to indicate IDLE before the link initialization and control logic enters L0s 00: 0 clocks (enter immediately) 01: 1 clock ... FF: 255 clocks The value of this register is only used if the Gen3 L0s Entry Idle Control register is set to [quote]11[/quote] and operating in Gen3 mode.
23:22	0h RW	**Gen3 L0s Entry Idle Control (G3L0SIC):** Gen3 L0s Entry Idle Control (G3L0SIC): 00 : Allow entry into L0s after the link has been idle for a period of time equal to of the received N_FTS total entry time (1/4 * N_FTS * 16) 01 : Allow entry into L0s after the link has been idle for for a period of time equal to of the received N_FTS total entry time (1/2 * N_FTS * 16) 10 : Allow entry after the link has been idle for for a period of time equal to the received N_FTS total entry time (N_FTS * 16) 11: Allow entry into L0s after the link has been idle for a period specified in the Gen3 Active State L0s Preparation Latency register. This register is only applied when operating in Gen3 mode.
21:16	0h RO	**Reserved (RSVD):** Reserved
15:8	28h RW	**Gen3 Unique Clock N_FTS (G3UCNFTS):** Gen3 Unique Clock N_FTS (G3UCNFTS): Number of Fast Training Sequence ordered sets required to be transmitted for a root port Receiver to exit L0s in a unique (non-common) clock configuration (LCTL.CCC=0) when operating in Gen3 mode. The N_FTS value is sent in TS1 and TS2 training sets during link training. 00: 0 FTS sets 01: 1 FTS set ... FF: 255 FTS sets Note: When operating in Mobile Express mode, the output of this field is not used to determine the number of FTS to be sent on TXL0s exit. Mobile Express does not support Fast Training Sequence. Instead, SYNC is used to achieve bit lock. However, the output of this field is still used in L0s Entry Idle Control registers to determine the L0s Entry Idle latency.

Bit Range	Default & Access	Field Name (ID): Description
7:0	1Eh RW	**Gen3 Common Clock N_FTS (G3CCNFTS):** Gen3 Common Clock N_FTS (G3CCNFTS): Number of Fast Training Sequence ordered sets required to be transmitted for a root port Receiver to exit L0s in a common clock configuration (LCTL.CCC=1) when operating in Gen3 mode. The N_FTS value is sent in TS1 and TS2 training sets during link training. 00: 0 FTS sets 01: 1 FTS set ... FF: 255 FTS sets Note: When operating in Mobile Express mode, the output of this field is not used to determine the number of FTS to be sent on TXL0s exit. Mobile Express does not support Fast Training Sequence. Instead, SYNC is used to achieve bit lock. However, the output of this field is still used in L0s Entry Idle Control registers to determine the L0s Entry Idle latency.

17.2.94 Equalization Configuration 2 (EQCFG2)—Offset 47Ch

Size:32 bits
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: A001h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Nine-Tiles Iteration Count (NTIC):** Nine-Tiles Iteration Count(NTIC): This field specifies the number of iterations to perform the 9-tiles search. Each iteration involves evaluating the neighboring 9-tiles for the best Preset/Coefficient margin and then use the Preset/Coefficient as the centerpoint to identify and evaluate the next 9-tiles. 00h: 1 iteration. 01h: 2 iterations. 02h: 3 iterations. ... FFh: 256 iterations.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**Equalization Margining Disable (EMD):** Equalization Margining Disable(EMD):When set, the Root Port will not request the PHY to perform Receiver Margining by asserting RxEqEval on each Preset/ Coefficient list traversed. This allows the receiver to still measure the Bit Error Count without margining. When cleared, the Root Port will request the PHY to perform Receiver Margining by asserting RxEqEval. This field is only valid when operating in Hardware Autonomous Preset/Coefficient Search mode. The Preset/Coefficient list will still be traversed to the end.
22:20	0h RW	**Nine-Tiles Step Size (NTSS):** Nine-Tiles Step Size(NTSS): This field specifies the step size used to identify the surrounding 9-tiles to be used for margining. 000b: 1 step. 001b: 2 steps. 010b: 3 steps. 011b: 4 steps. 100b: 5 steps. 101b: 6 steps. 110b: 7 steps. 111b: 8 steps. Each of the steps is measured in terms of incrementing of decrementing the coefficient values.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW	**Preset/Coefficient Evaluation Timeout (PCET):** Preset/ Coefficient Evaluation Timeout(PCET): This field specifies the evaluation timeout for a single Preset/Coefficient in the List when operating in Hardware Autonomous Preset/Coefficient Search mode. By spec, the evaluation phase must be completed before the 24 ms timeout. To support 12 Presets (11 Presets + 1 final good Preset), each Preset will have up to 2 ms for evaluation. This field allows the 2 ms timer to be programmable. This is useful if the EQCFG2.HAPCSB limits the Preset/Coefficient List to smaller than 12 such that each Preset/Coefficient could be evaluated for a time longer than 2 ms. 0h: 2 ms. 1h: 2.5 ms. 2h: 3 ms. 3h: 3.5 ms. 4h: 4 ms. 5h: 4.5 ms. 6h: 5 ms. 7h: 6 ms. 8h: 7 ms. 9h: 8 ms. Ah: 9 ms. Bh:10 ms. Ch:11 ms. Dh:21 ms. Eh:22 ms. Fh:23 ms.
15:12	Ah RW	**Hardware Autonomous Preset/Coefficient Search Bound (HAPCSB):** Hardware Autonomous Preset/Coefficient Search Bound(HAPCSB): This field defines the number of Preset/ Coefficient List to be traversed, out of 11 for Presets or out of 10 for Coefficients. The Preset/Coefficient list will be traversed from List 0 to the value specified by this field in incremental order. This field allows equalization to be done with smaller set of Preset/ Coefficient list and each of the Preset/Coefficient list could be run for a longer time. 0h: Preset/Coefficient List 0 only. 1h: Preset/Coefficient List 0 - 1. 2h: Preset/Coefficient List 0 - 2. : : 9h: Preset/Coefficient List 0 - 9. Ah: Preset List 0 - 10/Coefficient List 0-9. Others: Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Nine-Tiles Equalization Mechanism Enable (NTEME):** Nine-Tiles Equalization Mechanism Enable(NTEME): When set, the Nine-Tiles Equalization Mechanism is enabled when running in Hardware Autonomous Preset/Coefficient Search Mode.
10	0h RW	**Mid-Point Equalization Mechanism Enable (MPEME):** Mid-Point Equalization Mechanism Enable(MPEME): When set, the Mid-Point Equalization Mechanism is enabled when running in Hardware Autonomous Preset/Coefficient Search Mode.
9:8	0h RW	**Receiver Eye Width Margin Error Threshold Multiplier (REWMETM):** Receiver Eye Width Margin Error Threshold Multiplier (REWMETM): This field specifies the multiplier to be used with REWMET field. 00b: Multiply REWMET by 1 (effectively no multiplier). 01b: Multiply REWMET by 10. 10b: Multiply REWMET by 100. 11b: Multiply REWMET by 1000.
7:0	1h RW	**Receiver Eye Width Margin Error Threshold (REWMET):** Receiver Eye Width Margin Error Threshold (REWMET): This field specifies the count threshold which upon exceeded, will cause controller to terminate the current iteration of Receiver Eye Width Margining and move on to the next preset or coefficient in the list. The value specified in this field will need to be multiplied with the multiplier specified in REWMETM field to get the final threshold values. 00h: Terminate on 1 x REWMETM errors. 01h: Terminate on 2 x REWMETM errors. 02h: Terminate on 4 x REWMETM errors. 03h: Terminate on 6 x REWMETM errors. : : FEh: Terminate on 508 x REWMETM errors. FFh: Never terminate. Rely on PHY to terminate the margining.

17.2.95 Monitor Mux (MM)—Offset 480h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO/V	**Monitor Signal State (MSST):** Monitor Signal State(MSST): The internal signal groupings selected by MM.MSS field is reflected in this field. The intention of this monitor signal is provide software a capability to monitor some of the GEN3 related parameters accumulated by the controller through the Link Equalization that are too costly to be mapped to dedicated registers. Implementation MUST NEVER expose any security related information through this Monitor Mux.
7:0	0h RW	**Monitor Signal Select (MSS):** Monitor Signal Select(MSS): This field is essentially the mux select for the Monitor Signal mux. Setting this field allows different monitor signals to be muxed out and readable by software through the MM.MSST field.

17.2.96 Lane0 P0 and P1 Preset-Coefficient Mapping (L0P0P1PCM)—Offset 500h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.97 Lane0 P1, P2 and P3 Preset-Coefficient Mapping (L0P1P2P3PCM)—Offset 504h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.98 Lane0 P3 and P4 Preset-Coefficient Mapping (L0P3P4PCM)—Offset 508h

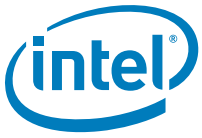
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.99 Lane0 P5 and P6 Preset-Coefficient Mapping (L0P5P6PCM)—Offset 50Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.100 Lane0 P6, P7 and P8 Preset-Coefficient Mapping (L0P6P7P8PCM)—Offset 510h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.101 Lane0 P8 and P9 Preset-Coefficient Mapping (L0P8P9PCM)—Offset 514h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

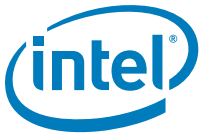
Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.102 Lane0 P10 Preset-Coefficient Mapping (L0P10PCM)—Offset 518h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.



Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.103 Lane0 LF and FS (L0LFFS)—Offset 51Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.104 Lane1 P0 and P1 Preset-Coefficient Mapping (L1P0P1PCM)—Offset 520h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.105 Lane1 P1, P2 and P3 Preset-Coefficient Mapping (L1P1P2P3PCM)—Offset 524h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.106 Lane1 P3 and P4 Preset-Coefficient Mapping (L1P3P4PCM)—Offset 528h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.107 Lane1 P5 and P6 Preset-Coefficient Mapping (L1P5P6PCM)—Offset 52Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.108 Lane1 P6, P7 and P8 Preset-Coefficient Mapping (L1P6P7P8PCM)—Offset 530h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.109 Lane1 P8 and P9 Preset-Coefficient Mapping (L1P8P9PCM)—Offset 534h

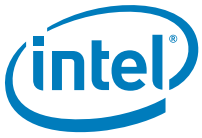
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.110 Lane1 P10 Preset-Coefficient Mapping (L1P10PCM)—Offset 538h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.111 Lane1 LF and FS (L1LFFS)—Offset 53Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.112 Lane2 P0 and P1 Preset-Coefficient Mapping (L2P0P1PCM)—Offset 540h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.113 Lane2 P1, P2 and P3 Preset-Coefficient Mapping (L2P1P2P3PCM)—Offset 544h

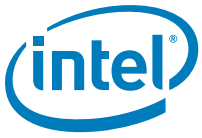
This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.114 Lane2 P3 and P4 Preset-Coefficient Mapping (L2P3P4PCM)—Offset 548h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.115 Lane2 P5 and P6 Preset-Coefficient Mapping (L2P5P6PCM)—Offset 54Ch

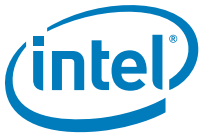
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.116 Lane2 P6, P7 and P8 Preset-Coefficient Mapping (L2P6P7P8PCM)—Offset 550h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.117 Lane2 P8 and P9 Preset-Coefficient Mapping (L2P8P9PCM)—Offset 554h

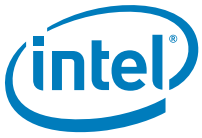
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.118 Lane2 P10 Preset-Coefficient Mapping (L2P10PCM)—Offset 558h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.119 Lane2 LF and FS (L2LFFS)—Offset 55Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.120 Lane3 P0 and P1 Preset-Coefficient Mapping (L3P0P1PCM)—Offset 560h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.121 Lane3 P1, P2 and P3 Preset-Coefficient Mapping (L3P1P2P3PCM)—Offset 564h

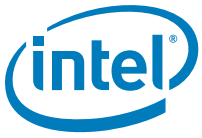
This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.122 Lane3 P3 and P4 Preset-Coefficient Mapping (L3P3P4PCM)—Offset 568h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.123 Lane3 P5 and P6 Preset-Coefficient Mapping (L3P5P6PCM)—Offset 56Ch

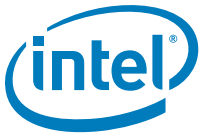
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.124 Lane3 P6, P7 and P8 Preset-Coefficient Mapping (L3P6P7P8PCM)—Offset 570h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.125 Lane3 P8 and P9 Preset-Coefficient Mapping (L3P8P9PCM)—Offset 574h

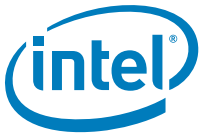
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.126 Lane3 P10 Preset-Coefficient Mapping (L3P10PCM)—Offset 578h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.2.127 Lane3 LF and FS (L3LFFS)—Offset 57Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 20 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3 Registers Summary

Table 17-3. Summary of pcie_cfg Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4h	7h	Device Command; Primary Status (CMD_PSTS)—Offset 4h	100000h
8h	Bh	Revision ID;Class Code (RID_CC)—Offset 8h	60400F0h
Ch	Fh	Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch	810000h
18h	1Bh	Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h	0h
1Ch	1Fh	I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch	0h
20h	23h	Memory Base and Limit (MBL)—Offset 20h	0h
24h	27h	Prefetchable Memory Base and Limit (PMBL)—Offset 24h	10001h
28h	2Bh	Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h	0h
2Ch	2Fh	Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch	0h
34h	37h	Capabilities List Pointer (CAPP)—Offset 34h	40h
3Ch	3Fh	Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch	0h
40h	43h	Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h	428010h
44h	47h	Device Capabilities (DCAP)—Offset 44h	8001h
48h	4Bh	Device Control; Device Status (DCTL_DSTS)—Offset 48h	100000h
4Ch	4Fh	Link Capabilities (LCAP)—Offset 4Ch	710C00h
50h	53h	Link Control; Link Status (LCTL_LSTS)—Offset 50h	10000h
54h	57h	Slot Capabilities (SLCAP)—Offset 54h	40060h
58h	5Bh	Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h	0h
5Ch	5Fh	Root Control (RCTL)—Offset 5Ch	0h
60h	63h	Root Status (RSTS)—Offset 60h	0h
64h	67h	Device Capabilities 2 (DCAP2)—Offset 64h	80837h
68h	6Bh	Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h	0h
6Ch	6Fh	Link Capabilities 2 (LCAP2)—Offset 6Ch	0h
70h	73h	Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h	0h
74h	77h	Slot Capabilities 2 (SLCAP2)—Offset 74h	0h

Table 17-3. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
78h	7Bh	Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h	0h
80h	83h	Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h	9005h
88h	8Bh	Message Signaled Interrupt Message Data (MD)—Offset 88h	0h
90h	93h	Subsystem Vendor Capability (SVCAP)—Offset 90h	A00Dh
94h	97h	Subsystem Vendor IDs (SVID)—Offset 94h	0h
A0h	A3h	Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h	C8030001h
A4h	A7h	PCI Power Management Control And Status (PMCS)—Offset A4h	8h
D4h	D7h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	800h
E4h	E7h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	0h
100h	103h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	0h
104h	107h	Uncorrectable Error Status (UES)—Offset 104h	0h
108h	10Bh	Uncorrectable Error Mask (UEM)—Offset 108h	0h
10Ch	10Fh	Uncorrectable Error Severity (UEV)—Offset 10Ch	60011h
110h	113h	Correctable Error Status (CES)—Offset 110h	0h
114h	117h	Correctable Error Mask (CEM)—Offset 114h	2000h
118h	11Bh	Advanced Error Capabilities and Control (AECC)—Offset 118h	0h
11Ch	11Fh	Header Log DW1 (HL_DW1)—Offset 11Ch	0h
120h	123h	Header Log DW2 (HL_DW2)—Offset 120h	0h
124h	127h	Header Log DW3 (HL_DW3)—Offset 124h	0h
128h	12Bh	Header Log DW4 (HL_DW4)—Offset 128h	0h
12Ch	12Fh	Root Error Command (REC)—Offset 12Ch	0h
134h	137h	Error Source Identification (ESID)—Offset 134h	0h
140h	143h	ACS Extended Capability Header (ACSECH)—Offset 140h	0h
144h	147h	ACS Capability Register (ACSCAPR)—Offset 144h	Fh
148h	14Bh	ACS Control Register (ACSCTLR)—Offset 148h	0h
150h	153h	PTM Extended Capability Header (PTMECH)—Offset 150h	0h
154h	157h	PTM Capability Register (PTMCAPR)—Offset 154h	400h
158h	15Bh	PTM Control Register (PTMCTLR)—Offset 158h	0h
200h	203h	L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h	0h
204h	207h	L1 Sub-States Capabilities (L1SCAP)—Offset 204h	28281Fh
208h	20Bh	L1 Sub-States Control 1 (L1SCTL1)—Offset 208h	0h
20Ch	20Fh	L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch	28h
220h	223h	Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h	0h
224h	227h	Link Control 3 (LCTL3)—Offset 224h	0h
228h	22Bh	Lane Error Status (LES)—Offset 228h	0h
22Ch	22Fh	Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch	7F7F7F7Fh

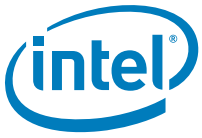


Table 17-3. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
230h	233h	Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h	7F7F7F7Fh
300h	303h	PCI Express Replay Timer Policy 1 (PCIERTP1)—Offset 300h	A64F96h
304h	307h	PCI Express Replay Timer Policy 2 (PCIERTP2)—Offset 304h	1BC00B86h
314h	317h	PCI Express Status 1 (PCIESTS1)—Offset 328h	54262A13h
328h	32Bh	PCI Express Status 1 (PCIESTS1)—Offset 328h	0h
32Ch	32Fh	PCI Express Status 2 (PCIESTS2)—Offset 32Ch	0h
330h	333h	PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h	2A000016h
334h	337h	PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h	4ABCB5BCh
390h	393h	PTM Propagation Delay (PTMPD)—Offset 390h	0h
394h	397h	PTM Lower Local Master Time (PTMLLMT)—Offset 394h	0h
398h	39Bh	PTM Upper Local Master Time (PTMULMT)—Offset 398h	0h
39Ch	39Fh	PTM Pipe Stage Delay Configuration 1 (PTMPSDC1)—Offset 39Ch	0h
3A0h	3A3h	PTM Pipe Stage Delay Configuration 2 (PTMPSDC2)—Offset 3A0h	0h
3A4h	3A7h	PTM Pipe Stage Delay Configuration 3 (PTMPSDC3)—Offset 3A4h	0h
3A8h	3ABh	PTM Pipe Stage Delay Configuration 4 (PTMPSDC4)—Offset 3A8h	0h
3ACh	3AFh	PTM Pipe Stage Delay Configuration 5 (PTMPSDC5)—Offset 3ACh	0h
3B0h	3B3h	PTM Extended Config (PTMECFG)—Offset 3B0h	0h
3B4h	3B7h	PTM Lower T2 Time Stamp (PTMLT2TSTMP)—Offset 3B4h	0h
3B8h	3BBh	PTM Upper T2 Time Stamp (PTMUT2TSTMP)—Offset 3B8h	0h
414h	417h	Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h	0h
418h	41Bh	Thermal and Power Throttling (TNPT)—Offset 418h	930h
41Ch	41Fh	Dynamic Lane Switch (DYNLNSW)—Offset 41Ch	0h
420h	423h	Power Control Enable (PCE)—Offset 428h	2AE8146h
428h	42Bh	Power Control Enable (PCE)—Offset 428h	9h
42Ch	42Fh	PGCB Control1 (PGCBCTL1)—Offset 42Ch	14155555h
430h	433h	PGCB Control2 (PGCBCTL2)—Offset 430h	54h
450h	453h	Equalization Configuration 1 (EQCFG1)—Offset 450h	3102h
454h	457h	Remote Transmitter Preset Coefficient List 1 (RTPCL1)—Offset 454h	0h
458h	45Bh	Remote Transmitter Preset Coefficient List 2 (RTPCL2)—Offset 458h	0h
45Ch	45Fh	Remote Transmitter Preset Coefficient List 3 (RTPCL3)—Offset 45Ch	0h
460h	463h	Remote Transmitter Preset Coefficient List 4 (RTPCL4)—Offset 460h	0h
464h	467h	Figure Of Merit Status (FOMS)—Offset 464h	0h
468h	46Bh	Hardware Autonomous Equalization Control (HAEQ)—Offset 468h	A0080E00h
470h	473h	Local Transmitter Coefficient Override 1 (LTCO1)—Offset 470h	0h
474h	477h	Local Transmitter Coefficient Override 2 (LTCO2)—Offset 474h	0h
478h	47Bh	GEN3 L0s Control (G3L0SCTL)—Offset 478h	C00281Eh
47Ch	47Fh	Equalization Configuration 2 (EQCFG2)—Offset 47Ch	A001h
480h	483h	Monitor Mux (MM)—Offset 480h	0h
500h	503h	Lane0 P0 and P1 Preset-Coefficient Mapping (L0P0P1PCM)—Offset 500h	0h

Table 17-3. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
504h	507h	Lane0 P1, P2 and P3 Preset-Coefficient Mapping (L0P1P2P3PCM)—Offset 504h	0h
508h	50Bh	Lane0 P3 and P4 Preset-Coefficient Mapping (L0P3P4PCM)—Offset 508h	0h
50Ch	50Fh	Lane0 P5 and P6 Preset-Coefficient Mapping (L0P5P6PCM)—Offset 50Ch	0h
510h	513h	Lane0 P6, P7 and P8 Preset-Coefficient Mapping (L0P6P7P8PCM)—Offset 510h	0h
514h	517h	Lane0 P8 and P9 Preset-Coefficient Mapping (L0P8P9PCM)—Offset 514h	0h
518h	51Bh	Lane0 P10 Preset-Coefficient Mapping (L0P10PCM)—Offset 518h	0h
51Ch	51Fh	Lane0 LF and FS (L0LFFS)—Offset 51Ch	0h
520h	523h	Lane1 P0 and P1 Preset-Coefficient Mapping (L1P0P1PCM)—Offset 520h	0h
524h	527h	Lane1 P1, P2 and P3 Preset-Coefficient Mapping (L1P1P2P3PCM)—Offset 524h	0h
528h	52Bh	Lane1 P3 and P4 Preset-Coefficient Mapping (L1P3P4PCM)—Offset 528h	0h
52Ch	52Fh	Lane1 P5 and P6 Preset-Coefficient Mapping (L1P5P6PCM)—Offset 52Ch	0h
530h	533h	Lane1 P6, P7 and P8 Preset-Coefficient Mapping (L1P6P7P8PCM)—Offset 530h	0h
534h	537h	Lane1 P8 and P9 Preset-Coefficient Mapping (L1P8P9PCM)—Offset 534h	0h
538h	53Bh	Lane1 P10 Preset-Coefficient Mapping (L1P10PCM)—Offset 538h	0h
53Ch	53Fh	Lane1 LF and FS (L1LFFS)—Offset 53Ch	0h
540h	543h	Lane2 P0 and P1 Preset-Coefficient Mapping (L2P0P1PCM)—Offset 540h	0h
544h	547h	Lane2 P1, P2 and P3 Preset-Coefficient Mapping (L2P1P2P3PCM)—Offset 544h	0h
548h	54Bh	Lane2 P3 and P4 Preset-Coefficient Mapping (L2P3P4PCM)—Offset 548h	0h
54Ch	54Fh	Lane2 P5 and P6 Preset-Coefficient Mapping (L2P5P6PCM)—Offset 54Ch	0h
550h	553h	Lane2 P6, P7 and P8 Preset-Coefficient Mapping (L2P6P7P8PCM)—Offset 550h	0h
554h	557h	Lane2 P8 and P9 Preset-Coefficient Mapping (L2P8P9PCM)—Offset 554h	0h
558h	55Bh	Lane2 P10 Preset-Coefficient Mapping (L2P10PCM)—Offset 558h	0h
55Ch	55Fh	Lane2 LF and FS (L2LFFS)—Offset 55Ch	0h
560h	563h	Lane3 P0 and P1 Preset-Coefficient Mapping (L3P0P1PCM)—Offset 560h	0h
564h	567h	Lane3 P1, P2 and P3 Preset-Coefficient Mapping (L3P1P2P3PCM)—Offset 564h	0h
568h	56Bh	Lane3 P3 and P4 Preset-Coefficient Mapping (L3P3P4PCM)—Offset 568h	0h
56Ch	56Fh	Lane3 P5 and P6 Preset-Coefficient Mapping (L3P5P6PCM)—Offset 56Ch	0h
570h	573h	Lane3 P6, P7 and P8 Preset-Coefficient Mapping (L3P6P7P8PCM)—Offset 570h	0h
574h	577h	Lane3 P8 and P9 Preset-Coefficient Mapping (L3P8P9PCM)—Offset 574h	0h
578h	57Bh	Lane3 P10 Preset-Coefficient Mapping (L3P10PCM)—Offset 578h	0h
57Ch	57Fh	Lane3 LF and FS (L3LFFS)—Offset 57Ch	0h

17.3.1 Device Command; Primary Status (CMD_PSTS)—Offset 4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**DPE - Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if CMD.PERE is not set.
30	0h RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
26:25	0h RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved per PCI-Express spec
24	0h RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and CMD.PERE is set.
23	0h RO	**Primary Fast Back to Back Capable (PFBC):** Reserved per PCI-Express spec.
22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Primary 66 MHz Capable (PC66):** Reserved per PCI-Express spec.
20	1h RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list.
19	0h RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID.
18:16	0h RO	**Reserved (RSVD_1):** Reserved
15:11	0h RO	**Reserved (RSVD_2):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec.
8	0h RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0h RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec.
6	0h RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** Reserved per PCI-Express spec.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec.
3	0h RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec.
2	0h RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0h RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0h RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone..

17.3.2 Revision ID;Class Code (RID_CC)—Offset 8h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 60400F0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	6h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	4h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h.
15:8	0h RO/V	**Programming Interface (PI):** The value reported in this register is a function of the Decode Control.Subtractive Decode Enable (SDE) register. SDE Value reported in this register 0: 00h 1: 01h
7:0	F0h RO/V	**Revision ID (RID):** Indicates the revision of the bridge.

17.3.3 Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 810000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved
23	1h RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device.
22:16	1h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h.
15:11	0h RO	**Latency Count (CT):** Reserved per PCI-Express spec
10:8	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec

17.3.4 Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V2	**Secodary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	0h RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.
15:8	0h RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port.
7:0	0h RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

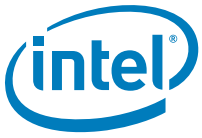
17.3.5 I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
30	0h RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with 'Unsupported Request' status from the device.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with 'Completion Abort' status from the device.



Bit Range	Default & Access	Field Name (ID): Description
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with 'Completion Abort' status to the device.
26:25	0h RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.
23	0h RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec
20:16	0h RO	**Reserved (RSVD_1):** Reserved
15:12	0h RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing.

17.3.6 Memory Base and Limit (MBL)—Offset 20h

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is MB [gt]= AD[lb]31:20[rb] [lt]= ML.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	0h RO	**Reserved (RSVD):** Reserved
15:4	0h RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	0h RO	**Reserved (RSVD_1):** Reserved

17.3.7 Prefetchable Memory Base and Limit (PMBL)—Offset 24h

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB [gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 10001h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing.
15:4	0h RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	1h RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing.

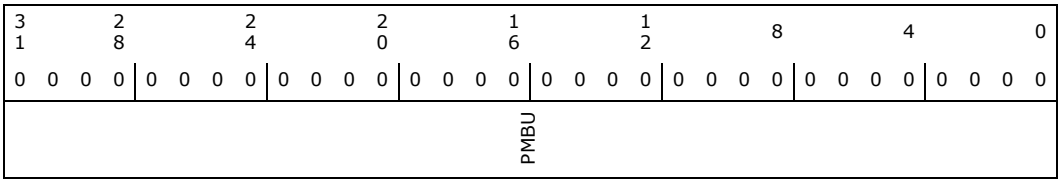
17.3.8 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.

17.3.9 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

17.3.10 Capabilities List Pointer (CAPP)—Offset 34h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 40h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	40h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) OffsetCapability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI) 90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List OffsetCapability Next Pointer 100h Advanced Error Reporting 000h

17.3.11 Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD):** Reserved
27	0h RW/V2	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
26	0h RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set.
25	0h RW/V2	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW/V2	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
23	0h RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec.
22	0h RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port.
21	0h RW/V2	**Master Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
20	0h RW	**VGA 16-Bit Decode (V16):** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.
19	0h RW	**VGA Enable (VE):** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h 3BBh and 3C0h 3DFh, and all aliases of bits 15:10 in any combination of 1's
18	0h RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
17	0h RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
16	0h RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG register in chipset config space: Port Bits[lb]15:12[rb] Bits[lb]11:08[rb] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP 4 0h STRPFUSECFG.P4IP 5 0h STRPFUSECFG.P5IP 6 0h STRPFUSECFG.P6IP 7 0h STRPFUSECFG.P7IP 8 0h STRPFUSECFG.P8IP The value that is programmed into STRPFUSECFG.PxIP is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above.
7:0	0h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

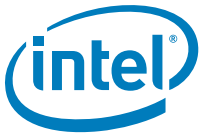
17.3.12 Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 428010h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved
30	0h RO	**Reserved (RSVD_1):** Reserved. This register at one time was for TCS Routing but that was later removed from the PCIe 2.0 spec
29:25	0h RO	**Interrupt Message Number (IMN):** The root port does not have multiple MSI interrupt numbers.
24	0h RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
23:20	4h RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port



Bit Range	Default & Access	Field Name (ID): Description
19:16	2h RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 specification which incorporates the Register Expansion ECN.
15:8	80h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h RO	**Capability ID (CID):** Indicates this is a PCI Express capability

17.3.13 Device Capabilities (DCAP)—Offset 44h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 8001h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD):** Reserved
28	0h RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports
27:26	0h RO	**Captured Slot Power Limit Scale (CSPS):** Not supported
25:18	0h RO	**Captured Slot Power Limit Value (CSPV):** Not supported
17:16	0h RO	**Reserved (RSVD_1):** Reserved
15	1h RO	**Role Based Error Reporting (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.
14	0h RO	**Reserved (RSVD_2):** Reserved. On previous version of the specification this was Power Indicator Present (PIP)
13	0h RO	**Reserved (RSVD_3):** Reserved. On previous version of the specification this was Attention Indicator Present (AIP)

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**Reserved (RSVD_4):** Reserved. On previous version of the specification this was Attention Button Present (ABP)
11:9	0h RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports.
8:6	0h RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port.
5	0h RO	**Extended Tag Field Supported (ETFS):** The root port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	0h RO	**Phantom Functions Supported (PFS):** No phantom functions supported
2:0	1h RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Only Max Payload Size of up to 256B is supported. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface.

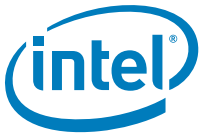
17.3.14 Device Control; Device Status (DCTL_DSTS)—Offset 48h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
20	1h RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup



Bit Range	Default & Access	Field Name (ID): Description
19	0h RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
18	0h RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp
17	0h RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout
16	0h RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout.
15	0h RO	**Reserved (RSVD_1):** Reserved
14:12	0h RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface.
11	0h RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.
10	0h RW/P	**Aux Power PM Enable (APME):** The OS will set this bit to '1' if the device connected has detected aux power.
9	0h RO	**Phantom Functions Enable (PFE):** Not supported
8	0h RO	**Extended Tag Field Enable (ETFE):** Not supported
7:5	0h RW	**Max Payload Size (MPS):** The root port only supports up to 256B max payload. Programming this field to any values other than 128B or 256B max payload size will result in aliasing to 128B max payload size. If the DCAP.MPS indicates 128B max payload size support, programming this field to any values other than 128B will result in aliasing to 128B max payload size. Programming this field to any values greater than DCAP.MPS will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME.
4	0h RO	**Enable Relaxed Ordering (ERO):** Not supported

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0h RW	**Fatal Error Reporting Enable (FEE):** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0h RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0h RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

17.3.15 Link Capabilities (LCAP)—Offset 4Ch

Access Method

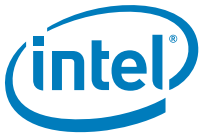
Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 710C00h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h
23	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
22	1h RW/O	**ASPM Optionality Compliance (ASPMOC):** ASPM Optionality Compliance(ASPMOC): This bit must be set to 1b for PCIe 3.0 compliant port. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests.
21	1h RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1h RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0h RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the root port does not support Surprise Down Error Reporting
18	0h RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism.
17:15	2h RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b Less than 1 us 001b 1 us to less than 2 us 010b 2 us to less than 4 us 011b 4 us to less than 8 us 100b 8 us to less than 16 us 101b 16 us to less than 32 us 110b 32 us to 64 us 111b More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency.
14:12	0h RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL

Bit Range	Default & Access	Field Name (ID): Description
11:10	3h RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 No ASPM Supported 01 L0s Supported 10 L1 Supported 11 L0s and L1 supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is '01'. Otherwise, the default of this field is '11'. If STRPFUSECFG.ASPMDIS is 1, BIOS writing '11' to this field will have the same effect as writing '01'. '01' will be reflected on this register when read and the register will turn to Read-Only once written once.
9:4	0h RO/V	**Maximum Link Width (MLW):** For the root ports, several values can be taken, based upon the value of the chipset configuration register field RPC.PC1 for ports 1-4: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h



Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RO/V	**Max Link Speeds (MLS):** Indicates the supported link speeds of the Root Port. 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5GT/s Link speeds supported This register reports a value of 0001b if the Root Port Gen2 Disable Fuse is set or the MPC.PCIEGEN2DIS bit is set, else this register reports a value of 0010b. Max Link Speeds (MLS): This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. This register reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through Fuse or MPC.PCIESD register. This register reports a value of 0010b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through Fuse or MPC.PCIESD register.

17.3.16 Link Control; Link Status (LCTL_LSTS)—Offset 50h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
29	0h RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.
28	0h RO/V	**Slot Clock Configuration (SCC):** In normal mode, root port uses the same reference clock as on the platform and does not generate its own clock. Note: The default of this register bit is dependent on the 'PCIe Non-Common Clock With SSC Mode Enable Strap'. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'.
27	0h RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
26	0h RO	**Reserved (RSVD):** Reserved. Previously this was defined as Link Training Error (LTE) but support for this bit was removed from subsequent versions of the PCI Express specification.
25:20	0h RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained.

Bit Range	Default & Access	Field Name (ID): Description
19:16	1h RO/V	**Current Link Speed (CLS):** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link This field indicates the negotiated Link speed of the given link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. The value of this field is undefined if the link is not up.
15:12	0h RO	**Reserved (RSVD_1):** Reserved
11	0h RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.
10	0h RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.
9	0h RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. Note: When operating as PCI Express, this bit defines the value of the Link Upconfigure Capability in TS2 Ordered Sets.
8	0h RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on Root Ports.
7	0h RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. Note: This functionality is not applicable for Mobile Express.
6	0h RW	**Common Clock Configuration (CCC):** When set, indicates that the root port and device are operating with a distributed common reference clock.

Bit Range	Default & Access	Field Name (ID): Description
5	0h WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0h RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state.
3	0h RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0h RO	**Reserved (RSVD_2):** Reserved
1:0	0h RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see '00' as an output from this register. BIOS reading this register should always return the correct value.

17.3.17 Slot Capabilities (SLCAP)—Offset 54h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 40060h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/O	**Physical Slot Number (PSN__31_24):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
23:19	0h RW/O	**Physical Slot Number (PSN__23_19):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.

Bit Range	Default & Access	Field Name (ID): Description
18	1h RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0h RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented.
16:15	0h RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:8	0h RW/O	**Slot Power Limit Value (SLV__14_8):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
7	0h RW/O	**Slot Power Limit Value (SLV__7_7):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1h RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported.
5	1h RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification.
4	0h RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot.
3	0h RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot.
2	0h RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present
1	0h RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot
0	0h RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot.

17.3.18 Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved (RSVD):** Reserved
24	0h RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
23	0h RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock.
22	0h RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'.
21	0h RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented.
20	0h RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller..
19	0h RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the SLSTS.PDS bit changes state.
18	0h RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented.
17	0h RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented.
16	0h RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button
15:13	0h RO	**Reserved (RSVD_1):** Reserved
12	0h RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed
11	0h RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock.
10	0h RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug.
9:8	0h RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller..
7:6	0h RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller..
5	0h RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0h RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller..

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state.
2	0h RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller..
1	0h RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller...
0	0h RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller..

17.3.19 Root Control (RCTL)—Offset 5Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:4	0h RO	**Reserved (RSVD_1):** Reserved
3	0h RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set).
2	0h RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0h RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0h RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

17.3.20 Root Status (RSTS)—Offset 60h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17	0h RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. Root ports have a one deep PME pending queue.
16	0h RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0h RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

17.3.21 Device Capabilities 2 (DCAP2)—Offset 64h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 80837h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved (RSVD):** Reserved
19:18	2h RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported.
17:12	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/ disable the root port from declaring support for the LTR capability.
10:6	0h RO	**Reserved (RSVD_2):** Reserved
5	1h RO	**ARI Forwarding Supported (AFS):** ARI Forwarding Supported (AFS): Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. Note: This bit is not made RWO to simplify implementation, since there is a requirement that the ARI Forwarding Enable bit must be hardwired to 0b if ARI Forwarding Supported bit is 0b. It is low risk to keep this risk 1b.
4	1h RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	7h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C 0111b Ranges A, B [amp] C [lt]-- This is what PCH supports 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved.

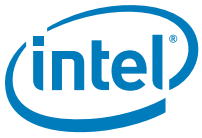
17.3.22 Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15	0h RO	**Reserved (RSVD_1):** Reserved
14:13	0h RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** 00b Disable OBFF mechanism. 01b Enable OBFF mechanism using Message signaling (Variation A). 10b Enable OBFF mechanism using Message signaling (Variation B). 11b Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect.
12:11	0h RO	**Reserved (RSVD_2):** Reserved
10	0h RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:6	0h RO	**Reserved (RSVD_3):** Reserved
5	0h RW	**ARI Forwarding Enable (AFE):** ARI Forwarding Enable (AFE): When set, the Downstream Port disables its traditional Device Number field being 0b enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port.
4	0h RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.



Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The root port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 us to 100 us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either when this value was changed or when each request was issued.

17.3.23 Link Capabilities 2 (LCAP2)—Offset 6Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved (RSVD):** Reserved
22:16	0h RO	**Lower SKP OS Reception Supported Speeds Vector (LSOSRSS):** Lower SKP OS Reception Supported Speeds Vector(LSOSRSS): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
15:9	0h RO	**Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV):** Lower SKP OS Generation Supported Speeds Vector(LSOSGSSV): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
8	0h RO	**Crosslink Supported (CS):** Crosslink Supported (CS): No support for Crosslink.
7:1	0h RO/V	**Supported Link Speeds Vector (SLSV):** Supported Link Speeds Vector (SLSV): This field indicates the supported Link speed of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. Bit definitions within this field are: Bit 0: 2.5 GT/s. Bit 1: 5.0 GT/s. Bit 2: 8.0 GT/s. Bits 6:3: Reserved. This register reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through Fuse or MPC.PCIESD register. This register reports a value of 0011b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through Fuse or MPC.PCIESD register.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**Reserved (RSVD_1):** Reserved

17.3.24 Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h

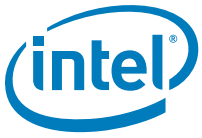
Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/1C/V/P	**Link Equalization Request (LER):** Link Equalization Request (LER): This bit is set by hardware to request the Link equalization process to be performed on the Link. Register Attribute: Dynamic.
20	0h RO/V/P	**Equalization Phase 3 Successful (EQP3S):** Equalization Phase 3 Successful (EQP3S): When set to 1, this bit indicates that Phase 3 of the Transmitter Equalization procedure has successfully completed.
19	0h RO/V/P	**Equalization Phase 2 Successful (EQP2S):** Equalization Phase 2 Successful (EQP2S): When set to 1, this bit indicates that Phase 2 of the Transmitter Equalization procedure has successfully completed.
18	0h RO/V/P	**Equalization Phase 1 Successful (EQP1S):** Equalization Phase 1 Successful (EQP1S): When set to 1, this bit indicates that Phase 1 of the Transmitter Equalization procedure has successfully completed.
17	0h RO/V/P	**Equalization Complete (EqC):** Equalization Complete (EC): When set to 1, this bit indicates that the Transmitter Equalization procedure has completed
16	0h RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/P	**Compliance Preset/De-emphasis (CD):** For 8.0 GT/s Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b -3.5 dB 0000b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. The default value of this field is 0000b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value.
11	0h RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only.
10	0h RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.



Bit Range	Default & Access	Field Name (ID): Description
9:7	0h RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0h RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5	0h RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value.
3:0	0h RW/V/P	**Target Link Speed (TLS):** Target Link Speed (TLS): This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. If a value is written to this field that does not correspond to a supported speed, as indicated by the Supported Link Speeds Vector, the result is undefined. The default value of this field is GEN1. Note: This register field could be used by REUT software to limit the link speed to 2.5 GT/s or 5 GT/s data rate.

17.3.25 Slot Capabilities 2 (SLCAP2)—Offset 74h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved (RSVD):** Reserved

17.3.26 Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:0	0h RO	**Reserved (RSVD_1):** Reserved

17.3.27 Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 9005h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved
23	0h RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
22:20	0h RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
19:17	0h RO	**Multiple Message Capable (MMC):** Only one message is required.
16	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.

Bit Range	Default & Access	Field Name (ID): Description
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	5h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

17.3.28 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction.

17.3.29 Subsystem Vendor Capability (SVCAP)—Offset 90h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: A00Dh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

17.3.30 Subsystem Vendor IDs (SVID)—Offset 94h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

17.3.31 Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: C8030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	19h RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Microsoft operating systems to enable PME# in devices connected behind this root port.
26	0h RO	**D2_Support (D2S):** The D2 state is not supported.
25	0h RO	**D1_Support (D1S):** The D1 state is not supported.
24:22	0h RO	**Aux_Current (AC):** Reports 0mA (self-powered), as use of this controller does not add to suspect well power consumption.
21	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
20	0h RO	**Reserved (RSVD):** Reserved
19	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
18:16	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	1h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

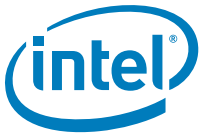
17.3.32 PCI Power Management Control And Status (PMCS)—Offset A4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Data (DTA):** Reserved
23	0h RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification
22	0h RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification.
21:16	0h RO	**Reserved (RSVD):** Reserved
15	0h RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.



Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0h RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Microsoft operating systems to enable PME# on devices connected to this root port.
7:4	0h RO	**Reserved (RSVD_1):** Reserved
3	1h RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved (RSVD_2):** Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 D0 state 11 D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

17.3.33 Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h

Size:32 bits
The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list.
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

17.3.34 Uncorrectable Error Status (UES)—Offset 104h

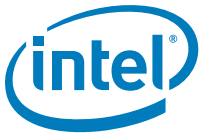
This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/1C/V/P	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0h RW/1C/V/P	**Completor Abort Status (CA):** Indicates a completer abort was received



Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Not supported.
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RO	**Training Error Status (TE):** Not supported.

17.3.35 Uncorrectable Error Mask (UEM)—Offset 108h

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/P	**ACS Violation Mask (AVM):** Reserved. Access Control Services are not supported
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0h RW/P	**Completor Abort Mask (CM):** Mask for completer abort.
14	0h RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.
13	0h RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RO	**Training Error Mask (TE):** Not supported.

17.3.36 Uncorrectable Error Severity (UEV)—Offset 10Ch

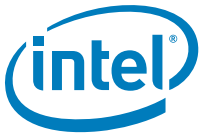
This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 60011h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/P	**ACS Violation Severity (AVS):** Severity for ACS violation.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	1h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.



Bit Range	Default & Access	Field Name (ID): Description
17	1h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0h RW/P	**Completor Abort Severity (CA):** Severity for completer abort.
14	0h RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	1h RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation..

17.3.37 Correctable Error Status (CES)—Offset 110h

This register is only reset by a loss of core power

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved (RSVD):** Reserved
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

17.3.38 Correctable Error Mask (CEM)—Offset 114h

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved (RSVD):** Reserved
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	**Reserved (RSVD_1):** Reserved
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.

Bit Range	Default & Access	Field Name (ID): Description
5:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

17.3.39 Advanced Error Capabilities and Control (AECC)—Offset 118h

This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved (RSVD):** Reserved
8	0h RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0h RO	**ECRC Check Capable (ECC):** ECRC is not supported.
6	0h RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0h RO	**ECRC Generation Capable (EGC):** ECRC is not supported.
4:0	0h RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

17.3.40 Header Log DW1 (HL_DW1)—Offset 11Ch

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**1st dWord of TLP (DW1):** Byte0 [amp][amp] Byte1 [amp][amp] Byte2 [amp][amp] Byte3

17.3.41 Header Log DW2 (HL_DW2)—Offset 120h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**2nd dWord of TLP (DW2):** Byte4 [amp][amp] Byte5 [amp][amp] Byte6 [amp][amp] Byte7

17.3.42 Header Log DW3 (HL_DW3)—Offset 124h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**3rd dWord of TLP (DW3):** Byte8 [amp][amp] Byte9 [amp][amp] Byte10 [amp][amp] Byte11

17.3.43 Header Log DW4 (HL_DW4)—Offset 128h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**4th dWord of TLP (DW4):** Byte12 [amp][amp] Byte13 [amp][amp] Byte14 [amp][amp] Byte15

17.3.44 Root Error Command (REC)—Offset 12Ch

This register allows errors to generate interrupts.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved (RSVD):** Reserved
2	0h RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0h RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0h RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

17.3.45 Error Source Identification (ESID)—Offset 134h

Size:32 bits
Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set.
15:0	0h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set.

17.3.46 ACS Extended Capability Header (ACSECH)—Offset 140h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support ACS Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support ACS Extended Capability, BIOS should write a 000Dh to this register else it should write 0.

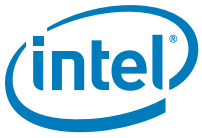
17.3.47 ACS Capability Register (ACSCAPR)—Offset 144h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: Fh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD_1):** Reserved for Egress Control Vector Size. This field is not applicable since ACS P2P Egress Control is not supported.
7	0h RO	**Reserved (RSVD_2):** Reserved
6	0h RO	**ACS Direct Translated P2P (T):** ACS Direct Translated P2P (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control (E):** ACS P2P Egress Control (E): ACS P2P Egress Control is not supported.
4	0h RO	**ACS Upstream Forwarding (U):** ACS Upstream Forwarding (U): ACS Upstream Forwarding is not supported.
3	1h RW/O	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Required for all Functions that support ACS P2P Request Redirect; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Completion Redirect.
2	1h RW/O	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Required for Root Ports that support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports; required for multi-function device Functions that support peer-to-peer traffic with other Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Request Redirect.
1	1h RW/O	**ACS Translation Blocking (B):** ACS Translation Blocking (B): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Translation Blocking.
0	1h RW/O	**ACS Source Validation (V):** ACS Source Validation (V): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Source Validation.

17.3.48 ACS Control Register (ACSCTLR)—Offset 148h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RSVD):** Reserved,
6	0h RO	**ACS Direct Translated P2P Enable (T):** ACS Direct Translated P2P Enable (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control Enable (E):** ACS P2P Egress Control Enable (E): ACS P2P Egress Control is not supported.
4	0h RO	**ACS Upstream Forwarding Enable (U):** ACS Upstream Forwarding Enable (U): ACS Upstream Forwarding is not supported.
3	0h RW	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Determines when the component redirects peer-to-peer Completions upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear.
2	0h RW	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Determines when the component redirects peer-to-peer memory Requests targeting another peer port upstream. I/O, Configuration, VDM Messages and Completions are never affected by ACS P2P Request Redirect.
1	0h RW	**ACS Translation Blocking (B):** ACS Translation Blocking (B): When set, the component blocks all upstream Memory Requests whose Address Translation (AT) field is not set to the default value. I/O, Configuration, Completions and Messages are never affected by ACS Translation Blocking.
0	0h RW	**ACS Source Validation (V):** ACS Source Validation (V): When set, the component validates the Bus Number from the Requester ID of upstream Requests against the secondary / subordinate Bus Numbers. I/O, Configuration and Completions are never affected by ACS Source Validation.

17.3.49 PTM Extended Capability Header (PTMECH)—Offset 150h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support PTM Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support PTM Extended Capability, BIOS should write a 001Fh to this register else it should write 0.

17.3.50 PTM Capability Register (PTMCAPR)—Offset 154h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 400h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved,
15:8	4h RW/O	**Local Clock Granularity (LCG):** Local Clock Granularity(LCG): 0000 0000b - Time Source does not implement a local clock. It simply propagates timing information obtained from further Upstream in the PTM Hierarchy when responding to PTM Request messages. 0000 0001b - 1111 1110b: Indicates the period of this Time Sources local clock in ns. 1111 1111b: Indicates the period of this Time Sources local clock is greater than 254 ns. If the PTM Root Select bit is Set, this local clock is used to provide PTM Master Time. Otherwise, the Time Source uses this local clock to locally track PTM Master Time received from further Upstream within a PTM Hierarchy.
7:3	0h RO	**Reserved (RSVD_1):** Reserved,
2	0h RW/O	**PTM Root Capable (PTMRC):** PTM Root Capable(PTMRC): Root Ports must set this bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW/O	**PTM Responder Capable (PTMRSPC):** PTM Responder Capable(PTMRSPC): Root Ports are permitted to set this bit to 1b to indicate that they implement the PTM Responder role.
0	0h RO	**PTM Requester Capable (PTMREQC):** PTM Requester Capable(PTMREQC): PTM Requester Role is not supported by Root Port.

17.3.51 PTM Control Register (PTMCTLR)—Offset 158h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:8	0h RO	**Effective Granularity (EG):** Effective Granularity(EG): Root Port does not support PTM Requester role.
7:2	0h RO	**Reserved (RSVD_1):** Reserved.
1	0h RW	**Root Select (RS):** Root Select(RS): When Set, if the PTM Enable bit is also Set, this Time Source is the PTM Root. Within each PTM Hierarchy, it is recommended that system software select only the furthest Upstream Time Source to be the PTM Root.
0	0h RW	**PTM Enable (PTME):** PTM Enable(PTME): When Set, this Function is permitted to participate in the PTM mechanism according to its selected role. Software must not have the PTM Enable bit Set in the PTM Control register on a Function associated with an Upstream Port unless the associated Downstream Port on the Link already has the PTM Enable bit Set in its associated PTM Control register. Register Attribute: Static.

17.3.52 L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h

Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 1h
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 001Eh. .

17.3.53 L1 Sub-States Capabilities (L1SCAP)—Offset 204h

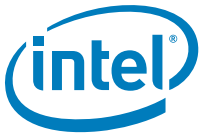
Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 28281Fh

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
23:19	5h RW/O	**Port Tpower_on Value (PTV):** Along with the Port T_POWER_ON Scale Field in the L1 Substates Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF.
18	0h RO	**Reserved (RSVD_1):** Reserved.
17:16	0h RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Substates Capabilities register. '00b': 2 us '01b': 10 us '10b': 100 us '11b': Reserved Required for all Ports that support L1.OFF.
15:8	28h RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF.
7:5	0h RO	**Reserved (RSVD_2):** Reserved
4	1h RW/O	**L1 PM Substates Supported (L1PSS):** When Set this bit indicates that this Port supports L1 PM Substates. For compatibility with possible future extensions, software must not enable L1 PM Substates unless this bit is set. This RWO field must be programmed prior to enabling ASPM.
3	1h RW/O	**ASPM L1.1 Substates Supported (AL11S):** When set, this bit indicates that this port supports L1 substates for ASPM L1.SNOOZ. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
2	1h RW/O	**ASPM L1.2 Supported (AL12S):** When set, this bit indicates that ASPM_L1.OFF is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
1	1h RW/O	**PCI-PM L1.1 Supported (PPL11S):** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static



Bit Range	Default & Access	Field Name (ID): Description
0	1h RW/O	**PCI-PM L1.2 Supported (PPL12S):** When set, this bit indicates that L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

17.3.54 L1 Sub-States Control 1 (L1SCTL1)—Offset 208h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**L1.2 LTR Threshold Latency ScaleValue (L12LTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe root port. The value in this field, together with L12LTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L12LTRSTLV times 1 ns 001: L12LTRSTLV times 32 ns 010: L12LTRSTLV times 1024 ns 011: L12LTRSTLV times 32768 ns 100: L12LTRSTLV times 1048576 ns 101: L12LTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
28:26	0h RO	**Reserved (RSVD):** Reserved
25:16	0h RW	**L1.2 LTR Threshold Latency Value (L12OFFLTRTLV):** This field contains the L1.2 LTR Threshold Latency Value for this particular PCIe root port. The value in this field, together with L12LTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
15:8	0h RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time the PCIe root port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved (RSVD_1):** Reserved
3	0h RW	**ASPM L1.1 Enabled (AL11E):** When set, this bit indicates that ASPM L1.SNOOZ substates are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic
2	0h RW	**ASPM L1.2 Enable (AL12E):** When set, this bit indicates that ASPM L1.OFF substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic
1	0h RW	**PCI-PM L1.SNOOZ Enable (PPL11E):** When set, this bit indicates that PCI-PM L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
0	0h RW	**PCI-PM L1.2 Enabled (PPL12E):** When set, this bit indicates that PCI-PM L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.

17.3.55 L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 28h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:3	5h RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# is sampled asserts in L1.OFF state. Tpower_on value is calculated by multiplying the value in this field by the value in the TPOS field. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
2	0h RO	**Reserved (RSVD_1):** Reserved
1:0	0h RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. '00b': 2 us '01b': 10 us '10b': 100us '11b': Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static

17.3.56 Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h

Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEECID):** PCI Express Extended Capability ID (PCIEECID): This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 0019h to this register else it should write 0.

17.3.57 Link Control 3 (LCTL3)—Offset 224h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:9	0h RO	**Enable Lower SKP OS Generation Vector (ELSOSGV):** Enable Lower SKP OS Generation Vector(ELSOSGV): When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is Set in this field and the corresponding bit in the Lower SKP OS Generation Supported Speeds Vector is not set.
8:2	0h RO	**Reserved (RSVD_1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Link Equalization Request Interrupt Enable (LERIE):** Link Equalization Request Interrupt Enable (LERIE): When set, this bit enables the generation of an interrupt to indicate that the Link Equalization Request bit has been set.
0	0h RW	**Perform Equalization (PE):** Perform Equalization (PE): When this bit is 1b and Link Retrain bit is set with the Target Link Speed field set to 8 GT/s, the Downstream Port must perform Link Equalization. This bit is cleared by Root Port upon entry to Link Equalization

17.3.58 Lane Error Status (LES)—Offset 228h

The Lane number is the default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD):** Reserved
3	0h RW/1C/V/P	**Lane 3 Error Status (L3ES):** Lane 3 Error Status (L3ES): Lane 3 detected a Lane-based error.
2	0h RW/1C/V/P	**Lane 2 Error Status (L2ES):** Lane 2 Error Status (L2ES): Lane 2 detected a Lane-based error.
1	0h RW/1C/V/P	**Lane 1 Error Status (L1ES):** Lane 1 Error Status (L1ES): Lane 1 detected a Lane-based error.
0	0h RW/1C/V/P	**Lane 0 Error Status (L0ES):** Lane 0 Error Status (L0ES): Lane 0 detected a Lane-based error.

17.3.59 Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 7F7F7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved.
30:28	7h RW	**Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH):** Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 1 Transmitter Preset (UPL1TP):** Upstream Port Lane 1 Transmitter Preset (UPL1TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	**Reserved (RSVD_1):** Reserved.
22:20	7h RW	**Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH):** Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 1 Transmitter Preset (DPL1TP):** Downstream Port Lane 1 Transmitter Preset (DPL1TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved (RSVD_2):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
14:12	7h RW	**Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH):** Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 0 Transmitter Preset (UPL0TP):** Upstream Port Lane 0 Transmitter Preset (UPL0TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	**Reserved (RSVD_3):** Reserved.
6:4	7h RW	**Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH):** Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 0 Transmitter Preset (DPL0TP):** Downstream Port Lane 0 Transmitter Preset (DPL0TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

17.3.60 Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 7F7F7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
30:28	7h RW	**Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH):** Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 3 Transmitter Preset (UPL3TP):** Upstream Port Lane 3 Transmitter Preset (UPL3TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	**Reserved (RSVD_1):** Reserved
22:20	7h RW	**Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH):** Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 3 Transmitter Preset (DPL3TP):** Downstream Port Lane 3 Transmitter Preset (DPL3TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved (RSVD_2):** Reserved
14:12	7h RW	**Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH):** Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 2 Transmitter Preset (UPL2TP):** Upstream Port Lane 2 Transmitter Preset (UPL2TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	**Reserved (RSVD_3):** Reserved
6:4	7h RW	**Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH):** Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
3:0	Fh RW	**Downstream Port Lane 2 Transmitter Preset (DPL2TP):** Downstream Port Lane 2 Transmitter Preset (DPL2TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

17.3.61 PCI Express Replay Timer Policy 1 (PCIERTP1)—Offset 300h

The Replay Timer controlled by the Replay Timeout field is started when the Retry Buffer is empty and a TLP is placed into it or an Ack/Nak DLLP is received and there are still non-acknowledged packets within the Retry Buffer. The counter continues to count until the next valid Ack DLLP or a NAK DLLP that acknowledges unacknowledged TLPs is received, or it reaches the timeout value specified by this register. When a valid Ack/Nak DLLP is received, the timer is reset to zero and restarted if there are still non-acknowledged packets within the Retry Buffer. Otherwise if the Retry Buffer is empty, the counter is just reset to zero. If the timer reaches the timeout value, the non-acknowledged packets within the Retry Buffer will be replayed.
The default for this register is dependent on the MAX_PAYLOAD_SIZE , the NEGOTIATED_WIDTH, and the NEGOTIATED_SPEED.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: A64F96h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved,
23:20	Ah RW	**Gen 2 x1 (G2X1):** Gen 2 x1 (G2X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 7) * 64 link clocks. For PCIE Gen 2 speed and x1 width For Mobile Express HS-Gear 3 speed and x1 width.

Bit Range	Default & Access	Field Name (ID): Description
19:16	6h RW	**Gen 2 x2 (G2X2):** Gen 2 x2 (G2X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 4) * 64 link clocks. For PCIe Gen 2 speed and x2 width. For Mobile Express HS-Gear 3 speed and x2 width.
15:12	4h RW	**Gen 2 x4 (G2X4):** Gen 2 x4 (G2X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 2 speed and x4 width. For Mobile Express HS-Gear 3 speed and x4 width.
11:8	Fh RW	**Gen 1 x1 (G1X1):** Gen 1 x1 (G1X1): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/ Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 10) * 64 link clocks. For 512B MPS: (nnn + 17) * 64 link clocks. For PCIe Gen 1 speed and x1 width. For Mobile Express HS-Gear 2 speed and x1 width.
7:4	9h RW	**Gen 1 x2 (G1X2):** Gen 1 x2 (G1X2): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/ Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For PCIe Gen 1 speed and x2 width. For Mobile Express HS-Gear 2 speed and x2 width.

Bit Range	Default & Access	Field Name (ID): Description
3:0	6h RW	**Gen 1 x4 (G1X4):** Gen 1 x4 (G1X4): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/ Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 1 speed and x4 width. For Mobile Express HS-Gear 2 speed and x4 width.

17.3.62 PCI Express Replay Timer Policy 2 (PCIERTP2)—Offset 304h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 1BC00B86h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Lane 0 Lane Number (L0LN):** Lane 0 Lane Number(L0LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 0 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
29:28	1h RW	**Lane 1 Lane Number (L1LN):** Lane 1 Lane Number(L1LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 1 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.

Bit Range	Default & Access	Field Name (ID): Description
27:26	2h RW	**Lane 2 Lane Number (L2LN):** Lane 2 Lane Number(L2LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 2 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
25:24	3h RW	**Lane 3 Lane Number (L3LN):** Lane 3 Lane Number(L3LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 3 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
23	1h RW	**Loopback Master EQ TS1 Enable (LMEQTS1E):** Loopback Master EQ TS1 Enable(LMEQTS1E): When set, the Loopback Master will use EQ TS1 Ordered Sets to direct the Loopback Slave into Loopback from Configuration.Linkwidth.Start. The Preset field of the EQ TS1 Ordered Sets will be specified by Upstream Port Lane X Transmitter Preset and Upstream Port Lane X Receiver Preset Hint fields in the Lane Equalization Control registers.
22	1h RW	**Loopback Master EQ Change Enable (LMEQCE):** Loopback Master EQ Change Enable(LMEQCE): This field is applicable to the case where Loopback is entered from Recovery state. When set, the Loopback Master will set the EC field of the GEN3 TS1 Ordered Sets to the appropriate value based on the ports direction(10b or 11b) to direct the Loopback Slave into Loopback from Recovery state. The Preset field of the GEN3 TS1 Ordered Sets will be specified by Upstream Port Lane X Transmitter Preset and Upstream Port Lane X Receiver Preset Hint fields in the Lane Equalization Control registers.
21:12	0h RO	**Reserved (RSVD):** Reserved
11:8	Bh RW	**Gen 3 x1 (G3X1):** Gen 3 x1 (G3X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For Gen 3 speed and x1 width

Bit Range	Default & Access	Field Name (ID): Description
7:4	8h RW	**Gen 3 x2 (G3X2):** Gen 3 x2 (G3X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For Gen 3 speed and x2 width
3:0	6h RW	**Gen 3 x4 (G3X4):** Gen 3 x4 (G3X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 1) * 64 link clocks. For 512B MPS: (nnn + 2) * 64 link clocks. For Gen 3 speed and x4 width

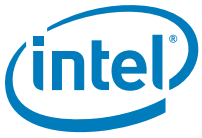
17.3.63 PCI Express Status 1 (PCIESTS1)—Offset 328h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LTSM State (LTSMSTATE):** Indicates the LTSM present state. Hex LTSSM States 00DETIDLE 01DETRDY 02DETIDLEP1TOP2 03DETRDYP2TOP1 04DETRDYINP1 05DETRDYINP1EXE 06DETP2POLLSTART 07DETP1POLLSTART 08DETP2TOP0 09DETP1TOP0 0AECPCMPRETRAIN 0BECPCMFAILP0TOP2 0CDETP0TOP2 0DPMODECHANGE 0EECPCMPCIE 0FECPCMUSB3 10DET2POLLINP0 11POLLINGACTIVE 12POLLINGCOMPLIANCEMARGINCNT 13POLLINGCOMPLIANCE 14POLLINGCOMPLIANCESPEEDUP 15POLLINGCOMPLIANCESPEEDDN 16POLLINGCOMPLIANCESPEEDTXEIDLE 17POLLINGCOMPLIANCESPEEDRXEIDLE 18POLLINGCOMPLIANCESPEED 19POLLINGCOMPLIANCESPEEDDONE 1APOLLINGCOMPLIANCEEXIT 1BPOLLINGCONFIGURATION 1CPOLLINGTXEIDLE 1DPOLLINGEND 1EPOLLINGENDWAIT 1FLINKWIDTHSTART 20LINKWIDTHACCEPT 21LANENUMWAIT 22LANENUMACCEPT 23LANEDESKEW 24CONFIGCOMPLETE 25CONFIGIDLE 26LWNEXITRECOVERY 27CONFIGLPBKENTRY 28CONFIGLPBKLWSTART 29CONFIGLPBKSPEEDTXEIDLE 2ACONFIGLPBKSPEEDSTART 2BCONFIGLPBKSPEEDRXEIDLE 2CCONFIGLPBKSPEED 2DCONFIGLPBKREUTSKIP 2ECONFIGLPBKREUT 2FCONFIGLPBKEXITM 30CONFIGLPBKTXEIDLE



Bit Range	Default & Access	Field Name (ID): Description
		31LWNEXIT 32LWNLNK2DETECT 33L0 34TXL0SRXL0 35RXL0STXL0 36TXL0SRXL0S 37L1TXEIDLE 38L1RCVEIDLE 39L1PREENTRY 3AL1ENTRY 3BL1IDLE 3CL1IDLEGEN2WAIT 3DL1EXIT 3EL2TXEIDLE 3FL2RCVEIDLE 40L2IDLEWAIT 41L2IDLERDY 42L2IDLE 43LOOPBACKENTRY 44LPBKACTIVEMTXSKP 45LPBKACTIVEMSKPDSKW 46LOOPBACKACTIVEM 47LPBKSLAVESPEEDTXEIDLE 48LPBKSLAVESPEEDRXEIDLE 49LPBKSLAVESPEED 4ALOOPBACKACTIVES 4BLOOPBACKCMMSKP 4CLOOPBACKCMM 4DLOOPBACKEXITM 4ELOOPBACKEXITS 4FLOOPBACKEXITL0 50LOOPBACKLNK2DETECT 51LOOPBACK2DETECT 52DISTX16TS1DIS 53DISTXEIDLE 54DISWAITSTART 55DISWAITGNT 56DISWAIT4TXMARGIN 57DISWAIT 58DIS2DETECT 59HOTRESETTS1 5AHOTRESETDONE 5BHOTRESETEIDLE 5CRECOVERYRCVRWAIT 5DRECOVERYRCVRMARGINCNT 5ERECOVERYRCVRLOCK 5FRECOVERYDESKEW 60RECOVERYRCVRCFG 61RECOVERYSPEED 62RECOVERYSPEEDTXEIDLE 63RECOVERYSPEEDRXEIDLE

Bit Range	Default & Access	Field Name (ID): Description
		64RECOVERYSPEEDREADY 65RECOVERYIDLE 66RECOVERYEXITDETECT 67RECOVERYLNK2DETECT 68RECOVERYEXITLPBK 69RECOVERYEXITL0 6ARECOVERYEXITDIS 6BRECOVERYEXITRST Note: This register field could be used by REUT software to monitor the link LTSSM substates.
23	0h RO	**Reserved (RSVD):** Reserved.
22:19	0h RO/V	**Link Status (LNKSTAT):** During Link initialization the Link will always traverse this list of state from the top (0000) to the bottom of the list (0111). One or more power management states may be skipped, but the direction of list traversal will remain the same. 0000 Link Down 0001 : Link Retrain 0011 : L1 0100 : L2 0101 : L3 0111 : L0 (Link Up) 1000 : L0s (Transmit [amp] Receive) 1001 : L0s (Transmit only) 1010 : L0s (Receive only) All others reserved
18:17	0h RO/V	**Replay Number (REPLAYNUM):** Number of times the Retry Buffer has been replayed since the last Link initialization / re-training. When the Data Link Layer has replayed the contents of the Retry Buffer four times a Link re-training will be initiated which will reset this value back to zero.
16	0h RO/V	**Data Link Layer Retry (DLLRETRY):** Indicates when the Data Link Layer has received a corrupted TLP or has detected a dropped packet and is currently waiting for the remote agent to re-transmit the corrupted/dropped packet. The value of Next Receive Sequence Number will be the sequence number associated with the corrupted packet.
15:12	0h RO/V	**Lane Status (LANESTAT):** Indicates which lanes are trained. A '1' indicates that the corresponding lane is trained (i.e. bit 0 = '1' means lane 0 is trained).
11:0	0h RO/V	**Next Transmitted Sequence Number (NXTTXSEQNUM):** This is the sequence number to be applied to and pre-pended to the next outgoing TLP.

17.3.64 PCI Express Status 2 (PCIESTS2)—Offset 32Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**PCIe Port 3 Non-Common Clock With SSC Mode Enable Strap (P3PNCCWSSCMES):** '0': PCIe port 3 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 3 is enabled to operate in non-common clock mode with SSC enabled.
30	0h RO/V	**PCIe Port 2 Non-Common Clock With SSC Mode Enable Strap (P2PNCCWSSCMES):** '0': PCIe port 2 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 2 is enabled to operate in non-common clock mode with SSC enabled.
29	0h RO/V	**PCIe Port 1 Non-Common Clock With SSC Mode Enable Strap (P1PNCCWSSCMES):** '0': PCIe port 1 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 1 is enabled to operate in non-common clock mode with SSC enabled.
28	0h RO/V	**PCIe Port 0 Non-Common Clock With SSC Mode Enable Strap (P0PNCCWSSCMES):** '0': PCIe port 0 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 0 is enabled to operate in non-common clock mode with SSC enabled.
27:16	0h RO/V	**Next Receive Sequence Number (NXTRCVSEQ):** This is the sequence number associated with the TLP that is expected to be received next.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/1C/V	**Cause of Last Recovery Event (CLRE):** Cause of Last Recovery Event (CLRE): This field logs the cause of the entry to Recovery from L0. Only the first cause of Recovery is captured, until the register is cleared. Encoding Recovery Event 0000 No Recovery. 0001 Recovery entry triggered by remote device. 0010 Link Layer initiated Link Retrain due to error. 0011 De-skew buffer full. 0100 L0s exit time-out. 0101 Elastic Buffer overrun/underrun. 0110 Triggered by speed change. 0111 Link upconfiguration/downconfiguration. 1000 L0 Electrical Idle Inference. 1001 Any of the Link Retrain, CMM Start, Hot Reset, Link Disable, REUT Loopback Master or REUT Forced Loopback Master bit set. 1010 Received EIOS for RXL0s entry when ASPM L0s is disabled. 1011 Entry to Recovery from RXL0s due to PME timeout. Others Reserved.
11:0	0h RO/V	**Last Acknowledged Sequence Number (LASTACKSEQNUM):** This is the sequence number associated with the last acknowledged TLP.

17.3.65 PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h

Note that selecting a lane number that does not exist for a port may result in undefined behavior.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 2A000016h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**GEN3 Intel CMM Scrambler Bypass (G3ICMMSB):** GEN3 Intel CMM Scrambler Bypass(G3ICMMSB): When set, the Intel CMM pattern will bypass scrambling in GEN3. This bit does not impact non Intel CMM pattern. The TSx and SOS prior to Intel CMM will still be scrambled normally. Note: This bit must be set prior to enabling Intel CMM, by setting the PCIECMMPC.START. Note: When operating in Mobile Express mode, this field is not applicable.
30	0h RO	**Reserved (RSVD):** Reserved
29	1h RW	**CMM Symbol[3] Select (SYM3SEL):** 0: selects CMM Symbol [lb]3[rb] to a control character 1: selects CMM Symbol [lb]3[rb] as a data character
28	0h RW	**CMM Symbol[2] Select (SYM2SEL):** 0: selects CMM Symbol [lb]2[rb] to a control character 1: selects CMM Symbol [lb]2[rb] as a data character
27	1h RW	**CMM Symbol[1] Select (SYM1SEL):** 0: selects CMM Symbol [lb]1[rb] to a control character 1: selects CMM Symbol [lb]1[rb] as a data character
26	0h RW	**CMM Symbol[0] Select (SYM0SEL):** 0: selects CMM Symbol [lb]0[rb] to a control character 1: selects CMM Symbol [lb]0[rb] as a data character
25:24	2h RW	**CMM Sync Header (CMMSH):** CMM Sync Header(CMMSH): Specifies the Sync Header for the Intel CMM pattern specified in PCIECMMSB. Note: Due to implementation limitation, only a value of 10b is supported. All the other values are not supported.
23:22	0h RO/V	**CMM Error Lane Number (ERRLANENUM):** This field contains the lane number of the failing lane. Only valid when CMM Error Detected is 1.
21:16	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO/V	**CMM Invert (INVERT):** Indicates which lanes are inverted 000: No inversion 001: Lanes 0 010: Lanes 1 011: Lanes 2 100: Lanes 3 This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated)
12:10	0h RO/V	**CMM Symbol Error Number Invert (SYMERRNUMINV):** Indicates which register number miscompared on the failing lane, if the failing lane was an inverted lane. Only valid when CMM Error Detected is 1. 000: CMM Data D0 001: CMM Data D0 010: CMM Data D0 011: CMM Data D1 100: CMM Data D2 101: CMM Data D3 110: CMM Data D0 111: CMM Data D0
9:8	0h RO/V	**CMM Symbol Error Number (SYMERRNUM):** Indicates which register number miscompared on the failing lane, if the failing lane was not inverted. Only valid when CMM Error Detected is 1. 00: CMM Data 0 01: CMM Data 1 10: CMM Data 2 11: CMM Data 3
7	0h RW/1C/V	**CMM Error Detected (ERRDET):** 1: An error was detected 0: No error detected Note: This bit will be shadowed to an observability pin that can be used for IRQ generation.
6:5	0h RW	**Select Lane Number to be inverted for CMM (SLNINVCMM):** Select Lane Number to be inverted for CMM
4	1h RW	**CMM AutoInvert (AUTOINVERT):** 1: CMM autosequences through the inversion 0: CMM does not sequence inversion
3	0h RO/V	**CMM Status (STAT):** This bit is set when the CMM Start bit is set and cleared when the CMM mode has been entered successfully. 0: Compliance Measurement Mode is not active or CMM mode has been entered successfully. 1: Set as a result of CMM Start bit being set.
2	1h RW	**CMM Invert Enable (INVEN):** 1: Enables the Inversion of the lane 0: Lane not inverted
1	1h RW	**Reserved (RSVD_2):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/L	**CMM Start (START):** 1: Start CMM 0: Stop CMM

17.3.66 PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 4ABCB5BCh

Bit Range	Default & Access	Field Name (ID): Description
31:24	4Ah RW	**CMM Data [3] (DATA3):** This character contains CMM Data [lb]3[rb] that will be transmitted on the link.
23:16	BCh RW	**CMM Data [2] (DATA2):** This character contains CMM Data [lb]2[rb] that will be transmitted on the link.
15:8	B5h RW	**CMM Data [1] (DATA1):** This character contains CMM Data [lb]1[rb] that will be transmitted on the link.
7:0	BCh RW	**CMM Data [0] (DATA0):** This character contains CMM Data [lb]0[rb] that will be transmitted on the link.

17.3.67 PTM Propagation Delay (PTMPD)—Offset 390h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Propagation Delay Value (CPTMPDV):** Current PTM Propagation Delay Value(CPTMPDV): This field reports the current PTM Propagation Delay value captured from the last successful PTM dialog.

17.3.68 PTM Lower Local Master Time (PTMLLMT)—Offset 394h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Lower Local Master Time Value (CPTMLLMTV):** Current PTM Lower Local Master Time Value(CPTMLLMTV): This field reports the lower fields bits 31:0 of the Local TSC time value.

17.3.69 PTM Upper Local Master Time (PTMULMT)—Offset 398h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Upper Local Master Time Value (CPTMULMTV):** Current PTM Upper Local Master Time Value(CPTMULMTV): This field reports the upper fields bits 63:32 of the Local TSC time value.

17.3.70 PTM Pipe Stage Delay Configuration 1 (PTMPSDC1)—Offset 39Ch

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN1 X2 RX Pipe Stage Delay (G1X2RPSD):** GEN1 X2 RX Pipe Stage Delay(G1X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN1 X2 TX Pipe Stage Delay (G1X2TPSD):** GEN1 X2 TX Pipe Stage Delay(G1X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN1 X1 RX Pipe Stage Delay (G1X1RPSD):** GEN1 X1 RX Pipe Stage Delay(G1X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN1 X1 TX Pipe Stage Delay (G1X1TPSD):** GEN1 X1 TX Pipe Stage Delay(G1X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.3.71 PTM Pipe Stage Delay Configuration 2 (PTMPSDC2)—Offset 3A0h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN2 X1 RX Pipe Stage Delay (G2X1RPSD):** GEN2 X1 RX Pipe Stage Delay(G2X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN2 X1 TX Pipe Stage Delay (G2X1TPSD):** GEN2 X1 TX Pipe Stage Delay(G2X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN1 X4 RX Pipe Stage Delay (G1X4RPSD):** GEN1 X4 RX Pipe Stage Delay(G1X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN1 X4 TX Pipe Stage Delay (G1X4TPSD):** GEN1 X4 TX Pipe Stage Delay(G1X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.3.72 PTM Pipe Stage Delay Configuration 3 (PTMPSDC3)—Offset 3A4h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN2 X4 RX Pipe Stage Delay (G2X4RPSD):** GEN2 X4 RX Pipe Stage Delay(G2X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN2 X4 TX Pipe Stage Delay (G2X4TPSD):** GEN2 X4 TX Pipe Stage Delay(G2X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN2 X2 RX Pipe Stage Delay (G2X2RPSD):** GEN2 X2 RX Pipe Stage Delay(G2X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN2 X2 TX Pipe Stage Delay (G2X2TPSD):** GEN2 X2 TX Pipe Stage Delay(G2X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.3.73 PTM Pipe Stage Delay Configuration 4 (PTMPSDC4)—Offset 3A8h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN3 X2 RX Pipe Stage Delay (G3X2RPSD):** GEN3 X2 RX Pipe Stage Delay(G3X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN3 X2 TX Pipe Stage Delay (G3X2TPSD):** GEN3 X2 TX Pipe Stage Delay(G3X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN3 X1 RX Pipe Stage Delay (G3X1RPSD):** GEN3 X1 RX Pipe Stage Delay(G3X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN3 X1 TX Pipe Stage Delay (G3X1TPSD):** GEN3 X1 TX Pipe Stage Delay(G3X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.3.74 PTM Pipe Stage Delay Configuration 5 (PTMPSDC5)—Offset 3ACh

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:8	0h RW	**GEN3 X4 RX Pipe Stage Delay (G3X4RPSD):** GEN3 X4 RX Pipe Stage Delay(G3X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN3 X4 TX Pipe Stage Delay (G3X4TPSD):** GEN3 X4 TX Pipe Stage Delay(G3X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.3.75 PTM Extended Config (PTMECFG)—Offset 3B0h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20:18	0h RW	**Periodic Local TSC Link Fetch Frequency (PLTLFF):** Periodic Local TSC Link Fetch Frequency (PLTLFF): When this register is programmed to a non-zero values, the Local TSC Link Clock would perform a periodic fetch to obtain the latest TSC from the Local TSC XTAL Clock domain. This mechanism would ensure the Root Port Local TSC Link is always synchronized with the actual TSC as Link Clock domain is able to drift due to SSC. 000: Disable this feature. 001: Always pull without waiting for expiration. 010: Every 8 clocks 011: Every 16 clocks 100: Every 32 clocks 101: Every 64 clocks 110: Every 128 clocks 111: Every 256 clocks This register is only available in Port 1. Note: Software is expected to program this register prior to setting PTM Enable.
17:15	0h RW/1C/V	**Global Time Fetch Retry Counter (GTFRC):** Global Time Fetch Retry Counter. This register is incremented when the Root Port detected a retry on each Global Time Fetch on IOSF Sideband. The Root Port would increment the value of this register whenever ARU re-sends a LocalSync message. If more than 7 Retries are detected during the Global Time Fetch, Root Port would keep the value of this register to 111 (max) value. Software is expected to write 111 to this register to clear the entire field to 0. Note: For each x4 instance, only the value from Port 1 is used.
14:13	0h RW/1C/V	**Global Time Fetch Fail Counter (GTFFC):** Global Time Fetch Fail Counter. This register is incremented when the Root Port detected a fail on each Global Time Fetch on IOSF Sideband. The Root Port would increment the value of this register whenever ARU sends a SyncComp with the Fail status. If more than 3 failures are detected in the Global Time Fetch, Root Port would keep the value of this register to 111 (max) value. Software is expected to write 11 to this register to clear the entire field to 0. Note: For each x4 instance, only the value from Port 1 is used.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Global Time Fetch Status Pending Completion (GTFSPC):** Global Time Fetch Status Pending Completion. This register is set to 1 by the Root Port when it is in progress of fetching the Global Time from ARU. Note: For each x4 instance, only the value from Port 1 is used.
11:9	0h RW	**Periodic Global Time Stamp Counter Fetch Frequency (PGTSCFF):** Periodic Global Time Stamp Counter Fetch Frequency (PGTSCFF) : This field determine the frequency the Root Port would autonomously fetch the Global Time Stamp Counter. 00: 10us 01: 100us 10: 500us 10: 1ms Software is expected to program this bit first before programming the PGTSCFE register. Attribute: Dynamic Note: For each x4 instance, only the value from Port 1 is used.
8	0h RW	**Periodic Global Time Stamp Counter Fetch Enable (PGTSCFE):** Periodic Global Time Stamp Counter Fetch Enable (PGTSCFE) : When this bit set, the Controller will re-fetch the Global Time from the Always Running Unit (ARU). Once Fetch is completed, the Controller would update all the Local TSC with the newly fetch Global Time. If any PTM dialog is initiated while the re-fetch occurred, the Controller would use the existing Local TSC timers. Hardware would clear this bit upon completed fetching the Global Time. Attribute : Dynamic Note: For each x4 instance, only the value from Port 1 is used.
7	0h RW	**Trigger Global Time Stamp Counter Fetch Enable (TGTSCFE):** Trigger Global Time Stamp Counter Fetch Enable (TGTSCFE) : When this bit set, the Controller will re-fetch the Global Time from the Always Running Unit (ARU). Once Fetch is completed, the Controller would update all the Local TSC with the newly fetch Global Time. If any PTM dialog is initiated while the re-fetch occurred, the Controller would use the existing Local TSC timers. Hardware would clear this bit upon completed fetching the Global Time. Software can only set this register if PGTSCFE is not set. Attribute : Dynamic Note: For each x4 instance, only the value from Port 1 is used.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**PTM Request Periodic ACK Enable (PTMRPAE):** PTM Request Periodic ACK Enable (PTMRPAE) : When this register is set to 1, whenever a valid PTM request TLP is received, the Link Layer would transmit multiple ACK DLLPs corresponding to the PTM Request message. The number of ACK DLLP that the Link Layer would transmit is based on the PTMRNOPAD register. Attribute : Static Note: For each x4 instance, only the value from Port 1 is used.
5:4	0h RW	**PTM Request Number Of Periodic ACK DLLP (PTMRNOPAD):** PTM Request Number Of Periodic ACK DLLP (PTMRNOPAD) : When PTMRPAE is enable, whenever a valid PTM Request message is received, the Link Layer would transmit multiple ACK DLLP corresponding to the receiving of the PTM Request message. This register define the number of DLLP ACK will be transmitted as high priority. 00 - TX 1 DLLP ACK 01 - TX 2 DLLP ACK 10 - TX 3 DLLP ACK 11 - TX 4 DLLP ACK Attribute : Static Note: For each x4 instance, only the value from Port 1 is used.
3:0	0h RW	**IOSF Max Allowed Delay programming (IOSFMADP):** IOSF Max Allowed Delay programming (IOSFMADP): bits Status 0000 Bound Range Low 0001 Bound Range 2 1000 Bound Range Max others reserved

17.3.76 PTM Lower T2 Time Stamp (PTMLT2TSTMP)—Offset 3B4h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Latest Captured Lower T2 TimeStamp (LCLT2TS):** Latest Captured Lower T2 TimeStamp (LCLT2TS). This field shows the latest lower 32-bit of T2 TimeStamp captured by the Root Port in TSC Clock Domain when the Root Port received a valid PTM Request message. The renewable T2 TimeStamp due to a duplicate PTM Request would also be reflected in this field.

17.3.77 PTM Upper T2 Time Stamp (PTMUT2TSTMP)—Offset 3B8h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Latest Captured Upper T2 TimeStamp (LCUT2TS):** Latest Captured Upper T2 TimeStamp (LCUT2TS). This field shows the latest upper 32-bit of T2 TimeStamp captured by the Root Port in TSC Clock Domain when the Root Port received a valid PTM Request message. The renewable T2 TimeStamp due to a duplicate PTM Request would also be reflected in this field.

17.3.78 Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**mod-PHY Power Gating Disable Fuse (mPHYPGD):** 0: mod-PHY power gating is enabled. 1: mod-PHY power gating is disabled. Note: Prior to fuse pull, the default of this bit is specified in the 'Reset' column of this field. The default value will reflect the fuse value once fuse pull is done.
30:0	0h RO	**Reserved (RSVD):** Reserved

17.3.79 Thermal and Power Throttling (TNPT)—Offset 418h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 930h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Throttle Period (TP):** Throttle Period (TP): If any of the TNPT.DRXLTE or TNPT.DTXLTE bit is '1, this field defines the duration in milliseconds that defines the Throttling Window. When TNPT.TTG is set to 0, the effective Throttling Period is: 00h: 1 ms 01h: 2 ms : : FFh: 256 ms Note: The Throttle Period will have an uncertainty of +/-1 ms. When TNPT.TTG is set to 1, the effective Throttling Period is: 00h: 100 us 01h: 200 us : : FFh: 25.6 ms Note: The Throttle Period will have an uncertainty of +/-100 us. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling. Note: If TNPT.TT is programmed to a value bigger than TNPT.TP, the hardware behavior is undefined.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RW	**Throttle Time (TT):** Throttle Time (TT): If any of the TNPT.DRXLTE or TNPT.DTXLTE bit is '1, this field defines the period of the Throttling Zone within the Throttling Window specified by TNPT.TP. The value specified in this field will be multiplied by the respective multiplier in TNPT.TSLxM fields depending on the throttling severity indication received together with the Throttling State change indication. When TNPT.TTG is set to 0, the effective Throttle Time is: 00h: 1 ms 01h: 2 ms : 3Fh: 64 ms Others: Alias to 3Fh. Note: The Throttle Period will have an uncertainty of +/-1 ms. When TNPT.TTG is set to 1, the effective Throttle Time is: 00h: 100 us 01h: 200 us : 3Fh: 6.4 ms Note: The Throttle Period will have an uncertainty of +/-100 us. Note: If the reserved encoding is programmed to this field, hardware will behave the same as if the field is programmed to 3Fh. Note: Since the design is using a 1 ms tick for this timer, the Throttle Time will have an uncertainty of +/-1 ms. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling. Note: If TNPT.TT is programmed to a value bigger than TNPT.TP, the hardware behavior is undefined.
15:12	0h RO	**Reserved (RSVD):** Reserved
11:10	2h RW	**Throttling Severity Level 3 Multiplier (TSL3M):** Throttling Severity Level 3 Multiplier (TSL3M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: Always throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.

Bit Range	Default & Access	Field Name (ID): Description
9:8	1h RW	**Throttling Severity Level 2 Multiplier (TSL2M):** Throttling Severity Level 2 Multiplier (TSL2M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: Always throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.
7:6	0h RW	**Throttling Severity Level 1 Multiplier (TSL1M):** Throttling Severity Level 1 Multiplier (TSL1M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: No throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the link throttling
5:4	3h RW	**Throttling Severity Level 0 Multiplier (TSL0M):** Throttling Severity Level 0 Multiplier (TSL0M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: No throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.
3	0h RO	**Reserved (RSVD_1):** Reserved
2	0h RW	**Throttling Timer Granuality (TTG):** Throttling Timer Granuality (TTG): This register determines the granuality of the Thermal Throttling timers. This provides a smaller granuality

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Dynamic RX Link Throttling Enable (DRXLTE):** Dynamic RX Link Throttling Enable (DRXLTE): '0b: Dynamic Link RX Throttling mechanism is disabled. '1b: Dynamic Link RX Throttling mechanism is enabled. PCIe Root Port will induce the link to enter RXL0s. The duty cycle of the throttling window is configurable based on the throttling severity. Note: This field can only be set if the remote component supports TXL0s.
0	0h RW	**Dynamic TX Link Throttling Enable (DTXLTE):** Dynamic TX Link Throttling Enable (DTXLTE): '0b: Dynamic Link TX Throttling mechanism is disabled. '1b: Dynamic Link TX Throttling mechanism is enabled. PCIe Root Port will induce the link to enter TXL0s. The duty cycle of the throttling window is configurable based on the throttling severity. Note: This field can only be set if the remote component supports TXL0s.

17.3.80 Dynamic Lane Switch (DYNLNSW)—Offset 41Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved (RSVD):** Reserved.
0	0h RW	**Hardware Re-Do Preset to Coefficient Mapping Query After Lane Switching (HWRP2CM):** Hardware Re-Do Preset to Coefficient Mapping Query After Lane Switching (HWRP2CM): When this bit is set, the PCIe-SIP Controller would query the Preset to Coefficient mapping through the PIPE GetLocalPresetCoefficients and LocalTxCoefficientsValid interface whenever the Lane Switch ownership has transitioned to PCIe (from another Controller). Note that if this bit is set while the HPCMQE bit is set, the PCIe-SIP Controller would only perform the query once. Unlike the HPCMQE bit, the PCIe-SIP Controller would not clear this bit after completing the query over the PIPE interface. Register Attribute: Static.

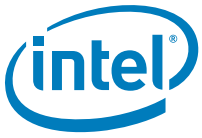
17.3.81 Power Control Enable (PCE)—Offset 428h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 9h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved (RSVD):** Reserved for Force Isolate and Reset Together. This bit is not used. The timing between isolate and reset can be controller through PGCBCTL register.
5	0h RW	**Hardware Autonomous Enable (HAE):** Hardware Autonomous Enable (HAE): If set, and the corresponding per-LTSSM state power gating enable bit is also set, then controller power gating will be done when the controller is idle and the controller power gating condition is met in that particular LTSSM state. Refer to PCIEPMECTL2 register for the per-LTSSM state power gating enable bit. If either this bit. is not set or the corresponding per-LTSSM state power gating enable bit is not set, then controller power gating will not be done in that LTSSM state. Note: For each x4 instance, only the value from Port 0 is used. NOTE: If this bit is set, then bits[lb]2:0[rb] must be '000.
4	0h RO	**Reserved (RSVD_1):** Reserved for Force Isolate and Reset Together. This bit is not used. The timing between isolate and reset can be controller through PGCBCTL register.
3	1h RW/L	**Sleep Enable (SE):** Sleep Enable (SE): If clear, Sleep indication to the retention flops will never assert. If set, Sleep indication will be assert to the retention flops as part of the hardware autonomous controller power gating entry flow.
2	0h RO	**Reserved (RSVD_2):** Reserved for D3-Hot Enable. Not supported. RTD3 is supported instead.
1	0h RO	**Reserved (RSVD_3):** Reserved for D0i3 Enable. No support for D0i3.
0	1h RW	**PMC Request Enable (PMCRE):** PMC Request Enable (PMCRE): When set, the controller will only power gate when pmc_[lt]ip[gt]_sw_pg_req_b = '0 and hardware autonomous controller power gating conditions are met. When clear, controller will power gate immediately when the hardware autonomous controller power gating conditions are met regardless of the state of pmc_[lt]ip[gt]_sw_pg_req_b.



17.3.82 PGCB Control1 (PGCBCTL1)—Offset 42Ch

This register specifies the minimum number of delay clocks the PGCB should wait between various states.
Note: For each x4 instance, only the value from Port 0 is used.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 14155555h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved for cfg_trsvd0. Not applicable since frc_clk_srst_en is tied to '0.
29:28	1h RW	**cfg_trstup2frcclks (trstup2frcclks):** cfg_trstup2frcclks(cfg_trstup2frcclks): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
27:26	1h RW	**cfg_tclksonack_cp (tclksonack_cp):** cfg_tclksonack_cp(cfg_tclksonack_cp): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
25:24	0h RO	**Reserved (RSVD_1):** Reserved for cfg_tclksoffack_srst. Not applicable since frc_clk_srst_en is tied to 0.
23:22	0h RO	**Reserved (RSVD_2):** Reserved for cfg_tclksonack_srst. Not applicable since frc_clk_srst_en is tied to 0.
21:20	1h RW	**cfg_tpokup (tpokup):** cfg_tpokup(cfg_tpokup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
19:18	1h RW	**cfg_tpokdown (tpokdown):** cfg_tpokdown(cfg_tpokdown): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
17:16	1h RW	**cfg_tlatchdis (tlatchdis):** cfg_tlatchdis(cfg_tlatchdis): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
15:14	1h RW	**cfg_tsleepinactiv (tsleepinactiv):** cfg_tsleepinactiv(cfg_tsleepinactiv): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
13:12	1h RW	**cfg_tinaccrstup (tinaccrstup):** cfg_tinaccrstup(cfg_tinaccrstup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
11:10	1h RW	**cfg_taccrstup (taccrstup):** cfg_taccrstup(cfg_taccrstup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
9:8	1h RW	**cfg_tlatchen (tlatchen):** cfg_tlatchen(cfg_tlatchen): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
7:6	1h RW	**cfg_tdeisolate (tdeisolate):** cfg_tdeisolate(cfg_tdeisolate): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
5:4	1h RW	**cfg_trstdown (trstdown):** cfg_trstdown(cfg_trstdown): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
3:2	1h RW	**cfg_tisolate (tisolate):** cfg_tisolate(cfg_tisolate): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
1:0	1h RW	**cfg_tsleepact (tsleepact):** cfg_tsleepact(cfg_tsleepact): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

17.3.83 PGCB Control2 (PGCBCTL2)—Offset 430h

This register specifies the minimum number of delay clocks the PGCB should wait between various states.
Note: For each x4 instance, only the value from Port 0 is used.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 54h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved.
7:6	1h RW	**cfg_trsvd4 (trsvd4):** cfg_trsvd4(cfg_trsvd4): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
5:4	1h RW	**cfg_trsvd3 (trsvd3):** cfg_trsvd3(cfg_trsvd3): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
3:2	1h RW	**cfg_trsvd2 (trsvd2):** cfg_trsvd2(cfg_trsvd2): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	**Reserved (RSVD_1):** Reserved for cfg_trsvd1. Not applicable since frc_clk_srst_en is tied to 0.

17.3.84 Equalization Configuration 1 (EQCFG1)—Offset 450h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 3102h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Recovery Entry Count (REC):** Recovery Entry Count (REC): This field indicates the value of the Recovery Entry Counter. This is a 1-based counter. Software must read this register multiple times. The value is valid only if the same value is read out on both of the reads.
23	0h RW	**Recovery Entry and Idle Framing Error Count Enable (REIFECE):** Recovery Entry and Idle Framing Error Count Enable (REIFECE): This bit, when set by software turns on the Recovery Entry Counter and the per-lane Idle Framing Error Counter. The counters are reset when this bit is cleared. This bit is expected to be used by the Software Preset/Coefficient Search tool but is not precluded to be used for other debug purpose. The value of the Recovery Entry Count can be read through EQCFG1.REC field. The value of the Idle Framing Error Count can be read through the Monitor Mux register.
22	0h RW	**Quiesce Guarantee (QG):** Quiesce Guarantee (QG): When set, the Quiesce Guarantee bit in the transmitted TS2 Ordered Set will be set in Recovery.RcvrCfg. When clear, the Quiesce Guarantee bit in the transmitted TS2 Ordered Set will be clear. In all other states, the Quiesce Guarantee bit is Reserved.
21	0h RW	**Link Equalization Request SMI Enable (LERSMIE):** Link Equalization Request SMI Enable (LERSMIE): When set, this bit enables the generation of an SMI to indicate that the Link Equalization Request bit has been set. This mode is meant for survivability purpose such that BIOS can be invoked to address the Re-Equalization request.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Reset EIEOS Interval Count (REIC):** Reset EIEOS Interval Count(REIC): When set, allows the root port to restrict the device from sending EIEOS until after 65536 TS1 Ordered Sets have been transmitted in Phase 3 of the Link Equalization, in the window when the receiver is evaluating the remote transmitter settings..
19	0h RW	**Link Equalization Bypass (LEB):** Link Equalization Bypass (LEB): When set, the root port will never initiate entry to Recovery.Equalization state. This includes never send EQ TS2 in Recovery.RcvrCfg that could cause the device to set start_equalization_w_preset variable. Note: This bit only affects the initial autonomous transition to Link Equalization state when equalization_done_8GT_data_rate = 0. This bit does not affect the software-direction to re-perform Link Equalization.
18	0h RW	**Link Equalization Phase 2 and 3 Bypass (LEP23B):** Link Equalization Phase 2 and 3 Bypass(LEP23B): When set, bypasses the Phase 2 and Phase 3 of Link Equalization. Once Phase 1 is completed, Root Port transitions from Phase 1 directly to Recovery.RcvrLock.
17	0h RW	**Link Equalization 3 Bypass (LEP3B):** Link Equalization 3 Bypass(LEP3B): When set, bypasses the Phase 3 of Link Equalization. Once Phase 2 is completed, Root Port transitions from Phase 2 directly to Recovery.RcvrLock.
16	0h RW	**Remote Transmit Link Equalization Preset/Coefficient Evaluation Bypass (RTLEPCEB):** Remote Transmit Link Equalization Preset/Coefficient Evaluation Bypass (RTLEPCEB): When set, this bit disables the Hardware Autonomous Preset/ Coefficient Search mechanism to search for the best Preset or Coefficient by traversing the Preset or Coefficient List and checking the receiver eye width margin for each of the settings. Instead, the Preset/Coefficient values used by the remote Transmitter will be accepted and the Link Equalization phase will be completed after one round of receiver link training, excluding margining. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Remote Transmitter Preset Coefficient Override Enable (RTPCOE):** Remote Transmitter Preset Coefficient Override Enable (RTPCOE): When set, this bit disables the hardware mechanism to search for the best Preset or Coefficient by traversing the Preset or Coefficient List and checking the receiver eye width margin for each of the settings. Instead, the Preset or Coefficient values specified by the override fields are used. If RTPCL1.PCM = 1, the Preset Override values for each lanes is derived from the following register fields: Lane 0: RTPCL1.RTPRECL0PL0. Lane 1: RTPCL1.RTPOSTCL0PL1. Lane 2: RTPCL1.RTPRECL1PL2. Lane 3: RTPCL1.RTPOSTCL1PL3. If RTPCL1.PCM = 0, the Coefficient Override values for each lanes is derived from the following register fields: Lane 0: RTPCL1.RTPRECL0PL0 and RTPCL1.RTPOSTCL0PL1. Lane 1: RTPCL1.RTPRECL1PL2 and RTPCL1.RTPOSTCL1PL3. Lane 2: RTPCL1.RTPRECL2PL4 and RTPCL2.RTPOSTCL2PL5. Lane 3: RTPCL2.RTPRECL3PL6 and RTPCL2.RTPOSTCL3PL7. BIOS must ensure that the corresponding RTPCL* registers above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
14	0h RW	**Link Equalization Request SCI Enable (LERSCIE):** Link Equalization Request SCI Enable (LERSCIE): When set, this bit enables the generation of an SCI to indicate that the Link Equalization Request bit has been set. This mode is meant for survivability purpose such that SCI handler can be invoked to address the Re-Equalization request.

Bit Range	Default & Access	Field Name (ID): Description
13	1h RW/1S/V	**Hardware Preset to Coefficient Mapping Query Enable (HPCMQE):** Hardware Preset to Coefficient Mapping Query Enable(HPCMQE): When set, the controller will query the Preset to Coefficient mapping through the PIPE GetLocalPresetCoefficients and LocalTxCoefficientsValid interface whenever this bit transitions from 0 to 1. The default of this register bit is 1, indicating that the Preset to Coefficient mapping query will be done on the PIPE interface once coming out of reset. Controller will then update the Preset-Coefficient Mapping registers with the corresponding Coefficient, for each Preset. Controller will also update the LFFS Local LF and Local FS field with the local PHY LF and FS values. Hardware will clear this bit when the Preset to Coefficient mapping query over the PIPE interface is completed. If the Hardware Preset to Coefficient Mapping mechanism is never enabled, the value of the Preset to Coefficient mapping configured by BIOS through the Preset-Coefficient Mapping registers will be used instead of querying through the PIPE interface. Note: BIOS should check to ensure that this field is cleared before enabling Controller Power Gating or mod-PHY Power Gating.
12	1h RO/V	**Hardware Autonomous Equalization Done (HAED):** Hardware Autonomous Equalization Done(HAED): This bit will be cleared when Hardware Autonomous Preset/Coefficient Search starts and will be set when Hardware Autonomous Preset/Coefficient Search is done. This bit is polled by software to ensure that the Hardware Autonomous Preset/Coefficient Search is done before proceeding with the next software sequencing. Some of the Hardware Autonomous Preset/ Coefficient search algorithm may involve the hardware initiating multiple speed change to allow multiple iterations of Link Equalization to be done with different Preset/Coefficient lists. This bit will remain cleared until the iterations are done.

Bit Range	Default & Access	Field Name (ID): Description
11:8	1h RW	**Receiver Wait Time For New Equalization Value Evaluation (RWTNEVE):** Receiver Wait Time For New Equalization Value Evaluation (RWTNEVE): For Downstream Port: This field specifies the amount of time the receiver will wait after entering Phase 3 and sending the new Preset or Coefficient values through the TS1 Ordered Sets before validating the Block Alignment and eventually evaluate the incoming ordered sets (RXEqEval on the PIPE interface asserts). For Upstream Port: This field specifies the amount of time the receiver will wait after entering Phase 2 and sending the new Preset or Coefficient values through the TS1 Ordered Sets before validating the Block Alignment and eventually evaluate the incoming ordered sets (RXEqEval on the PIPE interface asserts). For both Upstream and Downstream Port, this field also specifies the amount of time the receiver will wait after entering Phase 1 before instructing the receiver to adapt to the incoming ordered sets. For Loopback Master: This field specifies the amount of time the receiver will wait after instructing the Loopback Slave to apply a specific Preset through EQ TS1. 0h: 500 ns. 1h: 1 us. 2h: 2 us. 3h: 3 us. 4h: 4 us. : : Fh:15 us.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**EQ TS2 in Recovery.ReceiverConfig Enable (EQTS2IRRC):** EQ TS2 in Recovery.ReceiverConfig Enable(EQTS2IRRC): When set, enables the transmitter to send EQ TS2 in Recovery.RcvrCfg state even when equalization_done_8GT_data_rate variable is 1b, provided that the Downstream Port advertised 8.0 GT/s data rate support in Recovery.RcvrLock, and 8.0 GT/s data rate support has been advertised in the Configuration.Complete or Recovery.RcvrCfg substates by the Upstream Port since exiting the Detect state, and eight consecutive TS1 or TS2 Ordered Sets were received on any configured Lane prior to entry to this substate with speed_change bit set to 1b. When clear, the transmitter can only send EQ TS2 if equalization_done_8GT_data_rate variable is 0b and the Downstream Port advertised 8.0 GT/s data rate support in Recovery.RcvrLock, and 8.0 GT/s data rate support has been advertised in the Configuration.Complete or Recovery.RcvrCfg substates by the Upstream Port since exiting the Detect state, and eight consecutive TS1 or TS2 Ordered Sets were received on any configured Lane prior to entry to this substate with speed_change bit set to 1b. When this bit is used, hardware must ensure that the start_equalization_w_preset variable are in the correct state to ensure that the components on both sides of the link are never out of sync.
6:4	0h RO	**Reserved (RSVD):** Reserved
3	0h RW	**Link EQ Phase 1 Transmit Coefficient Settling Policy (LEQP1TCSP):** Link EQ Phase 1 Transmit Coefficient Settling Policy(LEQP1TCSP): When operating in GEN3 data rate and there is a software/hardware request to re-perform Link Equalization through the Recovery.RcvrLock to Recovery.Equalization arc, PCIe spec requires that the downstream port transmitter switch to the setting specified by the Downstream Port Lane X Transmitter Preset registers in Phase 1. This switching is happening while the downstream port is still actively transmitting TS1 and the upstream port is only required to sample 2 TS1 to determine the next sub-state to transition to. Since the new coefficient setting can take up to 256 ns to settle, the 2 TS1 sampled by the upstream port may be incorrect causing the two LTSSM to be out of sync. When this bit is set, the RP will continue to send EIEOS until the local transmitter setting has settled (specified by PHYCTL2.TXCFGCHGWAIT) before sending TS1 as required in Recovery.Equalization Phase 1. When this bit is clear, the RP will send TS1 with EC = 01 in Recovery.Equalization Phase 1 even though the transmitter setting is still settling.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Multi-Fragment Linear and Nine-Tile List Enable (MFLNTL):** Multi-Fragment Linear and Nine-Tile List Enable(MFLNTL): When set in Hardware Autonomous Linear Preset/Coefficient Search mode, the full Preset/Coefficient List will be traversed in multiple fragments, where each fragments is done in separate entry to Recovery. This is used in the case where a longer dwelling time is required for a particular Preset/Coefficient (configured through EQCFG2.PCET). Subsequent Preset/Coefficient entries within the list that could not be covered within that Recovery session will be covered in subsequent re-entries into Recovery. When set in Hardware Autonomous Nine-Tiles Search mode, the 9-tiles list that could not be covered within that Recovery session will be covered in subsequent re-entries into Recovery.
1	1h RW	**Transmitter Use Preset Policy (TUPP):** Transmitter Use Preset Policy(TUPP): This field applies to the Link Equalization Phase where the local transmitter setting is being adjusted. When set, the transmitted TS1 Use Preset bit will be set if the remote device requests the local transmitter to apply specific Preset(instead of Coefficient). When clear, the Use Preset bit will not be set in this case. Note: This bit must be set before changing speed to GEN3 data rate.
0	0h RW	**Receiver Use Preset Policy (RUPP):** Receiver Use Preset Policy(RUPP): This field applies to the Link Equalization Phase where the remote transmitter setting is being adjusted. When set, the received TS1 Use Preset bit will be checked. When clear, the Use Preset bit in the received TS1 will be ignored. Note: This bit must be set before changing speed to GEN3 data rate.

17.3.85 Remote Transmitter Preset Coefficient List 1 (RTPCL1)—Offset 454h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Preset/Coefficient Mode (PCM):** Preset/Coefficient Mode (PCM): This bit defines whether the Preset List or Coefficient List should be sent to the remote TX to adjust the remote TX setting. For Downstream Port, this is used in Phase 3 of the Link Equalization. For Upstream Port, this is used in Phase 2 of the Link Equalization. The list of coefficient or preset is configurable through the Remote Transmitter Preset Coefficient List [lb]1:4[rb] registers. When this bit is set, Coefficient Mode is enabled and the Remote Transmitter Preset Coefficient List [lb]1:4[rb] registers contain the Coefficient List. When this bit is clear, Preset Mode is enabled and the Remote Transmitter Preset Coefficient List [lb]1:3[rb] registers contain the Preset List.
30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 2/Preset List 4 (RTPRECL2PL4):** Remote Transmitter Pre-Cursor Coefficient List 2/Preset List 4 (RTPRECL2PL4): For Downstream Port: This field defines the pre-cursor coefficient List 2 or Preset List 4 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 2 or Preset List 4 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Remote Transmitter Post-Cursor Coefficient List 1/Preset List 3 (RTPOSTCL1PL3):** Remote Transmitter Post-Cursor Coefficient List 1/Preset List 3 (RTPOSTCL1PL3): For Downstream Port: This field defines the post-cursor coefficient List 1 or Preset List 3 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 1 or Preset List 3 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
17:12	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 1/Preset List 2 (RTPRECL1PL2):** Remote Transmitter Pre-Cursor Coefficient List 1/Preset List 2 (RTPRECL1PL2): For Downstream Port: This field defines the pre-cursor coefficient List 1 or Preset List 2 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 1 or Preset List 2 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Remote Transmitter Post-Cursor Coefficient List 0/Preset List 1 (RTPOSTCL0PL1):** Remote Transmitter Post-Cursor Coefficient List 0/Preset List 1 (RTPOSTCL0PL1): For Downstream Port: This field defines the post-cursor coefficient List 0 or Preset List 1 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 0 or Preset List 1 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
5:0	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 0/Preset List 0 (RTPRECL0PL0):** Remote Transmitter Pre-Cursor Coefficient List 0/Preset List 0 (RTPRECL0PL0): For Downstream Port: This field defines the pre-cursor coefficient List 0 or Preset List 0 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 0 or Preset List 0 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.3.86 Remote Transmitter Preset Coefficient List 2 (RTPCL2)—Offset 458h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Remote Transmitter Post-Cursor Coefficient List 4/Preset List 9 (RTPOSTCL4PL9):** Remote Transmitter Post-Cursor Coefficient List 4/Preset List 9(RTPOSTCL4PL9): For Downstream Port: This field defines the post-cursor coefficient List 4 or Preset List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 4 or Preset List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 4/Preset List 8 (RTPRECL4PL8):** Remote Transmitter Pre-Cursor Coefficient List 4/Preset List 8 (RTPRECL4PL8): For Downstream Port: This field defines the pre-cursor coefficient List 4 or Preset List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 4 or Preset List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Post-Cursor Coefficient List 3/Preset List 7 (RTPOSTCL3PL7):** Remote Transmitter Post-Cursor Coefficient List 3/Preset List 7 (RTPOSTCL3PL7): For Downstream Port: This field defines the post-cursor coefficient List 3 or Preset List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 3 or Preset List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 3/Preset List 6 (RTPRECL3PL6):** Remote Transmitter Pre-Cursor Coefficient List 3/Preset List 6 (RTPRECL3PL6): For Downstream Port: This field defines the pre-cursor coefficient List 3 or Preset List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 3 or Preset List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Post-Cursor Coefficient List 2/Preset List 5 (RTPOSTCL2PL5):** Remote Transmitter Post-Cursor Coefficient List 2/Preset List 5 (RTPOSTCL2PL5): For Downstream Port: This field defines the post-cursor coefficient List 2 or Preset List 5 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 2 or Preset List 5 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.3.87 Remote Transmitter Preset Coefficient List 3 (RTPCL3)—Offset 45Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 7 (RTPRECL7):** Remote Transmitter Pre-Cursor Coefficient List 7 (RTPRECL7): For Downstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Post-Cursor Coefficient List 6 (RTPOSTCL6):** Remote Transmitter Post-Cursor Coefficient List 6 (RTPOSTCL6): For Downstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 6 (RTPRECL6):** Remote Transmitter Pre-Cursor Coefficient List 6 (RTPRECL6): For Downstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Post-Cursor Coefficient List 5 (RTPOSTCL5):** Remote Transmitter Post-Cursor Coefficient List 5 (RTPOSTCL5): For Downstream Port: This field defines the pre-cursor coefficient List 5 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 5 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 5/Preset List 10 (RTPRECL5PL10):** Remote Transmitter Pre-Cursor Coefficient List 5/Preset List 10 (RTPRECL5PL10): For Downstream Port: This field defines the pre-cursor coefficient List 5 or Preset List 10 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 5 or Preset List 10 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.3.88 Remote Transmitter Preset Coefficient List 4 (RTPCL4)—Offset 460h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Remote Transmitter Post-Cursor Coefficient List 9 (RTPOSTCL9):** Remote Transmitter Post-Cursor Coefficient List 9 (RTPOSTCL9): For Downstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 9 (RTPRECL9):** Remote Transmitter Pre-Cursor Coefficient List 9 (RTPRECL9): For Downstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Post-Cursor Coefficient List 8 (RTPOSTCL8):** Remote Transmitter Post-Cursor Coefficient List 8 (RTPOSTCL8): For Downstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 8 (RTPRECL8):** Remote Transmitter Pre-Cursor Coefficient List 8 (RTPRECL8): For Downstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Post-Cursor Coefficient List 7 (RTPOSTCL7):** Remote Transmitter Post-Cursor Coefficient List 7 (RTPOSTCL7): For Downstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.3.89 Figure Of Merit Status (FOMS)—Offset 464h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved
30:29	0h RW	**Index (I):** Index (I): The FOMV field will reflect the Figure of Merit Scoreboard value for the index specified by this field. List N below refers to the Figure of Merit values captured in the scoreboard corresponding to the Preset or Coefficient List N. 00b: Index 0 =[gt] {List 2, List 1, List 0}. 01b: Index 1 =[gt] {List 5, List 4, List 3}. 10b: Index 2 =[gt] {List 8, List 7, List 6}. 11b: Index 3 =[gt] {Rsvd, List 10, List 9}.

Bit Range	Default & Access	Field Name (ID): Description
28:24	0h RW	**Lane Number (LN):** Lane Number (LN): The FOMV field will reflect the Figure of Merit Scoreboard value for the lane specified by this field. 00000b: Lane 0. 00001b: Lane 1. 00010b: Lane 2. 00011b: Lane 3. Others: Reserved.
23:0	0h RO/V	**Figure of Merit Scoreboard Value (FOMSV):** Figure of Merit Scoreboard Value (FOMSV): This field will reflect the Figure of Merit Scoreboard entries referenced by the Lane Number and Index field in this register. For example, when Index == 00b, this field will reflect the Figure of Merit values for Lane specified in Lane Number field and the encoding of this field is as shown below: 23:16: Figure of Merit for Preset/Coefficient List 2. 15:8 : Figure of Merit for Preset/Coefficient List 1. 7:0 : Figure of Merit for Preset/Coefficient List 0. If the Receiver Eye Width margining completes with error, the value of Figure of Merit should reflect 0x00.

17.3.90 Hardware Autonomous Equalization Control (HAEQ)—Offset 468h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: A0080E00h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Ah RW	**Hardware Autonomous Preset/Coefficient Count Per-Iteration (HAPCCPI):** Hardware Autonomous Preset/Coefficient Count Per-Iteration(HAPCCPI): This field defines the number of Preset/Coefficient to be traversed for every iteration of Recovery Equalization. For the Linear Mode, EQCFG2.HAPCSB specifies the total number of Presets/Coefficients to be checked in total while this field specifies the number of Presets/Coefficients to be checked per-iteration of Recovery Equalization. Hardware will enter Recovery Equalization and check the number of Presets/Coefficients specified by this field. Once that is done, hardware will exit Recovery Equalization and trigger another entry to Recovery Equalization to check another set of Presets/Coefficients. This goes on until the total number of Presets/Coefficients are checked. For Nine-Tiles Mode, EQCFG2.NTIC specifies the number of 9-tiles iterations, which indirectly specifies the total number of Presets/ Coefficients to be checked in total. Similar to Linear Mode, this field specifies the number of Presets/Coefficients to be checked per-iteration of Recovery Equalization. 0h: 1 Preset/Coefficient per-iteration. 1h: 2 Preset/Coefficient per-iteration. 2h: 3 Preset/Coefficient per-iteration. ... 9h: 10 Preset/Coefficient per-iteration. Ah: 11 Preset/Coefficient per-iteration. Others: Reserved.
27:20	0h RW	**FOM Error Mask (FOMEM):** FOM Error Mask(FOMEM): The FOM error counter will be masked(thus ignoring the FOM error) for all the FOM values prior to the FOM value specified in this field. If this field is programmed to 00h, this mechanism is disabled. This bit must be configured before training to GEN3 data rate.

Bit Range	Default & Access	Field Name (ID): Description
19	1h RW	**MAC FOM Control (MACFOMC):** MAC FOM Control(MACFOMC): When set, MAC controls the advancement of the FOM values completely while in the Link Equalization mode. For downstream port, this is done in Phase 3 and for upstream port, this is done in Phase 2 of the Link Equalization. The dwelling time for each of the FOM values are programmed through the remaining fields of this register. When enabled, the hardware will start in Speeding Mode, where it will instruct the PHY to increment the FOM value after the Speeding Latency specified by HAEQ.SL field. Once the FOM value matches HAEQ.SFOMFM, the hardware switches from Speeding Mode to Dwelling Mode. In Dwelling mode, the MAC will instruct PHY to increment the FOM value after the Dwelling Latency specified by HAEQ.DL field. This is done until the link equalization phase is completed. When cleared, PHY controls the advancement of the FOM values completely, during the Link Equalization mode. This bit must be configured before training to GEN3 data rate.
18:16	0h RW	**Speeding Latency (SL):** Speeding Latency(SL): Specifies the residency time for a particular FOM value in Speeding Mode. 000b: 192 ns. 001b: 256 ns. 010b: 512 ns. 011b: 1 us. 100b: 2 us. 101b: 4 us. 110b: 8 us. 111b: 16 us. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.
15:8	Eh RW	**Dwelling Latency (DL):** Dwelling Latency(DL): Specifies the residency time for a particular FOM value in Dwelling Mode. 00h: 2 us. 01h: 4 us. 02h: 6 us. ... FFh: 512 us. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Starting FOM For Margining (SFOMFM):** Starting FOM For Margining(SFOMFM): Define the FOM where MAC switches from Speeding Mode to Dwelling Mode after hitting the programmed FOM value in Hardware Autonomous Preset/Coefficient mode. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.

17.3.91 Local Transmitter Coefficient Override 1 (LTCO1)—Offset 470h

Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane bits are not used.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD):** Reserved
25	0h RW	**Lane 1 Transmitter Coefficient Override Enable (L1TCOE):** Lane 1 Transmitter Coefficient Override Enable (L1TCOE): When set, the transmitter coefficient override values LTPCO1.L1TPRECO and LTPCO1.L1TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO1.L1TPRECO and LTPCO1.L1TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Lane 0 Transmitter Coefficient Override Enable (L0TCOE):** Lane 0 Transmitter Coefficient Override Enable (L0TCOE): When set, the transmitter coefficient override values LTPCO1.L0TPRECO and LTPCO1.L0TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO1.L0TPRECO and LTPCO1.L0TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
23:18	0h RW	**Lane 1 Transmitter Post-Cursor Coefficient Override (L1TPOSTCO):** Lane 1 Transmitter Post-Cursor Coefficient Override (L1TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L1TCOE = 1.
17:12	0h RW	**Lane 1 Transmitter Pre-Cursor Coefficient Override (L1TPRECO):** Lane 1 Transmitter Pre-Cursor Coefficient Override (L1TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L1TCOE = 1.
11:6	0h RW	**Lane 0 Transmitter Post-Cursor Coefficient Override (L0TPOSTCO):** Lane 0 Transmitter Post-Cursor Coefficient Override (L0TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L0TCOE = 1.
5:0	0h RW	**Lane 0 Transmitter Pre-Cursor Coefficient Override (L0TPRECO):** Lane 0 Transmitter Pre-Cursor Coefficient Override (L0TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L0TCOE = 1.

17.3.92 Local Transmitter Coefficient Override 2 (LTCO2)—Offset 474h

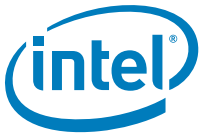
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane bits are not used.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD):** Reserved
25	0h RW	**Lane 3 Transmitter Coefficient Override Enable (L3TCOE):** Lane 3 Transmitter Coefficient Override Enable (L3TCOE): When set, the transmitter coefficient override values LTPCO2.L3TPRECO and LTPCO2.L3TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO2.L3TPRECO and LTPCO2.L3TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
24	0h RW	**Lane 2 Transmitter Coefficient Override Enable (L2TCOE):** Lane 2 Transmitter Coefficient Override Enable (L2TCOE): When set, the transmitter coefficient override values LTPCO2.L2TPRECO and LTPCO2.L2TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO2.L2TPRECO and LTPCO2.L2TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.



Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Lane 3 Transmitter Post-Cursor Coefficient Override (L3TPOSTCO):** Lane 3 Transmitter Post-Cursor Coefficient Override (L3TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L3TCOE = 1.
17:12	0h RW	**Lane 3 Transmitter Pre-Cursor Coefficient Override (L3TPRECO):** Lane 3 Transmitter Pre-Cursor Coefficient Override (L3TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L3TCOE = 1
11:6	0h RW	**Lane 2 Transmitter Post-Cursor Coefficient Override (L2TPOSTCO):** Lane 2 Transmitter Post-Cursor Coefficient Override (L2TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L2TCOE = 1.
5:0	0h RW	**Lane 2 Transmitter Pre-Cursor Coefficient Override (L2TPRECO):** Lane 2 Transmitter Pre-Cursor Coefficient Override (L2TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L2TCOE = 1.

17.3.93 GEN3 L0s Control (G3L0SCTL)—Offset 478h

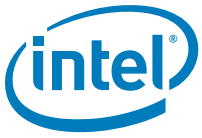
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: C00281Eh

Bit Range	Default & Access	Field Name (ID): Description
31:24	Ch RW	**Gen3 Active State L0s Preparation Latency (G3ASL0SPL):** Gen3 Active State L0s Preparation Latency (G3ASL0SPL) Determines how long the Link layer has to indicate IDLE before the link initialization and control logic enters L0s 00: 0 clocks (enter immediately) 01: 1 clock ... FF: 255 clocks The value of this register is only used if the Gen3 L0s Entry Idle Control register is set to [quote]11[/quote] and operating in Gen3 mode.
23:22	0h RW	**Gen3 L0s Entry Idle Control (G3L0SIC):** Gen3 L0s Entry Idle Control (G3L0SIC): 00 : Allow entry into L0s after the link has been idle for a period of time equal to of the received N_FTS total entry time (1/4 * N_FTS * 16) 01 : Allow entry into L0s after the link has been idle for for a period of time equal to of the received N_FTS total entry time (1/2 * N_FTS * 16) 10 : Allow entry after the link has been idle for for a period of time equal to the received N_FTS total entry time (N_FTS * 16) 11: Allow entry into L0s after the link has been idle for a period specified in the Gen3 Active State L0s Preparation Latency register. This register is only applied when operating in Gen3 mode.
21:16	0h RO	**Reserved (RSVD):** Reserved
15:8	28h RW	**Gen3 Unique Clock N_FTS (G3UCNFTS):** Gen3 Unique Clock N_FTS (G3UCNFTS): Number of Fast Training Sequence ordered sets required to be transmitted for a root port Receiver to exit L0s in a unique (non-common) clock configuration (LCTL.CCC=0) when operating in Gen3 mode. The N_FTS value is sent in TS1 and TS2 training sets during link training. 00: 0 FTS sets 01: 1 FTS set ... FF: 255 FTS sets Note: When operating in Mobile Express mode, the output of this field is not used to determine the number of FTS to be sent on TXL0s exit. Mobile Express does not support Fast Training Sequence. Instead, SYNC is used to achieve bit lock. However, the output of this field is still used in L0s Entry Idle Control registers to determine the L0s Entry Idle latency.



Bit Range	Default & Access	Field Name (ID): Description
7:0	1Eh RW	**Gen3 Common Clock N_FTS (G3CCNFTS):** Gen3 Common Clock N_FTS (G3CCNFTS): Number of Fast Training Sequence ordered sets required to be transmitted for a root port Receiver to exit L0s in a common clock configuration (LCTL.CCC=1) when operating in Gen3 mode. The N_FTS value is sent in TS1 and TS2 training sets during link training. 00: 0 FTS sets 01: 1 FTS set ... FF: 255 FTS sets Note: When operating in Mobile Express mode, the output of this field is not used to determine the number of FTS to be sent on TXL0s exit. Mobile Express does not support Fast Training Sequence. Instead, SYNC is used to achieve bit lock. However, the output of this field is still used in L0s Entry Idle Control registers to determine the L0s Entry Idle latency.

17.3.94 Equalization Configuration 2 (EQCFG2)—Offset 47Ch

Size:32 bits
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: A001h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Nine-Tiles Iteration Count (NTIC):** Nine-Tiles Iteration Count(NTIC): This field specifies the number of iterations to perform the 9-tiles search. Each iteration involves evaluating the neighboring 9-tiles for the best Preset/Coefficient margin and then use the Preset/Coefficient as the centerpoint to identify and evaluate the next 9-tiles. 00h: 1 iteration. 01h: 2 iterations. 02h: 3 iterations. ... FFh: 256 iterations.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**Equalization Margining Disable (EMD):** Equalization Margining Disable(EMD):When set, the Root Port will not request the PHY to perform Receiver Margining by asserting RxEqEval on each Preset/ Coefficient list traversed. This allows the receiver to still measure the Bit Error Count without margining. When cleared, the Root Port will request the PHY to perform Receiver Margining by asserting RxEqEval. This field is only valid when operating in Hardware Autonomous Preset/Coefficient Search mode. The Preset/Coefficient list will still be traversed to the end.
22:20	0h RW	**Nine-Tiles Step Size (NTSS):** Nine-Tiles Step Size(NTSS): This field specifies the step size used to identify the surrounding 9-tiles to be used for margining. 000b: 1 step. 001b: 2 steps. 010b: 3 steps. 011b: 4 steps. 100b: 5 steps. 101b: 6 steps. 110b: 7 steps. 111b: 8 steps. Each of the steps is measured in terms of incrementing of decrementing the coefficient values.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW	**Preset/Coefficient Evaluation Timeout (PCET):** Preset/ Coefficient Evaluation Timeout(PCET): This field specifies the evaluation timeout for a single Preset/Coefficient in the List when operating in Hardware Autonomous Preset/Coefficient Search mode. By spec, the evaluation phase must be completed before the 24 ms timeout. To support 12 Presets (11 Presets + 1 final good Preset), each Preset will have up to 2 ms for evaluation. This field allows the 2 ms timer to be programmable. This is useful if the EQCFG2.HAPCSB limits the Preset/Coefficient List to smaller than 12 such that each Preset/Coefficient could be evaluated for a time longer than 2 ms. 0h: 2 ms. 1h: 2.5 ms. 2h: 3 ms. 3h: 3.5 ms. 4h: 4 ms. 5h: 4.5 ms. 6h: 5 ms. 7h: 6 ms. 8h: 7 ms. 9h: 8 ms. Ah: 9 ms. Bh:10 ms. Ch:11 ms. Dh:21 ms. Eh:22 ms. Fh:23 ms.
15:12	Ah RW	**Hardware Autonomous Preset/Coefficient Search Bound (HAPCSB):** Hardware Autonomous Preset/Coefficient Search Bound(HAPCSB): This field defines the number of Preset/ Coefficient List to be traversed, out of 11 for Presets or out of 10 for Coefficients. The Preset/Coefficient list will be traversed from List 0 to the value specified by this field in incremental order. This field allows equalization to be done with smaller set of Preset/ Coefficient list and each of the Preset/Coefficient list could be run for a longer time. 0h: Preset/Coefficient List 0 only. 1h: Preset/Coefficient List 0 - 1. 2h: Preset/Coefficient List 0 - 2. : : 9h: Preset/Coefficient List 0 - 9. Ah: Preset List 0 - 10/Coefficient List 0-9. Others: Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Nine-Tiles Equalization Mechanism Enable (NTEME):** Nine-Tiles Equalization Mechanism Enable(NTEME): When set, the Nine-Tiles Equalization Mechanism is enabled when running in Hardware Autonomous Preset/Coefficient Search Mode.
10	0h RW	**Mid-Point Equalization Mechanism Enable (MPEME):** Mid-Point Equalization Mechanism Enable(MPEME): When set, the Mid-Point Equalization Mechanism is enabled when running in Hardware Autonomous Preset/Coefficient Search Mode.
9:8	0h RW	**Receiver Eye Width Margin Error Threshold Multiplier (REWMETM):** Receiver Eye Width Margin Error Threshold Multiplier (REWMETM): This field specifies the multiplier to be used with REWMET field. 00b: Multiply REWMET by 1 (effectively no multiplier). 01b: Multiply REWMET by 10. 10b: Multiply REWMET by 100. 11b: Multiply REWMET by 1000.
7:0	1h RW	**Receiver Eye Width Margin Error Threshold (REWMET):** Receiver Eye Width Margin Error Threshold (REWMET): This field specifies the count threshold which upon exceeded, will cause controller to terminate the current iteration of Receiver Eye Width Margining and move on to the next preset or coefficient in the list. The value specified in this field will need to be multiplied with the multiplier specified in REWMETM field to get the final threshold values. 00h: Terminate on 1 x REWMETM errors. 01h: Terminate on 2 x REWMETM errors. 02h: Terminate on 4 x REWMETM errors. 03h: Terminate on 6 x REWMETM errors. : : FEh: Terminate on 508 x REWMETM errors. FFh: Never terminate. Rely on PHY to terminate the margining.

17.3.95 Monitor Mux (MM)—Offset 480h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO/V	**Monitor Signal State (MSST):** Monitor Signal State(MSST): The internal signal groupings selected by MM.MSS field is reflected in this field. The intention of this monitor signal is provide software a capability to monitor some of the GEN3 related parameters accumulated by the controller through the Link Equalization that are too costly to be mapped to dedicated registers. Implementation MUST NEVER expose any security related information through this Monitor Mux.
7:0	0h RW	**Monitor Signal Select (MSS):** Monitor Signal Select(MSS): This field is essentially the mux select for the Monitor Signal mux. Setting this field allows different monitor signals to be muxed out and readable by software through the MM.MSST field.

17.3.96 Lane0 P0 and P1 Preset-Coefficient Mapping (L0P0P1PCM)—Offset 500h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.97 Lane0 P1, P2 and P3 Preset-Coefficient Mapping (L0P1P2P3PCM)—Offset 504h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.98 Lane0 P3 and P4 Preset-Coefficient Mapping (L0P3P4PCM)—Offset 508h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

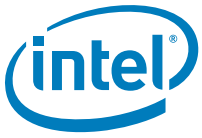
17.3.99 Lane0 P5 and P6 Preset-Coefficient Mapping (L0P5P6PCM)—Offset 50Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.100 Lane0 P6, P7 and P8 Preset-Coefficient Mapping (L0P6P7P8PCM)—Offset 510h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

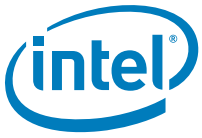
Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.101 Lane0 P8 and P9 Preset-Coefficient Mapping (L0P8P9PCM)—Offset 514h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method



Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.102 Lane0 P10 Preset-Coefficient Mapping (L0P10PCM)—Offset 518h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.103 Lane0 LF and FS (L0LFFS)—Offset 51Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.104 Lane1 P0 and P1 Preset-Coefficient Mapping (L1P0P1PCM)—Offset 520h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.105 Lane1 P1, P2 and P3 Preset-Coefficient Mapping (L1P1P2P3PCM)—Offset 524h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.106 Lane1 P3 and P4 Preset-Coefficient Mapping (L1P3P4PCM)—Offset 528h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.107 Lane1 P5 and P6 Preset-Coefficient Mapping (L1P5P6PCM)—Offset 52Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.108 Lane1 P6, P7 and P8 Preset-Coefficient Mapping (L1P6P7P8PCM)—Offset 530h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.109 Lane1 P8 and P9 Preset-Coefficient Mapping (L1P8P9PCM)—Offset 534h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.110 Lane1 P10 Preset-Coefficient Mapping (L1P10PCM)—Offset 538h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.111 Lane1 LF and FS (L1LFFS)—Offset 53Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.112 Lane2 P0 and P1 Preset-Coefficient Mapping (L2P0P1PCM)—Offset 540h

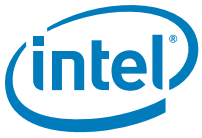
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.113 Lane2 P1, P2 and P3 Preset-Coefficient Mapping (L2P1P2P3PCM)—Offset 544h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.114 Lane2 P3 and P4 Preset-Coefficient Mapping (L2P3P4PCM)—Offset 548h

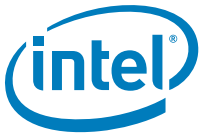
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.115 Lane2 P5 and P6 Preset-Coefficient Mapping (L2P5P6PCM)—Offset 54Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.116 Lane2 P6, P7 and P8 Preset-Coefficient Mapping (L2P6P7P8PCM)—Offset 550h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.117 Lane2 P8 and P9 Preset-Coefficient Mapping (L2P8P9PCM)—Offset 554h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.118 Lane2 P10 Preset-Coefficient Mapping (L2P10PCM)—Offset 558h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.119 Lane2 LF and FS (L2LFFS)—Offset 55Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.120 Lane3 P0 and P1 Preset-Coefficient Mapping (L3P0P1PCM)—Offset 560h

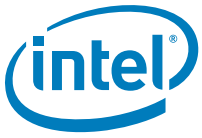
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.121 Lane3 P1, P2 and P3 Preset-Coefficient Mapping (L3P1P2P3PCM)—Offset 564h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.122 Lane3 P3 and P4 Preset-Coefficient Mapping (L3P3P4PCM)—Offset 568h

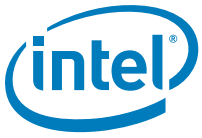
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.123 Lane3 P5 and P6 Preset-Coefficient Mapping (L3P5P6PCM)—Offset 56Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.124 Lane3 P6, P7 and P8 Preset-Coefficient Mapping (L3P6P7P8PCM)—Offset 570h

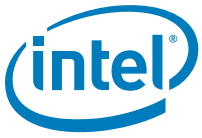
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.125 Lane3 P8 and P9 Preset-Coefficient Mapping (L3P8P9PCM)—Offset 574h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.126 Lane3 P10 Preset-Coefficient Mapping (L3P10PCM)—Offset 578h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.3.127 Lane3 LF and FS (L3LFFS)—Offset 57Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4 Registers Summary

Table 17-4. Summary of pcie_cfg Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4h	7h	Device Command; Primary Status (CMD_PSTS)—Offset 4h	100000h
8h	Bh	Revision ID;Class Code (RID_CC)—Offset 8h	60400F0h
Ch	Fh	Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch	810000h
18h	1Bh	Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h	0h
1Ch	1Fh	I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch	0h
20h	23h	Memory Base and Limit (MBL)—Offset 20h	0h
24h	27h	Prefetchable Memory Base and Limit (PMBL)—Offset 24h	10001h
28h	2Bh	Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h	0h
2Ch	2Fh	Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch	0h
34h	37h	Capabilities List Pointer (CAPP)—Offset 34h	40h
3Ch	3Fh	Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch	0h
40h	43h	Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h	428010h
44h	47h	Device Capabilities (DCAP)—Offset 44h	8001h
48h	4Bh	Device Control; Device Status (DCTL_DSTS)—Offset 48h	100000h
4Ch	4Fh	Link Capabilities (LCAP)—Offset 4Ch	710C00h
50h	53h	Link Control; Link Status (LCTL_LSTS)—Offset 50h	10000h
54h	57h	Slot Capabilities (SLCAP)—Offset 54h	40060h
58h	5Bh	Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h	0h
5Ch	5Fh	Root Control (RCTL)—Offset 5Ch	0h
60h	63h	Root Status (RSTS)—Offset 60h	0h
64h	67h	Device Capabilities 2 (DCAP2)—Offset 64h	80837h
68h	6Bh	Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h	0h
6Ch	6Fh	Link Capabilities 2 (LCAP2)—Offset 6Ch	0h
70h	73h	Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h	0h
74h	77h	Slot Capabilities 2 (SLCAP2)—Offset 74h	0h

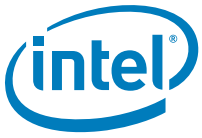


Table 17-4. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
78h	7Bh	Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h	0h
80h	83h	Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h	9005h
88h	8Bh	Message Signaled Interrupt Message Data (MD)—Offset 88h	0h
90h	93h	Subsystem Vendor Capability (SVCAP)—Offset 90h	A00Dh
94h	97h	Subsystem Vendor IDs (SVID)—Offset 94h	0h
A0h	A3h	Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h	C8030001h
A4h	A7h	PCI Power Management Control And Status (PMCS)—Offset A4h	8h
D4h	D7h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	800h
E4h	E7h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	0h
100h	103h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	0h
104h	107h	Uncorrectable Error Status (UES)—Offset 104h	0h
108h	10Bh	Uncorrectable Error Mask (UEM)—Offset 108h	0h
10Ch	10Fh	Uncorrectable Error Severity (UEV)—Offset 10Ch	60011h
110h	113h	Correctable Error Status (CES)—Offset 110h	0h
114h	117h	Correctable Error Mask (CEM)—Offset 114h	2000h
118h	11Bh	Advanced Error Capabilities and Control (AECC)—Offset 118h	0h
11Ch	11Fh	Header Log DW1 (HL_DW1)—Offset 11Ch	0h
120h	123h	Header Log DW2 (HL_DW2)—Offset 120h	0h
124h	127h	Header Log DW3 (HL_DW3)—Offset 124h	0h
128h	12Bh	Header Log DW4 (HL_DW4)—Offset 128h	0h
12Ch	12Fh	Root Error Command (REC)—Offset 12Ch	0h
134h	137h	Error Source Identification (ESID)—Offset 134h	0h
140h	143h	ACS Extended Capability Header (ACSECH)—Offset 140h	0h
144h	147h	ACS Capability Register (ACSCAPR)—Offset 144h	Fh
148h	14Bh	ACS Control Register (ACSCTLR)—Offset 148h	0h
150h	153h	PTM Extended Capability Header (PTMECH)—Offset 150h	0h
154h	157h	PTM Capability Register (PTMCAPR)—Offset 154h	400h
158h	15Bh	PTM Control Register (PTMCTLR)—Offset 158h	0h
200h	203h	L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h	0h
204h	207h	L1 Sub-States Capabilities (L1SCAP)—Offset 204h	28281Fh
208h	20Bh	L1 Sub-States Control 1 (L1SCTL1)—Offset 208h	0h
20Ch	20Fh	L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch	28h
220h	223h	Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h	0h
224h	227h	Link Control 3 (LCTL3)—Offset 224h	0h
228h	22Bh	Lane Error Status (LES)—Offset 228h	0h
22Ch	22Fh	Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch	7F7F7F7Fh

Table 17-4. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
230h	233h	Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h	7F7F7F7Fh
300h	303h	PCI Express Replay Timer Policy 1 (PCIERTP1)—Offset 300h	A64F96h
304h	307h	PCI Express Replay Timer Policy 2 (PCIERTP2)—Offset 304h	1BC00B86h
314h	317h	PCI Express Status 1 (PCIESTS1)—Offset 328h	54262A13h
328h	32Bh	PCI Express Status 1 (PCIESTS1)—Offset 328h	0h
32Ch	32Fh	PCI Express Status 2 (PCIESTS2)—Offset 32Ch	0h
330h	333h	PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h	2A000016h
334h	337h	PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h	4ABCB5BCh
390h	393h	PTM Propagation Delay (PTMPD)—Offset 390h	0h
394h	397h	PTM Lower Local Master Time (PTMLLMT)—Offset 394h	0h
398h	39Bh	PTM Upper Local Master Time (PTMULMT)—Offset 398h	0h
39Ch	39Fh	PTM Pipe Stage Delay Configuration 1 (PTMPSDC1)—Offset 39Ch	0h
3A0h	3A3h	PTM Pipe Stage Delay Configuration 2 (PTMPSDC2)—Offset 3A0h	0h
3A4h	3A7h	PTM Pipe Stage Delay Configuration 3 (PTMPSDC3)—Offset 3A4h	0h
3A8h	3ABh	PTM Pipe Stage Delay Configuration 4 (PTMPSDC4)—Offset 3A8h	0h
3ACh	3AFh	PTM Pipe Stage Delay Configuration 5 (PTMPSDC5)—Offset 3ACh	0h
3B0h	3B3h	PTM Extended Config (PTMECFG)—Offset 3B0h	0h
3B4h	3B7h	PTM Lower T2 Time Stamp (PTMLT2TSTMP)—Offset 3B4h	0h
3B8h	3BBh	PTM Upper T2 Time Stamp (PTMUT2TSTMP)—Offset 3B8h	0h
414h	417h	Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h	0h
418h	41Bh	Thermal and Power Throttling (TNPT)—Offset 418h	930h
41Ch	41Fh	Dynamic Lane Switch (DYNLNSW)—Offset 41Ch	0h
420h	423h	Power Control Enable (PCE)—Offset 428h	2AE8146h
428h	42Bh	Power Control Enable (PCE)—Offset 428h	9h
42Ch	42Fh	PGCB Control1 (PGCBCTL1)—Offset 42Ch	14155555h
430h	433h	PGCB Control2 (PGCBCTL2)—Offset 430h	54h
450h	453h	Equalization Configuration 1 (EQCFG1)—Offset 450h	3102h
454h	457h	Remote Transmitter Preset Coefficient List 1 (RTPCL1)—Offset 454h	0h
458h	45Bh	Remote Transmitter Preset Coefficient List 2 (RTPCL2)—Offset 458h	0h
45Ch	45Fh	Remote Transmitter Preset Coefficient List 3 (RTPCL3)—Offset 45Ch	0h
460h	463h	Remote Transmitter Preset Coefficient List 4 (RTPCL4)—Offset 460h	0h
464h	467h	Figure Of Merit Status (FOMS)—Offset 464h	0h
468h	46Bh	Hardware Autonomous Equalization Control (HAEQ)—Offset 468h	A0080E00h
470h	473h	Local Transmitter Coefficient Override 1 (LTCO1)—Offset 470h	0h
474h	477h	Local Transmitter Coefficient Override 2 (LTCO2)—Offset 474h	0h
478h	47Bh	GEN3 L0s Control (G3L0SCTL)—Offset 478h	C00281Eh
47Ch	47Fh	Equalization Configuration 2 (EQCFG2)—Offset 47Ch	A001h
480h	483h	Monitor Mux (MM)—Offset 480h	0h
500h	503h	Lane0 P0 and P1 Preset-Coefficient Mapping (L0P0P1PCM)—Offset 500h	0h

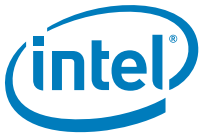


Table 17-4. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
504h	507h	Lane0 P1, P2 and P3 Preset-Coefficient Mapping (L0P1P2P3PCM)—Offset 504h	0h
508h	50Bh	Lane0 P3 and P4 Preset-Coefficient Mapping (L0P3P4PCM)—Offset 508h	0h
50Ch	50Fh	Lane0 P5 and P6 Preset-Coefficient Mapping (L0P5P6PCM)—Offset 50Ch	0h
510h	513h	Lane0 P6, P7 and P8 Preset-Coefficient Mapping (L0P6P7P8PCM)—Offset 510h	0h
514h	517h	Lane0 P8 and P9 Preset-Coefficient Mapping (L0P8P9PCM)—Offset 514h	0h
518h	51Bh	Lane0 P10 Preset-Coefficient Mapping (L0P10PCM)—Offset 518h	0h
51Ch	51Fh	Lane0 LF and FS (L0LFFS)—Offset 51Ch	0h
520h	523h	Lane1 P0 and P1 Preset-Coefficient Mapping (L1P0P1PCM)—Offset 520h	0h
524h	527h	Lane1 P1, P2 and P3 Preset-Coefficient Mapping (L1P1P2P3PCM)—Offset 524h	0h
528h	52Bh	Lane1 P3 and P4 Preset-Coefficient Mapping (L1P3P4PCM)—Offset 528h	0h
52Ch	52Fh	Lane1 P5 and P6 Preset-Coefficient Mapping (L1P5P6PCM)—Offset 52Ch	0h
530h	533h	Lane1 P6, P7 and P8 Preset-Coefficient Mapping (L1P6P7P8PCM)—Offset 530h	0h
534h	537h	Lane1 P8 and P9 Preset-Coefficient Mapping (L1P8P9PCM)—Offset 534h	0h
538h	53Bh	Lane1 P10 Preset-Coefficient Mapping (L1P10PCM)—Offset 538h	0h
53Ch	53Fh	Lane1 LF and FS (L1LFFS)—Offset 53Ch	0h
540h	543h	Lane2 P0 and P1 Preset-Coefficient Mapping (L2P0P1PCM)—Offset 540h	0h
544h	547h	Lane2 P1, P2 and P3 Preset-Coefficient Mapping (L2P1P2P3PCM)—Offset 544h	0h
548h	54Bh	Lane2 P3 and P4 Preset-Coefficient Mapping (L2P3P4PCM)—Offset 548h	0h
54Ch	54Fh	Lane2 P5 and P6 Preset-Coefficient Mapping (L2P5P6PCM)—Offset 54Ch	0h
550h	553h	Lane2 P6, P7 and P8 Preset-Coefficient Mapping (L2P6P7P8PCM)—Offset 550h	0h
554h	557h	Lane2 P8 and P9 Preset-Coefficient Mapping (L2P8P9PCM)—Offset 554h	0h
558h	55Bh	Lane2 P10 Preset-Coefficient Mapping (L2P10PCM)—Offset 558h	0h
55Ch	55Fh	Lane2 LF and FS (L2LFFS)—Offset 55Ch	0h
560h	563h	Lane3 P0 and P1 Preset-Coefficient Mapping (L3P0P1PCM)—Offset 560h	0h
564h	567h	Lane3 P1, P2 and P3 Preset-Coefficient Mapping (L3P1P2P3PCM)—Offset 564h	0h
568h	56Bh	Lane3 P3 and P4 Preset-Coefficient Mapping (L3P3P4PCM)—Offset 568h	0h
56Ch	56Fh	Lane3 P5 and P6 Preset-Coefficient Mapping (L3P5P6PCM)—Offset 56Ch	0h
570h	573h	Lane3 P6, P7 and P8 Preset-Coefficient Mapping (L3P6P7P8PCM)—Offset 570h	0h
574h	577h	Lane3 P8 and P9 Preset-Coefficient Mapping (L3P8P9PCM)—Offset 574h	0h
578h	57Bh	Lane3 P10 Preset-Coefficient Mapping (L3P10PCM)—Offset 578h	0h
57Ch	57Fh	Lane3 LF and FS (L3LFFS)—Offset 57Ch	0h

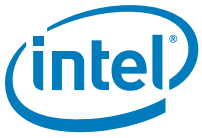
17.4.1 Device Command; Primary Status (CMD_PSTS)—Offset 4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**DPE - Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if CMD.PERE is not set.
30	0h RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
26:25	0h RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved per PCI-Express spec
24	0h RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and CMD.PERE is set.
23	0h RO	**Primary Fast Back to Back Capable (PFBC):** Reserved per PCI-Express spec.
22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Primary 66 MHz Capable (PC66):** Reserved per PCI-Express spec.
20	1h RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list.
19	0h RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID.
18:16	0h RO	**Reserved (RSVD_1):** Reserved
15:11	0h RO	**Reserved (RSVD_2):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec.
8	0h RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0h RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec.
6	0h RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** Reserved per PCI-Express spec.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec.
3	0h RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec.
2	0h RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0h RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0h RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone..

17.4.2 Revision ID;Class Code (RID_CC)—Offset 8h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 60400F0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	6h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	4h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h.
15:8	0h RO/V	**Programming Interface (PI):** The value reported in this register is a function of the Decode Control.Subtractive Decode Enable (SDE) register. SDE Value reported in this register 0: 00h 1: 01h
7:0	F0h RO/V	**Revision ID (RID):** Indicates the revision of the bridge.

17.4.3 Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 810000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved
23	1h RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device.
22:16	1h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h.
15:11	0h RO	**Latency Count (CT):** Reserved per PCI-Express spec
10:8	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec

17.4.4 Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V2	**Secondary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	0h RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.
15:8	0h RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port.
7:0	0h RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

17.4.5 I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
30	0h RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with 'Unsupported Request' status from the device.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with 'Completion Abort' status from the device.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with 'Completion Abort' status to the device.
26:25	0h RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.
23	0h RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec
20:16	0h RO	**Reserved (RSVD_1):** Reserved
15:12	0h RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing.

17.4.6 Memory Base and Limit (MBL)—Offset 20h

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is MB [gt]= AD[lb]31:20[rb] [lt]= ML.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	0h RO	**Reserved (RSVD):** Reserved
15:4	0h RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	0h RO	**Reserved (RSVD_1):** Reserved

17.4.7 Prefetchable Memory Base and Limit (PMBL)—Offset 24h

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB [gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 10001h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing.
15:4	0h RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	1h RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing.

17.4.8 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.

17.4.9 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

17.4.10 Capabilities List Pointer (CAPP)—Offset 34h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 40h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	40h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) OffsetCapability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI) 90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List OffsetCapability Next Pointer 100h Advanced Error Reporting 000h

17.4.11 Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch

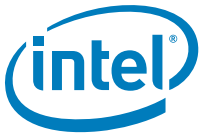
Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD):** Reserved
27	0h RW/V2	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
26	0h RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set.
25	0h RW/V2	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW/V2	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
23	0h RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec.
22	0h RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port.
21	0h RW/V2	**Master Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
20	0h RW	**VGA 16-Bit Decode (V16):** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.
19	0h RW	**VGA Enable (VE):** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h 3BBh and 3C0h 3DFh, and all aliases of bits 15:10 in any combination of 1's
18	0h RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
17	0h RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
16	0h RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG register in chipset config space: Port Bits[lb]15:12[rb] Bits[lb]11:08[rb] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP 4 0h STRPFUSECFG.P4IP 5 0h STRPFUSECFG.P5IP 6 0h STRPFUSECFG.P6IP 7 0h STRPFUSECFG.P7IP 8 0h STRPFUSECFG.P8IP The value that is programmed into STRPFUSECFG.PxIP is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above.
7:0	0h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

17.4.12 Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 428010h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved
30	0h RO	**Reserved (RSVD_1):** Reserved. This register at one time was for TCS Routing but that was later removed from the PCIe 2.0 spec
29:25	0h RO	**Interrupt Message Number (IMN):** The root port does not have multiple MSI interrupt numbers.
24	0h RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
23:20	4h RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port

Bit Range	Default & Access	Field Name (ID): Description
19:16	2h RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 specification which incorporates the Register Expansion ECN.
15:8	80h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h RO	**Capability ID (CID):** Indicates this is a PCI Express capability

17.4.13 Device Capabilities (DCAP)—Offset 44h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 8001h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD):** Reserved
28	0h RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports
27:26	0h RO	**Captured Slot Power Limit Scale (CSPS):** Not supported
25:18	0h RO	**Captured Slot Power Limit Value (CSPV):** Not supported
17:16	0h RO	**Reserved (RSVD_1):** Reserved
15	1h RO	**Role Based Error Reporting (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.
14	0h RO	**Reserved (RSVD_2):** Reserved. On previous version of the specification this was Power Indicator Present (PIP)
13	0h RO	**Reserved (RSVD_3):** Reserved. On previous version of the specification this was Attention Indicator Present (AIP)

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**Reserved (RSVD_4):** Reserved. On previous version of the specification this was Attention Button Present (ABP)
11:9	0h RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports.
8:6	0h RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port.
5	0h RO	**Extended Tag Field Supported (ETFS):** The root port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	0h RO	**Phantom Functions Supported (PFS):** No phantom functions supported
2:0	1h RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Only Max Payload Size of up to 256B is supported. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface.

17.4.14 Device Control; Device Status (DCTL_DSTS)—Offset 48h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
20	1h RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
18	0h RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp
17	0h RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completer abort, or completer timeout
16	0h RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout.
15	0h RO	**Reserved (RSVD_1):** Reserved
14:12	0h RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface.
11	0h RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.
10	0h RW/P	**Aux Power PM Enable (APME):** The OS will set this bit to '1' if the device connected has detected aux power.
9	0h RO	**Phantom Functions Enable (PFE):** Not supported
8	0h RO	**Extended Tag Field Enable (ETFE):** Not supported
7:5	0h RW	**Max Payload Size (MPS):** The root port only supports up to 256B max payload. Programming this field to any values other than 128B or 256B max payload size will result in aliasing to 128B max payload size. If the DCAP.MPS indicates 128B max payload size support, programming this field to any values other than 128B will result in aliasing to 128B max payload size. Programming this field to any values greater than DCAP.MPS will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME.
4	0h RO	**Enable Relaxed Ordering (ERO):** Not supported

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0h RW	**Fatal Error Reporting Enable (FEE):** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0h RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0h RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

17.4.15 Link Capabilities (LCAP)—Offset 4Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 710C00h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h
23	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
22	1h RW/O	**ASPM Optionality Compliance (ASPMOC):** ASPM Optionality Compliance(ASPMOC): This bit must be set to 1b for PCIe 3.0 compliant port. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests.
21	1h RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1h RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0h RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the root port does not support Surprise Down Error Reporting
18	0h RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism.
17:15	2h RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b Less than 1 us 001b 1 us to less than 2 us 010b 2 us to less than 4 us 011b 4 us to less than 8 us 100b 8 us to less than 16 us 101b 16 us to less than 32 us 110b 32 us to 64 us 111b More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency.
14:12	0h RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL

Bit Range	Default & Access	Field Name (ID): Description
11:10	3h RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 No ASPM Supported 01 L0s Supported 10 L1 Supported 11 L0s and L1 supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is '01'. Otherwise, the default of this field is '11'. If STRPFUSECFG.ASPMDIS is 1, BIOS writing '11' to this field will have the same effect as writing '01'. '01' will be reflected on this register when read and the register will turn to Read-Only once written once.
9:4	0h RO/V	**Maximum Link Width (MLW):** For the root ports, several values can be taken, based upon the value of the chipset configuration register field RPC.PC1 for ports 1-4: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RO/V	**Max Link Speeds (MLS):** Indicates the supported link speeds of the Root Port. 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5GT/s Link speeds supported This register reports a value of 0001b if the Root Port Gen2 Disable Fuse is set or the MPC.PCIEGEN2DIS bit is set, else this register reports a value of 0010b. Max Link Speeds (MLS): This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. This register reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through Fuse or MPC.PCIESD register. This register reports a value of 0010b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through Fuse or MPC.PCIESD register.

17.4.16 Link Control; Link Status (LCTL_LSTS)—Offset 50h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
29	0h RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.
28	0h RO/V	**Slot Clock Configuration (SCC):** In normal mode, root port uses the same reference clock as on the platform and does not generate its own clock. Note: The default of this register bit is dependent on the 'PCIe Non-Common Clock With SSC Mode Enable Strap'. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'.
27	0h RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
26	0h RO	**Reserved (RSVD):** Reserved. Previously this was defined as Link Training Error (LTE) but support for this bit was removed from subsequent versions of the PCI Express specification.
25:20	0h RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained.

Bit Range	Default & Access	Field Name (ID): Description
19:16	1h RO/V	**Current Link Speed (CLS):** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link This field indicates the negotiated Link speed of the given link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. The value of this field is undefined if the link is not up.
15:12	0h RO	**Reserved (RSVD_1):** Reserved
11	0h RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.
10	0h RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.
9	0h RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. Note: When operating as PCI Express, this bit defines the value of the Link Upconfigure Capability in TS2 Ordered Sets.
8	0h RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on Root Ports.
7	0h RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. Note: This functionality is not applicable for Mobile Express.
6	0h RW	**Common Clock Configuration (CCC):** When set, indicates that the root port and device are operating with a distributed common reference clock.

Bit Range	Default & Access	Field Name (ID): Description
5	0h WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0h RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state.
3	0h RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0h RO	**Reserved (RSVD_2):** Reserved
1:0	0h RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see '00' as an output from this register. BIOS reading this register should always return the correct value.

17.4.17 Slot Capabilities (SLCAP)—Offset 54h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 40060h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/O	**Physical Slot Number (PSN__31_24):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
23:19	0h RW/O	**Physical Slot Number (PSN__23_19):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.

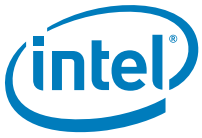
Bit Range	Default & Access	Field Name (ID): Description
18	1h RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0h RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented.
16:15	0h RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:8	0h RW/O	**Slot Power Limit Value (SLV__14_8):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
7	0h RW/O	**Slot Power Limit Value (SLV__7_7):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1h RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported.
5	1h RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification.
4	0h RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot.
3	0h RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot.
2	0h RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present
1	0h RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot
0	0h RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot.

17.4.18 Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved (RSVD):** Reserved
24	0h RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
23	0h RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock.
22	0h RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'.
21	0h RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented.
20	0h RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller..
19	0h RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the SLSTS.PDS bit changes state.
18	0h RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented.
17	0h RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented.
16	0h RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button
15:13	0h RO	**Reserved (RSVD_1):** Reserved
12	0h RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed
11	0h RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock.
10	0h RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug.
9:8	0h RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller..
7:6	0h RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller..
5	0h RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0h RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller..

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state.
2	0h RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller..
1	0h RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller...
0	0h RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller..

17.4.19 Root Control (RCTL)—Offset 5Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:4	0h RO	**Reserved (RSVD_1):** Reserved
3	0h RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set).
2	0h RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0h RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0h RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

17.4.20 Root Status (RSTS)—Offset 60h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17	0h RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. Root ports have a one deep PME pending queue.
16	0h RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0h RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

17.4.21 Device Capabilities 2 (DCAP2)—Offset 64h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 80837h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved (RSVD):** Reserved
19:18	2h RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported.
17:12	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/ disable the root port from declaring support for the LTR capability.
10:6	0h RO	**Reserved (RSVD_2):** Reserved
5	1h RO	**ARI Forwarding Supported (AFS):** ARI Forwarding Supported (AFS): Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. Note: This bit is not made RWO to simplify implementation, since there is a requirement that the ARI Forwarding Enable bit must be hardwired to 0b if ARI Forwarding Supported bit is 0b. It is low risk to keep this risk 1b.
4	1h RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	7h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C 0111b Ranges A, B [amp] C [lt]-- This is what PCH supports 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved.

17.4.22 Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15	0h RO	**Reserved (RSVD_1):** Reserved
14:13	0h RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** 00b Disable OBFF mechanism. 01b Enable OBFF mechanism using Message signaling (Variation A). 10b Enable OBFF mechanism using Message signaling (Variation B). 11b Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect.
12:11	0h RO	**Reserved (RSVD_2):** Reserved
10	0h RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:6	0h RO	**Reserved (RSVD_3):** Reserved
5	0h RW	**ARI Forwarding Enable (AFE):** ARI Forwarding Enable (AFE): When set, the Downstream Port disables its traditional Device Number field being 0b enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port.
4	0h RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The root port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 us to 100 us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either when this value was changed or when each request was issued.

17.4.23 Link Capabilities 2 (LCAP2)—Offset 6Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved (RSVD):** Reserved
22:16	0h RO	**Lower SKP OS Reception Supported Speeds Vector (LSOSRSS):** Lower SKP OS Reception Supported Speeds Vector(LSOSRSS): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
15:9	0h RO	**Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV):** Lower SKP OS Generation Supported Speeds Vector(LSOSGSSV): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
8	0h RO	**Crosslink Supported (CS):** Crosslink Supported (CS): No support for Crosslink.
7:1	0h RO/V	**Supported Link Speeds Vector (SLSV):** Supported Link Speeds Vector (SLSV): This field indicates the supported Link speed of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. Bit definitions within this field are: Bit 0: 2.5 GT/s. Bit 1: 5.0 GT/s. Bit 2: 8.0 GT/s. Bits 6:3: Reserved. This register reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through Fuse or MPC.PCIESD register. This register reports a value of 0011b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through Fuse or MPC.PCIESD register.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**Reserved (RSVD_1):** Reserved

17.4.24 Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h

Access Method

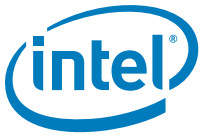
Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/1C/V/P	**Link Equalization Request (LER):** Link Equalization Request (LER): This bit is set by hardware to request the Link equalization process to be performed on the Link. Register Attribute: Dynamic.
20	0h RO/V/P	**Equalization Phase 3 Successful (EQP3S):** Equalization Phase 3 Successful (EQP3S): When set to 1, this bit indicates that Phase 3 of the Transmitter Equalization procedure has successfully completed.
19	0h RO/V/P	**Equalization Phase 2 Successful (EQP2S):** Equalization Phase 2 Successful (EQP2S): When set to 1, this bit indicates that Phase 2 of the Transmitter Equalization procedure has successfully completed.
18	0h RO/V/P	**Equalization Phase 1 Successful (EQP1S):** Equalization Phase 1 Successful (EQP1S): When set to 1, this bit indicates that Phase 1 of the Transmitter Equalization procedure has successfully completed.
17	0h RO/V/P	**Equalization Complete (EqC):** Equalization Complete (EC): When set to 1, this bit indicates that the Transmitter Equalization procedure has completed
16	0h RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/P	**Compliance Preset/De-emphasis (CD):** For 8.0 GT/s Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b -3.5 dB 0000b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. The default value of this field is 0000b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value.
11	0h RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only.
10	0h RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.

Bit Range	Default & Access	Field Name (ID): Description
9:7	0h RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0h RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5	0h RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds.



Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value.
3:0	0h RW/V/P	**Target Link Speed (TLS):** Target Link Speed (TLS): This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. If a value is written to this field that does not correspond to a supported speed, as indicated by the Supported Link Speeds Vector, the result is undefined. The default value of this field is GEN1. Note: This register field could be used by REUT software to limit the link speed to 2.5 GT/s or 5 GT/s data rate.

17.4.25 Slot Capabilities 2 (SLCAP2)—Offset 74h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved (RSVD):** Reserved

17.4.26 Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:0	0h RO	**Reserved (RSVD_1):** Reserved

17.4.27 Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 9005h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved
23	0h RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
22:20	0h RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
19:17	0h RO	**Multiple Message Capable (MMC):** Only one message is required.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	5h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

17.4.28 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction.

17.4.29 Subsystem Vendor Capability (SVCAP)—Offset 90h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: A00Dh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

17.4.30 Subsystem Vendor IDs (SVID)—Offset 94h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

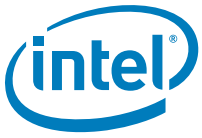
17.4.31 Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: C8030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	19h RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Microsoft operating systems to enable PME# in devices connected behind this root port.
26	0h RO	**D2_Support (D2S):** The D2 state is not supported.
25	0h RO	**D1_Support (D1S):** The D1 state is not supported.
24:22	0h RO	**Aux_Current (AC):** Reports 0mA (self-powered), as use of this controller does not add to suspect well power consumption.
21	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
20	0h RO	**Reserved (RSVD):** Reserved
19	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
18:16	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	1h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

17.4.32 PCI Power Management Control And Status (PMCS)—Offset A4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Data (DTA):** Reserved
23	0h RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification
22	0h RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification.
21:16	0h RO	**Reserved (RSVD):** Reserved
15	0h RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0h RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Microsoft operating systems to enable PME# on devices connected to this root port.
7:4	0h RO	**Reserved (RSVD_1):** Reserved
3	1h RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved (RSVD_2):** Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 D0 state 11 D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

17.4.33 Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h

Size:32 bits
The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list.
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

17.4.34 Uncorrectable Error Status (UES)—Offset 104h

This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/1C/V/P	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0h RW/1C/V/P	**Completer Abort Status (CA):** Indicates a completer abort was received

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Not supported.
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RO	**Training Error Status (TE):** Not supported.

17.4.35 Uncorrectable Error Mask (UEM)—Offset 108h

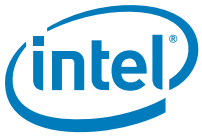
When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/P	**ACS Violation Mask (AVM):** Reserved. Access Control Services are not supported
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.



Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0h RW/P	**Completor Abort Mask (CM):** Mask for completer abort.
14	0h RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.
13	0h RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RO	**Training Error Mask (TE):** Not supported.

17.4.36 Uncorrectable Error Severity (UEV)—Offset 10Ch

This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 60011h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/P	**ACS Violation Severity (AVS):** Severity for ACS violation.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	1h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.

Bit Range	Default & Access	Field Name (ID): Description
17	1h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0h RW/P	**Completer Abort Severity (CA):** Severity for completer abort.
14	0h RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	1h RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation..

17.4.37 Correctable Error Status (CES)—Offset 110h

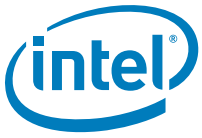
This register is only reset by a loss of core power

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved (RSVD):** Reserved
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	**Reserved (RSVD_1):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

17.4.38 Correctable Error Mask (CEM)—Offset 114h

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved (RSVD):** Reserved
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	**Reserved (RSVD_1):** Reserved
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.

Bit Range	Default & Access	Field Name (ID): Description
5:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

17.4.39 Advanced Error Capabilities and Control (AECC)—Offset 118h

This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved (RSVD):** Reserved
8	0h RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0h RO	**ECRC Check Capable (ECC):** ECRC is not supported.
6	0h RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0h RO	**ECRC Generation Capabile (EGC):** ECRC is not supported.
4:0	0h RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

17.4.40 Header Log DW1 (HL_DW1)—Offset 11Ch

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**1st dWord of TLP (DW1):** Byte0 [amp][amp] Byte1 [amp][amp] Byte2 [amp][amp] Byte3

17.4.41 Header Log DW2 (HL_DW2)—Offset 120h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**2nd dWord of TLP (DW2):** Byte4 [amp][amp] Byte5 [amp][amp] Byte6 [amp][amp] Byte7

17.4.42 Header Log DW3 (HL_DW3)—Offset 124h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**3rd dWord of TLP (DW3):** Byte8 [amp][amp] Byte9 [amp][amp] Byte10 [amp][amp] Byte11

17.4.43 Header Log DW4 (HL_DW4)—Offset 128h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**4th dWord of TLP (DW4):** Byte12 [amp][amp] Byte13 [amp][amp] Byte14 [amp][amp] Byte15

17.4.44 Root Error Command (REC)—Offset 12Ch

This register allows errors to generate interrupts.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved (RSVD):** Reserved
2	0h RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0h RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0h RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

17.4.45 Error Source Identification (ESID)—Offset 134h

Size:32 bits
Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set.
15:0	0h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set.

17.4.46 ACS Extended Capability Header (ACSECH)—Offset 140h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support ACS Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support ACS Extended Capability, BIOS should write a 000Dh to this register else it should write 0.

17.4.47 ACS Capability Register (ACSCAPR)—Offset 144h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: Fh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD_1):** Reserved for Egress Control Vector Size. This field is not applicable since ACS P2P Egress Control is not supported.
7	0h RO	**Reserved (RSVD_2):** Reserved
6	0h RO	**ACS Direct Translated P2P (T):** ACS Direct Translated P2P (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control (E):** ACS P2P Egress Control (E): ACS P2P Egress Control is not supported.
4	0h RO	**ACS Upstream Forwarding (U):** ACS Upstream Forwarding (U): ACS Upstream Forwarding is not supported.
3	1h RW/O	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Required for all Functions that support ACS P2P Request Redirect; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Completion Redirect.
2	1h RW/O	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Required for Root Ports that support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports; required for multi-function device Functions that support peer-to-peer traffic with other Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Request Redirect.
1	1h RW/O	**ACS Translation Blocking (B):** ACS Translation Blocking (B): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Translation Blocking.
0	1h RW/O	**ACS Source Validation (V):** ACS Source Validation (V): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Source Validation.

17.4.48 ACS Control Register (ACSCTLR)—Offset 148h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RSVD):** Reserved,
6	0h RO	**ACS Direct Translated P2P Enable (T):** ACS Direct Translated P2P Enable (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control Enable (E):** ACS P2P Egress Control Enable (E): ACS P2P Egress Control is not supported.
4	0h RO	**ACS Upstream Forwarding Enable (U):** ACS Upstream Forwarding Enable (U): ACS Upstream Forwarding is not supported.
3	0h RW	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Determines when the component redirects peer-to-peer Completions upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear.
2	0h RW	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Determines when the component redirects peer-to-peer memory Requests targeting another peer port upstream. I/O, Configuration, VDM Messages and Completions are never affected by ACS P2P Request Redirect.
1	0h RW	**ACS Translation Blocking (B):** ACS Translation Blocking (B): When set, the component blocks all upstream Memory Requests whose Address Translation (AT) field is not set to the default value. I/O, Configuration, Completions and Messages are never affected by ACS Translation Blocking.
0	0h RW	**ACS Source Validation (V):** ACS Source Validation (V): When set, the component validates the Bus Number from the Requester ID of upstream Requests against the secondary / subordinate Bus Numbers. I/O, Configuration and Completions are never affected by ACS Source Validation.

17.4.49 PTM Extended Capability Header (PTMECH)—Offset 150h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support PTM Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support PTM Extended Capability, BIOS should write a 001Fh to this register else it should write 0.

17.4.50 PTM Capability Register (PTMCAPR)—Offset 154h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 400h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved,
15:8	4h RW/O	**Local Clock Granularity (LCG):** Local Clock Granularity(LCG): 0000 0000b - Time Source does not implement a local clock. It simply propagates timing information obtained from further Upstream in the PTM Hierarchy when responding to PTM Request messages. 0000 0001b - 1111 1110b: Indicates the period of this Time Sources local clock in ns. 1111 1111b: Indicates the period of this Time Sources local clock is greater than 254 ns. If the PTM Root Select bit is Set, this local clock is used to provide PTM Master Time. Otherwise, the Time Source uses this local clock to locally track PTM Master Time received from further Upstream within a PTM Hierarchy.
7:3	0h RO	**Reserved (RSVD_1):** Reserved,
2	0h RW/O	**PTM Root Capable (PTMRC):** PTM Root Capable(PTMRC): Root Ports must set this bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW/O	**PTM Responder Capable (PTMRSPC):** PTM Responder Capable(PTMRSPC): Root Ports are permitted to set this bit to 1b to indicate that they implement the PTM Responder role.
0	0h RO	**PTM Requester Capable (PTMREQC):** PTM Requester Capable(PTMREQC): PTM Requester Role is not supported by Root Port.

17.4.51 PTM Control Register (PTMCTLR)—Offset 158h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:8	0h RO	**Effective Granularity (EG):** Effective Granularity(EG): Root Port does not support PTM Requester role.
7:2	0h RO	**Reserved (RSVD_1):** Reserved.
1	0h RW	**Root Select (RS):** Root Select(RS): When Set, if the PTM Enable bit is also Set, this Time Source is the PTM Root. Within each PTM Hierarchy, it is recommended that system software select only the furthest Upstream Time Source to be the PTM Root.
0	0h RW	**PTM Enable (PTME):** PTM Enable(PTME): When Set, this Function is permitted to participate in the PTM mechanism according to its selected role. Software must not have the PTM Enable bit Set in the PTM Control register on a Function associated with an Upstream Port unless the associated Downstream Port on the Link already has the PTM Enable bit Set in its associated PTM Control register. Register Attribute: Static.

17.4.52 L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h

Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 1h
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 001Eh. .

17.4.53 L1 Sub-States Capabilities (L1SCAP)—Offset 204h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 28281Fh

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
23:19	5h RW/O	**Port Tpower_on Value (PTV):** Along with the Port T_POWER_ON Scale Field in the L1 Substates Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF.
18	0h RO	**Reserved (RSVD_1):** Reserved.
17:16	0h RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Substates Capabilities register. '00b': 2 us '01b': 10 us '10b': 100 us '11b': Reserved Required for all Ports that support L1.OFF.
15:8	28h RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF.
7:5	0h RO	**Reserved (RSVD_2):** Reserved
4	1h RW/O	**L1 PM Substates Supported (L1PSS):** When Set this bit indicates that this Port supports L1 PM Substates. For compatibility with possible future extensions, software must not enable L1 PM Substates unless this bit is set. This RWO field must be programmed prior to enabling ASPM.
3	1h RW/O	**ASPM L1.1 Substates Supported (AL11S):** When set, this bit indicates that this port supports L1 substates for ASPM L1.SNOOZ. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
2	1h RW/O	**ASPM L1.2 Supported (AL12S):** When set, this bit indicates that ASPM_L1.OFF is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
1	1h RW/O	**PCI-PM L1.1 Supported (PPL11S):** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

Bit Range	Default & Access	Field Name (ID): Description
0	1h RW/O	**PCI-PM L1.2 Supported (PPL12S):** When set, this bit indicates that L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

17.4.54 L1 Sub-States Control 1 (L1SCTL1)—Offset 208h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**L1.2 LTR Threshold Latency ScaleValue (L12LTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe root port. The value in this field, together with L12LTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L12LTRSTLV times 1 ns 001: L12LTRSTLV times 32 ns 010: L12LTRSTLV times 1024 ns 011: L12LTRSTLV times 32768 ns 100: L12LTRSTLV times 1048576 ns 101: L12LTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
28:26	0h RO	**Reserved (RSVD):** Reserved
25:16	0h RW	**L1.2 LTR Threshold Latency Value (L12OFFLTRTLV):** This field contains the L1.2 LTR Threshold Latency Value for this particular PCIe root port. The value in this field, together with L12LTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
15:8	0h RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time the PCIe root port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved (RSVD_1):** Reserved
3	0h RW	**ASPM L1.1 Enabled (AL11E):** When set, this bit indicates that ASPM L1.SNOOZ substates are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic
2	0h RW	**ASPM L1.2 Enable (AL12E):** When set, this bit indicates that ASPM L1.OFF substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic
1	0h RW	**PCI-PM L1.SNOOZ Enable (PPL11E):** When set, this bit indicates that PCI-PM L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
0	0h RW	**PCI-PM L1.2 Enabled (PPL12E):** When set, this bit indicates that PCI-PM L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.

17.4.55 L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 28h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:3	5h RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# is sampled asserts in L1.OFF state. Tpower_on value is calculated by multiplying the value in this field by the value in the TPOS field. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
2	0h RO	**Reserved (RSVD_1):** Reserved
1:0	0h RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. '00b': 2 us '01b': 10 us '10b': 100us '11b': Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static

17.4.56 Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h

Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEECID):** PCI Express Extended Capability ID (PCIEECID): This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 0019h to this register else it should write 0.

17.4.57 Link Control 3 (LCTL3)—Offset 224h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:9	0h RO	**Enable Lower SKP OS Generation Vector (ELSOSGV):** Enable Lower SKP OS Generation Vector(ELSOSGV): When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is Set in this field and the corresponding bit in the Lower SKP OS Generation Supported Speeds Vector is not set.
8:2	0h RO	**Reserved (RSVD_1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Link Equalization Request Interrupt Enable (LERIE):** Link Equalization Request Interrupt Enable (LERIE): When set, this bit enables the generation of an interrupt to indicate that the Link Equalization Request bit has been set.
0	0h RW	**Perform Equalization (PE):** Perform Equalization (PE): When this bit is 1b and Link Retrain bit is set with the Target Link Speed field set to 8 GT/s, the Downstream Port must perform Link Equalization. This bit is cleared by Root Port upon entry to Link Equalization

17.4.58 Lane Error Status (LES)—Offset 228h

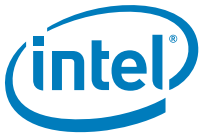
The Lane number is the default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD):** Reserved
3	0h RW/1C/V/P	**Lane 3 Error Status (L3ES):** Lane 3 Error Status (L3ES): Lane 3 detected a Lane-based error.
2	0h RW/1C/V/P	**Lane 2 Error Status (L2ES):** Lane 2 Error Status (L2ES): Lane 2 detected a Lane-based error.
1	0h RW/1C/V/P	**Lane 1 Error Status (L1ES):** Lane 1 Error Status (L1ES): Lane 1 detected a Lane-based error.
0	0h RW/1C/V/P	**Lane 0 Error Status (L0ES):** Lane 0 Error Status (L0ES): Lane 0 detected a Lane-based error.



17.4.59 Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 7F7F7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved.
30:28	7h RW	**Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH):** Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 1 Transmitter Preset (UPL1TP):** Upstream Port Lane 1 Transmitter Preset (UPL1TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	**Reserved (RSVD_1):** Reserved.
22:20	7h RW	**Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH):** Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 1 Transmitter Preset (DPL1TP):** Downstream Port Lane 1 Transmitter Preset (DPL1TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved (RSVD_2):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
14:12	7h RW	**Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH):** Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 0 Transmitter Preset (UPL0TP):** Upstream Port Lane 0 Transmitter Preset (UPL0TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	**Reserved (RSVD_3):** Reserved.
6:4	7h RW	**Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH):** Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 0 Transmitter Preset (DPL0TP):** Downstream Port Lane 0 Transmitter Preset (DPL0TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

17.4.60 Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 7F7F7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
30:28	7h RW	**Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH):** Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 3 Transmitter Preset (UPL3TP):** Upstream Port Lane 3 Transmitter Preset (UPL3TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	**Reserved (RSVD_1):** Reserved
22:20	7h RW	**Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH):** Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 3 Transmitter Preset (DPL3TP):** Downstream Port Lane 3 Transmitter Preset (DPL3TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved (RSVD_2):** Reserved
14:12	7h RW	**Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH):** Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 2 Transmitter Preset (UPL2TP):** Upstream Port Lane 2 Transmitter Preset (UPL2TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	**Reserved (RSVD_3):** Reserved
6:4	7h RW	**Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH):** Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
3:0	Fh RW	**Downstream Port Lane 2 Transmitter Preset (DPL2TP):** Downstream Port Lane 2 Transmitter Preset (DPL2TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

17.4.61 PCI Express Replay Timer Policy 1 (PCIERTP1)—Offset 300h

The Replay Timer controlled by the Replay Timeout field is started when the Retry Buffer is empty and a TLP is placed into it or an Ack/Nak DLLP is received and there are still non-acknowledged packets within the Retry Buffer. The counter continues to count until the next valid Ack DLLP or a NAK DLLP that acknowledges unacknowledged TLPs is received, or it reaches the timeout value specified by this register. When a valid Ack/Nak DLLP is received, the timer is reset to zero and restarted if there are still non-acknowledged packets within the Retry Buffer. Otherwise if the Retry Buffer is empty, the counter is just reset to zero. If the timer reaches the timeout value, the non-acknowledged packets within the Retry Buffer will be replayed.
The default for this register is dependant on the MAX_PAYLOAD_SIZE , the NEGOTIATED_WIDTH, and the NEGOTIATED_SPEED.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: A64F96h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved,
23:20	Ah RW	**Gen 2 x1 (G2X1):** Gen 2 x1 (G2X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 7) * 64 link clocks. For PCIE Gen 2 speed and x1 width For Mobile Express HS-Gear 3 speed and x1 width.

Bit Range	Default & Access	Field Name (ID): Description
19:16	6h RW	**Gen 2 x2 (G2X2):** Gen 2 x2 (G2X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 4) * 64 link clocks. For PCIe Gen 2 speed and x2 width. For Mobile Express HS-Gear 3 speed and x2 width.
15:12	4h RW	**Gen 2 x4 (G2X4):** Gen 2 x4 (G2X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 2 speed and x4 width. For Mobile Express HS-Gear 3 speed and x4 width.
11:8	Fh RW	**Gen 1 x1 (G1X1):** Gen 1 x1 (G1X1): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 10) * 64 link clocks. For 512B MPS: (nnn + 17) * 64 link clocks. For PCIe Gen 1 speed and x1 width. For Mobile Express HS-Gear 2 speed and x1 width.
7:4	9h RW	**Gen 1 x2 (G1X2):** Gen 1 x2 (G1X2): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For PCIe Gen 1 speed and x2 width. For Mobile Express HS-Gear 2 speed and x2 width.

Bit Range	Default & Access	Field Name (ID): Description
3:0	6h RW	**Gen 1 x4 (G1X4):** Gen 1 x4 (G1X4): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/ Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 1 speed and x4 width. For Mobile Express HS-Gear 2 speed and x4 width.

17.4.62 PCI Express Replay Timer Policy 2 (PCIERTP2)—Offset 304h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 1BC00B86h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Lane 0 Lane Number (L0LN):** Lane 0 Lane Number(L0LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 0 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
29:28	1h RW	**Lane 1 Lane Number (L1LN):** Lane 1 Lane Number(L1LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 1 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.

Bit Range	Default & Access	Field Name (ID): Description
27:26	2h RW	**Lane 2 Lane Number (L2LN):** Lane 2 Lane Number(L2LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 2 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
25:24	3h RW	**Lane 3 Lane Number (L3LN):** Lane 3 Lane Number(L3LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 3 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
23	1h RW	**Loopback Master EQ TS1 Enable (LMEQTS1E):** Loopback Master EQ TS1 Enable(LMEQTS1E): When set, the Loopback Master will use EQ TS1 Ordered Sets to direct the Loopback Slave into Loopback from Configuration.Linkwidth.Start. The Preset field of the EQ TS1 Ordered Sets will be specified by Upstream Port Lane X Transmitter Preset and Upstream Port Lane X Receiver Preset Hint fields in the Lane Equalization Control registers.
22	1h RW	**Loopback Master EQ Change Enable (LMEQCE):** Loopback Master EQ Change Enable(LMEQCE): This field is applicable to the case where Loopback is entered from Recovery state. When set, the Loopback Master will set the EC field of the GEN3 TS1 Ordered Sets to the appropriate value based on the ports direction(10b or 11b) to direct the Loopback Slave into Loopback from Recovery state. The Preset field of the GEN3 TS1 Ordered Sets will be specified by Upstream Port Lane X Transmitter Preset and Upstream Port Lane X Receiver Preset Hint fields in the Lane Equalization Control registers.
21:12	0h RO	**Reserved (RSVD):** Reserved
11:8	Bh RW	**Gen 3 x1 (G3X1):** Gen 3 x1 (G3X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For Gen 3 speed and x1 width

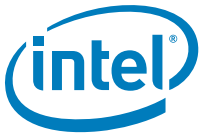
Bit Range	Default & Access	Field Name (ID): Description
7:4	8h RW	**Gen 3 x2 (G3X2):** Gen 3 x2 (G3X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For Gen 3 speed and x2 width
3:0	6h RW	**Gen 3 x4 (G3X4):** Gen 3 x4 (G3X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 1) * 64 link clocks. For 512B MPS: (nnn + 2) * 64 link clocks. For Gen 3 speed and x4 width

17.4.63 PCI Express Status 1 (PCIESTS1)—Offset 328h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LTSM State (LTSMSTATE):** Indicates the LTSM present state. Hex LTSSM States 00DETIDLE 01DETRDY 02DETIDLEP1TOP2 03DETRDYP2TOP1 04DETRDYINP1 05DETRDYINP1EXE 06DETP2POLLSTART 07DETP1POLLSTART 08DETP2TOP0 09DETP1TOP0 0AECPCMPRETRAIN 0BECPCMFAILP0TOP2 0CDETP0TOP2 0DPMODECHANGE 0EECPCMPCIE 0FECPCMUSB3 10DET2POLLINP0 11POLLINGACTIVE 12POLLINGCOMPLIANCEMARGINCNT 13POLLINGCOMPLIANCE 14POLLINGCOMPLIANCESPEEDUP 15POLLINGCOMPLIANCESPEEDDN 16POLLINGCOMPLIANCESPEEDTXEIDLE 17POLLINGCOMPLIANCESPEEDRXEIDLE 18POLLINGCOMPLIANCESPEED 19POLLINGCOMPLIANCESPEEDDONE 1APOLLINGCOMPLIANCEEXIT 1BPOLLINGCONFIGURATION 1CPOLLINGTXEIDLE 1DPOLLINGEND 1EPOLLINGENDWAIT 1FLINKWIDTHSTART 20LINKWIDTHACCEPT 21LANENUMWAIT 22LANENUMACCEPT 23LANEDESKEW 24CONFIGCOMPLETE 25CONFIGIDLE 26LWNEXITRECOVERY 27CONFIGLPBKENTRY 28CONFIGLPBKLWSTART 29CONFIGLPBKSPEEDTXEIDLE 2ACONFIGLPBKSPEEDSTART 2BCONFIGLPBKSPEEDRXEIDLE 2CCONFIGLPBKSPEED 2DCONFIGLPBKREUTSKIP 2ECONFIGLPBKREUT 2FCONFIGLPBKEXITM 30CONFIGLPBKTXEIDLE

Bit Range	Default & Access	Field Name (ID): Description
		31LWNEXIT 32LWNLNK2DETECT 33L0 34TXL0SRXL0 35RXL0STXL0 36TXL0SRXL0S 37L1TXEIDLE 38L1RCVEIDLE 39L1PREENTRY 3AL1ENTRY 3BL1IDLE 3CL1IDLEGEN2WAIT 3DL1EXIT 3EL2TXEIDLE 3FL2RCVEIDLE 40L2IDLEWAIT 41L2IDLERDY 42L2IDLE 43LOOPBACKENTRY 44LPBKACTIVEMTXSKP 45LPBKACTIVEMSKPDSKW 46LOOPBACKACTIVEM 47LPBKSLAVESPEEDTXEIDLE 48LPBKSLAVESPEEDRXEIDLE 49LPBKSLAVESPEED 4ALOOPBACKACTIVES 4BLOOPBACKCMMSKP 4CLOOPBACKCMM 4DLOOPBACKEXITM 4ELOOPBACKEXITS 4FLOOPBACKEXITL0 50LOOPBACKLNK2DETECT 51LOOPBACK2DETECT 52DISTX16TS1DIS 53DISTXEIDLE 54DISWAITSTART 55DISWAITGNT 56DISWAIT4TXMARGIN 57DISWAIT 58DIS2DETECT 59HOTRESETTS1 5AHOTRESETDONE 5BHOTRESETEIDLE 5CRECOVERYRCVRWAIT 5DRECOVERYRCVRMARGINCNT 5ERECOVERYRCVRLOCK 5FRECOVERYDESKEW 60RECOVERYRCVRCFG 61RECOVERYSPEED 62RECOVERYSPEEDTXEIDLE 63RECOVERYSPEEDRXEIDLE

Bit Range	Default & Access	Field Name (ID): Description
		64RECOVERYSPEEDREADY 65RECOVERYIDLE 66RECOVERYEXITDETECT 67RECOVERYLNK2DETECT 68RECOVERYEXITLPBK 69RECOVERYEXITL0 6ARECOVERYEXITDIS 6BRECOVERYEXITRST Note: This register field could be used by REUT software to monitor the link LTSSM substates.
23	0h RO	**Reserved (RSVD):** Reserved.
22:19	0h RO/V	**Link Status (LNKSTAT):** During Link initialization the Link will always traverse this list of state from the top (0000) to the bottom of the list (0111). One or more power management states may be skipped, but the direction of list traversal will remain the same. 0000 Link Down 0001 : Link Retrain 0011 : L1 0100 : L2 0101 : L3 0111 : L0 (Link Up) 1000 : L0s (Transmit [amp] Receive) 1001 : L0s (Transmit only) 1010 : L0s (Receive only) All others reserved
18:17	0h RO/V	**Replay Number (REPLAYNUM):** Number of times the Retry Buffer has been replayed since the last Link initialization / re-training. When the Data Link Layer has replayed the contents of the Retry Buffer four times a Link re-training will be initiated which will reset this value back to zero.
16	0h RO/V	**Data Link Layer Retry (DLLRETRY):** Indicates when the Data Link Layer has received a corrupted TLP or has detected a dropped packet and is currently waiting for the remote agent to re-transmit the corrupted/dropped packet. The value of Next Receive Sequence Number will be the sequence number associated with the corrupted packet.
15:12	0h RO/V	**Lane Status (LANESTAT):** Indicates which lanes are trained. A '1' indicates that the corresponding lane is trained (i.e. bit 0 = '1' means lane 0 is trained).
11:0	0h RO/V	**Next Transmitted Sequence Number (NXTTXSEQNUM):** This is the sequence number to be applied to and pre-pended to the next outgoing TLP.

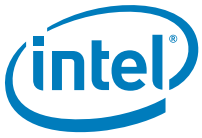
17.4.64 PCI Express Status 2 (PCIESTS2)—Offset 32Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**PCIe Port 3 Non-Common Clock With SSC Mode Enable Strap (P3PNCCWSSCMES):** '0': PCIe port 3 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 3 is enabled to operate in non-common clock mode with SSC enabled.
30	0h RO/V	**PCIe Port 2 Non-Common Clock With SSC Mode Enable Strap (P2PNCCWSSCMES):** '0': PCIe port 2 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 2 is enabled to operate in non-common clock mode with SSC enabled.
29	0h RO/V	**PCIe Port 1 Non-Common Clock With SSC Mode Enable Strap (P1PNCCWSSCMES):** '0': PCIe port 1 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 1 is enabled to operate in non-common clock mode with SSC enabled.
28	0h RO/V	**PCIe Port 0 Non-Common Clock With SSC Mode Enable Strap (P0PNCCWSSCMES):** '0': PCIe port 0 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 0 is enabled to operate in non-common clock mode with SSC enabled.
27:16	0h RO/V	**Next Receive Sequence Number (NXTRCVSEQ):** This is the sequence number associated with the TLP that is expected to be received next.



Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/1C/V	**Cause of Last Recovery Event (CLRE):** Cause of Last Recovery Event (CLRE): This field logs the cause of the entry to Recovery from L0. Only the first cause of Recovery is captured, until the register is cleared. Encoding Recovery Event 0000 No Recovery. 0001 Recovery entry triggered by remote device. 0010 Link Layer initiated Link Retrain due to error. 0011 De-skew buffer full. 0100 L0s exit time-out. 0101 Elastic Buffer overrun/underrun. 0110 Triggered by speed change. 0111 Link upconfiguration/downconfiguration. 1000 L0 Electrical Idle Inference. 1001 Any of the Link Retrain, CMM Start, Hot Reset, Link Disable, REUT Loopback Master or REUT Forced Loopback Master bit set. 1010 Received EIOS for RXL0s entry when ASPM L0s is disabled. 1011 Entry to Recovery from RXL0s due to PME timeout. Others Reserved.
11:0	0h RO/V	**Last Acknowledged Sequence Number (LASTACKSEQNUM):** This is the sequence number associated with the last acknowledged TLP.

17.4.65 PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h

Note that selecting a lane number that does not exist for a port may result in undefined behavior.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 2A000016h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**GEN3 Intel CMM Scrambler Bypass (G3ICMMSB):** GEN3 Intel CMM Scrambler Bypass(G3ICMMSB): When set, the Intel CMM pattern will bypass scrambling in GEN3. This bit does not impact non Intel CMM pattern. The TSx and SOS prior to Intel CMM will still be scrambled normally. Note: This bit must be set prior to enabling Intel CMM, by setting the PCIECMMPC.START. Note: When operating in Mobile Express mode, this field is not applicable.
30	0h RO	**Reserved (RSVD):** Reserved
29	1h RW	**CMM Symbol[3] Select (SYM3SEL):** 0: selects CMM Symbol [lb]3[rb] to a control character 1: selects CMM Symbol [lb]3[rb] as a data character
28	0h RW	**CMM Symbol[2] Select (SYM2SEL):** 0: selects CMM Symbol [lb]2[rb] to a control character 1: selects CMM Symbol [lb]2[rb] as a data character
27	1h RW	**CMM Symbol[1] Select (SYM1SEL):** 0: selects CMM Symbol [lb]1[rb] to a control character 1: selects CMM Symbol [lb]1[rb] as a data character
26	0h RW	**CMM Symbol[0] Select (SYM0SEL):** 0: selects CMM Symbol [lb]0[rb] to a control character 1: selects CMM Symbol [lb]0[rb] as a data character
25:24	2h RW	**CMM Sync Header (CMMSH):** CMM Sync Header(CMMSH): Specifies the Sync Header for the Intel CMM pattern specified in PCIECMMSB. Note: Due to implementation limitation, only a value of 10b is supported. All the other values are not supported.
23:22	0h RO/V	**CMM Error Lane Number (ERRLANENUM):** This field contains the lane number of the failing lane. Only valid when CMM Error Detected is 1.
21:16	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO/V	**CMM Invert (INVERT):** Indicates which lanes are inverted 000: No inversion 001: Lanes 0 010: Lanes 1 011: Lanes 2 100: Lanes 3 This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated)
12:10	0h RO/V	**CMM Symbol Error Number Invert (SYMERRNUMINV):** Indicates which register number miscompared on the failing lane, if the failing lane was an inverted lane. Only valid when CMM Error Detected is 1. 000: CMM Data D0 001: CMM Data D0 010: CMM Data D0 011: CMM Data D1 100: CMM Data D2 101: CMM Data D3 110: CMM Data D0 111: CMM Data D0
9:8	0h RO/V	**CMM Symbol Error Number (SYMERRNUM):** Indicates which register number miscompared on the failing lane, if the failing lane was not inverted. Only valid when CMM Error Detected is 1. 00: CMM Data 0 01: CMM Data 1 10: CMM Data 2 11: CMM Data 3
7	0h RW/1C/V	**CMM Error Detected (ERRDET):** 1: An error was detected 0: No error detected Note: This bit will be shadowed to an observability pin that can be used for IRQ generation.
6:5	0h RW	**Select Lane Number to be inverted for CMM (SLNINVCMM):** Select Lane Number to be inverted for CMM
4	1h RW	**CMM AutoInvert (AUTOINVERT):** 1: CMM autosequences through the inversion 0: CMM does not sequence inversion
3	0h RO/V	**CMM Status (STAT):** This bit is set when the CMM Start bit is set and cleared when the CMM mode has been entered successfully. 0: Compliance Measurement Mode is not active or CMM mode has been entered successfully. 1: Set as a result of CMM Start bit being set.
2	1h RW	**CMM Invert Enable (INVEN):** 1: Enables the Inversion of the lane 0: Lane not inverted
1	1h RW	**Reserved (RSVD_2):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/L	**CMM Start (START):** 1: Start CMM 0: Stop CMM

17.4.66 PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 4ABCB5BCh

Bit Range	Default & Access	Field Name (ID): Description
31:24	4Ah RW	**CMM Data [3] (DATA3):** This character contains CMM Data [lb]3[rb] that will be transmitted on the link.
23:16	BCh RW	**CMM Data [2] (DATA2):** This character contains CMM Data [lb]2[rb] that will be transmitted on the link.
15:8	B5h RW	**CMM Data [1] (DATA1):** This character contains CMM Data [lb]1[rb] that will be transmitted on the link.
7:0	BCh RW	**CMM Data [0] (DATA0):** This character contains CMM Data [lb]0[rb] that will be transmitted on the link.

17.4.67 PTM Propagation Delay (PTMPD)—Offset 390h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Propagation Delay Value (CPTMPDV):** Current PTM Propagation Delay Value(CPTMPDV): This field reports the current PTM Propagation Delay value captured from the last successful PTM dialog.

17.4.68 PTM Lower Local Master Time (PTMLLMT)—Offset 394h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Lower Local Master Time Value (CPTMLLMTV):** Current PTM Lower Local Master Time Value(CPTMLLMTV): This field reports the lower fields bits 31:0 of the Local TSC time value.

17.4.69 PTM Upper Local Master Time (PTMULMT)—Offset 398h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Upper Local Master Time Value (CPTMULMTV):** Current PTM Upper Local Master Time Value(CPTMULMTV): This field reports the upper fields bits 63:32 of the Local TSC time value.

17.4.70 PTM Pipe Stage Delay Configuration 1 (PTMPSDC1)—Offset 39Ch

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN1 X2 RX Pipe Stage Delay (G1X2RPSD):** GEN1 X2 RX Pipe Stage Delay(G1X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN1 X2 TX Pipe Stage Delay (G1X2TPSD):** GEN1 X2 TX Pipe Stage Delay(G1X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN1 X1 RX Pipe Stage Delay (G1X1RPSD):** GEN1 X1 RX Pipe Stage Delay(G1X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN1 X1 TX Pipe Stage Delay (G1X1TPSD):** GEN1 X1 TX Pipe Stage Delay(G1X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.4.71 PTM Pipe Stage Delay Configuration 2 (PTMPSDC2)—Offset 3A0h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN2 X1 RX Pipe Stage Delay (G2X1RPSD):** GEN2 X1 RX Pipe Stage Delay(G2X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN2 X1 TX Pipe Stage Delay (G2X1TPSD):** GEN2 X1 TX Pipe Stage Delay(G2X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN1 X4 RX Pipe Stage Delay (G1X4RPSD):** GEN1 X4 RX Pipe Stage Delay(G1X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN1 X4 TX Pipe Stage Delay (G1X4TPSD):** GEN1 X4 TX Pipe Stage Delay(G1X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.4.72 PTM Pipe Stage Delay Configuration 3 (PTMPSDC3)—Offset 3A4h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN2 X4 RX Pipe Stage Delay (G2X4RPSD):** GEN2 X4 RX Pipe Stage Delay(G2X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN2 X4 TX Pipe Stage Delay (G2X4TPSD):** GEN2 X4 TX Pipe Stage Delay(G2X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN2 X2 RX Pipe Stage Delay (G2X2RPSD):** GEN2 X2 RX Pipe Stage Delay(G2X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN2 X2 TX Pipe Stage Delay (G2X2TPSD):** GEN2 X2 TX Pipe Stage Delay(G2X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.4.73 PTM Pipe Stage Delay Configuration 4 (PTMPSDC4)—Offset 3A8h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN3 X2 RX Pipe Stage Delay (G3X2RPSD):** GEN3 X2 RX Pipe Stage Delay(G3X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN3 X2 TX Pipe Stage Delay (G3X2TPSD):** GEN3 X2 TX Pipe Stage Delay(G3X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN3 X1 RX Pipe Stage Delay (G3X1RPSD):** GEN3 X1 RX Pipe Stage Delay(G3X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN3 X1 TX Pipe Stage Delay (G3X1TPSD):** GEN3 X1 TX Pipe Stage Delay(G3X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.4.74 PTM Pipe Stage Delay Configuration 5 (PTMPSDC5)—Offset 3ACh

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:8	0h RW	**GEN3 X4 RX Pipe Stage Delay (G3X4RPSD):** GEN3 X4 RX Pipe Stage Delay(G3X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN3 X4 TX Pipe Stage Delay (G3X4TPSD):** GEN3 X4 TX Pipe Stage Delay(G3X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.4.75 PTM Extended Config (PTMECFG)—Offset 3B0h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20:18	0h RW	**Periodic Local TSC Link Fetch Frequency (PLTLFF):** Periodic Local TSC Link Fetch Frequency (PLTLFF): When this register is programmed to a non-zero values, the Local TSC Link Clock would perform a periodic fetch to obtain the latest TSC from the Local TSC XTAL Clock domain. This mechanism would ensure the Root Port Local TSC Link is always synchronized with the actual TSC as Link Clock domain is able to drift due to SSC. 000: Disable this feature. 001: Always pull without waiting for expiration. 010: Every 8 clocks 011: Every 16 clocks 100: Every 32 clocks 101: Every 64 clocks 110: Every 128 clocks 111: Every 256 clocks This register is only available in Port 1. Note: Software is expected to program this register prior to setting PTM Enable.
17:15	0h RW/1C/V	**Global Time Fetch Retry Counter (GTFRC):** Global Time Fetch Retry Counter. This register is incremented when the Root Port detected a retry on each Global Time Fetch on IOSF Sideband. The Root Port would increment the value of this register whenever ARU re-sends a LocalSync message. If more than 7 Retries are detected during the Global Time Fetch, Root Port would keep the value of this register to 111 (max) value. Software is expected to write 111 to this register to clear the entire field to 0. Note: For each x4 instance, only the value from Port 1 is used.
14:13	0h RW/1C/V	**Global Time Fetch Fail Counter (GTFFC):** Global Time Fetch Fail Counter. This register is incremented when the Root Port detected a fail on each Global Time Fetch on IOSF Sideband. The Root Port would increment the value of this register whenever ARU sends a SyncComp with the Fail status. If more than 3 failures are detected in the Global Time Fetch, Root Port would keep the value of this register to 111 (max) value. Software is expected to write 11 to this register to clear the entire field to 0. Note: For each x4 instance, only the value from Port 1 is used.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Global Time Fetch Status Pending Completion (GTFSPC):** Global Time Fetch Status Pending Completion. This register is set to 1 by the Root Port when it is in progress of fetching the Global Time from ARU. Note: For each x4 instance, only the value from Port 1 is used.
11:9	0h RW	**Periodic Global Time Stamp Counter Fetch Frequency (PGTSCFF):** Periodic Global Time Stamp Counter Fetch Frequency (PGTSCFF) : This field determine the frequency the Root Port would autonomously fetch the Global Time Stamp Counter. 00: 10us 01: 100us 10: 500us 10: 1ms Software is expected to program this bit first before programming the PGTSCFE register. Attribute: Dynamic Note: For each x4 instance, only the value from Port 1 is used.
8	0h RW	**Periodic Global Time Stamp Counter Fetch Enable (PGTSCFE):** Periodic Global Time Stamp Counter Fetch Enable (PGTSCFE) : When this bit set, the Controller will re-fetch the Global Time from the Always Running Unit (ARU). Once Fetch is completed, the Controller would update all the Local TSC with the newly fetch Global Time. If any PTM dialog is initiated while the re-fetch occurred, the Controller would use the existing Local TSC timers. Hardware would clear this bit upon completed fetching the Global Time. Attribute : Dynamic Note: For each x4 instance, only the value from Port 1 is used.
7	0h RW	**Trigger Global Time Stamp Counter Fetch Enable (TGTSCFE):** Trigger Global Time Stamp Counter Fetch Enable (TGTSCFE) : When this bit set, the Controller will re-fetch the Global Time from the Always Running Unit (ARU). Once Fetch is completed, the Controller would update all the Local TSC with the newly fetch Global Time. If any PTM dialog is initiated while the re-fetch occurred, the Controller would use the existing Local TSC timers. Hardware would clear this bit upon completed fetching the Global Time. Software can only set this register if PGTSCFE is not set. Attribute : Dynamic Note: For each x4 instance, only the value from Port 1 is used.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**PTM Request Periodic ACK Enable (PTMRPAE):** PTM Request Periodic ACK Enable (PTMRPAE) : When this register is set to 1, whenever a valid PTM request TLP is received, the Link Layer would transmit multiple ACK DLLPs corresponding to the PTM Request message. The number of ACK DLLP that the Link Layer would transmit is based on the PTMRNOPAD register. Attribute : Static Note: For each x4 instance, only the value from Port 1 is used.
5:4	0h RW	**PTM Request Number Of Periodic ACK DLLP (PTMRNOPAD):** PTM Request Number Of Periodic ACK DLLP (PTMRNOPAD) : When PTMRPAE is enable, whenever a valid PTM Request message is received, the Link Layer would transmit multiple ACK DLLP corresponding to the receiving of the PTM Request message. This register define the number of DLLP ACK will be transmitted as high priority. 00 - TX 1 DLLP ACK 01 - TX 2 DLLP ACK 10 - TX 3 DLLP ACK 11 - TX 4 DLLP ACK Attribute : Static Note: For each x4 instance, only the value from Port 1 is used.
3:0	0h RW	**IOSF Max Allowed Delay programming (IOSFMADP):** IOSF Max Allowed Delay programming (IOSFMADP): bits Status 0000 Bound Range Low 0001 Bound Range 2 1000 Bound Range Max others reserved

17.4.76 PTM Lower T2 Time Stamp (PTMLT2TSTMP)—Offset 3B4h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Latest Captured Lower T2 TimeStamp (LCLT2TS):** Latest Captured Lower T2 TimeStamp (LCLT2TS). This field shows the latest lower 32-bit of T2 TimeStamp captured by the Root Port in TSC Clock Domain when the Root Port received a valid PTM Request message. The renewable T2 TimeStamp due to a duplicate PTM Request would also be reflected in this field.

17.4.77 PTM Upper T2 Time Stamp (PTMUT2TSTMP)—Offset 3B8h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Latest Captured Upper T2 TimeStamp (LCUT2TS):** Latest Captured Upper T2 TimeStamp (LCUT2TS). This field shows the latest upper 32-bit of T2 TimeStamp captured by the Root Port in TSC Clock Domain when the Root Port received a valid PTM Request message. The renewable T2 TimeStamp due to a duplicate PTM Request would also be reflected in this field.

17.4.78 Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**mod-PHY Power Gating Disable Fuse (mPHYPGD):** 0: mod-PHY power gating is enabled. 1: mod-PHY power gating is disabled. Note: Prior to fuse pull, the default of this bit is specified in the 'Reset' column of this field. The default value will reflect the fuse value once fuse pull is done.
30:0	0h RO	**Reserved (RSVD):** Reserved

17.4.79 Thermal and Power Throttling (TNPT)—Offset 418h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 930h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Throttle Period (TP):** Throttle Period (TP): If any of the TNPT.DRXLTE or TNPT.DTXLTE bit is '1, this field defines the duration in milliseconds that defines the Throttling Window. When TNPT.TTG is set to 0, the effective Throttling Period is: 00h: 1 ms 01h: 2 ms : : FFh: 256 ms Note: The Throttle Period will have an uncertainty of +/-1 ms. When TNPT.TTG is set to 1, the effective Throttling Period is: 00h: 100 us 01h: 200 us : : FFh: 25.6 ms Note: The Throttle Period will have an uncertainty of +/-100 us. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling. Note: If TNPT.TT is programmed to a value bigger than TNPT.TP, the hardware behavior is undefined.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RW	**Throttle Time (TT):** Throttle Time (TT): If any of the TNPT.DRXLTE or TNPT.DTXLTE bit is '1, this field defines the period of the Throttling Zone within the Throttling Window specified by TNPT.TP. The value specified in this field will be multiplied by the respective multiplier in TNPT.TSLxM fields depending on the throttling severity indication received together with the Throttling State change indication. When TNPT.TTG is set to 0, the effective Throttle Time is: 00h: 1 ms 01h: 2 ms : 3Fh: 64 ms Others: Alias to 3Fh. Note: The Throttle Period will have an uncertainty of +/-1 ms. When TNPT.TTG is set to 1, the effective Throttle Time is: 00h: 100 us 01h: 200 us : 3Fh: 6.4 ms Note: The Throttle Period will have an uncertainty of +/-100 us. Note: If the reserved encoding is programmed to this field, hardware will behave the same as if the field is programmed to 3Fh. Note: Since the design is using a 1 ms tick for this timer, the Throttle Time will have an uncertainty of +/-1 ms. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling. Note: If TNPT.TT is programmed to a value bigger than TNPT.TP, the hardware behavior is undefined.
15:12	0h RO	**Reserved (RSVD):** Reserved
11:10	2h RW	**Throttling Severity Level 3 Multiplier (TSL3M):** Throttling Severity Level 3 Multiplier (TSL3M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: Always throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.

Bit Range	Default & Access	Field Name (ID): Description
9:8	1h RW	**Throttling Severity Level 2 Multiplier (TSL2M):** Throttling Severity Level 2 Multiplier (TSL2M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: Always throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.
7:6	0h RW	**Throttling Severity Level 1 Multiplier (TSL1M):** Throttling Severity Level 1 Multiplier (TSL1M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: No throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the link throttling
5:4	3h RW	**Throttling Severity Level 0 Multiplier (TSL0M):** Throttling Severity Level 0 Multiplier (TSL0M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: No throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.
3	0h RO	**Reserved (RSVD_1):** Reserved
2	0h RW	**Throttling Timer Granuality (TTG):** Throttling Timer Granuality (TTG): This register determines the granuality of the Thermal Throttling timers. This provides a smaller granuality

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Dynamic RX Link Throttling Enable (DRXLTE):** Dynamic RX Link Throttling Enable (DRXLTE): '0b: Dynamic Link RX Throttling mechanism is disabled. '1b: Dynamic Link RX Throttling mechanism is enabled. PCIe Root Port will induce the link to enter RXL0s. The duty cycle of the throttling window is configurable based on the throttling severity. Note: This field can only be set if the remote component supports TXL0s.
0	0h RW	**Dynamic TX Link Throttling Enable (DTXLTE):** Dynamic TX Link Throttling Enable (DTXLTE): '0b: Dynamic Link TX Throttling mechanism is disabled. '1b: Dynamic Link TX Throttling mechanism is enabled. PCIe Root Port will induce the link to enter TXL0s. The duty cycle of the throttling window is configurable based on the throttling severity. Note: This field can only be set if the remote component supports TXL0s.

17.4.80 Dynamic Lane Switch (DYNLNSW)—Offset 41Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved (RSVD):** Reserved.
0	0h RW	**Hardware Re-Do Preset to Coefficient Mapping Query After Lane Switching (HWRP2CM):** Hardware Re-Do Preset to Coefficient Mapping Query After Lane Switching (HWRP2CM): When this bit is set, the PCIe-SIP Controller would query the Preset to Coefficient mapping through the PIPE GetLocalPresetCoefficients and LocalTxCoefficientsValid interface whenever the Lane Switch ownership has transitioned to PCIe (from another Controller). Note that if this bit is set while the HPCMQE bit is set, the PCIe-SIP Controller would only perform the query once. Unlike the HPCMQE bit, the PCIe-SIP Controller would not clear this bit after completing the query over the PIPE interface. Register Attribute: Static.

17.4.81 Power Control Enable (PCE)—Offset 428h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 9h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved (RSVD):** Reserved for Force Isolate and Reset Together. This bit is not used. The timing between isolate and reset can be controller through PGCBCTL register.
5	0h RW	**Hardware Autonomous Enable (HAE):** Hardware Autonomous Enable (HAE): If set, and the corresponding per-LTSSM state power gating enable bit is also set, then controller power gating will be done when the controller is idle and the controller power gating condition is met in that particular LTSSM state. Refer to PCIEPMECTL2 register for the per-LTSSM state power gating enable bit. If either this bit. is not set or the corresponding per-LTSSM state power gating enable bit is not set, then controller power gating will not be done in that LTSSM state. Note: For each x4 instance, only the value from Port 0 is used. NOTE: If this bit is set, then bits[lb]2:0[rb] must be '000.
4	0h RO	**Reserved (RSVD_1):** Reserved for Force Isolate and Reset Together. This bit is not used. The timing between isolate and reset can be controller through PGCBCTL register.
3	1h RW/L	**Sleep Enable (SE):** Sleep Enable (SE): If clear, Sleep indication to the retention flops will never assert. If set, Sleep indication will be assert to the retention flops as part of the hardware autonomous controller power gating entry flow.
2	0h RO	**Reserved (RSVD_2):** Reserved for D3-Hot Enable. Not supported. RTD3 is supported instead.
1	0h RO	**Reserved (RSVD_3):** Reserved for D0i3 Enable. No support for D0i3.
0	1h RW	**PMC Request Enable (PMCRE):** PMC Request Enable (PMCRE): When set, the controller will only power gate when pmc_[lt]ip[gt]_sw_pg_req_b = '0 and hardware autonomous controller power gating conditions are met. When clear, controller will power gate immediately when the hardware autonomous controller power gating conditions are met regardless of the state of pmc_[lt]ip[gt]_sw_pg_req_b.

17.4.82 PGCB Control1 (PGCBCTL1)—Offset 42Ch

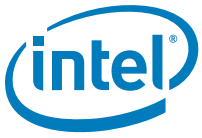
This register specifies the minimum number of delay clocks the PGCB should wait between various states.
Note: For each x4 instance, only the value from Port 0 is used.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 14155555h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved for cfg_trsvd0. Not applicable since frc_clk_srst_en is tied to '0.
29:28	1h RW	**cfg_trstup2frcclks (trstup2frcclks):** cfg_trstup2frcclks(cfg_trstup2frcclks): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
27:26	1h RW	**cfg_tclksonack_cp (tclksonack_cp):** cfg_tclksonack_cp(cfg_tclksonack_cp): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
25:24	0h RO	**Reserved (RSVD_1):** Reserved for cfg_tclksoffack_srst. Not applicable since frc_clk_srst_en is tied to 0.
23:22	0h RO	**Reserved (RSVD_2):** Reserved for cfg_tclksonack_srst. Not applicable since frc_clk_srst_en is tied to 0.
21:20	1h RW	**cfg_tpokup (tpokup):** cfg_tpokup(cfg_tpokup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
19:18	1h RW	**cfg_tpokdown (tpokdown):** cfg_tpokdown(cfg_tpokdown): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks



Bit Range	Default & Access	Field Name (ID): Description
17:16	1h RW	**cfg_tlatchdis (tlatchdis):** cfg_tlatchdis(cfg_tlatchdis): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
15:14	1h RW	**cfg_tsleepinactiv (tsleepinactiv):** cfg_tsleepinactiv(cfg_tsleepinactiv): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
13:12	1h RW	**cfg_tinaccrstup (tinaccrstup):** cfg_tinaccrstup(cfg_tinaccrstup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
11:10	1h RW	**cfg_taccrstup (taccrstup):** cfg_taccrstup(cfg_taccrstup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
9:8	1h RW	**cfg_tlatchen (tlatchen):** cfg_tlatchen(cfg_tlatchen): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
7:6	1h RW	**cfg_tdeisolate (tdeisolate):** cfg_tdeisolate(cfg_tdeisolate): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
5:4	1h RW	**cfg_trstdown (trstdown):** cfg_trstdown(cfg_trstdown): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
3:2	1h RW	**cfg_tisolate (tisolate):** cfg_tisolate(cfg_tisolate): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
1:0	1h RW	**cfg_tsleepact (tsleepact):** cfg_tsleepact(cfg_tsleepact): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

17.4.83 PGCB Control2 (PGCBCTL2)—Offset 430h

This register specifies the minimum number of delay clocks the PGCB should wait between various states.
Note: For each x4 instance, only the value from Port 0 is used.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 54h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved.
7:6	1h RW	**cfg_trsvd4 (trsvd4):** cfg_trsvd4(cfg_trsvd4): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
5:4	1h RW	**cfg_trsvd3 (trsvd3):** cfg_trsvd3(cfg_trsvd3): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
3:2	1h RW	**cfg_trsvd2 (trsvd2):** cfg_trsvd2(cfg_trsvd2): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	**Reserved (RSVD_1):** Reserved for cfg_trsvd1. Not applicable since frc_clk_srst_en is tied to 0.

17.4.84 Equalization Configuration 1 (EQCFG1)—Offset 450h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 3102h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Recovery Entry Count (REC):** Recovery Entry Count (REC): This field indicates the value of the Recovery Entry Counter. This is a 1-based counter. Software must read this register multiple times. The value is valid only if the same value is read out on both of the reads.
23	0h RW	**Recovery Entry and Idle Framing Error Count Enable (REIFECE):** Recovery Entry and Idle Framing Error Count Enable (REIFECE): This bit, when set by software turns on the Recovery Entry Counter and the per-lane Idle Framing Error Counter. The counters are reset when this bit is cleared. This bit is expected to be used by the Software Preset/Coefficient Search tool but is not precluded to be used for other debug purpose. The value of the Recovery Entry Count can be read through EQCFG1.REC field. The value of the Idle Framing Error Count can be read through the Monitor Mux register.
22	0h RW	**Quiesce Guarantee (QG):** Quiesce Guarantee (QG): When set, the Quiesce Guarantee bit in the transmitted TS2 Ordered Set will be set in Recovery.RcvrCfg. When clear, the Quiesce Guarantee bit in the transmitted TS2 Ordered Set will be clear. In all other states, the Quiesce Guarantee bit is Reserved.
21	0h RW	**Link Equalization Request SMI Enable (LERSMIE):** Link Equalization Request SMI Enable (LERSMIE): When set, this bit enables the generation of an SMI to indicate that the Link Equalization Request bit has been set. This mode is meant for survivability purpose such that BIOS can be invoked to address the Re-Equalization request.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Reset EIEOS Interval Count (REIC):** Reset EIEOS Interval Count(REIC): When set, allows the root port to restrict the device from sending EIEOS until after 65536 TS1 Ordered Sets have been transmitted in Phase 3 of the Link Equalization, in the window when the receiver is evaluating the remote transmitter settings..
19	0h RW	**Link Equalization Bypass (LEB):** Link Equalization Bypass (LEB): When set, the root port will never initiate entry to Recovery.Equalization state. This includes never send EQ TS2 in Recovery.RcvrCfg that could cause the device to set start_equalization_w_preset variable. Note: This bit only affects the initial autonomous transition to Link Equalization state when equalization_done_8GT_data_rate = 0. This bit does not affect the software-direction to re-perform Link Equalization.
18	0h RW	**Link Equalization Phase 2 and 3 Bypass (LEP23B):** Link Equalization Phase 2 and 3 Bypass(LEP23B): When set, bypasses the Phase 2 and Phase 3 of Link Equalization. Once Phase 1 is completed, Root Port transitions from Phase 1 directly to Recovery.RcvrLock.
17	0h RW	**Link Equalization 3 Bypass (LEP3B):** Link Equalization 3 Bypass(LEP3B): When set, bypasses the Phase 3 of Link Equalization. Once Phase 2 is completed, Root Port transitions from Phase 2 directly to Recovery.RcvrLock.
16	0h RW	**Remote Transmit Link Equalization Preset/Coefficient Evaluation Bypass (RTLEPCEB):** Remote Transmit Link Equalization Preset/Coefficient Evaluation Bypass (RTLEPCEB): When set, this bit disables the Hardware Autonomous Preset/ Coefficient Search mechanism to search for the best Preset or Coefficient by traversing the Preset or Coefficient List and checking the receiver eye width margin for each of the settings. Instead, the Preset/Coefficient values used by the remote Transmitter will be accepted and the Link Equalization phase will be completed after one round of receiver link training, excluding margining. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Remote Transmitter Preset Coefficient Override Enable (RTPCOE):** Remote Transmitter Preset Coefficient Override Enable (RTPCOE): When set, this bit disables the hardware mechanism to search for the best Preset or Coefficient by traversing the Preset or Coefficient List and checking the receiver eye width margin for each of the settings. Instead, the Preset or Coefficient values specified by the override fields are used. If RTPCL1.PCM = 1, the Preset Override values for each lanes is derived from the following register fields: Lane 0: RTPCL1.RTPRECL0PL0. Lane 1: RTPCL1.RTPOSTCL0PL1. Lane 2: RTPCL1.RTPRECL1PL2. Lane 3: RTPCL1.RTPOSTCL1PL3. If RTPCL1.PCM = 0, the Coefficient Override values for each lanes is derived from the following register fields: Lane 0: RTPCL1.RTPRECL0PL0 and RTPCL1.RTPOSTCL0PL1. Lane 1: RTPCL1.RTPRECL1PL2 and RTPCL1.RTPOSTCL1PL3. Lane 2: RTPCL1.RTPRECL2PL4 and RTPCL2.RTPOSTCL2PL5. Lane 3: RTPCL2.RTPRECL3PL6 and RTPCL2.RTPOSTCL3PL7. BIOS must ensure that the corresponding RTPCL* registers above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
14	0h RW	**Link Equalization Request SCI Enable (LERSCIE):** Link Equalization Request SCI Enable (LERSCIE): When set, this bit enables the generation of an SCI to indicate that the Link Equalization Request bit has been set. This mode is meant for survivability purpose such that SCI handler can be invoked to address the Re-Equalization request.

Bit Range	Default & Access	Field Name (ID): Description
13	1h RW/1S/V	**Hardware Preset to Coefficient Mapping Query Enable (HPCMQE):** Hardware Preset to Coefficient Mapping Query Enable(HPCMQE): When set, the controller will query the Preset to Coefficient mapping through the PIPE GetLocalPresetCoefficients and LocalTxCoefficientsValid interface whenever this bit transitions from 0 to 1. The default of this register bit is 1, indicating that the Preset to Coefficient mapping query will be done on the PIPE interface once coming out of reset. Controller will then update the Preset-Coefficient Mapping registers with the corresponding Coefficient, for each Preset. Controller will also update the LFFS Local LF and Local FS field with the local PHY LF and FS values. Hardware will clear this bit when the Preset to Coefficient mapping query over the PIPE interface is completed. If the Hardware Preset to Coefficient Mapping mechanism is never enabled, the value of the Preset to Coefficient mapping configured by BIOS through the Preset-Coefficient Mapping registers will be used instead of querying through the PIPE interface. Note: BIOS should check to ensure that this field is cleared before enabling Controller Power Gating or mod-PHY Power Gating.
12	1h RO/V	**Hardware Autonomous Equalization Done (HAED):** Hardware Autonomous Equalization Done(HAED): This bit will be cleared when Hardware Autonomous Preset/Coefficient Search starts and will be set when Hardware Autonomous Preset/Coefficient Search is done. This bit is polled by software to ensure that the Hardware Autonomous Preset/Coefficient Search is done before proceeding with the next software sequencing. Some of the Hardware Autonomous Preset/ Coefficient search algorithm may involve the hardware initiating multiple speed change to allow multiple iterations of Link Equalization to be done with different Preset/Coefficient lists. This bit will remain cleared until the iterations are done.

Bit Range	Default & Access	Field Name (ID): Description
11:8	1h RW	**Receiver Wait Time For New Equalization Value Evaluation (RWTNEVE):** Receiver Wait Time For New Equalization Value Evaluation (RWTNEVE): For Downstream Port: This field specifies the amount of time the receiver will wait after entering Phase 3 and sending the new Preset or Coefficient values through the TS1 Ordered Sets before validating the Block Alignment and eventually evaluate the incoming ordered sets (RXEqEval on the PIPE interface asserts). For Upstream Port: This field specifies the amount of time the receiver will wait after entering Phase 2 and sending the new Preset or Coefficient values through the TS1 Ordered Sets before validating the Block Alignment and eventually evaluate the incoming ordered sets (RXEqEval on the PIPE interface asserts). For both Upstream and Downstream Port, this field also specifies the amount of time the receiver will wait after entering Phase 1 before instructing the receiver to adapt to the incoming ordered sets. For Loopback Master: This field specifies the amount of time the receiver will wait after instructing the Loopback Slave to apply a specific Preset through EQ TS1. 0h: 500 ns. 1h: 1 us. 2h: 2 us. 3h: 3 us. 4h: 4 us. : : Fh:15 us.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**EQ TS2 in Recovery.ReceiverConfig Enable (EQTS2IRRC):** EQ TS2 in Recovery.ReceiverConfig Enable(EQTS2IRRC): When set, enables the transmitter to send EQ TS2 in Recovery.RcvrCfg state even when equalization_done_8GT_data_rate variable is 1b, provided that the Downstream Port advertised 8.0 GT/s data rate support in Recovery.RcvrLock, and 8.0 GT/s data rate support has been advertised in the Configuration.Complete or Recovery.RcvrCfg substates by the Upstream Port since exiting the Detect state, and eight consecutive TS1 or TS2 Ordered Sets were received on any configured Lane prior to entry to this substate with speed_change bit set to 1b. When clear, the transmitter can only send EQ TS2 if equalization_done_8GT_data_rate variable is 0b and the Downstream Port advertised 8.0 GT/s data rate support in Recovery.RcvrLock, and 8.0 GT/s data rate support has been advertised in the Configuration.Complete or Recovery.RcvrCfg substates by the Upstream Port since exiting the Detect state, and eight consecutive TS1 or TS2 Ordered Sets were received on any configured Lane prior to entry to this substate with speed_change bit set to 1b. When this bit is used, hardware must ensure that the start_equalization_w_preset variable are in the correct state to ensure that the components on both sides of the link are never out of sync.
6:4	0h RO	**Reserved (RSVD):** Reserved
3	0h RW	**Link EQ Phase 1 Transmit Coefficient Settling Policy (LEQP1TCSP):** Link EQ Phase 1 Transmit Coefficient Settling Policy(LEQP1TCSP): When operating in GEN3 data rate and there is a software/hardware request to re-perform Link Equalization through the Recovery.RcvrLock to Recovery.Equalization arc, PCIe spec requires that the downstream port transmitter switch to the setting specified by the Downstream Port Lane X Transmitter Preset registers in Phase 1. This switching is happening while the downstream port is still actively transmitting TS1 and the upstream port is only required to sample 2 TS1 to determine the next sub-state to transition to. Since the new coefficient setting can take up to 256 ns to settle, the 2 TS1 sampled by the upstream port may be incorrect causing the two LTSSM to be out of sync. When this bit is set, the RP will continue to send EIEOS until the local transmitter setting has settled (specified by PHYCTL2.TXCFGCHGWAIT) before sending TS1 as required in Recovery.Equalization Phase 1. When this bit is clear, the RP will send TS1 with EC = 01 in Recovery.Equalization Phase 1 even though the transmitter setting is still settling.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Multi-Fragment Linear and Nine-Tile List Enable (MFLNTL):** Multi-Fragment Linear and Nine-Tile List Enable(MFLNTL): When set in Hardware Autonomous Linear Preset/Coefficient Search mode, the full Preset/Coefficient List will be traversed in multiple fragments, where each fragments is done in separate entry to Recovery. This is used in the case where a longer dwelling time is required for a particular Preset/Coefficient (configured through EQCFG2.PCET). Subsequent Preset/Coefficient entries within the list that could not be covered within that Recovery session will be covered in subsequent re-entries into Recovery. When set in Hardware Autonomous Nine-Tiles Search mode, the 9-tiles list that could not be covered within that Recovery session will be covered in subsequent re-entries into Recovery.
1	1h RW	**Transmitter Use Preset Policy (TUPP):** Transmitter Use Preset Policy(TUPP): This field applies to the Link Equalization Phase where the local transmitter setting is being adjusted. When set, the transmitted TS1 Use Preset bit will be set if the remote device requests the local transmitter to apply specific Preset(instead of Coefficient). When clear, the Use Preset bit will not be set in this case. Note: This bit must be set before changing speed to GEN3 data rate.
0	0h RW	**Receiver Use Preset Policy (RUPP):** Receiver Use Preset Policy(RUPP): This field applies to the Link Equalization Phase where the remote transmitter setting is being adjusted. When set, the received TS1 Use Preset bit will be checked. When clear, the Use Preset bit in the received TS1 will be ignored. Note: This bit must be set before changing speed to GEN3 data rate.

17.4.85 Remote Transmitter Preset Coefficient List 1 (RTPCL1)—Offset 454h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Preset/Coefficient Mode (PCM):** Preset/Coefficient Mode (PCM): This bit defines whether the Preset List or Coefficient List should be sent to the remote TX to adjust the remote TX setting. For Downstream Port, this is used in Phase 3 of the Link Equalization. For Upstream Port, this is used in Phase 2 of the Link Equalization. The list of coefficient or preset is configurable through the Remote Transmitter Preset Coefficient List [lb]1:4[rb] registers. When this bit is set, Coefficient Mode is enabled and the Remote Transmitter Preset Coefficient List [lb]1:4[rb] registers contain the Coefficient List. When this bit is clear, Preset Mode is enabled and the Remote Transmitter Preset Coefficient List [lb]1:3[rb] registers contain the Preset List.
30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 2/Preset List 4 (RTPRECL2PL4):** Remote Transmitter Pre-Cursor Coefficient List 2/Preset List 4 (RTPRECL2PL4): For Downstream Port: This field defines the pre-cursor coefficient List 2 or Preset List 4 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 2 or Preset List 4 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Remote Transmitter Post-Cursor Coefficient List 1/Preset List 3 (RTPOSTCL1PL3):** Remote Transmitter Post-Cursor Coefficient List 1/Preset List 3 (RTPOSTCL1PL3): For Downstream Port: This field defines the post-cursor coefficient List 1 or Preset List 3 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 1 or Preset List 3 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
17:12	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 1/Preset List 2 (RTPRECL1PL2):** Remote Transmitter Pre-Cursor Coefficient List 1/Preset List 2 (RTPRECL1PL2): For Downstream Port: This field defines the pre-cursor coefficient List 1 or Preset List 2 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 1 or Preset List 2 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Remote Transmitter Post-Cursor Coefficient List 0/Preset List 1 (RTPOSTCL0PL1):** Remote Transmitter Post-Cursor Coefficient List 0/Preset List 1 (RTPOSTCL0PL1): For Downstream Port: This field defines the post-cursor coefficient List 0 or Preset List 1 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 0 or Preset List 1 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
5:0	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 0/Preset List 0 (RTPRECL0PL0):** Remote Transmitter Pre-Cursor Coefficient List 0/Preset List 0 (RTPRECL0PL0): For Downstream Port: This field defines the pre-cursor coefficient List 0 or Preset List 0 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 0 or Preset List 0 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.4.86 Remote Transmitter Preset Coefficient List 2 (RTPCL2)—Offset 458h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Remote Transmitter Post-Cursor Coefficient List 4/Preset List 9 (RTPOSTCL4PL9):** Remote Transmitter Post-Cursor Coefficient List 4/Preset List 9(RTPOSTCL4PL9): For Downstream Port: This field defines the post-cursor coefficient List 4 or Preset List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 4 or Preset List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 4/Preset List 8 (RTPRECL4PL8):** Remote Transmitter Pre-Cursor Coefficient List 4/Preset List 8 (RTPRECL4PL8): For Downstream Port: This field defines the pre-cursor coefficient List 4 or Preset List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 4 or Preset List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Post-Cursor Coefficient List 3/Preset List 7 (RTPOSTCL3PL7):** Remote Transmitter Post-Cursor Coefficient List 3/Preset List 7 (RTPOSTCL3PL7): For Downstream Port: This field defines the post-cursor coefficient List 3 or Preset List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 3 or Preset List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 3/Preset List 6 (RTPRECL3PL6):** Remote Transmitter Pre-Cursor Coefficient List 3/Preset List 6 (RTPRECL3PL6): For Downstream Port: This field defines the pre-cursor coefficient List 3 or Preset List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 3 or Preset List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Post-Cursor Coefficient List 2/Preset List 5 (RTPOSTCL2PL5):** Remote Transmitter Post-Cursor Coefficient List 2/Preset List 5 (RTPOSTCL2PL5): For Downstream Port: This field defines the post-cursor coefficient List 2 or Preset List 5 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 2 or Preset List 5 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.4.87 Remote Transmitter Preset Coefficient List 3 (RTPCL3)—Offset 45Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 7 (RTPRECL7):** Remote Transmitter Pre-Cursor Coefficient List 7 (RTPRECL7): For Downstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Post-Cursor Coefficient List 6 (RTPOSTCL6):** Remote Transmitter Post-Cursor Coefficient List 6 (RTPOSTCL6): For Downstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 6 (RTPRECL6):** Remote Transmitter Pre-Cursor Coefficient List 6 (RTPRECL6): For Downstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Post-Cursor Coefficient List 5 (RTPOSTCL5):** Remote Transmitter Post-Cursor Coefficient List 5 (RTPOSTCL5): For Downstream Port: This field defines the pre-cursor coefficient List 5 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 5 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 5/Preset List 10 (RTPRECL5PL10):** Remote Transmitter Pre-Cursor Coefficient List 5/Preset List 10 (RTPRECL5PL10): For Downstream Port: This field defines the pre-cursor coefficient List 5 or Preset List 10 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 5 or Preset List 10 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.4.88 Remote Transmitter Preset Coefficient List 4 (RTPCL4)—Offset 460h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Remote Transmitter Post-Cursor Coefficient List 9 (RTPOSTCL9):** Remote Transmitter Post-Cursor Coefficient List 9 (RTPOSTCL9): For Downstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 9 (RTPRECL9):** Remote Transmitter Pre-Cursor Coefficient List 9 (RTPRECL9): For Downstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Post-Cursor Coefficient List 8 (RTPOSTCL8):** Remote Transmitter Post-Cursor Coefficient List 8 (RTPOSTCL8): For Downstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 8 (RTPRECL8):** Remote Transmitter Pre-Cursor Coefficient List 8 (RTPRECL8): For Downstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Post-Cursor Coefficient List 7 (RTPOSTCL7):** Remote Transmitter Post-Cursor Coefficient List 7 (RTPOSTCL7): For Downstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.4.89 Figure Of Merit Status (FOMS)—Offset 464h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved
30:29	0h RW	**Index (I):** Index (I): The FOMV field will reflect the Figure of Merit Scoreboard value for the index specified by this field. List N below refers to the Figure of Merit values captured in the scoreboard corresponding to the Preset or Coefficient List N. 00b: Index 0 =[gt] {List 2, List 1, List 0}. 01b: Index 1 =[gt] {List 5, List 4, List 3}. 10b: Index 2 =[gt] {List 8, List 7, List 6}. 11b: Index 3 =[gt] {Rsvd, List 10, List 9}.

Bit Range	Default & Access	Field Name (ID): Description
28:24	0h RW	**Lane Number (LN):** Lane Number (LN): The FOMV field will reflect the Figure of Merit Scoreboard value for the lane specified by this field. 00000b: Lane 0. 00001b: Lane 1. 00010b: Lane 2. 00011b: Lane 3. Others: Reserved.
23:0	0h RO/V	**Figure of Merit Scoreboard Value (FOMSV):** Figure of Merit Scoreboard Value (FOMSV): This field will reflect the Figure of Merit Scoreboard entries referenced by the Lane Number and Index field in this register. For example, when Index == 00b, this field will reflect the Figure of Merit values for Lane specified in Lane Number field and the encoding of this field is as shown below: 23:16: Figure of Merit for Preset/Coefficient List 2. 15:8 : Figure of Merit for Preset/Coefficient List 1. 7:0 : Figure of Merit for Preset/Coefficient List 0. If the Receiver Eye Width margining completes with error, the value of Figure of Merit should reflect 0x00.

17.4.90 Hardware Autonomous Equalization Control (HAEQ)—Offset 468h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: A0080E00h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Ah RW	**Hardware Autonomous Preset/Coefficient Count Per-Iteration (HAPCCPI):** Hardware Autonomous Preset/Coefficient Count Per-Iteration(HAPCCPI): This field defines the number of Preset/Coefficient to be traversed for every iteration of Recovery Equalization. For the Linear Mode, EQCFG2.HAPCSB specifies the total number of Presets/Coefficients to be checked in total while this field specifies the number of Presets/Coefficients to be checked per-iteration of Recovery Equalization. Hardware will enter Recovery Equalization and check the number of Presets/Coefficients specified by this field. Once that is done, hardware will exit Recovery Equalization and trigger another entry to Recovery Equalization to check another set of Presets/Coefficients. This goes on until the total number of Presets/Coefficients are checked. For Nine-Tiles Mode, EQCFG2.NTIC specifies the number of 9-tiles iterations, which indirectly specifies the total number of Presets/ Coefficients to be checked in total. Similar to Linear Mode, this field specifies the number of Presets/Coefficients to be checked per-iteration of Recovery Equalization. 0h: 1 Preset/Coefficient per-iteration. 1h: 2 Preset/Coefficient per-iteration. 2h: 3 Preset/Coefficient per-iteration. ... 9h: 10 Preset/Coefficient per-iteration. Ah: 11 Preset/Coefficient per-iteration. Others: Reserved.
27:20	0h RW	**FOM Error Mask (FOMEM):** FOM Error Mask(FOMEM): The FOM error counter will be masked(thus ignoring the FOM error) for all the FOM values prior to the FOM value specified in this field. If this field is programmed to 00h, this mechanism is disabled. This bit must be configured before training to GEN3 data rate.

Bit Range	Default & Access	Field Name (ID): Description
19	1h RW	**MAC FOM Control (MACFOMC):** MAC FOM Control(MACFOMC): When set, MAC controls the advancement of the FOM values completely while in the Link Equalization mode. For downstream port, this is done in Phase 3 and for upstream port, this is done in Phase 2 of the Link Equalization. The dwelling time for each of the FOM values are programmed through the remaining fields of this register. When enabled, the hardware will start in Speeding Mode, where it will instruct the PHY to increment the FOM value after the Speeding Latency specified by HAEQ.SL field. Once the FOM value matches HAEQ.SFOMFM, the hardware switches from Speeding Mode to Dwelling Mode. In Dwelling mode, the MAC will instruct PHY to increment the FOM value after the Dwelling Latency specified by HAEQ.DL field. This is done until the link equalization phase is completed. When cleared, PHY controls the advancement of the FOM values completely, during the Link Equalization mode. This bit must be configured before training to GEN3 data rate.
18:16	0h RW	**Speeding Latency (SL):** Speeding Latency(SL): Specifies the residency time for a particular FOM value in Speeding Mode. 000b: 192 ns. 001b: 256 ns. 010b: 512 ns. 011b: 1 us. 100b: 2 us. 101b: 4 us. 110b: 8 us. 111b: 16 us. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.
15:8	Eh RW	**Dwelling Latency (DL):** Dwelling Latency(DL): Specifies the residency time for a particular FOM value in Dwelling Mode. 00h: 2 us. 01h: 4 us. 02h: 6 us. ... FFh: 512 us. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Starting FOM For Margining (SFOMFM):** Starting FOM For Margining(SFOMFM): Define the FOM where MAC switches from Speeding Mode to Dwelling Mode after hitting the programmed FOM value in Hardware Autonomous Preset/Coefficient mode. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.

17.4.91 Local Transmitter Coefficient Override 1 (LTCO1)—Offset 470h

Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane bits are not used.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD):** Reserved
25	0h RW	**Lane 1 Transmitter Coefficient Override Enable (L1TCOE):** Lane 1 Transmitter Coefficient Override Enable (L1TCOE): When set, the transmitter coefficient override values LTPCO1.L1TPRECO and LTPCO1.L1TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO1.L1TPRECO and LTPCO1.L1TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Lane 0 Transmitter Coefficient Override Enable (L0TCOE):** Lane 0 Transmitter Coefficient Override Enable (L0TCOE): When set, the transmitter coefficient override values LTPCO1.L0TPRECO and LTPCO1.L0TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO1.L0TPRECO and LTPCO1.L0TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
23:18	0h RW	**Lane 1 Transmitter Post-Cursor Coefficient Override (L1TPOSTCO):** Lane 1 Transmitter Post-Cursor Coefficient Override (L1TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L1TCOE = 1.
17:12	0h RW	**Lane 1 Transmitter Pre-Cursor Coefficient Override (L1TPRECO):** Lane 1 Transmitter Pre-Cursor Coefficient Override (L1TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L1TCOE = 1.
11:6	0h RW	**Lane 0 Transmitter Post-Cursor Coefficient Override (L0TPOSTCO):** Lane 0 Transmitter Post-Cursor Coefficient Override (L0TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L0TCOE = 1.
5:0	0h RW	**Lane 0 Transmitter Pre-Cursor Coefficient Override (L0TPRECO):** Lane 0 Transmitter Pre-Cursor Coefficient Override (L0TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L0TCOE = 1.

17.4.92 Local Transmitter Coefficient Override 2 (LTCO2)—Offset 474h

Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane bits are not used.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD):** Reserved
25	0h RW	**Lane 3 Transmitter Coefficient Override Enable (L3TCOE):** Lane 3 Transmitter Coefficient Override Enable (L3TCOE): When set, the transmitter coefficient override values LTPCO2.L3TPRECO and LTPCO2.L3TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO2.L3TPRECO and LTPCO2.L3TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
24	0h RW	**Lane 2 Transmitter Coefficient Override Enable (L2TCOE):** Lane 2 Transmitter Coefficient Override Enable (L2TCOE): When set, the transmitter coefficient override values LTPCO2.L2TPRECO and LTPCO2.L2TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO2.L2TPRECO and LTPCO2.L2TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Lane 3 Transmitter Post-Cursor Coefficient Override (L3TPOSTCO):** Lane 3 Transmitter Post-Cursor Coefficient Override (L3TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L3TCOE = 1.
17:12	0h RW	**Lane 3 Transmitter Pre-Cursor Coefficient Override (L3TPRECO):** Lane 3 Transmitter Pre-Cursor Coefficient Override (L3TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L3TCOE = 1
11:6	0h RW	**Lane 2 Transmitter Post-Cursor Coefficient Override (L2TPOSTCO):** Lane 2 Transmitter Post-Cursor Coefficient Override (L2TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L2TCOE = 1.
5:0	0h RW	**Lane 2 Transmitter Pre-Cursor Coefficient Override (L2TPRECO):** Lane 2 Transmitter Pre-Cursor Coefficient Override (L2TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L2TCOE = 1.

17.4.93 GEN3 L0s Control (G3L0SCTL)—Offset 478h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: C00281Eh

Bit Range	Default & Access	Field Name (ID): Description
31:24	Ch RW	**Gen3 Active State L0s Preparation Latency (G3ASL0SPL):** Gen3 Active State L0s Preparation Latency (G3ASL0SPL) Determines how long the Link layer has to indicate IDLE before the link initialization and control logic enters L0s 00: 0 clocks (enter immediately) 01: 1 clock ... FF: 255 clocks The value of this register is only used if the Gen3 L0s Entry Idle Control register is set to [quote]11[/quote] and operating in Gen3 mode.
23:22	0h RW	**Gen3 L0s Entry Idle Control (G3L0SIC):** Gen3 L0s Entry Idle Control (G3L0SIC): 00 : Allow entry into L0s after the link has been idle for a period of time equal to of the received N_FTS total entry time (1/4 * N_FTS * 16) 01 : Allow entry into L0s after the link has been idle for for a period of time equal to of the received N_FTS total entry time (1/2 * N_FTS * 16) 10 : Allow entry after the link has been idle for for a period of time equal to the received N_FTS total entry time (N_FTS * 16) 11: Allow entry into L0s after the link has been idle for a period specified in the Gen3 Active State L0s Preparation Latency register. This register is only applied when operating in Gen3 mode.
21:16	0h RO	**Reserved (RSVD):** Reserved
15:8	28h RW	**Gen3 Unique Clock N_FTS (G3UCNFTS):** Gen3 Unique Clock N_FTS (G3UCNFTS): Number of Fast Training Sequence ordered sets required to be transmitted for a root port Receiver to exit L0s in a unique (non-common) clock configuration (LCTL.CCC=0) when operating in Gen3 mode. The N_FTS value is sent in TS1 and TS2 training sets during link training. 00: 0 FTS sets 01: 1 FTS set ... FF: 255 FTS sets Note: When operating in Mobile Express mode, the output of this field is not used to determine the number of FTS to be sent on TXL0s exit. Mobile Express does not support Fast Training Sequence. Instead, SYNC is used to achieve bit lock. However, the output of this field is still used in L0s Entry Idle Control registers to determine the L0s Entry Idle latency.

Bit Range	Default & Access	Field Name (ID): Description
7:0	1Eh RW	**Gen3 Common Clock N_FTS (G3CCNFTS):** Gen3 Common Clock N_FTS (G3CCNFTS): Number of Fast Training Sequence ordered sets required to be transmitted for a root port Receiver to exit L0s in a common clock configuration (LCTL.CCC=1) when operating in Gen3 mode. The N_FTS value is sent in TS1 and TS2 training sets during link training. 00: 0 FTS sets 01: 1 FTS set ... FF: 255 FTS sets Note: When operating in Mobile Express mode, the output of this field is not used to determine the number of FTS to be sent on TXL0s exit. Mobile Express does not support Fast Training Sequence. Instead, SYNC is used to achieve bit lock. However, the output of this field is still used in L0s Entry Idle Control registers to determine the L0s Entry Idle latency.

17.4.94 Equalization Configuration 2 (EQCFG2)—Offset 47Ch

Size:32 bits
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: A001h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Nine-Tiles Iteration Count (NTIC):** Nine-Tiles Iteration Count(NTIC): This field specifies the number of iterations to perform the 9-tiles search. Each iteration involves evaluating the neighboring 9-tiles for the best Preset/Coefficient margin and then use the Preset/Coefficient as the centerpoint to identify and evaluate the next 9-tiles. 00h: 1 iteration. 01h: 2 iterations. 02h: 3 iterations. ... FFh: 256 iterations.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**Equalization Margining Disable (EMD):** Equalization Margining Disable(EMD):When set, the Root Port will not request the PHY to perform Receiver Margining by asserting RxEqEval on each Preset/ Coefficient list traversed. This allows the receiver to still measure the Bit Error Count without margining. When cleared, the Root Port will request the PHY to perform Receiver Margining by asserting RxEqEval. This field is only valid when operating in Hardware Autonomous Preset/Coefficient Search mode. The Preset/Coefficient list will still be traversed to the end.
22:20	0h RW	**Nine-Tiles Step Size (NTSS):** Nine-Tiles Step Size(NTSS): This field specifies the step size used to identify the surrounding 9-tiles to be used for margining. 000b: 1 step. 001b: 2 steps. 010b: 3 steps. 011b: 4 steps. 100b: 5 steps. 101b: 6 steps. 110b: 7 steps. 111b: 8 steps. Each of the steps is measured in terms of incrementing of decrementing the coefficient values.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW	**Preset/Coefficient Evaluation Timeout (PCET):** Preset/ Coefficient Evaluation Timeout(PCET): This field specifies the evaluation timeout for a single Preset/Coefficient in the List when operating in Hardware Autonomous Preset/Coefficient Search mode. By spec, the evaluation phase must be completed before the 24 ms timeout. To support 12 Presets (11 Presets + 1 final good Preset), each Preset will have up to 2 ms for evaluation. This field allows the 2 ms timer to be programmable. This is useful if the EQCFG2.HAPCSB limits the Preset/Coefficient List to smaller than 12 such that each Preset/Coefficient could be evaluated for a time longer than 2 ms. 0h: 2 ms. 1h: 2.5 ms. 2h: 3 ms. 3h: 3.5 ms. 4h: 4 ms. 5h: 4.5 ms. 6h: 5 ms. 7h: 6 ms. 8h: 7 ms. 9h: 8 ms. Ah: 9 ms. Bh:10 ms. Ch:11 ms. Dh:21 ms. Eh:22 ms. Fh:23 ms.
15:12	Ah RW	**Hardware Autonomous Preset/Coefficient Search Bound (HAPCSB):** Hardware Autonomous Preset/Coefficient Search Bound(HAPCSB): This field defines the number of Preset/ Coefficient List to be traversed, out of 11 for Presets or out of 10 for Coefficients. The Preset/Coefficient list will be traversed from List 0 to the value specified by this field in incremental order. This field allows equalization to be done with smaller set of Preset/ Coefficient list and each of the Preset/Coefficient list could be run for a longer time. 0h: Preset/Coefficient List 0 only. 1h: Preset/Coefficient List 0 - 1. 2h: Preset/Coefficient List 0 - 2. : : 9h: Preset/Coefficient List 0 - 9. Ah: Preset List 0 - 10/Coefficient List 0-9. Others: Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Nine-Tiles Equalization Mechanism Enable (NTEME):** Nine-Tiles Equalization Mechanism Enable(NTEME): When set, the Nine-Tiles Equalization Mechanism is enabled when running in Hardware Autonomous Preset/Coefficient Search Mode.
10	0h RW	**Mid-Point Equalization Mechanism Enable (MPEME):** Mid-Point Equalization Mechanism Enable(MPEME): When set, the Mid-Point Equalization Mechanism is enabled when running in Hardware Autonomous Preset/Coefficient Search Mode.
9:8	0h RW	**Receiver Eye Width Margin Error Threshold Multiplier (REWMETM):** Receiver Eye Width Margin Error Threshold Multiplier (REWMETM): This field specifies the multiplier to be used with REWMET field. 00b: Multiply REWMET by 1 (effectively no multiplier). 01b: Multiply REWMET by 10. 10b: Multiply REWMET by 100. 11b: Multiply REWMET by 1000.
7:0	1h RW	**Receiver Eye Width Margin Error Threshold (REWMET):** Receiver Eye Width Margin Error Threshold (REWMET): This field specifies the count threshold which upon exceeded, will cause controller to terminate the current iteration of Receiver Eye Width Margining and move on to the next preset or coefficient in the list. The value specified in this field will need to be multiplied with the multiplier specified in REWMETM field to get the final threshold values. 00h: Terminate on 1 x REWMETM errors. 01h: Terminate on 2 x REWMETM errors. 02h: Terminate on 4 x REWMETM errors. 03h: Terminate on 6 x REWMETM errors. : : FEh: Terminate on 508 x REWMETM errors. FFh: Never terminate. Rely on PHY to terminate the margining.

17.4.95 Monitor Mux (MM)—Offset 480h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO/V	**Monitor Signal State (MSST):** Monitor Signal State(MSST): The internal signal groupings selected by MM.MSS field is reflected in this field. The intention of this monitor signal is provide software a capability to monitor some of the GEN3 related parameters accumulated by the controller through the Link Equalization that are too costly to be mapped to dedicated registers. Implementation MUST NEVER expose any security related information through this Monitor Mux.
7:0	0h RW	**Monitor Signal Select (MSS):** Monitor Signal Select(MSS): This field is essentially the mux select for the Monitor Signal mux. Setting this field allows different monitor signals to be muxed out and readable by software through the MM.MSST field.

17.4.96 Lane0 P0 and P1 Preset-Coefficient Mapping (L0P0P1PCM)—Offset 500h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.97 Lane0 P1, P2 and P3 Preset-Coefficient Mapping (L0P1P2P3PCM)—Offset 504h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.98 Lane0 P3 and P4 Preset-Coefficient Mapping (L0P3P4PCM)—Offset 508h

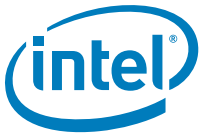
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.99 Lane0 P5 and P6 Preset-Coefficient Mapping (L0P5P6PCM)—Offset 50Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.100 Lane0 P6, P7 and P8 Preset-Coefficient Mapping (L0P6P7P8PCM)—Offset 510h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.101 Lane0 P8 and P9 Preset-Coefficient Mapping (L0P8P9PCM)—Offset 514h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

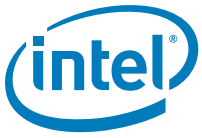
Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.102 Lane0 P10 Preset-Coefficient Mapping (L0P10PCM)—Offset 518h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.



Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.103 Lane0 LF and FS (L0LFFS)—Offset 51Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.104 Lane1 P0 and P1 Preset-Coefficient Mapping (L1P0P1PCM)—Offset 520h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.105 Lane1 P1, P2 and P3 Preset-Coefficient Mapping (L1P1P2P3PCM)—Offset 524h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.106 Lane1 P3 and P4 Preset-Coefficient Mapping (L1P3P4PCM)—Offset 528h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.107 Lane1 P5 and P6 Preset-Coefficient Mapping (L1P5P6PCM)—Offset 52Ch

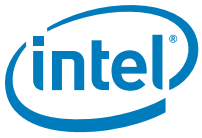
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



17.4.108 Lane1 P6, P7 and P8 Preset-Coefficient Mapping (L1P6P7P8PCM)—Offset 530h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.109 Lane1 P8 and P9 Preset-Coefficient Mapping (L1P8P9PCM)—Offset 534h

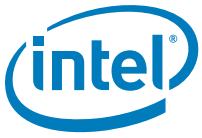
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.110 Lane1 P10 Preset-Coefficient Mapping (L1P10PCM)—Offset 538h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.111 Lane1 LF and FS (L1LFFS)—Offset 53Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.112 Lane2 P0 and P1 Preset-Coefficient Mapping (L2P0P1PCM)—Offset 540h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.113 Lane2 P1, P2 and P3 Preset-Coefficient Mapping (L2P1P2P3PCM)—Offset 544h

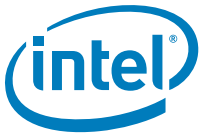
This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.114 Lane2 P3 and P4 Preset-Coefficient Mapping (L2P3P4PCM)—Offset 548h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.115 Lane2 P5 and P6 Preset-Coefficient Mapping (L2P5P6PCM)—Offset 54Ch

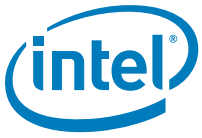
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.116 Lane2 P6, P7 and P8 Preset-Coefficient Mapping (L2P6P7P8PCM)—Offset 550h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.117 Lane2 P8 and P9 Preset-Coefficient Mapping (L2P8P9PCM)—Offset 554h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.118 Lane2 P10 Preset-Coefficient Mapping (L2P10PCM)—Offset 558h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.119 Lane2 LF and FS (L2LFFS)—Offset 55Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.120 Lane3 P0 and P1 Preset-Coefficient Mapping (L3P0P1PCM)—Offset 560h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.121 Lane3 P1, P2 and P3 Preset-Coefficient Mapping (L3P1P2P3PCM)—Offset 564h

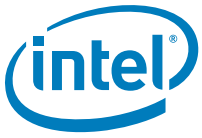
This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.122 Lane3 P3 and P4 Preset-Coefficient Mapping (L3P3P4PCM)—Offset 568h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.123 Lane3 P5 and P6 Preset-Coefficient Mapping (L3P5P6PCM)—Offset 56Ch

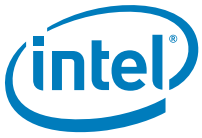
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.124 Lane3 P6, P7 and P8 Preset-Coefficient Mapping (L3P6P7P8PCM)—Offset 570h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.125 Lane3 P8 and P9 Preset-Coefficient Mapping (L3P8P9PCM)—Offset 574h

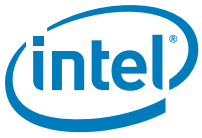
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.126 Lane3 P10 Preset-Coefficient Mapping (L3P10PCM)—Offset 578h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.4.127 Lane3 LF and FS (L3LFFS)—Offset 57Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5 Registers Summary

Table 17-5. Summary of pcie_cfg Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4h	7h	Device Command; Primary Status (CMD_PSTS)—Offset 4h	100000h
8h	Bh	Revision ID;Class Code (RID_CC)—Offset 8h	60400F0h
Ch	Fh	Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch	810000h
18h	1Bh	Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h	0h
1Ch	1Fh	I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch	0h
20h	23h	Memory Base and Limit (MBL)—Offset 20h	0h
24h	27h	Prefetchable Memory Base and Limit (PMBL)—Offset 24h	10001h
28h	2Bh	Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h	0h
2Ch	2Fh	Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch	0h
34h	37h	Capabilities List Pointer (CAPP)—Offset 34h	40h
3Ch	3Fh	Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch	0h
40h	43h	Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h	428010h
44h	47h	Device Capabilities (DCAP)—Offset 44h	8001h
48h	4Bh	Device Control; Device Status (DCTL_DSTS)—Offset 48h	100000h
4Ch	4Fh	Link Capabilities (LCAP)—Offset 4Ch	710C00h
50h	53h	Link Control; Link Status (LCTL_LSTS)—Offset 50h	10000h
54h	57h	Slot Capabilities (SLCAP)—Offset 54h	40060h
58h	5Bh	Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h	0h
5Ch	5Fh	Root Control (RCTL)—Offset 5Ch	0h
60h	63h	Root Status (RSTS)—Offset 60h	0h
64h	67h	Device Capabilities 2 (DCAP2)—Offset 64h	80837h
68h	6Bh	Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h	0h
6Ch	6Fh	Link Capabilities 2 (LCAP2)—Offset 6Ch	0h
70h	73h	Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h	0h
74h	77h	Slot Capabilities 2 (SLCAP2)—Offset 74h	0h

Table 17-5. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
78h	7Bh	Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h	0h
80h	83h	Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h	9005h
88h	8Bh	Message Signaled Interrupt Message Data (MD)—Offset 88h	0h
90h	93h	Subsystem Vendor Capability (SVCAP)—Offset 90h	A00Dh
94h	97h	Subsystem Vendor IDs (SVID)—Offset 94h	0h
A0h	A3h	Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h	C8030001h
A4h	A7h	PCI Power Management Control And Status (PMCS)—Offset A4h	8h
D4h	D7h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	800h
E4h	E7h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	0h
100h	103h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	0h
104h	107h	Uncorrectable Error Status (UES)—Offset 104h	0h
108h	10Bh	Uncorrectable Error Mask (UEM)—Offset 108h	0h
10Ch	10Fh	Uncorrectable Error Severity (UEV)—Offset 10Ch	60011h
110h	113h	Correctable Error Status (CES)—Offset 110h	0h
114h	117h	Correctable Error Mask (CEM)—Offset 114h	2000h
118h	11Bh	Advanced Error Capabilities and Control (AECC)—Offset 118h	0h
11Ch	11Fh	Header Log DW1 (HL_DW1)—Offset 11Ch	0h
120h	123h	Header Log DW2 (HL_DW2)—Offset 120h	0h
124h	127h	Header Log DW3 (HL_DW3)—Offset 124h	0h
128h	12Bh	Header Log DW4 (HL_DW4)—Offset 128h	0h
12Ch	12Fh	Root Error Command (REC)—Offset 12Ch	0h
134h	137h	Error Source Identification (ESID)—Offset 134h	0h
140h	143h	ACS Extended Capability Header (ACSECH)—Offset 140h	0h
144h	147h	ACS Capability Register (ACSCAPR)—Offset 144h	Fh
148h	14Bh	ACS Control Register (ACSCTLR)—Offset 148h	0h
150h	153h	PTM Extended Capability Header (PTMECH)—Offset 150h	0h
154h	157h	PTM Capability Register (PTMCAPR)—Offset 154h	400h
158h	15Bh	PTM Control Register (PTMCTLR)—Offset 158h	0h
200h	203h	L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h	0h
204h	207h	L1 Sub-States Capabilities (L1SCAP)—Offset 204h	28281Fh
208h	20Bh	L1 Sub-States Control 1 (L1SCTL1)—Offset 208h	0h
20Ch	20Fh	L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch	28h
220h	223h	Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h	0h
224h	227h	Link Control 3 (LCTL3)—Offset 224h	0h
228h	22Bh	Lane Error Status (LES)—Offset 228h	0h
22Ch	22Fh	Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch	7F7F7F7Fh

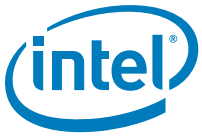


Table 17-5. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
230h	233h	Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h	7F7F7F7Fh
300h	303h	PCI Express Replay Timer Policy 1 (PCIERTP1)—Offset 300h	A64F96h
304h	307h	PCI Express Replay Timer Policy 2 (PCIERTP2)—Offset 304h	1BC00B86h
314h	317h	PCI Express Status 1 (PCIESTS1)—Offset 328h	54262A13h
328h	32Bh	PCI Express Status 1 (PCIESTS1)—Offset 328h	0h
32Ch	32Fh	PCI Express Status 2 (PCIESTS2)—Offset 32Ch	0h
330h	333h	PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h	2A000016h
334h	337h	PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h	4ABCB5BCh
390h	393h	PTM Propagation Delay (PTMPD)—Offset 390h	0h
394h	397h	PTM Lower Local Master Time (PTMLLMT)—Offset 394h	0h
398h	39Bh	PTM Upper Local Master Time (PTMULMT)—Offset 398h	0h
39Ch	39Fh	PTM Pipe Stage Delay Configuration 1 (PTMPSDC1)—Offset 39Ch	0h
3A0h	3A3h	PTM Pipe Stage Delay Configuration 2 (PTMPSDC2)—Offset 3A0h	0h
3A4h	3A7h	PTM Pipe Stage Delay Configuration 3 (PTMPSDC3)—Offset 3A4h	0h
3A8h	3ABh	PTM Pipe Stage Delay Configuration 4 (PTMPSDC4)—Offset 3A8h	0h
3ACh	3AFh	PTM Pipe Stage Delay Configuration 5 (PTMPSDC5)—Offset 3ACh	0h
3B0h	3B3h	PTM Extended Config (PTMECFG)—Offset 3B0h	0h
3B4h	3B7h	PTM Lower T2 Time Stamp (PTMLT2TSTMP)—Offset 3B4h	0h
3B8h	3BBh	PTM Upper T2 Time Stamp (PTMUT2TSTMP)—Offset 3B8h	0h
414h	417h	Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h	0h
418h	41Bh	Thermal and Power Throttling (TNPT)—Offset 418h	930h
41Ch	41Fh	Dynamic Lane Switch (DYNLNSW)—Offset 41Ch	0h
420h	423h	Power Control Enable (PCE)—Offset 428h	2AE8146h
428h	42Bh	Power Control Enable (PCE)—Offset 428h	9h
42Ch	42Fh	PGCB Control1 (PGCBCTL1)—Offset 42Ch	14155555h
430h	433h	PGCB Control2 (PGCBCTL2)—Offset 430h	54h
450h	453h	Equalization Configuration 1 (EQCFG1)—Offset 450h	3102h
454h	457h	Remote Transmitter Preset Coefficient List 1 (RTPCL1)—Offset 454h	0h
458h	45Bh	Remote Transmitter Preset Coefficient List 2 (RTPCL2)—Offset 458h	0h
45Ch	45Fh	Remote Transmitter Preset Coefficient List 3 (RTPCL3)—Offset 45Ch	0h
460h	463h	Remote Transmitter Preset Coefficient List 4 (RTPCL4)—Offset 460h	0h
464h	467h	Figure Of Merit Status (FOMS)—Offset 464h	0h
468h	46Bh	Hardware Autonomous Equalization Control (HAEQ)—Offset 468h	A0080E00h
470h	473h	Local Transmitter Coefficient Override 1 (LTCO1)—Offset 470h	0h
474h	477h	Local Transmitter Coefficient Override 2 (LTCO2)—Offset 474h	0h
478h	47Bh	GEN3 L0s Control (G3L0SCTL)—Offset 478h	C00281Eh
47Ch	47Fh	Equalization Configuration 2 (EQCFG2)—Offset 47Ch	A001h
480h	483h	Monitor Mux (MM)—Offset 480h	0h
500h	503h	Lane0 P0 and P1 Preset-Coefficient Mapping (L0P0P1PCM)—Offset 500h	0h

Table 17-5. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
504h	507h	Lane0 P1, P2 and P3 Preset-Coefficient Mapping (L0P1P2P3PCM)—Offset 504h	0h
508h	50Bh	Lane0 P3 and P4 Preset-Coefficient Mapping (L0P3P4PCM)—Offset 508h	0h
50Ch	50Fh	Lane0 P5 and P6 Preset-Coefficient Mapping (L0P5P6PCM)—Offset 50Ch	0h
510h	513h	Lane0 P6, P7 and P8 Preset-Coefficient Mapping (L0P6P7P8PCM)—Offset 510h	0h
514h	517h	Lane0 P8 and P9 Preset-Coefficient Mapping (L0P8P9PCM)—Offset 514h	0h
518h	51Bh	Lane0 P10 Preset-Coefficient Mapping (L0P10PCM)—Offset 518h	0h
51Ch	51Fh	Lane0 LF and FS (L0LFFS)—Offset 51Ch	0h
520h	523h	Lane1 P0 and P1 Preset-Coefficient Mapping (L1P0P1PCM)—Offset 520h	0h
524h	527h	Lane1 P1, P2 and P3 Preset-Coefficient Mapping (L1P1P2P3PCM)—Offset 524h	0h
528h	52Bh	Lane1 P3 and P4 Preset-Coefficient Mapping (L1P3P4PCM)—Offset 528h	0h
52Ch	52Fh	Lane1 P5 and P6 Preset-Coefficient Mapping (L1P5P6PCM)—Offset 52Ch	0h
530h	533h	Lane1 P6, P7 and P8 Preset-Coefficient Mapping (L1P6P7P8PCM)—Offset 530h	0h
534h	537h	Lane1 P8 and P9 Preset-Coefficient Mapping (L1P8P9PCM)—Offset 534h	0h
538h	53Bh	Lane1 P10 Preset-Coefficient Mapping (L1P10PCM)—Offset 538h	0h
53Ch	53Fh	Lane1 LF and FS (L1LFFS)—Offset 53Ch	0h
540h	543h	Lane2 P0 and P1 Preset-Coefficient Mapping (L2P0P1PCM)—Offset 540h	0h
544h	547h	Lane2 P1, P2 and P3 Preset-Coefficient Mapping (L2P1P2P3PCM)—Offset 544h	0h
548h	54Bh	Lane2 P3 and P4 Preset-Coefficient Mapping (L2P3P4PCM)—Offset 548h	0h
54Ch	54Fh	Lane2 P5 and P6 Preset-Coefficient Mapping (L2P5P6PCM)—Offset 54Ch	0h
550h	553h	Lane2 P6, P7 and P8 Preset-Coefficient Mapping (L2P6P7P8PCM)—Offset 550h	0h
554h	557h	Lane2 P8 and P9 Preset-Coefficient Mapping (L2P8P9PCM)—Offset 554h	0h
558h	55Bh	Lane2 P10 Preset-Coefficient Mapping (L2P10PCM)—Offset 558h	0h
55Ch	55Fh	Lane2 LF and FS (L2LFFS)—Offset 55Ch	0h
560h	563h	Lane3 P0 and P1 Preset-Coefficient Mapping (L3P0P1PCM)—Offset 560h	0h
564h	567h	Lane3 P1, P2 and P3 Preset-Coefficient Mapping (L3P1P2P3PCM)—Offset 564h	0h
568h	56Bh	Lane3 P3 and P4 Preset-Coefficient Mapping (L3P3P4PCM)—Offset 568h	0h
56Ch	56Fh	Lane3 P5 and P6 Preset-Coefficient Mapping (L3P5P6PCM)—Offset 56Ch	0h
570h	573h	Lane3 P6, P7 and P8 Preset-Coefficient Mapping (L3P6P7P8PCM)—Offset 570h	0h
574h	577h	Lane3 P8 and P9 Preset-Coefficient Mapping (L3P8P9PCM)—Offset 574h	0h
578h	57Bh	Lane3 P10 Preset-Coefficient Mapping (L3P10PCM)—Offset 578h	0h
57Ch	57Fh	Lane3 LF and FS (L3LFFS)—Offset 57Ch	0h

17.5.1 Device Command; Primary Status (CMD_PSTS)—Offset 4h

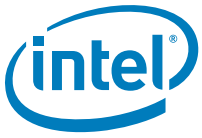
Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**DPE - Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if CMD.PERE is not set.
30	0h RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
26:25	0h RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved per PCI-Express spec
24	0h RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and CMD.PERE is set.
23	0h RO	**Primary Fast Back to Back Capable (PFBC):** Reserved per PCI-Express spec.
22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Primary 66 MHz Capable (PC66):** Reserved per PCI-Express spec.
20	1h RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list.
19	0h RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID.
18:16	0h RO	**Reserved (RSVD_1):** Reserved
15:11	0h RO	**Reserved (RSVD_2):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec.
8	0h RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0h RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec.
6	0h RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** Reserved per PCI-Express spec.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec.
3	0h RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec.
2	0h RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0h RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0h RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone..



17.5.2 Revision ID;Class Code (RID_CC)—Offset 8h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 60400F0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	6h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	4h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h.
15:8	0h RO/V	**Programming Interface (PI):** The value reported in this register is a function of the Decode Control.Subtractive Decode Enable (SDE) register. SDE Value reported in this register 0: 00h 1: 01h
7:0	F0h RO/V	**Revision ID (RID):** Indicates the revision of the bridge.

17.5.3 Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 810000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved
23	1h RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device.
22:16	1h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h.
15:11	0h RO	**Latency Count (CT):** Reserved per PCI-Express spec
10:8	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec

17.5.4 Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V2	**Secondary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	0h RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.
15:8	0h RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port.
7:0	0h RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

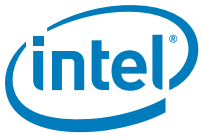
17.5.5 I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
30	0h RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with 'Unsupported Request' status from the device.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with 'Completion Abort' status from the device.



Bit Range	Default & Access	Field Name (ID): Description
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with 'Completion Abort' status to the device.
26:25	0h RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.
23	0h RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec
20:16	0h RO	**Reserved (RSVD_1):** Reserved
15:12	0h RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing.

17.5.6 Memory Base and Limit (MBL)—Offset 20h

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is MB [gt]= AD[lb]31:20[rb] [lt]= ML.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	0h RO	**Reserved (RSVD):** Reserved
15:4	0h RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	0h RO	**Reserved (RSVD_1):** Reserved

17.5.7 Prefetchable Memory Base and Limit (PMBL)—Offset 24h

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB [gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 10001h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing.
15:4	0h RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	1h RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing.

17.5.8 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.

17.5.9 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

17.5.10 Capabilities List Pointer (CAPP)—Offset 34h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 40h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	40h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) OffsetCapability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI) 90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List OffsetCapability Next Pointer 100h Advanced Error Reporting 000h

17.5.11 Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD):** Reserved
27	0h RW/V2	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
26	0h RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set.
25	0h RW/V2	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW/V2	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
23	0h RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec.
22	0h RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port.
21	0h RW/V2	**Master Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
20	0h RW	**VGA 16-Bit Decode (V16):** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.
19	0h RW	**VGA Enable (VE):** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h 3BBh and 3C0h 3DFh, and all aliases of bits 15:10 in any combination of 1's
18	0h RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
17	0h RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
16	0h RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG register in chipset config space: Port Bits[lb]15:12[rb] Bits[lb]11:08[rb] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP 4 0h STRPFUSECFG.P4IP 5 0h STRPFUSECFG.P5IP 6 0h STRPFUSECFG.P6IP 7 0h STRPFUSECFG.P7IP 8 0h STRPFUSECFG.P8IP The value that is programmed into STRPFUSECFG.PxIP is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above.
7:0	0h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

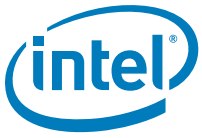
17.5.12 Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 428010h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved
30	0h RO	**Reserved (RSVD_1):** Reserved. This register at one time was for TCS Routing but that was later removed from the PCIe 2.0 spec
29:25	0h RO	**Interrupt Message Number (IMN):** The root port does not have multiple MSI interrupt numbers.
24	0h RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
23:20	4h RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port



Bit Range	Default & Access	Field Name (ID): Description
19:16	2h RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 specification which incorporates the Register Expansion ECN.
15:8	80h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h RO	**Capability ID (CID):** Indicates this is a PCI Express capability

17.5.13 Device Capabilities (DCAP)—Offset 44h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 8001h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD):** Reserved
28	0h RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports
27:26	0h RO	**Captured Slot Power Limit Scale (CSPS):** Not supported
25:18	0h RO	**Captured Slot Power Limit Value (CSPV):** Not supported
17:16	0h RO	**Reserved (RSVD_1):** Reserved
15	1h RO	**Role Based Error Reporting (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.
14	0h RO	**Reserved (RSVD_2):** Reserved. On previous version of the specification this was Power Indicator Present (PIP)
13	0h RO	**Reserved (RSVD_3):** Reserved. On previous version of the specification this was Attention Indicator Present (AIP)

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**Reserved (RSVD_4):** Reserved. On previous version of the specification this was Attention Button Present (ABP)
11:9	0h RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports.
8:6	0h RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port.
5	0h RO	**Extended Tag Field Supported (ETFS):** The root port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	0h RO	**Phantom Functions Supported (PFS):** No phantom functions supported
2:0	1h RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Only Max Payload Size of up to 256B is supported. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface.

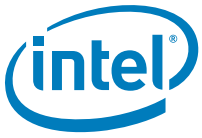
17.5.14 Device Control; Device Status (DCTL_DSTS)—Offset 48h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
20	1h RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup



Bit Range	Default & Access	Field Name (ID): Description
19	0h RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
18	0h RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp
17	0h RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout
16	0h RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout.
15	0h RO	**Reserved (RSVD_1):** Reserved
14:12	0h RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface.
11	0h RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.
10	0h RW/P	**Aux Power PM Enable (APME):** The OS will set this bit to '1' if the device connected has detected aux power.
9	0h RO	**Phantom Functions Enable (PFE):** Not supported
8	0h RO	**Extended Tag Field Enable (ETFE):** Not supported
7:5	0h RW	**Max Payload Size (MPS):** The root port only supports up to 256B max payload. Programming this field to any values other than 128B or 256B max payload size will result in aliasing to 128B max payload size. If the DCAP.MPS indicates 128B max payload size support, programming this field to any values other than 128B will result in aliasing to 128B max payload size. Programming this field to any values greater than DCAP.MPS will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME.
4	0h RO	**Enable Relaxed Ordering (ERO):** Not supported

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0h RW	**Fatal Error Reporting Enable (FEE):** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0h RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0h RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

17.5.15 Link Capabilities (LCAP)—Offset 4Ch

Access Method

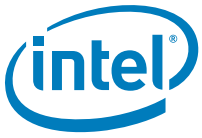
Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 710C00h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h
23	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
22	1h RW/O	**ASPM Optionality Compliance (ASPMOC):** ASPM Optionality Compliance(ASPMOC): This bit must be set to 1b for PCIe 3.0 compliant port. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests.
21	1h RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1h RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0h RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the root port does not support Surprise Down Error Reporting
18	0h RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism.
17:15	2h RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b Less than 1 us 001b 1 us to less than 2 us 010b 2 us to less than 4 us 011b 4 us to less than 8 us 100b 8 us to less than 16 us 101b 16 us to less than 32 us 110b 32 us to 64 us 111b More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency.
14:12	0h RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL

Bit Range	Default & Access	Field Name (ID): Description
11:10	3h RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 No ASPM Supported 01 L0s Supported 10 L1 Supported 11 L0s and L1 supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is '01'. Otherwise, the default of this field is '11'. If STRPFUSECFG.ASPMDIS is 1, BIOS writing '11' to this field will have the same effect as writing '01'. '01' will be reflected on this register when read and the register will turn to Read-Only once written once.
9:4	0h RO/V	**Maximum Link Width (MLW):** For the root ports, several values can be taken, based upon the value of the chipset configuration register field RPC.PC1 for ports 1-4: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h



Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RO/V	**Max Link Speeds (MLS):** Indicates the supported link speeds of the Root Port. 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5GT/s Link speeds supported This register reports a value of 0001b if the Root Port Gen2 Disable Fuse is set or the MPC.PCIEGEN2DIS bit is set, else this register reports a value of 0010b. Max Link Speeds (MLS): This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. This register reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through Fuse or MPC.PCIESD register. This register reports a value of 0010b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through Fuse or MPC.PCIESD register.

17.5.16 Link Control; Link Status (LCTL_LSTS)—Offset 50h

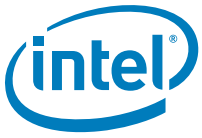
Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
29	0h RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.
28	0h RO/V	**Slot Clock Configuration (SCC):** In normal mode, root port uses the same reference clock as on the platform and does not generate its own clock. Note: The default of this register bit is dependent on the 'PCIe Non-Common Clock With SSC Mode Enable Strap'. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'.
27	0h RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
26	0h RO	**Reserved (RSVD):** Reserved. Previously this was defined as Link Training Error (LTE) but support for this bit was removed from subsequent versions of the PCI Express specification.
25:20	0h RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained.



Bit Range	Default & Access	Field Name (ID): Description
19:16	1h RO/V	**Current Link Speed (CLS):** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link This field indicates the negotiated Link speed of the given link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. The value of this field is undefined if the link is not up.
15:12	0h RO	**Reserved (RSVD_1):** Reserved
11	0h RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.
10	0h RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.
9	0h RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. Note: When operating as PCI Express, this bit defines the value of the Link Upconfigure Capability in TS2 Ordered Sets.
8	0h RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on Root Ports.
7	0h RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. Note: This functionality is not applicable for Mobile Express.
6	0h RW	**Common Clock Configuration (CCC):** When set, indicates that the root port and device are operating with a distributed common reference clock.

Bit Range	Default & Access	Field Name (ID): Description
5	0h WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0h RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state.
3	0h RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0h RO	**Reserved (RSVD_2):** Reserved
1:0	0h RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see '00' as an output from this register. BIOS reading this register should always return the correct value.

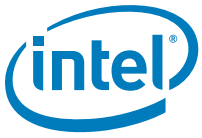
17.5.17 Slot Capabilities (SLCAP)—Offset 54h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 40060h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/O	**Physical Slot Number (PSN__31_24):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
23:19	0h RW/O	**Physical Slot Number (PSN__23_19):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.



Bit Range	Default & Access	Field Name (ID): Description
18	1h RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0h RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented.
16:15	0h RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:8	0h RW/O	**Slot Power Limit Value (SLV__14_8):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
7	0h RW/O	**Slot Power Limit Value (SLV__7_7):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1h RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported.
5	1h RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification.
4	0h RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot.
3	0h RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot.
2	0h RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present
1	0h RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot
0	0h RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot.

17.5.18 Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved (RSVD):** Reserved
24	0h RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
23	0h RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock.
22	0h RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'.
21	0h RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented.
20	0h RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller..
19	0h RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the SLSTS.PDS bit changes state.
18	0h RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented.
17	0h RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented.
16	0h RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button
15:13	0h RO	**Reserved (RSVD_1):** Reserved
12	0h RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed
11	0h RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock.
10	0h RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug.
9:8	0h RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller..
7:6	0h RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller..
5	0h RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0h RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller..

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state.
2	0h RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller..
1	0h RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller...
0	0h RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller..

17.5.19 Root Control (RCTL)—Offset 5Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:4	0h RO	**Reserved (RSVD_1):** Reserved
3	0h RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set).
2	0h RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0h RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0h RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

17.5.20 Root Status (RSTS)—Offset 60h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17	0h RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. Root ports have a one deep PME pending queue.
16	0h RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0h RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

17.5.21 Device Capabilities 2 (DCAP2)—Offset 64h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 80837h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved (RSVD):** Reserved
19:18	2h RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported.
17:12	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/ disable the root port from declaring support for the LTR capability.
10:6	0h RO	**Reserved (RSVD_2):** Reserved
5	1h RO	**ARI Forwarding Supported (AFS):** ARI Forwarding Supported (AFS): Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. Note: This bit is not made RWO to simplify implementation, since there is a requirement that the ARI Forwarding Enable bit must be hardwired to 0b if ARI Forwarding Supported bit is 0b. It is low risk to keep this risk 1b.
4	1h RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	7h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C 0111b Ranges A, B [amp] C [lt]-- This is what PCH supports 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved.

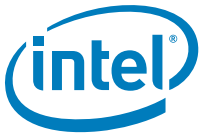
17.5.22 Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15	0h RO	**Reserved (RSVD_1):** Reserved
14:13	0h RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** 00b Disable OBFF mechanism. 01b Enable OBFF mechanism using Message signaling (Variation A). 10b Enable OBFF mechanism using Message signaling (Variation B). 11b Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect.
12:11	0h RO	**Reserved (RSVD_2):** Reserved
10	0h RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:6	0h RO	**Reserved (RSVD_3):** Reserved
5	0h RW	**ARI Forwarding Enable (AFE):** ARI Forwarding Enable (AFE): When set, the Downstream Port disables its traditional Device Number field being 0b enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port.
4	0h RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.



Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The root port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 us to 100 us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either when this value was changed or when each request was issued.

17.5.23 Link Capabilities 2 (LCAP2)—Offset 6Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved (RSVD):** Reserved
22:16	0h RO	**Lower SKP OS Reception Supported Speeds Vector (LSOSRSS):** Lower SKP OS Reception Supported Speeds Vector(LSOSRSS): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
15:9	0h RO	**Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV):** Lower SKP OS Generation Supported Speeds Vector(LSOSGSSV): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
8	0h RO	**Crosslink Supported (CS):** Crosslink Supported (CS): No support for Crosslink.
7:1	0h RO/V	**Supported Link Speeds Vector (SLSV):** Supported Link Speeds Vector (SLSV): This field indicates the supported Link speed of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. Bit definitions within this field are: Bit 0: 2.5 GT/s. Bit 1: 5.0 GT/s. Bit 2: 8.0 GT/s. Bits 6:3: Reserved. This register reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through Fuse or MPC.PCIESD register. This register reports a value of 0011b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through Fuse or MPC.PCIESD register.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**Reserved (RSVD_1):** Reserved

17.5.24 Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/1C/V/P	**Link Equalization Request (LER):** Link Equalization Request (LER): This bit is set by hardware to request the Link equalization process to be performed on the Link. Register Attribute: Dynamic.
20	0h RO/V/P	**Equalization Phase 3 Successful (EQP3S):** Equalization Phase 3 Successful (EQP3S): When set to 1, this bit indicates that Phase 3 of the Transmitter Equalization procedure has successfully completed.
19	0h RO/V/P	**Equalization Phase 2 Successful (EQP2S):** Equalization Phase 2 Successful (EQP2S): When set to 1, this bit indicates that Phase 2 of the Transmitter Equalization procedure has successfully completed.
18	0h RO/V/P	**Equalization Phase 1 Successful (EQP1S):** Equalization Phase 1 Successful (EQP1S): When set to 1, this bit indicates that Phase 1 of the Transmitter Equalization procedure has successfully completed.
17	0h RO/V/P	**Equalization Complete (EqC):** Equalization Complete (EC): When set to 1, this bit indicates that the Transmitter Equalization procedure has completed
16	0h RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/P	**Compliance Preset/De-emphasis (CD):** For 8.0 GT/s Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b -3.5 dB 0000b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. The default value of this field is 0000b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value.
11	0h RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only.
10	0h RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.

Bit Range	Default & Access	Field Name (ID): Description
9:7	0h RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0h RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5	0h RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value.
3:0	0h RW/V/P	**Target Link Speed (TLS):** Target Link Speed (TLS): This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. If a value is written to this field that does not correspond to a supported speed, as indicated by the Supported Link Speeds Vector, the result is undefined. The default value of this field is GEN1. Note: This register field could be used by REUT software to limit the link speed to 2.5 GT/s or 5 GT/s data rate.

17.5.25 Slot Capabilities 2 (SLCAP2)—Offset 74h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved (RSVD):** Reserved

17.5.26 Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:0	0h RO	**Reserved (RSVD_1):** Reserved

17.5.27 Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 9005h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved
23	0h RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
22:20	0h RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
19:17	0h RO	**Multiple Message Capable (MMC):** Only one message is required.
16	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.

Bit Range	Default & Access	Field Name (ID): Description
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	5h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

17.5.28 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction.

17.5.29 Subsystem Vendor Capability (SVCAP)—Offset 90h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: A00Dh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

17.5.30 Subsystem Vendor IDs (SVID)—Offset 94h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

17.5.31 Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: C8030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	19h RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Microsoft operating systems to enable PME# in devices connected behind this root port.
26	0h RO	**D2_Support (D2S):** The D2 state is not supported.
25	0h RO	**D1_Support (D1S):** The D1 state is not supported.
24:22	0h RO	**Aux_Current (AC):** Reports 0mA (self-powered), as use of this controller does not add to suspect well power consumption.
21	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
20	0h RO	**Reserved (RSVD):** Reserved
19	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
18:16	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	1h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

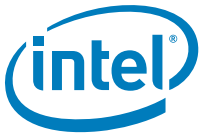
17.5.32 PCI Power Management Control And Status (PMCS)—Offset A4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Data (DTA):** Reserved
23	0h RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification
22	0h RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification.
21:16	0h RO	**Reserved (RSVD):** Reserved
15	0h RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.



Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0h RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Microsoft operating systems to enable PME# on devices connected to this root port.
7:4	0h RO	**Reserved (RSVD_1):** Reserved
3	1h RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved (RSVD_2):** Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 D0 state 11 D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

17.5.33 Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h

Size:32 bits
The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list.
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

17.5.34 Uncorrectable Error Status (UES)—Offset 104h

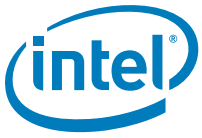
This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/1C/V/P	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0h RW/1C/V/P	**Completer Abort Status (CA):** Indicates a completer abort was received



Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Not supported.
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RO	**Training Error Status (TE):** Not supported.

17.5.35 Uncorrectable Error Mask (UEM)—Offset 108h

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/P	**ACS Violation Mask (AVM):** Reserved. Access Control Services are not supported
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0h RW/P	**Completor Abort Mask (CM):** Mask for completer abort.
14	0h RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.
13	0h RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RO	**Training Error Mask (TE):** Not supported.

17.5.36 Uncorrectable Error Severity (UEV)—Offset 10Ch

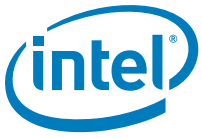
This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 60011h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/P	**ACS Violation Severity (AVS):** Severity for ACS violation.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	1h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.



Bit Range	Default & Access	Field Name (ID): Description
17	1h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0h RW/P	**Completer Abort Severity (CA):** Severity for completer abort.
14	0h RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	1h RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation..

17.5.37 Correctable Error Status (CES)—Offset 110h

This register is only reset by a loss of core power

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved (RSVD):** Reserved
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

17.5.38 Correctable Error Mask (CEM)—Offset 114h

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved (RSVD):** Reserved
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	**Reserved (RSVD_1):** Reserved
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.

Bit Range	Default & Access	Field Name (ID): Description
5:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

17.5.39 Advanced Error Capabilities and Control (AECC)—Offset 118h

This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved (RSVD):** Reserved
8	0h RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0h RO	**ECRC Check Capable (ECC):** ECRC is not supported.
6	0h RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0h RO	**ECRC Generation Capabile (EGC):** ECRC is not supported.
4:0	0h RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

17.5.40 Header Log DW1 (HL_DW1)—Offset 11Ch

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**1st dWord of TLP (DW1):** Byte0 [amp][amp] Byte1 [amp][amp] Byte2 [amp][amp] Byte3

17.5.41 Header Log DW2 (HL_DW2)—Offset 120h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**2nd dWord of TLP (DW2):** Byte4 [amp][amp] Byte5 [amp][amp] Byte6 [amp][amp] Byte7

17.5.42 Header Log DW3 (HL_DW3)—Offset 124h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**3rd dWord of TLP (DW3):** Byte8 [amp][amp] Byte9 [amp][amp] Byte10 [amp][amp] Byte11

17.5.43 Header Log DW4 (HL_DW4)—Offset 128h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**4th dWord of TLP (DW4):** Byte12 [amp][amp] Byte13 [amp][amp] Byte14 [amp][amp] Byte15

17.5.44 Root Error Command (REC)—Offset 12Ch

This register allows errors to generate interrupts.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved (RSVD):** Reserved
2	0h RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0h RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0h RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

17.5.45 Error Source Identification (ESID)—Offset 134h

Size:32 bits
Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set.
15:0	0h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set.

17.5.46 ACS Extended Capability Header (ACSECH)—Offset 140h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support ACS Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support ACS Extended Capability, BIOS should write a 000Dh to this register else it should write 0.

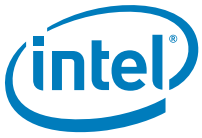
17.5.47 ACS Capability Register (ACSCAPR)—Offset 144h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: Fh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD_1):** Reserved for Egress Control Vector Size. This field is not applicable since ACS P2P Egress Control is not supported.
7	0h RO	**Reserved (RSVD_2):** Reserved
6	0h RO	**ACS Direct Translated P2P (T):** ACS Direct Translated P2P (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control (E):** ACS P2P Egress Control (E): ACS P2P Egress Control is not supported.
4	0h RO	**ACS Upstream Forwarding (U):** ACS Upstream Forwarding (U): ACS Upstream Forwarding is not supported.
3	1h RW/O	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Required for all Functions that support ACS P2P Request Redirect; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Completion Redirect.
2	1h RW/O	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Required for Root Ports that support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports; required for multi-function device Functions that support peer-to-peer traffic with other Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Request Redirect.
1	1h RW/O	**ACS Translation Blocking (B):** ACS Translation Blocking (B): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Translation Blocking.
0	1h RW/O	**ACS Source Validation (V):** ACS Source Validation (V): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Source Validation.

17.5.48 ACS Control Register (ACSCTLR)—Offset 148h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RSVD):** Reserved,
6	0h RO	**ACS Direct Translated P2P Enable (T):** ACS Direct Translated P2P Enable (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control Enable (E):** ACS P2P Egress Control Enable (E): ACS P2P Egress Control is not supported.
4	0h RO	**ACS Upstream Forwarding Enable (U):** ACS Upstream Forwarding Enable (U): ACS Upstream Forwarding is not supported.
3	0h RW	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Determines when the component redirects peer-to-peer Completions upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear.
2	0h RW	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Determines when the component redirects peer-to-peer memory Requests targeting another peer port upstream. I/O, Configuration, VDM Messages and Completions are never affected by ACS P2P Request Redirect.
1	0h RW	**ACS Translation Blocking (B):** ACS Translation Blocking (B): When set, the component blocks all upstream Memory Requests whose Address Translation (AT) field is not set to the default value. I/O, Configuration, Completions and Messages are never affected by ACS Translation Blocking.
0	0h RW	**ACS Source Validation (V):** ACS Source Validation (V): When set, the component validates the Bus Number from the Requester ID of upstream Requests against the secondary / subordinate Bus Numbers. I/O, Configuration and Completions are never affected by ACS Source Validation.

17.5.49 PTM Extended Capability Header (PTMECH)—Offset 150h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support PTM Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support PTM Extended Capability, BIOS should write a 001Fh to this register else it should write 0.

17.5.50 PTM Capability Register (PTMCAPR)—Offset 154h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 400h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved,
15:8	4h RW/O	**Local Clock Granularity (LCG):** Local Clock Granularity (LCG): 0000 0000b - Time Source does not implement a local clock. It simply propagates timing information obtained from further Upstream in the PTM Hierarchy when responding to PTM Request messages. 0000 0001b - 1111 1110b: Indicates the period of this Time Sources local clock in ns. 1111 1111b: Indicates the period of this Time Sources local clock is greater than 254 ns. If the PTM Root Select bit is Set, this local clock is used to provide PTM Master Time. Otherwise, the Time Source uses this local clock to locally track PTM Master Time received from further Upstream within a PTM Hierarchy.
7:3	0h RO	**Reserved (RSVD_1):** Reserved,
2	0h RW/O	**PTM Root Capable (PTMRC):** PTM Root Capable(PTMRC): Root Ports must set this bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW/O	**PTM Responder Capable (PTMRSPC):** PTM Responder Capable(PTMRSPC): Root Ports are permitted to set this bit to 1b to indicate that they implement the PTM Responder role.
0	0h RO	**PTM Requester Capable (PTMREQC):** PTM Requester Capable(PTMREQC): PTM Requester Role is not supported by Root Port.

17.5.51 PTM Control Register (PTMCTLR)—Offset 158h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:8	0h RO	**Effective Granularity (EG):** Effective Granularity(EG): Root Port does not support PTM Requester role.
7:2	0h RO	**Reserved (RSVD_1):** Reserved.
1	0h RW	**Root Select (RS):** Root Select(RS): When Set, if the PTM Enable bit is also Set, this Time Source is the PTM Root. Within each PTM Hierarchy, it is recommended that system software select only the furthest Upstream Time Source to be the PTM Root.
0	0h RW	**PTM Enable (PTME):** PTM Enable(PTME): When Set, this Function is permitted to participate in the PTM mechanism according to its selected role. Software must not have the PTM Enable bit Set in the PTM Control register on a Function associated with an Upstream Port unless the associated Downstream Port on the Link already has the PTM Enable bit Set in its associated PTM Control register. Register Attribute: Static.

17.5.52 L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h

Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 1h
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 001Eh. .

17.5.53 L1 Sub-States Capabilities (L1SCAP)—Offset 204h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 28281Fh

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
23:19	5h RW/O	**Port Tpower_on Value (PTV):** Along with the Port T_POWER_ON Scale Field in the L1 Substates Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF.
18	0h RO	**Reserved (RSVD_1):** Reserved.
17:16	0h RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Substates Capabilities register. '00b': 2 us '01b': 10 us '10b': 100 us '11b': Reserved Required for all Ports that support L1.OFF.
15:8	28h RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF.
7:5	0h RO	**Reserved (RSVD_2):** Reserved
4	1h RW/O	**L1 PM Substates Supported (L1PSS):** When Set this bit indicates that this Port supports L1 PM Substates. For compatibility with possible future extensions, software must not enable L1 PM Substates unless this bit is set. This RWO field must be programmed prior to enabling ASPM.
3	1h RW/O	**ASPM L1.1 Substates Supported (AL11S):** When set, this bit indicates that this port supports L1 substates for ASPM L1.SNOOZ. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
2	1h RW/O	**ASPM L1.2 Supported (AL12S):** When set, this bit indicates that ASPM_L1.OFF is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
1	1h RW/O	**PCI-PM L1.1 Supported (PPL11S):** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

Bit Range	Default & Access	Field Name (ID): Description
0	1h RW/O	**PCI-PM L1.2 Supported (PPL12S):** When set, this bit indicates that L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

17.5.54 L1 Sub-States Control 1 (L1SCTL1)—Offset 208h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**L1.2 LTR Threshold Latency ScaleValue (L12LTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe root port. The value in this field, together with L12LTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L12LTRSTLV times 1 ns 001: L12LTRSTLV times 32 ns 010: L12LTRSTLV times 1024 ns 011: L12LTRSTLV times 32768 ns 100: L12LTRSTLV times 1048576 ns 101: L12LTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
28:26	0h RO	**Reserved (RSVD):** Reserved
25:16	0h RW	**L1.2 LTR Threshold Latency Value (L12OFFLTRTLV):** This field contains the L1.2 LTR Threshold Latency Value for this particular PCIe root port. The value in this field, together with L12LTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
15:8	0h RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time the PCIe root port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved (RSVD_1):** Reserved
3	0h RW	**ASPM L1.1 Enabled (AL11E):** When set, this bit indicates that ASPM L1.SNOOZ substates are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic
2	0h RW	**ASPM L1.2 Enable (AL12E):** When set, this bit indicates that ASPM L1.OFF substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic
1	0h RW	**PCI-PM L1.SNOOZ Enable (PPL11E):** When set, this bit indicates that PCI-PM L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
0	0h RW	**PCI-PM L1.2 Enabled (PPL12E):** When set, this bit indicates that PCI-PM L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.

17.5.55 L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 28h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:3	5h RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# is sampled asserts in L1.OFF state. Tpower_on value is calculated by multiplying the value in this field by the value in the TPOS field. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
2	0h RO	**Reserved (RSVD_1):** Reserved
1:0	0h RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. '00b': 2 us '01b': 10 us '10b': 100us '11b': Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static

17.5.56 Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h

Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEECID):** PCI Express Extended Capability ID (PCIEECID): This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 0019h to this register else it should write 0.

17.5.57 Link Control 3 (LCTL3)—Offset 224h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:9	0h RO	**Enable Lower SKP OS Generation Vector (ELSOSGV):** Enable Lower SKP OS Generation Vector(ELSOSGV): When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is Set in this field and the corresponding bit in the Lower SKP OS Generation Supported Speeds Vector is not set.
8:2	0h RO	**Reserved (RSVD_1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Link Equalization Request Interrupt Enable (LERIE):** Link Equalization Request Interrupt Enable (LERIE): When set, this bit enables the generation of an interrupt to indicate that the Link Equalization Request bit has been set.
0	0h RW	**Perform Equalization (PE):** Perform Equalization (PE): When this bit is 1b and Link Retrain bit is set with the Target Link Speed field set to 8 GT/s, the Downstream Port must perform Link Equalization. This bit is cleared by Root Port upon entry to Link Equalization

17.5.58 Lane Error Status (LES)—Offset 228h

The Lane number is the default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD):** Reserved
3	0h RW/1C/V/P	**Lane 3 Error Status (L3ES):** Lane 3 Error Status (L3ES): Lane 3 detected a Lane-based error.
2	0h RW/1C/V/P	**Lane 2 Error Status (L2ES):** Lane 2 Error Status (L2ES): Lane 2 detected a Lane-based error.
1	0h RW/1C/V/P	**Lane 1 Error Status (L1ES):** Lane 1 Error Status (L1ES): Lane 1 detected a Lane-based error.
0	0h RW/1C/V/P	**Lane 0 Error Status (L0ES):** Lane 0 Error Status (L0ES): Lane 0 detected a Lane-based error.

17.5.59 Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 7F7F7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved.
30:28	7h RW	**Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH):** Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 1 Transmitter Preset (UPL1TP):** Upstream Port Lane 1 Transmitter Preset (UPL1TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	**Reserved (RSVD_1):** Reserved.
22:20	7h RW	**Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH):** Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 1 Transmitter Preset (DPL1TP):** Downstream Port Lane 1 Transmitter Preset (DPL1TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved (RSVD_2):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
14:12	7h RW	**Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH):** Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 0 Transmitter Preset (UPL0TP):** Upstream Port Lane 0 Transmitter Preset (UPL0TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	**Reserved (RSVD_3):** Reserved.
6:4	7h RW	**Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH):** Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 0 Transmitter Preset (DPL0TP):** Downstream Port Lane 0 Transmitter Preset (DPL0TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

17.5.60 Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 7F7F7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
30:28	7h RW	**Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH):** Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 3 Transmitter Preset (UPL3TP):** Upstream Port Lane 3 Transmitter Preset (UPL3TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	**Reserved (RSVD_1):** Reserved
22:20	7h RW	**Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH):** Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 3 Transmitter Preset (DPL3TP):** Downstream Port Lane 3 Transmitter Preset (DPL3TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved (RSVD_2):** Reserved
14:12	7h RW	**Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH):** Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 2 Transmitter Preset (UPL2TP):** Upstream Port Lane 2 Transmitter Preset (UPL2TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	**Reserved (RSVD_3):** Reserved
6:4	7h RW	**Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH):** Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
3:0	Fh RW	**Downstream Port Lane 2 Transmitter Preset (DPL2TP):** Downstream Port Lane 2 Transmitter Preset (DPL2TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

17.5.61 PCI Express Replay Timer Policy 1 (PCIERTP1)—Offset 300h

The Replay Timer controlled by the Replay Timeout field is started when the Retry Buffer is empty and a TLP is placed into it or an Ack/Nak DLLP is received and there are still non-acknowledged packets within the Retry Buffer. The counter continues to count until the next valid Ack DLLP or a NAK DLLP that acknowledges unacknowledged TLPs is received, or it reaches the timeout value specified by this register. When a valid Ack/Nak DLLP is received, the timer is reset to zero and restarted if there are still non-acknowledged packets within the Retry Buffer. Otherwise if the Retry Buffer is empty, the counter is just reset to zero. If the timer reaches the timeout value, the non-acknowledged packets within the Retry Buffer will be replayed.
The default for this register is dependant on the MAX_PAYLOAD_SIZE , the NEGOTIATED_WIDTH, and the NEGOTIATED_SPEED.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: A64F96h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved,
23:20	Ah RW	**Gen 2 x1 (G2X1):** Gen 2 x1 (G2X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 7) * 64 link clocks. For PCIE Gen 2 speed and x1 width For Mobile Express HS-Gear 3 speed and x1 width.

Bit Range	Default & Access	Field Name (ID): Description
19:16	6h RW	**Gen 2 x2 (G2X2):** Gen 2 x2 (G2X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 4) * 64 link clocks. For PCIe Gen 2 speed and x2 width. For Mobile Express HS-Gear 3 speed and x2 width.
15:12	4h RW	**Gen 2 x4 (G2X4):** Gen 2 x4 (G2X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 2 speed and x4 width. For Mobile Express HS-Gear 3 speed and x4 width.
11:8	Fh RW	**Gen 1 x1 (G1X1):** Gen 1 x1 (G1X1): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/ Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 10) * 64 link clocks. For 512B MPS: (nnn + 17) * 64 link clocks. For PCIe Gen 1 speed and x1 width. For Mobile Express HS-Gear 2 speed and x1 width.
7:4	9h RW	**Gen 1 x2 (G1X2):** Gen 1 x2 (G1X2): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/ Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For PCIe Gen 1 speed and x2 width. For Mobile Express HS-Gear 2 speed and x2 width.

Bit Range	Default & Access	Field Name (ID): Description
3:0	6h RW	**Gen 1 x4 (G1X4):** Gen 1 x4 (G1X4): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/ Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 1 speed and x4 width. For Mobile Express HS-Gear 2 speed and x4 width.

17.5.62 PCI Express Replay Timer Policy 2 (PCIERTP2)—Offset 304h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 1BC00B86h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Lane 0 Lane Number (L0LN):** Lane 0 Lane Number(L0LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 0 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
29:28	1h RW	**Lane 1 Lane Number (L1LN):** Lane 1 Lane Number(L1LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 1 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.

Bit Range	Default & Access	Field Name (ID): Description
27:26	2h RW	**Lane 2 Lane Number (L2LN):** Lane 2 Lane Number(L2LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 2 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
25:24	3h RW	**Lane 3 Lane Number (L3LN):** Lane 3 Lane Number(L3LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 3 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
23	1h RW	**Loopback Master EQ TS1 Enable (LMEQTS1E):** Loopback Master EQ TS1 Enable(LMEQTS1E): When set, the Loopback Master will use EQ TS1 Ordered Sets to direct the Loopback Slave into Loopback from Configuration.Linkwidth.Start. The Preset field of the EQ TS1 Ordered Sets will be specified by Upstream Port Lane X Transmitter Preset and Upstream Port Lane X Receiver Preset Hint fields in the Lane Equalization Control registers.
22	1h RW	**Loopback Master EQ Change Enable (LMEQCE):** Loopback Master EQ Change Enable(LMEQCE): This field is applicable to the case where Loopback is entered from Recovery state. When set, the Loopback Master will set the EC field of the GEN3 TS1 Ordered Sets to the appropriate value based on the ports direction(10b or 11b) to direct the Loopback Slave into Loopback from Recovery state. The Preset field of the GEN3 TS1 Ordered Sets will be specified by Upstream Port Lane X Transmitter Preset and Upstream Port Lane X Receiver Preset Hint fields in the Lane Equalization Control registers.
21:12	0h RO	**Reserved (RSVD):** Reserved
11:8	Bh RW	**Gen 3 x1 (G3X1):** Gen 3 x1 (G3X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For Gen 3 speed and x1 width

Bit Range	Default & Access	Field Name (ID): Description
7:4	8h RW	**Gen 3 x2 (G3X2):** Gen 3 x2 (G3X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For Gen 3 speed and x2 width
3:0	6h RW	**Gen 3 x4 (G3X4):** Gen 3 x4 (G3X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 1) * 64 link clocks. For 512B MPS: (nnn + 2) * 64 link clocks. For Gen 3 speed and x4 width

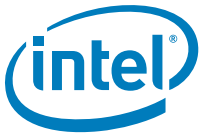
17.5.63 PCI Express Status 1 (PCIESTS1)—Offset 328h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LTSM State (LTSMSTATE):** Indicates the LTSM present state. Hex LTSSM States 00DETIDLE 01DETRDY 02DETIDLEP1TOP2 03DETRDYP2TOP1 04DETRDYINP1 05DETRDYINP1EXE 06DETP2POLLSTART 07DETP1POLLSTART 08DETP2TOP0 09DETP1TOP0 0AECPCMPRETRAIN 0BECPCMFAILP0TOP2 0CDETP0TOP2 0DPMODECHANGE 0EECPCMPCIE 0FECPCMUSB3 10DET2POLLINP0 11POLLINGACTIVE 12POLLINGCOMPLIANCEMARGINCNT 13POLLINGCOMPLIANCE 14POLLINGCOMPLIANCESPEEDUP 15POLLINGCOMPLIANCESPEEDDN 16POLLINGCOMPLIANCESPEEDTXEIDLE 17POLLINGCOMPLIANCESPEEDRXEIDLE 18POLLINGCOMPLIANCESPEED 19POLLINGCOMPLIANCESPEEDDONE 1APOLLINGCOMPLIANCEEXIT 1BPOLLINGCONFIGURATION 1CPOLLINGTXEIDLE 1DPOLLINGEND 1EPOLLINGENDWAIT 1FLINKWIDTHSTART 20LINKWIDTHACCEPT 21LANENUMWAIT 22LANENUMACCEPT 23LANEDESKEW 24CONFIGCOMPLETE 25CONFIGIDLE 26LWNEXITRECOVERY 27CONFIGLPBKENTRY 28CONFIGLPBKLWSTART 29CONFIGLPBKSPEEDTXEIDLE 2ACONFIGLPBKSPEEDSTART 2BCONFIGLPBKSPEEDRXEIDLE 2CCONFIGLPBKSPEED 2DCONFIGLPBKREUTSKIP 2ECONFIGLPBKREUT 2FCONFIGLPBKEXITM 30CONFIGLPBKTXEIDLE



Bit Range	Default & Access	Field Name (ID): Description
		31LWNEXIT 32LWNLNK2DETECT 33L0 34TXL0SRXL0 35RXL0STXL0 36TXL0SRXL0S 37L1TXEIDLE 38L1RCVEIDLE 39L1PREENTRY 3AL1ENTRY 3BL1IDLE 3CL1IDLEGEN2WAIT 3DL1EXIT 3EL2TXEIDLE 3FL2RCVEIDLE 40L2IDLEWAIT 41L2IDLERDY 42L2IDLE 43LOOPBACKENTRY 44LPBKACTIVEMTXSKP 45LPBKACTIVEMSKPDSKW 46LOOPBACKACTIVEM 47LPBKSLAVESPEEDTXEIDLE 48LPBKSLAVESPEEDRXEIDLE 49LPBKSLAVESPEED 4ALOOPBACKACTIVES 4BLOOPBACKCMMSKP 4CLOOPBACKCMM 4DLOOPBACKEXITM 4ELOOPBACKEXITS 4FLOOPBACKEXITL0 50LOOPBACKLNK2DETECT 51LOOPBACK2DETECT 52DISTX16TS1DIS 53DISTXEIDLE 54DISWAITSTART 55DISWAITGNT 56DISWAIT4TXMARGIN 57DISWAIT 58DIS2DETECT 59HOTRESETTS1 5AHOTRESETDONE 5BHOTRESETEIDLE 5CRECOVERYRCVRWAIT 5DRECOVERYRCVRMARGINCNT 5ERECOVERYRCVRLOCK 5FRECOVERYDESKEW 60RECOVERYRCVRCFG 61RECOVERYSPEED 62RECOVERYSPEEDTXEIDLE 63RECOVERYSPEEDRXEIDLE

Bit Range	Default & Access	Field Name (ID): Description
		64RECOVERYSPEEDREADY 65RECOVERYIDLE 66RECOVERYEXITDETECT 67RECOVERYLNK2DETECT 68RECOVERYEXITLPBK 69RECOVERYEXITL0 6ARECOVERYEXITDIS 6BRECOVERYEXITRST Note: This register field could be used by REUT software to monitor the link LTSSM substates.
23	0h RO	**Reserved (RSVD):** Reserved.
22:19	0h RO/V	**Link Status (LNKSTAT):** During Link initialization the Link will always traverse this list of state from the top (0000) to the bottom of the list (0111). One or more power management states may be skipped, but the direction of list traversal will remain the same. 0000 Link Down 0001 : Link Retrain 0011 : L1 0100 : L2 0101 : L3 0111 : L0 (Link Up) 1000 : L0s (Transmit [amp] Receive) 1001 : L0s (Transmit only) 1010 : L0s (Receive only) All others reserved
18:17	0h RO/V	**Replay Number (REPLAYNUM):** Number of times the Retry Buffer has been replayed since the last Link initialization / re-training. When the Data Link Layer has replayed the contents of the Retry Buffer four times a Link re-training will be initiated which will reset this value back to zero.
16	0h RO/V	**Data Link Layer Retry (DLLRETRY):** Indicates when the Data Link Layer has received a corrupted TLP or has detected a dropped packet and is currently waiting for the remote agent to re-transmit the corrupted/dropped packet. The value of Next Receive Sequence Number will be the sequence number associated with the corrupted packet.
15:12	0h RO/V	**Lane Status (LANESTAT):** Indicates which lanes are trained. A '1' indicates that the corresponding lane is trained (i.e. bit 0 = '1' means lane 0 is trained).
11:0	0h RO/V	**Next Transmitted Sequence Number (NXTTXSEQNUM):** This is the sequence number to be applied to and pre-pended to the next outgoing TLP.

17.5.64 PCI Express Status 2 (PCIESTS2)—Offset 32Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**PCIe Port 3 Non-Common Clock With SSC Mode Enable Strap (P3PNCCWSSCMES):** '0': PCIe port 3 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 3 is enabled to operate in non-common clock mode with SSC enabled.
30	0h RO/V	**PCIe Port 2 Non-Common Clock With SSC Mode Enable Strap (P2PNCCWSSCMES):** '0': PCIe port 2 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 2 is enabled to operate in non-common clock mode with SSC enabled.
29	0h RO/V	**PCIe Port 1 Non-Common Clock With SSC Mode Enable Strap (P1PNCCWSSCMES):** '0': PCIe port 1 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 1 is enabled to operate in non-common clock mode with SSC enabled.
28	0h RO/V	**PCIe Port 0 Non-Common Clock With SSC Mode Enable Strap (P0PNCCWSSCMES):** '0': PCIe port 0 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 0 is enabled to operate in non-common clock mode with SSC enabled.
27:16	0h RO/V	**Next Receive Sequence Number (NXTRCVSEQ):** This is the sequence number associated with the TLP that is expected to be received next.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/1C/V	**Cause of Last Recovery Event (CLRE):** Cause of Last Recovery Event (CLRE): This field logs the cause of the entry to Recovery from L0. Only the first cause of Recovery is captured, until the register is cleared. Encoding Recovery Event 0000 No Recovery. 0001 Recovery entry triggered by remote device. 0010 Link Layer initiated Link Retrain due to error. 0011 De-skew buffer full. 0100 L0s exit time-out. 0101 Elastic Buffer overrun/underrun. 0110 Triggered by speed change. 0111 Link upconfiguration/downconfiguration. 1000 L0 Electrical Idle Inference. 1001 Any of the Link Retrain, CMM Start, Hot Reset, Link Disable, REUT Loopback Master or REUT Forced Loopback Master bit set. 1010 Received EIOS for RXL0s entry when ASPM L0s is disabled. 1011 Entry to Recovery from RXL0s due to PME timeout. Others Reserved.
11:0	0h RO/V	**Last Acknowledged Sequence Number (LASTACKSEQNUM):** This is the sequence number associated with the last acknowledged TLP.

17.5.65 PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h

Note that selecting a lane number that does not exist for a port may result in undefined behavior.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 2A000016h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**GEN3 Intel CMM Scrambler Bypass (G3ICMMSB):** GEN3 Intel CMM Scrambler Bypass(G3ICMMSB): When set, the Intel CMM pattern will bypass scrambling in GEN3. This bit does not impact non Intel CMM pattern. The TSx and SOS prior to Intel CMM will still be scrambled normally. Note: This bit must be set prior to enabling Intel CMM, by setting the PCIECMMPC.START. Note: When operating in Mobile Express mode, this field is not applicable.
30	0h RO	**Reserved (RSVD):** Reserved
29	1h RW	**CMM Symbol[3] Select (SYM3SEL):** 0: selects CMM Symbol [lb]3[rb] to a control character 1: selects CMM Symbol [lb]3[rb] as a data character
28	0h RW	**CMM Symbol[2] Select (SYM2SEL):** 0: selects CMM Symbol [lb]2[rb] to a control character 1: selects CMM Symbol [lb]2[rb] as a data character
27	1h RW	**CMM Symbol[1] Select (SYM1SEL):** 0: selects CMM Symbol [lb]1[rb] to a control character 1: selects CMM Symbol [lb]1[rb] as a data character
26	0h RW	**CMM Symbol[0] Select (SYM0SEL):** 0: selects CMM Symbol [lb]0[rb] to a control character 1: selects CMM Symbol [lb]0[rb] as a data character
25:24	2h RW	**CMM Sync Header (CMMSH):** CMM Sync Header(CMMSH): Specifies the Sync Header for the Intel CMM pattern specified in PCIECMMSB. Note: Due to implementation limitation, only a value of 10b is supported. All the other values are not supported.
23:22	0h RO/V	**CMM Error Lane Number (ERRLANENUM):** This field contains the lane number of the failing lane. Only valid when CMM Error Detected is 1.
21:16	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO/V	**CMM Invert (INVERT):** Indicates which lanes are inverted 000: No inversion 001: Lanes 0 010: Lanes 1 011: Lanes 2 100: Lanes 3 This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated)
12:10	0h RO/V	**CMM Symbol Error Number Invert (SYMERRNUMINV):** Indicates which register number miscompared on the failing lane, if the failing lane was an inverted lane. Only valid when CMM Error Detected is 1. 000: CMM Data D0 001: CMM Data D0 010: CMM Data D0 011: CMM Data D1 100: CMM Data D2 101: CMM Data D3 110: CMM Data D0 111: CMM Data D0
9:8	0h RO/V	**CMM Symbol Error Number (SYMERRNUM):** Indicates which register number miscompared on the failing lane, if the failing lane was not inverted. Only valid when CMM Error Detected is 1. 00: CMM Data 0 01: CMM Data 1 10: CMM Data 2 11: CMM Data 3
7	0h RW/1C/V	**CMM Error Detected (ERRDET):** 1: An error was detected 0: No error detected Note: This bit will be shadowed to an observability pin that can be used for IRQ generation.
6:5	0h RW	**Select Lane Number to be inverted for CMM (SLNINVCMM):** Select Lane Number to be inverted for CMM
4	1h RW	**CMM AutoInvert (AUTOINVERT):** 1: CMM autosequences through the inversion 0: CMM does not sequence inversion
3	0h RO/V	**CMM Status (STAT):** This bit is set when the CMM Start bit is set and cleared when the CMM mode has been entered successfully. 0: Compliance Measurement Mode is not active or CMM mode has been entered successfully. 1: Set as a result of CMM Start bit being set.
2	1h RW	**CMM Invert Enable (INVEN):** 1: Enables the Inversion of the lane 0: Lane not inverted
1	1h RW	**Reserved (RSVD_2):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/L	**CMM Start (START):** 1: Start CMM 0: Stop CMM

17.5.66 PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 4ABCB5BCh

Bit Range	Default & Access	Field Name (ID): Description
31:24	4Ah RW	**CMM Data [3] (DATA3):** This character contains CMM Data [lb]3[rb] that will be transmitted on the link.
23:16	BCh RW	**CMM Data [2] (DATA2):** This character contains CMM Data [lb]2[rb] that will be transmitted on the link.
15:8	B5h RW	**CMM Data [1] (DATA1):** This character contains CMM Data [lb]1[rb] that will be transmitted on the link.
7:0	BCh RW	**CMM Data [0] (DATA0):** This character contains CMM Data [lb]0[rb] that will be transmitted on the link.

17.5.67 PTM Propagation Delay (PTMPD)—Offset 390h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Propagation Delay Value (CPTMPDV):** Current PTM Propagation Delay Value(CPTMPDV): This field reports the current PTM Propagation Delay value captured from the last successful PTM dialog.

17.5.68 PTM Lower Local Master Time (PTMLLMT)—Offset 394h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Lower Local Master Time Value (CPTMLLMTV):** Current PTM Lower Local Master Time Value(CPTMLLMTV): This field reports the lower fields bits 31:0 of the Local TSC time value.

17.5.69 PTM Upper Local Master Time (PTMULMT)—Offset 398h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Upper Local Master Time Value (CPTMULMTV):** Current PTM Upper Local Master Time Value(CPTMULMTV): This field reports the upper fields bits 63:32 of the Local TSC time value.

17.5.70 PTM Pipe Stage Delay Configuration 1 (PTMPSDC1)—Offset 39Ch

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN1 X2 RX Pipe Stage Delay (G1X2RPSD):** GEN1 X2 RX Pipe Stage Delay(G1X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN1 X2 TX Pipe Stage Delay (G1X2TPSD):** GEN1 X2 TX Pipe Stage Delay(G1X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN1 X1 RX Pipe Stage Delay (G1X1RPSD):** GEN1 X1 RX Pipe Stage Delay(G1X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN1 X1 TX Pipe Stage Delay (G1X1TPSD):** GEN1 X1 TX Pipe Stage Delay(G1X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.5.71 PTM Pipe Stage Delay Configuration 2 (PTMPSDC2)—Offset 3A0h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN2 X1 RX Pipe Stage Delay (G2X1RPSD):** GEN2 X1 RX Pipe Stage Delay(G2X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN2 X1 TX Pipe Stage Delay (G2X1TPSD):** GEN2 X1 TX Pipe Stage Delay(G2X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN1 X4 RX Pipe Stage Delay (G1X4RPSD):** GEN1 X4 RX Pipe Stage Delay(G1X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN1 X4 TX Pipe Stage Delay (G1X4TPSD):** GEN1 X4 TX Pipe Stage Delay(G1X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.5.72 PTM Pipe Stage Delay Configuration 3 (PTMPSDC3)—Offset 3A4h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN2 X4 RX Pipe Stage Delay (G2X4RPSD):** GEN2 X4 RX Pipe Stage Delay(G2X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN2 X4 TX Pipe Stage Delay (G2X4TPSD):** GEN2 X4 TX Pipe Stage Delay(G2X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN2 X2 RX Pipe Stage Delay (G2X2RPSD):** GEN2 X2 RX Pipe Stage Delay(G2X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN2 X2 TX Pipe Stage Delay (G2X2TPSD):** GEN2 X2 TX Pipe Stage Delay(G2X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.5.73 PTM Pipe Stage Delay Configuration 4 (PTMPSDC4)—Offset 3A8h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN3 X2 RX Pipe Stage Delay (G3X2RPSD):** GEN3 X2 RX Pipe Stage Delay(G3X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN3 X2 TX Pipe Stage Delay (G3X2TPSD):** GEN3 X2 TX Pipe Stage Delay(G3X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN3 X1 RX Pipe Stage Delay (G3X1RPSD):** GEN3 X1 RX Pipe Stage Delay(G3X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN3 X1 TX Pipe Stage Delay (G3X1TPSD):** GEN3 X1 TX Pipe Stage Delay(G3X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.5.74 PTM Pipe Stage Delay Configuration 5 (PTMPSDC5)—Offset 3ACh

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:8	0h RW	**GEN3 X4 RX Pipe Stage Delay (G3X4RPSD):** GEN3 X4 RX Pipe Stage Delay(G3X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN3 X4 TX Pipe Stage Delay (G3X4TPSD):** GEN3 X4 TX Pipe Stage Delay(G3X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.5.75 PTM Extended Config (PTMECFG)—Offset 3B0h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20:18	0h RW	**Periodic Local TSC Link Fetch Frequency (PLTLFF):** Periodic Local TSC Link Fetch Frequency (PLTLFF): When this register is programmed to a non-zero values, the Local TSC Link Clock would perform a periodic fetch to obtain the latest TSC from the Local TSC XTAL Clock domain. This mechanism would ensure the Root Port Local TSC Link is always synchronized with the actual TSC as Link Clock domain is able to drift due to SSC. 000: Disable this feature. 001: Always pull without waiting for expiration. 010: Every 8 clocks 011: Every 16 clocks 100: Every 32 clocks 101: Every 64 clocks 110: Every 128 clocks 111: Every 256 clocks This register is only available in Port 1. Note: Software is expected to program this register prior to setting PTM Enable.
17:15	0h RW/1C/V	**Global Time Fetch Retry Counter (GTFRC):** Global Time Fetch Retry Counter. This register is incremented when the Root Port detected a retry on each Global Time Fetch on IOSF Sideband. The Root Port would increment the value of this register whenever ARU re-sends a LocalSync message. If more than 7 Retries are detected during the Global Time Fetch, Root Port would keep the value of this register to 111 (max) value. Software is expected to write 111 to this register to clear the entire field to 0. Note: For each x4 instance, only the value from Port 1 is used.
14:13	0h RW/1C/V	**Global Time Fetch Fail Counter (GTFFC):** Global Time Fetch Fail Counter. This register is incremented when the Root Port detected a fail on each Global Time Fetch on IOSF Sideband. The Root Port would increment the value of this register whenever ARU sends a SyncComp with the Fail status. If more than 3 failures are detected in the Global Time Fetch, Root Port would keep the value of this register to 111 (max) value. Software is expected to write 11 to this register to clear the entire field to 0. Note: For each x4 instance, only the value from Port 1 is used.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Global Time Fetch Status Pending Completion (GTFSPC):** Global Time Fetch Status Pending Completion. This register is set to 1 by the Root Port when it is in progress of fetching the Global Time from ARU. Note: For each x4 instance, only the value from Port 1 is used.
11:9	0h RW	**Periodic Global Time Stamp Counter Fetch Frequency (PGTSCFF):** Periodic Global Time Stamp Counter Fetch Frequency (PGTSCFF) : This field determine the frequency the Root Port would autonomously fetch the Global Time Stamp Counter. 00: 10us 01: 100us 10: 500us 10: 1ms Software is expected to program this bit first before programming the PGTSCFE register. Attribute: Dynamic Note: For each x4 instance, only the value from Port 1 is used.
8	0h RW	**Periodic Global Time Stamp Counter Fetch Enable (PGTSCFE):** Periodic Global Time Stamp Counter Fetch Enable (PGTSCFE) : When this bit set, the Controller will re-fetch the Global Time from the Always Running Unit (ARU). Once Fetch is completed, the Controller would update all the Local TSC with the newly fetch Global Time. If any PTM dialog is initiated while the re-fetch occurred, the Controller would use the existing Local TSC timers. Hardware would clear this bit upon completed fetching the Global Time. Attribute : Dynamic Note: For each x4 instance, only the value from Port 1 is used.
7	0h RW	**Trigger Global Time Stamp Counter Fetch Enable (TGTSCFE):** Trigger Global Time Stamp Counter Fetch Enable (TGTSCFE) : When this bit set, the Controller will re-fetch the Global Time from the Always Running Unit (ARU). Once Fetch is completed, the Controller would update all the Local TSC with the newly fetch Global Time. If any PTM dialog is initiated while the re-fetch occurred, the Controller would use the existing Local TSC timers. Hardware would clear this bit upon completed fetching the Global Time. Software can only set this register if PGTSCFE is not set. Attribute : Dynamic Note: For each x4 instance, only the value from Port 1 is used.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**PTM Request Periodic ACK Enable (PTMRPAE):** PTM Request Periodic ACK Enable (PTMRPAE) : When this register is set to 1, whenever a valid PTM request TLP is received, the Link Layer would transmit multiple ACK DLLPs corresponding to the PTM Request message. The number of ACK DLLP that the Link Layer would transmit is based on the PTMRNOPAD register. Attribute : Static Note: For each x4 instance, only the value from Port 1 is used.
5:4	0h RW	**PTM Request Number Of Periodic ACK DLLP (PTMRNOPAD):** PTM Request Number Of Periodic ACK DLLP (PTMRNOPAD) : When PTMRPAE is enable, whenever a valid PTM Request message is received, the Link Layer would transmit multiple ACK DLLP corresponding to the receiving of the PTM Request message. This register define the number of DLLP ACK will be transmitted as high priority. 00 - TX 1 DLLP ACK 01 - TX 2 DLLP ACK 10 - TX 3 DLLP ACK 11 - TX 4 DLLP ACK Attribute : Static Note: For each x4 instance, only the value from Port 1 is used.
3:0	0h RW	**IOSF Max Allowed Delay programming (IOSFMADP):** IOSF Max Allowed Delay programming (IOSFMADP): bits Status 0000 Bound Range Low 0001 Bound Range 2 1000 Bound Range Max others reserved

17.5.76 PTM Lower T2 Time Stamp (PTMLT2TSTMP)—Offset 3B4h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Latest Captured Lower T2 TimeStamp (LCLT2TS):** Latest Captured Lower T2 TimeStamp (LCLT2TS). This field shows the latest lower 32-bit of T2 TimeStamp captured by the Root Port in TSC Clock Domain when the Root Port received a valid PTM Request message. The renewable T2 TimeStamp due to a duplicate PTM Request would also be reflected in this field.

17.5.77 PTM Upper T2 Time Stamp (PTMUT2TSTMP)—Offset 3B8h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Latest Captured Upper T2 TimeStamp (LCUT2TS):** Latest Captured Upper T2 TimeStamp (LCUT2TS). This field shows the latest upper 32-bit of T2 TimeStamp captured by the Root Port in TSC Clock Domain when the Root Port received a valid PTM Request message. The renewable T2 TimeStamp due to a duplicate PTM Request would also be reflected in this field.

17.5.78 Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**mod-PHY Power Gating Disable Fuse (mPHYPGD):** 0: mod-PHY power gating is enabled. 1: mod-PHY power gating is disabled. Note: Prior to fuse pull, the default of this bit is specified in the 'Reset' column of this field. The default value will reflect the fuse value once fuse pull is done.
30:0	0h RO	**Reserved (RSVD):** Reserved

17.5.79 Thermal and Power Throttling (TNPT)—Offset 418h

Access Method

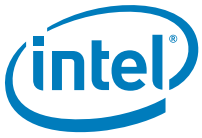
Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 930h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Throttle Period (TP):** Throttle Period (TP): If any of the TNPT.DRXLTE or TNPT.DTXLTE bit is '1, this field defines the duration in milliseconds that defines the Throttling Window. When TNPT.TTG is set to 0, the effective Throttling Period is: 00h: 1 ms 01h: 2 ms : : FFh: 256 ms Note: The Throttle Period will have an uncertainty of +/-1 ms. When TNPT.TTG is set to 1, the effective Throttling Period is: 00h: 100 us 01h: 200 us : : FFh: 25.6 ms Note: The Throttle Period will have an uncertainty of +/-100 us. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling. Note: If TNPT.TT is programmed to a value bigger than TNPT.TP, the hardware behavior is undefined.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RW	**Throttle Time (TT):** Throttle Time (TT): If any of the TNPT.DRXLTE or TNPT.DTXLTE bit is '1, this field defines the period of the Throttling Zone within the Throttling Window specified by TNPT.TP. The value specified in this field will be multiplied by the respective multiplier in TNPT.TSLxM fields depending on the throttling severity indication received together with the Throttling State change indication. When TNPT.TTG is set to 0, the effective Throttle Time is: 00h: 1 ms 01h: 2 ms : 3Fh: 64 ms Others: Alias to 3Fh. Note: The Throttle Period will have an uncertainty of +/-1 ms. When TNPT.TTG is set to 1, the effective Throttle Time is: 00h: 100 us 01h: 200 us : 3Fh: 6.4 ms Note: The Throttle Period will have an uncertainty of +/-100 us. Note: If the reserved encoding is programmed to this field, hardware will behave the same as if the field is programmed to 3Fh. Note: Since the design is using a 1 ms tick for this timer, the Throttle Time will have an uncertainty of +/-1 ms. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling. Note: If TNPT.TT is programmed to a value bigger than TNPT.TP, the hardware behavior is undefined.
15:12	0h RO	**Reserved (RSVD):** Reserved
11:10	2h RW	**Throttling Severity Level 3 Multiplier (TSL3M):** Throttling Severity Level 3 Multiplier (TSL3M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: Always throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.

Bit Range	Default & Access	Field Name (ID): Description
9:8	1h RW	**Throttling Severity Level 2 Multiplier (TSL2M):** Throttling Severity Level 2 Multiplier (TSL2M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: Always throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.
7:6	0h RW	**Throttling Severity Level 1 Multiplier (TSL1M):** Throttling Severity Level 1 Multiplier (TSL1M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: No throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the link throttling
5:4	3h RW	**Throttling Severity Level 0 Multiplier (TSL0M):** Throttling Severity Level 0 Multiplier (TSL0M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: No throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.
3	0h RO	**Reserved (RSVD_1):** Reserved
2	0h RW	**Throttling Timer Granuality (TTG):** Throttling Timer Granuality (TTG): This register determines the granuality of the Thermal Throttling timers. This provides a smaller granuality



Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Dynamic RX Link Throttling Enable (DRXLTE):** Dynamic RX Link Throttling Enable (DRXLTE): '0b: Dynamic Link RX Throttling mechanism is disabled. '1b: Dynamic Link RX Throttling mechanism is enabled. PCIe Root Port will induce the link to enter RXL0s. The duty cycle of the throttling window is configurable based on the throttling severity. Note: This field can only be set if the remote component supports TXL0s.
0	0h RW	**Dynamic TX Link Throttling Enable (DTXLTE):** Dynamic TX Link Throttling Enable (DTXLTE): '0b: Dynamic Link TX Throttling mechanism is disabled. '1b: Dynamic Link TX Throttling mechanism is enabled. PCIe Root Port will induce the link to enter TXL0s. The duty cycle of the throttling window is configurable based on the throttling severity. Note: This field can only be set if the remote component supports TXL0s.

17.5.80 Dynamic Lane Switch (DYNLNSW)—Offset 41Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved (RSVD):** Reserved.
0	0h RW	**Hardware Re-Do Preset to Coefficient Mapping Query After Lane Switching (HWRP2CM):** Hardware Re-Do Preset to Coefficient Mapping Query After Lane Switching (HWRP2CM): When this bit is set, the PCIe-SIP Controller would query the Preset to Coefficient mapping through the PIPE GetLocalPresetCoefficients and LocalTxCoefficientsValid interface whenever the Lane Switch ownership has transitioned to PCIe (from another Controller). Note that if this bit is set while the HPCMQE bit is set, the PCIe-SIP Controller would only perform the query once. Unlike the HPCMQE bit, the PCIe-SIP Controller would not clear this bit after completing the query over the PIPE interface. Register Attribute: Static.

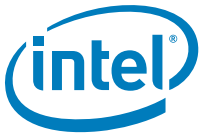
17.5.81 Power Control Enable (PCE)—Offset 428h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 9h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved (RSVD):** Reserved for Force Isolate and Reset Together. This bit is not used. The timing between isolate and reset can be controller through PGCBCTL register.
5	0h RW	**Hardware Autonomous Enable (HAE):** Hardware Autonomous Enable (HAE): If set, and the corresponding per-LTSSM state power gating enable bit is also set, then controller power gating will be done when the controller is idle and the controller power gating condition is met in that particular LTSSM state. Refer to PCIEPMECTL2 register for the per-LTSSM state power gating enable bit. If either this bit. is not set or the corresponding per-LTSSM state power gating enable bit is not set, then controller power gating will not be done in that LTSSM state. Note: For each x4 instance, only the value from Port 0 is used. NOTE: If this bit is set, then bits[lb]2:0[rb] must be '000.
4	0h RO	**Reserved (RSVD_1):** Reserved for Force Isolate and Reset Together. This bit is not used. The timing between isolate and reset can be controller through PGCBCTL register.
3	1h RW/L	**Sleep Enable (SE):** Sleep Enable (SE): If clear, Sleep indication to the retention flops will never assert. If set, Sleep indication will be assert to the retention flops as part of the hardware autonomous controller power gating entry flow.
2	0h RO	**Reserved (RSVD_2):** Reserved for D3-Hot Enable. Not supported. RTD3 is supported instead.
1	0h RO	**Reserved (RSVD_3):** Reserved for D0i3 Enable. No support for D0i3.
0	1h RW	**PMC Request Enable (PMCRE):** PMC Request Enable (PMCRE): When set, the controller will only power gate when pmc_[lt]ip[gt]_sw_pg_req_b = '0 and hardware autonomous controller power gating conditions are met. When clear, controller will power gate immediately when the hardware autonomous controller power gating conditions are met regardless of the state of pmc_[lt]ip[gt]_sw_pg_req_b.



17.5.82 PGCB Control1 (PGCBCTL1)—Offset 42Ch

This register specifies the minimum number of delay clocks the PGCB should wait between various states.
Note: For each x4 instance, only the value from Port 0 is used.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 14155555h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved for cfg_trsvd0. Not applicable since frc_clk_srst_en is tied to '0.
29:28	1h RW	**cfg_trstup2frcclks (trstup2frcclks):** cfg_trstup2frcclks(cfg_trstup2frcclks): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
27:26	1h RW	**cfg_tclksonack_cp (tclksonack_cp):** cfg_tclksonack_cp(cfg_tclksonack_cp): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
25:24	0h RO	**Reserved (RSVD_1):** Reserved for cfg_tclksoffack_srst. Not applicable since frc_clk_srst_en is tied to 0.
23:22	0h RO	**Reserved (RSVD_2):** Reserved for cfg_tclksonack_srst. Not applicable since frc_clk_srst_en is tied to 0.
21:20	1h RW	**cfg_tpokup (tpokup):** cfg_tpokup(cfg_tpokup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
19:18	1h RW	**cfg_tpokdown (tpokdown):** cfg_tpokdown(cfg_tpokdown): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
17:16	1h RW	**cfg_tlatchdis (tlatchdis):** cfg_tlatchdis(cfg_tlatchdis): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
15:14	1h RW	**cfg_tsleepinactiv (tsleepinactiv):** cfg_tsleepinactiv(cfg_tsleepinactiv): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
13:12	1h RW	**cfg_tinaccrstup (tinaccrstup):** cfg_tinaccrstup(cfg_tinaccrstup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
11:10	1h RW	**cfg_taccrstup (taccrstup):** cfg_taccrstup(cfg_taccrstup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
9:8	1h RW	**cfg_tlatchen (tlatchen):** cfg_tlatchen(cfg_tlatchen): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
7:6	1h RW	**cfg_tdeisolate (tdeisolate):** cfg_tdeisolate(cfg_tdeisolate): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
5:4	1h RW	**cfg_trstdown (trstdown):** cfg_trstdown(cfg_trstdown): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
3:2	1h RW	**cfg_tisolate (tisolate):** cfg_tisolate(cfg_tisolate): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
1:0	1h RW	**cfg_tsleepact (tsleepact):** cfg_tsleepact(cfg_tsleepact): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

17.5.83 PGCB Control2 (PGCBCTL2)—Offset 430h

This register specifies the minimum number of delay clocks the PGCB should wait between various states.
Note: For each x4 instance, only the value from Port 0 is used.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 54h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved.
7:6	1h RW	**cfg_trsvd4 (trsvd4):** cfg_trsvd4(cfg_trsvd4): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
5:4	1h RW	**cfg_trsvd3 (trsvd3):** cfg_trsvd3(cfg_trsvd3): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
3:2	1h RW	**cfg_trsvd2 (trsvd2):** cfg_trsvd2(cfg_trsvd2): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	**Reserved (RSVD_1):** Reserved for cfg_trsvd1. Not applicable since frc_clk_srst_en is tied to 0.

17.5.84 Equalization Configuration 1 (EQCFG1)—Offset 450h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 3102h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Recovery Entry Count (REC):** Recovery Entry Count (REC): This field indicates the value of the Recovery Entry Counter. This is a 1-based counter. Software must read this register multiple times. The value is valid only if the same value is read out on both of the reads.
23	0h RW	**Recovery Entry and Idle Framing Error Count Enable (REIFECE):** Recovery Entry and Idle Framing Error Count Enable (REIFECE): This bit, when set by software turns on the Recovery Entry Counter and the per-lane Idle Framing Error Counter. The counters are reset when this bit is cleared. This bit is expected to be used by the Software Preset/Coefficient Search tool but is not precluded to be used for other debug purpose. The value of the Recovery Entry Count can be read through EQCFG1.REC field. The value of the Idle Framing Error Count can be read through the Monitor Mux register.
22	0h RW	**Quiesce Guarantee (QG):** Quiesce Guarantee (QG): When set, the Quiesce Guarantee bit in the transmitted TS2 Ordered Set will be set in Recovery.RcvrCfg. When clear, the Quiesce Guarantee bit in the transmitted TS2 Ordered Set will be clear. In all other states, the Quiesce Guarantee bit is Reserved.
21	0h RW	**Link Equalization Request SMI Enable (LERSMIE):** Link Equalization Request SMI Enable (LERSMIE): When set, this bit enables the generation of an SMI to indicate that the Link Equalization Request bit has been set. This mode is meant for survivability purpose such that BIOS can be invoked to address the Re-Equalization request.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Reset EIEOS Interval Count (REIC):** Reset EIEOS Interval Count(REIC): When set, allows the root port to restrict the device from sending EIEOS until after 65536 TS1 Ordered Sets have been transmitted in Phase 3 of the Link Equalization, in the window when the receiver is evaluating the remote transmitter settings..
19	0h RW	**Link Equalization Bypass (LEB):** Link Equalization Bypass (LEB): When set, the root port will never initiate entry to Recovery.Equalization state. This includes never send EQ TS2 in Recovery.RcvrCfg that could cause the device to set start_equalization_w_preset variable. Note: This bit only affects the initial autonomous transition to Link Equalization state when equalization_done_8GT_data_rate = 0. This bit does not affect the software-direction to re-perform Link Equalization.
18	0h RW	**Link Equalization Phase 2 and 3 Bypass (LEP23B):** Link Equalization Phase 2 and 3 Bypass(LEP23B): When set, bypasses the Phase 2 and Phase 3 of Link Equalization. Once Phase 1 is completed, Root Port transitions from Phase 1 directly to Recovery.RcvrLock.
17	0h RW	**Link Equalization 3 Bypass (LEP3B):** Link Equalization 3 Bypass(LEP3B): When set, bypasses the Phase 3 of Link Equalization. Once Phase 2 is completed, Root Port transitions from Phase 2 directly to Recovery.RcvrLock.
16	0h RW	**Remote Transmit Link Equalization Preset/Coefficient Evaluation Bypass (RTLEPCEB):** Remote Transmit Link Equalization Preset/Coefficient Evaluation Bypass (RTLEPCEB): When set, this bit disables the Hardware Autonomous Preset/ Coefficient Search mechanism to search for the best Preset or Coefficient by traversing the Preset or Coefficient List and checking the receiver eye width margin for each of the settings. Instead, the Preset/Coefficient values used by the remote Transmitter will be accepted and the Link Equalization phase will be completed after one round of receiver link training, excluding margining. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Remote Transmitter Preset Coefficient Override Enable (RTPCOE):** Remote Transmitter Preset Coefficient Override Enable (RTPCOE): When set, this bit disables the hardware mechanism to search for the best Preset or Coefficient by traversing the Preset or Coefficient List and checking the receiver eye width margin for each of the settings. Instead, the Preset or Coefficient values specified by the override fields are used. If RTPCL1.PCM = 1, the Preset Override values for each lanes is derived from the following register fields: Lane 0: RTPCL1.RTPRECL0PL0. Lane 1: RTPCL1.RTPOSTCL0PL1. Lane 2: RTPCL1.RTPRECL1PL2. Lane 3: RTPCL1.RTPOSTCL1PL3. If RTPCL1.PCM = 0, the Coefficient Override values for each lanes is derived from the following register fields: Lane 0: RTPCL1.RTPRECL0PL0 and RTPCL1.RTPOSTCL0PL1. Lane 1: RTPCL1.RTPRECL1PL2 and RTPCL1.RTPOSTCL1PL3. Lane 2: RTPCL1.RTPRECL2PL4 and RTPCL2.RTPOSTCL2PL5. Lane 3: RTPCL2.RTPRECL3PL6 and RTPCL2.RTPOSTCL3PL7. BIOS must ensure that the corresponding RTPCL* registers above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
14	0h RW	**Link Equalization Request SCI Enable (LERSCIE):** Link Equalization Request SCI Enable (LERSCIE): When set, this bit enables the generation of an SCI to indicate that the Link Equalization Request bit has been set. This mode is meant for survivability purpose such that SCI handler can be invoked to address the Re-Equalization request.

Bit Range	Default & Access	Field Name (ID): Description
13	1h RW/1S/V	**Hardware Preset to Coefficient Mapping Query Enable (HPCMQE):** Hardware Preset to Coefficient Mapping Query Enable(HPCMQE): When set, the controller will query the Preset to Coefficient mapping through the PIPE GetLocalPresetCoefficients and LocalTxCoefficientsValid interface whenever this bit transitions from 0 to 1. The default of this register bit is 1, indicating that the Preset to Coefficient mapping query will be done on the PIPE interface once coming out of reset. Controller will then update the Preset-Coefficient Mapping registers with the corresponding Coefficient, for each Preset. Controller will also update the LFFS Local LF and Local FS field with the local PHY LF and FS values. Hardware will clear this bit when the Preset to Coefficient mapping query over the PIPE interface is completed. If the Hardware Preset to Coefficient Mapping mechanism is never enabled, the value of the Preset to Coefficient mapping configured by BIOS through the Preset-Coefficient Mapping registers will be used instead of querying through the PIPE interface. Note: BIOS should check to ensure that this field is cleared before enabling Controller Power Gating or mod-PHY Power Gating.
12	1h RO/V	**Hardware Autonomous Equalization Done (HAED):** Hardware Autonomous Equalization Done(HAED): This bit will be cleared when Hardware Autonomous Preset/Coefficient Search starts and will be set when Hardware Autonomous Preset/Coefficient Search is done. This bit is polled by software to ensure that the Hardware Autonomous Preset/Coefficient Search is done before proceeding with the next software sequencing. Some of the Hardware Autonomous Preset/ Coefficient search algorithm may involve the hardware initiating multiple speed change to allow multiple iterations of Link Equalization to be done with different Preset/Coefficient lists. This bit will remain cleared until the iterations are done.

Bit Range	Default & Access	Field Name (ID): Description
11:8	1h RW	**Receiver Wait Time For New Equalization Value Evaluation (RWTNEVE):** Receiver Wait Time For New Equalization Value Evaluation (RWTNEVE): For Downstream Port: This field specifies the amount of time the receiver will wait after entering Phase 3 and sending the new Preset or Coefficient values through the TS1 Ordered Sets before validating the Block Alignment and eventually evaluate the incoming ordered sets (RXEqEval on the PIPE interface asserts). For Upstream Port: This field specifies the amount of time the receiver will wait after entering Phase 2 and sending the new Preset or Coefficient values through the TS1 Ordered Sets before validating the Block Alignment and eventually evaluate the incoming ordered sets (RXEqEval on the PIPE interface asserts). For both Upstream and Downstream Port, this field also specifies the amount of time the receiver will wait after entering Phase 1 before instructing the receiver to adapt to the incoming ordered sets. For Loopback Master: This field specifies the amount of time the receiver will wait after instructing the Loopback Slave to apply a specific Preset through EQ TS1. 0h: 500 ns. 1h: 1 us. 2h: 2 us. 3h: 3 us. 4h: 4 us. : : Fh:15 us.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**EQ TS2 in Recovery.ReceiverConfig Enable (EQTS2IRRC):** EQ TS2 in Recovery.ReceiverConfig Enable(EQTS2IRRC): When set, enables the transmitter to send EQ TS2 in Recovery.RcvrCfg state even when equalization_done_8GT_data_rate variable is 1b, provided that the Downstream Port advertised 8.0 GT/s data rate support in Recovery.RcvrLock, and 8.0 GT/s data rate support has been advertised in the Configuration.Complete or Recovery.RcvrCfg substates by the Upstream Port since exiting the Detect state, and eight consecutive TS1 or TS2 Ordered Sets were received on any configured Lane prior to entry to this substate with speed_change bit set to 1b. When clear, the transmitter can only send EQ TS2 if equalization_done_8GT_data_rate variable is 0b and the Downstream Port advertised 8.0 GT/s data rate support in Recovery.RcvrLock, and 8.0 GT/s data rate support has been advertised in the Configuration.Complete or Recovery.RcvrCfg substates by the Upstream Port since exiting the Detect state, and eight consecutive TS1 or TS2 Ordered Sets were received on any configured Lane prior to entry to this substate with speed_change bit set to 1b. When this bit is used, hardware must ensure that the start_equalization_w_preset variable are in the correct state to ensure that the components on both sides of the link are never out of sync.
6:4	0h RO	**Reserved (RSVD):** Reserved
3	0h RW	**Link EQ Phase 1 Transmit Coefficient Settling Policy (LEQP1TCSP):** Link EQ Phase 1 Transmit Coefficient Settling Policy(LEQP1TCSP): When operating in GEN3 data rate and there is a software/hardware request to re-perform Link Equalization through the Recovery.RcvrLock to Recovery.Equalization arc, PCIe spec requires that the downstream port transmitter switch to the setting specified by the Downstream Port Lane X Transmitter Preset registers in Phase 1. This switching is happening while the downstream port is still actively transmitting TS1 and the upstream port is only required to sample 2 TS1 to determine the next sub-state to transition to. Since the new coefficient setting can take up to 256 ns to settle, the 2 TS1 sampled by the upstream port may be incorrect causing the two LTSSM to be out of sync. When this bit is set, the RP will continue to send EIEOS until the local transmitter setting has settled (specified by PHYCTL2.TXCFGCHGWAIT) before sending TS1 as required in Recovery.Equalization Phase 1. When this bit is clear, the RP will send TS1 with EC = 01 in Recovery.Equalization Phase 1 even though the transmitter setting is still settling.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Multi-Fragment Linear and Nine-Tile List Enable (MFLNTL):** Multi-Fragment Linear and Nine-Tile List Enable(MFLNTL): When set in Hardware Autonomous Linear Preset/Coefficient Search mode, the full Preset/Coefficient List will be traversed in multiple fragments, where each fragments is done in separate entry to Recovery. This is used in the case where a longer dwelling time is required for a particular Preset/Coefficient (configured through EQCFG2.PCET). Subsequent Preset/Coefficient entries within the list that could not be covered within that Recovery session will be covered in subsequent re-entries into Recovery. When set in Hardware Autonomous Nine-Tiles Search mode, the 9-tiles list that could not be covered within that Recovery session will be covered in subsequent re-entries into Recovery.
1	1h RW	**Transmitter Use Preset Policy (TUPP):** Transmitter Use Preset Policy(TUPP): This field applies to the Link Equalization Phase where the local transmitter setting is being adjusted. When set, the transmitted TS1 Use Preset bit will be set if the remote device requests the local transmitter to apply specific Preset(instead of Coefficient). When clear, the Use Preset bit will not be set in this case. Note: This bit must be set before changing speed to GEN3 data rate.
0	0h RW	**Receiver Use Preset Policy (RUPP):** Receiver Use Preset Policy(RUPP): This field applies to the Link Equalization Phase where the remote transmitter setting is being adjusted. When set, the received TS1 Use Preset bit will be checked. When clear, the Use Preset bit in the received TS1 will be ignored. Note: This bit must be set before changing speed to GEN3 data rate.

17.5.85 Remote Transmitter Preset Coefficient List 1 (RTPCL1)—Offset 454h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Preset/Coefficient Mode (PCM):** Preset/Coefficient Mode (PCM): This bit defines whether the Preset List or Coefficient List should be sent to the remote TX to adjust the remote TX setting. For Downstream Port, this is used in Phase 3 of the Link Equalization. For Upstream Port, this is used in Phase 2 of the Link Equalization. The list of coefficient or preset is configurable through the Remote Transmitter Preset Coefficient List [lb]1:4[rb] registers. When this bit is set, Coefficient Mode is enabled and the Remote Transmitter Preset Coefficient List [lb]1:4[rb] registers contain the Coefficient List. When this bit is clear, Preset Mode is enabled and the Remote Transmitter Preset Coefficient List [lb]1:3[rb] registers contain the Preset List.
30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 2/Preset List 4 (RTPRECL2PL4):** Remote Transmitter Pre-Cursor Coefficient List 2/Preset List 4 (RTPRECL2PL4): For Downstream Port: This field defines the pre-cursor coefficient List 2 or Preset List 4 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 2 or Preset List 4 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Remote Transmitter Post-Cursor Coefficient List 1/Preset List 3 (RTPOSTCL1PL3):** Remote Transmitter Post-Cursor Coefficient List 1/Preset List 3 (RTPOSTCL1PL3): For Downstream Port: This field defines the post-cursor coefficient List 1 or Preset List 3 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 1 or Preset List 3 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
17:12	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 1/Preset List 2 (RTPRECL1PL2):** Remote Transmitter Pre-Cursor Coefficient List 1/Preset List 2 (RTPRECL1PL2): For Downstream Port: This field defines the pre-cursor coefficient List 1 or Preset List 2 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 1 or Preset List 2 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Remote Transmitter Post-Cursor Coefficient List 0/Preset List 1 (RTPOSTCL0PL1):** Remote Transmitter Post-Cursor Coefficient List 0/Preset List 1 (RTPOSTCL0PL1): For Downstream Port: This field defines the post-cursor coefficient List 0 or Preset List 1 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 0 or Preset List 1 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
5:0	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 0/Preset List 0 (RTPRECL0PL0):** Remote Transmitter Pre-Cursor Coefficient List 0/Preset List 0 (RTPRECL0PL0): For Downstream Port: This field defines the pre-cursor coefficient List 0 or Preset List 0 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 0 or Preset List 0 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.5.86 Remote Transmitter Preset Coefficient List 2 (RTPCL2)—Offset 458h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Remote Transmitter Post-Cursor Coefficient List 4/Preset List 9 (RTPOSTCL4PL9):** Remote Transmitter Post-Cursor Coefficient List 4/Preset List 9(RTPOSTCL4PL9): For Downstream Port: This field defines the post-cursor coefficient List 4 or Preset List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 4 or Preset List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 4/Preset List 8 (RTPRECL4PL8):** Remote Transmitter Pre-Cursor Coefficient List 4/Preset List 8 (RTPRECL4PL8): For Downstream Port: This field defines the pre-cursor coefficient List 4 or Preset List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 4 or Preset List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Post-Cursor Coefficient List 3/Preset List 7 (RTPOSTCL3PL7):** Remote Transmitter Post-Cursor Coefficient List 3/Preset List 7 (RTPOSTCL3PL7): For Downstream Port: This field defines the post-cursor coefficient List 3 or Preset List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 3 or Preset List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 3/Preset List 6 (RTPRECL3PL6):** Remote Transmitter Pre-Cursor Coefficient List 3/Preset List 6 (RTPRECL3PL6): For Downstream Port: This field defines the pre-cursor coefficient List 3 or Preset List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 3 or Preset List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Post-Cursor Coefficient List 2/Preset List 5 (RTPOSTCL2PL5):** Remote Transmitter Post-Cursor Coefficient List 2/Preset List 5 (RTPOSTCL2PL5): For Downstream Port: This field defines the post-cursor coefficient List 2 or Preset List 5 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 2 or Preset List 5 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.5.87 Remote Transmitter Preset Coefficient List 3 (RTPCL3)—Offset 45Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 7 (RTPRECL7):** Remote Transmitter Pre-Cursor Coefficient List 7 (RTPRECL7): For Downstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Post-Cursor Coefficient List 6 (RTPOSTCL6):** Remote Transmitter Post-Cursor Coefficient List 6 (RTPOSTCL6): For Downstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 6 (RTPRECL6):** Remote Transmitter Pre-Cursor Coefficient List 6 (RTPRECL6): For Downstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Post-Cursor Coefficient List 5 (RTPOSTCL5):** Remote Transmitter Post-Cursor Coefficient List 5 (RTPOSTCL5): For Downstream Port: This field defines the pre-cursor coefficient List 5 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 5 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 5/Preset List 10 (RTPRECL5PL10):** Remote Transmitter Pre-Cursor Coefficient List 5/Preset List 10 (RTPRECL5PL10): For Downstream Port: This field defines the pre-cursor coefficient List 5 or Preset List 10 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 5 or Preset List 10 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.5.88 Remote Transmitter Preset Coefficient List 4 (RTPCL4)—Offset 460h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Remote Transmitter Post-Cursor Coefficient List 9 (RTPOSTCL9):** Remote Transmitter Post-Cursor Coefficient List 9 (RTPOSTCL9): For Downstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 9 (RTPRECL9):** Remote Transmitter Pre-Cursor Coefficient List 9 (RTPRECL9): For Downstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Post-Cursor Coefficient List 8 (RTPOSTCL8):** Remote Transmitter Post-Cursor Coefficient List 8 (RTPOSTCL8): For Downstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 8 (RTPRECL8):** Remote Transmitter Pre-Cursor Coefficient List 8 (RTPRECL8): For Downstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Post-Cursor Coefficient List 7 (RTPOSTCL7):** Remote Transmitter Post-Cursor Coefficient List 7 (RTPOSTCL7): For Downstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.5.89 Figure Of Merit Status (FOMS)—Offset 464h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved
30:29	0h RW	**Index (I):** Index (I): The FOMV field will reflect the Figure of Merit Scoreboard value for the index specified by this field. List N below refers to the Figure of Merit values captured in the scoreboard corresponding to the Preset or Coefficient List N. 00b: Index 0 =[gt] {List 2, List 1, List 0}. 01b: Index 1 =[gt] {List 5, List 4, List 3}. 10b: Index 2 =[gt] {List 8, List 7, List 6}. 11b: Index 3 =[gt] {Rsvd, List 10, List 9}.

Bit Range	Default & Access	Field Name (ID): Description
28:24	0h RW	**Lane Number (LN):** Lane Number (LN): The FOMV field will reflect the Figure of Merit Scoreboard value for the lane specified by this field. 00000b: Lane 0. 00001b: Lane 1. 00010b: Lane 2. 00011b: Lane 3. Others: Reserved.
23:0	0h RO/V	**Figure of Merit Scoreboard Value (FOMSV):** Figure of Merit Scoreboard Value (FOMSV): This field will reflect the Figure of Merit Scoreboard entries referenced by the Lane Number and Index field in this register. For example, when Index == 00b, this field will reflect the Figure of Merit values for Lane specified in Lane Number field and the encoding of this field is as shown below: 23:16: Figure of Merit for Preset/Coefficient List 2. 15:8 : Figure of Merit for Preset/Coefficient List 1. 7:0 : Figure of Merit for Preset/Coefficient List 0. If the Receiver Eye Width margining completes with error, the value of Figure of Merit should reflect 0x00.

17.5.90 Hardware Autonomous Equalization Control (HAEQ)—Offset 468h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: A0080E00h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Ah RW	**Hardware Autonomous Preset/Coefficient Count Per-Iteration (HAPCCPI):** Hardware Autonomous Preset/Coefficient Count Per-Iteration(HAPCCPI): This field defines the number of Preset/Coefficient to be traversed for every iteration of Recovery Equalization. For the Linear Mode, EQCFG2.HAPCSB specifies the total number of Presets/Coefficients to be checked in total while this field specifies the number of Presets/Coefficients to be checked per-iteration of Recovery Equalization. Hardware will enter Recovery Equalization and check the number of Presets/Coefficients specified by this field. Once that is done, hardware will exit Recovery Equalization and trigger another entry to Recovery Equalization to check another set of Presets/Coefficients. This goes on until the total number of Presets/Coefficients are checked. For Nine-Tiles Mode, EQCFG2.NTIC specifies the number of 9-tiles iterations, which indirectly specifies the total number of Presets/ Coefficients to be checked in total. Similar to Linear Mode, this field specifies the number of Presets/Coefficients to be checked per-iteration of Recovery Equalization. 0h: 1 Preset/Coefficient per-iteration. 1h: 2 Preset/Coefficient per-iteration. 2h: 3 Preset/Coefficient per-iteration. ... 9h: 10 Preset/Coefficient per-iteration. Ah: 11 Preset/Coefficient per-iteration. Others: Reserved.
27:20	0h RW	**FOM Error Mask (FOMEM):** FOM Error Mask(FOMEM): The FOM error counter will be masked(thus ignoring the FOM error) for all the FOM values prior to the FOM value specified in this field. If this field is programmed to 00h, this mechanism is disabled. This bit must be configured before training to GEN3 data rate.

Bit Range	Default & Access	Field Name (ID): Description
19	1h RW	**MAC FOM Control (MACFOMC):** MAC FOM Control(MACFOMC): When set, MAC controls the advancement of the FOM values completely while in the Link Equalization mode. For downstream port, this is done in Phase 3 and for upstream port, this is done in Phase 2 of the Link Equalization. The dwelling time for each of the FOM values are programmed through the remaining fields of this register. When enabled, the hardware will start in Speeding Mode, where it will instruct the PHY to increment the FOM value after the Speeding Latency specified by HAEQ.SL field. Once the FOM value matches HAEQ.SFOMFM, the hardware switches from Speeding Mode to Dwelling Mode. In Dwelling mode, the MAC will instruct PHY to increment the FOM value after the Dwelling Latency specified by HAEQ.DL field. This is done until the link equalization phase is completed. When cleared, PHY controls the advancement of the FOM values completely, during the Link Equalization mode. This bit must be configured before training to GEN3 data rate.
18:16	0h RW	**Speeding Latency (SL):** Speeding Latency(SL): Specifies the residency time for a particular FOM value in Speeding Mode. 000b: 192 ns. 001b: 256 ns. 010b: 512 ns. 011b: 1 us. 100b: 2 us. 101b: 4 us. 110b: 8 us. 111b: 16 us. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.
15:8	Eh RW	**Dwelling Latency (DL):** Dwelling Latency(DL): Specifies the residency time for a particular FOM value in Dwelling Mode. 00h: 2 us. 01h: 4 us. 02h: 6 us. ... FFh: 512 us. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Starting FOM For Margining (SFOMFM):** Starting FOM For Margining(SFOMFM): Define the FOM where MAC switches from Speeding Mode to Dwelling Mode after hitting the programmed FOM value in Hardware Autonomous Preset/Coefficient mode. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.

17.5.91 Local Transmitter Coefficient Override 1 (LTCO1)—Offset 470h

Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane bits are not used.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD):** Reserved
25	0h RW	**Lane 1 Transmitter Coefficient Override Enable (L1TCOE):** Lane 1 Transmitter Coefficient Override Enable (L1TCOE): When set, the transmitter coefficient override values LTPCO1.L1TPRECO and LTPCO1.L1TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO1.L1TPRECO and LTPCO1.L1TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Lane 0 Transmitter Coefficient Override Enable (L0TCOE):** Lane 0 Transmitter Coefficient Override Enable (L0TCOE): When set, the transmitter coefficient override values LTPCO1.L0TPRECO and LTPCO1.L0TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO1.L0TPRECO and LTPCO1.L0TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
23:18	0h RW	**Lane 1 Transmitter Post-Cursor Coefficient Override (L1TPOSTCO):** Lane 1 Transmitter Post-Cursor Coefficient Override (L1TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L1TCOE = 1.
17:12	0h RW	**Lane 1 Transmitter Pre-Cursor Coefficient Override (L1TPRECO):** Lane 1 Transmitter Pre-Cursor Coefficient Override (L1TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L1TCOE = 1.
11:6	0h RW	**Lane 0 Transmitter Post-Cursor Coefficient Override (L0TPOSTCO):** Lane 0 Transmitter Post-Cursor Coefficient Override (L0TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L0TCOE = 1.
5:0	0h RW	**Lane 0 Transmitter Pre-Cursor Coefficient Override (L0TPRECO):** Lane 0 Transmitter Pre-Cursor Coefficient Override (L0TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L0TCOE = 1.

17.5.92 Local Transmitter Coefficient Override 2 (LTCO2)—Offset 474h

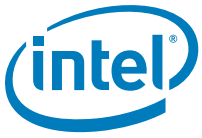
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane bits are not used.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD):** Reserved
25	0h RW	**Lane 3 Transmitter Coefficient Override Enable (L3TCOE):** Lane 3 Transmitter Coefficient Override Enable (L3TCOE): When set, the transmitter coefficient override values LTPCO2.L3TPRECO and LTPCO2.L3TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO2.L3TPRECO and LTPCO2.L3TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
24	0h RW	**Lane 2 Transmitter Coefficient Override Enable (L2TCOE):** Lane 2 Transmitter Coefficient Override Enable (L2TCOE): When set, the transmitter coefficient override values LTPCO2.L2TPRECO and LTPCO2.L2TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO2.L2TPRECO and LTPCO2.L2TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.



Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Lane 3 Transmitter Post-Cursor Coefficient Override (L3TPOSTCO):** Lane 3 Transmitter Post-Cursor Coefficient Override (L3TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L3TCOE = 1.
17:12	0h RW	**Lane 3 Transmitter Pre-Cursor Coefficient Override (L3TPRECO):** Lane 3 Transmitter Pre-Cursor Coefficient Override (L3TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L3TCOE = 1
11:6	0h RW	**Lane 2 Transmitter Post-Cursor Coefficient Override (L2TPOSTCO):** Lane 2 Transmitter Post-Cursor Coefficient Override (L2TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L2TCOE = 1.
5:0	0h RW	**Lane 2 Transmitter Pre-Cursor Coefficient Override (L2TPRECO):** Lane 2 Transmitter Pre-Cursor Coefficient Override (L2TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L2TCOE = 1.

17.5.93 GEN3 L0s Control (G3L0SCTL)—Offset 478h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: C00281Eh

Bit Range	Default & Access	Field Name (ID): Description
31:24	Ch RW	**Gen3 Active State L0s Preparation Latency (G3ASL0SPL):** Gen3 Active State L0s Preparation Latency (G3ASL0SPL) Determines how long the Link layer has to indicate IDLE before the link initialization and control logic enters L0s 00: 0 clocks (enter immediately) 01: 1 clock ... FF: 255 clocks The value of this register is only used if the Gen3 L0s Entry Idle Control register is set to [quote]11[/quote] and operating in Gen3 mode.
23:22	0h RW	**Gen3 L0s Entry Idle Control (G3L0SIC):** Gen3 L0s Entry Idle Control (G3L0SIC): 00 : Allow entry into L0s after the link has been idle for a period of time equal to of the received N_FTS total entry time (1/4 * N_FTS * 16) 01 : Allow entry into L0s after the link has been idle for for a period of time equal to of the received N_FTS total entry time (1/2 * N_FTS * 16) 10 : Allow entry after the link has been idle for for a period of time equal to the received N_FTS total entry time (N_FTS * 16) 11: Allow entry into L0s after the link has been idle for a period specified in the Gen3 Active State L0s Preparation Latency register. This register is only applied when operating in Gen3 mode.
21:16	0h RO	**Reserved (RSVD):** Reserved
15:8	28h RW	**Gen3 Unique Clock N_FTS (G3UCNFTS):** Gen3 Unique Clock N_FTS (G3UCNFTS): Number of Fast Training Sequence ordered sets required to be transmitted for a root port Receiver to exit L0s in a unique (non-common) clock configuration (LCTL.CCC=0) when operating in Gen3 mode. The N_FTS value is sent in TS1 and TS2 training sets during link training. 00: 0 FTS sets 01: 1 FTS set ... FF: 255 FTS sets Note: When operating in Mobile Express mode, the output of this field is not used to determine the number of FTS to be sent on TXL0s exit. Mobile Express does not support Fast Training Sequence. Instead, SYNC is used to achieve bit lock. However, the output of this field is still used in L0s Entry Idle Control registers to determine the L0s Entry Idle latency.

Bit Range	Default & Access	Field Name (ID): Description
7:0	1Eh RW	**Gen3 Common Clock N_FTS (G3CCNFTS):** Gen3 Common Clock N_FTS (G3CCNFTS): Number of Fast Training Sequence ordered sets required to be transmitted for a root port Receiver to exit L0s in a common clock configuration (LCTL.CCC=1) when operating in Gen3 mode. The N_FTS value is sent in TS1 and TS2 training sets during link training. 00: 0 FTS sets 01: 1 FTS set ... FF: 255 FTS sets Note: When operating in Mobile Express mode, the output of this field is not used to determine the number of FTS to be sent on TXL0s exit. Mobile Express does not support Fast Training Sequence. Instead, SYNC is used to achieve bit lock. However, the output of this field is still used in L0s Entry Idle Control registers to determine the L0s Entry Idle latency.

17.5.94 Equalization Configuration 2 (EQCFG2)—Offset 47Ch

Size:32 bits
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: A001h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Nine-Tiles Iteration Count (NTIC):** Nine-Tiles Iteration Count(NTIC): This field specifies the number of iterations to perform the 9-tiles search. Each iteration involves evaluating the neighboring 9-tiles for the best Preset/Coefficient margin and then use the Preset/Coefficient as the centerpoint to identify and evaluate the next 9-tiles. 00h: 1 iteration. 01h: 2 iterations. 02h: 3 iterations. ... FFh: 256 iterations.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**Equalization Margining Disable (EMD):** Equalization Margining Disable(EMD):When set, the Root Port will not request the PHY to perform Receiver Margining by asserting RxEqEval on each Preset/ Coefficient list traversed. This allows the receiver to still measure the Bit Error Count without margining. When cleared, the Root Port will request the PHY to perform Receiver Margining by asserting RxEqEval. This field is only valid when operating in Hardware Autonomous Preset/Coefficient Search mode. The Preset/Coefficient list will still be traversed to the end.
22:20	0h RW	**Nine-Tiles Step Size (NTSS):** Nine-Tiles Step Size(NTSS): This field specifies the step size used to identify the surrounding 9-tiles to be used for margining. 000b: 1 step. 001b: 2 steps. 010b: 3 steps. 011b: 4 steps. 100b: 5 steps. 101b: 6 steps. 110b: 7 steps. 111b: 8 steps. Each of the steps is measured in terms of incrementing of decrementing the coefficient values.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW	**Preset/Coefficient Evaluation Timeout (PCET):** Preset/ Coefficient Evaluation Timeout(PCET): This field specifies the evaluation timeout for a single Preset/Coefficient in the List when operating in Hardware Autonomous Preset/Coefficient Search mode. By spec, the evaluation phase must be completed before the 24 ms timeout. To support 12 Presets (11 Presets + 1 final good Preset), each Preset will have up to 2 ms for evaluation. This field allows the 2 ms timer to be programmable. This is useful if the EQCFG2.HAPCSB limits the Preset/Coefficient List to smaller than 12 such that each Preset/Coefficient could be evaluated for a time longer than 2 ms. 0h: 2 ms. 1h: 2.5 ms. 2h: 3 ms. 3h: 3.5 ms. 4h: 4 ms. 5h: 4.5 ms. 6h: 5 ms. 7h: 6 ms. 8h: 7 ms. 9h: 8 ms. Ah: 9 ms. Bh:10 ms. Ch:11 ms. Dh:21 ms. Eh:22 ms. Fh:23 ms.
15:12	Ah RW	**Hardware Autonomous Preset/Coefficient Search Bound (HAPCSB):** Hardware Autonomous Preset/Coefficient Search Bound(HAPCSB): This field defines the number of Preset/ Coefficient List to be traversed, out of 11 for Presets or out of 10 for Coefficients. The Preset/Coefficient list will be traversed from List 0 to the value specified by this field in incremental order. This field allows equalization to be done with smaller set of Preset/ Coefficient list and each of the Preset/Coefficient list could be run for a longer time. 0h: Preset/Coefficient List 0 only. 1h: Preset/Coefficient List 0 - 1. 2h: Preset/Coefficient List 0 - 2. : : 9h: Preset/Coefficient List 0 - 9. Ah: Preset List 0 - 10/Coefficient List 0-9. Others: Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Nine-Tiles Equalization Mechanism Enable (NTEME):** Nine-Tiles Equalization Mechanism Enable(NTEME): When set, the Nine-Tiles Equalization Mechanism is enabled when running in Hardware Autonomous Preset/Coefficient Search Mode.
10	0h RW	**Mid-Point Equalization Mechanism Enable (MPEME):** Mid-Point Equalization Mechanism Enable(MPEME): When set, the Mid-Point Equalization Mechanism is enabled when running in Hardware Autonomous Preset/Coefficient Search Mode.
9:8	0h RW	**Receiver Eye Width Margin Error Threshold Multiplier (REWMETM):** Receiver Eye Width Margin Error Threshold Multiplier (REWMETM): This field specifies the multiplier to be used with REWMET field. 00b: Multiply REWMET by 1 (effectively no multiplier). 01b: Multiply REWMET by 10. 10b: Multiply REWMET by 100. 11b: Multiply REWMET by 1000.
7:0	1h RW	**Receiver Eye Width Margin Error Threshold (REWMET):** Receiver Eye Width Margin Error Threshold (REWMET): This field specifies the count threshold which upon exceeded, will cause controller to terminate the current iteration of Receiver Eye Width Margining and move on to the next preset or coefficient in the list. The value specified in this field will need to be multiplied with the multiplier specified in REWMETM field to get the final threshold values. 00h: Terminate on 1 x REWMETM errors. 01h: Terminate on 2 x REWMETM errors. 02h: Terminate on 4 x REWMETM errors. 03h: Terminate on 6 x REWMETM errors. : : FEh: Terminate on 508 x REWMETM errors. FFh: Never terminate. Rely on PHY to terminate the margining.

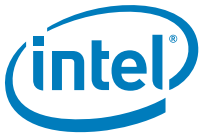
17.5.95 Monitor Mux (MM)—Offset 480h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO/V	**Monitor Signal State (MSST):** Monitor Signal State(MSST): The internal signal groupings selected by MM.MSS field is reflected in this field. The intention of this monitor signal is provide software a capability to monitor some of the GEN3 related parameters accumulated by the controller through the Link Equalization that are too costly to be mapped to dedicated registers. Implementation MUST NEVER expose any security related information through this Monitor Mux.
7:0	0h RW	**Monitor Signal Select (MSS):** Monitor Signal Select(MSS): This field is essentially the mux select for the Monitor Signal mux. Setting this field allows different monitor signals to be muxed out and readable by software through the MM.MSST field.

17.5.96 Lane0 P0 and P1 Preset-Coefficient Mapping (L0P0P1PCM)—Offset 500h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.97 Lane0 P1, P2 and P3 Preset-Coefficient Mapping (L0P1P2P3PCM)—Offset 504h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.98 Lane0 P3 and P4 Preset-Coefficient Mapping (L0P3P4PCM)—Offset 508h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

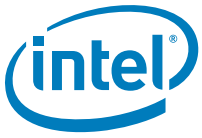
17.5.99 Lane0 P5 and P6 Preset-Coefficient Mapping (L0P5P6PCM)—Offset 50Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.100 Lane0 P6, P7 and P8 Preset-Coefficient Mapping (L0P6P7P8PCM)—Offset 510h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.101 Lane0 P8 and P9 Preset-Coefficient Mapping (L0P8P9PCM)—Offset 514h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.102 Lane0 P10 Preset-Coefficient Mapping (L0P10PCM)—Offset 518h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.103 Lane0 LF and FS (L0LFFS)—Offset 51Ch

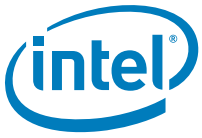
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.104 Lane1 P0 and P1 Preset-Coefficient Mapping (L1P0P1PCM)—Offset 520h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.105 Lane1 P1, P2 and P3 Preset-Coefficient Mapping (L1P1P2P3PCM)—Offset 524h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.106 Lane1 P3 and P4 Preset-Coefficient Mapping (L1P3P4PCM)—Offset 528h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.107 Lane1 P5 and P6 Preset-Coefficient Mapping (L1P5P6PCM)—Offset 52Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.108 Lane1 P6, P7 and P8 Preset-Coefficient Mapping (L1P6P7P8PCM)—Offset 530h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.109 Lane1 P8 and P9 Preset-Coefficient Mapping (L1P8P9PCM)—Offset 534h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.110 Lane1 P10 Preset-Coefficient Mapping (L1P10PCM)—Offset 538h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.111 Lane1 LF and FS (L1LFFS)—Offset 53Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.112 Lane2 P0 and P1 Preset-Coefficient Mapping (L2P0P1PCM)—Offset 540h

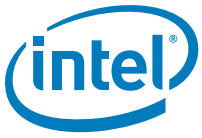
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.113 Lane2 P1, P2 and P3 Preset-Coefficient Mapping (L2P1P2P3PCM)—Offset 544h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.114 Lane2 P3 and P4 Preset-Coefficient Mapping (L2P3P4PCM)—Offset 548h

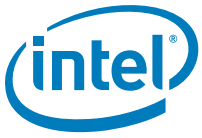
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.115 Lane2 P5 and P6 Preset-Coefficient Mapping (L2P5P6PCM)—Offset 54Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.116 Lane2 P6, P7 and P8 Preset-Coefficient Mapping (L2P6P7P8PCM)—Offset 550h

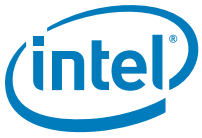
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.117 Lane2 P8 and P9 Preset-Coefficient Mapping (L2P8P9PCM)—Offset 554h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.118 Lane2 P10 Preset-Coefficient Mapping (L2P10PCM)—Offset 558h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.119 Lane2 LF and FS (L2LFFS)—Offset 55Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.120 Lane3 P0 and P1 Preset-Coefficient Mapping (L3P0P1PCM)—Offset 560h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.121 Lane3 P1, P2 and P3 Preset-Coefficient Mapping (L3P1P2P3PCM)—Offset 564h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.122 Lane3 P3 and P4 Preset-Coefficient Mapping (L3P3P4PCM)—Offset 568h

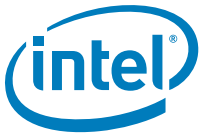
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.123 Lane3 P5 and P6 Preset-Coefficient Mapping (L3P5P6PCM)—Offset 56Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.124 Lane3 P6, P7 and P8 Preset-Coefficient Mapping (L3P6P7P8PCM)—Offset 570h

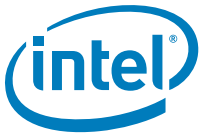
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.125 Lane3 P8 and P9 Preset-Coefficient Mapping (L3P8P9PCM)—Offset 574h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.126 Lane3 P10 Preset-Coefficient Mapping (L3P10PCM)—Offset 578h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.5.127 Lane3 LF and FS (L3LFFS)—Offset 57Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6 Registers Summary

Table 17-6. Summary of pcie_cfg Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4h	7h	Device Command; Primary Status (CMD_PSTS)—Offset 4h	100000h
8h	Bh	Revision ID;Class Code (RID_CC)—Offset 8h	60400F0h
Ch	Fh	Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch	810000h
18h	1Bh	Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h	0h
1Ch	1Fh	I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch	0h
20h	23h	Memory Base and Limit (MBL)—Offset 20h	0h
24h	27h	Prefetchable Memory Base and Limit (PMBL)—Offset 24h	10001h
28h	2Bh	Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h	0h
2Ch	2Fh	Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch	0h
34h	37h	Capabilities List Pointer (CAPP)—Offset 34h	40h
3Ch	3Fh	Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch	0h
40h	43h	Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h	428010h
44h	47h	Device Capabilities (DCAP)—Offset 44h	8001h
48h	4Bh	Device Control; Device Status (DCTL_DSTS)—Offset 48h	100000h
4Ch	4Fh	Link Capabilities (LCAP)—Offset 4Ch	710C00h
50h	53h	Link Control; Link Status (LCTL_LSTS)—Offset 50h	10000h
54h	57h	Slot Capabilities (SLCAP)—Offset 54h	40060h
58h	5Bh	Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h	0h
5Ch	5Fh	Root Control (RCTL)—Offset 5Ch	0h
60h	63h	Root Status (RSTS)—Offset 60h	0h
64h	67h	Device Capabilities 2 (DCAP2)—Offset 64h	80837h
68h	6Bh	Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h	0h
6Ch	6Fh	Link Capabilities 2 (LCAP2)—Offset 6Ch	0h
70h	73h	Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h	0h
74h	77h	Slot Capabilities 2 (SLCAP2)—Offset 74h	0h

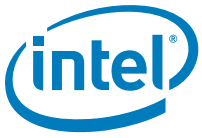


Table 17-6. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
78h	7Bh	Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h	0h
80h	83h	Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h	9005h
88h	8Bh	Message Signaled Interrupt Message Data (MD)—Offset 88h	0h
90h	93h	Subsystem Vendor Capability (SVCAP)—Offset 90h	A00Dh
94h	97h	Subsystem Vendor IDs (SVID)—Offset 94h	0h
A0h	A3h	Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h	C8030001h
A4h	A7h	PCI Power Management Control And Status (PMCS)—Offset A4h	8h
D4h	D7h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	800h
E4h	E7h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	0h
100h	103h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	0h
104h	107h	Uncorrectable Error Status (UES)—Offset 104h	0h
108h	10Bh	Uncorrectable Error Mask (UEM)—Offset 108h	0h
10Ch	10Fh	Uncorrectable Error Severity (UEV)—Offset 10Ch	60011h
110h	113h	Correctable Error Status (CES)—Offset 110h	0h
114h	117h	Correctable Error Mask (CEM)—Offset 114h	2000h
118h	11Bh	Advanced Error Capabilities and Control (AECC)—Offset 118h	0h
11Ch	11Fh	Header Log DW1 (HL_DW1)—Offset 11Ch	0h
120h	123h	Header Log DW2 (HL_DW2)—Offset 120h	0h
124h	127h	Header Log DW3 (HL_DW3)—Offset 124h	0h
128h	12Bh	Header Log DW4 (HL_DW4)—Offset 128h	0h
12Ch	12Fh	Root Error Command (REC)—Offset 12Ch	0h
134h	137h	Error Source Identification (ESID)—Offset 134h	0h
140h	143h	ACS Extended Capability Header (ACSECH)—Offset 140h	0h
144h	147h	ACS Capability Register (ACSCAPR)—Offset 144h	Fh
148h	14Bh	ACS Control Register (ACSCTLR)—Offset 148h	0h
150h	153h	PTM Extended Capability Header (PTMECH)—Offset 150h	0h
154h	157h	PTM Capability Register (PTMCAPR)—Offset 154h	400h
158h	15Bh	PTM Control Register (PTMCTLR)—Offset 158h	0h
200h	203h	L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h	0h
204h	207h	L1 Sub-States Capabilities (L1SCAP)—Offset 204h	28281Fh
208h	20Bh	L1 Sub-States Control 1 (L1SCTL1)—Offset 208h	0h
20Ch	20Fh	L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch	28h
220h	223h	Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h	0h
224h	227h	Link Control 3 (LCTL3)—Offset 224h	0h
228h	22Bh	Lane Error Status (LES)—Offset 228h	0h
22Ch	22Fh	Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch	7F7F7F7Fh

Table 17-6. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
230h	233h	Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h	7F7F7F7Fh
300h	303h	PCI Express Replay Timer Policy 1 (PCIERTP1)—Offset 300h	A64F96h
304h	307h	PCI Express Replay Timer Policy 2 (PCIERTP2)—Offset 304h	1BC00B86h
314h	317h	PCI Express Status 1 (PCIESTS1)—Offset 328h	54262A13h
328h	32Bh	PCI Express Status 1 (PCIESTS1)—Offset 328h	0h
32Ch	32Fh	PCI Express Status 2 (PCIESTS2)—Offset 32Ch	0h
330h	333h	PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h	2A000016h
334h	337h	PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h	4ABCB5BCh
390h	393h	PTM Propagation Delay (PTMPD)—Offset 390h	0h
394h	397h	PTM Lower Local Master Time (PTMLLMT)—Offset 394h	0h
398h	39Bh	PTM Upper Local Master Time (PTMULMT)—Offset 398h	0h
39Ch	39Fh	PTM Pipe Stage Delay Configuration 1 (PTMPSDC1)—Offset 39Ch	0h
3A0h	3A3h	PTM Pipe Stage Delay Configuration 2 (PTMPSDC2)—Offset 3A0h	0h
3A4h	3A7h	PTM Pipe Stage Delay Configuration 3 (PTMPSDC3)—Offset 3A4h	0h
3A8h	3ABh	PTM Pipe Stage Delay Configuration 4 (PTMPSDC4)—Offset 3A8h	0h
3ACh	3AFh	PTM Pipe Stage Delay Configuration 5 (PTMPSDC5)—Offset 3ACh	0h
3B0h	3B3h	PTM Extended Config (PTMECFG)—Offset 3B0h	0h
3B4h	3B7h	PTM Lower T2 Time Stamp (PTMLT2TSTMP)—Offset 3B4h	0h
3B8h	3BBh	PTM Upper T2 Time Stamp (PTMUT2TSTMP)—Offset 3B8h	0h
414h	417h	Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h	0h
418h	41Bh	Thermal and Power Throttling (TNPT)—Offset 418h	930h
41Ch	41Fh	Dynamic Lane Switch (DYNLNSW)—Offset 41Ch	0h
420h	423h	Power Control Enable (PCE)—Offset 428h	2AE8146h
428h	42Bh	Power Control Enable (PCE)—Offset 428h	9h
42Ch	42Fh	PGCB Control1 (PGCBCTL1)—Offset 42Ch	14155555h
430h	433h	PGCB Control2 (PGCBCTL2)—Offset 430h	54h
450h	453h	Equalization Configuration 1 (EQCFG1)—Offset 450h	3102h
454h	457h	Remote Transmitter Preset Coefficient List 1 (RTPCL1)—Offset 454h	0h
458h	45Bh	Remote Transmitter Preset Coefficient List 2 (RTPCL2)—Offset 458h	0h
45Ch	45Fh	Remote Transmitter Preset Coefficient List 3 (RTPCL3)—Offset 45Ch	0h
460h	463h	Remote Transmitter Preset Coefficient List 4 (RTPCL4)—Offset 460h	0h
464h	467h	Figure Of Merit Status (FOMS)—Offset 464h	0h
468h	46Bh	Hardware Autonomous Equalization Control (HAEQ)—Offset 468h	A0080E00h
470h	473h	Local Transmitter Coefficient Override 1 (LTCO1)—Offset 470h	0h
474h	477h	Local Transmitter Coefficient Override 2 (LTCO2)—Offset 474h	0h
478h	47Bh	GEN3 L0s Control (G3L0SCTL)—Offset 478h	C00281Eh
47Ch	47Fh	Equalization Configuration 2 (EQCFG2)—Offset 47Ch	A001h
480h	483h	Monitor Mux (MM)—Offset 480h	0h
500h	503h	Lane0 P0 and P1 Preset-Coefficient Mapping (L0P0P1PCM)—Offset 500h	0h

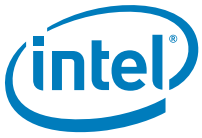


Table 17-6. Summary of pcie_cfg Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
504h	507h	Lane0 P1, P2 and P3 Preset-Coefficient Mapping (L0P1P2P3PCM)—Offset 504h	0h
508h	50Bh	Lane0 P3 and P4 Preset-Coefficient Mapping (L0P3P4PCM)—Offset 508h	0h
50Ch	50Fh	Lane0 P5 and P6 Preset-Coefficient Mapping (L0P5P6PCM)—Offset 50Ch	0h
510h	513h	Lane0 P6, P7 and P8 Preset-Coefficient Mapping (L0P6P7P8PCM)—Offset 510h	0h
514h	517h	Lane0 P8 and P9 Preset-Coefficient Mapping (L0P8P9PCM)—Offset 514h	0h
518h	51Bh	Lane0 P10 Preset-Coefficient Mapping (L0P10PCM)—Offset 518h	0h
51Ch	51Fh	Lane0 LF and FS (L0LFFS)—Offset 51Ch	0h
520h	523h	Lane1 P0 and P1 Preset-Coefficient Mapping (L1P0P1PCM)—Offset 520h	0h
524h	527h	Lane1 P1, P2 and P3 Preset-Coefficient Mapping (L1P1P2P3PCM)—Offset 524h	0h
528h	52Bh	Lane1 P3 and P4 Preset-Coefficient Mapping (L1P3P4PCM)—Offset 528h	0h
52Ch	52Fh	Lane1 P5 and P6 Preset-Coefficient Mapping (L1P5P6PCM)—Offset 52Ch	0h
530h	533h	Lane1 P6, P7 and P8 Preset-Coefficient Mapping (L1P6P7P8PCM)—Offset 530h	0h
534h	537h	Lane1 P8 and P9 Preset-Coefficient Mapping (L1P8P9PCM)—Offset 534h	0h
538h	53Bh	Lane1 P10 Preset-Coefficient Mapping (L1P10PCM)—Offset 538h	0h
53Ch	53Fh	Lane1 LF and FS (L1LFFS)—Offset 53Ch	0h
540h	543h	Lane2 P0 and P1 Preset-Coefficient Mapping (L2P0P1PCM)—Offset 540h	0h
544h	547h	Lane2 P1, P2 and P3 Preset-Coefficient Mapping (L2P1P2P3PCM)—Offset 544h	0h
548h	54Bh	Lane2 P3 and P4 Preset-Coefficient Mapping (L2P3P4PCM)—Offset 548h	0h
54Ch	54Fh	Lane2 P5 and P6 Preset-Coefficient Mapping (L2P5P6PCM)—Offset 54Ch	0h
550h	553h	Lane2 P6, P7 and P8 Preset-Coefficient Mapping (L2P6P7P8PCM)—Offset 550h	0h
554h	557h	Lane2 P8 and P9 Preset-Coefficient Mapping (L2P8P9PCM)—Offset 554h	0h
558h	55Bh	Lane2 P10 Preset-Coefficient Mapping (L2P10PCM)—Offset 558h	0h
55Ch	55Fh	Lane2 LF and FS (L2LFFS)—Offset 55Ch	0h
560h	563h	Lane3 P0 and P1 Preset-Coefficient Mapping (L3P0P1PCM)—Offset 560h	0h
564h	567h	Lane3 P1, P2 and P3 Preset-Coefficient Mapping (L3P1P2P3PCM)—Offset 564h	0h
568h	56Bh	Lane3 P3 and P4 Preset-Coefficient Mapping (L3P3P4PCM)—Offset 568h	0h
56Ch	56Fh	Lane3 P5 and P6 Preset-Coefficient Mapping (L3P5P6PCM)—Offset 56Ch	0h
570h	573h	Lane3 P6, P7 and P8 Preset-Coefficient Mapping (L3P6P7P8PCM)—Offset 570h	0h
574h	577h	Lane3 P8 and P9 Preset-Coefficient Mapping (L3P8P9PCM)—Offset 574h	0h
578h	57Bh	Lane3 P10 Preset-Coefficient Mapping (L3P10PCM)—Offset 578h	0h
57Ch	57Fh	Lane3 LF and FS (L3LFFS)—Offset 57Ch	0h

17.6.1 Device Command; Primary Status (CMD_PSTS)—Offset 4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**DPE - Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if CMD.PERE is not set.
30	0h RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
26:25	0h RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved per PCI-Express spec
24	0h RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and CMD.PERE is set.
23	0h RO	**Primary Fast Back to Back Capable (PFBC):** Reserved per PCI-Express spec.
22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Primary 66 MHz Capable (PC66):** Reserved per PCI-Express spec.
20	1h RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list.
19	0h RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID.
18:16	0h RO	**Reserved (RSVD_1):** Reserved
15:11	0h RO	**Reserved (RSVD_2):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec.
8	0h RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0h RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec.
6	0h RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** Reserved per PCI-Express spec.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec.
3	0h RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec.
2	0h RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0h RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0h RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone..

17.6.2 Revision ID;Class Code (RID_CC)—Offset 8h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 60400F0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	6h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	4h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h.
15:8	0h RO/V	**Programming Interface (PI):** The value reported in this register is a function of the Decode Control.Subtractive Decode Enable (SDE) register. SDE Value reported in this register 0: 00h 1: 01h
7:0	F0h RO/V	**Revision ID (RID):** Indicates the revision of the bridge.

17.6.3 Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 810000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved
23	1h RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device.
22:16	1h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h.
15:11	0h RO	**Latency Count (CT):** Reserved per PCI-Express spec
10:8	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec

17.6.4 Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V2	**Secondary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	0h RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.
15:8	0h RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port.
7:0	0h RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

17.6.5 I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
30	0h RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with 'Unsupported Request' status from the device.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with 'Completion Abort' status from the device.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with 'Completion Abort' status to the device.
26:25	0h RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.
23	0h RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec
20:16	0h RO	**Reserved (RSVD_1):** Reserved
15:12	0h RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing.

17.6.6 Memory Base and Limit (MBL)—Offset 20h

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is MB [gt]= AD[lb]31:20[rb] [lt]= ML.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	0h RO	**Reserved (RSVD):** Reserved
15:4	0h RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	0h RO	**Reserved (RSVD_1):** Reserved

17.6.7 Prefetchable Memory Base and Limit (PMBL)—Offset 24h

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB [gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 10001h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing.
15:4	0h RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	1h RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing.

17.6.8 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.

17.6.9 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

17.6.10 Capabilities List Pointer (CAPP)—Offset 34h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 40h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	40h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) OffsetCapability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI) 90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List OffsetCapability Next Pointer 100h Advanced Error Reporting 000h

17.6.11 Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch

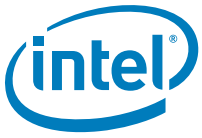
Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD):** Reserved
27	0h RW/V2	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
26	0h RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set.
25	0h RW/V2	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW/V2	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
23	0h RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec.
22	0h RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port.
21	0h RW/V2	**Master Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
20	0h RW	**VGA 16-Bit Decode (V16):** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.
19	0h RW	**VGA Enable (VE):** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h 3BBh and 3C0h 3DFh, and all aliases of bits 15:10 in any combination of 1's
18	0h RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
17	0h RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
16	0h RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG register in chipset config space: Port Bits[lb]15:12[rb] Bits[lb]11:08[rb] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP 4 0h STRPFUSECFG.P4IP 5 0h STRPFUSECFG.P5IP 6 0h STRPFUSECFG.P6IP 7 0h STRPFUSECFG.P7IP 8 0h STRPFUSECFG.P8IP The value that is programmed into STRPFUSECFG.PxIP is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above.
7:0	0h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

17.6.12 Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 428010h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved
30	0h RO	**Reserved (RSVD_1):** Reserved. This register at one time was for TCS Routing but that was later removed from the PCIe 2.0 spec
29:25	0h RO	**Interrupt Message Number (IMN):** The root port does not have multiple MSI interrupt numbers.
24	0h RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
23:20	4h RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port

Bit Range	Default & Access	Field Name (ID): Description
19:16	2h RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 specification which incorporates the Register Expansion ECN.
15:8	80h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h RO	**Capability ID (CID):** Indicates this is a PCI Express capability

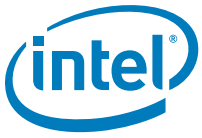
17.6.13 Device Capabilities (DCAP)—Offset 44h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 8001h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD):** Reserved
28	0h RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports
27:26	0h RO	**Captured Slot Power Limit Scale (CSPS):** Not supported
25:18	0h RO	**Captured Slot Power Limit Value (CSPV):** Not supported
17:16	0h RO	**Reserved (RSVD_1):** Reserved
15	1h RO	**Role Based Error Reporting (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.
14	0h RO	**Reserved (RSVD_2):** Reserved. On previous version of the specification this was Power Indicator Present (PIP)
13	0h RO	**Reserved (RSVD_3):** Reserved. On previous version of the specification this was Attention Indicator Present (AIP)



Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**Reserved (RSVD_4):** Reserved. On previous version of the specification this was Attention Button Present (ABP)
11:9	0h RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports.
8:6	0h RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port.
5	0h RO	**Extended Tag Field Supported (ETFS):** The root port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	0h RO	**Phantom Functions Supported (PFS):** No phantom functions supported
2:0	1h RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Only Max Payload Size of up to 256B is supported. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface.

17.6.14 Device Control; Device Status (DCTL_DSTS)—Offset 48h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
20	1h RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
18	0h RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp
17	0h RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout
16	0h RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout.
15	0h RO	**Reserved (RSVD_1):** Reserved
14:12	0h RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface.
11	0h RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.
10	0h RW/P	**Aux Power PM Enable (APME):** The OS will set this bit to '1' if the device connected has detected aux power.
9	0h RO	**Phantom Functions Enable (PFE):** Not supported
8	0h RO	**Extended Tag Field Enable (ETFE):** Not supported
7:5	0h RW	**Max Payload Size (MPS):** The root port only supports up to 256B max payload. Programming this field to any values other than 128B or 256B max payload size will result in aliasing to 128B max payload size. If the DCAP.MPS indicates 128B max payload size support, programming this field to any values other than 128B will result in aliasing to 128B max payload size. Programming this field to any values greater than DCAP.MPS will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME.
4	0h RO	**Enable Relaxed Ordering (ERO):** Not supported

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0h RW	**Fatal Error Reporting Enable (FEE):** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0h RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0h RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

17.6.15 Link Capabilities (LCAP)—Offset 4Ch

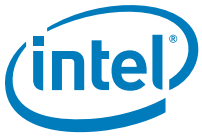
Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 710C00h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h
23	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
22	1h RW/O	**ASPM Optionality Compliance (ASPMOC):** ASPM Optionality Compliance(ASPMOC): This bit must be set to 1b for PCIe 3.0 compliant port. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests.
21	1h RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1h RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0h RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the root port does not support Surprise Down Error Reporting
18	0h RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism.
17:15	2h RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b Less than 1 us 001b 1 us to less than 2 us 010b 2 us to less than 4 us 011b 4 us to less than 8 us 100b 8 us to less than 16 us 101b 16 us to less than 32 us 110b 32 us to 64 us 111b More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency.
14:12	0h RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL



Bit Range	Default & Access	Field Name (ID): Description
11:10	3h RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 No ASPM Supported 01 L0s Supported 10 L1 Supported 11 L0s and L1 supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is '01'. Otherwise, the default of this field is '11'. If STRPFUSECFG.ASPMDIS is 1, BIOS writing '11' to this field will have the same effect as writing '01'. '01' will be reflected on this register when read and the register will turn to Read-Only once written once.
9:4	0h RO/V	**Maximum Link Width (MLW):** For the root ports, several values can be taken, based upon the value of the chipset configuration register field RPC.PC1 for ports 1-4: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RO/V	**Max Link Speeds (MLS):** Indicates the supported link speeds of the Root Port. 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5GT/s Link speeds supported This register reports a value of 0001b if the Root Port Gen2 Disable Fuse is set or the MPC.PCIEGEN2DIS bit is set, else this register reports a value of 0010b. Max Link Speeds (MLS): This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. This register reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through Fuse or MPC.PCIESD register. This register reports a value of 0010b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through Fuse or MPC.PCIESD register.

17.6.16 Link Control; Link Status (LCTL_LSTS)—Offset 50h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
29	0h RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.
28	0h RO/V	**Slot Clock Configuration (SCC):** In normal mode, root port uses the same reference clock as on the platform and does not generate its own clock. Note: The default of this register bit is dependent on the 'PCIe Non-Common Clock With SSC Mode Enable Strap'. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'.
27	0h RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
26	0h RO	**Reserved (RSVD):** Reserved. Previously this was defined as Link Training Error (LTE) but support for this bit was removed from subsequent versions of the PCI Express specification.
25:20	0h RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained.

Bit Range	Default & Access	Field Name (ID): Description
19:16	1h RO/V	**Current Link Speed (CLS):** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link This field indicates the negotiated Link speed of the given link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. The value of this field is undefined if the link is not up.
15:12	0h RO	**Reserved (RSVD_1):** Reserved
11	0h RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.
10	0h RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.
9	0h RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. Note: When operating as PCI Express, this bit defines the value of the Link Upconfigure Capability in TS2 Ordered Sets.
8	0h RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on Root Ports.
7	0h RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. Note: This functionality is not applicable for Mobile Express.
6	0h RW	**Common Clock Configuration (CCC):** When set, indicates that the root port and device are operating with a distributed common reference clock.

Bit Range	Default & Access	Field Name (ID): Description
5	0h WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0h RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state.
3	0h RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0h RO	**Reserved (RSVD_2):** Reserved
1:0	0h RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see '00' as an output from this register. BIOS reading this register should always return the correct value.

17.6.17 Slot Capabilities (SLCAP)—Offset 54h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 40060h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/O	**Physical Slot Number (PSN__31_24):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
23:19	0h RW/O	**Physical Slot Number (PSN__23_19):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.

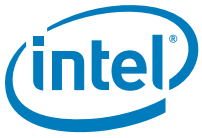
Bit Range	Default & Access	Field Name (ID): Description
18	1h RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0h RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented.
16:15	0h RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:8	0h RW/O	**Slot Power Limit Value (SLV__14_8):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
7	0h RW/O	**Slot Power Limit Value (SLV__7_7):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1h RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported.
5	1h RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification.
4	0h RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot.
3	0h RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot.
2	0h RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present
1	0h RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot
0	0h RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot.

17.6.18 Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved (RSVD):** Reserved
24	0h RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
23	0h RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock.
22	0h RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'.
21	0h RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented.
20	0h RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller..
19	0h RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the SLSTS.PDS bit changes state.
18	0h RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented.
17	0h RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented.
16	0h RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button
15:13	0h RO	**Reserved (RSVD_1):** Reserved
12	0h RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed
11	0h RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock.
10	0h RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug.
9:8	0h RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller..
7:6	0h RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller..
5	0h RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0h RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller..

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state.
2	0h RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller..
1	0h RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller...
0	0h RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller..

17.6.19 Root Control (RCTL)—Offset 5Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:4	0h RO	**Reserved (RSVD_1):** Reserved
3	0h RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set).
2	0h RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0h RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0h RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

17.6.20 Root Status (RSTS)—Offset 60h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17	0h RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. Root ports have a one deep PME pending queue.
16	0h RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0h RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

17.6.21 Device Capabilities 2 (DCAP2)—Offset 64h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 80837h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved (RSVD):** Reserved
19:18	2h RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported.
17:12	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/ disable the root port from declaring support for the LTR capability.
10:6	0h RO	**Reserved (RSVD_2):** Reserved
5	1h RO	**ARI Forwarding Supported (AFS):** ARI Forwarding Supported (AFS): Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. Note: This bit is not made RWO to simplify implementation, since there is a requirement that the ARI Forwarding Enable bit must be hardwired to 0b if ARI Forwarding Supported bit is 0b. It is low risk to keep this risk 1b.
4	1h RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	7h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C 0111b Ranges A, B [amp] C [lt]-- This is what PCH supports 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved.

17.6.22 Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15	0h RO	**Reserved (RSVD_1):** Reserved
14:13	0h RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** 00b Disable OBFF mechanism. 01b Enable OBFF mechanism using Message signaling (Variation A). 10b Enable OBFF mechanism using Message signaling (Variation B). 11b Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect.
12:11	0h RO	**Reserved (RSVD_2):** Reserved
10	0h RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:6	0h RO	**Reserved (RSVD_3):** Reserved
5	0h RW	**ARI Forwarding Enable (AFE):** ARI Forwarding Enable (AFE): When set, the Downstream Port disables its traditional Device Number field being 0b enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port.
4	0h RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The root port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 us to 100 us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either when this value was changed or when each request was issued.

17.6.23 Link Capabilities 2 (LCAP2)—Offset 6Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved (RSVD):** Reserved
22:16	0h RO	**Lower SKP OS Reception Supported Speeds Vector (LSOSRSS):** Lower SKP OS Reception Supported Speeds Vector(LSOSRSS): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
15:9	0h RO	**Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV):** Lower SKP OS Generation Supported Speeds Vector(LSOSGSSV): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
8	0h RO	**Crosslink Supported (CS):** Crosslink Supported (CS): No support for Crosslink.
7:1	0h RO/V	**Supported Link Speeds Vector (SLSV):** Supported Link Speeds Vector (SLSV): This field indicates the supported Link speed of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. Bit definitions within this field are: Bit 0: 2.5 GT/s. Bit 1: 5.0 GT/s. Bit 2: 8.0 GT/s. Bits 6:3: Reserved. This register reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through Fuse or MPC.PCIESD register. This register reports a value of 0011b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through Fuse or MPC.PCIESD register.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**Reserved (RSVD_1):** Reserved

17.6.24 Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/1C/V/P	**Link Equalization Request (LER):** Link Equalization Request (LER): This bit is set by hardware to request the Link equalization process to be performed on the Link. Register Attribute: Dynamic.
20	0h RO/V/P	**Equalization Phase 3 Successful (EQP3S):** Equalization Phase 3 Successful (EQP3S): When set to 1, this bit indicates that Phase 3 of the Transmitter Equalization procedure has successfully completed.
19	0h RO/V/P	**Equalization Phase 2 Successful (EQP2S):** Equalization Phase 2 Successful (EQP2S): When set to 1, this bit indicates that Phase 2 of the Transmitter Equalization procedure has successfully completed.
18	0h RO/V/P	**Equalization Phase 1 Successful (EQP1S):** Equalization Phase 1 Successful (EQP1S): When set to 1, this bit indicates that Phase 1 of the Transmitter Equalization procedure has successfully completed.
17	0h RO/V/P	**Equalization Complete (EqC):** Equalization Complete (EC): When set to 1, this bit indicates that the Transmitter Equalization procedure has completed
16	0h RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/P	**Compliance Preset/De-emphasis (CD):** For 8.0 GT/s Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b -3.5 dB 0000b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. The default value of this field is 0000b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value.
11	0h RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only.
10	0h RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.

Bit Range	Default & Access	Field Name (ID): Description
9:7	0h RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0h RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5	0h RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value.
3:0	0h RW/V/P	**Target Link Speed (TLS):** Target Link Speed (TLS): This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. If a value is written to this field that does not correspond to a supported speed, as indicated by the Supported Link Speeds Vector, the result is undefined. The default value of this field is GEN1. Note: This register field could be used by REUT software to limit the link speed to 2.5 GT/s or 5 GT/s data rate.

17.6.25 Slot Capabilities 2 (SLCAP2)—Offset 74h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved (RSVD):** Reserved

17.6.26 Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:0	0h RO	**Reserved (RSVD_1):** Reserved

17.6.27 Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 9005h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved
23	0h RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
22:20	0h RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
19:17	0h RO	**Multiple Message Capable (MMC):** Only one message is required.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	5h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

17.6.28 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction.

17.6.29 Subsystem Vendor Capability (SVCAP)—Offset 90h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: A00Dh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

17.6.30 Subsystem Vendor IDs (SVID)—Offset 94h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

17.6.31 Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: C8030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	19h RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Microsoft operating systems to enable PME# in devices connected behind this root port.
26	0h RO	**D2_Support (D2S):** The D2 state is not supported.
25	0h RO	**D1_Support (D1S):** The D1 state is not supported.
24:22	0h RO	**Aux_Current (AC):** Reports 0mA (self-powered), as use of this controller does not add to suspect well power consumption.
21	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
20	0h RO	**Reserved (RSVD):** Reserved
19	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
18:16	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	1h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

17.6.32 PCI Power Management Control And Status (PMCS)—Offset A4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Data (DTA):** Reserved
23	0h RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification
22	0h RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification.
21:16	0h RO	**Reserved (RSVD):** Reserved
15	0h RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0h RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Microsoft operating systems to enable PME# on devices connected to this root port.
7:4	0h RO	**Reserved (RSVD_1):** Reserved
3	1h RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved (RSVD_2):** Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 D0 state 11 D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

17.6.33 Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h

Size:32 bits
The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list.
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

17.6.34 Uncorrectable Error Status (UES)—Offset 104h

This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/1C/V/P	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0h RW/1C/V/P	**Completor Abort Status (CA):** Indicates a completer abort was received

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Not supported.
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RO	**Training Error Status (TE):** Not supported.

17.6.35 Uncorrectable Error Mask (UEM)—Offset 108h

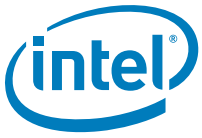
When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/P	**ACS Violation Mask (AVM):** Reserved. Access Control Services are not supported
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.



Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0h RW/P	**Completor Abort Mask (CM):** Mask for completer abort.
14	0h RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.
13	0h RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RO	**Training Error Mask (TE):** Not supported.

17.6.36 Uncorrectable Error Severity (UEV)—Offset 10Ch

This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 60011h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD):** Reserved
21	0h RW/P	**ACS Violation Severity (AVS):** Severity for ACS violation.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	1h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.

Bit Range	Default & Access	Field Name (ID): Description
17	1h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0h RW/P	**Completor Abort Severity (CA):** Severity for completer abort.
14	0h RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:6	0h RO	**Reserved (RSVD_1):** Reserved
5	0h RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	**Reserved (RSVD_2):** Reserved
0	1h RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation..

17.6.37 Correctable Error Status (CES)—Offset 110h

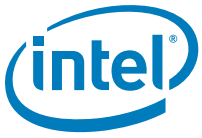
This register is only reset by a loss of core power

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved (RSVD):** Reserved
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	**Reserved (RSVD_1):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

17.6.38 Correctable Error Mask (CEM)—Offset 114h

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved (RSVD):** Reserved
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	**Reserved (RSVD_1):** Reserved
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.

Bit Range	Default & Access	Field Name (ID): Description
5:1	0h RO	**Reserved (RSVD_2):** Reserved
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

17.6.39 Advanced Error Capabilities and Control (AECC)—Offset 118h

This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved (RSVD):** Reserved
8	0h RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0h RO	**ECRC Check Capable (ECC):** ECRC is not supported.
6	0h RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0h RO	**ECRC Generation Capabile (EGC):** ECRC is not supported.
4:0	0h RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

17.6.40 Header Log DW1 (HL_DW1)—Offset 11Ch

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**1st dWord of TLP (DW1):** Byte0 [amp][amp] Byte1 [amp][amp] Byte2 [amp][amp] Byte3

17.6.41 Header Log DW2 (HL_DW2)—Offset 120h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**2nd dWord of TLP (DW2):** Byte4 [amp][amp] Byte5 [amp][amp] Byte6 [amp][amp] Byte7

17.6.42 Header Log DW3 (HL_DW3)—Offset 124h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**3rd dWord of TLP (DW3):** Byte8 [amp][amp] Byte9 [amp][amp] Byte10 [amp][amp] Byte11

17.6.43 Header Log DW4 (HL_DW4)—Offset 128h

Size:32 bits
These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V/P	**4th dWord of TLP (DW4):** Byte12 [amp][amp] Byte13 [amp][amp] Byte14 [amp][amp] Byte15

17.6.44 Root Error Command (REC)—Offset 12Ch

This register allows errors to generate interrupts.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved (RSVD):** Reserved
2	0h RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0h RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0h RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

17.6.45 Error Source Identification (ESID)—Offset 134h

Size:32 bits
Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set.
15:0	0h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set.

17.6.46 ACS Extended Capability Header (ACSECH)—Offset 140h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support ACS Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support ACS Extended Capability, BIOS should write a 000Dh to this register else it should write 0.

17.6.47 ACS Capability Register (ACSCAPR)—Offset 144h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: Fh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved (RSVD_1):** Reserved for Egress Control Vector Size. This field is not applicable since ACS P2P Egress Control is not supported.
7	0h RO	**Reserved (RSVD_2):** Reserved
6	0h RO	**ACS Direct Translated P2P (T):** ACS Direct Translated P2P (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control (E):** ACS P2P Egress Control (E): ACS P2P Egress Control is not supported.
4	0h RO	**ACS Upstream Forwarding (U):** ACS Upstream Forwarding (U): ACS Upstream Forwarding is not supported.
3	1h RW/O	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Required for all Functions that support ACS P2P Request Redirect; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Completion Redirect.
2	1h RW/O	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Required for Root Ports that support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports; required for multi-function device Functions that support peer-to-peer traffic with other Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Request Redirect.
1	1h RW/O	**ACS Translation Blocking (B):** ACS Translation Blocking (B): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Translation Blocking.
0	1h RW/O	**ACS Source Validation (V):** ACS Source Validation (V): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Source Validation.

17.6.48 ACS Control Register (ACSCTLR)—Offset 148h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved (RSVD):** Reserved,
6	0h RO	**ACS Direct Translated P2P Enable (T):** ACS Direct Translated P2P Enable (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control Enable (E):** ACS P2P Egress Control Enable (E): ACS P2P Egress Control is not supported.
4	0h RO	**ACS Upstream Forwarding Enable (U):** ACS Upstream Forwarding Enable (U): ACS Upstream Forwarding is not supported.
3	0h RW	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Determines when the component redirects peer-to-peer Completions upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear.
2	0h RW	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Determines when the component redirects peer-to-peer memory Requests targeting another peer port upstream. I/O, Configuration, VDM Messages and Completions are never affected by ACS P2P Request Redirect.
1	0h RW	**ACS Translation Blocking (B):** ACS Translation Blocking (B): When set, the component blocks all upstream Memory Requests whose Address Translation (AT) field is not set to the default value. I/O, Configuration, Completions and Messages are never affected by ACS Translation Blocking.
0	0h RW	**ACS Source Validation (V):** ACS Source Validation (V): When set, the component validates the Bus Number from the Requester ID of upstream Requests against the secondary / subordinate Bus Numbers. I/O, Configuration and Completions are never affected by ACS Source Validation.

17.6.49 PTM Extended Capability Header (PTMECH)—Offset 150h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support PTM Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support PTM Extended Capability, BIOS should write a 001Fh to this register else it should write 0.

17.6.50 PTM Capability Register (PTMCAPR)—Offset 154h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 400h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved,
15:8	4h RW/O	**Local Clock Granularity (LCG):** Local Clock Granularity(LCG): 0000 0000b - Time Source does not implement a local clock. It simply propagates timing information obtained from further Upstream in the PTM Hierarchy when responding to PTM Request messages. 0000 0001b - 1111 1110b: Indicates the period of this Time Sources local clock in ns. 1111 1111b: Indicates the period of this Time Sources local clock is greater than 254 ns. If the PTM Root Select bit is Set, this local clock is used to provide PTM Master Time. Otherwise, the Time Source uses this local clock to locally track PTM Master Time received from further Upstream within a PTM Hierarchy.
7:3	0h RO	**Reserved (RSVD_1):** Reserved,
2	0h RW/O	**PTM Root Capable (PTMRC):** PTM Root Capable(PTMRC): Root Ports must set this bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW/O	**PTM Responder Capable (PTMRSPC):** PTM Responder Capable(PTMRSPC): Root Ports are permitted to set this bit to 1b to indicate that they implement the PTM Responder role.
0	0h RO	**PTM Requester Capable (PTMREQC):** PTM Requester Capable(PTMREQC): PTM Requester Role is not supported by Root Port.

17.6.51 PTM Control Register (PTMCTLR)—Offset 158h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:8	0h RO	**Effective Granularity (EG):** Effective Granularity(EG): Root Port does not support PTM Requester role.
7:2	0h RO	**Reserved (RSVD_1):** Reserved.
1	0h RW	**Root Select (RS):** Root Select(RS): When Set, if the PTM Enable bit is also Set, this Time Source is the PTM Root. Within each PTM Hierarchy, it is recommended that system software select only the furthest Upstream Time Source to be the PTM Root.
0	0h RW	**PTM Enable (PTME):** PTM Enable(PTME): When Set, this Function is permitted to participate in the PTM mechanism according to its selected role. Software must not have the PTM Enable bit Set in the PTM Control register on a Function associated with an Upstream Port unless the associated Downstream Port on the Link already has the PTM Enable bit Set in its associated PTM Control register. Register Attribute: Static.

17.6.52 L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h

Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 1h
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 001Eh. .

17.6.53 L1 Sub-States Capabilities (L1SCAP)—Offset 204h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 28281Fh

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
23:19	5h RW/O	**Port Tpower_on Value (PTV):** Along with the Port T_POWER_ON Scale Field in the L1 Substates Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF.
18	0h RO	**Reserved (RSVD_1):** Reserved.
17:16	0h RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Substates Capabilities register. '00b': 2 us '01b': 10 us '10b': 100 us '11b': Reserved Required for all Ports that support L1.OFF.
15:8	28h RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF.
7:5	0h RO	**Reserved (RSVD_2):** Reserved
4	1h RW/O	**L1 PM Substates Supported (L1PSS):** When Set this bit indicates that this Port supports L1 PM Substates. For compatibility with possible future extensions, software must not enable L1 PM Substates unless this bit is set. This RWO field must be programmed prior to enabling ASPM.
3	1h RW/O	**ASPM L1.1 Substates Supported (AL11S):** When set, this bit indicates that this port supports L1 substates for ASPM L1.SNOOZ. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
2	1h RW/O	**ASPM L1.2 Supported (AL12S):** When set, this bit indicates that ASPM_L1.OFF is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
1	1h RW/O	**PCI-PM L1.1 Supported (PPL11S):** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

Bit Range	Default & Access	Field Name (ID): Description
0	1h RW/O	**PCI-PM L1.2 Supported (PPL12S):** When set, this bit indicates that L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

17.6.54 L1 Sub-States Control 1 (L1SCTL1)—Offset 208h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**L1.2 LTR Threshold Latency ScaleValue (L12LTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe root port. The value in this field, together with L12LTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L12LTRSTLV times 1 ns 001: L12LTRSTLV times 32 ns 010: L12LTRSTLV times 1024 ns 011: L12LTRSTLV times 32768 ns 100: L12LTRSTLV times 1048576 ns 101: L12LTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
28:26	0h RO	**Reserved (RSVD):** Reserved
25:16	0h RW	**L1.2 LTR Threshold Latency Value (L12OFFLTRTLV):** This field contains the L1.2 LTR Threshold Latency Value for this particular PCIe root port. The value in this field, together with L12LTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
15:8	0h RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time the PCIe root port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**Reserved (RSVD_1):** Reserved
3	0h RW	**ASPM L1.1 Enabled (AL11E):** When set, this bit indicates that ASPM L1.SNOOZ substates are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic
2	0h RW	**ASPM L1.2 Enable (AL12E):** When set, this bit indicates that ASPM L1.OFF substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic
1	0h RW	**PCI-PM L1.SNOOZ Enable (PPL11E):** When set, this bit indicates that PCI-PM L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
0	0h RW	**PCI-PM L1.2 Enabled (PPL12E):** When set, this bit indicates that PCI-PM L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.

17.6.55 L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 28h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:3	5h RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# is sampled asserts in L1.OFF state. Tpower_on value is calculated by multiplying the value in this field by the value in the TPOS field. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
2	0h RO	**Reserved (RSVD_1):** Reserved
1:0	0h RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. '00b': 2 us '01b': 10 us '10b': 100us '11b': Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static

17.6.56 Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h

Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEECID):** PCI Express Extended Capability ID (PCIEECID): This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 0019h to this register else it should write 0.

17.6.57 Link Control 3 (LCTL3)—Offset 224h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:9	0h RO	**Enable Lower SKP OS Generation Vector (ELSOSGV):** Enable Lower SKP OS Generation Vector(ELSOSGV): When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is Set in this field and the corresponding bit in the Lower SKP OS Generation Supported Speeds Vector is not set.
8:2	0h RO	**Reserved (RSVD_1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Link Equalization Request Interrupt Enable (LERIE):** Link Equalization Request Interrupt Enable (LERIE): When set, this bit enables the generation of an interrupt to indicate that the Link Equalization Request bit has been set.
0	0h RW	**Perform Equalization (PE):** Perform Equalization (PE): When this bit is 1b and Link Retrain bit is set with the Target Link Speed field set to 8 GT/s, the Downstream Port must perform Link Equalization. This bit is cleared by Root Port upon entry to Link Equalization

17.6.58 Lane Error Status (LES)—Offset 228h

The Lane number is the default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (RSVD):** Reserved
3	0h RW/1C/V/P	**Lane 3 Error Status (L3ES):** Lane 3 Error Status (L3ES): Lane 3 detected a Lane-based error.
2	0h RW/1C/V/P	**Lane 2 Error Status (L2ES):** Lane 2 Error Status (L2ES): Lane 2 detected a Lane-based error.
1	0h RW/1C/V/P	**Lane 1 Error Status (L1ES):** Lane 1 Error Status (L1ES): Lane 1 detected a Lane-based error.
0	0h RW/1C/V/P	**Lane 0 Error Status (L0ES):** Lane 0 Error Status (L0ES): Lane 0 detected a Lane-based error.

17.6.59 Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 7F7F7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved.
30:28	7h RW	**Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH):** Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 1 Transmitter Preset (UPL1TP):** Upstream Port Lane 1 Transmitter Preset (UPL1TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	**Reserved (RSVD_1):** Reserved.
22:20	7h RW	**Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH):** Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 1 Transmitter Preset (DPL1TP):** Downstream Port Lane 1 Transmitter Preset (DPL1TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved (RSVD_2):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
14:12	7h RW	**Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH):** Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 0 Transmitter Preset (UPL0TP):** Upstream Port Lane 0 Transmitter Preset (UPL0TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	**Reserved (RSVD_3):** Reserved.
6:4	7h RW	**Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH):** Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 0 Transmitter Preset (DPL0TP):** Downstream Port Lane 0 Transmitter Preset (DPL0TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

17.6.60 Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 7F7F7F7Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
30:28	7h RW	**Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH):** Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 3 Transmitter Preset (UPL3TP):** Upstream Port Lane 3 Transmitter Preset (UPL3TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	**Reserved (RSVD_1):** Reserved
22:20	7h RW	**Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH):** Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 3 Transmitter Preset (DPL3TP):** Downstream Port Lane 3 Transmitter Preset (DPL3TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	**Reserved (RSVD_2):** Reserved
14:12	7h RW	**Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH):** Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 2 Transmitter Preset (UPL2TP):** Upstream Port Lane 2 Transmitter Preset (UPL2TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	**Reserved (RSVD_3):** Reserved
6:4	7h RW	**Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH):** Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
3:0	Fh RW	**Downstream Port Lane 2 Transmitter Preset (DPL2TP):** Downstream Port Lane 2 Transmitter Preset (DPL2TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

17.6.61 PCI Express Replay Timer Policy 1 (PCIERTP1)—Offset 300h

The Replay Timer controlled by the Replay Timeout field is started when the Retry Buffer is empty and a TLP is placed into it or an Ack/Nak DLLP is received and there are still non-acknowledged packets within the Retry Buffer. The counter continues to count until the next valid Ack DLLP or a NAK DLLP that acknowledges unacknowledged TLPs is received, or it reaches the timeout value specified by this register. When a valid Ack/Nak DLLP is received, the timer is reset to zero and restarted if there are still non-acknowledged packets within the Retry Buffer. Otherwise if the Retry Buffer is empty, the counter is just reset to zero. If the timer reaches the timeout value, the non-acknowledged packets within the Retry Buffer will be replayed.
The default for this register is dependant on the MAX_PAYLOAD_SIZE , the NEGOTIATED_WIDTH, and the NEGOTIATED_SPEED.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: A64F96h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD):** Reserved,
23:20	Ah RW	**Gen 2 x1 (G2X1):** Gen 2 x1 (G2X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 7) * 64 link clocks. For PCIE Gen 2 speed and x1 width For Mobile Express HS-Gear 3 speed and x1 width.

Bit Range	Default & Access	Field Name (ID): Description
19:16	6h RW	**Gen 2 x2 (G2X2):** Gen 2 x2 (G2X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 4) * 64 link clocks. For PCIe Gen 2 speed and x2 width. For Mobile Express HS-Gear 3 speed and x2 width.
15:12	4h RW	**Gen 2 x4 (G2X4):** Gen 2 x4 (G2X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 2 speed and x4 width. For Mobile Express HS-Gear 3 speed and x4 width.
11:8	Fh RW	**Gen 1 x1 (G1X1):** Gen 1 x1 (G1X1): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 10) * 64 link clocks. For 512B MPS: (nnn + 17) * 64 link clocks. For PCIe Gen 1 speed and x1 width. For Mobile Express HS-Gear 2 speed and x1 width.
7:4	9h RW	**Gen 1 x2 (G1X2):** Gen 1 x2 (G1X2): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For PCIe Gen 1 speed and x2 width. For Mobile Express HS-Gear 2 speed and x2 width.

Bit Range	Default & Access	Field Name (ID): Description
3:0	6h RW	**Gen 1 x4 (G1X4):** Gen 1 x4 (G1X4): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/ Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 1 speed and x4 width. For Mobile Express HS-Gear 2 speed and x4 width.

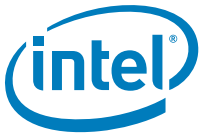
17.6.62 PCI Express Replay Timer Policy 2 (PCIERTP2)—Offset 304h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 1BC00B86h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Lane 0 Lane Number (L0LN):** Lane 0 Lane Number(L0LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 0 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
29:28	1h RW	**Lane 1 Lane Number (L1LN):** Lane 1 Lane Number(L1LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 1 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.



Bit Range	Default & Access	Field Name (ID): Description
27:26	2h RW	**Lane 2 Lane Number (L2LN):** Lane 2 Lane Number(L2LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 2 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
25:24	3h RW	**Lane 3 Lane Number (L3LN):** Lane 3 Lane Number(L3LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 3 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
23	1h RW	**Loopback Master EQ TS1 Enable (LMEQTS1E):** Loopback Master EQ TS1 Enable(LMEQTS1E): When set, the Loopback Master will use EQ TS1 Ordered Sets to direct the Loopback Slave into Loopback from Configuration.Linkwidth.Start. The Preset field of the EQ TS1 Ordered Sets will be specified by Upstream Port Lane X Transmitter Preset and Upstream Port Lane X Receiver Preset Hint fields in the Lane Equalization Control registers.
22	1h RW	**Loopback Master EQ Change Enable (LMEQCE):** Loopback Master EQ Change Enable(LMEQCE): This field is applicable to the case where Loopback is entered from Recovery state. When set, the Loopback Master will set the EC field of the GEN3 TS1 Ordered Sets to the appropriate value based on the ports direction(10b or 11b) to direct the Loopback Slave into Loopback from Recovery state. The Preset field of the GEN3 TS1 Ordered Sets will be specified by Upstream Port Lane X Transmitter Preset and Upstream Port Lane X Receiver Preset Hint fields in the Lane Equalization Control registers.
21:12	0h RO	**Reserved (RSVD):** Reserved
11:8	Bh RW	**Gen 3 x1 (G3X1):** Gen 3 x1 (G3X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For Gen 3 speed and x1 width

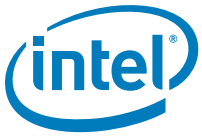
Bit Range	Default & Access	Field Name (ID): Description
7:4	8h RW	**Gen 3 x2 (G3X2):** Gen 3 x2 (G3X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For Gen 3 speed and x2 width
3:0	6h RW	**Gen 3 x4 (G3X4):** Gen 3 x4 (G3X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 1) * 64 link clocks. For 512B MPS: (nnn + 2) * 64 link clocks. For Gen 3 speed and x4 width

17.6.63 PCI Express Status 1 (PCIESTS1)—Offset 328h

Access Method

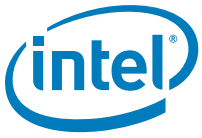
Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**LTSM State (LTSMSTATE):** Indicates the LTSM present state. Hex LTSSM States 00DETIDLE 01DETRDY 02DETIDLEP1TOP2 03DETRDYP2TOP1 04DETRDYINP1 05DETRDYINP1EXE 06DETP2POLLSTART 07DETP1POLLSTART 08DETP2TOP0 09DETP1TOP0 0AECPCMPRETRAIN 0BECPCMFAILP0TOP2 0CDETP0TOP2 0DPMODECHANGE 0EECPCMPCIE 0FECPCMUSB3 10DET2POLLINP0 11POLLINGACTIVE 12POLLINGCOMPLIANCEMARGINCNT 13POLLINGCOMPLIANCE 14POLLINGCOMPLIANCESPEEDUP 15POLLINGCOMPLIANCESPEEDDN 16POLLINGCOMPLIANCESPEEDTXEIDLE 17POLLINGCOMPLIANCESPEEDRXEIDLE 18POLLINGCOMPLIANCESPEED 19POLLINGCOMPLIANCESPEEDDONE 1APOLLINGCOMPLIANCEEXIT 1BPOLLINGCONFIGURATION 1CPOLLINGTXEIDLE 1DPOLLINGEND 1EPOLLINGENDWAIT 1FLINKWIDTHSTART 20LINKWIDTHACCEPT 21LANENUMWAIT 22LANENUMACCEPT 23LANEDESKEW 24CONFIGCOMPLETE 25CONFIGIDLE 26LWNEXITRECOVERY 27CONFIGLPBKENTRY 28CONFIGLPBKLWSTART 29CONFIGLPBKSPEEDTXEIDLE 2ACONFIGLPBKSPEEDSTART 2BCONFIGLPBKSPEEDRXEIDLE 2CCONFIGLPBKSPEED 2DCONFIGLPBKREUTSKIP 2ECONFIGLPBKREUT 2FCONFIGLPBKEXITM 30CONFIGLPBKTXEIDLE

Bit Range	Default & Access	Field Name (ID): Description
		31LWNEXIT 32LWNLNK2DETECT 33L0 34TXL0SRXL0 35RXL0STXL0 36TXL0SRXL0S 37L1TXEIDLE 38L1RCVEIDLE 39L1PREENTRY 3AL1ENTRY 3BL1IDLE 3CL1IDLEGEN2WAIT 3DL1EXIT 3EL2TXEIDLE 3FL2RCVEIDLE 40L2IDLEWAIT 41L2IDLERDY 42L2IDLE 43LOOPBACKENTRY 44LPBKACTIVEMTXSKP 45LPBKACTIVEMSKPDSKW 46LOOPBACKACTIVEM 47LPBKSLAVESPEEDTXEIDLE 48LPBKSLAVESPEEDRXEIDLE 49LPBKSLAVESPEED 4ALOOPBACKACTIVES 4BLOOPBACKCMMSKP 4CLOOPBACKCMM 4DLOOPBACKEXITM 4ELOOPBACKEXITS 4FLOOPBACKEXITL0 50LOOPBACKLNK2DETECT 51LOOPBACK2DETECT 52DISTX16TS1DIS 53DISTXEIDLE 54DISWAITSTART 55DISWAITGNT 56DISWAIT4TXMARGIN 57DISWAIT 58DIS2DETECT 59HOTRESETTS1 5AHOTRESETDONE 5BHOTRESETEIDLE 5CRECOVERYRCVRWAIT 5DRECOVERYRCVRMARGINCNT 5ERECOVERYRCVRLOCK 5FRECOVERYDESKEW 60RECOVERYRCVRCFG 61RECOVERYSPEED 62RECOVERYSPEEDTXEIDLE 63RECOVERYSPEEDRXEIDLE



Bit Range	Default & Access	Field Name (ID): Description
		64RECOVERYSPEEDREADY 65RECOVERYIDLE 66RECOVERYEXITDETECT 67RECOVERYLNK2DETECT 68RECOVERYEXITLPBK 69RECOVERYEXITL0 6ARECOVERYEXITDIS 6BRECOVERYEXITRST Note: This register field could be used by REUT software to monitor the link LTSSM substates.
23	0h RO	**Reserved (RSVD):** Reserved.
22:19	0h RO/V	**Link Status (LNKSTAT):** During Link initialization the Link will always traverse this list of state from the top (0000) to the bottom of the list (0111). One or more power management states may be skipped, but the direction of list traversal will remain the same. 0000 Link Down 0001 : Link Retrain 0011 : L1 0100 : L2 0101 : L3 0111 : L0 (Link Up) 1000 : L0s (Transmit [amp] Receive) 1001 : L0s (Transmit only) 1010 : L0s (Receive only) All others reserved
18:17	0h RO/V	**Replay Number (REPLAYNUM):** Number of times the Retry Buffer has been replayed since the last Link initialization / re-training. When the Data Link Layer has replayed the contents of the Retry Buffer four times a Link re-training will be initiated which will reset this value back to zero.
16	0h RO/V	**Data Link Layer Retry (DLLRETRY):** Indicates when the Data Link Layer has received a corrupted TLP or has detected a dropped packet and is currently waiting for the remote agent to re-transmit the corrupted/dropped packet. The value of Next Receive Sequence Number will be the sequence number associated with the corrupted packet.
15:12	0h RO/V	**Lane Status (LANESTAT):** Indicates which lanes are trained. A '1' indicates that the corresponding lane is trained (i.e. bit 0 = '1' means lane 0 is trained).
11:0	0h RO/V	**Next Transmitted Sequence Number (NXTTXSEQNUM):** This is the sequence number to be applied to and pre-pended to the next outgoing TLP.

17.6.64 PCI Express Status 2 (PCIESTS2)—Offset 32Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**PCIe Port 3 Non-Common Clock With SSC Mode Enable Strap (P3PNCCWSSCMES):** '0': PCIe port 3 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 3 is enabled to operate in non-common clock mode with SSC enabled.
30	0h RO/V	**PCIe Port 2 Non-Common Clock With SSC Mode Enable Strap (P2PNCCWSSCMES):** '0': PCIe port 2 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 2 is enabled to operate in non-common clock mode with SSC enabled.
29	0h RO/V	**PCIe Port 1 Non-Common Clock With SSC Mode Enable Strap (P1PNCCWSSCMES):** '0': PCIe port 1 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 1 is enabled to operate in non-common clock mode with SSC enabled.
28	0h RO/V	**PCIe Port 0 Non-Common Clock With SSC Mode Enable Strap (P0PNCCWSSCMES):** '0': PCIe port 0 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 0 is enabled to operate in non-common clock mode with SSC enabled.
27:16	0h RO/V	**Next Receive Sequence Number (NXTRCVSEQ):** This is the sequence number associated with the TLP that is expected to be received next.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW/1C/V	**Cause of Last Recovery Event (CLRE):** Cause of Last Recovery Event (CLRE): This field logs the cause of the entry to Recovery from L0. Only the first cause of Recovery is captured, until the register is cleared. Encoding Recovery Event 0000 No Recovery. 0001 Recovery entry triggered by remote device. 0010 Link Layer initiated Link Retrain due to error. 0011 De-skew buffer full. 0100 L0s exit time-out. 0101 Elastic Buffer overrun/underrun. 0110 Triggered by speed change. 0111 Link upconfiguration/downconfiguration. 1000 L0 Electrical Idle Inference. 1001 Any of the Link Retrain, CMM Start, Hot Reset, Link Disable, REUT Loopback Master or REUT Forced Loopback Master bit set. 1010 Received EIOS for RXL0s entry when ASPM L0s is disabled. 1011 Entry to Recovery from RXL0s due to PME timeout. Others Reserved.
11:0	0h RO/V	**Last Acknowledged Sequence Number (LASTACKSEQNUM):** This is the sequence number associated with the last acknowledged TLP.

17.6.65 PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h

Note that selecting a lane number that does not exist for a port may result in undefined behavior.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 2A000016h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**GEN3 Intel CMM Scrambler Bypass (G3ICMMSB):** GEN3 Intel CMM Scrambler Bypass(G3ICMMSB): When set, the Intel CMM pattern will bypass scrambling in GEN3. This bit does not impact non Intel CMM pattern. The TSx and SOS prior to Intel CMM will still be scrambled normally. Note: This bit must be set prior to enabling Intel CMM, by setting the PCIECMMPC.START. Note: When operating in Mobile Express mode, this field is not applicable.
30	0h RO	**Reserved (RSVD):** Reserved
29	1h RW	**CMM Symbol[3] Select (SYM3SEL):** 0: selects CMM Symbol [lb]3[rb] to a control character 1: selects CMM Symbol [lb]3[rb] as a data character
28	0h RW	**CMM Symbol[2] Select (SYM2SEL):** 0: selects CMM Symbol [lb]2[rb] to a control character 1: selects CMM Symbol [lb]2[rb] as a data character
27	1h RW	**CMM Symbol[1] Select (SYM1SEL):** 0: selects CMM Symbol [lb]1[rb] to a control character 1: selects CMM Symbol [lb]1[rb] as a data character
26	0h RW	**CMM Symbol[0] Select (SYM0SEL):** 0: selects CMM Symbol [lb]0[rb] to a control character 1: selects CMM Symbol [lb]0[rb] as a data character
25:24	2h RW	**CMM Sync Header (CMMSH):** CMM Sync Header(CMMSH): Specifies the Sync Header for the Intel CMM pattern specified in PCIECMMSB. Note: Due to implementation limitation, only a value of 10b is supported. All the other values are not supported.
23:22	0h RO/V	**CMM Error Lane Number (ERRLANENUM):** This field contains the lane number of the failing lane. Only valid when CMM Error Detected is 1.
21:16	0h RO	**Reserved (RSVD_1):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO/V	**CMM Invert (INVERT):** Indicates which lanes are inverted 000: No inversion 001: Lanes 0 010: Lanes 1 011: Lanes 2 100: Lanes 3 This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated)
12:10	0h RO/V	**CMM Symbol Error Number Invert (SYMERRNUMINV):** Indicates which register number miscompared on the failing lane, if the failing lane was an inverted lane. Only valid when CMM Error Detected is 1. 000: CMM Data D0 001: CMM Data D0 010: CMM Data D0 011: CMM Data D1 100: CMM Data D2 101: CMM Data D3 110: CMM Data D0 111: CMM Data D0
9:8	0h RO/V	**CMM Symbol Error Number (SYMERRNUM):** Indicates which register number miscompared on the failing lane, if the failing lane was not inverted. Only valid when CMM Error Detected is 1. 00: CMM Data 0 01: CMM Data 1 10: CMM Data 2 11: CMM Data 3
7	0h RW/1C/V	**CMM Error Detected (ERRDET):** 1: An error was detected 0: No error detected Note: This bit will be shadowed to an observability pin that can be used for IRQ generation.
6:5	0h RW	**Select Lane Number to be inverted for CMM (SLNINVCMM):** Select Lane Number to be inverted for CMM
4	1h RW	**CMM AutoInvert (AUTOINVERT):** 1: CMM autosequences through the inversion 0: CMM does not sequence inversion
3	0h RO/V	**CMM Status (STAT):** This bit is set when the CMM Start bit is set and cleared when the CMM mode has been entered successfully. 0: Compliance Measurement Mode is not active or CMM mode has been entered successfully. 1: Set as a result of CMM Start bit being set.
2	1h RW	**CMM Invert Enable (INVEN):** 1: Enables the Inversion of the lane 0: Lane not inverted
1	1h RW	**Reserved (RSVD_2):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/L	**CMM Start (START):** 1: Start CMM 0: Stop CMM

17.6.66 PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 4ABCB5BCh

Bit Range	Default & Access	Field Name (ID): Description
31:24	4Ah RW	**CMM Data [3] (DATA3):** This character contains CMM Data [lb]3[rb] that will be transmitted on the link.
23:16	BCh RW	**CMM Data [2] (DATA2):** This character contains CMM Data [lb]2[rb] that will be transmitted on the link.
15:8	B5h RW	**CMM Data [1] (DATA1):** This character contains CMM Data [lb]1[rb] that will be transmitted on the link.
7:0	BCh RW	**CMM Data [0] (DATA0):** This character contains CMM Data [lb]0[rb] that will be transmitted on the link.

17.6.67 PTM Propagation Delay (PTMPD)—Offset 390h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Propagation Delay Value (CPTMPDV):** Current PTM Propagation Delay Value(CPTMPDV): This field reports the current PTM Propagation Delay value captured from the last successful PTM dialog.

17.6.68 PTM Lower Local Master Time (PTMLLMT)—Offset 394h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Lower Local Master Time Value (CPTMLLMTV):** Current PTM Lower Local Master Time Value(CPTMLLMTV): This field reports the lower fields bits 31:0 of the Local TSC time value.

17.6.69 PTM Upper Local Master Time (PTMULMT)—Offset 398h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Current PTM Upper Local Master Time Value (CPTMULMTV):** Current PTM Upper Local Master Time Value(CPTMULMTV): This field reports the upper fields bits 63:32 of the Local TSC time value.

17.6.70 PTM Pipe Stage Delay Configuration 1 (PTMPSDC1)—Offset 39Ch

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN1 X2 RX Pipe Stage Delay (G1X2RPSD):** GEN1 X2 RX Pipe Stage Delay(G1X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN1 X2 TX Pipe Stage Delay (G1X2TPSD):** GEN1 X2 TX Pipe Stage Delay(G1X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN1 X1 RX Pipe Stage Delay (G1X1RPSD):** GEN1 X1 RX Pipe Stage Delay(G1X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN1 X1 TX Pipe Stage Delay (G1X1TPSD):** GEN1 X1 TX Pipe Stage Delay(G1X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.6.71 PTM Pipe Stage Delay Configuration 2 (PTMPSDC2)—Offset 3A0h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN2 X1 RX Pipe Stage Delay (G2X1RPSD):** GEN2 X1 RX Pipe Stage Delay(G2X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN2 X1 TX Pipe Stage Delay (G2X1TPSD):** GEN2 X1 TX Pipe Stage Delay(G2X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN1 X4 RX Pipe Stage Delay (G1X4RPSD):** GEN1 X4 RX Pipe Stage Delay(G1X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN1 X4 TX Pipe Stage Delay (G1X4TPSD):** GEN1 X4 TX Pipe Stage Delay(G1X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.6.72 PTM Pipe Stage Delay Configuration 3 (PTMPSDC3)—Offset 3A4h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN2 X4 RX Pipe Stage Delay (G2X4RPSD):** GEN2 X4 RX Pipe Stage Delay(G2X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN2 X4 TX Pipe Stage Delay (G2X4TPSD):** GEN2 X4 TX Pipe Stage Delay(G2X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN2 X2 RX Pipe Stage Delay (G2X2RPSD):** GEN2 X2 RX Pipe Stage Delay(G2X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN2 X2 TX Pipe Stage Delay (G2X2TPSD):** GEN2 X2 TX Pipe Stage Delay(G2X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.6.73 PTM Pipe Stage Delay Configuration 4 (PTMPSDC4)—Offset 3A8h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**GEN3 X2 RX Pipe Stage Delay (G3X2RPSD):** GEN3 X2 RX Pipe Stage Delay(G3X2RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
23:16	0h RW	**GEN3 X2 TX Pipe Stage Delay (G3X2TPSD):** GEN3 X2 TX Pipe Stage Delay(G3X2TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
15:8	0h RW	**GEN3 X1 RX Pipe Stage Delay (G3X1RPSD):** GEN3 X1 RX Pipe Stage Delay(G3X1RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN3 X1 TX Pipe Stage Delay (G3X1TPSD):** GEN3 X1 TX Pipe Stage Delay(G3X1TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.6.74 PTM Pipe Stage Delay Configuration 5 (PTMPSDC5)—Offset 3ACh

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved.
15:8	0h RW	**GEN3 X4 RX Pipe Stage Delay (G3X4RPSD):** GEN3 X4 RX Pipe Stage Delay(G3X4RPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.
7:0	0h RW	**GEN3 X4 TX Pipe Stage Delay (G3X4TPSD):** GEN3 X4 TX Pipe Stage Delay(G3X4TPSD): 00h: 1 link clock delay. 01h: 2 link clock delay. 02h: 3 link clock delay. : : FFh: 256 link clock delay.

17.6.75 PTM Extended Config (PTMECFG)—Offset 3B0h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20:18	0h RW	**Periodic Local TSC Link Fetch Frequency (PLTLFF):** Periodic Local TSC Link Fetch Frequency (PLTLFF): When this register is programmed to a non-zero values, the Local TSC Link Clock would perform a periodic fetch to obtain the latest TSC from the Local TSC XTAL Clock domain. This mechanism would ensure the Root Port Local TSC Link is always synchronized with the actual TSC as Link Clock domain is able to drift due to SSC. 000: Disable this feature. 001: Always pull without waiting for expiration. 010: Every 8 clocks 011: Every 16 clocks 100: Every 32 clocks 101: Every 64 clocks 110: Every 128 clocks 111: Every 256 clocks This register is only available in Port 1. Note: Software is expected to program this register prior to setting PTM Enable.
17:15	0h RW/1C/V	**Global Time Fetch Retry Counter (GTFRC):** Global Time Fetch Retry Counter. This register is incremented when the Root Port detected a retry on each Global Time Fetch on IOSF Sideband. The Root Port would increment the value of this register whenever ARU re-sends a LocalSync message. If more than 7 Retries are detected during the Global Time Fetch, Root Port would keep the value of this register to 111 (max) value. Software is expected to write 111 to this register to clear the entire field to 0. Note: For each x4 instance, only the value from Port 1 is used.
14:13	0h RW/1C/V	**Global Time Fetch Fail Counter (GTFFC):** Global Time Fetch Fail Counter. This register is incremented when the Root Port detected a fail on each Global Time Fetch on IOSF Sideband. The Root Port would increment the value of this register whenever ARU sends a SyncComp with the Fail status. If more than 3 failures are detected in the Global Time Fetch, Root Port would keep the value of this register to 111 (max) value. Software is expected to write 11 to this register to clear the entire field to 0. Note: For each x4 instance, only the value from Port 1 is used.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Global Time Fetch Status Pending Completion (GTFSPC):** Global Time Fetch Status Pending Completion. This register is set to 1 by the Root Port when it is in progress of fetching the Global Time from ARU. Note: For each x4 instance, only the value from Port 1 is used.
11:9	0h RW	**Periodic Global Time Stamp Counter Fetch Frequency (PGTSCFF):** Periodic Global Time Stamp Counter Fetch Frequency (PGTSCFF) : This field determine the frequency the Root Port would autonomously fetch the Global Time Stamp Counter. 00: 10us 01: 100us 10: 500us 10: 1ms Software is expected to program this bit first before programming the PGTSCFE register. Attribute: Dynamic Note: For each x4 instance, only the value from Port 1 is used.
8	0h RW	**Periodic Global Time Stamp Counter Fetch Enable (PGTSCFE):** Periodic Global Time Stamp Counter Fetch Enable (PGTSCFE) : When this bit set, the Controller will re-fetch the Global Time from the Always Running Unit (ARU). Once Fetch is completed, the Controller would update all the Local TSC with the newly fetch Global Time. If any PTM dialog is initiated while the re-fetch occurred, the Controller would use the existing Local TSC timers. Hardware would clear this bit upon completed fetching the Global Time. Attribute : Dynamic Note: For each x4 instance, only the value from Port 1 is used.
7	0h RW	**Trigger Global Time Stamp Counter Fetch Enable (TGTSCFE):** Trigger Global Time Stamp Counter Fetch Enable (TGTSCFE) : When this bit set, the Controller will re-fetch the Global Time from the Always Running Unit (ARU). Once Fetch is completed, the Controller would update all the Local TSC with the newly fetch Global Time. If any PTM dialog is initiated while the re-fetch occurred, the Controller would use the existing Local TSC timers. Hardware would clear this bit upon completed fetching the Global Time. Software can only set this register if PGTSCFE is not set. Attribute : Dynamic Note: For each x4 instance, only the value from Port 1 is used.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**PTM Request Periodic ACK Enable (PTMRPAE):** PTM Request Periodic ACK Enable (PTMRPAE) : When this register is set to 1, whenever a valid PTM request TLP is received, the Link Layer would transmit multiple ACK DLLPs corresponding to the PTM Request message. The number of ACK DLLP that the Link Layer would transmit is based on the PTMRNOPAD register. Attribute : Static Note: For each x4 instance, only the value from Port 1 is used.
5:4	0h RW	**PTM Request Number Of Periodic ACK DLLP (PTMRNOPAD):** PTM Request Number Of Periodic ACK DLLP (PTMRNOPAD) : When PTMRPAE is enable, whenever a valid PTM Request message is received, the Link Layer would transmit multiple ACK DLLP corresponding to the receiving of the PTM Request message. This register define the number of DLLP ACK will be transmitted as high priority. 00 - TX 1 DLLP ACK 01 - TX 2 DLLP ACK 10 - TX 3 DLLP ACK 11 - TX 4 DLLP ACK Attribute : Static Note: For each x4 instance, only the value from Port 1 is used.
3:0	0h RW	**IOSF Max Allowed Delay programming (IOSFMADP):** IOSF Max Allowed Delay programming (IOSFMADP): bits Status 0000 Bound Range Low 0001 Bound Range 2 1000 Bound Range Max others reserved

17.6.76 PTM Lower T2 Time Stamp (PTMLT2TSTMP)—Offset 3B4h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Latest Captured Lower T2 TimeStamp (LCLT2TS):** Latest Captured Lower T2 TimeStamp (LCLT2TS). This field shows the latest lower 32-bit of T2 TimeStamp captured by the Root Port in TSC Clock Domain when the Root Port received a valid PTM Request message. The renewable T2 TimeStamp due to a duplicate PTM Request would also be reflected in this field.

17.6.77 PTM Upper T2 Time Stamp (PTMUT2TSTMP)—Offset 3B8h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Latest Captured Upper T2 TimeStamp (LCUT2TS):** Latest Captured Upper T2 TimeStamp (LCUT2TS). This field shows the latest upper 32-bit of T2 TimeStamp captured by the Root Port in TSC Clock Domain when the Root Port received a valid PTM Request message. The renewable T2 TimeStamp due to a duplicate PTM Request would also be reflected in this field.

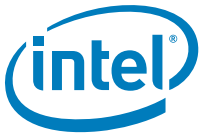
17.6.78 Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**mod-PHY Power Gating Disable Fuse (mPHYPGD):** 0: mod-PHY power gating is enabled. 1: mod-PHY power gating is disabled. Note: Prior to fuse pull, the default of this bit is specified in the 'Reset' column of this field. The default value will reflect the fuse value once fuse pull is done.
30:0	0h RO	**Reserved (RSVD):** Reserved



17.6.79 Thermal and Power Throttling (TNPT)—Offset 418h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 930h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Throttle Period (TP):** Throttle Period (TP): If any of the TNPT.DRXLTE or TNPT.DTXLTE bit is '1, this field defines the duration in milliseconds that defines the Throttling Window. When TNPT.TTG is set to 0, the effective Throttling Period is: 00h: 1 ms 01h: 2 ms : : FFh: 256 ms Note: The Throttle Period will have an uncertainty of +/-1 ms. When TNPT.TTG is set to 1, the effective Throttling Period is: 00h: 100 us 01h: 200 us : : FFh: 25.6 ms Note: The Throttle Period will have an uncertainty of +/-100 us. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling. Note: If TNPT.TT is programmed to a value bigger than TNPT.TP, the hardware behavior is undefined.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RW	**Throttle Time (TT):** Throttle Time (TT): If any of the TNPT.DRXLTE or TNPT.DTXLTE bit is '1, this field defines the period of the Throttling Zone within the Throttling Window specified by TNPT.TP. The value specified in this field will be multiplied by the respective multiplier in TNPT.TSLxM fields depending on the throttling severity indication received together with the Throttling State change indication. When TNPT.TTG is set to 0, the effective Throttle Time is: 00h: 1 ms 01h: 2 ms : 3Fh: 64 ms Others: Alias to 3Fh. Note: The Throttle Period will have an uncertainty of +/-1 ms. When TNPT.TTG is set to 1, the effective Throttle Time is: 00h: 100 us 01h: 200 us : 3Fh: 6.4 ms Note: The Throttle Period will have an uncertainty of +/-100 us. Note: If the reserved encoding is programmed to this field, hardware will behave the same as if the field is programmed to 3Fh. Note: Since the design is using a 1 ms tick for this timer, the Throttle Time will have an uncertainty of +/-1 ms. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling. Note: If TNPT.TT is programmed to a value bigger than TNPT.TP, the hardware behavior is undefined.
15:12	0h RO	**Reserved (RSVD):** Reserved
11:10	2h RW	**Throttling Severity Level 3 Multiplier (TSL3M):** Throttling Severity Level 3 Multiplier (TSL3M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: Always throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.

Bit Range	Default & Access	Field Name (ID): Description
9:8	1h RW	**Throttling Severity Level 2 Multiplier (TSL2M):** Throttling Severity Level 2 Multiplier (TSL2M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: Always throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.
7:6	0h RW	**Throttling Severity Level 1 Multiplier (TSL1M):** Throttling Severity Level 1 Multiplier (TSL1M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: No throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the link throttling
5:4	3h RW	**Throttling Severity Level 0 Multiplier (TSL0M):** Throttling Severity Level 0 Multiplier (TSL0M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: No throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.
3	0h RO	**Reserved (RSVD_1):** Reserved
2	0h RW	**Throttling Timer Granuality (TTG):** Throttling Timer Granuality (TTG): This register determines the granuality of the Thermal Throttling timers. This provides a smaller granuality

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Dynamic RX Link Throttling Enable (DRXLTE):** Dynamic RX Link Throttling Enable (DRXLTE): '0b: Dynamic Link RX Throttling mechanism is disabled. '1b: Dynamic Link RX Throttling mechanism is enabled. PCIe Root Port will induce the link to enter RXL0s. The duty cycle of the throttling window is configurable based on the throttling severity. Note: This field can only be set if the remote component supports TXL0s.
0	0h RW	**Dynamic TX Link Throttling Enable (DTXLTE):** Dynamic TX Link Throttling Enable (DTXLTE): '0b: Dynamic Link TX Throttling mechanism is disabled. '1b: Dynamic Link TX Throttling mechanism is enabled. PCIe Root Port will induce the link to enter TXL0s. The duty cycle of the throttling window is configurable based on the throttling severity. Note: This field can only be set if the remote component supports TXL0s.

17.6.80 Dynamic Lane Switch (DYNLNSW)—Offset 41Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved (RSVD):** Reserved.
0	0h RW	**Hardware Re-Do Preset to Coefficient Mapping Query After Lane Switching (HWRP2CM):** Hardware Re-Do Preset to Coefficient Mapping Query After Lane Switching (HWRP2CM): When this bit is set, the PCIe-SIP Controller would query the Preset to Coefficient mapping through the PIPE GetLocalPresetCoefficients and LocalTxCoefficientsValid interface whenever the Lane Switch ownership has transitioned to PCIe (from another Controller). Note that if this bit is set while the HPCMQE bit is set, the PCIe-SIP Controller would only perform the query once. Unlike the HPCMQE bit, the PCIe-SIP Controller would not clear this bit after completing the query over the PIPE interface. Register Attribute: Static.

17.6.81 Power Control Enable (PCE)—Offset 428h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 9h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved (RSVD):** Reserved for Force Isolate and Reset Together. This bit is not used. The timing between isolate and reset can be controller through PGCBCTL register.
5	0h RW	**Hardware Autonomous Enable (HAE):** Hardware Autonomous Enable (HAE): If set, and the corresponding per-LTSSM state power gating enable bit is also set, then controller power gating will be done when the controller is idle and the controller power gating condition is met in that particular LTSSM state. Refer to PCIEPMECTL2 register for the per-LTSSM state power gating enable bit. If either this bit. is not set or the corresponding per-LTSSM state power gating enable bit is not set, then controller power gating will not be done in that LTSSM state. Note: For each x4 instance, only the value from Port 0 is used. NOTE: If this bit is set, then bits[lb]2:0[rb] must be '000.
4	0h RO	**Reserved (RSVD_1):** Reserved for Force Isolate and Reset Together. This bit is not used. The timing between isolate and reset can be controller through PGCBCTL register.
3	1h RW/L	**Sleep Enable (SE):** Sleep Enable (SE): If clear, Sleep indication to the retention flops will never assert. If set, Sleep indication will be assert to the retention flops as part of the hardware autonomous controller power gating entry flow.
2	0h RO	**Reserved (RSVD_2):** Reserved for D3-Hot Enable. Not supported. RTD3 is supported instead.
1	0h RO	**Reserved (RSVD_3):** Reserved for D0i3 Enable. No support for D0i3.
0	1h RW	**PMC Request Enable (PMCRE):** PMC Request Enable (PMCRE): When set, the controller will only power gate when pmc_[lt]ip[gt]_sw_pg_req_b = '0 and hardware autonomous controller power gating conditions are met. When clear, controller will power gate immediately when the hardware autonomous controller power gating conditions are met regardless of the state of pmc_[lt]ip[gt]_sw_pg_req_b.

17.6.82 PGCB Control1 (PGCBCTL1)—Offset 42Ch

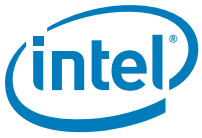
This register specifies the minimum number of delay clocks the PGCB should wait between various states.
Note: For each x4 instance, only the value from Port 0 is used.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 14155555h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved for cfg_trsvd0. Not applicable since frc_clk_srst_en is tied to '0.
29:28	1h RW	**cfg_trstup2frcclks (trstup2frcclks):** cfg_trstup2frcclks(cfg_trstup2frcclks): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
27:26	1h RW	**cfg_tclksonack_cp (tclksonack_cp):** cfg_tclksonack_cp(cfg_tclksonack_cp): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
25:24	0h RO	**Reserved (RSVD_1):** Reserved for cfg_tclksoffack_srst. Not applicable since frc_clk_srst_en is tied to 0.
23:22	0h RO	**Reserved (RSVD_2):** Reserved for cfg_tclksonack_srst. Not applicable since frc_clk_srst_en is tied to 0.
21:20	1h RW	**cfg_tpokup (tpokup):** cfg_tpokup(cfg_tpokup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
19:18	1h RW	**cfg_tpokdown (tpokdown):** cfg_tpokdown(cfg_tpokdown): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks



Bit Range	Default & Access	Field Name (ID): Description
17:16	1h RW	**cfg_tlatchdis (tlatchdis):** cfg_tlatchdis(cfg_tlatchdis): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
15:14	1h RW	**cfg_tsleepinactiv (tsleepinactiv):** cfg_tsleepinactiv(cfg_tsleepinactiv): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
13:12	1h RW	**cfg_tinaccrstup (tinaccrstup):** cfg_tinaccrstup(cfg_tinaccrstup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
11:10	1h RW	**cfg_taccrstup (taccrstup):** cfg_taccrstup(cfg_taccrstup): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
9:8	1h RW	**cfg_tlatchen (tlatchen):** cfg_tlatchen(cfg_tlatchen): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
7:6	1h RW	**cfg_tdeisolate (tdeisolate):** cfg_tdeisolate(cfg_tdeisolate): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
5:4	1h RW	**cfg_trstdown (trstdown):** cfg_trstdown(cfg_trstdown): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
3:2	1h RW	**cfg_tisolate (tisolate):** cfg_tisolate(cfg_tisolate): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
1:0	1h RW	**cfg_tsleepact (tsleepact):** cfg_tsleepact(cfg_tsleepact): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

17.6.83 PGCB Control2 (PGCBCTL2)—Offset 430h

This register specifies the minimum number of delay clocks the PGCB should wait between various states.
Note: For each x4 instance, only the value from Port 0 is used.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 54h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** Reserved.
7:6	1h RW	**cfg_trsvd4 (trsvd4):** cfg_trsvd4(cfg_trsvd4): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
5:4	1h RW	**cfg_trsvd3 (trsvd3):** cfg_trsvd3(cfg_trsvd3): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks
3:2	1h RW	**cfg_trsvd2 (trsvd2):** cfg_trsvd2(cfg_trsvd2): '00: 1 clock '01: 2 clocks '10: 8 clocks '11: 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	**Reserved (RSVD_1):** Reserved for cfg_trsvd1. Not applicable since frc_clk_srst_en is tied to 0.

17.6.84 Equalization Configuration 1 (EQCFG1)—Offset 450h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 3102h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Recovery Entry Count (REC):** Recovery Entry Count (REC): This field indicates the value of the Recovery Entry Counter. This is a 1-based counter. Software must read this register multiple times. The value is valid only if the same value is read out on both of the reads.
23	0h RW	**Recovery Entry and Idle Framing Error Count Enable (REIFECE):** Recovery Entry and Idle Framing Error Count Enable (REIFECE): This bit, when set by software turns on the Recovery Entry Counter and the per-lane Idle Framing Error Counter. The counters are reset when this bit is cleared. This bit is expected to be used by the Software Preset/Coefficient Search tool but is not precluded to be used for other debug purpose. The value of the Recovery Entry Count can be read through EQCFG1.REC field. The value of the Idle Framing Error Count can be read through the Monitor Mux register.
22	0h RW	**Quiesce Guarantee (QG):** Quiesce Guarantee (QG): When set, the Quiesce Guarantee bit in the transmitted TS2 Ordered Set will be set in Recovery.RcvrCfg. When clear, the Quiesce Guarantee bit in the transmitted TS2 Ordered Set will be clear. In all other states, the Quiesce Guarantee bit is Reserved.
21	0h RW	**Link Equalization Request SMI Enable (LERSMIE):** Link Equalization Request SMI Enable (LERSMIE): When set, this bit enables the generation of an SMI to indicate that the Link Equalization Request bit has been set. This mode is meant for survivability purpose such that BIOS can be invoked to address the Re-Equalization request.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Reset EIEOS Interval Count (REIC):** Reset EIEOS Interval Count(REIC): When set, allows the root port to restrict the device from sending EIEOS until after 65536 TS1 Ordered Sets have been transmitted in Phase 3 of the Link Equalization, in the window when the receiver is evaluating the remote transmitter settings..
19	0h RW	**Link Equalization Bypass (LEB):** Link Equalization Bypass (LEB): When set, the root port will never initiate entry to Recovery.Equalization state. This includes never send EQ TS2 in Recovery.RcvrCfg that could cause the device to set start_equalization_w_preset variable. Note: This bit only affects the initial autonomous transition to Link Equalization state when equalization_done_8GT_data_rate = 0. This bit does not affect the software-direction to re-perform Link Equalization.
18	0h RW	**Link Equalization Phase 2 and 3 Bypass (LEP23B):** Link Equalization Phase 2 and 3 Bypass(LEP23B): When set, bypasses the Phase 2 and Phase 3 of Link Equalization. Once Phase 1 is completed, Root Port transitions from Phase 1 directly to Recovery.RcvrLock.
17	0h RW	**Link Equalization 3 Bypass (LEP3B):** Link Equalization 3 Bypass(LEP3B): When set, bypasses the Phase 3 of Link Equalization. Once Phase 2 is completed, Root Port transitions from Phase 2 directly to Recovery.RcvrLock.
16	0h RW	**Remote Transmit Link Equalization Preset/Coefficient Evaluation Bypass (RTLEPCEB):** Remote Transmit Link Equalization Preset/Coefficient Evaluation Bypass (RTLEPCEB): When set, this bit disables the Hardware Autonomous Preset/ Coefficient Search mechanism to search for the best Preset or Coefficient by traversing the Preset or Coefficient List and checking the receiver eye width margin for each of the settings. Instead, the Preset/Coefficient values used by the remote Transmitter will be accepted and the Link Equalization phase will be completed after one round of receiver link training, excluding margining. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Remote Transmitter Preset Coefficient Override Enable (RTPCOE):** Remote Transmitter Preset Coefficient Override Enable (RTPCOE): When set, this bit disables the hardware mechanism to search for the best Preset or Coefficient by traversing the Preset or Coefficient List and checking the receiver eye width margin for each of the settings. Instead, the Preset or Coefficient values specified by the override fields are used. If RTPCL1.PCM = 1, the Preset Override values for each lanes is derived from the following register fields: Lane 0: RTPCL1.RTPRECL0PL0. Lane 1: RTPCL1.RTPOSTCL0PL1. Lane 2: RTPCL1.RTPRECL1PL2. Lane 3: RTPCL1.RTPOSTCL1PL3. If RTPCL1.PCM = 0, the Coefficient Override values for each lanes is derived from the following register fields: Lane 0: RTPCL1.RTPRECL0PL0 and RTPCL1.RTPOSTCL0PL1. Lane 1: RTPCL1.RTPRECL1PL2 and RTPCL1.RTPOSTCL1PL3. Lane 2: RTPCL1.RTPRECL2PL4 and RTPCL2.RTPOSTCL2PL5. Lane 3: RTPCL2.RTPRECL3PL6 and RTPCL2.RTPOSTCL3PL7. BIOS must ensure that the corresponding RTPCL* registers above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
14	0h RW	**Link Equalization Request SCI Enable (LERSCIE):** Link Equalization Request SCI Enable (LERSCIE): When set, this bit enables the generation of an SCI to indicate that the Link Equalization Request bit has been set. This mode is meant for survivability purpose such that SCI handler can be invoked to address the Re-Equalization request.

Bit Range	Default & Access	Field Name (ID): Description
13	1h RW/1S/V	**Hardware Preset to Coefficient Mapping Query Enable (HPCMQE):** Hardware Preset to Coefficient Mapping Query Enable(HPCMQE): When set, the controller will query the Preset to Coefficient mapping through the PIPE GetLocalPresetCoefficients and LocalTxCoefficientsValid interface whenever this bit transitions from 0 to 1. The default of this register bit is 1, indicating that the Preset to Coefficient mapping query will be done on the PIPE interface once coming out of reset. Controller will then update the Preset-Coefficient Mapping registers with the corresponding Coefficient, for each Preset. Controller will also update the LFFS Local LF and Local FS field with the local PHY LF and FS values. Hardware will clear this bit when the Preset to Coefficient mapping query over the PIPE interface is completed. If the Hardware Preset to Coefficient Mapping mechanism is never enabled, the value of the Preset to Coefficient mapping configured by BIOS through the Preset-Coefficient Mapping registers will be used instead of querying through the PIPE interface. Note: BIOS should check to ensure that this field is cleared before enabling Controller Power Gating or mod-PHY Power Gating.
12	1h RO/V	**Hardware Autonomous Equalization Done (HAED):** Hardware Autonomous Equalization Done(HAED): This bit will be cleared when Hardware Autonomous Preset/Coefficient Search starts and will be set when Hardware Autonomous Preset/Coefficient Search is done. This bit is polled by software to ensure that the Hardware Autonomous Preset/Coefficient Search is done before proceeding with the next software sequencing. Some of the Hardware Autonomous Preset/ Coefficient search algorithm may involve the hardware initiating multiple speed change to allow multiple iterations of Link Equalization to be done with different Preset/Coefficient lists. This bit will remain cleared until the iterations are done.

Bit Range	Default & Access	Field Name (ID): Description
11:8	1h RW	**Receiver Wait Time For New Equalization Value Evaluation (RWTNEVE):** Receiver Wait Time For New Equalization Value Evaluation (RWTNEVE): For Downstream Port: This field specifies the amount of time the receiver will wait after entering Phase 3 and sending the new Preset or Coefficient values through the TS1 Ordered Sets before validating the Block Alignment and eventually evaluate the incoming ordered sets (RXEqEval on the PIPE interface asserts). For Upstream Port: This field specifies the amount of time the receiver will wait after entering Phase 2 and sending the new Preset or Coefficient values through the TS1 Ordered Sets before validating the Block Alignment and eventually evaluate the incoming ordered sets (RXEqEval on the PIPE interface asserts). For both Upstream and Downstream Port, this field also specifies the amount of time the receiver will wait after entering Phase 1 before instructing the receiver to adapt to the incoming ordered sets. For Loopback Master: This field specifies the amount of time the receiver will wait after instructing the Loopback Slave to apply a specific Preset through EQ TS1. 0h: 500 ns. 1h: 1 us. 2h: 2 us. 3h: 3 us. 4h: 4 us. : : Fh:15 us.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**EQ TS2 in Recovery.ReceiverConfig Enable (EQTS2IRRC):** EQ TS2 in Recovery.ReceiverConfig Enable(EQTS2IRRC): When set, enables the transmitter to send EQ TS2 in Recovery.RcvrCfg state even when equalization_done_8GT_data_rate variable is 1b, provided that the Downstream Port advertised 8.0 GT/s data rate support in Recovery.RcvrLock, and 8.0 GT/s data rate support has been advertised in the Configuration.Complete or Recovery.RcvrCfg substates by the Upstream Port since exiting the Detect state, and eight consecutive TS1 or TS2 Ordered Sets were received on any configured Lane prior to entry to this substate with speed_change bit set to 1b. When clear, the transmitter can only send EQ TS2 if equalization_done_8GT_data_rate variable is 0b and the Downstream Port advertised 8.0 GT/s data rate support in Recovery.RcvrLock, and 8.0 GT/s data rate support has been advertised in the Configuration.Complete or Recovery.RcvrCfg substates by the Upstream Port since exiting the Detect state, and eight consecutive TS1 or TS2 Ordered Sets were received on any configured Lane prior to entry to this substate with speed_change bit set to 1b. When this bit is used, hardware must ensure that the start_equalization_w_preset variable are in the correct state to ensure that the components on both sides of the link are never out of sync.
6:4	0h RO	**Reserved (RSVD):** Reserved
3	0h RW	**Link EQ Phase 1 Transmit Coefficient Settling Policy (LEQP1TCSP):** Link EQ Phase 1 Transmit Coefficient Settling Policy(LEQP1TCSP): When operating in GEN3 data rate and there is a software/hardware request to re-perform Link Equalization through the Recovery.RcvrLock to Recovery.Equalization arc, PCIe spec requires that the downstream port transmitter switch to the setting specified by the Downstream Port Lane X Transmitter Preset registers in Phase 1. This switching is happening while the downstream port is still actively transmitting TS1 and the upstream port is only required to sample 2 TS1 to determine the next sub-state to transition to. Since the new coefficient setting can take up to 256 ns to settle, the 2 TS1 sampled by the upstream port may be incorrect causing the two LTSSM to be out of sync. When this bit is set, the RP will continue to send EIEOS until the local transmitter setting has settled (specified by PHYCTL2.TXCFGCHGWAIT) before sending TS1 as required in Recovery.Equalization Phase 1. When this bit is clear, the RP will send TS1 with EC = 01 in Recovery.Equalization Phase 1 even though the transmitter setting is still settling.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Multi-Fragment Linear and Nine-Tile List Enable (MFLNTL):** Multi-Fragment Linear and Nine-Tile List Enable(MFLNTL): When set in Hardware Autonomous Linear Preset/Coefficient Search mode, the full Preset/Coefficient List will be traversed in multiple fragments, where each fragments is done in separate entry to Recovery. This is used in the case where a longer dwelling time is required for a particular Preset/Coefficient (configured through EQCFG2.PCET). Subsequent Preset/Coefficient entries within the list that could not be covered within that Recovery session will be covered in subsequent re-entries into Recovery. When set in Hardware Autonomous Nine-Tiles Search mode, the 9-tiles list that could not be covered within that Recovery session will be covered in subsequent re-entries into Recovery.
1	1h RW	**Transmitter Use Preset Policy (TUPP):** Transmitter Use Preset Policy(TUPP): This field applies to the Link Equalization Phase where the local transmitter setting is being adjusted. When set, the transmitted TS1 Use Preset bit will be set if the remote device requests the local transmitter to apply specific Preset(instead of Coefficient). When clear, the Use Preset bit will not be set in this case. Note: This bit must be set before changing speed to GEN3 data rate.
0	0h RW	**Receiver Use Preset Policy (RUPP):** Receiver Use Preset Policy(RUPP): This field applies to the Link Equalization Phase where the remote transmitter setting is being adjusted. When set, the received TS1 Use Preset bit will be checked. When clear, the Use Preset bit in the received TS1 will be ignored. Note: This bit must be set before changing speed to GEN3 data rate.

17.6.85 Remote Transmitter Preset Coefficient List 1 (RTPCL1)—Offset 454h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Preset/Coefficient Mode (PCM):** Preset/Coefficient Mode (PCM): This bit defines whether the Preset List or Coefficient List should be sent to the remote TX to adjust the remote TX setting. For Downstream Port, this is used in Phase 3 of the Link Equalization. For Upstream Port, this is used in Phase 2 of the Link Equalization. The list of coefficient or preset is configurable through the Remote Transmitter Preset Coefficient List [lb]1:4[rb] registers. When this bit is set, Coefficient Mode is enabled and the Remote Transmitter Preset Coefficient List [lb]1:4[rb] registers contain the Coefficient List. When this bit is clear, Preset Mode is enabled and the Remote Transmitter Preset Coefficient List [lb]1:3[rb] registers contain the Preset List.
30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 2/Preset List 4 (RTPRECL2PL4):** Remote Transmitter Pre-Cursor Coefficient List 2/Preset List 4 (RTPRECL2PL4): For Downstream Port: This field defines the pre-cursor coefficient List 2 or Preset List 4 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 2 or Preset List 4 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Remote Transmitter Post-Cursor Coefficient List 1/Preset List 3 (RTPOSTCL1PL3):** Remote Transmitter Post-Cursor Coefficient List 1/Preset List 3 (RTPOSTCL1PL3): For Downstream Port: This field defines the post-cursor coefficient List 1 or Preset List 3 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 1 or Preset List 3 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
17:12	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 1/Preset List 2 (RTPRECL1PL2):** Remote Transmitter Pre-Cursor Coefficient List 1/Preset List 2 (RTPRECL1PL2): For Downstream Port: This field defines the pre-cursor coefficient List 1 or Preset List 2 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 1 or Preset List 2 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Remote Transmitter Post-Cursor Coefficient List 0/Preset List 1 (RTPOSTCL0PL1):** Remote Transmitter Post-Cursor Coefficient List 0/Preset List 1 (RTPOSTCL0PL1): For Downstream Port: This field defines the post-cursor coefficient List 0 or Preset List 1 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 0 or Preset List 1 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
5:0	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 0/Preset List 0 (RTPRECL0PL0):** Remote Transmitter Pre-Cursor Coefficient List 0/Preset List 0 (RTPRECL0PL0): For Downstream Port: This field defines the pre-cursor coefficient List 0 or Preset List 0 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 0 or Preset List 0 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.6.86 Remote Transmitter Preset Coefficient List 2 (RTPCL2)—Offset 458h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Remote Transmitter Post-Cursor Coefficient List 4/Preset List 9 (RTPOSTCL4PL9):** Remote Transmitter Post-Cursor Coefficient List 4/Preset List 9(RTPOSTCL4PL9): For Downstream Port: This field defines the post-cursor coefficient List 4 or Preset List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 4 or Preset List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 4/Preset List 8 (RTPRECL4PL8):** Remote Transmitter Pre-Cursor Coefficient List 4/Preset List 8 (RTPRECL4PL8): For Downstream Port: This field defines the pre-cursor coefficient List 4 or Preset List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 4 or Preset List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Post-Cursor Coefficient List 3/Preset List 7 (RTPOSTCL3PL7):** Remote Transmitter Post-Cursor Coefficient List 3/Preset List 7 (RTPOSTCL3PL7): For Downstream Port: This field defines the post-cursor coefficient List 3 or Preset List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 3 or Preset List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 3/Preset List 6 (RTPRECL3PL6):** Remote Transmitter Pre-Cursor Coefficient List 3/Preset List 6 (RTPRECL3PL6): For Downstream Port: This field defines the pre-cursor coefficient List 3 or Preset List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 3 or Preset List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Post-Cursor Coefficient List 2/Preset List 5 (RTPOSTCL2PL5):** Remote Transmitter Post-Cursor Coefficient List 2/Preset List 5 (RTPOSTCL2PL5): For Downstream Port: This field defines the post-cursor coefficient List 2 or Preset List 5 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 2 or Preset List 5 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.6.87 Remote Transmitter Preset Coefficient List 3 (RTPCL3)—Offset 45Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 7 (RTPRECL7):** Remote Transmitter Pre-Cursor Coefficient List 7 (RTPRECL7): For Downstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Post-Cursor Coefficient List 6 (RTPOSTCL6):** Remote Transmitter Post-Cursor Coefficient List 6 (RTPOSTCL6): For Downstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 6 (RTPRECL6):** Remote Transmitter Pre-Cursor Coefficient List 6 (RTPRECL6): For Downstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Post-Cursor Coefficient List 5 (RTPOSTCL5):** Remote Transmitter Post-Cursor Coefficient List 5 (RTPOSTCL5): For Downstream Port: This field defines the pre-cursor coefficient List 5 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 5 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 5/Preset List 10 (RTPRECL5PL10):** Remote Transmitter Pre-Cursor Coefficient List 5/Preset List 10 (RTPRECL5PL10): For Downstream Port: This field defines the pre-cursor coefficient List 5 or Preset List 10 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 5 or Preset List 10 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.6.88 Remote Transmitter Preset Coefficient List 4 (RTPCL4)—Offset 460h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Remote Transmitter Post-Cursor Coefficient List 9 (RTPOSTCL9):** Remote Transmitter Post-Cursor Coefficient List 9 (RTPOSTCL9): For Downstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 9 (RTPRECL9):** Remote Transmitter Pre-Cursor Coefficient List 9 (RTPRECL9): For Downstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Post-Cursor Coefficient List 8 (RTPOSTCL8):** Remote Transmitter Post-Cursor Coefficient List 8 (RTPOSTCL8): For Downstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
11:6	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 8 (RTPRECL8):** Remote Transmitter Pre-Cursor Coefficient List 8 (RTPRECL8): For Downstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Remote Transmitter Post-Cursor Coefficient List 7 (RTPOSTCL7):** Remote Transmitter Post-Cursor Coefficient List 7 (RTPOSTCL7): For Downstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

17.6.89 Figure Of Merit Status (FOMS)—Offset 464h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved (RSVD):** Reserved
30:29	0h RW	**Index (I):** Index (I): The FOMV field will reflect the Figure of Merit Scoreboard value for the index specified by this field. List N below refers to the Figure of Merit values captured in the scoreboard corresponding to the Preset or Coefficient List N. 00b: Index 0 =[gt] {List 2, List 1, List 0}. 01b: Index 1 =[gt] {List 5, List 4, List 3}. 10b: Index 2 =[gt] {List 8, List 7, List 6}. 11b: Index 3 =[gt] {Rsvd, List 10, List 9}.

Bit Range	Default & Access	Field Name (ID): Description
28:24	0h RW	**Lane Number (LN):** Lane Number (LN): The FOMV field will reflect the Figure of Merit Scoreboard value for the lane specified by this field. 00000b: Lane 0. 00001b: Lane 1. 00010b: Lane 2. 00011b: Lane 3. Others: Reserved.
23:0	0h RO/V	**Figure of Merit Scoreboard Value (FOMSV):** Figure of Merit Scoreboard Value (FOMSV): This field will reflect the Figure of Merit Scoreboard entries referenced by the Lane Number and Index field in this register. For example, when Index == 00b, this field will reflect the Figure of Merit values for Lane specified in Lane Number field and the encoding of this field is as shown below: 23:16: Figure of Merit for Preset/Coefficient List 2. 15:8 : Figure of Merit for Preset/Coefficient List 1. 7:0 : Figure of Merit for Preset/Coefficient List 0. If the Receiver Eye Width margining completes with error, the value of Figure of Merit should reflect 0x00.

17.6.90 Hardware Autonomous Equalization Control (HAEQ)—Offset 468h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: A0080E00h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Ah RW	**Hardware Autonomous Preset/Coefficient Count Per-Iteration (HAPCCPI):** Hardware Autonomous Preset/Coefficient Count Per-Iteration(HAPCCPI): This field defines the number of Preset/Coefficient to be traversed for every iteration of Recovery Equalization. For the Linear Mode, EQCFG2.HAPCSB specifies the total number of Presets/Coefficients to be checked in total while this field specifies the number of Presets/Coefficients to be checked per-iteration of Recovery Equalization. Hardware will enter Recovery Equalization and check the number of Presets/Coefficients specified by this field. Once that is done, hardware will exit Recovery Equalization and trigger another entry to Recovery Equalization to check another set of Presets/Coefficients. This goes on until the total number of Presets/Coefficients are checked. For Nine-Tiles Mode, EQCFG2.NTIC specifies the number of 9-tiles iterations, which indirectly specifies the total number of Presets/ Coefficients to be checked in total. Similar to Linear Mode, this field specifies the number of Presets/Coefficients to be checked per-iteration of Recovery Equalization. 0h: 1 Preset/Coefficient per-iteration. 1h: 2 Preset/Coefficient per-iteration. 2h: 3 Preset/Coefficient per-iteration. ... 9h: 10 Preset/Coefficient per-iteration. Ah: 11 Preset/Coefficient per-iteration. Others: Reserved.
27:20	0h RW	**FOM Error Mask (FOMEM):** FOM Error Mask(FOMEM): The FOM error counter will be masked(thus ignoring the FOM error) for all the FOM values prior to the FOM value specified in this field. If this field is programmed to 00h, this mechanism is disabled. This bit must be configured before training to GEN3 data rate.

Bit Range	Default & Access	Field Name (ID): Description
19	1h RW	**MAC FOM Control (MACFOMC):** MAC FOM Control(MACFOMC): When set, MAC controls the advancement of the FOM values completely while in the Link Equalization mode. For downstream port, this is done in Phase 3 and for upstream port, this is done in Phase 2 of the Link Equalization. The dwelling time for each of the FOM values are programmed through the remaining fields of this register. When enabled, the hardware will start in Speeding Mode, where it will instruct the PHY to increment the FOM value after the Speeding Latency specified by HAEQ.SL field. Once the FOM value matches HAEQ.SFOMFM, the hardware switches from Speeding Mode to Dwelling Mode. In Dwelling mode, the MAC will instruct PHY to increment the FOM value after the Dwelling Latency specified by HAEQ.DL field. This is done until the link equalization phase is completed. When cleared, PHY controls the advancement of the FOM values completely, during the Link Equalization mode. This bit must be configured before training to GEN3 data rate.
18:16	0h RW	**Speeding Latency (SL):** Speeding Latency(SL): Specifies the residency time for a particular FOM value in Speeding Mode. 000b: 192 ns. 001b: 256 ns. 010b: 512 ns. 011b: 1 us. 100b: 2 us. 101b: 4 us. 110b: 8 us. 111b: 16 us. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.
15:8	Eh RW	**Dwelling Latency (DL):** Dwelling Latency(DL): Specifies the residency time for a particular FOM value in Dwelling Mode. 00h: 2 us. 01h: 4 us. 02h: 6 us. ... FFh: 512 us. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Starting FOM For Margining (SFOMFM):** Starting FOM For Margining(SFOMFM): Define the FOM where MAC switches from Speeding Mode to Dwelling Mode after hitting the programmed FOM value in Hardware Autonomous Preset/Coefficient mode. This register is only applicable when HAEC.MACFOMC is set and must be configured before setting the HAEC.MACFOMC bit.

17.6.91 Local Transmitter Coefficient Override 1 (LTCO1)—Offset 470h

Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane bits are not used.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD):** Reserved
25	0h RW	**Lane 1 Transmitter Coefficient Override Enable (L1TCOE):** Lane 1 Transmitter Coefficient Override Enable (L1TCOE): When set, the transmitter coefficient override values LTPCO1.L1TPRECO and LTPCO1.L1TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO1.L1TPRECO and LTPCO1.L1TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Lane 0 Transmitter Coefficient Override Enable (L0TCOE):** Lane 0 Transmitter Coefficient Override Enable (L0TCOE): When set, the transmitter coefficient override values LTPCO1.L0TPRECO and LTPCO1.L0TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO1.L0TPRECO and LTPCO1.L0TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
23:18	0h RW	**Lane 1 Transmitter Post-Cursor Coefficient Override (L1TPOSTCO):** Lane 1 Transmitter Post-Cursor Coefficient Override (L1TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L1TCOE = 1.
17:12	0h RW	**Lane 1 Transmitter Pre-Cursor Coefficient Override (L1TPRECO):** Lane 1 Transmitter Pre-Cursor Coefficient Override (L1TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L1TCOE = 1.
11:6	0h RW	**Lane 0 Transmitter Post-Cursor Coefficient Override (L0TPOSTCO):** Lane 0 Transmitter Post-Cursor Coefficient Override (L0TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L0TCOE = 1.
5:0	0h RW	**Lane 0 Transmitter Pre-Cursor Coefficient Override (L0TPRECO):** Lane 0 Transmitter Pre-Cursor Coefficient Override (L0TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO1.L0TCOE = 1.

17.6.92 Local Transmitter Coefficient Override 2 (LTCO2)—Offset 474h

Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane bits are not used.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved (RSVD):** Reserved
25	0h RW	**Lane 3 Transmitter Coefficient Override Enable (L3TCOE):** Lane 3 Transmitter Coefficient Override Enable (L3TCOE): When set, the transmitter coefficient override values LTPCO2.L3TPRECO and LTPCO2.L3TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO2.L3TPRECO and LTPCO2.L3TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.
24	0h RW	**Lane 2 Transmitter Coefficient Override Enable (L2TCOE):** Lane 2 Transmitter Coefficient Override Enable (L2TCOE): When set, the transmitter coefficient override values LTPCO2.L2TPRECO and LTPCO2.L2TPOSTCO are used as the local transmitter coefficient value, and the coefficient requested by the remote device is ignored. BIOS must ensure that the corresponding LTPCO2.L2TPRECO and LTPCO2.L2TPOSTCO fields above are programmed correctly prior to setting this bit. BIOS must ensure that the link runs in either GEN1 or GEN2 when the registers are configured. Once the register programming are done, BIOS should set the Perform Equalization bit to '1, Target Link Speed register to 0011b and initiate Link Retrain by setting the Retrain Link bit to 1b.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Lane 3 Transmitter Post-Cursor Coefficient Override (L3TPOSTCO):** Lane 3 Transmitter Post-Cursor Coefficient Override (L3TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L3TCOE = 1.
17:12	0h RW	**Lane 3 Transmitter Pre-Cursor Coefficient Override (L3TPRECO):** Lane 3 Transmitter Pre-Cursor Coefficient Override (L3TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L3TCOE = 1
11:6	0h RW	**Lane 2 Transmitter Post-Cursor Coefficient Override (L2TPOSTCO):** Lane 2 Transmitter Post-Cursor Coefficient Override (L2TPOSTCO): For Downstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the post-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L2TCOE = 1.
5:0	0h RW	**Lane 2 Transmitter Pre-Cursor Coefficient Override (L2TPRECO):** Lane 2 Transmitter Pre-Cursor Coefficient Override (L2TPRECO): For Downstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 2. For Upstream Port: This field defines the pre-cursor coefficient override values to be used for the local TX in Phase 3. This override value is used only when LTPCO2.L2TCOE = 1.

17.6.93 GEN3 L0s Control (G3L0SCTL)—Offset 478h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: C00281Eh

Bit Range	Default & Access	Field Name (ID): Description
31:24	Ch RW	**Gen3 Active State L0s Preparation Latency (G3ASL0SPL):** Gen3 Active State L0s Preparation Latency (G3ASL0SPL) Determines how long the Link layer has to indicate IDLE before the link initialization and control logic enters L0s 00: 0 clocks (enter immediately) 01: 1 clock ... FF: 255 clocks The value of this register is only used if the Gen3 L0s Entry Idle Control register is set to [quote]11[/quote] and operating in Gen3 mode.
23:22	0h RW	**Gen3 L0s Entry Idle Control (G3L0SIC):** Gen3 L0s Entry Idle Control (G3L0SIC): 00 : Allow entry into L0s after the link has been idle for a period of time equal to of the received N_FTS total entry time (1/4 * N_FTS * 16) 01 : Allow entry into L0s after the link has been idle for for a period of time equal to of the received N_FTS total entry time (1/2 * N_FTS * 16) 10 : Allow entry after the link has been idle for for a period of time equal to the received N_FTS total entry time (N_FTS * 16) 11: Allow entry into L0s after the link has been idle for a period specified in the Gen3 Active State L0s Preparation Latency register. This register is only applied when operating in Gen3 mode.
21:16	0h RO	**Reserved (RSVD):** Reserved
15:8	28h RW	**Gen3 Unique Clock N_FTS (G3UCNFTS):** Gen3 Unique Clock N_FTS (G3UCNFTS): Number of Fast Training Sequence ordered sets required to be transmitted for a root port Receiver to exit L0s in a unique (non-common) clock configuration (LCTL.CCC=0) when operating in Gen3 mode. The N_FTS value is sent in TS1 and TS2 training sets during link training. 00: 0 FTS sets 01: 1 FTS set ... FF: 255 FTS sets Note: When operating in Mobile Express mode, the output of this field is not used to determine the number of FTS to be sent on TXL0s exit. Mobile Express does not support Fast Training Sequence. Instead, SYNC is used to achieve bit lock. However, the output of this field is still used in L0s Entry Idle Control registers to determine the L0s Entry Idle latency.

Bit Range	Default & Access	Field Name (ID): Description
7:0	1Eh RW	**Gen3 Common Clock N_FTS (G3CCNFTS):** Gen3 Common Clock N_FTS (G3CCNFTS): Number of Fast Training Sequence ordered sets required to be transmitted for a root port Receiver to exit L0s in a common clock configuration (LCTL.CCC=1) when operating in Gen3 mode. The N_FTS value is sent in TS1 and TS2 training sets during link training. 00: 0 FTS sets 01: 1 FTS set ... FF: 255 FTS sets Note: When operating in Mobile Express mode, the output of this field is not used to determine the number of FTS to be sent on TXL0s exit. Mobile Express does not support Fast Training Sequence. Instead, SYNC is used to achieve bit lock. However, the output of this field is still used in L0s Entry Idle Control registers to determine the L0s Entry Idle latency.

17.6.94 Equalization Configuration 2 (EQCFG2)—Offset 47Ch

Size:32 bits
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: A001h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Nine-Tiles Iteration Count (NTIC):** Nine-Tiles Iteration Count(NTIC): This field specifies the number of iterations to perform the 9-tiles search. Each iteration involves evaluating the neighboring 9-tiles for the best Preset/Coefficient margin and then use the Preset/Coefficient as the centerpoint to identify and evaluate the next 9-tiles. 00h: 1 iteration. 01h: 2 iterations. 02h: 3 iterations. ... FFh: 256 iterations.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**Equalization Margining Disable (EMD):** Equalization Margining Disable(EMD):When set, the Root Port will not request the PHY to perform Receiver Margining by asserting RxEqEval on each Preset/ Coefficient list traversed. This allows the receiver to still measure the Bit Error Count without margining. When cleared, the Root Port will request the PHY to perform Receiver Margining by asserting RxEqEval. This field is only valid when operating in Hardware Autonomous Preset/Coefficient Search mode. The Preset/Coefficient list will still be traversed to the end.
22:20	0h RW	**Nine-Tiles Step Size (NTSS):** Nine-Tiles Step Size(NTSS): This field specifies the step size used to identify the surrounding 9-tiles to be used for margining. 000b: 1 step. 001b: 2 steps. 010b: 3 steps. 011b: 4 steps. 100b: 5 steps. 101b: 6 steps. 110b: 7 steps. 111b: 8 steps. Each of the steps is measured in terms of incrementing of decrementing the coefficient values.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RW	**Preset/Coefficient Evaluation Timeout (PCET):** Preset/ Coefficient Evaluation Timeout(PCET): This field specifies the evaluation timeout for a single Preset/Coefficient in the List when operating in Hardware Autonomous Preset/Coefficient Search mode. By spec, the evaluation phase must be completed before the 24 ms timeout. To support 12 Presets (11 Presets + 1 final good Preset), each Preset will have up to 2 ms for evaluation. This field allows the 2 ms timer to be programmable. This is useful if the EQCFG2.HAPCSB limits the Preset/Coefficient List to smaller than 12 such that each Preset/Coefficient could be evaluated for a time longer than 2 ms. 0h: 2 ms. 1h: 2.5 ms. 2h: 3 ms. 3h: 3.5 ms. 4h: 4 ms. 5h: 4.5 ms. 6h: 5 ms. 7h: 6 ms. 8h: 7 ms. 9h: 8 ms. Ah: 9 ms. Bh:10 ms. Ch:11 ms. Dh:21 ms. Eh:22 ms. Fh:23 ms.
15:12	Ah RW	**Hardware Autonomous Preset/Coefficient Search Bound (HAPCSB):** Hardware Autonomous Preset/Coefficient Search Bound(HAPCSB): This field defines the number of Preset/ Coefficient List to be traversed, out of 11 for Presets or out of 10 for Coefficients. The Preset/Coefficient list will be traversed from List 0 to the value specified by this field in incremental order. This field allows equalization to be done with smaller set of Preset/ Coefficient list and each of the Preset/Coefficient list could be run for a longer time. 0h: Preset/Coefficient List 0 only. 1h: Preset/Coefficient List 0 - 1. 2h: Preset/Coefficient List 0 - 2. : : 9h: Preset/Coefficient List 0 - 9. Ah: Preset List 0 - 10/Coefficient List 0-9. Others: Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**Nine-Tiles Equalization Mechanism Enable (NTEME):** Nine-Tiles Equalization Mechanism Enable(NTEME): When set, the Nine-Tiles Equalization Mechanism is enabled when running in Hardware Autonomous Preset/Coefficient Search Mode.
10	0h RW	**Mid-Point Equalization Mechanism Enable (MPEME):** Mid-Point Equalization Mechanism Enable(MPEME): When set, the Mid-Point Equalization Mechanism is enabled when running in Hardware Autonomous Preset/Coefficient Search Mode.
9:8	0h RW	**Receiver Eye Width Margin Error Threshold Multiplier (REWMETM):** Receiver Eye Width Margin Error Threshold Multiplier (REWMETM): This field specifies the multiplier to be used with REWMET field. 00b: Multiply REWMET by 1 (effectively no multiplier). 01b: Multiply REWMET by 10. 10b: Multiply REWMET by 100. 11b: Multiply REWMET by 1000.
7:0	1h RW	**Receiver Eye Width Margin Error Threshold (REWMET):** Receiver Eye Width Margin Error Threshold (REWMET): This field specifies the count threshold which upon exceeded, will cause controller to terminate the current iteration of Receiver Eye Width Margining and move on to the next preset or coefficient in the list. The value specified in this field will need to be multiplied with the multiplier specified in REWMETM field to get the final threshold values. 00h: Terminate on 1 x REWMETM errors. 01h: Terminate on 2 x REWMETM errors. 02h: Terminate on 4 x REWMETM errors. 03h: Terminate on 6 x REWMETM errors. : : FEh: Terminate on 508 x REWMETM errors. FFh: Never terminate. Rely on PHY to terminate the margining.

17.6.95 Monitor Mux (MM)—Offset 480h

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO/V	**Monitor Signal State (MSST):** Monitor Signal State(MSST): The internal signal groupings selected by MM.MSS field is reflected in this field. The intention of this monitor signal is provide software a capability to monitor some of the GEN3 related parameters accumulated by the controller through the Link Equalization that are too costly to be mapped to dedicated registers. Implementation MUST NEVER expose any security related information through this Monitor Mux.
7:0	0h RW	**Monitor Signal Select (MSS):** Monitor Signal Select(MSS): This field is essentially the mux select for the Monitor Signal mux. Setting this field allows different monitor signals to be muxed out and readable by software through the MM.MSST field.

17.6.96 Lane0 P0 and P1 Preset-Coefficient Mapping (L0P0P1PCM)—Offset 500h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.97 Lane0 P1, P2 and P3 Preset-Coefficient Mapping (L0P1P2P3PCM)—Offset 504h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.98 Lane0 P3 and P4 Preset-Coefficient Mapping (L0P3P4PCM)—Offset 508h

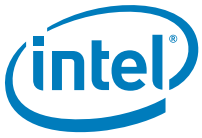
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.99 Lane0 P5 and P6 Preset-Coefficient Mapping (L0P5P6PCM)—Offset 50Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.100 Lane0 P6, P7 and P8 Preset-Coefficient Mapping (L0P6P7P8PCM)—Offset 510h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.101 Lane0 P8 and P9 Preset-Coefficient Mapping (L0P8P9PCM)—Offset 514h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

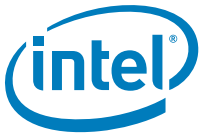
Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.102 Lane0 P10 Preset-Coefficient Mapping (L0P10PCM)—Offset 518h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.



Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.103 Lane0 LF and FS (L0LFFS)—Offset 51Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.104 Lane1 P0 and P1 Preset-Coefficient Mapping (L1P0P1PCM)—Offset 520h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.105 Lane1 P1, P2 and P3 Preset-Coefficient Mapping (L1P1P2P3PCM)—Offset 524h

This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.106 Lane1 P3 and P4 Preset-Coefficient Mapping (L1P3P4PCM)—Offset 528h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.107 Lane1 P5 and P6 Preset-Coefficient Mapping (L1P5P6PCM)—Offset 52Ch

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.108 Lane1 P6, P7 and P8 Preset-Coefficient Mapping (L1P6P7P8PCM)—Offset 530h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.109 Lane1 P8 and P9 Preset-Coefficient Mapping (L1P8P9PCM)—Offset 534h

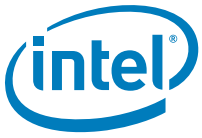
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.110 Lane1 P10 Preset-Coefficient Mapping (L1P10PCM)—Offset 538h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.111 Lane1 LF and FS (L1LFFS)—Offset 53Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.112 Lane2 P0 and P1 Preset-Coefficient Mapping (L2P0P1PCM)—Offset 540h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.113 Lane2 P1, P2 and P3 Preset-Coefficient Mapping (L2P1P2P3PCM)—Offset 544h

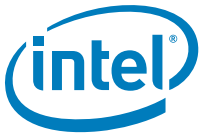
This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.114 Lane2 P3 and P4 Preset-Coefficient Mapping (L2P3P4PCM)—Offset 548h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.115 Lane2 P5 and P6 Preset-Coefficient Mapping (L2P5P6PCM)—Offset 54Ch

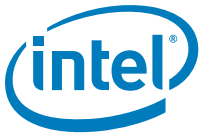
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.116 Lane2 P6, P7 and P8 Preset-Coefficient Mapping (L2P6P7P8PCM)—Offset 550h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.117 Lane2 P8 and P9 Preset-Coefficient Mapping (L2P8P9PCM)—Offset 554h

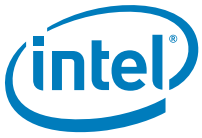
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.118 Lane2 P10 Preset-Coefficient Mapping (L2P10PCM)—Offset 558h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.119 Lane2 LF and FS (L2LFFS)—Offset 55Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.120 Lane3 P0 and P1 Preset-Coefficient Mapping (L3P0P1PCM)—Offset 560h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 1 Pre-Cursor Coefficient (P1PRECC):** Preset 1 Pre-Cursor Coefficient (P1PRECC): Pre-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 1 Cursor Coefficient (P1CC):** Preset 1 Cursor Coefficient (P1CC): Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 0 Post-Cursor Coefficient (P0PSTCC):** Preset 0 Post-Cursor Coefficient (P0PSTCC): Post-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 0 Pre-Cursor Coefficient (P0PRECC):** Preset 0 Pre-Cursor Coefficient (P0PRECC): Pre-Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 0 Cursor Coefficient (P0CC):** Preset 0 Cursor Coefficient (P0CC): Cursor coefficient for Preset 0. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.121 Lane3 P1, P2 and P3 Preset-Coefficient Mapping (L3P1P2P3PCM)—Offset 564h

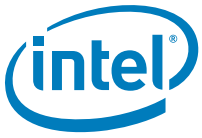
This register must be configured prior to enabling 8.0 GT/s data rate
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 3 Cursor Coefficient (P3CC):** Preset 3 Cursor Coefficient (P3CC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 2 Post-Cursor Coefficient (P2PSTCC):** Preset 2 Post-Cursor Coefficient (P2PSTCC): Post-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 2 Pre-Cursor Coefficient (P2PRECC):** Preset 2 Pre-Cursor Coefficient (P2PRECC): Pre-Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 2 Cursor Coefficient (P2CC):** Preset 2 Cursor Coefficient (P2CC): Cursor coefficient for Preset 2. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 1 Post-Cursor Coefficient (P1PSTCC):** Preset 1 Post-Cursor Coefficient (P1PSTCC): Post-Cursor coefficient for Preset 1. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.122 Lane3 P3 and P4 Preset-Coefficient Mapping (L3P3P4PCM)—Offset 568h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RW	**Preset 4 Post-Cursor Coefficient (P4PSTCC):** Preset 4 Post-Cursor Coefficient (P4PSTCC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 4 Pre-Cursor Coefficient (P4PRECC):** Preset 4 Pre-Cursor Coefficient (P4PRECC): Pre-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 4 Cursor Coefficient (P4CC):** Preset 4 Cursor Coefficient (P4CC): Post-Cursor coefficient for Preset 4. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 3 Post-Cursor Coefficient (P3PSTCC):** Preset 3 Post-Cursor Coefficient (P3PSTCC): Post-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 3 Pre-Cursor Coefficient (P3PRECC):** Preset 3 Pre-Cursor Coefficient (P3PRECC): Pre-Cursor coefficient for Preset 3. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.123 Lane3 P5 and P6 Preset-Coefficient Mapping (L3P5P6PCM)—Offset 56Ch

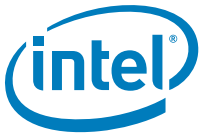
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 6 Pre-Cursor Coefficient (P6PRECC):** Preset 6 Pre-Cursor Coefficient (P6PRECC): Pre-Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 6 Cursor Coefficient (P6CC):** Preset 6 Cursor Coefficient (P6CC): Cursor coefficient for Preset 6. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 5 Post-Cursor Coefficient (P5PSTCC):** Preset 5 Post-Cursor Coefficient (P5PSTCC): Post-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 5 Pre-Cursor Coefficient (P5PRECC):** Preset 5 Pre-Cursor Coefficient (P5PRECC): Pre-Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 5 Cursor Coefficient (P5CC):** Preset 5 Cursor Coefficient (P5CC): Cursor coefficient for Preset 5. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.124 Lane3 P6, P7 and P8 Preset-Coefficient Mapping (L3P6P7P8PCM)—Offset 570h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved.
29:24	0h RW	**Preset 8 Cursor Coefficient (P8CC):** Preset 8 Cursor Coefficient (P8CC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 7 Post-Cursor Coefficient (P7PSTCC):** Preset 7 Post-Cursor Coefficient (P7PSTCC): Post-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 7 Pre-Cursor Coefficient (P7PRECC):** Preset 7 Pre-Cursor Coefficient (P7PRECC): Pre-Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 7 Cursor Coefficient (P7CC):** Preset 7 Cursor Coefficient (P7CC): Cursor coefficient for Preset 7. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 6 Post-Cursor Coefficient (P6PSTCC):** Preset 6 Post-Cursor Coefficient (P6PSTCC): Post-Cursor coefficient for Preset 6. The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.125 Lane3 P8 and P9 Preset-Coefficient Mapping (L3P8P9PCM)—Offset 574h

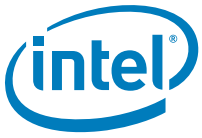
This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved,
29:24	0h RW	**Preset 9 Post-Cursor Coefficient (P9PSTCC):** Preset 9 Post-Cursor Coefficient (P9PSTCC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
23:18	0h RW	**Preset 9 Pre-Cursor Coefficient (P9PRECC):** Preset 9 Pre-Cursor Coefficient (P9PRECC): Pre-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
17:12	0h RW	**Preset 9 Cursor Coefficient (P9CC):** Preset 9 Cursor Coefficient (P9CC): Post-Cursor coefficient for Preset 9. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.



Bit Range	Default & Access	Field Name (ID): Description
11:6	0h RW	**Preset 8 Post-Cursor Coefficient (P8PSTCC):** Preset 8 Post-Cursor Coefficient (P8PSTCC): Post-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
5:0	0h RW	**Preset 8 Pre-Cursor Coefficient (P8PRECC):** Preset 8 Pre-Cursor Coefficient (P8PRECC): Pre-Cursor coefficient for Preset 8. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.126 Lane3 P10 Preset-Coefficient Mapping (L3P10PCM)—Offset 578h

This register must be configured prior to enabling 8.0 GT/s data rate.
This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved (RSVD):** Reserved
17:12	0h RW	**Preset 10 Post-Cursor Coefficient (P10PSTCC):** Preset 10 Post-Cursor Coefficient (P10PSTCC): Post-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
11:6	0h RW	**Preset 10 Pre-Cursor Coefficient (P10PRECC):** Preset 10 Pre-Cursor Coefficient (P10PRECC): Pre-Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Preset 10 Cursor Coefficient (P10CC):** Preset 10 Cursor Coefficient (P10CC): Cursor coefficient for Preset 10. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

17.6.127 Lane3 LF and FS (L3LFFS)—Offset 57Ch

This register is not applicable when operating in Mobile Express mode.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 19 **Function:** 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD):** Reserved
29:24	0h RO/V	**Remote PHY Full Swing Value (RPFSV):** Remote PHY Full Swing Value (RPFSV): The FS value for remote PHY. This value is logged from Lane 0.
23:22	0h RO	**Reserved (RSVD_1):** Reserved
21:16	0h RO/V	**Remote PHY Low Frequency Value (RPLFV):** Remote PHY Low Frequency Value (RPLFV): The LF value for remote PHY. This value is logged from Lane 0.
15:14	0h RO	**Reserved (RSVD_2):** Reserved
13:8	0h RW	**Local PHY Full Swing Value (LPFSV):** Local PHY Full Swing Value (LPFSV): The FS value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to FS value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.
7:6	0h RO	**Reserved (RSVD_3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:0	0h RW	**Local PHY Low Frequency Value (LPLFV):** Local PHY Low Frequency Value (LPLFV): The LF value for local PHY. Note: BIOS is responsible to ensure that the values programmed to the Preset-Coefficient Mapping table meets the requirement defined in PCI Express base specification with respect to LF value programmed in this field. This field must be configured prior to enabling 8.0 GT/s data rate. Note: The default value of this field is modified by the hardware to reflect the value queried from local PHY when Hardware Preset to Coefficient Mapping is completed.

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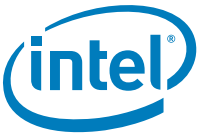


18 SATA

18.1 Registers Summary

Table 18-1. Summary of sata_configreg_top Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4h	5h	Command (CMD)—Offset 4h	0h
6h	7h	Device Status (STS)—Offset 6h	2B0h
8h	8h	Revision ID (RID)—Offset 8h	0h
9h	9h	Programming Interface (PI)—Offset 9h	1h
Ch	Ch	Cache Line Size (CLS)—Offset Ch	0h
Dh	Dh	Master Latency Timer (MLT)—Offset Dh	0h
Eh	Eh	Header Type (HTYPE)—Offset Eh	0h
10h	13h	MSI-X Table Base Address (MXTBA)—Offset 10h	0h
14h	17h	MXP Base Address (MXPBA)—Offset 14h	0h
18h	1Bh	SCMDBA (SCMDBA)—Offset 18h	1h
1Ch	1Fh	SCTLBA (SCTLBA)—Offset 1Ch	1h
20h	23h	AHCI Index Data Pair Base Address (AIDPBA)—Offset 20h	1h
24h	27h	AHCI Base Address (ABAR)—Offset 24h	0h
2Ch	2Fh	Sub System Identifiers (SS)—Offset 2Ch	0h
34h	34h	Capabilities Pointer (CAP)—Offset 34h	80h
3Ch	3Dh	Interrupt Information (INTR)—Offset 3Ch	100h
70h	71h	PCI Power Management Capability ID (PID)—Offset 70h	A801h
74h	75h	PCI Power Management Control and Status (PMCS)—Offset 74h	8h
80h	81h	Message Signalled Interrupt Identifier (MID)—Offset 80h	7005h
82h	83h	Message Signalled Interrupt Message Control (MC)—Offset 82h	0h
88h	89h	Message Signaled Interrupt Message Data (MD)—Offset 88h	0h
90h	93h	Port Mapping Register (MAP)—Offset 90h	0h
9Ch	9Fh	SATA General Configuration (SATAGC)—Offset 9Ch	0h
A0h	A0h	SATA Initialization Register Index (SIRI)—Offset A0h	0h
A4h	A7h	SATA Initialization Register Data (SIRD)—Offset A4h	0h
A8h	ABh	Serial ATA Capability Register 0 (SATACR0)—Offset A8h	100012h
ACh	AFh	Serial ATA Capability Register 1 (SATACR1)—Offset ACh	48h
B0h	B1h	FLR Capability ID (FLRCID)—Offset B0h	13h
B2h	B3h	FLR Capability Length and Version (FLRCAP)—Offset B2h	306h
B4h	B5h	FLR Control (FLRCTL)—Offset B4h	0h
C0h	C3h	Scratch Pad (SP)—Offset C0h	0h
D0h	D1h	MSI-X Identifiers (MXID)—Offset D0h	11h
D2h	D3h	MSI-X Message Control (MXC)—Offset D2h	0h
D4h	D7h	MSI-X Table Offset / Table BIR (MXT)—Offset D4h	0h

Table 18-1. Summary of sata_configreg_top Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
D8h	DBh	MSI-X PBA Offset / PBA BIR (MXP)—Offset D8h	0h
E0h	E3h	BIST FIS Control/Status (BFCS)—Offset E0h	0h
E4h	E7h	BIST FIS Transmit Data 1 (BFTD1)—Offset E4h	0h
E8h	EBh	BIST FIS Transmit Data 2 (BFTD2)—Offset E8h	0h
F8h	FBh	Manufacturing ID (MFID)—Offset F8h	8000FB1h

18.1.1 Command (CMD)—Offset 4h

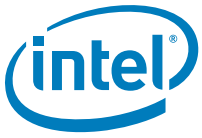
Command

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. When set, internal INTx# will not be generated. When cleared, internal INTx# are generated if there is an interrupt and MSI is not enabled.
9	0h RO	**Fast Back-to-Back Enable (FBE):** Reserved.
8	0h RW	**SERR# Enable (SEE):** When set to 1, the HBA is allowed to generate SERR# on DPD or SATAGC.URD event that is enabled for SERR# generation. When cleared to 0, it is not.
7	0h RO	**Wait Cycle Enable (WCC):** Reserved.
6	0h RW	**Parity Error Response Enable (PEE):** When set, the SATA Controller will corrupt the outbound DATA FIS CRC if a forwarded data parity error is indicated.
5	0h RO	**VGA Palette Snooping Enable (VGA):** Reserved.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved.
3	0h RO	**Special Cycle Enable (SCE):** Reserved.
2	0h RW	**Bus Master Enable (BME):** Controls the SATA Controller's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands.



Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Memory Space Enable (MSE):** Controls access to the SATA Controller's target memory space (for AHCI).
0	0h RW	**I/O Space Enable (IOSE):** Controls access to the SATA Controller's target I/O space.

18.1.2 Device Status (STS)—Offset 6h

Device Status

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 18 **Function:** 0

Default: 2B0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the SATA Controller detects a parity error on its interface.
14	0h RW/1C/V	**Signalled System Error (SSE):** Set when SATA Controller generates an SERR#.
13	0h RW/1C/V	**Received Master-Abort Status (RMA):** Set when the SATA Controller receives a master abort to a cycle it generated.
12	0h RW/1C/V	**Received Target-Abort Status (RTA):** Set when the SATA Controller receives a target abort to a cycle it generated.
11	0h RW/1C/V	**Signalled Target-Abort Status (STA):** This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that will never signal Target-Abort do not need to implement this bit.
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** Controls the device select time for the SATA Controller's PCI interface.
8	0h RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the SATA Controller, as a master, either detects a parity error or sees the parity error line asserted, and the parity error response bit (bit 6 of the command register) is set. This bit can only be set on read completions received from the backbone where there is a parity error.
7	1h RO	**Fast Back-to-Back Capable (FBC):** Reserved.
6	0h RO	Reserved.
5	1h RO	**66 MHz Capable (RSV):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	1h RO	**Capabilities List (CL):** Indicates the presence of a capabilities list. The minimum requirement for the capabilities list must be PCI power management for the SATA Controller.
3	0h RO/V	**Interrupt Status (IS):** Reflects the state of INTx# messages, IRQ14 or IRQ15. This bit is set when the interrupt is to be asserted. This bit is a 0 after the interrupt is cleared
2:0	0h RO	Reserved.

18.1.3 Revision ID (RID)—Offset 8h

Revision ID

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Revision ID (RID):** Indicates stepping of the host controller hardware.

18.1.4 Programming Interface (PI)—Offset 9h

Programming Interface

Access Method

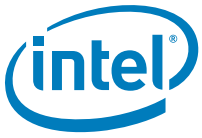
Type: CFG Register (Size: 8 bits)	**Device:** 18 **Function:** 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
7:0	1h RO	**Interface (IF):** If CC.SCC=06h(AHCI mode), it indicates that this is an AHCI HBA that has a major revision of 1 (as specified in the AHCI Version register). If CC.SCC=04h(RAID mode), it indicates that there is no programming interface(IF=00h). Internally, under this condition, the SATA controller is in native mode and its I/O spaces are only accessible through the I/O BARs.

18.1.5 Cache Line Size (CLS)—Offset Ch

Cache Line Size



Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Cache Line Size (CLS):** This register has no meaning for the SATA controller.

18.1.6 Master Latency Timer (MLT)—Offset Dh

Master Latency Timer

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Master Latency Timer (MLT):** This register has no meaning for the SATA controller.

18.1.7 Header Type (HTYPE)—Offset Eh

Header Type

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi-function Device (MFD):** Indicates this controller is not part of a multi-function device.
6:0	0h RO	**Header Layout (HL):** Indicates that the controller uses a target device layout.

18.1.8 MSI-X Table Base Address (MXTBA)—Offset 10h

This BAR is used to allocate 32K, 16K or 8K Memory space for the MSI-X Table. The Memory space size is determined by BIOS by making bit-14 and bit-13 Read-Only '1' or Read-Write '0' based on SATAGC.MSS[1:0].

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Base Address (BA):** Base address of memory space.
14	0h RW/V	**Base Address Bit 14 (BAB14):** When SATAGC.MSS[1:0]=00, this bit is Read Only '0' else it's Read Write '0'.
13	0h RW/V	**Base Address Bit 13 (BAB13):** When SATAGC.MSS[1:0]=00 or 01, this bit is Read Only '0' else it's Read Write '0'.
12:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable.
2:1	0h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for Memory space.

18.1.9 MXP Base Address (MXPBA)—Offset 14h

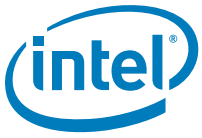
This BAR is used to allocate 256-byte Memory space for the MSI-X PBA.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Base Address (BA):** Base address of memory space (aligned to 256B).
7:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable.
2:1	0h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for Memory space.



18.1.10 SCMDBA (SCMDBA)—Offset 18h

BAR2 register define a 8-byte I/O space but this space is not implemented. Accesses to this space will get master abort. This space is created to workaround an issue in RST.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:3	0h RW	**Base Address (BAR):** Base address of the I/O space.
2:1	0h RO	Reserved.
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

18.1.11 SCTLBA (SCTLBA)—Offset 1Ch

BAR3 register define a 4-byte I/O space but this space is not implemented. Accesses to this space will get master abort. This space is created to workaround an issue in RST.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:2	0h RW	**Base Address (BAR):** Base address of the I/O space.
1	0h RO	Reserved.
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

18.1.12 AHCI Index Data Pair Base Address (AIDPBA)—Offset 20h

This BAR is used to allocate I/O space for the AHCI index/data pair mechanism. Note that hardware does not clear the BA bits (including BA4) when switching from IDE mode to non-IDE mode or vice versa. BIOS is responsible for clearing those bits to 0 since the number of writable bits changes after mode switching.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:5	0h RW	**Base Address (BA):** Base address of the I/O space.
4:1	0h RO	Reserved.
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

18.1.13 AHCI Base Address (ABAR)—Offset 24h

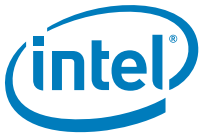
This register represents a memory BAR allocating space for the AHCI memory registers. Note that bit[31:16] of this register must be programmed to a value greater than 0 to ensure the memory is mapped to an address of 1 MBytes and greater (i.e. ABAR must be 00010000h or greater). Otherwise, memory cycle targeting the ABAR range may not be accepted.. The Memory space size is determined by BIOS by making bit 15:11 Read-Only '1' or Read-Write '0' based on SATAGC.ASSEL[1:0].

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RW	**Base Address (BA):** Base address of register memory space.
18	0h RW	**Base Address Bit 18 (BAB18):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 256K, this bit is Read Only '0' else it's Read Write '0'.
17	0h RW	**Base Address Bit 17 (BAB17):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 128K, this bit is Read Only '0' else it's Read Write '0'.



Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Base Address Bit 16 (BAB16):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 64K, this bit is Read Only '0' else it's Read Write '0'.
15	0h RW	**Base Address Bit 15 (BAB15):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 32K, this bit is Read Only '0' else it's Read Write '0'.
14	0h RW	**Base Address Bit 14 (BAB14):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 16K, this bit is Read Only '0' else it's Read Write '0'.
13:11	0h RW	**Base Address Bit 13-11 (BAB1311):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 2K, this bit is Read Only '0' else it's Read Write '0'.
10:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable
2:1	0h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

18.1.14 Sub System Identifiers (SS)—Offset 2Ch

This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion. This register is not reset by FLR.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

18.1.15 Capabilities Pointer (CAP)—Offset 34h

Capabilities Pointer

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 18 **Function:** 0

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Capability Pointer (CP):** Indicates that the first capability pointer offset is offset 80h (the Message Signalled Interrupt capability). The following capability structures are linked by default: CAP.CP -> 80h (MSI) -> D0h (MSI-X)-> 70h (PCI Power) -> A8h (SATA) -> 00h end. BIOS may alter the capability structure list above (by programming a leading capability structure's Next Pointer field) if BIOS wants to bypass any specific capability. The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.

18.1.16 Interrupt Information (INTR)—Offset 3Ch

Interrupt Information

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 18 **Function:** 0

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
15:8	1h RW/O	**Interrupt Pin (IPIN):** This register tells which interrupt pin the device function uses. A value of 1 corresponds to INTA#. A value of 2 corresponds to INTB#. A value of 3 corresponds to INTC#. A value of 4 corresponds to INTD#. This register is not reset by FLR.
7:0	0h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. Interrupt Line register is not reset by FLR.

18.1.17 PCI Power Management Capability ID (PID)—Offset 70h

PCI Power Management Capability ID

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 18 **Function:** 0

Default: A801h

Bit Range	Default & Access	Field Name (ID): Description
15:8	A8h RW/L	**Next Capability (NEXT):** A8h is location of the Serial ATA Capability structure. The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.
7:0	1h RO	**Cap ID (CID):** Indicates that this pointer is a PCI power management capability.

18.1.18 PCI Power Management Control and Status (PMCS)—Offset 74h

PCI Power Management Control and Status

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 18 **Function:** 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**PME Status (PMES):** This bit is set when a PME event is to be requested, and if this bit is set and PMEE is set, a PME# will be generated. This register field is not reset by FLR.
14:9	0h RO	Reserved.
8	0h RW	**PME Enable (PMEE):** When set, the SATA controller generates PME# from D3HOT on a wake event. Note: Software is advised to clear PMEE together with PMES prior to changing CC.SCC thru SATAGC.SMS. This register field is not reset by FLR.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NSFRST):** A 1 indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration context is preserved. Upon transition from the D3hot to the D0 state initialized state, no additional operating system intervention is required to preserve configuration context beyond writing to the PowerState bits. Regardless of this bit, the controller transition from D3hot to the D0 by a system or bus segment reset will return to the state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the SATA Controller and to set a new power state. The values are: 00 = D0 state; 11 = D3HOT state. When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a 10 or 01 to these bits, the write will be ignored. Refer to PCI PM specification section 8.2.2. on software requirements in ensuring I/O space, memory space and Bus Master are disabled prior to entering D3 state.

18.1.19 Message Signalled Interrupt Identifier (MID)—Offset 80h

Message Signalled Interrupt Identifier

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 18 **Function:** 0

Default: 7005h

Bit Range	Default & Access	Field Name (ID): Description
15:8	70h RW/L	**Next Pointer (NEXT):** Indicates the next item in the list is the PCI power management pointer. This is the recommended value. BIOS may program this field to A8h indicating that the next item is Serial ATA Capability structure. The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.
7:0	5h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

18.1.20 Message Signalled Interrupt Message Control (MC)—Offset 82h

Message Signalled Interrupt Message Control

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
6:4	0h RO	**Multiple Message Enable (MME):** When this field is cleared to 000 (and MSIE is set), only a single MSI message will be generated for all SATA ports, and bits [15:0] of the message vector will be driven from MD[15:0].
3:1	0h RO	**Multiple Message Capable (MMC):** Not supported.
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. Note that CMD.ID bit has not effect on MSI. Software must clear this bit to 0 to disable MSI first before changing the number of messages allocated in the MMC field.

18.1.21 Message Signaled Interrupt Message Data (MD)—Offset 88h

Message Signaled Interrupt Message Data

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word of the data bus of the MSI memory write transaction.

18.1.22 Port Mapping Register (MAP)—Offset 90h

Port Mapping Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW/O	**SATA Port 7 Disable (SPD7):** Similar to SPD0 but for port 7. This bit is RO-one if ANY of the fuse/strap/gpio condition below is true else this bit is RW-zero. PCIe/SATA muxing for port 7 based on fuses, soft straps and GPIO does not select SATA. This bit is only applicable to project(s): that has port 7 physically.
22	0h RW/O	**SATA Port 6 Disable (SPD6):** Similar to SPD0 but for port 6. This bit is RO-one if ANY of the fuse/strap/gpio condition below is true else this bit is RW-zero. PCIe/SATA muxing for port 6 based on fuses, soft straps and GPIO does not select SATA. This bit is only applicable to project(s): that has port 6 physically.
21	0h RW/O	**SATA Port 5 Disable (SPD5):** Similar to SPD0 but for port 5. This bit is RO-one if ANY of the fuse/strap/gpio condition below is true else this bit is RW-zero. PCIe/SATA muxing for port 5 based on fuses, soft straps and GPIO does not select SATA. This bit is only applicable to project(s): that has port 5 physically.
20	0h RW/O	**SATA Port 4 Disable (SPD4):** Similar to SPD0 but for port 4. This bit is RO-one if ANY of the fuse/strap/gpio condition below is true else this bit is RW-zero. PCIe/SATA muxing for port 4 based on fuses, soft straps and GPIO does not select SATA. This bit is only applicable to project(s): that has port 4 physically.
19	0h RW/O	**SATA Port 3 Disable (SPD3):** Similar to SPD0 but for port 3. This bit is RO-one if ANY of the fuse/strap/gpio condition below is true else this bit is RW-zero. 1.Fuse FFSATA7 (disable port 2 & 3). 2.Fuse FFSATA8 (disable port 1 & 3). 3. PCIe/SATA muxing for port 3 based on fuses, soft straps and GPIO does not select SATA. This bit is only applicable to project(s): that has port 3 physically.
18	0h RW/O	**SATA Port 2 Disable (SPD2):** Similar to SPD0 but for port 2. This bit is RO-one if ANY of the fuse/strap/gpio condition below is true else this bit is RW-zero. 1.Fuse FFSATA7 (disable port 2 & 3). 2.PCIe/SATA muxing for port 3 based on fuses, soft straps and GPIO does not select SATA. This bit is only applicable to project(s): that has port 3 physically.
17	0h RW/O	**SATA Port 1 Disable (SPD1):** Similar to SPD0 but for port 1. This bit is RO-one if ANY of the fuse/strap/gpio condition below is true else this bit is RW-zero. 1.Fuse FFSATA8 (disable port 1 & 3). 2.PCIe/SATA muxing for port 3 based on fuses, soft straps and GPIO does not select SATA. This bit is only applicable to project(s): that has port 1 physically.
16	0h RW/O	**SATA Port 0 Disable (SPD0):** A 1 prevents the SATA port from being enabled via config PCS.PxE. Write of 1 to PCS.PxE has no effect when the corresponding SPD[x] bit is 1.In preventing a port(s) from being enabled, BIOS shall first configure MAP.SPDx. And only then BIOS configures the PCS.PxE. This field is not reset by FLR. This bit is only applicable to project(s): that has port 0 physically.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h RW	**Port Clock Disable (PCD):** When any of these bits is set to 1, the backbone clock driven to the associated port logic is gated and will not toggle. When this bit is cleared to 0, all clocks to the associated port logic will operate normally. Assignment of the bits is: Bit 7: Port 7, this bit is applicable to projects: that has port 7 physically; Bit 6: Port 6, this bit is only applicable to project(s): that has port 6 physically; Bit 5: Port 5, this bit is only applicable to project(s): that has port 5 physically; Bit 4: Port 4, this bit is only applicable to project(s): that has port 4 physically; Bit 3: Port 3, this bit is only applicable to project(s): that has port 3 physically; Bit 2: Port 2, this bit is only applicable to project(s): that has port 2 physically; Bit 1: Port 1, this bit is only applicable to project(s): that has port 1 physically; Bit 0: Port 0, this bit is only applicable to project(s): That has port 0 physically. If a particular port is not available, software shall set the corresponding bit to 1. Software can also set the corresponding bit(s) to 1 after disabling particular port(s). Software cannot set the PCD[port x]=1 if the corresponding config PCS.PxE=1 or AHCI MMIO GHC.PI[x]=1.

18.1.23 SATA General Configuration (SATAGC)—Offset 9Ch

SATA General Configuration

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/O	**Register Lock (REGLOCK):** BIOS can set this bit to 1 to lock the following registers with RW/L attribute: CAP,CP, MID.NEXT, PIE.NEXT, SATACR0.NEXT. Once locked the register attribute of above list changes from RW/L to RO holding the existing value. BIOS is required to program this field to 1 prior to handle off to OS. If BIOS needs the SATA host controller to change operation a few times (i.e. changing CC.SCC mode) and need different capability structures for each specific operation mode, BIOS need not activate the lock until BIOS is ready to hand off to OS. BIOS may need to separate write access to this byte offset (x9Fh) from write to the lower 3-byte of the dword (x9C-9Eh) if there is a need to program the lower 3-byte dword location early during boot process. This field is not reset by FLR.
30:18	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Do SERR Disable (DOSERRD):** When 1,SERR reporting is disabled (DO_SERR Sideband message sending is disabled or SERR# Wire is supressed. STS.SSE setting is not governed by this policy bit). When 0, SERR reporting is enabled (DO_SERR Sideband message sending is enabled or SERR# Wire is not supressed)
16	0h RW	**SATA Mode Select (SMS):** Software (SW) programs these bits to control the mode in which the SATA HBA should operate: 0b = AHCI mode; 1b = RAID mode; Notes : SW shall not manipulate SATAGC.SMS during runtime operation; i.e. the OS will not do this. The BIOS may choose to switch from one mode to another during POST; AHCI mode may be selected when RAID feature is enabled by fuse; RAID mode may only be selected when FFSATA5 & FFSATA3 (concatenated value not indicating No RAID); This register field is not reset by FLR.
15	0h RW	**Data Phase Parity Error Enable (DPPEE):** When 1, IOSF data phase parity error handling is enabled. When 0, the data phase parity error handling is disabled.
14:12	0h RW	**Write Request_Size Select/Max_Payload_Size (WRRSELMPS):** These two bits select the max write request size that SATA host controller will initiate for DMA write to memory. SATA host controller will internally break up larger write request based on these bits. The request is address-aligned to the selected size. Defined encodings for this field are: 000b = 128 address aligned bytes max payload size; 111b = 64 address aligned bytes max payload size. All other values are reserved for SATA host controller. This field is not reset by FLR.
11	0h RW	**Command Parity Error Enable (CPEE):** When 1, command parity error handling is enabled. When 0, the command parity error handling is disabled.
10	0h RW	**SATA Controller Function Disable (SCFD):** BIOS program this bit to 1 to disable the SATA Controller function. When 0, SATA Controller function is enabled. When disable, SATA Host Controller will not claimed the register access targeting its Configuration Space. In IOSF primary Fabric Decode scheme, it's expected BIOS also program the corresponding bit used by the Fabric Decoder accordingly hence both SATA SIP and Fabric Decoder are in sync, and BIOS need to program this bit before programming the one in Fabric Decoder. Once this bit is set, BIOS isnot able to revert it back to Function Enable until next round of platform reset.
9	0h RW	**Unsupported Request Reporting Enable (URRE):** If set to 1 by software, it allows reporting of an Unsupported Request as a system error. If both URRE and PCI configuration SERR# Enable registers are set to a 1, then the agent must set the Signalled System Error bit in the PCI Status register and send a DO_SERR message in IOSF-SB interface.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C/V	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unsupported Request on IOSF Primary interface that is not considered Advisory Non-Fatal. Cleared to 0 by SW.
7	0h RW/O	**Alternate ID Enable (AIE):** When programmed to 0, HW will report the following device id's: 2822h for desktop or 282Ah for mobile. When programmed to a 1, HW will not report these device id's. Refer to Table 46 and Table 47 for resultant DIDs. Note: Programming this bit to a 1 will prevent the Windows in-box version of the Intel AHCI driver from loading on the platform - will require that the user perform an 'F6' install of the Intel driver that is appropriate for the reported DID. This field is applicable when the AHCI is configured for RAID mode of operation. It has no impact for AHCI and IDE modes of operation. Note: BIOS is recommended to program this bit prior to programming the MAP.SMS field to reflect RAID. This field is reset by PLTRST# and BIOS is required to reprogram the value (either 0 or 1) after resuming from S3, S4 or S5. This insures that the value is properly and cannot be changed during runtime. This field is not reset by FLR.
6	0h RW/O/V	**AIE0 DevID Selection (DEVIDSEL):** This register allows BIOS to select Device ID when AIE=0 and Server Feature (SATA AIE DEVIDSEL) Disable Fuse =0. This bit only has effect in Desktop SKU. In Mobile SKU this bit has no effect at all. Refer to config register offset 09h PI for usage. Note: WBG BIOS is required to program this field to 1 together with the write to the AIE bit in a single configuration write cycle. NOTE: When Server Feature (SATA AIE DEVIDSEL) Disable Fuse is programmed to 1, this disables the writeability of this DEVIDSEL register bit, and becomes RO with a value of 0, which only allows a choice of 2822h. This field is not reset by FLR.
5	0h RW/O	**FLR Capability Selection (FLRCSSEL):** This allows the FLR Capability to be bypassed. Refer to config offset B0h. BIOS is required to program this bit to 1 and config offset A8h SATACR0.NEXT to 00h. This field is not reset by FLR.
4:3	0h RW/O	**MXTBA Size Select (MSS):** These 2 bits select the size of the Memory space for the MSI-X Table defined in BAR 0 (Configuration space offset 10h). MSI-X Table Memory space size is 32k when MSS[1:0]=00, 16k when MSS[1:0]=01, 8k when MSS[1:0]=10. This field is not reset by FLR.
2:0	0h RW/O	**ABAR Size Select (ASSEL):** These 3 bits select the size of the Memory space for the ABAR in BAR 5 (Configuration space offset 24h). ABAR Memory space size is 2k when ASSEL[2:0]=000, 16k when ASSEL[2:0]=001, 32k when ASSEL[2:0]=010, 64k when ASSEL[2:0]=011, 128k when ASSEL[2:0]=100, 256k when ASSEL[2:0]=101, 512k when ASSEL[2:0]=110. This field is not reset by FLR.

18.1.24 SATA Initialization Register Index (SIRI)—Offset A0h

SATA Initialization Register Index

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RW	**Index (IDX):** 6-bit index pointer into the 256-byte space. Data is written into the SIRD register and read from the SIRD register. This point to a DWord register. The byte enables on the SIRD register affect what will be written. Refer to SATA Initialization Register section for detail of the register space.
1:0	0h RO	Reserved.

18.1.25 SATA Initialization Register Data (SIRD)—Offset A4h

SATA Initialization Register Data

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Data (DTA):** 32-bit data value that is written to the register pointed to by SIRI, or read from the register pointed to by SIRI.

18.1.26 Serial ATA Capability Register 0 (SATACR0)—Offset A8h

Note that the SATACR0.NEXT is not changed from RO to become RWO because there is an existing method (SATAGC.FLRCSSEL bit) to bypass the FLR Capability structure. And FLR Capability ID.NEXT is already indicating end of capability structure, it does not need change to be RWO.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 100012h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	1h RO	**Major Revision (MAJREV):** Major revision number of the SATA Capability Pointer implemented.
19:16	0h RO	**Minor Revision (MINREV):** Minor revision number of the SATA Capability Pointer implemented.
15:8	0h RW/L	**Next Capability Pointer (NEXT):** 00h indicating the final item in the Capability List. The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.
7:0	12h RO	**Capability ID (CAP):** The value of 12h has been assigned by the PCI SIG to designate the SATA Capability pointer.

18.1.27 Serial ATA Capability Register 1 (SATACR1)—Offset ACh

Serial ATA Capability Register 1

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 48h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:4	4h RO	**BAR Offset (BAROFST):** Indicates the offset into the BAR where the AHCI Index/Data pair are located (in Dword granularity). The Index and Data I/O registers are located at offset 10h within the I/O space defined by LBAR (BAR4). A value of 004h indicates offset 10h. 000h = 0h offset; 001h = 4h offset; 002h = 8h offset; 003h = Ch offset; 004h = 10h offset; ...; FFFh = 3FFFh offset (max 16 KB)
3:0	8h RO	**BAR Location (BARLOC):** Indicates the absolute PCI Configuration Register address of the BAR containing the Index/ Data pair (in Dword granularity). The Index and Data I/O registers reside within the space defined by LBAR (BAR4) in the SATA controller. A value of 8h indicates offset 20h, which is LBAR (BAR4). 0000 - 0011b = reserved; 0100b = 10h => BAR0; 0101b = 14h => BAR1; 0110b = 18h => BAR2; 0111b = 1Ch => BAR3; 1000b = 20h => AIDPBA; 1001b = 24h => BAR5; 1010 - 1110b = reserved; 1111b = Index/Data pair in PCI Configuration space which is not supported.

18.1.28 FLR Capability ID (FLRCID)—Offset B0h

FLR Capability ID

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 18 **Function:** 0

Default: 13h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Next Capability (NEXT):** 00h indicating the final item in the Capability List.
7:0	13h RO/V	**Capability ID (CID):** The value of this field depends on the FLRCSSEL bit. • SATAGC.FLRCSSEL = 0, Capability ID = 13h. • SATAGC.FLRCSSEL = 1, Capability ID = 00h (capability is bypassed).

18.1.29 FLR Capability Length and Version (FLRCAP)—Offset B2h

This register shall be read-only 0 when SATAGC.FLRCSSEL=1. This register is not reset by FLR.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 18 **Function:** 0

Default: 306h

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	Reserved.
9	1h RW/O	**FLR Capability (FLRCAP):** A 1 in this bit indicates support for Function Level Reset (FLR).
8	1h RW/O	**TXP Capability (TXPCAP):** A 1 in this bit indicates support for the Transactions Pending (TXP) bit. TXP must be supported if FLR is supported.
7:0	6h RO	**Capability Length (CAPL):** This field indicates the # of bytes as required by the PCI spec. It has the value of 06h for the FLR Capability.

18.1.30 FLR Control (FLRCTL)—Offset B4h

This register shall be read-only 0 when SATAGC.FLRCSSEL=1.

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved.
8	0h RO	**Transactions Pending (TXP):** A 1 indicates that the controller has issued Non-Posted request which has not been completed. A 0 indicates that Completions for all non-posted requests have been received by the controller.
7:1	0h RO	Reserved.
0	0h RW	**Initiate FLR (Initiate_FLR):** Used to initiated FLR transition. A write of 1 indicates FLR transition. Since hardware must not respond to any cycles till FLR completion, the value read by software from this bit is 0. Refer to Function Level Reset (FLR) on specifics to SATA.

18.1.31 Scratch Pad (SP)—Offset C0h

Scratch Pad

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DT):** This is a read/write register that is available for software to use. No hardware action is taken on this register.

18.1.32 MSI-X Identifiers (MXID)—Offset D0h

MSI-X Identifiers

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 18 **Function:** 0

Default: 11h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW/L	**Next Pointer (NEXT):** Indicates the next item in the list. This may be other capability pointers or it may be the last item in the list.The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.
7:0	11h RO	**Capability ID (CID):** Capabilities ID indicates this is an MSI-X capability.

18.1.33 MSI-X Message Control (MXC)—Offset D2h

MSI-X Message Control

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**MSI-X Enable (MXE):** If set to '1' and the MSI Enable bit in the MSI Message Control register is cleared to '0', the function is permitted to use MSI-X to request service and is prohibited from using its INTx# pin (if implemented). If cleared to '0', the function is prohibited from using MSI-X to request service.
14	0h RW	**Function Mask (FM):** If set to '1', all of the vectors associated with the function are masked, regardless of their per vector Mask bit states. If cleared to '0', each vector's Mask bit determines whether the vector is masked or not. Setting or clearing the MSI-X Function Mask bit has no effect on the state of the per vector Mask bits.
13:11	0h RO	Reserved.
10:0	0h RO	**Table Size (TS):** This value indicates the size of the MSI-X Table as the value n, which is encoded as n - 1. For example, a returned value of 3h corresponds to a table size of 4..

18.1.34 MSI-X Table Offset / Table BIR (MXT)—Offset D4h

MSI-X Table Offset / Table BIR

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW/O	**Table Offset (TO):** Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X Table. The lower three Table BIR bits are masked off (cleared to 000b) by system software to form a 32-bit Qword-aligned offset.
2:0	0h RO	**Table BIR (TBIR):** This field indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X Table into system memory. A read-only value of '0' means 10h.

18.1.35 MSI-X PBA Offset / PBA BIR (MXP)—Offset D8h

MSI-X PBA Offset / PBA BIR

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW/O	**PBA Offset (PBAO):** Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X PBA. The lower three PBA BIR bits are masked off (cleared to 000b) by software to form a 32-bit Qword-aligned offset.
2:0	0h RO	**PBA BIR (PBIR):** This field indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X PBA into system memory. A read-only value of '1' means 14h.

18.1.36 BIST FIS Control/Status (BFCS)—Offset E0h

BIST FIS Control/Status

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**Port 7 BIST FIS Initiate (P7BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 7, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable the PCS.P7E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s): That has port 7 physically.
16	0h RW	**Port 6 BIST FIS Initiate (P6BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 6, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable the PCS.P6E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s): That has port 6 physically.
15	0h RW	**Port 5 BIST FIS Initiate (P5BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 5, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable the PCS.P5E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s): That has port 5 physically.
14	0h RW	**Port 4 BIST FIS Initiate (P4BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 4, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable PCS.P4E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s): That has port 4 physically.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Port 3 BIST FIS Initiate (P3BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 3, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable the PCS.P3E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s): That has port 3 physically.
12	0h RW	**Port 2 BIST FIS Initiate (P2BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 2, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable PCS.P2E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s): That has port 2 physically.
11	0h RW/1C/V	**BIST FIS Successful (BFS):** This bit is set any time a BIST FIS transmitted by the SATA controller receives an R_OK completion status from the device.
10	0h RW/1C/V	**BIST FIS Failed (BFF):** This bit is set any time that a BIST FIS transmitted by the SATA controller receives an R_ERR completion status from the device.
9	0h RW	**Port 1 BIST FIS Initiate (P1BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 1, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable PCS.P1E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s): That has port 1 physically.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Port 0 BIST FIS Initiate (P0BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 0, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable PCS.P0E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS. This bit is only applicable to project(s): That has port 0 physically.
7:2	0h RW	**BIST FIS Parameters (BFP):** These bits form the contents of the upper 6 bits of the BIST FIS Pattern Definition in the BIST FIS transmitted by the SATA controller. This field is not port specific - its contents will be used for any BIST FIS initiated on the SATA controller. The specific bit definitions are: Bit 7 (T) Far End Transmit mode; bit 6 (A) Align Bypass mode; bit 5 (S) Bypass Scrambling; bit 4 (L) Far End Retimed Loopback; bit 3 (F) Far End Analog Loopback; bit 2 (P) Primitive bit for use with Transmit mode.
1:0	0h RO	Reserved.

18.1.37 BIST FIS Transmit Data 1 (BFTD1)—Offset E4h

BIST FIS Transmit Data 1

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** The data programmed into this register will form the contents of the second DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 2nd DW regardless of whether or not the T bit is indicated in the BFCS register.

18.1.38 BIST FIS Transmit Data 2 (BFTD2)—Offset E8h

BIST FIS Transmit Data 2

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** The data programmed into this register will form the contents of the third DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 3rd DW regardless of whether or not the T bit is set in the BFCS register.

18.1.39 Manufacturing ID (MFID)—Offset F8h

Manufacturing ID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 18 **Function:** 0

Default: 8000FB1h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:24	8h RO/V	**Dot portion of Process ID (DPID):** Indicates the dot. Process is reflected in bits [7:0]. This 8-bit value is received via the IOSF Sideband SetID message.
23:16	0h RO/V	**Stepping Identifier (SID):** This field is incremented for each stepping of the part. Note that this field can be used by software to differentiate steppings when the Revision ID may not change. This is SIP customer implementation specific and SIP customer provides this 8-bit value via the Sideband SetID message.
15:8	Fh RO/V	**Manufacturer Identifier (MID):** This is SIP customer implementation specific and SIP customer provides this 8-bit value via the Sideband SetID message.
7:0	B1h RO/V	**Process/Dot Identifier (PID):** Indicates the Process. Dot is reflected in bits [27:24]. This is SIP customer implementation specific and SIP customer provides this 8-bit value via the Sideband SetID message.

18.2 Registers Summary

Table 18-2. Summary of sata_configreg_top Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
14h	17h	AHCI Data Register (DATA)—Offset 14h	0h

18.2.1 AHCI Data Register (DATA)—Offset 14h

This registers are index into all memory registers defined in Memory Registers and the message buffer used for enclosure management.

Access Method

Type: IO Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** This Data register is a window through which data is read or written to the memory mapped register pointed to by the Index register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the default value is the same as the default value of the register pointed to by Index.

18.3 Registers Summary

Table 18-3. Summary of sata_configreg_top Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	HBA Capabilities (GHC_CAP)—Offset 0h	FF36FF07h
4h	7h	Global HBA Control (GHC)—Offset 4h	80000000h
Ch	Fh	Ports Implemented (GHC_PI)—Offset Ch	0h
10h	13h	AHCI Version (VS)—Offset 10h	10300h
1Ch	1Fh	Enclosure Management Location (EM_LOC)—Offset 1Ch	1600002h
20h	23h	Enclosure Management Control (EM_CTL)—Offset 20h	7010000h
24h	27h	HBA Capabilities Extended (GHC_CAP2)—Offset 24h	3Ch
A0h	A3h	Vendor Specific (VSP)—Offset A0h	48h
A4h	A7h	Vendor-Specific Capabilities Register (VS_CAP)—Offset A4h	1002DEh
A8h	ABh	Remapping Under NVMe (RUN)—Offset A8h	0h
C0h	C3h	RAID Platform ID (RPID)—Offset C0h	311C02h
C4h	C5h	Premium Feature Block (PFB)—Offset C4h	0h
C8h	C9h	SW Feature Mask (SFM)—Offset C8h	3Fh
100h	103h	Port [0-7] Command List Base Address (PxCLB0)—Offset 100h	0h

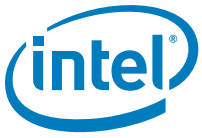


Table 18-3. Summary of sata_configreg_top Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
104h	107h	Port [0-7] Command List Base Address Upper 32-bits (PxCLBU0)—Offset 104h	0h
108h	10Bh	Port [0-7] FIS Base Address (PxFB0)—Offset 108h	0h
10Ch	10Fh	Port [0-7] FIS Base Address Upper 32-bits (PxFBU0)—Offset 10Ch	0h
110h	113h	Port [0-7] Interrupt Status (PxIS0)—Offset 110h	0h
114h	117h	Port [0-7] Interrupt Enable (PxIE0)—Offset 114h	0h
118h	11Bh	Port [0-7] Command (PxCMD0)—Offset 118h	4h
120h	123h	Port [0-7] Task File Data (PxTFD0)—Offset 120h	7Fh
124h	127h	Port [0-7] Signature (PxSIG0)—Offset 124h	FFFFFFFFh
128h	12Bh	Port [0-7] Serial ATA Status (PxSSTS0)—Offset 128h	0h
12Ch	12Fh	Port [0-7] Serial ATA Control (PxSCTL0)—Offset 12Ch	0h
130h	133h	Port [0-7] Serial ATA Error (PxSERR0)—Offset 130h	0h
134h	137h	Port [0-7] Serial ATA Active (PxSACT0)—Offset 134h	0h
138h	13Bh	Port [0-7] Commands Issued (PxCI0)—Offset 138h	0h
13Ch	13Fh	Port [0-7] SNotification (PxSNTF0)—Offset 13Ch	0h
144h	147h	Port [0-7] Device Sleep (PxDEVSLP0)—Offset 144h	1E022852h
180h	183h	Port [0-7] Command List Base Address (PxCLB1)—Offset 180h	0h
184h	187h	Port [0-7] Command List Base Address Upper 32-bits (PxCLBU1)—Offset 184h	0h
188h	18Bh	Port [0-7] FIS Base Address (PxFB1)—Offset 188h	0h
18Ch	18Fh	Port [0-7] FIS Base Address Upper 32-bits (PxFBU1)—Offset 18Ch	0h
190h	193h	Port [0-7] Interrupt Status (PxIS1)—Offset 190h	0h
194h	197h	Port [0-7] Interrupt Enable (PxIE1)—Offset 194h	0h
198h	19Bh	Port [0-7] Command (PxCMD1)—Offset 198h	4h
1A0h	1A3h	Port [0-7] Task File Data (PxTFD1)—Offset 1A0h	7Fh
1A4h	1A7h	Port [0-7] Signature (PxSIG1)—Offset 1A4h	FFFFFFFFh
1A8h	1ABh	Port [0-7] Serial ATA Status (PxSSTS1)—Offset 1A8h	0h
1ACh	1AFh	Port [0-7] Serial ATA Control (PxSCTL1)—Offset 1ACh	0h
1B0h	1B3h	Port [0-7] Serial ATA Error (PxSERR1)—Offset 1B0h	0h
1B4h	1B7h	Port [0-7] Serial ATA Active (PxSACT1)—Offset 1B4h	0h
1B8h	1BBh	Port [0-7] Commands Issued (PxCI1)—Offset 1B8h	0h
1BCh	1BFh	Port [0-7] SNotification (PxSNTF1)—Offset 1BCh	0h
1C4h	1C7h	Port [0-7] Device Sleep (PxDEVSLP1)—Offset 1C4h	1E022852h
580h	583h	Enclosure Management Message Format (EM_MF)—Offset 580h	0h
584h	587h	Enclosure Management LED (EM_LED)—Offset 584h	0h

18.3.1 HBA Capabilities (GHC_CAP)—Offset 0h

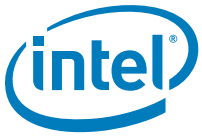
This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon PLTRST#. This register is not reset by FLR.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FF36FF07h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW/O	**Supports 64-bit Addressing (S64A):** Indicates the S-ATA controller can access 64-bit data structures. The 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry are read/write.
30	1h RW/O	**Supports Native Command Queuing Acceleration (SCQA):** Indicates the SATA controller supports Serial-ATA Native Command Queueing. The HBA will handle DMA Setup FISes in hardware, including support for auto-activiate optimization through the FIS.
29	1h RW/O	**Supports SNotification Register (SSNTF):** When set to 1, indicates that the HBA supports the PxSNTF (SNotification) register and its associated functionality. When cleared to 0., the HBA does not support the PxSNTF (SNotification) register and its associated functionality.
28	1h RW/O	**Supports Mechanical Presence Switch (SMPS):** When set to 1, the HBA supports mechanical presence switches on its ports for use in hot plug operations. When cleared to 0, this function is not supported. This value is loaded by the BIOS prior to OS initialization..
27	1h RW/O	**Supports Staggered Spin-up (SSS):** Indicates whether the S-ATA controller supports staggered spin-up on its ports, for use in balancing power spikes. This value is loaded by platform BIOS prior to OS initiallization.
26	1h RW/O	**Supports Aggressive Link Power Management (SALP):** Indicates the S-ATA controller supports auto-generating link requests to the partial or slumber states when there are no commands to process. When cleared to 0, software shall treat the PxCMD.ALPE and PxCMD.ASP bits as reserved.
25	1h RW/O	**Supports Activity LED (SAL):** Indicates the S-ATA controller supports a single output pin (SATALED#) which indicates activity.
24	1h RW/O	**Supports Command List Override (SCLO):** When set to 1, indicates that the HBA supports the PxCMD.CLO bit and it's associated function. When cleared to 0., The HBA is not capable of clearing the BSY and DRQ bits in the Status register in order to issue a software reset if these bits are still set from a previous operation.



Bit Range	Default & Access	Field Name (ID): Description
23:20	3h RW/O	**Interface Speed Support (ISS):** Indicates the maximum speed the S-ATA controller can support on its ports. These encodings match the system software programmable PxSCTL.DET.SPD field. 0000 = Reserved; 0001 = Gen 1 (1.5 Gbps); 0010 = Gen 2 (3 Gbps); 0011 = Gen 3 (6 Gbps); 0100 - 1111 = Reserved. Note: if (FFSATA0p0, FFSATA0p1, FFSATA0p2, FFSATA0p3, FFSATA0p4 and FFSATA0p5) is 1, this field is RWO defaulting to 0010 and ignores software write value of 0011. If either FFSATA0p0, FFSATA0p1, , FFSATA0p2, FFSATA0p3, FFSATA0p4 or FFSATA0p5 is 0, this field is RWO defaulting to 0011.
19	0h RO	**Supports Non-Zero DMA Offsets (SNZO):** Reserved as per AHCI 1.3
18	1h RO	**Supports AHCI mode only (SAM):** The SATA controller may optionally support AHCI access mechanism only. A value of 0 indicates that in addition to the native AHCI mechanism (via ABAR), the SATA controller implements a legacy, task-file based register interface such as SFF-8038i. A value of 1 indicates that the SATA controller does not implement a legacy, task-file based register interface.
17	1h RO	**Supports Port Multiplier (SPM):** The SATA controller may optionally support command-based switching Port Multipliers. BIOS must clear this bit if Port Multipliers are not supported.
16	0h RO	**FIS-based Switching Supported (FBSS):** Not supported.
15	1h RO	**PIO Multiple DRQ Block (PMD):** If set to 1, the HBA supports multiple DRQ block data transfers for the PIO command protocol.
14	1h RW/O	**Slumber State Capable (SSC):** The SATA controller supports the slumber state.
13	1h RW/O	**Partial State Capable (PSC):** The SATA controller supports the partial state.
12:8	1Fh RO	**Number of Command Slots (NCS):** 1Fh indicating support for 32 slots.
7	0h RO	**Command Completion Coalescing Supported (CCCS):** When set to 1, indicates that the HBA supports command completion coalescing. When command completion coalescing is supported, the HBA has implemented the CCC_CTL and the CCC_PORTS global HBA registers. When cleared to 0, indicates that the HBA does not support command completion coalescing and the CCC_CTL and CCC_PORTS global HBA registers are not implemented.
6	0h RW/O/V	**Enclosure Management Supported (EMS):** When set to 1, indicates that the HBA supports enclosure management. When enclosure management is supported, the HBA has implemented the EM_LOC and EM_CTL global HBA registers. When cleared to 0, indicates that the HBA does not support enclosure management and the EM_LOC and EM_CTL global HBA registers are not implemented.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/O	**Supports External SATA (SXS):** When set to 1, indicates that the HBA has one or more Serial ATA ports that has a signal only connector that is externally accessible. If this bit is set, software may refer to the PxCMD.ESP bit to determine whether a specific port has its signal connector externally accessible as a signal only connector (i.e. power is not part of that connector). When the bit is cleared to 0, indicates that the HBA has no Serial ATA ports that have a signal only connector externally accessible.
4:0	7h RO/V	**Number of Ports (NP):** 0's based value indicating the maximum number of ports supported. Note that the number of ports indicated in this field may be more than the number of ports indicated in the PI register. Number of ports shall be dependent on MAP.SC, fuses (FFSATA7, FFSATA8) and PCIe/SATA muxing configuration where if ANY of these parameter disable a particular port then that port is disabled and not counted. The maximum number of ports supported by SIP is 8 and the least is 0 (i.e. Function Disable). In the case of 0 port configuration, the value of NP is a don't care (while implementation has it fixed as 07h). Any combination in between is supported by SATA host controller. Indicates the number of supported ports.

18.3.2 Global HBA Control (GHC)—Offset 4h

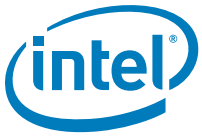
This register controls various global actions of the HBA.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 80000000h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**AHCI Enable (AE):** When set, indicates that an AHCI driver is loaded and communication to the HBA shall be via AHCI mechanisms. This can be used by an HBA that supports both legacy mechanisms (such as SFF-8038i) and AHCI to know when the HBA is running under an AHCI driver. When set, software shall only talk to the HBA using AHCI. The HBA will not have to allow command processing via both AHCI and legacy mechanisms. When cleared, software will only communicate with the HBA using legacy mechanisms. Software shall set this bit to 1 before accessing other AHCI registers. Note: The implementation of this bit is dependent upon the value of the CAP.SAM bit. If CAP.SAM is 0, then GHC.AE should be RW and shall have a reset value of 0. If CAP.SAM is 1, then AE shall be read only and shall have a reset value of 1.
30:3	0h RO	Reserved.



Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**MSI Revert to Single Message (MRSM):** When set to 1 by hardware, indicates that the HBA requested more than one MSI vector but has reverted to using the first vector only. When this bit is cleared to 0, the HBA has not reverted to single MSI mode (i.e. hardware is already in single MSI mode, software has allocated the number of messages requested, or hardware is sharing interrupt vectors if MC.MME < MC.MMC). The HBA may revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. This bit shall only be set to 1 when the following conditions hold: MC.MSIE = 1 (MSI is enabled); MC.MMC > 0 (multiple messages requested); MC.MME > 0 (more than one message allocated); MC.MME != MC.MMC (messages allocated not equal to number requested). When this bit is set to 1, single MSI mode operation is in use and software is responsible for clearing bits in the IS register to clear interrupts. This bit shall be cleared to 0 by hardware when any of the four conditions stated is false. This bit is also cleared to 0 when MC.MSIE = 1 and MC.MME = 0h. In this case, the hardware has been programmed to use single MSI mode, and is not reverting to that mode. The HBA shall always revert to single MSI mode when the number of vectors allocated by the host is leass than the number requested. Value of MRSM is a don't care when GHC.HR=1.
1	0h RW	**Interrupt Enable (IE):** This global bit enables interrupts from the HBA. When cleared (reset default), all interrupt sources from all ports are disabled. When set, interrupts are enabled.
0	0h RW/1S	**HBA Reset (HR):** When set by SW, this bit causes an internal reset of the HBA. All state machines that relate to data transfers and native command queuing will return to an idle condition, and all ports will be re-initialized via COMRESET. When the HBA has performed the reset action, it will reset this bit to 0. A software write of 0 will have no effect. For a description on which bits are reset when this bit is set, see the AHCI specification, section 10.3.3.

18.3.3 Ports Implemented (GHC_PI)—Offset Ch

This register indicates which ports are exposed to the HBA. It is loaded by platform BIOS. It indicates which ports that the device supports are available for software to use. Any available port may not be implemented. This register is not reset by FLR. There is BIOS programming requirement on the PI register. Please refer to section 7.9.13.1.1 for details.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW/O/V	**Port 7 Implemented (PI7):** If set, then port 7 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Refer to CAP.NP where port 7 is not available.
6	0h RW/O/V	**Port 6 Implemented (PI6):** If set, then port 6 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Refer to CAP.NP where port 6 is not available.
5	0h RW/O/V	**Port 5 Implemented (PI5):** If set, then port 5 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Refer to CAP.NP where port 5 is not available.
4	0h RW/O/V	**Port 4 Implemented (PI4):** If set, then port 4 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Refer to CAP.NP where port 4 is not available.
3	0h RW/O/V	**Port 3 Implemented (PI3):** If set, then port 3 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Refer to CAP.NP where port 3 is not available.
2	0h RW/O/V	**Port 2 Implemented (PI2):** If set, then port 2 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Refer to CAP.NP where port 2 is not available.
1	0h RW/O/V	**Port 1 Implemented (PI1):** If set, then port 1 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Refer to CAP.NP where port 1 is not available.
0	0h RW/O/V	**Port 0 Implemented (PI0):** If set, then port 0 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Refer to CAP.NP where port 0 is not available.

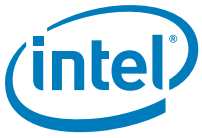
18.3.4 AHCI Version (VS)—Offset 10h

This register indicates the major and minor version of the AHCI specification. It is BCD encoded. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number. Example: Version 3.12 would be represented as 00030102h.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10300h



Bit Range	Default & Access	Field Name (ID): Description
31:16	1h RO	**Major Version Number (MJR):** Indicates the major version is 1.
15:0	300h RO	**Minor Version Number (MNR):** Indicates the minor version is 30.

18.3.5 Enclosure Management Location (EM_LOC)—Offset 1Ch

The enclosure management location register identifies the location and size of the enclosure management message buffer. This register is not implemented if enclosure management is not supported (i.e. CAP.EMS = 0).

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1600002h

Bit Range	Default & Access	Field Name (ID): Description
31:16	160h RO	**Offset (OFST):** The offset of the message buffer in Dwords from the beginning of the ABAR.
15:0	2h RO	**Buffer Size (SZ):** Specifies the size of the transmit message buffer area in Dwords. If both transmit and receive buffers are supported, then the transmit buffer begins at ABAR[EM_LOC.OFST*4] and the receive buffer directly follows it. If both transmit and receive buffers are supported, both buffers are of the size indicated in the Buffer Size field. A value of 0 is invalid. Note that SATA controller only supports transmit buffer.

18.3.6 Enclosure Management Control (EM_CTL)—Offset 20h

This register is used to control and obtain status for the enclosure management interface. The register incluldes information on the attributes of the implementation, enclosure management messages supported, the status of the interface, whether any messages are pending, and is used to initiate sending messages. This register is not implemented if enclosure management is not supported (i.e. CAP.EMS = 0).

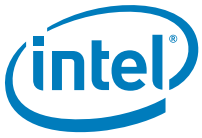
Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 7010000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RO	**Port Multiplier Support (ATTR_PM):** The HBA does not support enclosure management messages for devices attached via a Port Multiplier. Software should use the Serial ATA enclosure management bridge that is built into many Port Multipliers for enclosure services with these devices. For more information on Serial ATA enclosure management bridges, refer to the Serial ATA II: Extensions to Serial ATA 1.0a revision 1.2 specification.
26	1h RW/O	**Activity LED Hardware Driven (ATTR_ALHD):** If set to 1, the HBA drives the activity LED for the LED message type in hardware and does not utilize software settings for this LED. The HBA does not begin transmitting the hardware based activity signal until after software has written CTL.TM=1 after a reset condition.
25	1h RO	**Transmit Only (ATTR_XMT):** If set to 1, the HBA only supports transmitting messages and does not support receiving messages. If cleared to 0, the HBA supports transmitting and receiving messages.
24	1h RO	**Single Message Buffer (ATTR_SMB):** If set to 1, the HBA has one message buffer that is shared for messages to transmit and messages received. In this case, unsolicited receive messages are not supported and it is software's responsibility to manage access to this buffer. If cleared to 0, there are separate receive and transmit buffers such that unsolicited messages could be supported.
23:20	0h RO	Reserved.
19	0h RO	**SGPIO Enclosure Management Messages (SUPP_SGPIO):** If set to 1, the HBA supports the SGPIO register interface message type.
18	0h RO	**SES-2 Enclosure Management Messages (SUPP_SES2):** If set to 1, the HBA supports the SES-2 message type.
17	0h RO	**SAF-TE Enclosure Management Messages (SUPP_SAFTE):** If set to 1, the HBA supports the SAF-TE message type.
16	1h RO	**LED Message Types (SUPP_LED):** If set to 1, the HBA supports the LED message type defined in LED Message Type.
15:10	0h RO	Reserved.
9	0h RW/1S	**Reset (RST):** When set to 1 by software, the HBA shall reset all enclosure management message logic and take all appropriate reset actions to ensure messages can be transmitted/received after the reset. After the HBA completes the reset operation, the HBA shall set the value to 0. A write of 0 by software to this field shall have no effect.



Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1S	**Transmit Message (CTL_TM):** When set to 1 by software, the HBA shall transmit the message contained in the message buffer. When the message is completely sent, the HBA shall clear this bit to 0. A write of 0 to this bit by software shall have no effect. Software shall not change the contents of the message buffer while CTL.TM is set to 1.
7:1	0h RO	Reserved.
0	0h RO	**Message Received (STS_MR):** Message received is not supported.

18.3.7 HBA Capabilities Extended (GHC_CAP2)—Offset 24h

This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon PLTRST#. This register is not reset by FLR.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3Ch

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	1h RW/O	**DEVSLP Entrance from Slumber Only (DESO):** This field specifies that the HBA shall only assert DEVSLP if the interface is in Slumber. When this bit is set to 1, the HBA shall ignore software directed entrance to DEVSLP via PxCMD.ICC unless PxSSTS.IPM = 6h. When this bit is cleared to 0, the HBA may enter DEVSLP from any link state (active, Partial, or Slumber). BIOS is required to program this field to 1.
4	1h RW/O/V	**Supports Aggressive DEVSLP Management (SADM):** When set to 1, the HBA supports hardware assertion of the DEVSLP signal after the idle timeout expires. When cleared to 0, this function is not supported and software shall treat the PxDEVSLP.ADSE field as reserved. Note: If PHY IO PM Disable Fuse is 1, this register will read 0. Else this register will read 1 with RWO attribute.
3	1h RW/O/V	**Supports DEVSLP (SDS):** When set to 1, the HBA supports the DEVSLP feature. When cleared to 0, DEVSLP is not supported. Note: If PHY IO PM Disable Fuse is 1, this register will read 0. Else this register will read 1 with RWO attribute.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/O/V	**Automatic Partial to Slumber Transitions (APST):** When set to 1, the HBA supports Automatic Partial to Slumber Transitions. When cleared to 0, Automatic Partial to Slumber Transition is not supported. Note: If SATA PHY PM Disable Fuse is 1, this register will read only 0. Else this register will read 1 with RWO attribute.
1	0h RO	Reserved.
0	0h RO	**BIOS/OS Handoff (BOH):** Not supported.

18.3.8 Vendor Specific (VSP)—Offset A0h

Vendor Specific

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 48h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6	1h RO	**Software Feature Mask Supported (SFMS):** Set to 1 if the platform is enabled for premium storage features mask (SFM) as described in VS MMIO space at offset ABAR[RPID.(OFST*4)+4].
5	0h RO/V	**Premium Features Supported (PFS):** Set to 1 if the platform is enabled for premium storage features (PFB) as described in VS MMIO space at offset ABAR[RPID.OFST*4]. Set to 0 if the platform is not enabled for premium storage features.
4	0h RO/V	**Platform Type (PT):** Set to 1 if mobile platform. Clear (0) if desktop.
3	1h RO	**Supports RAID Platform ID Reporting (SRPIR):** If set to 1, then indicates that the RAID Platform ID is reported via ABAR + C0h. Set to 0 if this ID is not reported via MMIO space.
2:0	0h RO	Reserved.

18.3.9 Vendor-Specific Capabilities Register (VS_CAP)—Offset A4h

Vendor-Specific Capabilities Register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1002DEh

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:16	10h RW/O	**NVM Remapped Register Offset (NRMO):** Specifies the offset (in 128B unit) within ABAR as to where the PCIe NAND memory BAR register space is remapped. For example, NRMO=1 means ABAR + 128B. This allows the remapped offset to shift between ABAR + 0B, and ABAR + 512KK - 128B, with 128B step. The remapped offset into the AHCI memory space must not overlap with the memory space used for SATA. The remapped offset into the AHCI memory space and the remapped size must not exceed the allocated AHCI memory space of the integrated AHCI controller. Only valid when NRMBE = 1. The reset default of this field is 10h, this places the start of the PCIe NAND memory BAR register space at ABAR + 2K. This field is not reset by FLR.
15:13	0h RO	Reserved.
12:1	16Fh RW/O	**Memory Space Limit. (MSL):** This field specifies the size (in 128B unit) of the remapped memory space for the PCIe NAND device. It is a 0-based field. For example, MSL=1 means 256B. This allows the remapped size to shift between 128B and 512K in steps of 128B. Memory BAR offset from 0 to MSL of the PCIe NAND device are remapped under the integrated AHCI controller memory space. The remapped offset into the AHCI memory space and the value programmed in this field must not exceed the allocated AHCI memory space of the integrated AHCI controller. Only valid when NRMBE = 1. The reset default of this field is 16Fh, which specifies the size of the remapped memory space as 34k. This field is not reset by FLR.
0	0h RW/O	**PCIe NAND Memory BAR Remapped Enable (NRMBE):** Set to 1 if a PCIe NAND device is present and remapping of its memory BAR register space is enabled. Cleared to 0 if there is no PCIe NAND device present or the remapping of its memory BAR register space is disabled. This bit is not reset by FLR.

18.3.10 Remapping Under NVMe (RUN)—Offset A8h

Remapping Under NVMe

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW/O	**Remapping Under NVMe Enable (RUNE):** When set to 1, AHCI Host Controller become a Remapped Device under the NVMe Host Controller hence the Bus Device Function of AHCI Host Controller is hidden from the OS. When this bit is 0, AHCI Host Controller is not remapped under NVMe Host Controller
15:8	0h RO	Reserved.
7:0	0h RW/O	**NVMe Device Function (NVMEDF):** Device and function number of NVMe Host Controller that AHCI Host Controller is remapped to. Bit 7:3 is the device number, bit 2:0 is the function number

18.3.11 RAID Platform ID (RPID)—Offset C0h

This register is used by the Intel Matrix Storage Manager OROM to match the features supported by the OROM with the platform on which the OROM is executing. This prevents the use of an OROM designed for newer chipsets from being use on older chipsets as this could reduce up-sell potential.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

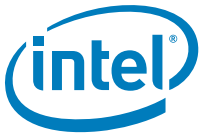
Default: 311C02h

Bit Range	Default & Access	Field Name (ID): Description
31:16	31h RO	**Offset (OFST):** The offset of the Premium Feature Block (PFB) in DWords from the beginning of the ABAR. SFM follows directly after PFB.
15:0	1C02h RO/V	**RAID Platform ID (RPID):** Specifies the DID value that has been assigned to the platform. This is the same DID that is reported by the SATA controller when SATAGC.AIE is set to 1 except that the DID is always reported through this register, regardless if the programming of SATAGC.AIE.

18.3.12 Premium Feature Block (PFB)—Offset C4h

Note: Bits 4-0 are not bit-mapped to individual fuses and/or soft SKU settings; rather a single fuse FFSATA5& FFSATA 3 /soft sku is used to indicate support for all of these features (refer to VSP.PFS). These registers indicate to the Intel Rapid Storage Technology AHCI driver that those premium RAID features that can be supported on the platform.

Access Method



Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	Reserved.
4	0h RO/V	**Reserved (RSVD_1):** Read value is the same as VSP.PFS.
3	0h RO/V	**Reserved (RSVD_2):** Read value is the same as VSP.PFS.
2	0h RO/V	**Reserved (RSVD_3):** Read value is the same as VSP.PFS.
1	0h RO/V	**Supports Email Alert (SEA):** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.
0	0h RO/V	**Supports OEM IOCTL (SOI):** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.

18.3.13 SW Feature Mask (SFM)—Offset C8h

The following will be programmed by the BIOS when VS_CAP.SFMS == 1. The feature mask is used by SW to determine which non-premium features shall be supported by SW. These register bits are not reset by FLR since they are programmed by BIOS.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 3Fh

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	Reserved.
11:10	0h RW/O	**OROM UI Normal Delay. (OROM_UI_Normal_Delay):** Values of these bits specify the delay of the OROM UI Splash Screen in a normal status. 00 = 2 secs (default and previous value); 01 = 4 secs; 10 = 6 secs; 11 = 8 secs. If bit 5 == 0, then these values are disregarded.
9	0h RW/O	**Smart Response Technology. (Smart_Response_Technology):** If set to '1', then Smart Response Technology is enabled. If cleared to '0', the feature is disabled.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/O	**RRT Only on ESATA (IRRT_Only_on_ESATA):** If set to 1, then only RRT volumes can span internal and external SATA ports (e.g. eSATA). If cleared to 0, then any RAID volume can span internal and external SATA ports (e.g. eSATA).
7	0h RW/O	**LED Locate (LED_Locate):** If set to 1, then LED/SGPIO hardware is attached and the ping to locate feature is enabled in the OS.
6	0h RW/O	**HDDUNLOCK (HDDUNLOCK):** If set to 1, then HDD password unlock is enabled in the OS.
5	1h RW/O	**OROM UI and BANNER (OROM_UI_and_BANNER):** If set to 1, then the OROM UI is displayed. When cleared to 0, the OROM UI and BANNER are not displayed if all disks and volumes have a normal status.
4	1h RW/O	**RRT (IRRT):** If set to 1, then Rapid Recovery Technology is enabled.
3	1h RW/O	**R5 (R5):** If set to 1, then RAID5 is enabled.
2	1h RW/O	**R10 (R10):** If set to 1, then RAID10 is enabled.
1	1h RW/O	**R1 (R1):** If set to 1, then RAID1 is enabled.
0	1h RW/O	**R0 (R0):** If set to 1, then RAID0 is enabled.

18.3.14 Port [0-7] Command List Base Address (PxCLB0)—Offset 100h

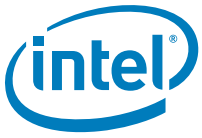
Port [0-7] Command List Base Address

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RW	**Command List Base Address (CLB):** Indicates the 32-bit base for the command list for this port. This base is used when fetching commands to execute. This address must be 1K aligned as indicated by bits 31:10 being read/write. Note that these bits are not reset on a HBA reset.
9:0	0h RO	Reserved.



18.3.15 Port [0-7] Command List Base Address Upper 32-bits (PxCLBU0)—Offset 104h

Port [0-7] Command List Base Address Upper 32-bits

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Command List Base Address Upper (CLBU):** Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute. Note that these bits are not reset on a HBA reset.

18.3.16 Port [0-7] FIS Base Address (PxFB0)—Offset 108h

Port [0-7] FIS Base Address

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**FIS Base Address (FB):** Indicates the 32-bit base for received FISes. This address must be 256-byte aligned as indicated by bits 31:08 being read/write. When FIS-based switching is in use, this structure is 4KB in length and the address shall be 4KB aligned. Note that these bits are not reset on a HBA reset.
7:0	0h RO	Reserved.

18.3.17 Port [0-7] FIS Base Address Upper 32-bits (PxFBU0)—Offset 10Ch

Port [0-7] FIS Base Address Upper 32-bits

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**FIS Base Address Upper (FBU):** Indicates the upper 32-bits for the received FIS base for this port. Note that these bits are not reset on a HBA reset.

18.3.18 Port [0-7] Interrupt Status (PxIS0)—Offset 110h

Port [0-7] Interrupt Status

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Cold Presence Detect Status (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW/1C/V	**Task File Error Status (TFES):** This bit is set whenever the status register is updated by the device and the error bit (bit 0 of the Status field in the received FIS) is set.
29	0h RW/1C/V	**Host Bus Fatal Error Status (HBFS):** Indicates that the HBA encountered a host bus error that it cannot recover from, such as a bad software pointer. In PCI, such an indication would be a target or master abort.
28	0h RW/1C/V	**Host Bus Data Error Status (HBDS):** Indicates that the HBA encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
27	0h RW/1C/V	**Interface Fatal Error Status (IFS):** Indicates that the HBA encountered an error on the SATA interface which caused the transfer to stop.
26	0h RW/1C/V	**Interface Non-fatal Error Status (INFS):** Indicates that the HBA encountered an error on the SATA interface but was able to continue operation.
25	0h RO	Reserved.
24	0h RW/1C/V	**Overflow Status (OFS):** Indicates that the HBA received more bytes from a device than was specified in the PRD table for the command.
23	0h RW/1C/V	**Incorrect Port Multiplier Status (IPMS):** Indicates that the HBA received a FIS from a device whose port multiplier field did not match what was expected. The IPMS bit may be set during emuneration process. It is recommended that IPMS only be used after enumeration is complete on the Port Multiplier.

Bit Range	Default & Access	Field Name (ID): Description
22	0h RO/V	**PhyRdy Change Status (PRCS):** When set to one indicates the internal PhyRdy signal changed state. This bit reflects the state of PxSERR.DIAG.N. This bit is RO and is only cleared when PxSERR.DIAG.N is cleared.
21:8	0h RO	Reserved.
7	0h RW/1C/V	**Device Mechanical Presence Status (DMPS):** When set, indicates that a platform mechanical presence switch has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid in systems that support mechanical presence switch (CAP.SMPS and PxCMD.MPSP are set).
6	0h RO/V	**Port Connect Change Status (PCS):** • 1: Change in Current Connect Status. • 0: No change in Current Connect Status. This bit reflects the state of PxSERR.DIAG.X. This bit is only cleared when PxSERR.DIAG.X is cleared.
5	0h RW/1C/V	**Descriptor Processed (DPS):** A PRD with the I. bit set has transferred all of its data.
4	0h RO/V	**Unknown FIS Interrupt (UFS):** When set to 1 indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by software clearing the PxSERR.DIAG.F bit to 0. Note that this bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when the FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to 1 or the two bits may become out of sync.
3	0h RW/1C/V	**Set Device Bits Interrupt (SDBS):** A Set Device Bits FIS has been received with the I. bit set and has been copied into system memory.
2	0h RW/1C/V	**DMA Setup FIS Interrupt (DSS):** A DMA Setup FIS has been received with the I. bit set and has been copied into system memory.
1	0h RW/1C/V	**PIO Setup FIS Interrupt (PSS):** A PIO Setup FIS has been received with the I. bit set, it has been copied into system memory, and the data related to that FIS has been transferred. This bit shall be set even if the data transfer resulted in an error.
0	0h RW/1C/V	**Device to Host Register FIS Interrupt (DHRS):** A D2H register FIS has been received with the I. bit set, and has been copied into system memory.

18.3.19 Port [0-7] Interrupt Enable (PxIE0)—Offset 114h

Port [0-7] Interrupt Enable

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Cold Presence Detect Enable (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW	**Task File Error Enable (TFEE):** When set, GHC.IE is set, and P0S.TFES is set, the HBA shall generate an interrupt.
29	0h RW	**Host Bus Fatal Error Enable (HBFE):** When set, GHC.IE is set, and P0IS.HBFS is set, the HBA shall generate an interrupt.
28	0h RW	**Host Bus Data Error Enable (HBDE):** when set, GHC.IE is set, and P0IS.HBDS is set, the HBA shall generate an interrupt.
27	0h RW	**Interface Fatal Error Enable (IFE):** When set, GHC.IE is set, and P0IS.IFS is set, the HBA shall generate an interrupt.
26	0h RW	**Interface Non-fatal Error Enable (INFE):** When set, GHC.IE is set, and P0IS.INFS is set, the HBA shall generate an interrupt.
25	0h RO	Reserved.
24	0h RW	**Overflow Enable (OFE):** When set, and GHC.IE and P0IS.OFS are set, the HBA shall generate an interrupt.
23	0h RW	**Incorrect Port Multiplier Enable (IPME):** When set, and GHC.IE and P0IS.IPMS are set, the HBA shall generate an interrupt. BIOS is required to program this field to '0'. The same applies to AHCI driver.
22	0h RW	**PhyRdy Change Interrupt Enable (PRCE):** When set, and GHC.IE is set, and PxIS.PRCS is set, the HBA shall generate an interrupt.
21:8	0h RO	Reserved.
7	0h RW	**Device Mechanical Enable (DMPE):** When set, and P0IS.DMPS is set, the HBA shall generate an interrupt.
6	0h RW/V	**Port Change Interrupt Enable (PCE):** When set, GHC.IE is set, and P0IS.PCS is set, the HBA shall generate an interrupt.
5	0h RW	**Descriptor Processed Interrupt Enable (DPE):** When set, GHC.IE is set, and P0IS.DPS is set, the HBA shall generate an interrupt.
4	0h RW	**Unknown FIS Interrupt Enable (UFE):** When set, GHC.IE is set, and PxIS.UFS is set to 1, the HBA shall generate an interrupt.
3	0h RW	**Set Device Bits FIS Interrupt Enable (SDBE):** When set, GHC.IE is set, and P0IS.SDBS is set, the HBA shall generate an interrupt.
2	0h RW	**DMA Setup FIS Interrupt Enable (DSE):** When set, GHC.IE is set, and P0IS.DSS is set, the HBA shall generate an interrupt.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**PIO Setup FIS Interrupt Enable (PSE):** When set, GHC.IE is set, and P0IS.PSS is set, the HBA shall generate an interrupt.
0	0h RW	**Device to Host Register FIS Interrupt Enable (DHRE):** When set, GHC.IE is set, and P0IS.DHRS is set, the HBA shall generate an interrupt.

18.3.20 Port [0-7] Command (PxCMD0)—Offset 118h

Port [0-7] Command

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Interface Communication Control (ICC):** This is a four-bit field which can be used to control reset and power states of the interface. If the Link layer is currently in the L_IDLE state, writes to this field shall cause the HBA to initiate a transition to the interface power management state requested. If the Link layer is not currently in the L_IDLE state, writes to this field shall have no effect.
27	0h RW	**Aggressive Slumber Partial (ASP):** When set to 1, and the ALPE bit is set, the HBA shall aggressively enter the Slumber state when it clears a bit in the PxCI or PxSACT register and the register values are then PxCI = 0h and PxSACT = 0h. When cleared, and the ALPE bit is set, the HBA will aggressively enter the Partial state when it clears a bit in the PxCI or PxSACT register and the register values are then PxCI = 0h and PxSACT = 0h. If CAP.SALP is cleared to 0., software shall treat this bit as reserved.
26	0h RW	**Aggressive Link Power Management Enable (ALPE):** When set, the HBA will aggressively enter a lower link power state (Partial or Slumber) based upon the setting of the ASP bit. Software shall only set this bit to 1 if CAP.SALP is set to 1. If CAP.SALP is cleared to 0, software shall treat this bit as reserved. BIOS is recommended to program this field to 1.
25	0h RW	**Drive LED on ATAPI Enable (DLAE):** When set, the HBA will drive the LED pin active for commands regardless of the state of PxCMD.ATAPI. When cleared, the HBA will only drive the LED pin active for commands if PxCMD.ATAPI is set to 0.. This bit is set by software
24	0h RW	**Device is ATAPI (ATAPI):** When set, the connected device is an ATAPI device. This bit is used by the HBA to control whether or not to generate the desktop LED when commands are active.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**Automatic Partial to Slumber Transitions Enabled (APSTE):** When set to 1., the HBA may perform Automatic Partial to Slumber Transitions. When cleared to 0. the port shall not perform Automatic Partial to Slumber Transitions. Software shall only set this bit to 1. if CAP2.APST is set to 1.; if CAP2.APST is cleared to 0. software shall treat this bit as reserved.
22	0h RO	**FIS-based Switching Capable Port (FBSCP):** The SATA controller does not support FIS-Based Switching.
21	0h RW/O	**External SATA Port (ESP):** When set to 1, indicates that this port is routed externally and will be used with an external SATA device. When set to 1, CAP.SXS must also be set to 1. When cleared (0), indicates that this port is not routed externally and supports internal SATA devices only. If ESP is set to '1', then the port may experience hot plug events.
20	0h RO	**Cold Presence Detection (CPD):** The SATA controller does not support cold presence detect.
19	0h RW/O	**Mechanical Presence Switch Attached to Port (MPSP):** If set to 1, the platform supports a mechanical presence switch attached to this port. If cleared to 0, the platform does not support a mechanical presence switch attached to this port.
18	0h RW/O	**Hot Plug Capable Port (HPCP):** This indicates whether the this port is connected to a device which can be hot plugged. SATA by definition is hot-pluggable, but not all platforms are constructed to allow the device to be removed (it may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as eject device to the end-user.
17	0h RW/V	**Port Multiplier Attached (PMA):** When set, a Port Multiplier is attached to the HBA for this port. When cleared, a Port Multiplier is not attached to the HBA for this port. This bit is a read only 0. when CAP.PMS = 0., and read/write when CAP.PMS = 1.. Note that this bit is set by software; hardware does not auto-detect that a Port Multiplier is attached.
16	0h RO	Reserved.
15	0h RO/V	**Command List Running (CR):** When this bit is set it indicates that the command list DMA engine for the port is running.
14	0h RO/V	**FIS Receive Running (FR):** When this bit is set it indicates that the FIS Receive DMA engine for the port is running. Note to software: When FR bit stays set, please read the PxIS.PCS and PxSERR.DET.X to service the PCS interrupt accordingly if any
13	0h RO/V	**Mechanical Presence Switch State (MPSS):** The MPSS bit reports the state of a mechanical presence switch attached to this port. If CAP.SMPS is set to 1 and the mechanical presence switch is closed then this bit is cleared to 0. If CAP.SMPS is set to 1 and the mechanical presence switch is open then this bit is set to 1. If CAP.SMPS is set to 0 then this bit is cleared to 0. Software should only use this bit if both CAP.SMPS and PxCMD.MPSP are set to 1.

Bit Range	Default & Access	Field Name (ID): Description
12:8	0h RO/V	**Current Command Slot (CCS):** Indicates the current command slot the HBA is processing. This field is valid when the PxCMD.ST bit is set, and is constantly updated by the HBA. This field can be updated as soon as the HBA recognizes an active command slot, or at some point soon after when it begins processing the command. When PxCMD.ST transitions from a 1 to a 0, the HBA will reset this field to 0. After PxCMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is PxCMD.CCS + 1. For example, after the HBA has issued its first command, if PxCMD.CCS = 0h and PxCI is set to 3h, the next command that will be issued is from command slot 1.
7:5	0h RO	Reserved.
4	0h RW	**FIS Receive Enable (FRE):** When set, the HBA may post received FISes into the FIS receive area pointed to by PxFB and PxFBU. When cleared, received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence.
3	0h RW/1S	**Command List Override (CLO):** Setting this bit to 1 causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to 0 when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to 0. A write to this register with a value of 0 shall have no effect.
2	1h RO	**Power On Device (POD):** The SATA controller does not support cold presence detect.
1	0h RW/V	**Spin-Up Device (SUD):** This bit is read/write for HBAs that support staggered spin-up via CAP.SSS. This bit is read only 1. for HBAs that do not support staggered spin-up. On an edge detect from 0. to 1, the HBA shall start a COMRESET initializatoin sequence to the device. Clearing this bit causes no action on the interface. Clearing this bit to0 does not cause any OOB signal to be sent on the interface. When this bit is cleared to 0. and PxSCTL.DET = 0h, the HBA will enter listen mode.
0	0h RW	**Start (ST):** When set, the HBA may process the command list. When cleared, the HBA may not process the command list. Whenever this bit is changed from a 0 to a 1, the HBA starts processing the command list at entry 0. Whenever this bit is changed from a 1 ot a 0, the PxCI and PxSACT register is cleared by the HBA upon the HBA putting the controller into an idle state. PxTFD shall be updated also.

18.3.21 Port [0-7] Task File Data (PxTFD0)—Offset 120h

Port [0-7] Task File Data

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 7Fh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	0h RO/V	**Error (ERR):** Contains the latest copy of the task file error register.
7	0h RO/V	**Status Busy (STS_BSY):** Status - Indicates the interface is busy.
6:4	7h RO/V	**Status Rsvd0 (STS_RSVD0):** Status - Not Applicable.
3	1h RO/V	**Status Drq (STS_DRQ):** Status - Indicates a data transfer is requested.
2:1	3h RO/V	**Status Rsvd1 (STS_RSVD1):** Status - Not Applicable.
0	1h RO/V	**Status Err (STS_ERR):** Status - Indicates an error during the transfer.

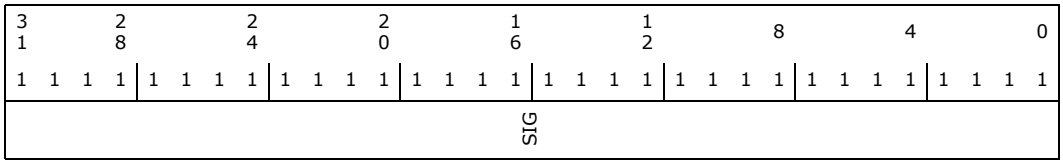
18.3.22 Port [0-7] Signature (PxSIG0)—Offset 124h

Port [0-7] Signature

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RO/V	**Signature (SIG):** Contains the signature received from a device on the first D2H Register FIS.

18.3.23 Port [0-7] Serial ATA Status (PxSSTS0)—Offset 128h

Port [0-7] Serial ATA Status

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:8	0h RO/V	**Interface Power Management (IPM):** Indicates the current interface state
7:4	0h RO/V	**Current Interface Speed (SPD):** Indicates the negotiated interface communication speed.
3:0	0h RO/V	**Device Detection (DET):** Indicates the interface device detection and Phy state.

18.3.24 Port [0-7] Serial ATA Control (PxSCTL0)—Offset 12Ch

Port [0-7] Serial ATA Control

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:16	0h RW	**Port Multiplier Port (PMP):** This field is not used by AHCI.
15:12	0h RW	**Select Power Management (SPM):** This field is not used by AHCI.
11:8	0h RW	**Interface Power Management Transitions Allowed (IPM):** Indicates which power states the HBA is allowed to transition to. If an interface power management state is not allowed via this register field, the HBA will not initiate that state and the HBA will PMNAKP any request from the device to enter that state.
7:4	0h RW	**Speed Allowed (SPD):** Indicates the highest allowable speed of the interface.
3:0	0h RW	**Device Detection Initialization (DET):** Controls the HBA.s device detection and interface initialization.

18.3.25 Port [0-7] Serial ATA Error (PxSERR0)—Offset 130h

Port [0-7] Serial ATA Error

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/1C/V	**Diagnostics (DIAG):** Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes.
15:0	0h RW/1C/V	**Error (ERR):** The ERR field contains error information for use by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer.

18.3.26 Port [0-7] Serial ATA Active (PxSACT0)—Offset 134h

Port [0-7] Serial ATA Active

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/1S/V	**Device Status (DS):** System software sets this bit for native command queuing commands prior to setting the PxCI.CI bit in the same command slot entry. This field is cleared via the Set Device Bits FIS.

18.3.27 Port [0-7] Commands Issued (PxCI0)—Offset 138h

Port [0-7] Commands Issued

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/1S/V	**Commands Issued (CI):** This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, ERR, and DRQ bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to 1 by software when PxCMD.ST is set to 1.

18.3.28 Port [0-7] SNotification (PxSNTF0)—Offset 13Ch

Port [0-7] SNotification

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW/1C/V	**PM Notify (PMN):** This field indicates whether a particular device with the corresponding PM Port number issued a Set Device Bits FIS to the host with the Notification bit set. PM Port 0h sets bit 0. PM Port Fh sets bit 15. Individual bits are cleared by software writing 1's to the corresponding bit positions. Note that, while this field is reset to default on a HBA Reset, it is not reset by COMRESET or SRST

18.3.29 Port [0-7] Device Sleep (PxDEVSLP0)—Offset 144h

Port [0-7] Device Sleep

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1E022852h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28:25	Fh RW/V	**DITO Multiplier (DM):** 0's based value that specifies the DITO multiplier that the HBA applies to the specified DITO value, effectively extending the range of DITO from 1ms to 16368ms. A value of 0h indicates a multiplier of 1. A maximum multiplier of 16 may be applied. The HBA computes the total idle timeout as a product of DM and DITO (i.e. DITO actual = DITO * DM).
24:15	4h RW/V	**DEVSLP Idle Timeout (DITO):** This field specifies the amount of the time (in approximate 1ms granularity) that the HBA shall wait before driving the DEVSLP signal.Hardware reloads its port specific DEVSLP timer with this value each time the port transitions out of DEVSLP state. For example: from DEVSLP to active or PxDEVSLP.ADSE transitions from 0 to a 1. If CAP2.SDS or CAP2.SADM or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0 and PxDEVSLP.ADSE is cleared to 0.
14:10	Ah RW/V	**DEVSLP Minimum Assertion Time (MDAT):** This field specifies the minimum amount of time (in 1ms granularity) that the HBA must assert the DEVSLP signal before it may be de-asserted. The nominal value is 10ms and the minimum is 1ms depending on device identification information. If CAP2.SDS is cleared to 0 or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0, PxDEVSLP.ADSE is cleared to 0, and prior to setting PxCMD.ICC to 8h.
9:2	14h RW/V	**DEVSLP Exit Timeout (DETO):** This field specifies the maximum duration (in approximate 1ms granularity) from DEVSLP de-assertion until the device is ready to accept OOB. The nominal value is 20ms while the max value is 255ms depending on device identification information. If CAP2.SDS is cleared to 0 or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0, PxDEVSLP.ADSE is cleared to 0, and prior to setting PxCMD.ICC to 8h.
1	1h RW/O	**DEVSLP Present (DSP):** If set to '1', the platform supports DEVSLP on this port. If cleared to '0', the platform does not support DEVSLP on this port. This bit may only be set to '1' if CAP2.SDS is set to '1'.DSP is mutually exclusive with the PxCMD.HPCP bit and PxCMD.ESP bit. Note that these bits are not reset on a HBA reset.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/V	**Aggressive DEVSLP Enable (ADSE):** This bit is read/write for HBAs that support aggressive DEVSLP management (CAP2. SADM = 1). When this bit is set to 1, the HBA shall assert the DEVSLP signal after the port has been idle (PxCI = 0h and PxSACT = 0h) for the amount of time specified by the PxDEVSLP.DITO register and the interface is in Slumber (PxSSTS.IPM = 6h). When this bit is cleared to 0, the HBA does not enter DEVSLP unless software directed via PxCMD.ICC. This bit shall only be set to 1 if PxDEVSLP.DSP is set to 1. If this bit is set to 1 and software clears the bit to 0, then the HBA shall de-assert the DEVSLP signal if asserted. Note that these bits are not reset on a HBA reset. BIOS is recommended to program this field to 1 if the platform support the DEVSLP feature. If CAP2.SDS is cleared to 0 or CAP2.SADM is cleared to 0, or if PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved.

18.3.30 Port [0-7] Command List Base Address (PxCLB1)—Offset 180h

Port [0-7] Command List Base Address

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RW	**Command List Base Address (CLB):** Indicates the 32-bit base for the command list for this port. This base is used when fetching commands to execute. This address must be 1K aligned as indicated by bits 31:10 being read/write. Note that these bits are not reset on a HBA reset.
9:0	0h RO	Reserved.

18.3.31 Port [0-7] Command List Base Address Upper 32-bits (PxCLBU1)—Offset 184h

Port [0-7] Command List Base Address Upper 32-bits

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Command List Base Address Upper (CLBU):** Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute. Note that these bits are not reset on a HBA reset.

18.3.32 Port [0-7] FIS Base Address (PxFB1)—Offset 188h

Port [0-7] FIS Base Address

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**FIS Base Address (FB):** Indicates the 32-bit base for received FISes. This address must be 256-byte aligned as indicated by bits 31:08 being read/write. When FIS-based switching is in use, this structure is 4KB in length and the address shall be 4KB aligned. Note that these bits are not reset on a HBA reset.
7:0	0h RO	Reserved.

18.3.33 Port [0-7] FIS Base Address Upper 32-bits (PxFBU1)—Offset 18Ch

Port [0-7] FIS Base Address Upper 32-bits

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**FIS Base Address Upper (FBU):** Indicates the upper 32-bits for the received FIS base for this port. Note that these bits are not reset on a HBA reset.

18.3.34 Port [0-7] Interrupt Status (PxIS1)—Offset 190h

Port [0-7] Interrupt Status

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Cold Presence Detect Status (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW/1C/V	**Task File Error Status (TFES):** This bit is set whenever the status register is updated by the device and the error bit (bit 0 of the Status field in the received FIS) is set.
29	0h RW/1C/V	**Host Bus Fatal Error Status (HBFS):** Indicates that the HBA encountered a host bus error that it cannot recover from, such as a bad software pointer. In PCI, such an indication would be a target or master abort.
28	0h RW/1C/V	**Host Bus Data Error Status (HBDS):** Indicates that the HBA encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
27	0h RW/1C/V	**Interface Fatal Error Status (IFS):** Indicates that the HBA encountered an error on the SATA interface which caused the transfer to stop.
26	0h RW/1C/V	**Interface Non-fatal Error Status (INFS):** Indicates that the HBA encountered an error on the SATA interface but was able to continue operation.
25	0h RO	Reserved.
24	0h RW/1C/V	**Overflow Status (OFS):** Indicates that the HBA received more bytes from a device than was specified in the PRD table for the command.
23	0h RW/1C/V	**Incorrect Port Multiplier Status (IPMS):** Indicates that the HBA received a FIS from a device whose port multiplier field did not match what was expected. The IPMS bit may be set during emuneration process. It is recommended that IPMS only be used after enumeration is complete on the Port Multiplier.
22	0h RO/V	**PhyRdy Change Status (PRCS):** When set to one indicates the internal PhyRdy signal changed state. This bit reflects the state of PxSERR.DIAG.N. This bit is RO and is only cleared when PxSERR.DIAG.N is cleared.
21:8	0h RO	Reserved.
7	0h RW/1C/V	**Device Mechanical Presence Status (DMPS):** When set, indicates that a platform mechanical presence switch has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid in systems that support mechanical presence switch (CAP.SMPS and PxCMD.MPSP are set).

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO/V	**Port Connect Change Status (PCS):** • 1: Change in Current Connect Status. • 0: No change in Current Connect Status. This bit reflects the state of PxSERR.DIAG.X. This bit is only cleared when PxSERR.DIAG.X is cleared.
5	0h RW/1C/V	**Descriptor Processed (DPS):** A PRD with the I. bit set has transferred all of its data.
4	0h RO/V	**Unknown FIS Interrupt (UFS):** When set to 1 indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by software clearing the PxSERR.DIAG.F bit to 0. Note that this bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when the FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to 1 or the two bits may become out of sync.
3	0h RW/1C/V	**Set Device Bits Interrupt (SDBS):** A Set Device Bits FIS has been received with the I. bit set and has been copied into system memory.
2	0h RW/1C/V	**DMA Setup FIS Interrupt (DSS):** A DMA Setup FIS has been received with the I. bit set and has been copied into system memory.
1	0h RW/1C/V	**PIO Setup FIS Interrupt (PSS):** A PIO Setup FIS has been received with the I. bit set, it has been copied into system memory, and the data related to that FIS has been transferred. This bit shall be set even if the data transfer resulted in an error.
0	0h RW/1C/V	**Device to Host Register FIS Interrupt (DHRS):** A D2H register FIS has been received with the I. bit set, and has been copied into system memory.

18.3.35 Port [0-7] Interrupt Enable (PxIE1)—Offset 194h

Port [0-7] Interrupt Enable

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Cold Presence Detect Enable (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW	**Task File Error Enable (TFEE):** When set, GHC.IE is set, and P0S.TFES is set, the HBA shall generate an interrupt.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RW	**Host Bus Fatal Error Enable (HBFE):** When set, GHC.IE is set, and P0IS.HBFS is set, the HBA shall generate an interrupt.
28	0h RW	**Host Bus Data Error Enable (HBDE):** when set, GHC.IE is set, and P0IS.HBDS is set, the HBA shall generate an interrupt.
27	0h RW	**Interface Fatal Error Enable (IFE):** When set, GHC.IE is set, and P0IS.IFS is set, the HBA shall generate an interrupt.
26	0h RW	**Interface Non-fatal Error Enable (INFE):** When set, GHC.IE is set, and P0IS.INFS is set, the HBA shall generate an interrupt.
25	0h RO	Reserved.
24	0h RW	**Overflow Enable (OFE):** When set, and GHC.IE and P0IS.OFS are set, the HBA shall generate an interrupt.
23	0h RW	**Incorrect Port Multiplier Enable (IPME):** When set, and GHC.IE and P0IS.IPMS are set, the HBA shall generate an interrupt. BIOS is required to program this field to '0'. The same applies to AHCI driver.
22	0h RW	**PhyRdy Change Interrupt Enable (PRCE):** When set, and GHC.IE is set, and PxIS.PRCS is set, the HBA shall generate an interrupt.
21:8	0h RO	Reserved.
7	0h RW	**Device Mechanical Enable (DMPE):** When set, and P0IS.DMPS is set, the HBA shall generate an interrupt.
6	0h RW/V	**Port Change Interrupt Enable (PCE):** When set, GHC.IE is set, and P0IS.PCS is set, the HBA shall generate an interrupt.
5	0h RW	**Descriptor Processed Interrupt Enable (DPE):** When set, GHC.IE is set, and P0IS.DPS is set, the HBA shall generate an interrupt.
4	0h RW	**Unknown FIS Interrupt Enable (UFE):** When set, GHC.IE is set, and PxIS.UFS is set to 1, the HBA shall generate an interrupt.
3	0h RW	**Set Device Bits FIS Interrupt Enable (SDBE):** When set, GHC.IE is set, and P0IS.SDBS is set, the HBA shall generate an interrupt.
2	0h RW	**DMA Setup FIS Interrupt Enable (DSE):** When set, GHC.IE is set, and P0IS.DSS is set, the HBA shall generate an interrupt.
1	0h RW	**PIO Setup FIS Interrupt Enable (PSE):** When set, GHC.IE is set, and P0IS.PSS is set, the HBA shall generate an interrupt.
0	0h RW	**Device to Host Register FIS Interrupt Enable (DHRE):** When set, GHC.IE is set, and P0IS.DHRS is set, the HBA shall generate an interrupt.

18.3.36 Port [0-7] Command (PxCMD1)—Offset 198h

Port [0-7] Command

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4h

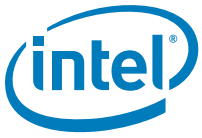
Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Interface Communication Control (ICC):** This is a four-bit field which can be used to control reset and power states of the interface. If the Link layer is currently in the L_IDLE state, writes to this field shall cause the HBA to initiate a transition to the interface power management state requested. If the Link layer is not currently in the L_IDLE state, writes to this field shall have no effect.
27	0h RW	**Aggressive Slumber Partial (ASP):** When set to 1, and the ALPE bit is set, the HBA shall aggressively enter the Slumber state when it clears a bit in the PxCI or PxSACT register and the register values are then PxCI = 0h and PxSACT = 0h. When cleared, and the ALPE bit is set, the HBA will aggressively enter the Partial state when it clears a bit in the PxCI or PxSACT register and the register values are then PxCI = 0h and PxSACT = 0h. If CAP.SALP is cleard to 0., software shall treat this bit as reserved.
26	0h RW	**Aggressive Link Power Management Enable (ALPE):** When set, the HBA will aggressively enter a lower link power state (Partial or Slumber) based upon the setting of the ASP bit. Software shall only set this bit to 1 if CAP.SALP is set to 1. If CAP.SALP is cleared to 0, software shall treat this bit as reserved. BIOS is recommeded to program this field to 1.
25	0h RW	**Drive LED on ATAPI Enable (DLAE):** When set, the HBA will drive the LED pin active for commands regardless of the state of PxCMD.ATAPI. When cleared, the HBA will only drive the LED pin active for commands if PxCMD.ATAPI is set to 0.. This bit is set by software
24	0h RW	**Device is ATAPI (ATAPI):** When set, the connected device is an ATAPI device. This bit is used by the HBA to control whether or not to generate the desktop LED when commands are active.
23	0h RW	**Automatic Partial to Slumber Transitions Enabled (APSTE):** When set to 1., the HBA may perform Automatic Partial to Slumber Transitions. When cleared to 0. the port shall not perform Automatic Partial to Slumber Transitions. Software shall only set this bit to 1. if CAP2.APST is set to 1.; if CAP2.APST is cleared to 0. software shall treat this bit as reserved.
22	0h RO	**FIS-based Switching Capable Port (FBSCP):** The SATA controller does not support FIS-Based Switching.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/O	**External SATA Port (ESP):** When set to 1, indicates that this port is routed externally and will be used with an external SATA device. When set to 1, CAP.SXS must also be set to 1. When cleared (0), indicates that this port is not routed externally and supports internal SATA devices only. If ESP is set to '1', then the port may experience hot plug events.
20	0h RO	**Cold Presence Detection (CPD):** The SATA controller does not support cold presence detect.
19	0h RW/O	**Mechanical Presence Switch Attached to Port (MPSP):** If set to 1, the platform supports a mechanical presence switch attached to this port. If cleared to 0, the platform does not support a mechanical presence switch attached to this port.
18	0h RW/O	**Hot Plug Capable Port (HPCP):** This indicates whether the this port is connected to a device which can be hot plugged. SATA by definition is hot-pluggable, but not all platforms are constructed to allow the device to be removed (it may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as eject device to the end-user.
17	0h RW/V	**Port Multiplier Attached (PMA):** When set, a Port Multiplier is attached to the HBA for this port. When cleared, a Port Multiplier is not attached to the HBA for this port. This bit is a read only 0. when CAP.PMS = 0., and read/write when CAP.PMS = 1.. Note that this bit is set by software; hardware does not auto-detect that a Port Multiplier is attached.
16	0h RO	Reserved.
15	0h RO/V	**Command List Running (CR):** When this bit is set it indicates that the command list DMA engine for the port is running.
14	0h RO/V	**FIS Receive Running (FR):** When this bit is set it indicates that the FIS Receive DMA engine for the port is running. Note to software: When FR bit stays set, please read the PxIS.PCS and PxSERR.DET.X to service the PCS interrupt accordingly if any
13	0h RO/V	**Mechanical Presence Switch State (MPSS):** The MPSS bit reports the state of a mechanical presence switch attached to this port. If CAP.SMPS is set to 1 and the mechanical presence switch is closed then this bit is cleared to 0. If CAP.SMPS is set to 1 and the mechanical presence switch is open then this bit is set to 1. If CAP.SMPS is set to 0 then this bit is cleared to 0. Software should only use this bit if both CAP.SMPS and PxCMD.MPSP are set to 1.

Bit Range	Default & Access	Field Name (ID): Description
12:8	0h RO/V	**Current Command Slot (CCS):** Indicates the current command slot the HBA is processing. This field is valid when the PxCMD.ST bit is set, and is constantly updated by the HBA. This field can be updated as soon as the HBA recognizes an active command slot, or at some point soon after when it begins processing the command. When PxCMD.ST transitions from a 1 to a 0, the HBA will reset this field to 0. After PxCMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is PxCMD.CCS + 1. For example, after the HBA has issued its first command, if PxCMD.CCS = 0h and PxCI is set to 3h, the next command that will be issued is from command slot 1.
7:5	0h RO	Reserved.
4	0h RW	**FIS Receive Enable (FRE):** When set, the HBA may post received FISes into the FIS receive area pointed to by PxFB and PxFBU. When cleared, received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence.
3	0h RW/1S	**Command List Override (CLO):** Setting this bit to 1 causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to 0 when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to 0. A write to this register with a value of 0 shall have no effect.
2	1h RO	**Power On Device (POD):** The SATA controller does not support cold presence detect.
1	0h RW/V	**Spin-Up Device (SUD):** This bit is read/write for HBAs that support staggered spin-up via CAP.SSS. This bit is read only 1. for HBAs that do not support staggered spin-up. On an edge detect from 0. to 1, the HBA shall start a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface. Clearing this bit to0 does not cause any OOB signal to be sent on the interface. When this bit is cleared to 0. and PxSCTL.DET = 0h, the HBA will enter listen mode.
0	0h RW	**Start (ST):** When set, the HBA may process the command list. When cleared, the HBA may not process the command list. Whenever this bit is changed from a 0 to a 1, the HBA starts processing the command list at entry 0. Whenever this bit is changed from a 1 ot a 0, the PxCI and PxSACT register is cleared by the HBA upon the HBA putting the controller into an idle state. PxTFD shall be updated also.

18.3.37 Port [0-7] Task File Data (PxTFD1)—Offset 1A0h

Port [0-7] Task File Data



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 7Fh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	0h RO/V	**Error (ERR):** Contains the latest copy of the task file error register.
7	0h RO/V	**Status Busy (STS_BSY):** Status - Indicates the interface is busy.
6:4	7h RO/V	**Status Rsvd0 (STS_RSVD0):** Status - Not Applicable.
3	1h RO/V	**Status Drq (STS_DRQ):** Status - Indicates a data transfer is requested.
2:1	3h RO/V	**Status Rsvd1 (STS_RSVD1):** Status - Not Applicable.
0	1h RO/V	**Status Err (STS_ERR):** Status - Indicates an error during the transfer.

18.3.38 Port [0-7] Signature (PxSIG1)—Offset 1A4h

Port [0-7] Signature

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RO/V	**Signature (SIG):** Contains the signature received from a device on the first D2H Register FIS.

18.3.39 Port [0-7] Serial ATA Status (PxSSTS1)—Offset 1A8h

Port [0-7] Serial ATA Status

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:8	0h RO/V	**Interface Power Management (IPM):** Indicates the current interface state
7:4	0h RO/V	**Current Interface Speed (SPD):** Indicates the negotiated interface communication speed.
3:0	0h RO/V	**Device Detection (DET):** Indicates the interface device detection and Phy state.

18.3.40 Port [0-7] Serial ATA Control (PxSCTL1)—Offset 1ACh

Port [0-7] Serial ATA Control

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:16	0h RW	**Port Multiplier Port (PMP):** This field is not used by AHCI.
15:12	0h RW	**Select Power Management (SPM):** This field is not used by AHCI.
11:8	0h RW	**Interface Power Management Transitions Allowed (IPM):** Indicates which power states the HBA is allowed to transition to. If an interface power management state is not allowed via this register field, the HBA will not initiate that state and the HBA will PMNAKP any request from the device to enter that state.
7:4	0h RW	**Speed Allowed (SPD):** Indicates the highest allowable speed of the interface.
3:0	0h RW	**Device Detection Initialization (DET):** Controls the HBA.s device detection and interface initialization.

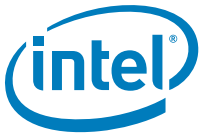
18.3.41 Port [0-7] Serial ATA Error (PxSERR1)—Offset 1B0h

Port [0-7] Serial ATA Error

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/1C/V	**Diagnostics (DIAG):** Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes.
15:0	0h RW/1C/V	**Error (ERR):** The ERR field contains error information for use by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer.

18.3.42 Port [0-7] Serial ATA Active (PxSACT1)—Offset 1B4h

Port [0-7] Serial ATA Active

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/1S/V	**Device Status (DS):** System software sets this bit for native command queuing commands prior to setting the PxCI.CI bit in the same command slot entry. This field is cleared via the Set Device Bits FIS.

18.3.43 Port [0-7] Commands Issued (PxCI1)—Offset 1B8h

Port [0-7] Commands Issued

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/1S/V	**Commands Issued (CI):** This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, ERR, and DRQ bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to 1 by software when PxCMD.ST is set to 1.

18.3.44 Port [0-7] SNotification (PxSNTF1)—Offset 1BCh

Port [0-7] SNotification

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW/1C/V	**PM Notify (PMN):** This field indicates whether a particular device with the corresponding PM Port number issued a Set Device Bits FIS to the host with the Notification bit set. PM Port 0h sets bit 0. PM Port Fh sets bit 15. Individual bits are cleared by software writing 1's to the corresponding bit positions. Note that, while this field is reset to default on a HBA Reset, it is not reset by COMRESET or SRST

18.3.45 Port [0-7] Device Sleep (PxDEVSLP1)—Offset 1C4h

Port [0-7] Device Sleep

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1E022852h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:25	Fh RW/V	**DITO Multiplier (DM):** 0's based value that specifies the DITO multiplier that the HBA applies to the specified DITO value, effectively extending the range of DITO from 1ms to 16368ms. A value of 0h indicates a multiplier of 1. A maximum multiplier of 16 may be applied. The HBA computes the total idle timeout as a product of DM and DITO (i.e. DITO actual = DITO * DM).

Bit Range	Default & Access	Field Name (ID): Description
24:15	4h RW/V	**DEVSLP Idle Timeout (DITO):** This field specifies the amount of the time (in approximate 1ms granularity) that the HBA shall wait before driving the DEVSLP signal.Hardware reloads its port specific DEVSLP timer with this value each time the port transitions out of DEVSLP state. For example: from DEVSLP to active or PxDEVSLP.ADSE transitions from 0 to a 1. If CAP2.SDS or CAP2.SADM or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0 and PxDEVSLP.ADSE is cleared to 0.
14:10	Ah RW/V	**DEVSLP Minimum Assertion Time (MDAT):** This field specifies the minimum amount of time (in 1ms granularity) that the HBA must assert the DEVSLP signal before it may be de-asserted. The nominal value is 10ms and the minimum is 1ms depending on device identification information. If CAP2.SDS is cleared to 0 or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0, PxDEVSLP.ADSE is cleared to 0, and prior to setting PxCMD.ICC to 8h.
9:2	14h RW/V	**DEVSLP Exit Timeout (DETO):** This field specifies the maximum duration (in approximate 1ms granularity) from DEVSLP de-assertion until the device is ready to accept OOB. The nominal value is 20ms while the max value is 255ms depending on device identification information. If CAP2.SDS is cleared to 0 or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0, PxDEVSLP.ADSE is cleared to 0, and prior to setting PxCMD.ICC to 8h.
1	1h RW/O	**DEVSLP Present (DSP):** If set to '1', the platform supports DEVSLP on this port. If cleared to '0', the platform does not support DEVSLP on this port. This bit may only be set to '1' if CAP2.SDS is set to '1'.DSP is mutually exclusive with the PxCMD.HPCP bit and PxCMD.ESP bit. Note that these bits are not reset on a HBA reset.
0	0h RW/V	**Aggressive DEVSLP Enable (ADSE):** This bit is read/write for HBAs that support aggressive DEVSLP management (CAP2. SADM = 1). When this bit is set to 1, the HBA shall assert the DEVSLP signal after the port has been idle (PxCI = 0h and PxSACT = 0h) for the amount of time specified by the PxDEVSLP.DITO register and the interface is in Slumber (PxSSTS.IPM = 6h). When this bit is cleared to 0, the HBA does not enter DEVSLP unless software directed via PxCMD.ICC. This bit shall only be set to 1 if PxDEVSLP.DSP is set to 1. If this bit is set to 1 and software clears the bit to 0, then the HBA shall de-assert the DEVSLP signal if asserted. Note that these bits are not reset on a HBA reset. BIOS is recommended to program this field to 1 if the platform support the DEVSLP feature. If CAP2.SDS is cleared to 0 or CAP2.SADM is cleared to 0, or if PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved.

18.3.46 Enclosure Management Message Format (EM_MF)—Offset 580h

Enclosure Management Message Format

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:24	0h RW	**Message Type (MTYPE):** Specifies the type of the message. The message types are: • 0h: LED. • 1h: SAF-TE. • 2h: SES-2. • 3h: SGPIO (register based interface). • All other values reserved.
23:16	0h RW	**Data Size (DSIZE):** Specifies the data size in bytes. If the message (enclosure services command) has a data buffer that is associated with it that is transferred, the size of that data buffer is specified in this field. If there is no separate data buffer, this field shall have a value of '0'. The data directly follows the message in the message buffer. This value should always be '0'.
15:8	0h RW	**Message Size (MSIZE):** Specifies the size of the message in bytes. The message size does not include the one Dword header. A value of '0'. is invalid. The message size is always 4 bytes.
7:0	0h RO	Reserved.

18.3.47 Enclosure Management LED (EM_LED)—Offset 584h

Enclosure Management LED

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Value (VAL):** This field describes the state of each LED for a particular location. There are three LEDs that may be supported by the HBA. Each LED has 3 bits of control. LED values are: 000b - LED shall be off; 001b - LED shall be solid on as perceived by human eye; All other values reserved. The LED bit locations are: Bits 2:0 - Activity LED (may be driven by hardware); Bits 5:3 - Vendor Specific LED (e.g. locate); Bits 8:6 - Vendor Specific LED (e.g. fault); Bits 15:9 - Reserved. Vendor specific message is: Bit 3:0 - Vendor Specific Pattern; Bit 15:4 - Reserved. Note: If Activity LED Hardware Driven (ATTR.ALHD) bit is set, host will output the hardware LED value sampled internally and will ignore software written activity value on bit [2:0]. Since Enclosure Management does not support port multiplier based LED message, the LED message will be generated independently based on respective port's operation activity. Vendor specific LED values Locate (Bits 5:3) and Fault (Bits 8:6) always are driven by software..
15:8	0h RW	**Port Multiplier Information (PM):** Specifies slot specific information related to Port Multiplier. Bits 3:0 specify the Port Multiplier port number for the slot that requires the status update. If a Port Multiplier is not attached to the device in the affected slot, the Port Multiplier port number shall be '0'. Bits 7:4 are reserved. SATA does not support LED messages for devices behind a Port MUltiplier. This byte should be 0.
7:0	0h RW	**HBA Information (HBA):** Specifies slot specific information related to the HBA. Bits 4:0 - HBA port number for the slot that requires the status update. Bit 5 - If set to '1', Value is a vendor specific message that applies to the entire enclosure. If cleared to '0', Value applies to the port specified in bits 4:0. Bits 7:6 - Reserved.

18.4 Registers Summary

Table 18-4. Summary of sata_configreg_top Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	MSI-X Pending Bit Array QW 0 (MXPQW0_DW0)—Offset 0h	0h
4h	7h	MSI-X Pending Bit Array QW 1 (MXPQW0_DW1)—Offset 4h	0h

18.4.1 MSI-X Pending Bit Array QW 0 (MXPQW0_DW0)—Offset 0h

MSI-X Pending Bit Array QW 0

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO/V	**MSI-X Vector Pending (MXVP):** For each Pending Bit that is set, the function has a pending message for the associated MSI-X Table entry. Pending bits that have no associated MSI-X Table entry are reserved. After reset, the state of reserved Pending bits must be 0. Software should never write, and should only read Pending Bits. If software writes to Pending Bits, the result is undefined. Each Pending Bit's state after reset is 0 (no message pending).

18.4.2 MSI-X Pending Bit Array QW 1 (MXPQW0_DW1)—Offset 4h

MSI-X Pending Bit Array QW 1

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**MSI-X Vector Pending QW1 (Rsvd):** For each Pending Bit that is set, the function has a pending message for the associated MSI-X Table entry. Pending bits that have no associated MSI-X Table entry are reserved. After reset, the state of reserved Pending bits must be 0. Software should never write, and should only read Pending Bits. If software writes to Pending Bits, the result is undefined. Each Pending Bit's state after reset is 0 (no message pending).

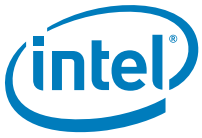
18.5 Registers Summary

Table 18-5. Summary of sata_configreg_top Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	MSI-X Table Entries 0 Message Lower Address (MXTE0MLA)—Offset 0h	0h
4h	7h	MSI-X Table Entries 0 Message Upper Address (MXTE0MUA)—Offset 4h	0h
8h	Bh	MSI-X Table Entries 0 Message Data (MXTE0MD)—Offset 8h	0h
Ch	Fh	MSI-X Table Entries 0 Vector Control (MXTE0VC)—Offset Ch	1h

18.5.1 MSI-X Table Entries 0 Message Lower Address (MXTE0MLA)—Offset 0h

MSI-X Table Entries 0 Message Lower Address



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**MSI-X Message Lower Address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

18.5.2 MSI-X Table Entries 0 Message Upper Address (MXTE0MUA)—Offset 4h

MSI-X Table Entries 0 Message Upper Address

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSI-X Message Upper 32-Bit Address (MXMUA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.

18.5.3 MSI-X Table Entries 0 Message Data (MXTE0MD)—Offset 8h

MSI-X Table Entries 0 Message Data

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSI-X Message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

18.5.4 MSI-X Table Entries 0 Vector Control (MXTE0VC)—Offset Ch

MSI-X Table Entries 0 Vector Control

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X Vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

§ §

19 USB

19.1 Registers Summary

Table 19-1. Summary of 0_20_0_USBx MMIO Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	0h	Capability Registers Length (CAPLENGTH)—Offset 0h	80h
2h	3h	Host Controller Interface Version Number (HCIVERSION)—Offset 2h	100h
4h	7h	Structural Parameters 1 (HCSPARAMS1)—Offset 4h	F000820h
8h	Bh	Structural Parameters 2 (HCSPARAMS2)—Offset 8h	94000054h
Ch	Fh	Structural Parameters 3 (HCSPARAMS3)—Offset Ch	40001h
10h	13h	Capability Parameters (HCCPARAMS)—Offset 10h	200077C1h
14h	17h	Doorbell Offset (DBOFF)—Offset 14h	3000h
18h	1Bh	Runtime Register Space Offset (RTSOFF)—Offset 18h	2000h
80h	83h	USB Command (USBCMD)—Offset 80h	0h
84h	87h	USB Status (USBSTS)—Offset 84h	1h
88h	8Bh	Page Size (PAGESIZE)—Offset 88h	1h
94h	97h	Device Notification Control (DNCTRL)—Offset 94h	0h
98h	9Bh	Command Ring Low (CRCR_LO)—Offset 98h	0h
9Ch	9Fh	Command Ring High (CRCR_HI)—Offset 9Ch	0h
B0h	B3h	Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h	0h
B4h	B7h	Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h	0h
B8h	BBh	Configure (CONFIG)—Offset B8h	0h
480h	483h	Port Status and Control USB2 (PORTSC1)—Offset 480h	2A0h
484h	487h	Port Power Management Status and Control USB2 (PORTPMSC1)—Offset 484h	0h
48Ch	48Fh	Port X Hardware LPM Control Register (PORTHLPMC1)—Offset 48Ch	0h
490h	493h	Port Status and Control USB2 (PORTSC2)—Offset 490h	2A0h
494h	497h	Port Power Management Status and Control USB2 (PORTPMSC2)—Offset 494h	0h
49Ch	49Fh	Port X Hardware LPM Control Register (PORTHLPMC2)—Offset 49Ch	0h
4A0h	4A3h	Port Status and Control USB2 (PORTSC3)—Offset 4A0h	2A0h
4A4h	4A7h	Port Power Management Status and Control USB2 (PORTPMSC3)—Offset 4A4h	0h
4ACh	4AFh	Port X Hardware LPM Control Register (PORTHLPMC3)—Offset 4ACh	0h
4B0h	4B3h	Port Status and Control USB2 (PORTSC4)—Offset 4B0h	2A0h
4B4h	4B7h	Port Power Management Status and Control USB2 (PORTPMSC4)—Offset 4B4h	0h

Table 19-1. Summary of 0_20_0_USBx MMIO Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4BCh	4BFh	Port X Hardware LPM Control Register (PORTHLPMC4)—Offset 4BCh	0h
4C0h	4C3h	Port Status and Control USB2 (PORTSC5)—Offset 4C0h	2A0h
4C4h	4C7h	Port Power Management Status and Control USB2 (PORTPMSC5)—Offset 4C4h	0h
4CCh	4CFh	Port X Hardware LPM Control Register (PORTHLPMC5)—Offset 4CCh	0h
4D0h	4D3h	Port Status and Control USB2 (PORTSC6)—Offset 4D0h	2A0h
4D4h	4D7h	Port Power Management Status and Control USB2 (PORTPMSC6)—Offset 4D4h	0h
4DCh	4DFh	Port X Hardware LPM Control Register (PORTHLPMC6)—Offset 4DCh	0h
4E0h	4E3h	Port Status and Control USB2 (PORTSC7)—Offset 4E0h	2A0h
4E4h	4E7h	Port Power Management Status and Control USB2 (PORTPMSC7)—Offset 4E4h	0h
4ECh	4EFh	Port X Hardware LPM Control Register (PORTHLPMC7)—Offset 4ECh	0h
4F0h	4F3h	Port Status and Control USB2 (PORTSC8)—Offset 4F0h	2A0h
4F4h	4F7h	Port Power Management Status and Control USB2 (PORTPMSC8)—Offset 4F4h	0h
4FCh	4FFh	Port X Hardware LPM Control Register (PORTHLPMC8)—Offset 4FCh	0h
500h	503h	Port Status and Control USB3 (PORTSC9)—Offset 500h	2A0h
504h	507h	Port Power Management Status and Control USB3 (PORTPMSC9)—Offset 504h	0h
508h	50Bh	USB3 Port Link Info (PORTLI9)—Offset 508h	0h
510h	513h	Port Status and Control USB3 (PORTSC10)—Offset 510h	2A0h
514h	517h	Port Power Management Status and Control USB3 (PORTPMSC10)—Offset 514h	0h
518h	51Bh	USB3 Port Link Info (PORTLI10)—Offset 518h	0h
520h	523h	Port Status and Control USB3 (PORTSC11)—Offset 520h	2A0h
524h	527h	Port Power Management Status and Control USB3 (PORTPMSC11)—Offset 524h	0h
528h	52Bh	USB3 Port Link Info (PORTLI11)—Offset 528h	0h
530h	533h	Port Status and Control USB3 (PORTSC12)—Offset 530h	2A0h
534h	537h	Port Power Management Status and Control USB3 (PORTPMSC12)—Offset 534h	0h
538h	53Bh	USB3 Port Link Info (PORTLI12)—Offset 538h	0h
540h	543h	Port Status and Control USB3 (PORTSC13)—Offset 540h	2A0h
544h	547h	Port Power Management Status and Control USB3 (PORTPMSC13)—Offset 544h	0h
548h	54Bh	USB3 Port Link Info (PORTLI13)—Offset 548h	0h
550h	553h	Port Status and Control USB3 (PORTSC14)—Offset 550h	2A0h
554h	557h	Port Power Management Status and Control USB3 (PORTPMSC14)—Offset 554h	0h
558h	55Bh	USB3 Port Link Info (PORTLI14)—Offset 558h	0h

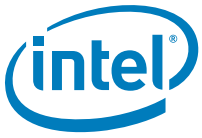


Table 19-1. Summary of 0_20_0_USBx MMIO Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
560h	563h	Port Status and Control USB3 (PORTSC15)—Offset 560h	2A0h
564h	567h	Port Power Management Status and Control USB3 (PORTPMSC15)—Offset 564h	0h
568h	56Bh	USB3 Port Link Info (PORTLI15)—Offset 568h	0h
2000h	2003h	Microframe Index (RTMFINDEX)—Offset 2000h	0h
2020h	2023h	Interrupter 1 Management (IMAN0)—Offset 2020h	0h
2024h	2027h	Interrupter 1 Moderation (IMOD0)—Offset 2024h	FA0h
2028h	202Bh	Event Ring Segment Table Size 1 (ERSTSZ0)—Offset 2028h	0h
2030h	2033h	Event Ring Segment Table Base Address Low 1 (ERSTBA_LO0)—Offset 2030h	0h
2034h	2037h	Event Ring Segment Table Base Address High 1 (ERSTBA_HI0)—Offset 2034h	0h
2038h	203Bh	Event Ring Dequeue Pointer Low 1 (ERDP_LO0)—Offset 2038h	0h
203Ch	203Fh	Event Ring Dequeue Pointer High 1 (ERDP_HI0)—Offset 203Ch	0h
2040h	2043h	Interrupter 2 Management (IMAN1)—Offset 2040h	0h
2044h	2047h	Interrupter 2 Moderation (IMOD1)—Offset 2044h	FA0h
2048h	204Bh	Event Ring Segment Table Size 2 (ERSTSZ1)—Offset 2048h	0h
2050h	2053h	Event Ring Segment Table Base Address Low 2 (ERSTBA_LO1)—Offset 2050h	0h
2054h	2057h	Event Ring Segment Table Base Address High 2 (ERSTBA_HI1)—Offset 2054h	0h
2058h	205Bh	Event Ring Dequeue Pointer Low 2 (ERDP_LO1)—Offset 2058h	0h
205Ch	205Fh	Event Ring Dequeue Pointer High 2 (ERDP_HI1)—Offset 205Ch	0h
2060h	2063h	Interrupter 3 Management (IMAN2)—Offset 2060h	0h
2064h	2067h	Interrupter 3 Moderation (IMOD2)—Offset 2064h	FA0h
2068h	206Bh	Event Ring Segment Table Size 3 (ERSTSZ2)—Offset 2068h	0h
2070h	2073h	Event Ring Segment Table Base Address Low 3 (ERSTBA_LO2)—Offset 2070h	0h
2074h	2077h	Event Ring Segment Table Base Address High 3 (ERSTBA_HI2)—Offset 2074h	0h
2078h	207Bh	Event Ring Dequeue Pointer Low 3 (ERDP_LO2)—Offset 2078h	0h
207Ch	207Fh	Event Ring Dequeue Pointer High 3 (ERDP_HI2)—Offset 207Ch	0h
2080h	2083h	Interrupter 4 Management (IMAN3)—Offset 2080h	0h
2084h	2087h	Interrupter 4 Moderation (IMOD3)—Offset 2084h	FA0h
2088h	208Bh	Event Ring Segment Table Size 4 (ERSTSZ3)—Offset 2088h	0h
2090h	2093h	Event Ring Segment Table Base Address Low 4 (ERSTBA_LO3)—Offset 2090h	0h
2094h	2097h	Event Ring Segment Table Base Address High 4 (ERSTBA_HI3)—Offset 2094h	0h
2098h	209Bh	Event Ring Dequeue Pointer Low 4 (ERDP_LO3)—Offset 2098h	0h
209Ch	209Fh	Event Ring Dequeue Pointer High 4 (ERDP_HI3)—Offset 209Ch	0h
20A0h	20A3h	Interrupter 5 Management (IMAN4)—Offset 20A0h	0h
20A4h	20A7h	Interrupter 5 Moderation (IMOD4)—Offset 20A4h	FA0h
20A8h	20ABh	Event Ring Segment Table Size 5 (ERSTSZ4)—Offset 20A8h	0h

Table 19-1. Summary of 0_20_0_USBx MMIO Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
20B0h	20B3h	Event Ring Segment Table Base Address Low 5 (ERSTBA_LO4)—Offset 20B0h	0h
20B4h	20B7h	Event Ring Segment Table Base Address High 5 (ERSTBA_HI4)—Offset 20B4h	0h
20B8h	20BBh	Event Ring Dequeue Pointer Low 5 (ERDP_LO4)—Offset 20B8h	0h
20BCh	20BFh	Event Ring Dequeue Pointer High 5 (ERDP_HI4)—Offset 20BCh	0h
20C0h	20C3h	Interrupter 6 Management (IMAN5)—Offset 20C0h	0h
20C4h	20C7h	Interrupter 6 Moderation (IMOD5)—Offset 20C4h	FA0h
20C8h	20CBh	Event Ring Segment Table Size 6 (ERSTSZ5)—Offset 20C8h	0h
20D0h	20D3h	Event Ring Segment Table Base Address Low 6 (ERSTBA_LO5)—Offset 20D0h	0h
20D4h	20D7h	Event Ring Segment Table Base Address High 6 (ERSTBA_HI5)—Offset 20D4h	0h
20D8h	20DBh	Event Ring Dequeue Pointer Low 6 (ERDP_LO5)—Offset 20D8h	0h
20DCh	20DFh	Event Ring Dequeue Pointer High 6 (ERDP_HI5)—Offset 20DCh	0h
20E0h	20E3h	Interrupter 7 Management (IMAN6)—Offset 20E0h	0h
20E4h	20E7h	Interrupter 7 Moderation (IMOD6)—Offset 20E4h	FA0h
20E8h	20EBh	Event Ring Segment Table Size 7 (ERSTSZ6)—Offset 20E8h	0h
20F0h	20F3h	Event Ring Segment Table Base Address Low 7 (ERSTBA_LO6)—Offset 20F0h	0h
20F4h	20F7h	Event Ring Segment Table Base Address High 7 (ERSTBA_HI6)—Offset 20F4h	0h
20F8h	20FBh	Event Ring Dequeue Pointer Low 7 (ERDP_LO6)—Offset 20F8h	0h
20FCh	20FFh	Event Ring Segment Table Base Address Low 1 (ERSTBA_LO0)—Offset 2030h	0h
2100h	2103h	Interrupter 8 Management (IMAN7)—Offset 2100h	0h
2104h	2107h	Interrupter 8 Moderation (IMOD7)—Offset 2104h	FA0h
2108h	210Bh	Event Ring Segment Table Size 8 (ERSTSZ7)—Offset 2108h	0h
2110h	2113h	Event Ring Segment Table Base Address Low 8 (ERSTBA_LO7)—Offset 2110h	0h
2114h	2117h	Event Ring Segment Table Base Address High 8 (ERSTBA_HI7)—Offset 2114h	0h
2118h	211Bh	Event Ring Dequeue Pointer Low 8 (ERDP_LO7)—Offset 2118h	0h
211Ch	211Fh	Event Ring Dequeue Pointer High 8 (ERDP_HI7)—Offset 211Ch	0h
3000h	3003h	Door Bell 1 (DB0)—Offset 3000h	0h
3004h	3007h	Door Bell 2 (DB1)—Offset 3004h	0h
3008h	300Bh	Door Bell 3 (DB2)—Offset 3008h	0h
300Ch	300Fh	Door Bell 4 (DB3)—Offset 300Ch	0h
3010h	3013h	Door Bell 5 (DB4)—Offset 3010h	0h
3014h	3017h	Door Bell 6 (DB5)—Offset 3014h	0h
3018h	301Bh	Door Bell 7 (DB6)—Offset 3018h	0h
301Ch	301Fh	Door Bell 8 (DB7)—Offset 301Ch	0h
3020h	3023h	Door Bell 9 (DB8)—Offset 3020h	0h
3024h	3027h	Door Bell 10 (DB9)—Offset 3024h	0h

Table 19-1. Summary of 0_20_0_USBx MMIO Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3028h	302Bh	Door Bell 11 (DB10)—Offset 3028h	0h
302Ch	302Fh	Door Bell 12 (DB11)—Offset 302Ch	0h
3030h	3033h	Door Bell 13 (DB12)—Offset 3030h	0h
3034h	3037h	Door Bell 14 (DB13)—Offset 3034h	0h
3038h	303Bh	Door Bell 15 (DB14)—Offset 3038h	0h
303Ch	303Fh	Door Bell 16 (DB15)—Offset 303Ch	0h
3040h	3043h	Door Bell 17 (DB16)—Offset 3040h	0h
3044h	3047h	Door Bell 18 (DB17)—Offset 3044h	0h
3048h	304Bh	Door Bell 19 (DB18)—Offset 3048h	0h
304Ch	304Fh	Door Bell 20 (DB19)—Offset 304Ch	0h
3050h	3053h	Door Bell 21 (DB20)—Offset 3050h	0h
3054h	3057h	Door Bell 22 (DB21)—Offset 3054h	0h
3058h	305Bh	Door Bell 23 (DB22)—Offset 3058h	0h
305Ch	305Fh	Door Bell 24 (DB23)—Offset 305Ch	0h
3060h	3063h	Door Bell 25 (DB24)—Offset 3060h	0h
3064h	3067h	Door Bell 26 (DB25)—Offset 3064h	0h
3068h	306Bh	Door Bell 27 (DB26)—Offset 3068h	0h
306Ch	306Fh	Door Bell 28 (DB27)—Offset 306Ch	0h
3070h	3073h	Door Bell 29 (DB28)—Offset 3070h	0h
3074h	3077h	Door Bell 30 (DB29)—Offset 3074h	0h
3078h	307Bh	Door Bell 31 (DB30)—Offset 3078h	0h
307Ch	307Fh	Door Bell 32 (DB31)—Offset 307Ch	0h
3080h	3083h	Door Bell 32 (DB32)—Offset 3080h	0h
8000h	8003h	XECP_SUPP_USB2_0 (XECP_SUPP_USB2_0)—Offset 8000h	2000802h
8004h	8007h	XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1)—Offset 8004h	20425355h
8008h	800Bh	XECP_SUPP_USB2_2 (XECP_SUPP_USB2_2)—Offset 8008h	30190801h
8010h	8013h	XECP_SUPP_USB2_3 (Full Speed) (XECP_SUPP_USB2_3)—Offset 8010h	C0021h
8014h	8017h	XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_4)—Offset 8014h	5DC0012h
8018h	801Bh	XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_5)—Offset 8018h	1E00023h
8020h	8023h	XECP_SUPP_USB3_0 (XECP_SUPP_USB3_0)—Offset 8020h	3001402h
8024h	8027h	XECP_SUPP_USB3_1 (XECP_SUPP_USB3_1)—Offset 8024h	20425355h
8028h	802Bh	XECP_SUPP_USB3_2 (XECP_SUPP_USB3_2)—Offset 8028h	30000709h
8030h	8033h	XECP_SUPP_USB3_3 (XECP_SUPP_USB3_3)—Offset 8030h	4E00121h
8034h	8037h	XECP_SUPP_USB3_4 (XECP_SUPP_USB3_4)—Offset 8034h	9C00122h
8038h	803Bh	XECP_SUPP_USB3_5 (XECP_SUPP_USB3_5)—Offset 8038h	13800123h
803Ch	803Fh	XECP_SUPP_USB3_6 (XECP_SUPP_USB3_6)—Offset 803Ch	50134h
8040h	8043h	XECP_SUPP_USB3_7 (XECP_SUPP_USB3_7)—Offset 8040h	5B10125h
8044h	8047h	XECP_SUPP_USB3_8 (XECP_SUPP_USB3_8)—Offset 8044h	B630126h

Table 19-1. Summary of 0_20_0_USBx MMIO Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8048h	804Bh	XECP_SUPP_USB3_9 (XECP_SUPP_USB3_9)—Offset 8048h	16C60127h
8070h	8073h	Host Controller Capability (HOST_CTRL_CAP_REG)—Offset 8070h	4DFFC0h
8078h	807Bh	Override EP Flow Control (HOST_CLR_MASK_REG)—Offset 8078h	0h
807Ch	807Fh	Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG)—Offset 807Ch	0h
8080h	8083h	Clear Poll Mask Control (HOST_CLR_PMASK_REG)—Offset 8080h	0h
8084h	8087h	Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h	0h
8088h	808Bh	Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h	4000h
8090h	8093h	Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h	4C1BD105h
8094h	8097h	Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h	8100h
8098h	809Bh	Global Port Control (HOST_CTRL_PORT_CTRL)—Offset 80A0h	14003002h
80A0h	80A3h	Global Port Control (HOST_CTRL_PORT_CTRL)—Offset 80A0h	380Fh
80A4h	80A7h	Power Management Control (PMCTRL_REG)—Offset 80A4h	2DFF90h
80A8h	80ABh	PGCB Control (PGCBCTRL_REG)—Offset 80A8h	315555h
80ACh	80AFh	D0I3 Control (DOI3CTRL_REG)—Offset 80ACh	8h
80B0h	80B3h	HOST_CTRL_MISC_REG (HOST_CTRL_MISC_REG)—Offset 80B0h	1037Fh
80B4h	80B7h	HOST_CTRL_MISC_REG2 (HOST_CTRL_MISC_REG2)—Offset 80B4h	0h
80B8h	80BBh	SSPE_REG (SSPE_REG)—Offset 80B8h	0h
80BCh	80BFh	(SSPITPE)—Offset 80BCh	7Fh
80C0h	80C3h	AUX Reset Control (AUX_CTRL_REG)—Offset 80C0h	15FC0F0h
80C4h	80C7h	Super Speed Bandwidth Overload (HOST_BW_OV_SS_REG)—Offset 80C4h	4A4008h
80C8h	80CBh	High Speed TT Bandwidth Overload (HOST_BW_OV_HS_REG)—Offset 80C8h	1A01Fh
80CCh	80CFh	Bandwidth Overload Full Low Speed (HOST_BW_OV_FS_LS_REG)—Offset 80CCh	14080h
80D0h	80D3h	System Bandwidth Overload (HOST_BW_OV_SYS_REG)—Offset 80D0h	32010h
80D4h	80D7h	Scheduler Async Delay (HOST_CTRL_SCH_ASYNC_DELAY_REG)—Offset 80D4h	0h
80D8h	80DBh	DEVICE MODE CONTROL REG 0 (DUAL_ROLE_CFG_REG0)—Offset 80D8h	800h
80DCh	80DFh	DEVICE MODE CONTROL REG 1 (DUAL_ROLE_CFG_REG1)—Offset 80DCh	10000000h
80E0h	80E3h	AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h	808DBCA0h
80E4h	80E7h	Battery Charge (BATTERY_CHARGE_REG)—Offset 80E4h	0h
80E8h	80EBh	Port Watermark (HOST_CTRL_WATERMARK_REG)—Offset 80E8h	800080h

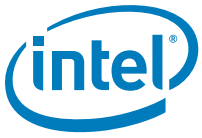


Table 19-1. Summary of 0_20_0_USBx MMIO Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
80ECh	80EFh	SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh	18010000h
80F0h	80F3h	USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h	310803A0h
80F4h	80F7h	USB2 Port Link Control 2 (USB2_LINK_MGR_CTRL_REG2)—Offset 80F4h	80C40620h
80F8h	80FBh	USB2 Port Link Control 3 (USB2_LINK_MGR_CTRL_REG3)—Offset 80F8h	F865EB6Bh
80FCh	80FFh	USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh	8003h
8100h	8103h	Bandwidth Calc Control (HOST_CTRL_BW_CTRL_REG)—Offset 8100h	8008h
8108h	810Bh	Host Interface Control (HOST_IF_CTRL_REG)—Offset 8108h	1h
810Ch	810Fh	Bandwidth Overload Burst (HOST_BW_OV_BURST_REG)—Offset 810Ch	8020h
8110h	8113h	USB Max Bandwidth Control 4 (HOST_CTRL_BW_MAX_REG)—Offset 8128h	F0EC838Ch
8128h	812Fh	USB Max Bandwidth Control 4 (HOST_CTRL_BW_MAX_REG)—Offset 8128h	F42528505647F42h
8130h	8133h	USB2 Linestate Debug (LINESTATE_DEBUG_REG)—Offset 8130h	0h
8134h	813Bh	USB2 Protocol Gap Timer (USB2_PROTOCOL_GAP_TIMER_REG)—Offset 8134h	C3C640C05140Ch
813Ch	813Fh	USB2 Protocol Bus Timeout Timer (USB2_PROTOCOL_BTO_TIMER_REG)—Offset 813Ch	8D4258B8h
8140h	8143h	Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h	A019132h
8144h	8147h	Power Scheduler Control-2 (PWR_SCHED_CTRL2)—Offset 8144h	33Fh
8154h	8157h	AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h	81390206h
8164h	8167h	USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h	FCh
8168h	816Bh	USB Power Gating Control (USB_PGC)—Offset 8168h	282EEh
816Ch	816Fh	xHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch	400h
8170h	8173h	USB LPM Parameters (USB_LPM_PARAM)—Offset 8170h	96090032h
8174h	8177h	xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1)—Offset 8174h	40047Dh
8178h	817Bh	xHC Latency Tolerance Parameters LTV Control 2 (XLTP_LTV2)—Offset 8178h	17FFh
817Ch	817Fh	xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC)—Offset 817Ch	0h
8180h	8183h	xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC)—Offset 8180h	0h
8184h	8187h	xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h	0h
8188h	818Bh	HOST_CTRL_BW_MAX3_REG (HOST_CTRL_BW_MAX3_REG)—Offset 8188h	F42F42h
818Ch	818Fh	PDDIS_REG (PDDIS_REG)—Offset 8198h	3500AFFCh

Table 19-1. Summary of 0_20_0_USBx MMIO Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8198h	819Bh	PDDIS_REG (PDDIS_REG)—Offset 8198h	0h
819Ch	819Fh	THRM_HOST_CTRL_REG (THRM_HOST_CTRL_REG)—Offset 819Ch	0h
81A0h	81A3h	LFPS_PM_CTRL_REG (LFPS_PM_CTRL_REG)—Offset 81A0h	0h
81A4h	81A7h	U2PDM (U2PDM)—Offset 81A4h	0h
81A8h	81ABh	U2PCM (U2PCM)—Offset 81A8h	0h
81ACh	81AFh	U3PDM (U3PDM)—Offset 81ACh	0h
81B0h	81B3h	U3PCM (U3PCM)—Offset 81B0h	0h
81B4h	81B7h	THRM_HOST_CTRL_REG2 (THRM_HOST_CTRL_REG2)—Offset 81B4h	7Fh
81B8h	81BBh	LFPSONCOUNT_REG (LFPSONCOUNT_REG)—Offset 81B8h	20C8h
81BCh	81BFh	(D0i2_CTRL_REG)—Offset 81BCh	84204B0h
81C0h	81C3h	(D0i2_SCH_ALARM_CTRL_REG)—Offset 81C0h	0h
81C4h	81C7h	(USB2PMCTRL_REG)—Offset 81C4h	0h
83F8h	83FBh	ECC_PARITY_ERROR_LOG_REG (ECC_PARITY_ERROR_LOG_REG)—Offset 83F8h	0h
83FCh	83FFh	ECC_POISONING_CTRL_REG (ECC_POISONING_CTRL_REG)—Offset 83FCh	0h
8400h	8407h	USB2_PORT_STATE_REG (USB2_PORT_STATE_REG)—Offset 8400h	0h
8408h	840Fh	USB3_PORT_STATE_REG (USB3_PORT_STATE_REG)—Offset 8408h	0h
8410h	8413h	FUS1_REG (FUS1_REG)—Offset 8410h	10000h
8414h	8417h	FUS2_REG (FUS2_REG)—Offset 8414h	0h
8418h	841Bh	FUS3_REG (FUS3_REG)—Offset 8418h	0h
841Ch	841Fh	STRAP1_REG (STRAP1_REG)—Offset 841Ch	0h
8420h	8423h	STRAP2_REG (STRAP2_REG)—Offset 8420h	0h
8424h	8427h	STRAP3_REG (STRAP3_REG)—Offset 8424h	0h
8430h	8433h	DFT_REG1 (DFT_REG1)—Offset 8430h	0h
8434h	8437h	DFT_REG2 (DFT_REG2)—Offset 8434h	0h
8438h	843Bh	DFT_REG3 (DFT_REG3)—Offset 8438h	0h
843Ch	843Fh	dft_reg4 (DFT_REG4)—Offset 843Ch	0h
8440h	8443h	dft_reg5 (DFT_REG5)—Offset 8440h	0h
8448h	844Bh	XECP_CMDM_STS0 (XECP_CMDM_STS0)—Offset 8448h	0h
844Ch	844Fh	XECP_CMDM_STS1 (XECP_CMDM_STS1)—Offset 844Ch	3FC0000h
8450h	8453h	XECP_CMDM_STS2 (XECP_CMDM_STS2)—Offset 8450h	0h
8454h	8457h	XECP_CMDM_STS3 (XECP_CMDM_STS3)—Offset 8454h	0h
8458h	845Bh	XECP_CMDM_STS4 (XECP_CMDM_STS4)—Offset 8458h	0h
845Ch	845Fh	XECP_CMDM_STS5 (XECP_CMDM_STS5)—Offset 845Ch	0h
8460h	8463h	AUX Power PHY Reset (UPORTS_PON_RST_REG)—Offset 8460h	0h
8464h	8467h	Latency Tolerance Control 0 (HOST_IF_LAT_TOL_CTRL_REG0)—Offset 8464h	D0000h

Table 19-1. Summary of 0_20_0_USBx MMIO Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
846Ch	846Fh	USB Legacy Support Capability (USBLEGSUP)—Offset 846Ch	2201h
8470h	8473h	USB Legacy Support Control Status (USBLEGCTLSTS)—Offset 8470h	0h
84F4h	84F7h	Port Disable Override capability register (PDO_CAPABILITY)—Offset 84F4h	3C6h
84F8h	84FBh	USB2 Port Disable Override (USB2PDO)—Offset 84F8h	0h
84FCh	84FFh	USB3 Port Disable Override (USB3PDO)—Offset 84FCh	0h
8500h	8503h	HW state capability register (HW_STATE_CAPABILITY)—Offset 8500h	1F40C7h
8504h	8507h	HW state register 1 (HW_STATE_REG1)—Offset 8504h	0h
8508h	850Bh	HW state register 2 (HW_STATE_REG2)—Offset 8508h	0h
850Ch	850Fh	HW state register 3 (HW_STATE_REG3)—Offset 850Ch	0h
8510h	8513h	HW state register 4 (HW_STATE_REG4)—Offset 8510h	0h
8600h	8603h	CONFIG mirror capability register (CONFIG_MIRROR_CAPABILITY)—Offset 8600h	40C2h
8604h	8605h	Command (CMD_MMIO)—Offset 8604h	0h
8606h	8607h	Device Status (STS_MMIO)—Offset 8606h	290h
8608h	8608h	Revision ID (RID_MMIO)—Offset 8608h	0h
8609h	8609h	Programming Interface (PI_MMIO)—Offset 8609h	30h
860Ah	860Ah	Sub Class Code (SCC_MMIO)—Offset 860Ah	3h
860Bh	860Bh	Base Class Code (BCC_MMIO)—Offset 860Bh	Ch
860Dh	860Dh	Master Latency Timer (MLT_MMIO)—Offset 860Dh	0h
860Eh	860Eh	Header Type (HT_MMIO)—Offset 860Eh	80h
8610h	8617h	Memory Base Address (MBAR_MMIO)—Offset 8610h	4h
862Ch	862Dh	USB Subsystem Vendor ID (SSVID_MMIO)—Offset 862Ch	0h
862Eh	862Fh	USB Subsystem ID (SSID_MMIO)—Offset 862Eh	0h
8634h	8634h	Capabilities Pointer (CAP_PTR_MMIO)—Offset 8634h	70h
863Ch	863Ch	Interrupt Line (ILINE_MMIO)—Offset 863Ch	0h
863Dh	863Dh	Interrupt Pin (IPIN_MMIO)—Offset 863Dh	0h
8640h	8643h	XHC System Bus Configuration 1 (XHCC1_MMIO)—Offset 8640h	1FDh
8644h	8647h	XHC System Bus Configuration 2 (XHCC2_MMIO)—Offset 8644h	3C000h
8650h	8653h	Clock Gating (XHCLKGTEN_MMIO)—Offset 8650h	0h
8658h	865Bh	Audio Time Synchronization (AUDSYNC_MMIO)—Offset 8658h	0h
8660h	8660h	Serial Bus Release Number (SBRN_MMIO)—Offset 8660h	30h
8661h	8661h	Frame Length Adjustment (FLADJ_MMIO)—Offset 8661h	60h
8662h	8662h	Best Effort Service Latency (BESL_MMIO)—Offset 8662h	0h
8670h	8670h	PCI Power Management Capability ID (PM_CID_MMIO)—Offset 8670h	1h
8671h	8671h	Next Item Pointer #1 (PM_NEXT_MMIO)—Offset 8671h	80h
8672h	8673h	Power Management Capabilities (PM_CAP_MMIO)—Offset 8672h	C1C2h

Table 19-1. Summary of 0_20_0_USBx MMIO Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8674h	8675h	Power Management Control/Status (PM_CS_MMIO)—Offset 8674h	8h
8680h	8680h	Message Signaled Interrupt CID (MSI_CID_MMIO)—Offset 8680h	5h
8681h	8681h	Next item pointer (MSI_NEXT_MMIO)—Offset 8681h	0h
8682h	8683h	Message Signaled Interrupt Message Control (MSI_MCTL_MMIO)—Offset 8682h	86h
8684h	8687h	Message Signaled Interrupt Message Address (MSI_MAD_MMIO)—Offset 8684h	0h
8688h	868Bh	Message Signaled Interrupt Upper Address (MSI_MUAD_MMIO)—Offset 8688h	0h
868Ch	868Dh	Message Signaled Interrupt Message Data (MSI_MD_MMIO)—Offset 868Ch	0h
8690h	8693h	Device Idle Capability (DEVIDLE_MMIO)—Offset 8690h	F0140009h
8694h	8697h	Vendor Specific Header (VSHDR_MMIO)—Offset 8694h	1400010h
8698h	869Bh	SW LTR POINTER (SWLTRPTR_MMIO)—Offset 8698h	0h
869Ch	869Fh	Device Idle Pointer Register (DEVIDLEPTR_MMIO)—Offset 869Ch	80AC1h
86A0h	86A1h	Device Idle Power ON Latency (DEVIDLEPOL_MMIO)—Offset 86A0h	800h
86A2h	86A3h	High Speed Configuration 2 (HSCFG2_MMIO)—Offset 86A4h	8h
86A4h	86A7h	High Speed Configuration 2 (HSCFG2_MMIO)—Offset 86A4h	2000h
86A8h	86ABh	XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1_MMIO)—Offset 86B0h	8Fh
86ACh	86AFh	XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1_MMIO)—Offset 86B0h	100h
86B0h	86B3h	XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1_MMIO)—Offset 86B0h	0h
86B4h	86B7h	XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM2_MMIO)—Offset 86B4h	0h
86D0h	86D3h	XHCI USB3 Overcurrent Pin Mapping 1 (U3OCM1_MMIO)—Offset 86D0h	0h
86D4h	86D7h	XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM2_MMIO)—Offset 86D4h	0h
86FCh	86FFh	XHCC3 (XHCC3_MMIO)—Offset 86FCh	2h
8700h	8703h	Debug Capability ID Register (DCID)—Offset 8700h	5100Ah
8704h	8707h	Debug Capability Doorbell Register (DCDB)—Offset 8704h	0h
8708h	870Bh	Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)—Offset 8708h	0h
8710h	8717h	Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)—Offset 8710h	0h
8718h	871Fh	Debug Capability Event Ring Dequeue Pointer Register (DCERDP)—Offset 8718h	0h
8720h	8723h	Debug Capability Control Register (DCCTRL)—Offset 8720h	0h
8724h	8727h	Debug Capability Status Register (DCST)—Offset 8724h	0h
8728h	872Bh	Debug Capability Port Status and Control Register (DCPORTSC)—Offset 8728h	80h

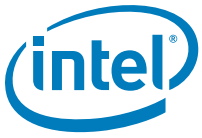


Table 19-1. Summary of 0_20_0_USBx MMIO Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8730h	8737h	Debug Capability Context Pointer Register (DCCP)—Offset 8730h	0h
8738h	873Bh	Debug Capability Device Descriptor Info Register 1 (DCDDI1)—Offset 8738h	80870000h
873Ch	873Fh	Debug Capability Device Descriptor Info Register 2 (DCDDI2)—Offset 873Ch	0h
8740h	8743h	Debug Capability Descriptor Parameters (DCDP)—Offset 8740h	30C3h
8744h	8747h	Debug Device Control ODMA (DBGDEV_CTRL_ODMA_REG)—Offset 8748h	C101105h
8748h	874Bh	Debug Device Control ODMA (DBGDEV_CTRL_ODMA_REG)—Offset 8748h	0h
874Ch	874Fh	DBC Control Register 1 (DBCCTL_REG)—Offset 8760h	0h
8750h	8753h	DBC Control Register 1 (DBCCTL_REG)—Offset 8760h	F8A8008Ch
8760h	8763h	DBC Control Register 1 (DBCCTL_REG)—Offset 8760h	0h
890Ch	890Fh	(PORT1_PROFILE_ATTRIBUTES_REG0)—Offset 890Ch	0h
8910h	8913h	(PORT1_PROFILE_ATTRIBUTES_REG1)—Offset 8910h	0h
8914h	8917h	(PORT1_PROFILE_ATTRIBUTES_REG2)—Offset 8914h	0h
8918h	891Bh	(PORT1_PROFILE_ATTRIBUTES_REG3)—Offset 8918h	0h
891Ch	891Fh	(PORT1_PROFILE_ATTRIBUTES_REG4)—Offset 891Ch	0h
8920h	8923h	(PORT1_PROFILE_ATTRIBUTES_REG5)—Offset 8920h	0h
8924h	8927h	(PORT1_PROFILE_ATTRIBUTES_REG6)—Offset 8924h	0h
8928h	892Bh	(PORT1_PROFILE_ATTRIBUTES_REG7)—Offset 8928h	0h
892Ch	892Fh	(PORT1_PROFILE_ATTRIBUTES_REG8)—Offset 892Ch	0h
8930h	8933h	(PORT1_PROFILE_ATTRIBUTES_REG9)—Offset 8930h	0h
8934h	8937h	(PORT1_PROFILE_ATTRIBUTES_REG10)—Offset 8934h	0h
8938h	893Bh	(PORT1_PROFILE_ATTRIBUTES_REG11)—Offset 8938h	0h
893Ch	893Fh	(PORT1_PROFILE_ATTRIBUTES_REG12)—Offset 893Ch	0h
8940h	8943h	(PORT1_PROFILE_ATTRIBUTES_REG13)—Offset 8940h	0h
8944h	8947h	(PORT1_PROFILE_ATTRIBUTES_REG14)—Offset 8944h	0h
8948h	894Bh	(PORT1_PROFILE_ATTRIBUTES_REG15)—Offset 8948h	0h
894Ch	894Fh	(PORT1_PROFILE_ATTRIBUTES_REG16)—Offset 894Ch	0h
8950h	8953h	(PORT1_PROFILE_ATTRIBUTES_REG17)—Offset 8950h	0h
8954h	8957h	(PORT1_PROFILE_ATTRIBUTES_REG18)—Offset 8954h	0h
8958h	895Bh	(PORT1_PROFILE_ATTRIBUTES_REG19)—Offset 8958h	0h
895Ch	895Fh	(PORT1_PROFILE_ATTRIBUTES_REG20)—Offset 895Ch	0h
8960h	8963h	(PORT1_PROFILE_ATTRIBUTES_REG21)—Offset 8960h	0h
8964h	8967h	(PORT1_PROFILE_ATTRIBUTES_REG22)—Offset 8964h	0h
8968h	896Bh	(PORT1_PROFILE_ATTRIBUTES_REG23)—Offset 8968h	0h
896Ch	896Fh	(PORT1_PROFILE_ATTRIBUTES_REG24)—Offset 896Ch	0h
8970h	8973h	(PORT1_PROFILE_ATTRIBUTES_REG25)—Offset 8970h	0h
8974h	8977h	(PORT1_PROFILE_ATTRIBUTES_REG26)—Offset 8974h	0h
8978h	897Bh	(PORT1_PROFILE_ATTRIBUTES_REG27)—Offset 8978h	0h

Table 19-1. Summary of 0_20_0_USBx MMIO Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
897Ch	897Fh	(PORT1_PROFILE_ATTRIBUTES_REG28)—Offset 897Ch	0h
8980h	8983h	(PORT1_PROFILE_ATTRIBUTES_REG29)—Offset 8980h	0h
8984h	8987h	(PORT1_PROFILE_ATTRIBUTES_REG30)—Offset 8984h	0h
8988h	898Bh	(PORT1_PROFILE_ATTRIBUTES_REG31)—Offset 8988h	0h
898Ch	898Fh	(PORT1_PROFILE_ATTRIBUTES_REG32)—Offset 898Ch	0h
8990h	8993h	(PORT1_PROFILE_ATTRIBUTES_REG33)—Offset 8990h	0h
8994h	8997h	(PORT1_PROFILE_ATTRIBUTES_REG34)—Offset 8994h	0h
8998h	899Bh	(PORT1_PROFILE_ATTRIBUTES_REG35)—Offset 8998h	0h
899Ch	899Fh	(PORT1_PROFILE_ATTRIBUTES_REG36)—Offset 899Ch	0h
89A0h	89A3h	(PORT1_PROFILE_ATTRIBUTES_REG37)—Offset 89A0h	0h
89A4h	89A7h	(PORT1_PROFILE_ATTRIBUTES_REG38)—Offset 89A4h	0h
89A8h	89ABh	(PORT1_PROFILE_ATTRIBUTES_REG39)—Offset 89A8h	0h
89ACh	89AFh	(PORT1_PROFILE_ATTRIBUTES_REG40)—Offset 89ACh	0h
89B0h	89B3h	(PORT1_PROFILE_ATTRIBUTES_REG41)—Offset 89B0h	0h
89B4h	89B7h	(PORT1_PROFILE_ATTRIBUTES_REG42)—Offset 89B4h	0h
89B8h	89BBh	(PORT1_PROFILE_ATTRIBUTES_REG43)—Offset 89B8h	0h
89BCh	89BFh	(PORT1_PROFILE_ATTRIBUTES_REG44)—Offset 89BCh	0h
89C0h	89C3h	(PORT1_PROFILE_ATTRIBUTES_REG45)—Offset 89C0h	0h
89C4h	89C7h	(PORT1_PROFILE_ATTRIBUTES_REG46)—Offset 89C4h	0h
89C8h	89CBh	(PORT1_PROFILE_ATTRIBUTES_REG47)—Offset 89C8h	0h
89CCh	89CFh	(PORT1_PROFILE_ATTRIBUTES_REG48)—Offset 89CCh	0h
89D0h	89D3h	(PORT1_PROFILE_ATTRIBUTES_REG49)—Offset 89D0h	0h
89D4h	89D7h	(PORT1_PROFILE_ATTRIBUTES_REG50)—Offset 89D4h	0h
89D8h	89DBh	(PORT1_PROFILE_ATTRIBUTES_REG51)—Offset 89D8h	0h
89DCh	89DFh	(PORT1_PROFILE_ATTRIBUTES_REG52)—Offset 89DCh	0h
89E0h	89E3h	(PORT1_PROFILE_ATTRIBUTES_REG53)—Offset 89E0h	0h
89E4h	89E7h	(PORT1_PROFILE_ATTRIBUTES_REG54)—Offset 89E4h	0h
89E8h	89EBh	(PORT1_PROFILE_ATTRIBUTES_REG55)—Offset 89E8h	0h
89ECh	89EFh	(PORT1_PROFILE_ATTRIBUTES_REG56)—Offset 89ECh	0h
89F0h	89F3h	(PORT1_PROFILE_ATTRIBUTES_REG57)—Offset 89F0h	0h
89F4h	89F7h	(PORT1_PROFILE_ATTRIBUTES_REG58)—Offset 89F4h	0h
89F8h	89FBh	(PORT1_PROFILE_ATTRIBUTES_REG59)—Offset 89F8h	0h
89FCh	89FFh	(PORT1_PROFILE_ATTRIBUTES_REG60)—Offset 89FCh	0h
8A00h	8A03h	(PORT1_PROFILE_ATTRIBUTES_REG61)—Offset 8A00h	0h
8A04h	8A07h	(PORT1_PROFILE_ATTRIBUTES_REG62)—Offset 8A04h	0h
8A08h	8A0Bh	(PORT1_PROFILE_ATTRIBUTES_REG63)—Offset 8A08h	0h
8E10h	8E13h	GLOBAL_TIME_SYNC_CAP_REG (GLOBAL_TIME_SYNC_CAP_REG)—Offset 8E10h	12C9h
8E14h	8E17h	GLOBAL_TIME_SYNC_CTRL_REG (GLOBAL_TIME_SYNC_CTRL_REG)—Offset 8E14h	0h

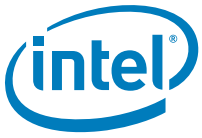


Table 19-1. Summary of 0_20_0_USBx MMIO Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8E18h	8E1Bh	MICROFRAME_TIME_REG (MICROFRAME_TIME_REG)—Offset 8E18h	0h
8E20h	8E23h	GLOBAL_TIME_LOW_REG (GLOBAL_TIME_LOW_REG)—Offset 8E20h	0h
8E24h	8E27h	GLOBAL_TIME_HI_REG (GLOBAL_TIME_HI_REG)—Offset 8E24h	0h
8E58h	8E5Bh	Debug Status Capability Register (DEBUG_STATUS_CAPABILITY_REG)—Offset 8E58h	CBh
8E5Ch	8E5Fh	Host Ctrl USB3 Soft Error Count Register 1 (HOST_CTRL_USB3_ERR_COUNT_REG1)—Offset 8E5Ch	0h
8E60h	8E63h	Host Ctrl USB3 Soft Error Count Register 2 (HOST_CTRL_USB3_ERR_COUNT_REG2)—Offset 8E60h	0h
8E64h	8E67h	Host Ctrl USB3 Soft Error Count Register 3 (HOST_CTRL_USB3_ERR_COUNT_REG3)—Offset 8E64h	0h
8E68h	8E6Bh	Host Ctrl USB3 Soft Error Count Register 4 (HOST_CTRL_USB3_ERR_COUNT_REG4)—Offset 8E68h	0h
8E6Ch	8E6Fh	Host Ctrl USB3 Soft Error Count Register 5 (HOST_CTRL_USB3_ERR_COUNT_REG5)—Offset 8E6Ch	0h
8E70h	8E73h	Host Ctrl USB3 Soft Error Count Register 6 (HOST_CTRL_USB3_ERR_COUNT_REG6)—Offset 8E70h	0h
8E74h	8E77h	Host Ctrl USB3 Soft Error Count Register 7 (HOST_CTRL_USB3_ERR_COUNT_REG7)—Offset 8E74h	0h
0h		IOSFCTL - Control Register (IOSFCTL)—Offset 0h	Fh
1D0h		Power Management Control Register (PMCTL)—Offset 1D0h	0h
200h		PCI Configuration Control 1 Register (PCICFGCTR1)—Offset 200h	100h
4001h		c73usb280_USB2 PER PORT (USB2_PER_PORT_PP0)—Offset 4100h	5DA81h
402Bh		GLB ADP VBUS COMP REG (GLB_ADP_VBUS_COMP_REG)—Offset 402Bh	0h
402Ch		c73usb280_USB2 GLOBAL PORT 2 (USB2_GLOBAL_PORT_2)—Offset 402Ch	0h
7F04h		c73usb280_USB2 COMPBG (USB2_COMPBG)—Offset 7F04h	600h
7014h		CONFIG_3—Offset 7014h	0h
1Ch		DBC_GP2_IN_PAYLOAD_BP_LOW—Offset 1Ch	0h
20h		DBC_GP2_IN_PAYLOAD_BP_HI—Offset 20h	0h
24h		DBC_GP2_IN_PAYLOAD_QUALIFIERS—Offset 24h	0h
34h		DBC_GP2_IN_STATUS_QUALIFIERS—Offset 34h	0h
2Ch		DBC_GP2_IN_STATUS_BP_LOW—Offset 2Ch	0h
30h		DBC_GP2_IN_STATUS_BP_HI—Offset 30h	0h
00A8h		Super Speed Configuration 1 (SSCFG1) —Offset 00A8h	8Fh
00ACh		High Speed Configuration 1 (HSCFG1) —Offset 00ACh	100h
00BCh		GEN_REGRW4 —Offset 00BCh	0h

19.1.1 Capability Registers Length (CAPLENGTH)—Offset 0h

This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Capability Registers Length (CAPLENGTH)**

19.1.2 Host Controller Interface Version Number (HCIVERSION)—Offset 2h

This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
15:0	100h RW/L	**Host Controller Interface Version Number (HCIVERSION)**

19.1.3 Structural Parameters 1 (HCSPARAMS1)—Offset 4h

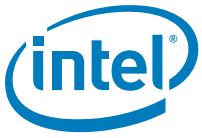
This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: F000820h

Bit Range	Default & Access	Field Name (ID): Description
31:24	Fh RW/L	**Number of Ports (MaxPorts)**
23:19	0h RW/L	**Rsvd1 (Rsvd1)**
18:8	8h RW/L	**Number of Interrupters (MaxIntrs)**
7:0	20h RW/L	**Number of Device Slots (MaxSlots)**



19.1.4 Structural Parameters 2 (HCSPARAMS2)—Offset 8h

This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 94000054h

Bit Range	Default & Access	Field Name (ID): Description
31:27	12h RW/L	**Max Scratchpad Buffers LO (MaxScratchpadBufs)**
26	1h RW/L	**Scratchpad Restore (SPR)**
25:21	0h RW/L	**Max Scratchpad Buffers HI (MaxScratchpadBufs_HI)**
20:8	0h RW/L	**Rsvd1 (Rsvd1)**
7:4	5h RW/L	**Event Ring Segment Table Max (ERSTMax)**
3:0	4h RW/L	**Isochronous Scheduling Threshold (IST)**

19.1.5 Structural Parameters 3 (HCSPARAMS3)—Offset Ch

This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40001h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4h RW/L	**U2 Device Exit Latency (U2DEL)**
15:8	0h RW/L	**Rsvd1 (Rsvd1)**
7:0	1h RW/L	**U1 Device Exit Latency (U1DEL)**

19.1.6 Capability Parameters (HCCPARAMS)—Offset 10h

This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 200077C1h

Bit Range	Default & Access	Field Name (ID): Description
31:16	2000h RW/L	**xHCI Extended Capabilities Pointer (xECP)**
15:12	7h RW/L	**Maximum Primary Stream Array Size (MaxPSASize)**
11	0h RW/L	**Contiguous Frame ID Capability (CFC)**
10	1h RW/L	**Stopped EDLTA Capabilty (SEC)**
9	1h RW/L	**Stopped - Short Packet Capability (SPC)**
8	1h RW/L	**Parst All Event Data (PAE)**
7	1h RW/L	**No Secondary SID Support (NSS)**
6	1h RW/L	**Latency Tolerance Messaging Capability (LTC)**
5	0h RW/L	**Light HC Reset Capability (LHRC)**
4	0h RW/L	**Port Indicators (PIND)**
3	0h RW/L	**Port Power Control (PPC)**
2	0h RW/L	**Context Size (CSZ)**
1	0h RW/L	**BW Negotiation Capability (BNC)**
0	1h RW/L	**64-bit Addressing Capability (AC64)**

19.1.7 Doorbell Offset (DBOFF)—Offset 14h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	C00h RO	**Doorbell Array Offset (DBAO)**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	**Rsvd1 (Rsvd1)**

19.1.8 Runtime Register Space Offset (RTSOFF)—Offset 18h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	100h RO	**Runtime Register Space Offset (RTRSO)**
4:0	0h RO	**Rsvd1 (Rsvd1)**

19.1.9 USB Command (USBCMD)—Offset 80h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Rsvd2 (Rsvd2)**
11	0h RW	**Enable U3 MFINDEX Stop (EU3S)**
10	0h RW	**Enable Wrap Event (EWE)**
9	0h RW	**Controller Restore State (CRS)**
8	0h RW	**Controller Save State (CSS)**
7	0h RW	**Light Host Controller Reset (LHCRST)**
6:4	0h RO	**Rsvd1 (Rsvd1)**
3	0h RW	**Host System Error Enable (HSEE)**
2	0h RW	**Interrupter Enable (INTE)**

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Host Controller Reset (HCRST)**
0	0h RW	**Run/Stop (RS)**

19.1.10 USB Status (USBSTS)—Offset 84h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Rsvd3 (Rsvd3)**
12	0h RO	**Host Controller Error (HCE):** This bit is not preset in HC, this is deviation from XHCI 1.0 spec.
11	0h RO	**Controller Not Ready (CNR):** This is deviation from XHCI 1.0 spec.
10	0h RW/C	**Save/Restore Error (SRE)**
9	0h RO	**Restore State Status (RSS)**
8	0h RO	**Save State Status (SSS)**
7:5	0h RO	**Rsvd2 (Rsvd2)**
4	0h RW/C	**Port Change Detect (PCD)**
3	0h RW/C	**Event Interrupt (EINT)**
2	0h RW/C	**Host System Error (HSE)**
1	0h RO	**Rsvd1 (Rsvd1)**
0	1h RO	**HCHalted (HCH)**

19.1.11 Page Size (PAGESIZE)—Offset 88h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	1h RO	**Page Size (PAGESIZE)**

19.1.12 Device Notification Control (DNCTRL)—Offset 94h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RW	**Notification Enable (N0_N15)**

19.1.13 Command Ring Low (CRCR_LO)—Offset 98h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Command Ring Pointer (CRP)**
5:4	0h RO	**Rsvd1 (Rsvd1)**
3	0h RO	**Command Ring Running (CRR)**
2	0h RW/1S	**Command Abort (CA)**
1	0h RW/1S	**Command Stop (CS)**
0	0h RW	**Ring Cycle State (RCS)**

19.1.14 Command Ring High (CRCR_HI)—Offset 9Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Command Ring Pointer (CRP)**

19.1.15 Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Device Context Base Address Array Pointer (DCBAAP)**
5:0	0h RO	**Rsvd1 (Rsvd1)**

19.1.16 Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Device Context Base Address Array Pointer (DCBAAP)**

19.1.17 Configure (CONFIG)—Offset B8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**Max Device Slots Enabled (MaxSlotsEn)**

19.1.18 Port Status and Control USB2 (PORTSC1)—Offset 480h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.19 Port Power Management Status and Control USB2 (PORTPMSC1)—Offset 484h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27:17	0h RO	**Rsvd1 (Rsvd1)**
16	0h RW	**Hardware LPM Enable (HLE)**
15:8	0h RW	**Device Address (DA):** Note: This register is sticky.
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0h RW	**Remote Wake Enable (RWE):** Note: This register is sticky.

Bit Range	Default & Access	Field Name (ID): Description
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

19.1.20 Port X Hardware LPM Control Register (PORTHLPMC1)—Offset 48Ch

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**RESERVED (RSVD)**
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	0h RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

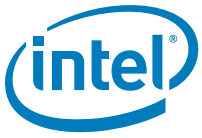
19.1.21 Port Status and Control USB2 (PORTSC2)—Offset 490h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.



Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.22 Port Power Management Status and Control USB2 (PORTPMSC2)—Offset 494h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27:17	0h RO	**Rsvd1 (Rsvd1)**
16	0h RW	**Hardware LPM Enable (HLE)**
15:8	0h RW	**Device Address (DA):** Note: This register is sticky.
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0h RW	**Remote Wake Enable (RWE):** Note: This register is sticky.
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

19.1.23 Port X Hardware LPM Control Register (PORTHLPMC2)—Offset 49Ch

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**RESERVED (RSVD)**
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	0h RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

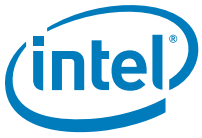
19.1.24 Port Status and Control USB2 (PORTSC3)—Offset 4A0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.



Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.25 Port Power Management Status and Control USB2 (PORTPMSC3)—Offset 4A4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27:17	0h RO	**Rsvd1 (Rsvd1)**

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Hardware LPM Enable (HLE)**
15:8	0h RW	**Device Address (DA):** Note: This register is sticky.
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0h RW	**Remote Wake Enable (RWE):** Note: This register is sticky.
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

19.1.26 Port X Hardware LPM Control Register (PORTHLPMC3)—Offset 4ACh

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**RESERVED (RSVD)**
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	0h RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

19.1.27 Port Status and Control USB2 (PORTSC4)—Offset 4B0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.28 Port Power Management Status and Control USB2 (PORTPMSC4)—Offset 4B4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27:17	0h RO	**Rsvd1 (Rsvd1)**
16	0h RW	**Hardware LPM Enable (HLE)**
15:8	0h RW	**Device Address (DA):** Note: This register is sticky.
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0h RW	**Remote Wake Enable (RWE):** Note: This register is sticky.
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

19.1.29 Port X Hardware LPM Control Register (PORTHLPMC4)—Offset 4BCh

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**RESERVED (RSVD)**
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	0h RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

19.1.30 Port Status and Control USB2 (PORTSC5)—Offset 4C0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.31 Port Power Management Status and Control USB2 (PORTPMSC5)—Offset 4C4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27:17	0h RO	**Rsvd1 (Rsvd1)**
16	0h RW	**Hardware LPM Enable (HLE)**
15:8	0h RW	**Device Address (DA):** Note: This register is sticky.
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0h RW	**Remote Wake Enable (RWE):** Note: This register is sticky.
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

19.1.32 Port X Hardware LPM Control Register (PORTHLPMC5)—Offset 4CCh

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters necessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**RESERVED (RSVD)**
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	0h RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

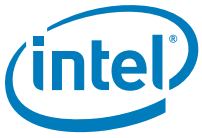
19.1.33 Port Status and Control USB2 (PORTSC6)—Offset 4D0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**



Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.34 Port Power Management Status and Control USB2 (PORTPMSC6)—Offset 4D4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27:17	0h RO	**Rsvd1 (Rsvd1)**
16	0h RW	**Hardware LPM Enable (HLE)**
15:8	0h RW	**Device Address (DA):** Note: This register is sticky.
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0h RW	**Remote Wake Enable (RWE):** Note: This register is sticky.
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

19.1.35 Port X Hardware LPM Control Register (PORTHLPMC6)—Offset 4DCh

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**RESERVED (RSVD)**
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	0h RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

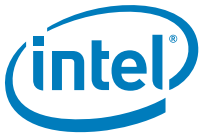
19.1.36 Port Status and Control USB2 (PORTSC7)—Offset 4E0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**



Bit Range	Default & Access	Field Name (ID): Description
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.37 Port Power Management Status and Control USB2 (PORTPMSC7)—Offset 4E4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27:17	0h RO	**Rsvd1 (Rsvd1)**
16	0h RW	**Hardware LPM Enable (HLE)**
15:8	0h RW	**Device Address (DA):** Note: This register is sticky.
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0h RW	**Remote Wake Enable (RWE):** Note: This register is sticky.
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

19.1.38 Port X Hardware LPM Control Register (PORTHLPMC7)—Offset 4ECh

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**RESERVED (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	0h RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

19.1.39 Port Status and Control USB2 (PORTSC8)—Offset 4F0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.40 Port Power Management Status and Control USB2 (PORTPMSC8)—Offset 4F4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27:17	0h RO	**Rsvd1 (Rsvd1)**
16	0h RW	**Hardware LPM Enable (HLE)**

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Device Address (DA):** Note: This register is sticky.
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0h RW	**Remote Wake Enable (RWE):** Note: This register is sticky.
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

19.1.41 Port X Hardware LPM Control Register (PORTHLPMC8)—Offset 4FCh

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**RESERVED (RSVD)**
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	0h RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

19.1.42 Port Status and Control USB3 (PORTSC9)—Offset 500h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.43 Port Power Management Status and Control USB3 (PORTPMSC9)—Offset 504h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved (RSVD)**
16	0h RW	**Force Link PM Accept (FLA)**
15:8	0h RW/S	**U2 Timeout (U2T)**
7:0	0h RW/S	**U1 Timeout (U1T)**

19.1.44 USB3 Port Link Info (PORTLI9)—Offset 508h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RO	**Link Error Count (LEC)**

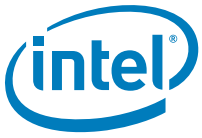
19.1.45 Port Status and Control USB3 (PORTSC10)—Offset 510h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.



Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.46 Port Power Management Status and Control USB3 (PORTPMSC10)—Offset 514h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved (RSVD)**
16	0h RW	**Force Link PM Accept (FLA)**
15:8	0h RW/S	**U2 Timeout (U2T)**
7:0	0h RW/S	**U1 Timeout (U1T)**

19.1.47 USB3 Port Link Info (PORTLI10)—Offset 518h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RO	**Link Error Count (LEC)**

19.1.48 Port Status and Control USB3 (PORTSC11)—Offset 520h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.49 Port Power Management Status and Control USB3 (PORTPMSC11)—Offset 524h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved (RSVD)**
16	0h RW	**Force Link PM Accept (FLA)**
15:8	0h RW/S	**U2 Timeout (U2T)**
7:0	0h RW/S	**U1 Timeout (U1T)**

19.1.50 USB3 Port Link Info (PORTLI11)—Offset 528h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RO	**Link Error Count (LEC)**

19.1.51 Port Status and Control USB3 (PORTSC12)—Offset 530h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.52 Port Power Management Status and Control USB3 (PORTPMSC12)—Offset 534h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved (RSVD)**
16	0h RW	**Force Link PM Accept (FLA)**
15:8	0h RW/S	**U2 Timeout (U2T)**
7:0	0h RW/S	**U1 Timeout (U1T)**

19.1.53 USB3 Port Link Info (PORTLI12)—Offset 538h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RO	**Link Error Count (LEC)**

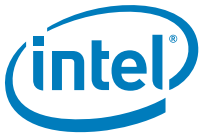
19.1.54 Port Status and Control USB3 (PORTSC13)—Offset 540h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.



Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.55 Port Power Management Status and Control USB3 (PORTPMSC13)—Offset 544h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved (RSVD)**
16	0h RW	**Force Link PM Accept (FLA)**
15:8	0h RW/S	**U2 Timeout (U2T)**
7:0	0h RW/S	**U1 Timeout (U1T)**

19.1.56 USB3 Port Link Info (PORTLI13)—Offset 548h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RO	**Link Error Count (LEC)**

19.1.57 Port Status and Control USB3 (PORTSC14)—Offset 550h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.58 Port Power Management Status and Control USB3 (PORTPMSC14)—Offset 554h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved (RSVD)**
16	0h RW	**Force Link PM Accept (FLA)**
15:8	0h RW/S	**U2 Timeout (U2T)**
7:0	0h RW/S	**U1 Timeout (U1T)**

19.1.59 USB3 Port Link Info (PORTLI14)—Offset 558h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RO	**Link Error Count (LEC)**

19.1.60 Port Status and Control USB3 (PORTSC15)—Offset 560h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	**Rsvd2 (Rsvd2)**
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PortSpeed):** Note: This register is sticky.
9	1h RW	**Port Power (PP):** Note: This register is sticky.
8:5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0h RW/1S	**Port Reset (PR)**
3	0h RW	**Over-current Active (OCA):** Note: This register is sticky.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0h RW	**Current Connect Status (CCS):** Note: This register is sticky.

19.1.61 Port Power Management Status and Control USB3 (PORTPMSC15)—Offset 564h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	**Reserved (RSVD)**
16	0h RW	**Force Link PM Accept (FLA)**
15:8	0h RW/S	**U2 Timeout (U2T)**
7:0	0h RW/S	**U1 Timeout (U1T)**

19.1.62 USB3 Port Link Info (PORTLI15)—Offset 568h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RO	**Link Error Count (LEC)**

19.1.63 Microframe Index (RTMFINDEX)—Offset 2000h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Rsvd1 (Rsvd1)**
13:0	0h RO	**Microframe Index (IMAN0)**

19.1.64 Interrupter 1 Management (IMAN0)—Offset 2020h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW	**Interrupt Enable (IE)**
0	0h RW/C	**Interrupt Pending (IP)**

19.1.65 Interrupter 1 Moderation (IMOD0)—Offset 2024h

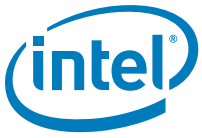
There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Interrupt Moderation Counter (IMODC)**
15:0	FA0h RW	**Interrupt Moderation Interval (IMODI)**



19.1.66 Event Ring Segment Table Size 1 (ERSTSZ0)—Offset 2028h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RW	**Event Ring Segment Table Size (ERSTS)**

19.1.67 Event Ring Segment Table Base Address Low 1 (ERSTBA_LO0)—Offset 2030h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Event Ring Segment Table Base Address Register (ERSTBA)**
5:0	0h RO	**Rsvd1 (Rsvd1)**

19.1.68 Event Ring Segment Table Base Address High 1 (ERSTBA_HI0)—Offset 2034h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Segment Table Base Address (ERSTBA)**

19.1.69 Event Ring Dequeue Pointer Low 1 (ERDP_LO0)—Offset 2038h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RW	**Event Ring Dequeue Pointer (ERDP)**
3	0h RW/C	**Event Handler Busy (EHB)**
2:0	0h RW	**Dequeue ERST Segment Index (DESI)**

19.1.70 Event Ring Dequeue Pointer High 1 (ERDP_HI0)—Offset 203Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Dequeue Pointer (ERDP)**

19.1.71 Interrupter 2 Management (IMAN1)—Offset 2040h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW	**Interrupt Enable (IE)**
0	0h RW/C	**Interrupt Pending (IP)**

19.1.72 Interrupter 2 Moderation (IMOD1)—Offset 2044h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Interrupt Moderation Counter (IMODC)**
15:0	FA0h RW	**Interrupt Moderation Interval (IMODI)**

19.1.73 Event Ring Segment Table Size 2 (ERSTSZ1)—Offset 2048h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RW	**Event Ring Segment Table Size (ERSTS)**

19.1.74 Event Ring Segment Table Base Address Low 2 (ERSTBA_LO1)—Offset 2050h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Event Ring Segment Table Base Address Register (ERSTBA)**
5:0	0h RO	**Rsvd1 (Rsvd1)**

19.1.75 Event Ring Segment Table Base Address High 2 (ERSTBA_HI1)—Offset 2054h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Segment Table Base Address (ERSTBA)**

19.1.76 Event Ring Dequeue Pointer Low 2 (ERDP_LO1)—Offset 2058h

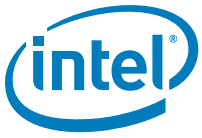
There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RW	**Event Ring Dequeue Pointer (ERDP)**
3	0h RW/C	**Event Handler Busy (EHB)**
2:0	0h RW	**Dequeue ERST Segment Index (DESI)**



19.1.77 Event Ring Dequeue Pointer High 2 (ERDP_HI1)—Offset 205Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Dequeue Pointer (ERDP)**

19.1.78 Interrupter 3 Management (IMAN2)—Offset 2060h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW	**Interrupt Enable (IE)**
0	0h RW/C	**Interrupt Pending (IP)**

19.1.79 Interrupter 3 Moderation (IMOD2)—Offset 2064h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Interrupt Moderation Counter (IMODC)**

Bit Range	Default & Access	Field Name (ID): Description
15:0	FA0h RW	**Interrupt Moderation Interval (IMODI)**

19.1.80 Event Ring Segment Table Size 3 (ERSTSZ2)—Offset 2068h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RW	**Event Ring Segment Table Size (ERSTS)**

19.1.81 Event Ring Segment Table Base Address Low 3 (ERSTBA_LO2)—Offset 2070h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Event Ring Segment Table Base Address Register (ERSTBA)**
5:0	0h RO	**Rsvd1 (Rsvd1)**

19.1.82 Event Ring Segment Table Base Address High 3 (ERSTBA_HI2)—Offset 2074h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Segment Table Base Address (ERSTBA)**

19.1.83 Event Ring Dequeue Pointer Low 3 (ERDP_LO2)—Offset 2078h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RW	**Event Ring Dequeue Pointer (ERDP)**
3	0h RW/C	**Event Handler Busy (EHB)**
2:0	0h RW	**Dequeue ERST Segment Index (DESI)**

19.1.84 Event Ring Dequeue Pointer High 3 (ERDP_HI2)—Offset 207Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Dequeue Pointer (ERDP)**

19.1.85 Interrupter 4 Management (IMAN3)—Offset 2080h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW	**Interrupt Enable (IE)**
0	0h RW/C	**Interrupt Pending (IP)**

19.1.86 Interrupter 4 Moderation (IMOD3)—Offset 2084h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Interrupt Moderation Counter (IMODC)**
15:0	FA0h RW	**Interrupt Moderation Interval (IMODI)**

19.1.87 Event Ring Segment Table Size 4 (ERSTSZ3)—Offset 2088h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

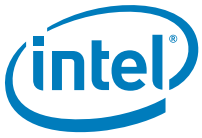
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RW	**Event Ring Segment Table Size (ERSTS)**

19.1.88 Event Ring Segment Table Base Address Low 4 (ERSTBA_LO3)—Offset 2090h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Event Ring Segment Table Base Address Register (ERSTBA)**
5:0	0h RO	**Rsvd1 (Rsvd1)**

19.1.89 Event Ring Segment Table Base Address High 4 (ERSTBA_HI3)—Offset 2094h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Segment Table Base Address (ERSTBA)**

19.1.90 Event Ring Dequeue Pointer Low 4 (ERDP_LO3)—Offset 2098h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RW	**Event Ring Dequeue Pointer (ERDP)**
3	0h RW/C	**Event Handler Busy (EHB)**
2:0	0h RW	**Dequeue ERST Segment Index (DESI)**

19.1.91 Event Ring Dequeue Pointer High 4 (ERDP_HI3)—Offset 209Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Dequeue Pointer (ERDP)**

19.1.92 Interrupter 5 Management (IMAN4)—Offset 20A0h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW	**Interrupt Enable (IE)**
0	0h RW/C	**Interrupt Pending (IP)**

19.1.93 Interrupter 5 Moderation (IMOD4)—Offset 20A4h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Interrupt Moderation Counter (IMODC)**

Bit Range	Default & Access	Field Name (ID): Description
15:0	FA0h RW	**Interrupt Moderation Interval (IMODI)**

19.1.94 Event Ring Segment Table Size 5 (ERSTSZ4)—Offset 20A8h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RW	**Event Ring Segment Table Size (ERSTS)**

19.1.95 Event Ring Segment Table Base Address Low 5 (ERSTBA_LO4)—Offset 20B0h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Event Ring Segment Table Base Address Register (ERSTBA)**
5:0	0h RO	**Rsvd1 (Rsvd1)**

19.1.96 Event Ring Segment Table Base Address High 5 (ERSTBA_HI4)—Offset 20B4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Segment Table Base Address (ERSTBA)**

19.1.97 Event Ring Dequeue Pointer Low 5 (ERDP_LO4)—Offset 20B8h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RW	**Event Ring Dequeue Pointer (ERDP)**
3	0h RW/C	**Event Handler Busy (EHB)**
2:0	0h RW	**Dequeue ERST Segment Index (DESI)**

19.1.98 Event Ring Dequeue Pointer High 5 (ERDP_HI4)—Offset 20BCh

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Dequeue Pointer (ERDP)**

19.1.99 Interrupter 6 Management (IMAN5)—Offset 20C0h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW	**Interrupt Enable (IE)**
0	0h RW/C	**Interrupt Pending (IP)**

19.1.100 Interrupter 6 Moderation (IMOD5)—Offset 20C4h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Interrupt Moderation Counter (IMODC)**
15:0	FA0h RW	**Interrupt Moderation Interval (IMODI)**

19.1.101 Event Ring Segment Table Size 6 (ERSTSZ5)—Offset 20C8h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RW	**Event Ring Segment Table Size (ERSTS)**

19.1.102 Event Ring Segment Table Base Address Low 6 (ERSTBA_LO5)—Offset 20D0h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Event Ring Segment Table Base Address Register (ERSTBA)**
5:0	0h RO	**Rsvd1 (Rsvd1)**

19.1.103 Event Ring Segment Table Base Address High 6 (ERSTBA_HI5)—Offset 20D4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Segment Table Base Address (ERSTBA)**

19.1.104 Event Ring Dequeue Pointer Low 6 (ERDP_LO5)—Offset 20D8h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RW	**Event Ring Dequeue Pointer (ERDP)**

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/C	**Event Handler Busy (EHB)**
2:0	0h RW	**Dequeue ERST Segment Index (DESI)**

19.1.105 Event Ring Dequeue Pointer High 6 (ERDP_HI5)—Offset 20DCh

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Dequeue Pointer (ERDP)**

19.1.106 Interrupter 7 Management (IMAN6)—Offset 20E0h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW	**Interrupt Enable (IE)**
0	0h RW/C	**Interrupt Pending (IP)**

19.1.107 Interrupter 7 Moderation (IMOD6)—Offset 20E4h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Interrupt Moderation Counter (IMODC)**
15:0	FA0h RW	**Interrupt Moderation Interval (IMODI)**

19.1.108 Event Ring Segment Table Size 7 (ERSTSZ6)—Offset 20E8h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RW	**Event Ring Segment Table Size (ERSTS)**

19.1.109 Event Ring Segment Table Base Address Low 7 (ERSTBA_LO6)—Offset 20F0h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Event Ring Segment Table Base Address Register (ERSTBA)**
5:0	0h RO	**Rsvd1 (Rsvd1)**

19.1.110 Event Ring Segment Table Base Address High 7 (ERSTBA_HI6)—Offset 20F4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Segment Table Base Address (ERSTBA)**

19.1.111 Event Ring Dequeue Pointer Low 7 (ERDP_LO6)—Offset 20F8h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RW	**Event Ring Dequeue Pointer (ERDP)**
3	0h RW/C	**Event Handler Busy (EHB)**
2:0	0h RW	**Dequeue ERST Segment Index (DESI)**

19.1.112 Event Ring Dequeue Pointer High 7 (ERDP_HI6)—Offset 20FCh

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Dequeue Pointer (ERDP)**

19.1.113 Interrupter 8 Management (IMAN7)—Offset 2100h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Rsvd1 (Rsvd1)**
1	0h RW	**Interrupt Enable (IE)**
0	0h RW/C	**Interrupt Pending (IP)**

19.1.114 Interrupter 8 Moderation (IMOD7)—Offset 2104h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FA0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Interrupt Moderation Counter (IMODC)**
15:0	FA0h RW	**Interrupt Moderation Interval (IMODI)**

19.1.115 Event Ring Segment Table Size 8 (ERSTSZ7)—Offset 2108h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd1 (Rsvd1)**
15:0	0h RW	**Event Ring Segment Table Size (ERSTS)**

19.1.116 Event Ring Segment Table Base Address Low 8 (ERSTBA_LO7)—Offset 2110h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Event Ring Segment Table Base Address Register (ERSTBA)**
5:0	0h RO	**Rsvd1 (Rsvd1)**

19.1.117 Event Ring Segment Table Base Address High 8 (ERSTBA_HI7)—Offset 2114h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Segment Table Base Address (ERSTBA)**

19.1.118 Event Ring Dequeue Pointer Low 8 (ERDP_LO7)—Offset 2118h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RW	**Event Ring Dequeue Pointer (ERDP)**
3	0h RW/C	**Event Handler Busy (EHB)**
2:0	0h RW	**Dequeue ERST Segment Index (DESI)**

19.1.119 Event Ring Dequeue Pointer High 8 (ERDP_HI7)—Offset 211Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Dequeue Pointer (ERDP)**

19.1.120 Door Bell 1 (DB0)—Offset 3000h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.121 Door Bell 2 (DB1)—Offset 3004h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.122 Door Bell 3 (DB2)—Offset 3008h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.123 Door Bell 4 (DB3)—Offset 300Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.124 Door Bell 5 (DB4)—Offset 3010h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.125 Door Bell 6 (DB5)—Offset 3014h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**DB Target (DT)**

19.1.126 Door Bell 7 (DB6)—Offset 3018h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.127 Door Bell 8 (DB7)—Offset 301Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.128 Door Bell 9 (DB8)—Offset 3020h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.129 Door Bell 10 (DB9)—Offset 3024h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.130 Door Bell 11 (DB10)—Offset 3028h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.131 Door Bell 12 (DB11)—Offset 302Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.132 Door Bell 13 (DB12)—Offset 3030h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.133 Door Bell 14 (DB13)—Offset 3034h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.134 Door Bell 15 (DB14)—Offset 3038h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.135 Door Bell 16 (DB15)—Offset 303Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.136 Door Bell 17 (DB16)—Offset 3040h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.137 Door Bell 18 (DB17)—Offset 3044h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**DB Target (DT)**

19.1.138 Door Bell 19 (DB18)—Offset 3048h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.139 Door Bell 20 (DB19)—Offset 304Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

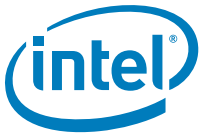
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.140 Door Bell 21 (DB20)—Offset 3050h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.141 Door Bell 22 (DB21)—Offset 3054h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.142 Door Bell 23 (DB22)—Offset 3058h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.143 Door Bell 24 (DB23)—Offset 305Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.144 Door Bell 25 (DB24)—Offset 3060h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.145 Door Bell 26 (DB25)—Offset 3064h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.146 Door Bell 27 (DB26)—Offset 3068h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.147 Door Bell 28 (DB27)—Offset 306Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.148 Door Bell 29 (DB28)—Offset 3070h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.149 Door Bell 30 (DB29)—Offset 3074h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**DB Target (DT)**

19.1.150 Door Bell 31 (DB30)—Offset 3078h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.151 Door Bell 32 (DB31)—Offset 307Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.152 Door Bell 32 (DB32)—Offset 3080h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI)**
15:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW	**DB Target (DT)**

19.1.153 XECP_SUPP_USB2_0 (XECP_SUPP_USB2_0)—Offset 8000h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2000802h

Bit Range	Default & Access	Field Name (ID): Description
31:24	2h RO	**USB Major Revision: 2.0 (USB2_MAJ_REV)**
23:16	0h RO	**USB Minor Revision (USB_MIN_REV)**
15:8	8h RO	**Next Capability Pointer (NCP)**
7:0	2h RO	**Supported Protocol ID (SPID)**

19.1.154 XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1)—Offset 8004h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 20425355h

Bit Range	Default & Access	Field Name (ID): Description
31:0	20425355h RO	**XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1):** Namestring USB

19.1.155 XECP_SUPP_USB2_2 (XECP_SUPP_USB2_2)—Offset 8008h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 30190801h

Bit Range	Default & Access	Field Name (ID): Description
31:28	3h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 3 USB 2.0 Speed (High, Full, Low)
27:21	0h RO	**Rsvd0 (Rsvd0)**
20	1h RW/L	**BESL LPM Capability (BLC):** Bit is set to 1 to indicate that the the ports described by this xHCI Supported Protocol Capability will apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMCC registers.
19	1h RW/L	**Protocol Defined - Hardware LMP Capability (HLC)**
18	0h RO	**Protocol Defined - Integrated Hub Implementation (IHI)**
17	0h RO	**Protocol Defined - High SPeed Only (HSO)**
16	1h RO	**Reserved (RSVD)**
15:8	8h RO	**Compatible Port Count (CPC)**
7:0	1h RO	**Compatible Port Offset (CPO)**

19.1.156 XECP_SUPP_USB2_3 (Full Speed) (XECP_SUPP_USB2_3)—Offset 8010h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: C0021h

Bit Range	Default & Access	Field Name (ID): Description
31:16	Ch RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	**Rsvd0 (Rsvd0)**
8	0h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	1h RO	**Protocol Speed ID Value (PSIV)**

19.1.157 XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_4)—Offset 8014h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 5DC0012h

Bit Range	Default & Access	Field Name (ID): Description
31:16	5DCh RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	**Rsvd0 (Rsvd0)**
8	0h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	1h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	2h RO	**Protocol Speed ID Value (PSIV)**

19.1.158 XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_5)—Offset 8018h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1E00023h

Bit Range	Default & Access	Field Name (ID): Description
31:16	1E0h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	**Rsvd0 (Rsvd0)**
8	0h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	3h RO	**Protocol Speed ID Value (PSIV)**

19.1.159 XECP_SUPP_USB3_0 (XECP_SUPP_USB3_0)—Offset 8020h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3001402h

Bit Range	Default & Access	Field Name (ID): Description
31:24	3h RO	**USB Major Revision: 3.0 (USB3_MAJ_REV)**
23:16	0h RO	**USB Minor Revision (USB_MIN_REV)**
15:8	14h RO	**Next Capability Pointer (NCP)**
7:0	2h RO	**Supported Protocol ID (SPID)**

19.1.160 XECP_SUPP_USB3_1 (XECP_SUPP_USB3_1)—Offset 8024h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 20425355h

Bit Range	Default & Access	Field Name (ID): Description
31:0	20425355h RO	**XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1):** Namestring USB

19.1.161 XECP_SUPP_USB3_2 (XECP_SUPP_USB3_2)—Offset 8028h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 30000709h

Bit Range	Default & Access	Field Name (ID): Description
31:28	3h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 1 USB 3.0 Speed (Supper Speed)
27:16	0h RO	**Rsvd0 (Rsvd0)**
15:8	7h RO	**Compatible Port Count (CPC)**
7:0	9h RO	**Compatible Port Offset (CPO)**

19.1.162 XECP_SUPP_USB3_3 (XECP_SUPP_USB3_3)—Offset 8030h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4E00121h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4E0h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	**Rsvd0 (Rsvd0)**
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**

Bit Range	Default & Access	Field Name (ID): Description
3:0	1h RO	**Protocol Speed ID Value (PSIV)**

19.1.163 XECP_SUPP_USB3_4 (XECP_SUPP_USB3_4)—Offset 8034h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 9C00122h

Bit Range	Default & Access	Field Name (ID): Description
31:16	9C0h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	**Rsvd0 (Rsvd0)**
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	2h RO	**Protocol Speed ID Value (PSIV)**

19.1.164 XECP_SUPP_USB3_5 (XECP_SUPP_USB3_5)—Offset 8038h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 13800123h

Bit Range	Default & Access	Field Name (ID): Description
31:16	1380h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	**Rsvd0 (Rsvd0)**
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**

Bit Range	Default & Access	Field Name (ID): Description
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	3h RO	**Protocol Speed ID Value (PSIV)**

19.1.165 XECP_SUPP_USB3_6 (XECP_SUPP_USB3_6)—Offset 803Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 50134h

Bit Range	Default & Access	Field Name (ID): Description
31:16	5h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	**Rsvd0 (Rsvd0)**
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	3h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	4h RO	**Protocol Speed ID Value (PSIV)**

19.1.166 XECP_SUPP_USB3_7 (XECP_SUPP_USB3_7)—Offset 8040h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 5B10125h

Bit Range	Default & Access	Field Name (ID): Description
31:16	5B1h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	**Rsvd0 (Rsvd0)**
8	1h RO	**PSI Full Duplex (PFD)**

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	5h RO	**Protocol Speed ID Value (PSIV)**

19.1.167 XECP_SUPP_USB3_8 (XECP_SUPP_USB3_8)—Offset 8044h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: B630126h

Bit Range	Default & Access	Field Name (ID): Description
31:16	B63h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	**Rsvd0 (Rsvd0)**
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	6h RO	**Protocol Speed ID Value (PSIV)**

19.1.168 XECP_SUPP_USB3_9 (XECP_SUPP_USB3_9)—Offset 8048h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 16C60127h

Bit Range	Default & Access	Field Name (ID): Description
31:16	16C6h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	**Rsvd0 (Rsvd0)**

Bit Range	Default & Access	Field Name (ID): Description
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	7h RO	**Protocol Speed ID Value (PSIV)**

19.1.169 Host Controller Capability (HOST_CTRL_CAP_REG)—Offset 8070h

This is a register that describe the host controller the extended cap location. It includes the , XECP_HOST_NEXT_CAP_OFFSET and VEND_DEF_HOST_CAP_ID_192. This register is not subject to HW save and restore.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4DFFC0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD)**
23:16	4Dh RW/L	**Valid Length (VALID_LENGTH):** Indicates the number of valid DWords in the capability, that need to be saved and restored. 47h -> 818Bh is the last valid byte
15:8	FFh RW/L	**Next Capability Pointer (XECP_HOST_NEXT_CAP_OFFSET)**
7:0	C0h RW/L	**Supported Protocol ID (VEND_DEF_HOST_CAP_ID)**

19.1.170 Override EP Flow Control (HOST_CLR_MASK_REG)—Offset 8078h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**RESERVED (RSVD)**
9:5	0h WO	**Slot Number Default Config (SNDC):** 5bits of slot number as a default configuration. It can scale to max of 128 slots
4:1	0h WO	**EP Number (EP_NUM):** 4bits of EP number
0	0h WO	**Clear Internal Scheduler's Mask (CISM):** This is a register that is used to clear the internal scheduler's mask that is used to stop scheduling a particular EP. Bit0 indicates the direction of the EP

19.1.171 Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG)—Offset 807Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h WO	**Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG):** This register is used to clear the internal valid IN EP array that TRM stored in order to guarantee one IN EP per port. This register allows software to clear the valid bit of each port IN EP. This field indicates the port number. For a 2port configuration, only bit1:0 are valid. It can scale for the max number of ports that we support.

19.1.172 Clear Poll Mask Control (HOST_CLR_PMASK_REG)—Offset 8080h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**RESERVED (RSVD)**
9:5	0h WO	**Slot Number Default Config (SNDC):** 5bits of slot number as a default configuration. It can scale to max of 128 slots

Bit Range	Default & Access	Field Name (ID): Description
4:1	0h WO	**EP Number (EP_NUM):** 4bits of EP number
0	0h WO	**Clear Internal Scheduler's Poll Mask (CISPM):** This is a register that is used to clear the internal scheduler's poll mask that is used to indicate whether we need to poll this EP. This is used for USB2. Bit0 indicates the direction of the EP

19.1.173 Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8100h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RW	**Scheduler Host Control Reg Cont (SCHED_HOST_CTRL_CONT):** 31:25 Reserved (24): disable marking overlap flag on all TT periodic INs. (23): disable async. scheduling while periodic active to same port (22): disable "level" method of USB2 port periodic done check (on by default) (21): enable "strobe" method of USB2 port periodic done check (off by default)
20:13	4h RW	**TTE Host Control (TTE_HOST_CTRL):** (0): disable interrupt complete split limit to 3 microframes (1): disable checking of missed microframes (2): disable split error request w/NULL pointer on speculative INs with data payload and no TRB. (3): disable deferred split error request on speculative IN with data payload and no TRB. (7:4): reserved
12:11	0h RW	**Cache Size Control Reg (CACHE_SZ_CTRL):** 0: 64 1: 32 2,3: 16
10:9	0h RW	**Maximum EP Per Slot (MAX_EP_SLOT):** 0: 32 1: 16 2: 8 3: 4
8	1h RW	**Turn on scratch_pad_en (TO_SCRATCH_PAD_EN)**

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Scheduler Host Control Reg (SCHED_HOST_CTRL):** (0): disable poll delay (1): disable TRM active in EP valid check (2): enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip) (3) enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip) (5:4) scheduler sort pattern 00 (default) search ISO ahead of interrupt within each service interval 01 - search USB2-ISO, USB3-ISO, USB2-Interrupt, USB3-Interrupt within each service interval 10 - search strictly by interval 11 - search all ISO intervals ahead interrupt intervals and within each interval, USB2 ahead of USB3 (6): disable 1 pack scheduling limit when ISO pending in present microframe (7): enable check to stop scheduling on port that are not connected

19.1.174 Global Port Control (HOST_CTRL_PORT_CTRL)—Offset 80A0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 380Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**OVERFLOW ERROR DETECTION ENABLE (OVERFLOW_ERR_DETECT_EN)**
30:12	3h RW	**HBUF_WATER_MARK (HBUF_WATER_MARK)**
11	1h RW	**CPL Cut Thru Enable (CPL_CUT_THRU_EN)**
10:4	0h RW	**RESERVED (RSVD0)**
3:0	Fh RW	**RESERVED (RSVD1)**

19.1.175 Power Management Control (PMCTRL_REG)—Offset 80A4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2DFF90h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Async PME Source Enable (ASYNC_PME_SRC_EN):** This field allows the async PME source to be allowed to generate PME. This is specifically required for SOCs that do not allow for any clock other than RTC to be available during RTD3.
30	0h RW	**Legacy PME Source Enable (LEGACY_PME_SRC_EN):** This field allows the legacy PME source to be used in PME generation. The legacy source in in reference to the source prior to the RTD3 changes.
29	0h RW	**Reset Warn Power Gate Trigger Disable (RESET_WARN_PWR_GATE_TRIGGER_DISABLE):** This field controls the actions taken for due to reset warn. 0 - Reset Warn will trigger a HW autonomous Power Gate 1 - Reset Warn will not trigger a HW autonomous Power Gate
28	0h RW	**CLR_PME_FLAG_PULSE_AUX_CCLK (CLR_PME_FLAG_PULSE_AUX_CCLK)**
27	0h RW	**RESERVED (RSVD)**
26	0h RW	**XLFPSCOUNTSRC (XLFPSCOUNTSRC):** XLFPSCOUNTSRC (Source for LFPS OFF Counter) 0: Central RTC Counter for LFPS detection 1: Local Counter for LFPS detection
25	0h RW	**XELFPSRTC (XELFPSRTC):** XELFPSRTC (Enable LFPS Filtering on RTC) 0: Use Oscillator clock for LFPS Filtering during P3 1: Use RTC Clock for LFPS Filtering during P3
24	0h RW	**XMPHYSPGDD0I2 (XMPHYSPGDD0I2):** XMPHYSPGDD0I2 (ModPhy Sus Well Power Gate Disable for D0I2) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
23	0h RW	**XMPHYSPGDD0I3 (XMPHYSPGDD0I3):** XMPHYSPGDD0I3 (ModPhy Sus Well Power Gate Disable for D0I3) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
22	0h RW	**XMPHYSPGDRTD3 (XMPHYSPGDRTD3):** XMPHYSPGDRTD3 (ModPhy Sus Well Power Gate Disable for RTD3) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
21:18	Bh RW	**XD3RTCPTTM (XD3RTCPTTM):** XD3RTCPTTM (D3 RTC Port Timer Tick Multiplier) This register will be the multiplication factor for determining RXDET based on the XD3RTCPTTC value. If XD3RTCPTTC is 9h and this register is Bh, frequency for RXDET a detection while MODPHY SUS Power gating is enabled would be 99ms.
17	0h RW	**U3 LFPS Periodic Sampling ON Time Control (U3_LFPS_PRDC_SAMPLING_ON_TIME_CTRL):** This field controls the ON time for the LFPS periodic sampling for USB3 ports. 0 ON time is 2 rtc clocks 1 ON time is 3 rtc clocks Note: This field is ignored if USB3 PHY SUS Well Power Gating is enabled.

Bit Range	Default & Access	Field Name (ID): Description
16	1h RW	**AON LFPS Detector Enable Mode (AON_LFPS_DETECTOR_EN_MODE):** 1 - Allow the LFSP Detector in AON to own LFPS detection when the port is in PS3 for U2/U3 - not RxD regardless of port ownership. 0 - Allow the LFPS Detector in AON to own the LFPS detection only when the AON owns the port and in U2/U3 - not RxD
15:8	FFh RW	**SS U3 LFPS Detection Threshold (SS_U3_LFPS_DETECTION_THRESHOLD):** This field controls the threshold used to determine when a valid U3 Wake is detected through when using the unfiltered LFPS source. The value on this field will reflect the binary count required to have been detected on the counter being clocked by the unfiltered lfps source to result in a valid U3 wake detection.
7:4	9h RW	**SS_U3_LFPS_PRDC_SAMPLING_OFFTIME_CTRL (SS_U3_LFPS_PRDC_SAMPLING_OFFTIME_CTRL):** This field controls the OFF time for the LFPS periodic sampling for USB3 Ports 0x0 periodic sampling is disabled. 0x1 OFF time is 1ms 0x2 OFF time is 2ms 0xF OFF time is 15ms The ON Time is determined by the amount of time required to reliably determine if there is a valid LFPS and is HW implementation specific. A speed up mode shall be implemented where this field is in units of us. i.e. 0x1 = 1 us OFF time, 0x2 = 2 us OFF time, etc.
3	0h RW	**PS3 LFPS Source Select (PS3_LFPS_SRC_SEL):** 0 LFPS Source is unfiltered 1 LFPS Source is filtered (Rx-Elec-Idle) LFPS Source is Rx-Elec-Idle for any non PS3 state.
2	0h RW	**XHCI Engine Autonomous Power Gate Exit Reset Policy (XHC_AUTO_PWRGATE_EXITRST_POLICY):** Controls when the xHCI engine is brought out of reset due to a power ungate. 0 Engine is brought out of reset when D3 to D0 is triggered. This allows for a quick power up sequence while leaving the virtual PCIe LTSSM in L23 is power ungate is not due to D3 to D0. 1 Engine is brought out of reset along with the rest of the IP. This is required for PMC save/restore flow.
1	0h RW	**USB2 Port Wake Unit Coupling Policy (USB2_PORT_WAKE_COUPLING_POLICY):** Controls the trigger for USB2 Port Wake Units to initiate Port Level Power Off Preparation. 0 RTD3 triggered 1 - Port Triggered when in L1, L2 or Disabled, Disconnected
0	0h RW	**USB3 Port Wake Unit Coupling Policy (USB3_PORT_WAKE_COUPLING_POLICY):** Controls the trigger for USB3 Port Wake Units to initiate Port Level Power Off Preparation. 0 - RTD3 Triggered 1 - Port Triggered when in PS3 due to RxDetect, U3, U2 or Disabled

19.1.176 PGCB Control (PGCBCTRL_REG)—Offset 80A8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 315555h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**RESERVED (RSVD)**
27:25	0h RW	**IP_INACCESSIBLE_HYSTERESIS_TIMER (IP_INACCESSIBLE_HYSTERESIS_TIMER):** 000 ? 50us 001 ? 100us 010 ? 150us 011 ? 200us 000 ? 250us 001 ? 300us 010 ? 350us 111 ? 400us
24	0h RW	**Override_Disable (OVERRIDE_DISABLE)**
23:20	3h RW	**CDH Aggregation Minimum Wait Time (CDH_MIN_WAIT_TIME):** This field controls the minimum time that we must wait for resets to propagate before allowing Power Up flow to complete. The Power Up flow requires special handling of clocks, reset and sleep signaling which requires the CDH to monitor reset propagation. This timer allow for flexibility on when we consider all resets propagated. 0h Disabled 1h 2 clocks 2h 4 clocks 3h 8 clocks 4h 16 clocks 5h 32 clocks 6h 64 clocks 7h 128 clocks
19	0h RW	**RESERVED (CDH_RST_PROPAGATION_CNTRL):** This bit will indicate the mode of operation for the CDH Reset Propagation Aggregator. It allows for a mode where the aggregation will wait for an indication from each CDH before proceeding OR ignore the CDH indication before proceeding. Regardless of the mode, the aggregator will enforce the CDH Aggregation Mini Wait Time. 0 Aggregate all the CDH indications before triggering the CDH Aggregation Mini Wait Time. Once the Min Wait Time is met a notification to the Power Sequencer/Control will be initiated 1 Trigger the CDH Aggregation Mini Wait Time w/o waiting for CDH indication. Once the Min Wait time is met a notification to the Power Sequencer/Control will be initiated.
18	0h RW	**MMP_PFET_REQ_OVRD (MMP_PFET_REQ_OVRD):** This bit will disable the MMP PFET request condition for PGCB control. 1 MMP PFET Request Ignored 0 Default
17:16	1h RW	**PGCB Clock Gate Request to PGCB Sleep (PGCB_CLK_GATE_REQ_2_PGCB_SLEEP):** Value representing the minimum number of delay clocks required between the assertion of pgcb_ip_clkgate_b to the deassertion of pgcb_sleep on PG exit. (This is only applicable for IP-Accessible PG with state-retention enabled.) Please see the description of cfg_tsleepact for more details.

Bit Range	Default & Access	Field Name (ID): Description
15:14	1h RW	**PGCB Sleep Deassertion to PGCB ISM Unlock Req (PGCB_SLEEP_DEASRTN_2_ISM_UNLOCK_REQ):** For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the deassertion of gcb_sleepto the deassertion of pgcb_ip_*_lock_req_b. For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the deassertion of pgcb_sleep to the deassertion of pgcb_isol_en_b.
13:12	1h RW	**PGCB Prim Reset Deassertion to PGCB Next State (PGCB_PRIMRST_DEASRTN_2_NSTATE):** For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the deassertion of pgcb_sleep to the deassertion of pgcb_ip_*_lock_req_b. For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the deassertion of pgcb_sleep to the deassertion of pgcb_isol_en_b.
11:10	1h RW	**PGCB Side Reset Deassertion to PGCB Prim Reset Deassertion (PGCB_SIDERST_DEASRTN_2_PRIMERST_DEASRTN):** Value representing the number of delay clocks required between the deassertion of gcb_force_rst_bto the deassertion of gcb_force_prim_rst_b (This is only applicable for IP-Accessible PG.) Please see the description of cfg_tsleepact for more details.
9:8	1h RW	**PGCB Latch Isolation High to PGCB Clock Ungate Request (PGCB_LATCH_ISO_HI_2_PGCB_CLK_UNGATE_REQ):** Value representing the number of delay clocks required between the assertion of pgcb_isol_latchen to the deassertion of pgcb_ip_clkgate_req_b. Please see the description of cfg_tsleepact for more details.
7:6	1h RW	**PGCB Isolation Deassertion to PGCB Latch Isolation High Count (PGCB_ISO_DEASRTN_2_PGCB_ISO_HI_CNT):** Value representing the minimum number of delay clocks required between the deassertion of pgcb_isol_en_b to the assertion of gcb_isol_latchen. Please see the description of cfg_tsleepact for more details.
5:4	1h RW	**PGCB Reset Assertion to PGCB Power Down Request Count (PGCB_RST_2_PGCB_PWRDOWN_REQCNT):** For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the assertion of pgcb_force_prim_rst_b and pgcb_force_rst_b to the assertion of pgcb_pmc_pg_req_b. For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the assertion of pgcb_force_prim_rst_b and pgcb_force_rst_b to the assertion of pgcb_sleep. Please see the description of cfg_tsleepact for more details.

Bit Range	Default & Access	Field Name (ID): Description
3:2	1h RW	**PGCB Isolation Assertion to PGCB Reset Assertion Count (PGCB_ISO_ASRTN_2_PGCB_RST_ASRTN_CNT):** Value representing the minimum number of delay clocks required between the assertion of gcb_isol_en_bto the assertion of gcb_force_prim_rst_band gcb_force_rst_b Please see the description of [1:0] for more details.
1:0	1h RW	**PGCB Sleep Assertion to PGCB Isolation Enable Count (PGCB_SLEEP_ASRTN_2_PGCB_ISO_EN_CNT):** For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the assertion of pgcb_sleep (and the deassertion of pgcb_isol_latchen) to the assertion of pgcb_isol_en_b. For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the deassertion of pgcb_isol_latchen to the assertion of pgcb_isol_en_b, as well as the minimum number of delay clocks required between the assertion of pgcb_sleep to the assertion of pgcb_pmc_pg_req_b. Common for all cfg_t* inputs: 0 1 clock 1 2 clocks 0 8 clocks 1 256 clocks For any of the cfg_t* inputs that an IP may feel are a don-care and the IP does not feel they will be useful for post-silicon debug, the recommendation is to tie the input to 201 (2 clocks). Otherwise, the inputs may be tied to another relevant value or connected to a configuration register. Note: These signals may only change while pgcb_pwrupidle is asserted, if pgcb_pwrupidle is deasserted it should be valid and stable. (It may change the same cycle that ip_pgcb_pg_rdy_req_b asserts.)

19.1.177 D0I3 Control (DOI3CTRL_REG)—Offset 80ACh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**RESERVED (RSVD)**
3	1h RW/1C	**RestoreRequired (RESTORE_REQUIRED):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3 (D0I3):** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1:0	0h RO	**RESERVED (RSVD1)**

19.1.178 HOST_CTRL_MISC_REG (HOST_CTRL_MISC_REG)—Offset 80B0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1037Fh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**USB2_LTRUPDT_DIS (USB2_LTRUPDT_DIS)**
30	0h RW	**USB2 Line State Debounce During Port Reset Policy (USB2_LINE_STATE_DEBOUNCE_DURING_PORT_RESET_POLICY):** This register controls how the debounce is enforced during the Port Reset phase. 0 do not enable the line state debounce during port reset. 1 enable the line state debounce during port reset.
29	0h RW	**TTE PEXE Credit Fix Disable (TTE_PEXE_CREDIT_FIX_DISABLE):** When set, it disables a fix implemented to re-deem PEXE credits when a port is disconnected
28	0h RW	**TTE Scheduling policy (TTE_SCHEDULING_POLICY):** This register controls a fix made to prevent over-scheduling by not account for 188B in each uFrame. Setting this bit will disable the fix and allow for over-scheduling.
27	0h RW	**USB3 ITP Delta Timer Source Select (USB3_ITP_DELTA_TIMER_SOURCE_SELECT):** This register selects the source for the delta timer tracking used for ITP generation. 0 the source is a 16.666 ns tick generated from a crystal reference clock 1 - the source is a 16.666 ns tick generated from the aux_cclk. This field needs to remain in sync with Frame Timer Source Select to ensure the are both set or both cleared. There is no support for any other combination.
26	0h RW	**Frame Timer Source Select (FRAME_TIMER_SOURCE_SELECT):** This register controls the source for the frame timer. 0 the source for the frame timer is a crystal reference clock 1 the source for the frame timer is the aux_cclk.
25	0h RW	**uFrame Masking Enable (UFRAME_MASKING_ENABLE):** If set, enables the uFrame tick to be masked due to ports being in U3/NC. This controls a fix made to disable the auto masking of uFrame tick due to port state w/o any pipeline idle condition. When cleared, we rely on gating of frame timer due to proper port state and idleness tracking from the pipeline.
24	0h RW	**Late FID Check Disable (LATE_FID_CHECK_DISABLE):** This register disables the Late FID Check performed when starting an ISOCH stream.

Bit Range	Default & Access	Field Name (ID): Description
23:20	0h RW	**RESERVED (RSVD1)**
19	0h RW	**USB2 Resume Cx Inhibit Disable (USB2_RESUME_CX_INHIBIT_DISABLE):** Controls if USB2 L1 Resume is allowed to contribute to DMA Active which will inhibit Cx state. 0 USB2 L1 Resume is allowed to inhibit Cx via DMA Active 1 USB2 L1 Resume is NOT allowed to inhibit Cx via DMA Active When cleared, Cx will only be inhibited when the DMA traffic for the port begins.
18:16	1h RW	**Extra uFrame (EXTRA_UFRAME):** This register controls the extra number of uFrames added onto the advancing of late FID check.
15:0	37Fh RW	**Valid Isoch Scheduling Range (VALID_ISOCH_SCHEDULING_RANGE):** This register defines the window in miliseconds from the current Frame that will be considered for scheduling in an upcoming Frame. Anything scheduled outside of this window will be considered as late and will trigger the Missed Service Error.

19.1.179 HOST_CTRL_MISC_REG2 (HOST_CTRL_MISC_REG2)—Offset 80B4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**max_short_pkt_adv_cnt (MAX_SHORT_PKT_ADV_CNT)**
28	0h RW	**dis_sch_frameid_chk (DIS_SCH_FRAMEID_CHK)**
27:13	0h RW	**misc_config_reg2_27_13_rsvd (RSVD1)**
12	0h RW	**disable_idt_fix_odma (DISABLE_IDT_FIX_ODMA)**
11	0h RW	**disable_ping_fix_odma (DISABLE_PING_FIX_ODMA)**
10	0h RW	**disable_cerr_fix_idma 0: fix is enabled 1:fix is disabled (DISABLE_CERR_FIX_IDMA)**
9	0h RW	**en_100ms_watch_dog_timer (EN_100MS_WATCH_DOG_TIMER)**
8	0h RW	**en_watch_dog_timer (EN_WATCH_DOG_TIMER)**

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**misc_config_reg2_bit7_rsvd (RSVD2)**
6	0h RW	**disable_tcg_ungate_on_flush (DISABLE_TCG_UNGATE_ON_FLUSH)**
5	0h RW	**disable_vnn_frame_timer (DISABLE_VNN_FRAME_TIMER)**
4	0h RW	**disable_clr_ccs_on_cas_set (DISABLE_CLR_CCS_ON_CAS_SET)**
3	0h RW	**disable_rhub_park_at_dbcDisc (DISABLE_RHUB_PARK_AT_DBCDISC)**
2	0h RW	**disable_block_wpr_on_disPorts (DISABLE_BLOCK_WPR_ON_DISPORTS)**
1:0	0h RW	**HOST_CTRL_MISC_REG2_bits1_0 (HOST_CTRL_MISC_REG2_1_0)**

19.1.180 SSPE_REG (SSPE_REG)—Offset 80B8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ssCfgBlockPwrDwn4ActLFPS (SS_CFG_BLOCK_PWRDWN_4_ACT_LFPS)**
30	0h RW	**dis_clr_ccs_4hcreset (DIS_CLR_CCS_4_HCRESET)**
29	0h RW	**disable_rawlfps_based_wake_fix (DISABLE_RAWLFPS_BASED_WAKE_FIX)**
28:7	0h RO	**Rsvd (Rsvd)**
6:0	0h RW	**SSPE_REG (SSPE_REG)**

19.1.181 (SSPITPE)—Offset 80BCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 7Fh

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**RSVD (RSVD)**
6:0	7Fh RW	**ITP Transmit Enable (ITP_TRANSMIT_EN):** Width is scaled with USB3 Port Count PortCount=4

19.1.182 AUX Reset Control (AUX_CTRL_REG)—Offset 80C0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 15FC0F0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Reset USB3 AUX/Main PD Logic (RST_U3_AM_PDL):** A reset that is designed to reset all USB3 port AUX + Main power domain logic. This is a debug function. It is called cold reset. Write 1 to this register will issue a cold reset to USB3 ports.
30	0h RW	**RESERVED (RSVD)**
29	0h RW	**Enable PCIe PIPE Reset As PCIe PHY Reset (EN_PPIPE_PPHY_RST):** This bit set to 1 selects the PCIe PIPE reset as a PCIe PHY power on reset. 0 selects the AUX powerup reset as a PCIe PHY powerup reset.
28	0h RW	**Ensure PIPE Powerdown On PERST# (EN_PPWRDN_PERST):** This bit ensures any PERST# being asserted will cause PIPE powerdown state transition to P1.
27	0h RW	**Disable PERST# Main RST (DIS_PERST_MRST):** There is a feature where we only allow PERST# to be treated as a main powerdown reset when it is asserted during the state that is not in D3. This bit disables this feature when it is set to 1. If this bit is set to 1, it means that any PERST# will be treated as a main power domain reset regardless of its Dstate.
26	0h RW	**Disable PCIe PERST# Host Controller (DIS_PERST_HC):** There is a feature where we can disable PCIe PERST# from reset the host controller until power management control module has done its clock switching. This is for a case where PM entered L23 and immediately PERST# asserted. This bit is designed to enable this feature when set to 1.
25	0h RW	**Enable Fast Simulation Reset Mode (EN_FAST_RST):** Enable a fast simulation mode for reset function. This is a feature for GLS
24	1h RW	**Prevent USB3 Link Down Reset (PREV_U3_LDRST):** When set to 1 prevent a reset being generated due to the USB3 port link down condition.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**Ignore Main Power Up Reset (IGN_MPU_RST):** When set to 1 ignore the main power up reset for USB3 PIPE PHY reset.
22	1h RW	**RESERVED (RSVD_1)**
21	0h RW	**Ignore HC Reset USB2 (IGN_HC_RST_U2):** When set to '1' ignore HC reset to reset the USB2 Port logic
20	1h RW	**Ignore HC Reset USB PHY (IGN_HC_RST_UP_POR):** When set to '1' ignore HC reset to the USB PHY power-on reset
19	1h RW	**Enable PCIe Link-Down Reset (EN_PLD_RST):** Enable a reset due to a PCIe link-down condition. The PCIe link down condition will cause a HC reset liked. If this bit is set 1, the PCIe link down condition will only reset the PCIe core.
18	1h RW	**Enable EEPROM Reload On Power Up (EN_EEP_REL_PU):** When set to '1' enable EEPROM reload on every main power-up
17	1h RW	**Ignore HC Reset PCIe PHY PIPE (IGN_HC_RST_PPP):** When set to '1' ignore HC reset to the PCIe PHY PIPE reset
16	1h RW	**Ignore LTSSM Reset USB PHY PIPE (IGN_LRST_UPP):** When set to '1' ignore the LTSSM of USB link state transition caused reset to USB PHY PIPE reset
15	1h RW	**Ignore Warm Reset USB PHY Power (IGN_WR_UPP):** When set to '1' ignore warm reset the USB PHY power on reset
14	1h RW	**Allow Core PCIe Link Down Reset (ALL_CPLD_RST):** When set to '1' allow PCIe link down to cause a reset to the rest of the core
13	0h RW	**Ignore Hot Reset USB3 (IGN_HR_U3):** When set to '1' ignore hot reset to the USB3 port logic
12	0h RW	**Ignore Warm Reset USB3 (IGN_WR_U3):** When set to '1' ignore warm reset to the USB3 port logic
11	0h RW	**Ignore Main Power Up Reset USB3 (IGN_MPU_RST_U3):** When set to '1' ignore main power up reset to USB3 port logic
10	0h RW	**Ignore Main Power Up Reset USB2 (IGN_MPU_RST_U2):** When set to '1' ignore main power up reset to USB2 port logic
9	0h RW	**Ignore Main Power Up Reset PCIe Core (IGN_MPU_RST_PC):** When set to '1' ignore main power up reset to PCIe core
8	0h RW	**Ignore Main Power Up Reset PCIe PHY (IGN_MPU_RST_PP):** When set to '1' ignore main power up reset to PCIe PHY
7	1h RW	**Ignore HC Reset USB PHY (IGN_HC_RST_UP):** When set to '1' ignore HC reset to the USB PHY
6	1h RW	**Ignore Warm Reset USB PHY (IGN_WRST_UP):** When set to '1' ignore warm reset to the USB PHY
5	1h RW	**Enable HC Reset Per Port Isolation (EN_HC_RST_PPI):** Enables the HC reset or per port reset isolation function

Bit Range	Default & Access	Field Name (ID): Description
4	1h RW	**Allow Power Off Power Domain Reset (ALL_PO_PDRST):** When set to '1' allow main power off condition to trigger a main power domain reset
3	0h RW	**Ignore Wait For PERST# During Power Show Down (IGN_PERST_PSD):** When set to '1' ignore waiting for PERST# deassertion during main power show down.
2	0h RW	**Ignore Fundamental Reset During AUX Power Up (IGN_FRST_AUX_PU):** When fundamental reset is asserted during AUX power up, if this bit is set, then we will ignore PERST# such that purely wait for timeout to deassert fundamental reset.
1:0	0h RW	**Trigger Fundamental Reset (TRIG_FRST):** Writing to bit(1:0) to value of 2'b11 will cause a fundamental reset

19.1.183 Super Speed Bandwidth Overload (HOST_BW_OV_SS_REG)—Offset 80C4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4A4008h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**RESERVED (RSVD)**
23:12	4A4h RW	**Max. TT BW Allowed (MAX_TT_BWA):** see white paper
11:0	8h RW	**Per Packet Overhead SS BW (PP_OVRH_SSBW):** BW calculation: Overhead per packet for SS BW calculations. see white paper.

19.1.184 High Speed TT Bandwidth Overload (HOST_BW_OV_HS_REG)—Offset 80C8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1A01Fh

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**RESERVED (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
23:12	1Ah RW	**Per Packet Overhead HS-TT BW (PP_OVRH_HSTTBW):** BW calculation: Overhead per packet for HS-TT BW calculations. see white paper.
11:0	1Fh RW	**Per Packet Overhead HS BW (PP_OVRH_HSBW):** BW calculation: Overhead per packet for HS BW calculations. see white paper.

19.1.185 Bandwidth Overload Full Low Speed (HOST_BW_OV_FS_LS_REG)—Offset 80CCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 14080h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**RESERVED (RSVD)**
23:12	14h RW	**Per Packet Overhead FS BW (PP_OVRH_FSBW):** BW calculation: Overhead per packet for FS BW calculations. see white paper.
11:0	80h RW	**Per Packet Overhead LS BW (PP_OVRH_LSBW):** BW calculation: Overhead per packet for LS BW calculations. see white paper.

19.1.186 System Bandwidth Overload (HOST_BW_OV_SYS_REG)—Offset 80D0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 32010h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**RESERVED (RSVD)**
23:12	32h RW	**Per TT Packet Overhead System BW (PTTP_OVRH_SBW):** BW calculation: Overhead per TT packet for System BW calculations. see white paper.

Bit Range	Default & Access	Field Name (ID): Description
11:0	10h RW	**Per Packet Overhead System BW (PP_OVRH_SBW):** BW calculation: Overhead per packet for System BW calculations. see white paper.

19.1.187 Scheduler Async Delay (HOST_CTRL_SCH_ASYNC_DELAY_REG)—Offset 80D4h

Global defaults for inserting delays between packets in the scheduler for async. types.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**RESERVED (RSVD)**
19	0h RW	**High-Speed Bulk Delay Enable (HS_BD_EN)**
18:16	0h RW	**High-Speed Bulk Delay Default (HS_BD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...)
15	0h RW	**Full-Speed Bulk Delay Enable (FS_BD_EN)**
14:12	0h RW	**Full-Speed Bulk Delay Default (FS_BD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...)
11	0h RW	**High-Speed Control Delay Enable (HS_CD_EN)**
10:8	0h RW	**High-Speed Control Delay Default (HS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...)
7	0h RW	**Full-Speed Control Delay Enable (FS_CD_EN)**
6:4	0h RW	**Full-Speed Control Default (FS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...)
3	0h RW	**Low-Speed Control Delay Enable (LS_CD_EN)**
2:0	0h RW	**Low-Speed Control Delay Default (LS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...)

19.1.188 DEVICE MODE CONTROL REG 0 (DUAL_ROLE_CFG_REG0)—Offset 80D8h

All bits in this register must be in the Always ON Power domain (ungated SUS or AON as appropriate)

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**XDCI_DRD_CTRL_EN (REG_IN_XDCI):** When DRD_ACCESS_MODE (bit 18) =1, 0 -- The policies below is controlled by register in the XHCI MMIO 1 -- The policies below is controlled by register in the XDCI MMIO When DRD_ACCESS_MODE =0, this bit is a don?t care.
30:28	0h RW	**DRD_WDT_TIMER (DRD_WDT_TIMER):** 0-based incremental of 500ms
27	0h RW	**EN_DRD_WDT_SWITCH_FROM_HOST_TO_DEVICE (EN_DRD_WDT_SWITCH_FROM_HOST_TO_DEVICE)**
26	0h RW	**EN_DRD_WDT_SWITCH_FROM_DEVICE_TO_HOST (EN_DRD_WDT_SWITCH_FROM_DEVICE_TO_HOST)**
25	0h RW	**EN_DRD_WDT_SWITCH_OUT_OF_COLD_RESET (EN_DRD_WDT_SWITCH_OUT_OF_COLD_RESET)**
24	0h RW	**SW_VBUS_VALID (SW_VBUS_VALID):** if SW_IDPIN_EN (bit 21) is 1, 0 ? deassert sw vbus valid 1 ? assert sw vbus valid
23	0h RW	**EN_PIPE_4_1_SYNC_PHY_STATUS (EN_PIPE_4_1_SYNC_PHY_STATUS)**
22	0h RW	**EN_PIPE_RX_ON_IDPIN (EN_PIPE_RX_ON_IDPIN):** During the connection to a device, there may be a delay in DRD switch from XDCI to XHCI mode,the rx term can be low after idpin deasserts. If this bit is 0, the rx term will be assert immediately after idpin toggle. Otherwise, the device may fall back to USB2 mode. 1 -- drive 0s on utmi rx signals to controller if not connected.
21	0h RW	**SW_IDPIN_EN (SW_IDPIN_EN):** SW_IDPIN_EN 1 -- enable SW id pin (pre DRD) 0 -- disable SW id pin.
20	0h RW	**SW_IDPIN (SW_IDPIN):** if SW_IDPIN_EN (bit 21) is 1, 0 - host mode 1 - device mode
19	0h RW	**USB2_SUSP_OR_DIS (USB2_SUSP_OR_DIS):** 1 - The DRD UTMI suspendm will be controlled by host/device based on the DRD switch. 0 - whenever device or host deassert suspendm, the DRD UTMI suspendm will be deasserted.
18	0h RW	**DRD_ACCESS_MODE (DRD_ACCESS_MODE):** 0 - The DUAL_ROLE register from host and device are ORed to control DRD 1 - The DUAL_ROLE register from host and device are selected by XDCI_DRD_CTRL_EN (bit 31) to control DRD

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**EN_DIRECT_DRD_SWITCH_ON_USB3PORT_BY_IDPIN (EN_DIRECT_DRD_SWITCH_ON_USB3PORT_BY_IDPIN):** 0 enable the direct DRD switch on USB3 port by idpin 1 disable the direct DRD switch
16	0h RW	**SW_SWITCH_ENABLE (SW_SWITCH_ENABLE):** SW switch enable 0 (default) ID pin HW controlled DRD. 1 -- SW controlled DRD (ignore idpin), switch based on the DRD_CONFIG.
15	0h RW	**RSVD (RSVD)**
14:3	100h RW	**DEBOUNCE_VAL (DEBOUNCE_VAL):** ID ping debounce timer (DEBOUNCE_VAL): in the unit of RTC clock (33us) default to 8.448 ms
2	0h RW	**SYNCHRONIZE_SS_HS_SWITCH (SYNCHRONIZE_SS_HS_SWITCH):** Synchronize the SS and HS switch: 0 (default) Does not synchronize. i.e. HS switch on the debounced id pin, while SS switch independently controlled by the sequencer. 1 synchronize HS and SS switch. Both speeds switch when sequencer switch.
1:0	0h RW	**DRD_CONFIG (DRD_CONFIG):** 00 Dynamic DRD switch mode 01 static host mode 10 static device mode 11 -- reserved

19.1.189 DEVICE MODE CONTROL REG 1 (DUAL_ROLE_CFG_REG1)—Offset 80DCh

All bits in this register must be in the Always ON Power domain (ungated SUS or AON as appropriate)

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**BVALID_HW (HW_BVALID):** hardware bvalid
30	0h RO	**DRD_STATUS_B31_30 (DRD_STATUS_30)**
29	0h RO	**DRD_MODE (DRD_MODE):** SS DRD mode 0 device mode 1 host mode
28	1h RO	**IDPIN (IDPIN):** IDPIN value hw version
27:16	0h RO	**DRD_STATUS_B27_16 (DRD_STATUS_B27_16)**

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**DRD_CONTROL_B15_0 (DRD_CONTROL_B15_0)**

19.1.190 AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 808DBCA0h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**D3 Hot function enable register (D3_HOT_FXN_EN):** This bit is from pin input which is set 1. But we allow software to alter it if it is needed. 1: D3 hot enabled 0: D3 hot not abled.
30	0h RW	**Allow L1 Core Clock Gating (ALL_L1_CORE_CG):** When set to 1 allows core clock being gated during L1 state.
29	0h RW	**Allow Engine PHY Status Extension (AL_EP_SEXT):** When set to 1 allows the engine to extend PHY status of PCIe PIPE for one more cycle. This is due to the fact that our rate change function has a potential of not being able to sample the phystatus signal.
28	0h RW	**Allow Engine PCIe Rate Change Passing (ALL_EP_RCP):** When set to 1 allows the engine to pass PCIe rate change signal as it is from PCIe core to PCIe PHY.
27	0h RW	**Allow Engine PERST Fundamental Reset (AL_PERST_FRST):** When set to 1 allow engine to treat PERST# as a foundamental reset
26	0h RW	**Overwrite PCIe P2 to P1 (OVR_PCIE_P2_P1):** When set to 1 will overwrite a PCIe powerdown state of P2 to P1.
25	0h RW	**Set Internal SSV 1 (SET_ISSV_1):** When set to 1 set the internal SSV to 1.
24	0h RW	**Clear Internal SSV 0 (CLR_ISSV_0):** When set to 1 clear the internal SSV to 0.
23	1h RW	**Enable save_restore_enable SW Loading (EN_SRE_SW_LD):** This is a bit that enables the save_restore_enable signal being loaded when a software command has set Save bit. This is a debug function.
22	0h RW	**RESERVED (RSVD_1)**

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Force save_restore 1 (FORCE_SR1):** When set to 1, it will force the save_restore flag to 1. This flag is an bit to ensure that we have masked the update during low power state. If software write this bit to 1, it must write it to 0 in order to resume the normal save and restore function.
20	0h RW	**cfg pcie txreg rd (CPTR)**
19	1h RW	**cfg iob drivestrength[1] (CIDS1)**
18	1h RW	**cfg iob drivestrength[0] (CIDS0)**
17	0h RW	**Enable CFG USB P2 (EN_CFG_UP2):** When set to '1' enable cfg usb p2
16	1h RW	**cfg clk gate dis (CCGD)**
15	1h RW	**Enable CFG RXDET P3 (EN_CFG_RDP3):** When set to '1' enable cfg rxdet p3
14	0h RW	**Enable CFG PIPE Reset (EN_CFG_PIPE_RST):** When set to '1' enable cfg pipe rst
13	1h RW	**Enable Filter TX Idle (EN_FILT_TX_IDLE):** When set to 1 enables a filter function to TX electrical idle signal at PCie PIPE. We have a filter that will set TXelecidle signal of PCIe PIPE to 1 whenever we are in isolation state or power down transition states.
12	1h RW	**Enable Host Engine Generate PME (EN_HE_GEN_PME):** This is a global switch to whether or not eable this host engine to generate PME message.
11	1h RW	**Enable Isolation (EN_ISOL):** When set to '1' enable isolation
10	1h RW	**Enable L1 Caused P2 Overwrite (EN_L1_P2_OVR):** Set 1 to enable a new feature. This new feature is designed to use L1 as a state to identify whether we should do P2 Overwrite or not. We used to use P1 state to identify whether or not to invoke P2 overwrite function.
9	0h RW	**Enable Core Clock Gating (EN_CORE_CG):** When set to '1' enable core clock gating based on low power state entered
8	0h RW	**Enable PHY Status Timeout (EN_PHY_STS_TO):** When set to '1' enable PHY status timeout function which is designed to cover the PCIePHY issue that we may have not able to detect the PHY status toggle.
7	1h RW	**Ignore aux_pm_en PCIe Core (IGN_APE_PC):** When set to '1' ignore the aux_pm_en reg from PCIe core to continue the remote wake/clock switching support

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Enable P2 Overwrite P1 (EN_P2_OVR_P1):** When set to '1' enable P2 overwrite P1 when PCIe core has indicated the transition from P0 to P1. This is to enable entering the even lower power state.
5	1h RW	**Enable P2 Remote Wake (EN_P2_REM_WAKE):** When set 1 '1' enable the remote wake function by allowing P2 clock/ switching and P2 entering
4:1	0h RW	**Forced PM State (FORCED_PM_STATE)**
0	0h RW	**Initiate Force PM State (INIT_FPMS):** When set to '1' force PM state to go to the state indicated in bit 4:1

19.1.191 Battery Charge (BATTERY_CHARGE_REG)—Offset 80E4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable DM_SRC Battery Charge (EN_DS_BC):** 1 - Always enable battery charge DM_SRC if not connected. Don't wait for portable device detect. (spec. ver. 1.2) 0 - Battery charge spec ver. 1.1.
30:4	0h RO	**RESERVED (RSVD)**
3	0h RW	**Enable Port 3 Battery Charging (EN_P3_BC):** 0 - Battery charging disabled (Physical Port #3) 1 - Battery charging enabled (Physical Port #3)
2	0h RW	**Enable Port 2 Battery Charging (EN_P2_BC):** 0 - Battery charging disabled (Physical Port #2) 1 - Battery charging enabled (Physical Port #2)
1	0h RW	**Enable Port 1 Battery Charging (EN_P1_BC):** 0 - Battery charging disabled (Physical Port #1) 1 - Battery charging enabled (Physical Port #1)
0	0h RW	**Enable Port 0 Battery Charging (EN_P0_BC):** 0 - Battery charging disabled (Physical Port #0) 1 - Battery charging enabled (Physical Port #0)

19.1.192 Port Watermark (HOST_CTRL_WATERMARK_REG)—Offset 80E8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 800080h

Bit Range	Default & Access	Field Name (ID): Description
31:16	80h RW	**RBUF water mark (RBUF_WM)**
15:0	80h RW	**XBUF water mark (XBUF_WM)**

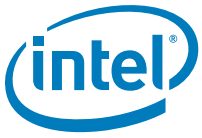
19.1.193 SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 18010000h

Bit Range	Default & Access	Field Name (ID): Description
31:27	3h RW	**Force LTSSM State (FORCE_LTSSM_ST):** LTSSM state to be forced This value is for test purpose only.
26	0h RW	**Direct Link LTSSM State (DL_LTSSM_ST):** 0: Normal operation mode 1: Direct link to a specific state specified by bit 31:27 This bit is for test purpose only. It shall be written 0 in normal operation mode.
25	0h RW	**Direct Link To U0 (DL_U0):** 0: Normal operation mode 1: Direct link to U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
24:21	0h RW	**Forced Compliance Pattern (FORCED_CMP_PAT):** Compliance pattern to be forced to enter compliance mode This value is for test purpose only.
20	0h RW	**Enable Link Error Slave Count (EN_LES_CNT):** 0: Disable link error slave count 1: Enable link error slave count
19:17	0h RW	**Debug Mode Select (DEBUG_MD_SEL)**
16:15	2h RW	**PHY Low Power Latency (PHY_LP_LAT):** This field defines the latency to drive the PHY to enter low power mode 0: 4 cycles 1: 8 cycles 2: 16 cycles 3: 32 cycles
14:12	0h RW	**Link Recovery Minimum Time (LR_MIN_TM):** This value defines the minimum time for the link to stay in Recovery.Active other than from U3. The granuity is 128us.



Bit Range	Default & Access	Field Name (ID): Description
11:9	0h RW	**Link Polling Minimum Time (LP_MIN_TM):** This value defines the minimum time for the link to stay in Polling.Active and Recovery.Active from U3. The granuity is 128us.
8	0h RW	**Force Link Accept PM Command (FORCE_LA_PMC):** 0: Normal operation mode 1: Force link to accept power management command
7	0h RW	**Direct Link Recovery U0 (DL_REC_U0):** 0: Normal operation mode 1: Direct link to Recovery from U0
6	0h RW	**Link Fast Training Mode (LINK_FTM):** 0: Normal operation mode 1: Link fast training mode This bit should be written 0 in normal operation.
5	0h RW	**Disable Link Scrambler (DIS_LINK_SCRAM):** 0: Enable link scrambler 1: Disable link scrambler
4	0h RW	**Direct Link U3 From U0 (DL_U3_U0):** 0: Normal operation mode 1: Direct link to U3 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
3	0h RW	**Direct Link U3 From U0 (DL_U2_U0):** 0: Normal operation mode 1: Direct link to U2 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
2	0h RW	**Direct Link U3 From U0 (DL_U1_U0):** 0: Normal operation mode 1: Direct link to U1 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
1	0h RW	**Enable Link Loopback Master Mode (EN_LINK_LB_MAST):** 0: Disable link loopback master mode 1: Enable link loopback master mode
0	0h RW	**Disable Link Compliance Mode (DIS_LINK_CM):** 0: Enable link compliance mode 1: Disable link compliance mode

19.1.194 USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h

These set of registers is used to control USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 310803A0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	31h RW	**FS/LS Mode SE0 Disconnect Delay[7:0] (FSLS_SE0_DIS_DEL_7_0):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred.

Bit Range	Default & Access	Field Name (ID): Description
23:21	0h RW	**Reserved (RSVD0)**
20	0h RW	**L1_EXIT_RECOVERY_MODE (L1_EXIT_RECOVERY_MODE):** Mode for extended L1 Exit recovery delay: 0: 12us 1: 50us
19	1h RW	**L1_TO_INCR_MODE (L1_TO_INCR_MODE):** Mode select for L1 Timeout increments: 0: time out increments are in 125us 1: L1 Timeout increments are in 256us. Refer to USB2 PORTHLPMC.L1 Timeout in XHCI Spec for additional details
18	0h RW	**Reserved (RSVD1)**
17	0h RW	**EN_DETECT_NOMINAL_PKT_EOP (EN_DETECT_NOMINAL_PKT_EOP):** 0: Detect minimal packet EOP. 1: Detect nominal packet EOP.
16	0h RW	**Disable Chirp Response (DIS_CHIRP_RESPONSE):** 0: Normal 1: Force full speed on host ports (disable chirp response)
15	0h RW	**Disable 192 Byte Limit Check (DIS_192B_LIM):** 0: Enforce 192 byte limit on complete-split INs. Treat any packet) 192 as babble case. 1: Disable 192 byte limit check.
14	0h RW	**External Provided FS/LS Disconnect (EXT_FSLS_DIS):** 0: Internal FS/LS Disconnect from linestate(1:0) 1: External provided FS/LS Disconnect from hostdisconnect input
13:12	0h RW	**UTMI Reset Source Select (UTMI_RST_SEL):** Select UTMI Reset Source (FRD UTMI Reset Only) 00: HCReset or Force PHY Reset or internal reset after disconnect/suspend for restart (default) 01,11: UTMI reset = ~UTMI suspendm 10: UTMI reset = ~UTMI suspendm and synchronization to port clk.
11	0h RW	**Disable HS Disconnect Window (DIS_HS_DIS_WIN):** 0: Enable HS Disconnect Window Function 1: Disable HS Disconnect Window Function
10	0h RW	**Disable Port Error Detection (DIS_PERR_DET):** 0: Enable Port Error Detection (default) 1: Disable Port Error Detection
9	1h RW	**Disable Peek Function for ISO-OUT (DIS_PF_IOUT):** 0: Enable Peek function for ISO-OUT (default) 1: Disable Peek function for ISO-OUT
8	1h RW	**Drive Resume-K FS/LS Serial Interface (DRV_RESK_FSLS_SER):** 0: Drive Resume-K on parallel Interface 1: Drive Resume-K directly on FS/LS Serial Interface (default)
7	1h RW	**Enable USB2 Drop-Ping (EN_U2_DROP_PING):** 0: Disable Drop-Ping Function in USB2 Protocol (default) 1: Enable Drop-Ping Function in USB2 Protocol
6	0h RW	**Enable USB2 Force-Ping (EN_U2_FORCE_PING):** 0: Disable Force-Ping Function in USB2 Protocol (default) 1: Enable Force-Ping Function in USB2 Protocol

Bit Range	Default & Access	Field Name (ID): Description
5	1h RW	**Enable USB2 Auto-Ping (EN_U2_AUTO_PING):** 0: Disable Auto-Ping Function 1: Enable Auto-Ping Function in USB2 Protocol (default)
4	0h RW	**Disable PHY SuspendM (DIS_PHY_SUSM):** 0: PHY is suspend=U3,U2,disconnect (default) 1: Disable PHY SuspendM in All States
3	0h RW	**UTMI Internal Clock Gate Disable (UTMI_INT_CG_DIS):** 0: Normal operation (internal clock gated in U2,U3,disconnect) 1: UTMI Internal Clock Gate Disable
2	0h RW	**Disable PHY SuspendM in Disconnect State (DIS_PSUSM_DS):** 0: PHY is suspendM=0 in Disconnect State (default) 1: Disable PHY SuspendM in Disconnect State
1	0h RW	**Force PHY Reset (FORCE_PHY_RST):** 0: Normal Operation (default) 1: Force PHY Reset
0	0h RW	**USB2 Accelerated Simulation Timing (U2_ACC_SIM_TIM):** 0: Normal Operation (default - FPGA/ASIC) 1: USB2 Accelerated Simulation Timing (default - simulation)

19.1.195 USB2 Port Link Control 2 (USB2_LINK_MGR_CTRL_REG2)—Offset 80F4h

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 80C40620h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Total Reset Duration[0] (TOT_RST_DUR_0):** # of microseconds for total reset duration
30:18	31h RW	**Chirp-K Duration (CHIRPK_DUR):** # of microseconds of Chirp-K to register that a device is chirping
17:5	31h RW	**K/J Disconnect Connect Delay (KJ_DIS_CON_DEL):** # of microseconds of K/J in disconnected state to register connect has occurred.
4:0	0h RW	**FS/LS Mode SE0 Disconnect Delay[12:8] (FSLS_SE0_DIS_DEL_12_8):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred.

19.1.196 USB2 Port Link Control 3 (USB2_LINK_MGR_CTRL_REG3)—Offset 80F8h

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: F865EB6Bh

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RW	**U2 Entry Ignore Linestate Changes Duration[3:0] (U2_IGN_LS_DUR_3_0):** # of microseconds after entering U2, linestate changes are ignored as bus settles
27:15	10CBh RW	**U3 Entry Ignore Linestate Changes Duration (U3_IGN_LS_DUR):** # of microseconds after entering U3, linestate changes are ignored as bus settles
14:0	6B6Bh RW	**Total Reset Duration[15:1] (TOT_RST_DUR_15_1):** # of microseconds for total reset duration

19.1.197 USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8003h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**RESERVED (RSVD)**
21:9	40h RW	**U2 Detect Remote Wake Delay (U2D_RWAKE_DEL):** #of microseconds after detecting U2 remote wake condition to reflect K
8:0	3h RW	**U2 Entry Ignore Linestate Changes Duration[12:4] (U2_IGN_LS_DUR_12_4):** # of microseconds after entering U2, linestate changes are ignored as bus settles

19.1.198 Bandwidth Calc Control (HOST_CTRL_BW_CTRL_REG)—Offset 8100h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD)**
15:0	8008h RW	**Reserved (RSVD_1)**

19.1.199 Host Interface Control (HOST_IF_CTRL_REG)—Offset 8108h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RW	**Rsvd1 (Rsvd1)**
0	1h RW	**Host IF (HOSTIF)**

19.1.200 Bandwidth Overload Burst (HOST_BW_OV_BURST_REG)—Offset 810Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8020h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**RESERVED (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
23:12	8h RW	**Per Burst Overhead System BW (PB_OVRH_SBW):** BW calculation: Overhead per burst for system BW calculations. see white paper.
11:0	20h RW	**Per Burst Overhead System BW (PB_OVRH_SSBW):** BW calculation: Overhead per burst for SS BW calculations. see white paper.

19.1.201 USB Max Bandwidth Control 4 (HOST_CTRL_BW_MAX_REG)—Offset 8128h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: F42528505647F42h

Bit Range	Default & Access	Field Name (ID): Description
63:60	0h RO	**Reserved (RSVD)**
59:48	F42h RW	**PCIe Max BW Units (PCIE_MAX_BW):** Max. Number of BW units for PCIe (system interface) (denominator in 90% calculation)
47:36	528h RW	**TT Max BW Units (TT_MAX_BW):** Max. Number of BW units for TTs. (denominator in 90% calculation)
35:24	505h RW	**FS/LS Max BW Units (FSLS_MAX_BW):** Max. Number of BW units for FS/LS ports. (denominator in 90% calculation)
23:12	647h RW	**HS Max BW Units (HS_MAX_BW):** Max. Number of BW units for HS ports. (denominator in 80% calculation)
11:0	F42h RW	**SS Max BW Units (SS_MAX_BW):** Max. Number of BW units for SS ports. (denominator in 90% calculation)

19.1.202 USB2 Linestate Debug (LINESTATE_DEBUG_REG)—Offset 8130h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**RESERVED (RSVD)**
27:26	0h RO	**Port 14 UTMI Linestate (P14_UTMI_LS)**
25:24	0h RO	**Port 13 UTMI Linestate (P13_UTMI_LS)**
23:22	0h RO	**Port 12 UTMI Linestate (P12_UTMI_LS)**
21:20	0h RO	**Port 11 UTMI Linestate (P11_UTMI_LS)**
19:18	0h RO	**Port 10 UTMI Linestate (P10_UTMI_LS)**
17:16	0h RO	**Port 9 UTMI Linestate (P9_UTMI_LS)**
15:14	0h RO	**Port 8 UTMI Linestate (P8_UTMI_LS)**
13:12	0h RO	**Port 7 UTMI Linestate (P7_UTMI_LS)**
11:10	0h RO	**Port 6 UTMI Linestate (P6_UTMI_LS)**
9:8	0h RO	**Port 5 UTMI Linestate (P5_UTMI_LS)**
7:6	0h RO	**Port 4 UTMI Linestate (P4_UTMI_LS)**
5:4	0h RO	**Port 3 UTMI Linestate (P3_UTMI_LS)**
3:2	0h RO	**Port 2 UTMI Linestate (P2_UTMI_LS)**
1:0	0h RO	**Port 1 UTMI Linestate (P1_UTMI_LS)**

19.1.203 USB2 Protocol Gap Timer (USB2_PROTOCOL_GAP_TIMER_REG)—Offset 8134h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: C3C640C05140Ch

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RO	**Reserved (RSVD)**
55:48	Ch RW	**GAP time after LS TX thru FS hub (LSTX_GAP_TIME)**

Bit Range	Default & Access	Field Name (ID): Description
47:40	3Ch RW	**GAP time after LS RX thru FS hub (LSRX_GAP_TIME)**
39:32	64h RW	**GAP timer after LS (LS_GAP_TIME)**
31:24	Ch RW	**GAP time after FS (FS_GAP_TIME)**
23:16	5h RW	**GAP time after HS RX (HSRX_GAP_TIME)**
15:8	14h RW	**GAP time after HS TX SOF (HSTXSOF_GAP_TIME)**
7:0	Ch RW	**GAP time HS TX Packet (HSTX_GAP_TIME)**

19.1.204 USB2 Protocol Bus Timeout Timer (USB2_PROTOCOL_BTO_TIMER_REG)—Offset 813Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8D4258B8h

Bit Range	Default & Access	Field Name (ID): Description
31:21	46Ah RW	**Bus timeout count for LS (LS_BUS_TO)**
20:10	96h RW	**Bus timeout count for FS (FS_BUS_TO)**
9:0	B8h RW	**Bus timeout count for HS (HS_BUS_TO)**

19.1.205 Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: A019132h

Bit Range	Default & Access	Field Name (ID): Description
31:24	Ah RW	**Engine Idle Hysteresis (EIH):** This register controls the min. idle span that has to be observed from the engine idle indicators before the power state flags (xhc_*_idle) will indicate a 1.

Bit Range	Default & Access	Field Name (ID): Description
23:12	19h RW	**Backbone PLL Shutdown Advance Wake (BPSAW):** This register controls the time before the next scheduled transaction where the Backbone PLL request will assert. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)
11:0	132h RW	**Backbone PLL Shutdown Min. Idle Duration (BPSMID):** The sum of this register plus the Backbone PLL Shutdown Advance Wake form to a Total Idle time. When the next scheduled periodic transaction is after present time + Total Idle, the Backbone PLL request will de-assert, allowing the PLL to shutdwon. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)

19.1.206 Power Scheduler Control-2 (PWR_SCHED_CTRL2)—Offset 8144h

These bit enable by EP type those EPs classes that are considered for determining next periodic active interval for pre-wake of the periodic_active signal. EP classes that are disabled may never be observed in setting of the periodic_active signal.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 33Fh

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved (RSVD)**
9	1h RW	**HS Interrupt-OUT Alarm (HS_INT_OUT_ALRM)**
8	1h RW	**HS Interrupt-IN Alarm (HS_INT_IN_ALRM)**
7	0h RW	**SS Interrupt-OUT FC Alarm (SS_INT_OUT_FC_ALRM)**
6	0h RW	**SS Interrupt-IN Alarm (SS_INT_IN_FC_ALRM)**
5	1h RW	**SS Interrupt-OUT & not in FC Alarm (SS_INT_OUT_ALRM)**
4	1h RW	**SS Interrupt-IN & not in FC Alarm (SS_INT_IN_ALRM)**
3	1h RW	**HS ISO-OUT Alarm (HS_ISO_OUT_ALRM)**
2	1h RW	**HS ISO-IN Alarm (HS_ISO_IN_ALRM)**
1	1h RW	**SS ISO-OUT Alarm (SS_ISO_OUT_ALRM)**

Bit Range	Default & Access	Field Name (ID): Description
0	1h RW	**SS ISO-IN Alarm (SS_ISO_IN_ALRM)**

19.1.207 AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 81390206h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**DIS_L1P2_EXIT_ON_WAKE_EN (DIS_L1P2_EXIT_ON_WAKE_EN):** This bit disables the dependency on Wake Enables defined in PORTSC for L1P2 exit when in D0
30:28	0h RW	**RESERVED0 (RSVD0)**
27:25	0h RW	**RESERVED (RSVD)**
24	1h RW	**Enable L1 exit notification to SNPS PCIe core (EN_L1_EXIT_NOTIF_PCIE):** This bit enables a L1 exit notification to SNPS PCIe core. There is a case where USB ports have waked up and AUX PM module has started the wakeup process. The AUX PM control state got into a wait for P0 state because it needs to wait until PCie core to signal powerdown state change. Due to the fact that the core is in D3Hot, there is no run_stop bit set such that no internal interrupt will be fired. This causes the LTSSM of PCIe stayed in L1 even though AUX PM has known that it needs an L1 exit. This bit works together with bit21 of this register. 1: enables this feature 0: disables this feature.
23	0h RW	**DISABLE PLC ON DISCONNECT (DIS_PLC_ON_DISCONNECT):** 1: do not assert PLC for disconnection 0: assert PLC for disconnection
22	0h RW	**TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2 (TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2):** This bit enables a feature in PCie core LTSSM to treat IDLE received as TS2 when LTSSM is in wait for TS2 receive state. This is a function requested from PHY where it is possible to not able to receive TS2 without error. 1: treat Logic IDLE as TS2 received when in some PCIe LTSSM state. 0: disable this feature.

Bit Range	Default & Access	Field Name (ID): Description
21	1h RW	**Disable p2 overwrite due to the D3HOT where PCIe core enters the L1 (DIS_P2_OVERWRITE_DUE2_D3HOT):** We added a feature where if PCIe core LTSSM enters L1 due to the D3hot, the aux PM control will not start a P2 overwrite function in anticipating for the next L23 enter. 1: disables p2 overwrite due to the D3HOT where PCIe core enters the L1. 0: enables P2 overwrite even if we are in D3Hot.
20	1h RW	**Enable the port to enter U3 automatically when in U1/U2 (ENABLE_AUTO_U3_ENTRY_FROM_U2_U3):** 1: enables the port to enter U3 automatically when in U1/U2 0: disables the port to enter U3 automatically when in U1/U2
19	1h RW	**No linkdown reset is issue during low power state (DIS_LINKDOWN_RST_DURING_LOW_POWER):** No linkdown reset is issue during low power state
18	0h RW	**EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0 (EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0):** This bit enables a feature in AUX PM module where if PCIe core LTSSM is in P0 for a duration of time, we will exit the deep sleep state. This is for failure control in case. 1: enables this feature 0: disable this feature
17	0h RW	**U2_EXIT_LFPS_TIMER_VALUE (U2_EXIT_LFPS_TIMER_VALUE):** This bit selects U2 exit LFPS timer value 0: 320ns 400ns in 25MHz domain 1: 240ns 320ns in 25MHz domain
16	1h RW	**EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP (EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP):** This bit enables a function that AUX PM module exits from the deep sleep state due to the USB ports wakeup level signal. We have added this feature where USB ports will generated a wakeup level signal to wakeup the AUX PM module if it is in deep sleep state and this level signal will be cleared if the change bits are updated by software. 1: enables this function 0: disables this function which means that a wakeup pulse generated from each USB PortSC event will wake up the AUX PM module from deep sleep if the D3 state is programmed.
15:14	0h RW	**P3_ENTRY_TIMEOUT (P3_ENTRY_TIMEOUT):** This field defines the timeout value to enter P3 mode in U2. 00: 7us 8us 01: 511us 512us 10: disables the timer (0us) 11: disables the timer (0us)
13	0h RW	**Enable U2 P3 Mode (EN_U2_P3):** 0: Disable U2 P3 mode 1: Enable U2 P3 mode
12:11	0h RW	**Fine Debug Mode Select (FINE_DM_SEL)**
10	0h RW	**Enable Low Power State Based Core Clock Gating (EN_LP_CORE_CG):** When set to '1' enable core clock gating based on low power state entered

Bit Range	Default & Access	Field Name (ID): Description
9	1h RW	**Disable USB3 Port Status Changed Event (DIS_U3_PORT_SCE):** 0: Enable USB3 port status change event generation if any change bit is not cleared 1: Disable USB3 port status change event generation if any change bit is not cleared Bit 12 default 0
8:4	0h RW	**Debug Mode Select Register (DEB_MODE_SEL)**
3	0h RW	**Enable Auto Wakeup Non-IDLE (EN_AWAK_NIDLE):** When set to 1 enables the auto wakeup function when engine has identified non IDLE condition.
2	1h RW	**Enable PM Control P1 Exit P2 (EN_PMC_P1_EXIT_P2):** When set 1 enables the PM control module to transition to P1 instead of P0 when exit P2.
1	1h RW	**Enable PCIe PIPE CLK Isolation (EN_PP_CLK_ISOL):** When set to 1 enables the PCIe PIPE CLK to be isolated when main power is removed.
0	0h RW	**Enable P2 Overwrite P1 Allowed Detect (EN_P2OVRP1_ADET):** When set to 1 enables a function that can detect whether or not enable P2 overwrite P1 function. The condition to get to P2 overwrite is when engine is in idle conditions. This means that there is no ISO EP pending.

19.1.208 USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: FCh

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD)**
7	1h RW	**EN_CMDM_TXRXB (EN_CMDM_TXRXB):** Enable Command Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
6	1h RW	**EN_TTE_TXRXB (EN_TTE_TXRXB):** Enable TTE Active indication for Tx/Rx Bias circuit HS Phy PM Policy
5	1h RW	**EN_IDMA_TXRXB (EN_IDMA_TXRXB):** Enable IDMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
4	1h RW	**EN_ODMA_TXRXB (EN_ODMA_TXRXB):** Enable ODMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
3	1h RW	**EN_TRM_TXRXB (EN_TRM_TXRXB):** Enable Transfer Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW	**EN_SCH_TXRXB (EN_SCH_TXRXB):** Enable Scheduler Active indication for Tx/Rx Bias circuit HS Phy PM Policy
1	0h RW	**Enable Rx Bias ckt disable (EN_RXB_CD):** When set enables the Rx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)
0	0h RW	**Enable Tx Bias ckt disable (EN_TXB_CD):** When set enables the Tx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)

19.1.209 USB Power Gating Control (USB_PGC)—Offset 8168h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 282EEh

Bit Range	Default & Access	Field Name (ID): Description
31:1	14177h RO	**Reserved (RSVD)**
0	0h RW	**USB SRAM power gating enable (USB_SRAM_PGE):** When set enables power gating on USB ports. Usage of this bit is further qualified with xHCI SRAM Dynamic Power Gating Disable fuse. If the fuse disables dynamic power gating, setting this bit to 1 shall not enable power gating feature. This bit always returns the value that was written to it irrespective of the setting of xHCI SRAM Dynamic Power Gating Disable fuse.

19.1.210 xHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 400h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved (RSVD)**
19	0h RW	**USB3 Partition Engine/Link trunk gating Enable (PARUSB3_ENG_GEN):** When set to 1 enables gating of the SOSC trunk to the XHCI engine and link in the PARUSB3 partition.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**USB3 Partition Frame Timer trunk gating Enable (PARUSB3_LINK_GEN):** When set to 1 enables gating of the SOSC trunk to the Frame timer in the PARUSB3 partition.
17	0h RW	**USB2 link partition clock gating enable (PARUSB2_CLK_GEN):** When set to 1 enables gating of the SOSC trunk to the USB2 link and Phy logic in the PARUSB2 partition.
16	0h RW	**USB2/USHIP 12.5 MHz partition clock gating enable (USHIP_PCGEN):** When set to 1 enables gating of the 12.5 MHz SOSC trunk to the USB2 and USHIP logic in the PARUSB2 partition.
15	0h RO	**Reserved1 (RSVD1):** Reserved
14	0h RW	**USB3 Port Aux/Core clock gating enable (USB3_AC_CGE):** When set, allows the aux_cclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
13:12	0h RW	**Rx Detect Timer when port Aux Clock is Gated (RX_DT_ACG):** This field defines the value of the timer used to perform Rx Detect when port Aux Clock has been gated. 0x0: 100ms 0x1: 12ms Others: Reserved Note: This timer shall use the Fast Training Timer Tick (about 1us tick) for simulation purposes. For Fast Training mode, the above timeouts will become about 11us and about 100us, +/- implementation uncertainty, respectively.
11:8	4h RW	**U2 Residency Before ModPHY Clock Gating (U2R_BM_CG):** Before gating ModPHY Aux clock, Host Controller shall wait for this time in U2. This time is meant to ensure that the attached device has entered U2 as well. 0x0: 1us 0x1: 128us 0x2: 256us 0x3: 512us 0x4: 640us 0x5: 768us 0x6: 896us 0x7: 1024us Others: Reserved Note: This counter shall start counting once pipe has entered PS3 state in response to link in U2.
7	0h RW	**Frame Timer Clock Gating Ports in U2 Enable (FTCGPU2E):** This bit, when set, allows Host Controller to gate the clock to the Frame Timer when ports are in U2.
6	0h RW	**USB2 port clock throttle enable (USB2_PC_TE):** When set, allows the Aux clock into the USB2 ports to be throttled when conditions allow.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**XHCI Engine Aux clock gating enable (XHCI_AC_GE):** When set, allows the aux clock into the XHCI engine to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
4	0h RW	**XHCI Aux PM block clock gating enable (XHCI_APMB_CGE):** When set, allows the aux clock into the Aux PM block to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
3	0h RW	**USB3 Aux Clock Trunk Gating Enable (USB3_AC_TGE):** When set, allows Aux Clock Trunk feeding to USB3.0 ports to be gated when port Aux clock is gated at all USB3.0 ports and all USB3.0 modPHY instances. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
2	0h RW	**USB3 Port Aux/Port clock gating enable (USB3_AP_CGE):** When set, allows the aux_pclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
1	0h RW	**ModPHY port Aux clock gating enable in U2 (MPP_AC_GEU2):** When set, allows the aux clock into the ModPhy to be gated when Link is in U2 and pipe has been in PS3 for at least the time defined by U2 Residency Before ModPHY Clock Gating field. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
0	0h RW	**ModPHY port Aux clock gating enable in Disconnected, U3 or Disabled (MPP_AC_GE_DDU3):** When set, allows the aux clock into the ModPHY to be gated when Link is in Disconnected, U3 or Disabled state. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.

19.1.211 USB LPM Parameters (USB_LPM_PARAM)—Offset 8170h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 96090032h

Bit Range	Default & Access	Field Name (ID): Description
31:22	258h RW	**USB2_LPM_REG_RSM_U3_DET_NORM (USB2_LPM_REG_RSM_U3_DET_NORM)**
21:19	1h RW	**Min U3 Exit LFPS Duration (MIN_U3E_LFPS_D):** Min U3 Exit LFPS Duration This field defines the minimum duration of LFPS driven by Host Controller upon U3 exit LFPS handshake. Note that theres an uncertainty of +-16us in actual duration driven by the Host Controller. 0b000: 96us 0b001: 160us 0b010: 224us 0b011: 288us 0b100: 352us 0b101: 416us 0b110: 480us 0b111: 544us
18:16	1h RW	**Min U2 Exit LFPS Duration (MIN_U2_ELFPS_D):** Min U2 Exit LFPS Duration This field defines the minimum duration of LFPS driven by Host Controller upon U2 exit LFPS handshake. Note that theres an uncertainty of +-16us in actual duration driven by the Host Controller. 0b000: 96us 0b001: 160us 0b010: 224us 0b011: 288us 0b100: 352us 0b101: 416us 0b110: 480us 0b111: 544us
15	0h RW	**Max PING LFPS Rx Detection (XHCI_MAX_PING_LFPS):** This field defines the maximum timing for PING LFPS. If an incoming LFPS will be considered a PING if it has a timing such that it is less than or equal to the selected value. Otherwise it will be considered for the other types of LFPS. 0b Max PING LFPS timing set to 256 ns (32 link clocks) 1b Max PING LFPS timing set to 320 ns (40 link clocks)
14:10	0h RO	**Reserved (RSVD_1)**
9:0	32h RW	**xHCI BESL to HIRD Distance (XHCI_BESL_HIRD_DT):** This field defines the gap between BESL and duration of Resume signalling from Host upon Host Initiated Resume from USB2.0 LPM. Default value of this register corresponds to xHCI spec defined 50us value. Value BESL to HIRD Distance 000h 0us 001h 1us 002h 2us 3FFh 1023us

19.1.212 xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1)—Offset 8174h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40047Dh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Disable scheduler direct transition from IDLE to NO requirement (DIS_SDT_IDL_NR):** 0: (default) allow scheduler direct transition from IDLE to NO requirement 1: Disable scheduler direct transition from IDLE to NO requirement
30:26	0h RW	**Reserved (RSVD)**
25	0h RW	**XHCI LTR Transition Policy (XLTRTP):** When '0', LTR messaging state machine transitions from High, Medium, or Low LTR states to Active state upon the Alarm Timer timout and stays in Active until the next service boundary. When '1', the LTR messaging state machine transitions through High ? Med ? Low ? Active states assuming enough latency is available for each transition.
24	0h RW	**XHCI LTR Enable (XLTRE):** This bit must be set to enable LTV messaging from XHCI to the PMC.
23:12	400h RW	**Periodic Active LTV (PA_LTV):** 23:22 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 21:12 Latency Value (ns) Defaults to 0 micro seconds
11:0	47Dh RW	**USB2 Port L0 LTV (USB2_PL0_LTV):** 11:10 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 9:0 Latency Value (ns) Defaults to 128 Micro Seconds

19.1.213 xHC Latency Tolerance Parameters LTV Control 2 (XLTP_LTV2)—Offset 8178h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 17FFh

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
12:0	17FFh RW	**LTV Limit (LTV_LMT):** This register defines a maximum LTR value that is allowed to be advertised to the PMC. This is meant to be used as a workaround or mitigation if issues are discovered with the LTR values generated by the XHC using the defined algorithms. If the LTR value of the XHC is larger than the value in this register field, the value in this field is sent to the PMC instead. Default value is the highest possible - 101b 12:10: Latency Multiplier Field 000b - Value times 1 ns 001b - Value times 32 ns 010b - Value times 1,024 ns 011b - Value times 32,768 ns 100b - Value times 1,048,576 ns 101b - Value times 33,554,432 ns 110b-111b - Not Permitted 9:0: Latency Value Default = 3FFh

19.1.214 xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC)—Offset 817Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD)**
28:16	0h RW	**Minimum High Idle Time (MHIT):** This is the minimum schedule idle time that must be available before a "High" LTR value can be indicated. This value must be larger than HIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	**Reserved (RSVD_1)**
12:0	0h RW	**High Idle Wake Latency (HIWL):** This is the latency to access memory from the High Idle Latency state. This value must be larger than MIWL and LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

19.1.215 xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC)—Offset 8180h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD)**
28:16	0h RW	**Minimum Medium Idle Time (MMIT):** This is the minimum schedule idle time that must be available before a "Medium" LTR value can be indicated. This value must be larger than MIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	**Reserved (RSVD_1)**
12:0	0h RW	**Medium Idle Wake Latency (MIWL):** This is the latency to access memory from the Medium Idle Latency state. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

19.1.216 xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD)**
28:16	0h RW	**Minimum Low Idle Time (MLIT):** This is the minimum schedule idle time that must be available before a "Low" LTR value can be indicated. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	**Reserved (RSVD_1)**
12:0	0h RW	**Low Idle Wake Latency (LIWL):** This is the latency to access memory from the Medium Idle Latency state. 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

19.1.217 HOST_CTRL_BW_MAX3_REG (HOST_CTRL_BW_MAX3_REG)—Offset 8188h

Added for CHV

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: F42F42h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Rsvd (Rsvd)**
23:0	F42F42h RW	**MAX_OUT_BW_UNITS_FOR_SS_PORTS (MAX_OUT_BW_UNITS_FOR_SS_PORTS):** Max. Number of OUT BW units for SS ports - denominator in 90% calculation

19.1.218 PDDIS_REG (PDDIS_REG)—Offset 8198h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Rsvd (Rsvd)**
7:0	0h RW	**PDDISEN (PDDISEN)**

19.1.219 THRM_HOST_CTRL_REG (THRM_HOST_CTRL_REG)—Offset 819Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RW	**Rsvd (Rsvd)**
20	0h RW	**Rsvd**

Bit Range	Default & Access	Field Name (ID): Description
19:18	0h RW	**USB3 Thermal Throttle Ux LGO delay (USB3_THRM_UX_LGO_DELAY):** Controls the delay enforced between LMP for FLPMA and LMP for Ux LGO. After sending LPMA ON , wait for pre-defined number of clocks to initiate LGO_U1/ LGO_U2 00: 8 clocks 01: 32 clocks 10: 128 clocks 11: 0 clocks This field does not apply to ports that are not operating in the mode required to issue FLMA ON.
17	0h RW	**THRM_THROTTLING_DISABLE (THRM_THROTTLING_DISABLE):** 0: Thermal throttling is enabled. 1: Thermal throtling is disabled. The host controller ignores the TT control inputs and does not throttle.
16	0h RW	**USB3 Thermal Throttle Ux Mapping (USB3_THRM_UX_MAPPING):** Controls if U1 or U2 is forced upon the start of thermal throttle OFF period. 0 Force ports into U2 during Thermal Throttle triggered Ux entry. 1 Force ports into U1 during Thermal Throttle triggered Ux entry.
15	0h RW	**THROTTLE_PRIORITY_MODE (THROTTLE_PRIORITY_MODE):** 0: Off period has priority: In this case, when the throttle signal is asserted, the host controller enters the off state on the next uframe boundary, and stays in the off state for the prescribed duration or until the end of the 16 uframe throttle period whichever occurs first. On subsequent throttle periods, the off period occurs first and then the on period. 1: The On period has priority: In this case, when the throttle signal is asserted, the host controller completes the required On period first before entering the off period. If the required number of uFrames has already been executed in a 16 uframe throttle window, the controller enters the off period immediately.
14	0h RW	**DISABLE_FORCE_L1_WHEN_THROTTLED (DISABLE_FORCE_L1_WHEN_THROTTLED):** 0: USB2 port will not force L1 entry on throttled ports. L1 entry will be based on the normal idle timeout 1: USB2 ports will attempt to enter L1 immediately after throttled ports are idle.
13	0h RW	**DISABLE_INTERRUPT_THROTTLING (DISABLE_INTERRUPT_THROTTLING):** 0: Interrupt traffic is throttled 1: Interrupt traffic is not throttled
12	0h RW	**DISABLE_ISOCHRONOUS_THROTTLING (DISABLE_ISOCHRONOUS_THROTTLING):** 0: Isochronous traffic is throttled 1: Isochronous traffic is not throttled
11:8	0h RW	**T1_ACTION (T1_ACTION):** # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15.
7:4	0h RW	**T2_ACTION (T2_ACTION):** # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15.
3:0	0h RW	**T3_ACTION (T3_ACTION):** # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15.

19.1.220 LFPS_PM_CTRL_REG (LFPS_PM_CTRL_REG)—Offset 81A0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Rsvd (Rsvd)**
6:0	0h RW	**LFPS_PM_EN (LFPS_PM_EN)**

19.1.221 U2PDM (U2PDM)—Offset 81A4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Rsvd (Rsvd)**
7:0	0h RW	**U2PDM (U2PDM)**

19.1.222 U2PCM (U2PCM)—Offset 81A8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Rsvd (Rsvd)**
7:0	0h RW	**U2PCM (U2PCM)**

19.1.223 U3PDM (U3PDM)—Offset 81ACh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Rsvd (Rsvd)**
6:0	0h RW	**U3PDM (U3PDM)**

19.1.224 U3PCM (U3PCM)—Offset 81B0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Rsvd (Rsvd)**
6:0	0h RW	**U3PCM (U3PCM)**

19.1.225 THRM_HOST_CTRL_REG2 (THRM_HOST_CTRL_REG2)—Offset 81B4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 7Fh

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Rsvd (Rsvd)**
6:0	7Fh RW	**Force LPM Accept Enable (FORCE_LPM_ACCEPT_EN):** Per Port Control to allow for enforcement to be based on device detection if certain devices do not support FLPMA. 0: Do not set FLPMA prior to Ux entry due to TT 1: Set FLPMA prior to Ux entry due to TT

19.1.226 LFPSONCOUNT_REG (LFPSONCOUNT_REG)—Offset 81B8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 20C8h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Rsvd (Rsvd)**
17:16	0h RW	**U2P3 LFPS Periodic Sampling Control (XU2P3LPSC):** This field controls the OFF time for the LFPS periodic sampling for SS port in U2P3. If LFPSPM for a port is 1, it will override the OFF time and LFPS receiver will remain OFF permanently. For Fast Sim mode, 500us will be equivalent to 5us. 0x0 Polling Disable. (RXDET Polling will become 100ms.) 0x1 500us OFF Time 0x2 1ms OFF Time 0x3 1.5ms OFF Time
15:10	8h RW	**RSVD**
9:0	C8h RW	**XLFPSONCNTSS (XLFPSONCNTSS):** This time would describe the number of clocks LFPS will remain ON. LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 200.

19.1.227 (D0i2_CTRL_REG)—Offset 81BCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 84204B0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved (RSVD)**
29:26	2h RW	**D0i2 Minimum Residency (D0I2_MIN_RESIDENCY):** This field controls the minimum time that we must stay in D0i2 to ensure that the entry sequence has settled before we attempt to exit. 0h Disabled 1h 8 clocks 2h 16 clocks 3h 32 clocks 4h 128 clocks 5h 256 clocks 6h 512 clocks 7h 1024 clocks

Bit Range	Default & Access	Field Name (ID): Description
25:22	1h RW	**D0i2 Entry Hysteresis Timer (D0I2_ENTRY_HYSTERESIS_TIMER):** This field allows for a hysteresis timer to be implemented specifically for D0i2. This will allow for D0i2 entry to be controlled independently from the timer used for D0i3 and D3. 0h Disabled 1h 8 clocks 2h 16 clocks 3h 32 clocks 4h 64 clocks 5h 128 clocks 6h 256 clocks 7h 512 clocks
21	0h RW	**Active Periodic EP Disable (ACTIVE_PERIODIC_EP_DISABLE):** This field allows the xHC to control how aggressive it enters D0i2 in the presence of active Periodic EPs. Setting this field will allow D0i2 only when there are no active Periodic EPs on the schedule. Either there are no active DB or any active Interrupt EP is flow controlled.
20:16	2h RW	**MSI D0i2 Pre Wake Time (MSID0I2PWT):** This is the latency that is expected to be incurred to exit the D0i2 state. This wake latency is the latency to be added to the tracked D0i2 wake by the MSI module. Example: If while allowing D0i2 there is an MSI generation that will trigger in 250 us from now ,the MSI module will trigger a D0i2 wake up 250 us MSI D0i2 Pre Wake Time. The D0I2WL is to ensure that the act of D0i2 exit does not impact the action(s) required by the alarm(s) that was enabled prior to D0i2. 3:0 250 ns ticks 0h 0 ns 1h 250 ns . 1Fh 3750 ns
15:4	4Bh RW	**MSI Idle Threshold (MSI_IDLE_THRESHOLD):** This field allows the xHC to control how aggressive it enters D0i2 in the presence of pending MSI. This field is valid only if Pending MSI Disable is 0, allowing D0i2 in the presence of pending MSIs. D0i2 will be prevented if the amount of idle time between Event Ring being idle to the time an MSI will be generated does not exceed this time. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)
3	0h RW	**Pending MSI Disable (PENDING_MSI_DISABLE):** This field allows the xHC to disable D0i2 when there are pending MSIs in the event manager. Setting this field will require all IMOD counters to be 0h and all MSIs delivered. Clearing this field will allow for D0i2 power gating while there are 1 or more IMOD counters decrementing which implies that an MSI is pending and will be generated once the corresponding IMOD counter reaches 0h.
2	0h RW	**Frame Timer Run Disable (FRAME_TIMER_RUN_DISABLE):** This field allows the xHC to disable D0i2 when the frame timer is running. Clearing this field will allow D0i2 when the frame timer is required as defined in the XHCI Spec. Setting this field will not allow D0i2 when the frame timer is required and will limit D0i2 for the condition where the frame timer is not required.
1	0h RW	**USB2 L1 Disable (USB2_L1_DISABLE):** This field allows the xHC to disable D0i2 when USB2 ports are in L1. This implies that D0i2 will only be triggered when ports are in L2 or deeper.
0	0h RW	**USB3 U2 Disable (USB3_U2_DISABLE):** This field allows the xHC to disable D0i2 when USB3 ports are in U2. This implies that D0i2 will only be triggered when ports are in U3 or deeper.

19.1.228 (D0i2_SCH_ALARM_CTRL_REG)—Offset 81C0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved (RSVD)**
28:16	0h RW	**D0i2 Idle Time (D0I2IT):** This is the minimum schedule idle time that must be available before D0i2 can allowed. 12:7 Time value in # of 125s Bus Intervals (0 8ms) 6:0 Fractional BI Time value in s (0 124s) This field controls how much scheduler idle time is required to trigger D0i2. The scheduler idle time is the same idle time that is used by other functions implementing alarm timers such as PLL shutdown, LTR and USB2 L1 override. If there is a need to require other alarm timers to have been set such as LTR has triggered a Low Idle time, then this field needs to be as aggressive as LTR Low Min Idle Time to ensure D0i2 is triggered once the scheduler has detected IDLE in the schedule. This is only to be used as alternate modes of operation or back up modes.
15:13	0h RO	**Reserved (RSVD1)**
12:0	0h RW	**D0i2 Wake Latency (D0I2WL):** This is the latency that is expected to be incurred to exit the D0i2 state. This wake latency is the latency to be added to the tracked D0i2 wake by the scheduler. Example: If while allowing D0i2 there is an alarm that will trigger in 250 us from now , the scheduler will allow D0i2 and track this alarm with an adjustment to wake up 250ns D0I2WL) from. The D0I2WL is to ensure that the act of D0i2 exit does not impact the action(s) required by the alarm(s) that was enabled prior to D0i2. 12:7 Time value in # of 125s Bus Intervals (0 8ms) 6:0 Fractional BI Time value in s (0124s)

19.1.229 (USB2PMCTRL_REG)—Offset 81C4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2PSPGPSCBP):** This controls the policy for blocking PORTSC Updates while the USB2 PHY SUS Well is power gated. When set, the controller will block any updates to the PORTSC caused by port status change if the USB2 PHY SUS is power gated. 0 Do not
10:8	0h RW	**USB2 PHY SUS Well Power Gate Entry Hysteresis Count (U2PSPGEHC):** This controls the amount of hysteresis time the controller will enforce after detecting the USB2 PHY SUS Power Gate entry condition. 0h 0 clocks 1h 32 clocks 2h 64 clocks 3h 128 clocks 4h 256 clocks 5h 512 clocks 6h 1024 clocks 7h 2048 clocks
7:4	0h RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2CLPGLAT):** This field represents the worst case latency for the USB2 Common Lane to enter and exit its power gate state. This fields is required to be compared to a ports HIRD/HIRD value for the ports that have allowed L1 to L2 mapping to determine if the Common Lane can be allowed to power off. If the power gate entry/exit latency is greater than the HIRD/HIRDD then the common lane should not be allowed to power gate as this will result in a L1 exit violation. 0h 100 us 1h 200 us 2h 300 us Eh 1500us Fh 1600 us
3:2	0h RW	**USB2 PHY SUS Well Power Gate Policy (U2PSUSPGP):** This field controls when to enable the USB2 PHY SUS Well Power Gating when the proper conditions are met. 00 USB2 PHY SUS Power Gating is Disabled. 01 USB2 PHY SUS Power Gating is Enabled in Only D0 and D0i2 (Excludes D0i3 and D3) 10 USB2 PHY SUS Power Gating is Eanabled in only in D0, D0i2 and D0i3 (Excludes D3) 11 USB2 PHY SUS Power Gating is Eanabled in D0/ D0i2/D0i3/D3
1	0h RW	**USB2 Common Lane Power Gating Enable During L1 to L2 Mapping for USB2 PHY Power Gating (U2CLPGEL1L2):** This field when set enables the controller to allow for the common lane power gating to be enabled when all ports are exposed as in L2 to the USB2 PHY while at least 1 port has been mapped to L2 from L1. This field alone does not guarantee power gating since the L1 HIRD/HIRDD Value must be compared with the PHYs power gate exit latency (U2CLPGLAT) held in this register to ensure that L1 exit is not violated. 0 USB2 Common Lane Power Gating is disabled when any port has been mapped from L1 to L2. 1 USB2 Common Lane Power Gating is allowed when any port has been mapped to L2 from L1 with the additional condition that the HIRD/ HIRDD is greater than the PHYs Power Gate exit latency.
0	0h RW	**USB2 Data Lane L1 to L2 Mapping Enable for USB2 PHY Power Gating (U2DLL1L2ME):** This field when set enables the controller to map an L1 entry directly to L2 to allow the USB2 PHY to trigger its Autonomous Power Gating. The USB2 PHY will trigger PG only when in L2 since it does not fully understand the requirements for L1. 0 USB2 L1 to L2 mapping is disabled for all ports 1 USB2 L1 to L2 mapping is enabled for all ports

19.1.230 ECC_PARITY_ERROR_LOG_REG (ECC_PARITY_ERROR_LOG_REG)—Offset 83F8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**COMMAND_PARITY_DETECTED (COMMAND_PARITY_DETECTED):** Command Parity Error detected on received IOSF transaction
30	0h RW/1C	**DATA_PARITY_DETECTED (DATA_PARITY_DETECTED):** Data Parity Error detected on received IOSF transaction
29	0h RW/1C	**ERROR_PRESENT_DETECTED (ERROR_PRESENT_DETECTED):** Error present detected on received IOSF transaction
28:26	0h RO	**RSVD (RSVD):** Reserved
25:21	0h RW/1C	**Correctable ECC Error Source RF (CORRECTABLE_ECC_ERROR_SOURCE_RF):** When set indicates the specific RF the ECC Error was detected on. This is used along with the ECC Source, and Port Info to determine the specific RF on which Correctable ECC Error was seen on. USB2 Port RF: 00000: Reserved 00001: Async. TX Payload 00010: Periodic TX Payload 00011: RX Payload 00100: TTE Periodic TX Payload 00101: TTE RX Payload Others: Reserved USB3 Port RF: 00000: Reserved 00001: Async TX Payload 00010: Periodic TX Payload 00011: RX Payload Others: Reserved XHCI Engine RF: 00000: Reserved 00001: TTE Context 00010: TRM Context 00011: XHCI Completion Collect 00100: Debug Device Completion Collect 00101: DBC-EXI Trace Data
20:15	0h RW/1C	**CORRECTABLE_ECC_ERROR_SOURCE_PORT (CORRECTABLE_ECC_ERROR_SOURCE_PORT):** When set indicates the Port# if the ECC Error was detected on any of the USB2/USB3 Port RFs. This is valid only when bit[1:0] != 00
14:13	0h RW/1C	**CORRECTABLE_ECC_ERROR_SOURCE_LOG (CORRECTABLE_ECC_ERROR_SOURCE_LOG):** When an Correctable ECC is detected for an RF, the corresponding bit is set to '1' 11: Detected Uncorrectable ECC Error on USB3 RFs 10 : Detected Uncorrectable ECC Error on USB2 RFs 01: Detected Uncorrectable ECC Error on XHCI Engine RFs 00 : No Error Note: On detection of first Uncorrectable ECC Error HW shall lock the Correctable log registers (Source, Port, RF) until SW clears the ECC Error log or cleared by reset.

Bit Range	Default & Access	Field Name (ID): Description
12:8	0h RW/1C	**UNCORRECTABLE_ECC_ERROR_SOURCE_RF (UNCORRECTABLE_ECC_ERROR_SOURCE_RF):** When set indicates the specific RF the ECC Error was detected on. This is used along with the ECC Source, and Port Info to determine the specific RF on which uncorrectable ECC Error was seen on. USB2 Port RF: 00000: Reserved 00001: Async. TX Payload 00010: Periodic TX Payload 00011: RX Payload 00100: TTE Periodic TX Payload 00101: TTE RX Payload Others: Reserved USB3 Port RF: 00000: Reserved 00001: Async TX Payload 00010: Periodic TX Payload 00011: RX Payload Others: Reserved XHCI Engine RF: 00000: Reserved 00001: TTE Context 00010: TRM Context 00011: XHCI Completion Collect 00100: Debug Device Completion Collect 00101: DBC-EXI Trace Data
7:2	0h RW/1C	**UNCORRECTABLE_ECC_ERROR_SOURCE_PORT (UNCORRECTABLE_ECC_ERROR_SOURCE_PORT):** When set indicates the Port# if the ECC Error was detected on any of the USB2/USB3 Port RFs. This is valid only when bit[1:0] != 00
1:0	0h RW/1C	**UNCORRECTABLE_ECC_ERROR_SOURCE_LOG (UNCORRECTABLE_ECC_ERROR_SOURCE_LOG):** When an uncorrectable ECC is detected for an RF, the corresponding bit is set to '1' 11: Detected Uncorrectable ECC Error on USB3 RFs 10 : Detected Uncorrectable ECC Error on USB2 RFs 01: Detected Uncorrectable ECC Error on XHCI Engine RFs 00 : No Error Note: On detection of first Uncorrectable ECC Error HW shall lock the Uncorrectable log registers (Source, Port, RF) until SW clears the ECC Error log or cleared by reset.

19.1.231 ECC_POISONING_CTRL_REG (ECC_POISONING_CTRL_REG)—Offset 83FCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RW	**ENGINE_RF_ECC_POISONING_VECTOR (ENGINE_RF_ECC_POISONING_VECTOR):** XHCI Engine RFs ECC Poisoning Inversion bits for the 64b or 128bit based on RF width
22:14	0h RW	**USB3_RF_ECC_POISONING_VECTOR (USB3_RF_ECC_POISONING_VECTOR):** USB3 RFs ECC Poisoning Inversion bits for the 64b or 128bit based on RF width

Bit Range	Default & Access	Field Name (ID): Description
13:5	0h RW	**USB2_RF_ECC_POISONING_VECTOR (USB2_RF_ECC_POISONING_VECTOR):** USB2 RFs ECC Poisoning Inversion bits for the 64b or 128bit based on RF width
4:3	0h RO	**RSVD (RSVD)**
2	0h RW	**ENGINE_RF_ECC_POISONING_EN (ENGINE_RF_ECC_POISONING_EN):** Enable ECC Poisoning for XHCI Engine related RFs that support ECC
1	0h RW	**USB3_RF_ECC_POISONING_EN (USB3_RF_ECC_POISONING_EN):** Enable ECC Poisoning for USB3 Port related RFs that support ECC. Setting this bit enables poisoning of USB3 Port related RFs. This applies to all USB3 ports
0	0h RW	**USB2_RF_ECC_POISONING_EN (USB2_RF_ECC_POISONING_EN):** Enable ECC Poisoning for USB2 Port related RFs that support ECC. Setting this bit enables poisoning of USB2 Port related RFs. This applies to all USB2 ports

19.1.232 USB2_PORT_STATE_REG (USB2_PORT_STATE_REG)—Offset 8400h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:16	0h RO	**RSVD (RSVD)**
15:0	0h RO	**USB2_PORT_STATE_REG (USB2_PORT_STATE_REG):** Per USB2 Port State Register indicating the following states 0x0 - Connected 0x1 - Suspended 0x2 - Disabled 0x3 - Reserved This register is Read Only and will reflect the state of the ports. Status can change at any time and any usage of this information must be done with care and under specific flows where port state change race conditions are properly handled.

19.1.233 USB3_PORT_STATE_REG (USB3_PORT_STATE_REG)—Offset 8408h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:14	0h RO	**RSVD (RSVD)**
13:0	0h RO	**USB3_PORT_STATE_REG (USB3_PORT_STATE_REG):** Per USB3 Port State Register indicating the following states 0x0 - Connected 0x1 - Suspended 0x2 - Disabled 0x3 - Reserved This register is Read Only and will reflect the state of the ports. Status can change at any time and any usage of this information must be done with care and under specific flows where port state change race conditions are properly handled.

19.1.234 FUS1_REG (FUS1_REG)—Offset 8410h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**RSVD (RSVD)**
20:18	0h RO	**DEV_ID (DEV_ID):** Provides a fuse over-ride for the lower 3 bits of device ID.
17	0h RO	**XHC_DPGDIS (XHC_DPGDIS):** When asserted, it indicates that the xHCI will not dynamically power gate the controller.
16	1h RO	**USBR_DIS (USBR_DIS):** When asserted, it indicates that xHCI does not support USBr
15	0h RO	**XHC_FXN_DIS (XHC_FXN_DIS):** When asserted, it indicates the xHCI is fused to function disabled.
14:10	0h RO	**USB2_PORT_COUNT (USB2_PORT_COUNT):** 0x0 = MAX USB2 Ports enabled 0x1 = Max USB2 Ports -1 enabled 0x1F = All ports disabled
9:5	0h RO	**USB3_PORT_COUNT (USB3_PORT_COUNT):** 0x0 = MAX USB3 Ports enabled 0x1 = Max USB3 Ports -1 enabled 0x1F = All ports disabled
4	0h RO	**DEBUG_MODE_ENABLE (DEBUG_MODE_ENABLE):** 0 = USB debug mode disabled 1 = USB debug mode enabled.
3	0h RO	**XHC_DCGDIS (XHC_DCGDIS):** 0= USB3 (xHC) dynamic clock gating enabled 1= USB3 (xHC) dynamic clock gating disabled
2	0h RO	**REGFILE_DPGDIS (REGFILE_DPGDIS):** 0 = USB3 (xHC) dynamic RF power gating enabled 1 = USB3 (xHC) dynamic RF power gating disabled

Bit Range	Default & Access	Field Name (ID): Description
1	0h RO	**USBIO_PMDIS (USBIO_PMDIS):** 0=USB2 HW LPM and USB3 HW Ux under xHC enabled 1= USB2 HW LPM and USB3 HW Ux under xHC disabled
0	0h RO	**USB2_PLL_SHUTDOWN_DIS (USB2_PLL_SHUTDOWN_DIS):** 0= USB2 PLL Shutdown enabled 1= USB2 PLL Shutdown disabled

19.1.235 FUS2_REG (FUS2_REG)—Offset 8414h

This register is NOT subject to HW save and restore.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**RSVD (RSVD)**
11:0	0h RO	**PORT_MAP_FUS1 (PORT_MAP_FUS1):** 1:0 Port 1 3:2 Port 2 5:4 Port 3 31:30 Port 16 Bit Description: 00: Port assgned to USB3 01: Port assigned to non-XHCI controller 10: Port assigned to Flex IO mapping. Mapping is based on Soft Straps. 11: Reserved.

19.1.236 FUS3_REG (FUS3_REG)—Offset 8418h

This register is NOT subject to HW save and restore.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**RSVD (RSVD)**

19.1.237 STRAP1_REG (STRAP1_REG)—Offset 841Ch

This register is NOT subject to HW save and restore.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**RSVD (RSVD)**
5:0	0h RO	**FlexIO mapping (FLEX_IO_MAPPING):** Each bit corresponds to the appropriately numbered USB3 port (zero based) Bit 0 = port 1, bit 1 = port 2 etc. 0: Port is owned by XHCI 1: Port is not owned by XHCI

19.1.238 STRAP2_REG (STRAP2_REG)—Offset 8420h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**RSVD (RSVD)**

19.1.239 STRAP3_REG (STRAP3_REG)—Offset 8424h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**RSVD (RSVD)**
1:0	0h RO	**XHCI_PRI_CLK_FREQ_SEL (XHCI_PRI_CLK_FREQ_SEL):** Specifies the frequency of the Primary clock (iosf_prim_mux_clk) used by XHCI 00 : 200 MHz (default) 01 : 125 MHz 10 : 250 MHz

19.1.240 DFT_REG1 (DFT_REG1)—Offset 8430h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RSVD**
15:12	0h RO	**RSVD0 (RSVD0):** RSVD0
11	0h RW	**DFTLFPSSEL (DFTLFPSSEL):** DFTLFPSSEL 0: Rxelecidle is driven from GPIO Pin 1: Rxelecidle is Driven as specified by Super Speed DFT LFPS Mode Select
10	0h RW	**Super Speed DFT LFPS Mode Select (SSDFTLMSEL):** This bit selects the Super Speed DFT LFPS mode, and will only take effect when Super Speed HBP mode is enabled. 0b: HBP logic will internally loopback TX LFPS as RX LFPS and AFE RX LFPS path to the controller is disconnected. 1b: RX LFPS path works normally
9:6	0h RW	**RSVD**
5	0h RO	**RSVD1 (RSVD1):** RSVD1
4:0	0h RW	**RSVD**

19.1.241 DFT_REG2 (DFT_REG2)—Offset 8434h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**HS TX CRC (TXCRC):** These register bits contain the value of TX CRC. This TX CRC is placed right after the 480MHz XCLKQ.
15:11	0h RW	**UTMI+ DFT Port Select (UTMIDFTPS):** One CRC is shared for all the UTMI+ ports. These bits select the UTMI+ port for which CRC data will be updated and loopback status reflected in UTMILPBKSTS. 0h: (default) No UTMI+ Port is selected 1h: UTMI+ Port 0 2h: UTMI+ Port 1 3h: UTMI+ Port 2 4h: UTMI+ Port 3 5h: UTMI+ Port 4 6h: UTMI+ Port 5 7h: UTMI+ Port 6 8h: UTMI+ Port 7 9h: UTMI+ Port 8 Ah: UTMI+ Port 9 Bh: UTMI+ Port 10 Ch: UTMI+ Port 11 Dh: UTMI+ Port 12 Eh: UTMI+ Port 13 Others: Reserved

Bit Range	Default & Access	Field Name (ID): Description
10:7	0h RW	**Loop Number (UTMILPBKLOOPN_3_0):** Number of repeatable fixed pattern within a packet Note: Connect register bit 3 to counter bit 7, register bit 2 to counter bit 5, register bit 1 to counter bit 3, register bit 0 to counter bit 1. Counter bits 6, 4, 2 and 0 will be tied off to 0. Hence, the programmable loop number shall be: 0000b: 0 loop 0001b: 2 loops 0010b: 8 loops 0011b: 10 loops 1100b: 160 loops 1101b: 162 loops 1110b: 168 loops 1111b: 170 loops (max) +E27
6:5	0h RW	**Operational Mode (UTMIOPMODE_1_0):** Operational Mode in test mode. These signals select between various operational modes: 00b: Normal Operation 01b: Non-Driving 10b: Disable Bit Stuffing and NRZI encoding 11b: Reserved
4	0h RW	**Termination Select (UTMITERMSEL):** Termination Select in test mode. This signal selects between the FS and HS terminations: 0b: HS termination enabled 1b: FS termination enabled
3:2	0h RW	**Transceiver Select (UTMIXCVRSELECT_1_0):** Transceiver Select in test mode. This signal selects between the LS, FS and HS transceivers: 00b: HS transceiver enabled 01b: FS transceiver enabled 10b: LS transceiver enabled 11b: Reserved
1:0	0h RW	**UTMI+ Loopback Status (UTMILPBKSTS):** Loopback Status for port selected by UTMIDFTPS 00b: Reset condition 01b: Comparator has started receiving data and the received data matches with the TX pattern. 10b: Comparator has started receiving data the received data does not match with the TX pattern but there was no assertion of RC error from UTMI. 11b: Comparator has started receiving data and RX ERROR was asserted for at least one clock by UTMI. Note that this does not reflect the status of pattern comparison since RX error from UTMI is unexpected for loopback.

19.1.242 DFT_REG3 (DFT_REG3)—Offset 8438h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Loopback Pattern (UTMILPBKPAT):** 2-byte pattern for loopback Note: This 2-byte pattern will be replicated to the upper 2-byte to form the DW pattern
15:2	0h RW	**Loopback Lane Select (UTMILPBKSEL_13_0):** Port is selected if the corresponding bit is selected Note: MSB is for UTMI+ Port13, LSB is for UTMI+ Port0

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Loopback Pattern (UTMILPBKPATSEL):** Near end loopback pattern generation type: 0b: Fixed pattern 1b: USB2 test packet
0	0h RW	**Loopback Type (UTMILPBKTYPE):** Loopback Type in test mode. This signal selects between DNELB and ANELB, and will only take effect if DTUTMILPBKEN is set. 0b: Digital Near-End Loopback (DNELB) 1b: Analog Near-End Loopback (ANELB) Note: Analog Far-End Loopback (AFELB) is not supported

19.1.243 dft_reg4 (DFT_REG4)—Offset 843Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RW	**RSVD (RSVD)**
10:0	0h RW	**Loopback Pattern (UTMILPBKPATSEL):** Loopback Lane Select (UTMILPBKSEL): Port is selected if the corresponding bit (zero based) is selected Bit 0 = Port 1 Bit 1 = Port 2 Etc.

19.1.244 dft_reg5 (DFT_REG5)—Offset 8440h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**High Speed Bypass Enable (HIGH_SPEED_BYPASS_ENABLE):** 0000 - Disable all HBP 0001 - Enable SS HBP 0010 - Enable HS HBP 0011
27	0h RW	**DFTIDPINSEL (DFTIDPINSEL):** Select Between Device and Host Controller in HBP mode 0h : Device Controller is selected 1h : Host Controller is selected
26	0h RW/O	**Lock Bit (LOCK):** This bit is used by BIOS to lock/unlock lockable bits. When set to '1' the write access to HBP Enable is disabled (locked state). When set to '0', the write access to bit locked are enable (unlocked state). Writable once after platform reset.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW/L	**Loopback Enable (UTMILPBKEN):** Enable loopback test mode. If asserted, loopback test mode is enabled
24:0	0h RO	**Rsvd (Rsvd)**

19.1.245 XECP_CMDM_STS0 (XECP_CMDM_STS0)—Offset 8448h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**IDMA_OWNS_CNTX (IDMA_OWNS_CNTX):** Indicates that IDMA module owns the context access currently
30	0h RO	**ODMA_OWNS_CNTX (ODMA_OWNS_CNTX):** Indicates that ODMA module owns the context access currently
29	0h RO	**TRM_OWNS_CNTX (TRM_OWNS_CNTX):** Indicates that TRM modules owns the context access currently
28	0h RO	**CMD_RING_REQUESTED_CNTX_LOCK (CMD_RING_REQUESTED_CNTX_LOCK):** Indicates that Command Manager has requested a context lock
27	0h RO	**CMD_RING_STOP_IN_PROGRESS (CMD_RING_STOP_IN_PROGRESS):** Indicates that Command Ring stop command is in progress
26	0h RO	**SCH_UPDATE_CLR_EP_IN_PROGRESS (SCH_UPDATE_CLR_EP_IN_PROGRESS):** Indicates that clearing an EP out of schedule is in progress
25	0h RO	**ADDR_DEV_DONE (ADDR_DEV_DONE):** Indicates that current address device command is done by ODMA
24	0h RO	**ADDR_DEV_IN_PROGRESS (ADDR_DEV_IN_PROGRESS):** Indicates that ODMA has an address device command in progress
23	0h RO	**EP_STATE_UPDATE_IN_PROGRESS (EP_STATE_UPDATE_IN_PROGRESS):** Indicates that updating of EP state is in progress
22	0h RO	**EP_STATE_IN_PROGRESS_FROM_STOP_DUE_TO_DB (EP_STATE_IN_PROGRESS_FROM_STOP_DUE_TO_DB):** Indicates that doorbell manager is issuing and EP update due to a doorbell ring on an EP that is in stop state

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_EP_ERROR (EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_EP_ERROR):** Indicates that transfer ring manager is isuing and EP update due to an EP error condition detected
20	0h RO	**EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_STALL (EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_STALL):** Indicates that transfer ring manager is issuing an EP state update due to stall received
19	0h RO	**Reserved (RSVD)**
18	0h RO	**STOP in progress (STOP_IN_PROGRESS):** Indicates that a STOP on the Command Ring is in progress
17	0h RO	**commend ring has doorbell pending (CMD_RING_DB_PENDING):** Indicates that the commend ring has doorbell pending
16	0h RO	**commend ring running (CMD_RING_RUNNING):** Indicates that the commend ring is running
15:8	0h RO	**Command next capability offset (CMD_NEXT_CAP_OFFSET)**
7:0	0h RO	**Vendor defined capability ID (VID)**

19.1.246 XECP_CMDM_STS1 (XECP_CMDM_STS1)—Offset 844Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3FC0000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Rsvd0 (Rsvd0)**
25:18	FFh RO	**Event manager Producer Cycle State (EMPCS)**
17:12	0h RO	**Interrupter 7 TRB Count [5:0] (INT7_TRB_CNT)**
11:6	0h RO	**Interrupter 6 TRB Count [5:0] (INT6_TRB_CNT)**
5:0	0h RO	**Interrupter 5 TRB Count [5:0] (INT5_TRB_CNT)**

19.1.247 XECP_CMDM_STS2 (XECP_CMDM_STS2)—Offset 8450h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Rsvd0 (Rsvd0)**
4:0	0h RO	**Event Ring Segment Table (ERST):** count low

19.1.248 XECP_CMDM_STS3 (XECP_CMDM_STS3)—Offset 8454h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd0 (Rsvd0)**
15:0	0h RO	**Event Ring Segment Table (ERST):** count high

19.1.249 XECP_CMDM_STS4 (XECP_CMDM_STS4)—Offset 8458h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Event Ring Enqueue Pointer Low (EREPL)**

19.1.250 XECP_CMDM_STS5 (XECP_CMDM_STS5)—Offset 845Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Event Ring Enqueue Pointer High (EREPH)**

19.1.251 AUX Power PHY Reset (UPORTS_PON_RST_REG)—Offset 8460h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**RESERVED (RSVD)**
3:0	0h WO	**Allow Software USB PHY RST (ALL_SW_UP_RST):** Allow a USB PHY reset being issued by software. Writing to this register with bit set to 1 will reset the USB PHY that is connected to the port. Bit3:0 indicates the port number of the USB PHY

19.1.252 Latency Tolerance Control 0 (HOST_IF_LAT_TOL_CTRL_REG0)—Offset 8464h

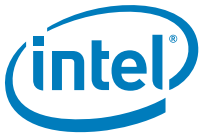
The Latency Tolerance Control Register is used by SW to control which BELT is returned when this register is read. SW shall write to this register to program a Slot-ID, Port-ID and BELT Select to determine which BELT is selected. When this register is read the selected BELT is returned.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: D0000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h WO	**BELT Select (BELT_SEL):** This field determines what value will be selected to read back from SW when reading this register 0: Returns the SW programmed Latency Tolerance Value 1: Returns the Lowest BELT in the Host 2: Returns the BELT for the requested Slot-ID (Slot Select) 3: Returns the BELT for the requested Port-ID (Port Select)
29:20	0h RO	**Rsvd1 (Rsvd1)**



Bit Range	Default & Access	Field Name (ID): Description
19:16	Dh WO	**Port Select (PORT_SEL):** Used to select the BELT for a given Port # when the BELT Select is programmed to select the Port-ID (this field is 0 based)
15:12	0h RO	**Rsvd (Rsvd)**
11:5	0h RO	**BELT Value (BELTV):** Value of selected BELT is return in this field
4:0	0h RW	**Slot Select (SLOT_SEL):** Reads will return: BELT Value (BELTV) [4:0]: Value of selected BELT is return in this field Writes will control : Slot Select (): Used to select the BELT for a given Slot # when the BELT Select is programmed to select the Slot-ID (this field is zero based)

19.1.253 USB Legacy Support Capability (USBLEGSUP)—Offset 846Ch

This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2201h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Rsvd2 (Rsvd2)**
24	0h RW	**HC OS Owned Semaphore (HCOSOS)**
23:17	0h RO	**Rsvd1 (Rsvd1)**
16	0h RW	**HC BIOS Owned Semaphore (HCBIOSOS)**
15:8	22h RW/S	**Next Capability Pointer (NextCP)**
7:0	1h RW/L	**Capability ID (CID)**

19.1.254 USB Legacy Support Control Status (USBLEGCTLSTS)—Offset 8470h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/C	**SMI on BAR (SMIBAR)**
30	0h RW/C	**SMI on PCI Command (SMIPCIC)**
29	0h RW/C	**SMI on OS Ownership Change (SMIOSOC)**
28:21	0h RO	**Rsvd4 (Rsvd4)**
20	0h RO	**SMI on Host System Error (SMIHSE)**
19:17	0h RO	**Rsvd3 (Rsvd3)**
16	0h RO	**SMI on Event Interrupt (SMIEI)**
15	0h RW	**SMI on BAR Enable (SMIBARE)**
14	0h RW	**SMI on PCI Command Enable (SMIPCICE)**
13	0h RW	**SMI on OS Ownership Enable (SMIOSOE)**
12:5	0h RO	**Rsvd2 (Rsvd2)**
4	0h RW	**SMI on Host System Error Enable (SMIHSEE)**
3:1	0h RO	**Rsvd1 (Rsvd1)**
0	0h RW	**USB SMI Enable (USBSMIE)**

19.1.255 Port Disable Override capability register (PDO_CAPABILITY)—Offset 84F4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3C6h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd (Rsvd)**
15:8	3h RO	**Next Capability Pointer (NCP)**

Bit Range	Default & Access	Field Name (ID): Description
7:0	C6h RO	**Capability ID (CID)**

19.1.256 USB2 Port Disable Override (USB2PDO)—Offset 84F8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Rsvd1 (Rsvd1)**
7:0	0h RW/O	**USB2PDO (USB2PDO)**

19.1.257 USB3 Port Disable Override (USB3PDO)—Offset 84FCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Rsvd1 (Rsvd1)**
6:0	0h RW/O	**USB3 Port Disable Override (USB3PDO):** A '1' in a bit position prevents the corresponding USB3 port from reporting a Device Connection to the XHC.

19.1.258 HW state capability register (HW_STATE_CAPABILITY)—Offset 8500h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1F40C7h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Rsvd (Rsvd)**
23:16	1Fh RO	**Save Length (SAVE_LENGTH):** Indicates the number of DWords in this capability starting at offset 04h, that need to be saved and restored
15:8	40h RO	**Next Capability Pointer (NCP)**
7:0	C7h RO	**Capability ID (CID)**

19.1.259 HW state register 1 (HW_STATE_REG1)—Offset 8504h

Implementation defined HW state: SW must not access this register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**HW_STATE_REG1 (HW_STATE_REG1)**

19.1.260 HW state register 2 (HW_STATE_REG2)—Offset 8508h

Implementation defined HW state: SW must not access this register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**HW_STATE_REG2 (HW_STATE_REG2)**

19.1.261 HW state register 3 (HW_STATE_REG3)—Offset 850Ch

Implementation defined HW state: SW must not access this register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**HW_STATE_REG3 (HW_STATE_REG3)**

19.1.262 HW state register 4 (HW_STATE_REG4)—Offset 8510h

Implementation defined HW state: SW must not access this register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**HW_STATE_REG4 (HW_STATE_REG4)**

19.1.263 CONFIG mirror capability register (CONFIG_MIRROR_CAPABILITY)—Offset 8600h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40C2h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd (Rsvd)**
15:8	40h RO	**Next Capability Pointer (NCP)**
7:0	C2h RO	**Capability ID (CID)**

19.1.264 Command (CMD_MMIO)—Offset 8604h

Dummy register, mirror of physical register as CMD

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved (RSVD)**
10	0h RW	**Interrupt Disable (ID):** When cleared to 0, the function is capable of generating interrupts. When 1, the function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable.
9	0h RO	**Fast Back to Back Enable (FBE)**
8	0h RW	**SERR# Enable (SERR):** When set to 1, the XHC is capable of generating (internally) SERR#.
7	0h RO	**Wait Cycle Control (WCC)**
6	0h RW	**Parity Error Response (PER):** When set to 1, the XHCI Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the XHCI specification. Note that this applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.
5	0h RO	**VGA Palette Snoop (VPS)**
4	0h RO	**Memory Write Invalidate (MWI)**
3	0h RO	**Special Cycle Enable (SCE)**
2	0h RW	**Bus Master Enable (BME):** When set, it allows XHC to act as a bus master. When cleared, it disable XHC from initiating transactions on the system bus.
1	0h RW	**Memory Space Enable (MSE):** This bit controls access to the XHC Memory Space registers. If this bit is set, accesses to the XHC registers are enabled. The Base Address register for the XHC should be programmed before this bit is set.
0	0h RO	**I/O Space Enable (IOSE):** Reserved as 0. Read-Only.

19.1.265 Device Status (STS_MMIO)—Offset 8606h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 290h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE):** This bit is set by the SoC whenever a parity error is seen on the internal interface to the XHC host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a 1 to this bit location.
14	0h RW/1C	**Signaled System Error (SSE):** This bit is set by the SoC whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set. Software clears this bit by writing a 1 to this bit location.
13	0h RW/1C	**Received Master-Abort Status (RMA):** This bit is set when XHC, as a master, receives a master-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
12	0h RW/1C	**Received Target Abort Status (RTA):** This bit is set when XHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
11	0h RW/1C	**Signaled Target-Abort Status (STA):** This bit is used to indicate when the XHC function responds to a cycle with a target abort.
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only.
8	0h RW/1C	**Master Data Parity Error Detected (MDPED):** This bit is set by the SoC whenever a data parity error is detected on a XHC read completion packet on the internal interface to the XHC host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a 1 to this bit location.
7	1h RO	**Fast Back-to-Back Capable (FBBC):** Reserved as 1 Read-Only.
6	0h RO	**User Definable Features (UDF):** Reserved as 0. Read-Only.
5	0h RO	**66 MHz Capable (MC):** Reserved as 0. Read-Only.
4	1h RO	**Capabilities List (CL):** Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	0h RO/V	**Interrupt Status (IS):** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	0h RO	**Reserved (RSVD)**

19.1.266 Revision ID (RID_MMIO)—Offset 8608h

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO/V	**Revision ID (RID):** See Chap 6 for value.

19.1.267 Programming Interface (PI_MMIO)—Offset 8609h

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 30h

Bit Range	Default & Access	Field Name (ID): Description
7:0	30h RO	**Programming Interface (PI):** A value of 30h indicates that this USB Host Controller conforms to the XHCI specification.

19.1.268 Sub Class Code (SCC_MMIO)—Offset 860Ah

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 3h

Bit Range	Default & Access	Field Name (ID): Description
7:0	3h RO	**Sub Class Code (SCC):** A value of 03h indicates that this is a Universal Serial Bus Host Controller.

19.1.269 Base Class Code (BCC_MMIO)—Offset 860Bh

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: Ch

Bit Range	Default & Access	Field Name (ID): Description
7:0	Ch RO	**Base Class Code (BCC):** A value of 0Ch indicates that this is a Serial Bus controller.

19.1.270 Master Latency Timer (MLT_MMIO)—Offset 860Dh

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Master Latency Timer (MLT):** Because the XHC controller is internally implemented with arbitration on an internal interface, it does not need a master latency timer. The bits will be fixed at 0.

19.1.271 Header Type (HT_MMIO)—Offset 860Eh

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Multi-Function Bit (MFB):** Read only indicating single function device.
6:0	0h RO	**Configuration layout (CL):** Hardwired to 0 to indicate a standard PCI configuration layout.

19.1.272 Memory Base Address (MBAR_MMIO)—Offset 8610h

Dummy register, mirror of physical register as MBAR. Value in this register will be different after the enumeration process.

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
63:16	0h RW	**Base Address (BA):** Bits (63:16) correspond to memory address signals (63:16), respectively. This gives 64 KB of relocatable memory space aligned to 64 KB boundaries.
15:4	0h RO	**Reserved (RSVD):** Reserved. Read-Only 0, this indicates that this function is requesting an 64KB block of memory.
3	0h RO	**Prefetchable (Prefetchable):** This bit is hardwired to 0 indicating that this range should not be prefetched.
2:1	2h RO	**Type (Type):** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** This bit is hardwired to 0 indicating that the base address field in this register maps to memory space

19.1.273 USB Subsystem Vendor ID (SSVID_MMIO)—Offset 862Ch

Dummy register, mirror of physical register as SSVID. This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/L	**USB Subsystem Vendor ID (SSVID):** This register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others.

19.1.274 USB Subsystem ID (SSID_MMIO)—Offset 862Eh

Dummy register, mirror of physical register as SSID. This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/L	**USB Subsystem ID (SSID):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s).

19.1.275 Capabilities Pointer (CAP_PTR_MMIO)—Offset 8634h

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 70h

Bit Range	Default & Access	Field Name (ID): Description
7:0	70h RO	**Capabilities Pointer (CAP_PTR):** This register points to the starting offset of the capabilities ranges.

19.1.276 Interrupt Line (ILINE_MMIO)—Offset 863Ch

Dummy register, mirror of physical register as ILINE.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (ILINE):** This data is not used by the SoC. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

19.1.277 Interrupt Pin (IPIN_MMIO)—Offset 863Dh

Dummy register, mirror of physical register as IPIN.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW/L	**Interrupt pin (IPIN):** Bits 7:0 reflect the Interrupt Pin assigned to the host controller by the platform (and are hardwired).

19.1.278 XHC System Bus Configuration 1 (XHCC1_MMIO)—Offset 8640h

Dummy register, mirror of physical register as XHCC1

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1FDh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/O	**Access Control (ACCTRL):** This bit is used by BIOS to lock/ unlock lockable bits. When set to '1' the write access to bits locked by this bit is disabled (locked state). When set to '0', the write access to bit locked by this bit is enabled (unlocked state). Writable once after platform reset.
30:25	0h RW	**Reserved**
24	0h RW	**Master/Target Abort SERR (RMTASERR):** When set, it allows the out-of-band error reporting from the xHCI Controller to be reported as SERR# (if SERR# reporting is enabled) and thus set the STS.SSE bit.
23	0h RW/C	**Unsupported Request Detected (URD):** Set the HW when xHCI Controller received an unsupported request posted cycle. Cleared by SW when the bit is written with value of '1'.
22	0h RW	**Unsupported Request Report Enable (URRE):** When set this bit allows the URD bit to be reported as SERR# (if SERR# reporting is enabled) and thus set the STS.SSE bit.
21:19	0h RW	**Inactivity Initiated L1 Enable (IIL1E):** If programmed to non-zero, it allows L1 power managed to be enabled after the time-out period specified. 000: Disabled 001: 32 bb_cclk 010: 64 bb_cclk 011: 128 bb_cclk 100: 256 bb_cclk 101: 512 bb_cclk 110: 1024 bb_cclk 111: 131072 bb_cclk
18	0h RW	**XHC Initiated L1 Enable (XHCIL1E):** If set, allow the XHC initiated L1 power mangement to be enabled.
17	0h RW	**D3 Initiated L1 Enable (D3IL1E):** If set, allow PCI device state D3 initiated L1 power managment to be enables.

Bit Range	Default & Access	Field Name (ID): Description
16:12	0h RW	**Periodic Complete Pre Wake Time (PCPWT):** The value programmed in this field determines how far in advance of the start of the next micro-frame the host controller must de-assert the "Periodic Complete" signal . This allows for platform wake time before the next scheduled periodic transaction. The value programmed in this field represents the # of bytes consumed in the current micro-frame which is required to allow for the periodic complete to de-assert. This allows for a programmable time to cause the periodic complete to de-assert prior to the start of the next micro-frame. Register Format: Bits (16:12) represnets the # of bytes remaining with a 256B granularity. Periodic Complete will de-assert if the bytes consumed in the current micro-frame is less
11	0h RW	**SW Assisted xHC Idle (SWAXHCI):** This bit being set will indicate xHC idleness (through SW means), which must be a '1' to allow L1 entry, and subsequently allow backbone clock to be gated. This bit is to be set by Intel xHCI driver after checking that the xHCI Controller will stay in idle state for a significant period of time, e.g. all ports disconnected. This bit can be cleared under the following conditions (see SWAXHCI Policy bits in xHC System Bus Configuration 2 register): n SW: SW could write 0 to clear this bit. n HW: HW, under policy control, will clear this bit on an MMIO access to the Host Controller. n HW: HW, under policy control, will clear this bit when HW exits Idle state.
10:8	1h RW	**L23 to Host Reset Acknowledge Wait Count (L23HRAWC):** If programmed to non zero, it allows a wait period after the L23 PHY has shutdown before returning host reset acknowledge to PMC. 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk
7:6	3h RW	**Upstream Type Arbiter Grant Count Posted (UTAGCP):** Grant count for IOSF upstream L2 request type arbiter for posted type
5:4	3h RW	**Upstream Type Arbiter Grant Count Non Posted (UDAGCNP):** Grant count for IOSF upstream L2 type arbiter for non-posted type
3:2	3h RW	**Upstream Type Arbiter Grant Count Completion (UDAGCCP) (UDAGCCP):** Grant count for IOSF upstream L2 type arbiter for completion type
1:0	1h RW	**Upstream Device Arbiter Grant Count (UDAGC) (UDAGC):** Grant count for IOSF upstream L1 device arbiter

19.1.279 XHC System Bus Configuration 2 (XHCC2_MMIO)—Offset 8644h

Dummy register, mirror of physical register as XHCC2

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3C000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**OC Configuration Done (OCCFGDONE):** This bit is used by BIOS to prevent spurious switching during OC configuration. It must be set by BIOS after configuration of the OC mapping bits is complete. Once this bit is set, OC mapping shall not be changed by SW.
30:26	0h RW	**Reserved.**
25	0h RW	**DMA Request Boundary Crossing Control (DREQBCC):** This bit controls the boundary crossing limit of each Read/Write Request. 0: 4KB 1: 64B
24:22	0h RW	**IDMA Read Request Size Control (IDMA_RDREQSZCTRL):** Read Request Size Control: This bit controls the maximum size of each Read Request. 000: 128B 001: 256B 011 - 110: Reserved 111: 64B
21	0h RW	**XHC Upstream Read Relaxed Ordering Enable (XHCUPRDROE):** This policy controls the Relaxed Ordering attribute for upstream reads. 0 - xHC will clear RO for all upstream read requests. 1 - xHC will set RO for all upstream read requests.
20	0h RW	**IOSF Sideband Register Access Disable (IOSFSRAD):** When set, it disables the IOSF sideband interface from accepting any host space register access.
19:14	Fh RW	**Upstream Non-Posted Pre-Allocation (UNPPA):** This field reserves data sizes, in 64 byte chunks, of the downstream completion resource. This value is zero based. 000000 - 111111: Pre-allocate 64 bytes - 4096 bytes If set greater than the default allows over-allocation If set less than default allows under-allocation Only allowed to be programmed when BME = 0 and no outstanding downstream completion
13:12	0h RW	**SW Assisted xHC Idle Policy (SWAXHCIP):** Note: Irrespective of the setting of this field, SW write of 0 to SWAXHCI will clear the bit. 00b (default): xHC HW clears SWAXHCI bit upon: n MMIO access to Host Controller OR n xHC HW exits Idle state 01b: xHC HW does not autonomously clear SWAXHCI bit. The bit could be cleared only by SW. 10b: xHC HW clears SWAXHCI upon MMIO acces to Host Controller. xHC HW exit from Idle state will not clear SWAXHCI. 11b: Reserved
11	0h RW	**MMIO Read After MMIO Write Delay Disable (RAWDD):** This field controls delay on MMIO Read after MMIO Write. 0b (Default): Delay MMIO Read after MMIO Write 1b: Do not delay MMIO Read after MMIO Write Note that this delay applies after the second of the two DW writes in the case where the IOSF Gasket splits a QW write into two single DW writes to the IP.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**MMIO Write After MMIO Write Delay Enable (WAWDE):** This field controls delay on MMIO Write after previous MMIO Write. 0b (Default): Do not delay MMIO Write after previous MMIO Write 1b: Delay MMIO Write after previous MMIO Write Note that the delay count does not apply on the second of the two DW writes that are generated by IOSF Gasket when it splits a QW write into two. In other words, the second of the two DW writes could happen without any delay with respect to the first DW write. This choice is being made for ease of ECO. The delay count, in this case, will apply after the second of the two DW writes.
9:8	0h RW	**SW Assisted Cx Inhibit (SWACXIHB):** This field controls how the DMI L1 inhibit signal from USB3 to PMC will behave. 00: Never inhibit Cx 01: Inhibit Cx when Isochronous Endpoint is active (PPT Behavior) 10: Inhibit Cx when Periodic Active as defined in 40.4.3.2.1 11: Always inhibit Cx
7:6	0h RW	**SW Assisted DMI L1 Inhibit (SWADMIL1IHB):** This field controls how the DMI L1 inhibit signal from USB3 to DMI will behave. 00: Never inhibit DMI L1. 01: Inhibit DMI L1 when Isochronous Endpoint is active (PPT Behavior). 10: Inhibit DMI L1 when Priodic Active as defined in 40.4.3.2.1. 11: Inhibit DMI L1 if XHCC1.SWAXHCI = 0.
5:3	0h RW	**L1 Force P2 Clock Gating Wait Count (L1FP2CGWC):** If programmed to non zero, it allows L1 force P2 gating off the clock to be delayed after the time-out period specified. If wake up event is detected before the time-out, pclk remains alive and trigger L1 exit as though CPU host is causing the wake, 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk
2:0	0h RW	**Read Request Size Control (RDREQSZCTRL):** Read Request Size Control: This bit controls the maximum size of each Read Request. 000: 128B 001: 256B 010: 512B 011 - 110: Reserved 111: 64B

19.1.280 Clock Gating (XHCLKGTEN_MMIO)—Offset 8650h

Dummy register, mirror of physical register as XHCLKGTEN

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Rsvd2 (Rsvd2):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
28	0h RW	**Nak'ing USB2.0 EPs for Backbone Clock Gating and PLL Shutdown (NUEFBCGPS):** This field controls whether Naking USB2.0 EPs, once in Naking low priority schedule, should be considered as active for the considerations for backbone clock gating and PLL shutdown or not. 0: Naking USB2.0 EPs are not considered to be active for Backbone Clock Gating and PLL Shutdown evaluation. 1: Naking USB2.0 EPs are considered to be active for Backbone clock gating and PLL shutdown evaluation.
27	0h RW	**SRAM Power Gate Enable (SRAMPGTEN):** This register enables the SRAM Power Gating when PLL shutdown conditions for all clock domains have been met 0 - Disallow SRAM Power Gating. 1 - Allow SRAM Power Gating
26	0h RW	**SS Link PLL Shutdown Enable (SSLSE):** This register enables the SS P3 state to be exposed to PXP PLL Shutdown conditions on behalf of all USB SS Ports ontop of trunk clock gating. 0 - P3 state NOT allowed to result in PXP PLL shutdown. 1- P3 state allowed to result in PXP PLL shutdown
25	0h RW	**USB2 PLL Shutdown Enable (USB2PLLSE):** When set, this bit allows USB2 PLL to be shutdown when HS Link trunk clock is gated, and xHC can tolerate PLL spin up time for subsequent clock request. Note: if USB2 PLL Shutdown Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
24	0h RW	**IOSF Sideband Trunk Clock Gating Enable (IOSFSTCGE):** When set, this bit allows the IOSF sideband clock trunk to be gated when idle conditions are met.
23:20	0h RW	**HS Backbone PXP Trunk Clock Gate Enable (HSTCGE):** This register determines the HS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==) U0 or deeper (1) ==) NA (no support for U1) (2) ==) U2 (L1) or deeper (3) ==) U3 (L2) or deeper
19:16	0h RW	**SS Backbone PXP Trunk Clock Gate Enable (SSTCGE):** This register determines the SS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==) U0 or deeper (1) ==) U1 or deeper (2) ==) U2 or deeper (3) ==) U3 or deeper
15	0h RW	**XHC Ignore_EU3S (XHCIGEU3S):** This register determines if the xHC will use the EU3S as a condition to allow for Frame timer gating. 0 - xHC may allow frame timer to be gated when EU3S is set and all ports are in the required state. 1 - xHC may allow frame timer to be gated regardless of EU3S.
14	0h RW	**XHC Frame Timer Clock Shutdown Enable (XHCFTCLKSE):** This register determines if the xHC will allow the frame timer clock to be gated. 0 - xHC will not allow ICC PLL 96MHz output to be shutdown thus keeping the frame timer running. 1 - xHC will allow ICC PLL 96MHz output to be shutdown under specific conditions.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**XHC Backbone PXP Trunk Clock Gate In Presence of ISOCH EP (XHCBBTCGIPISO):** This register controls the policy on allowing Backbone PXP trunk clock gate in the presence of IDLE ISOCH EP s with active DB. Allows the periodic active to be used in enabling Backbone PXP trunk clock gating of core clock. 0 Trunk gate of core clock is not allowed when ISOCH EP DB is set and ISOCH EP s are idle. 1 Allow trunk gate of core clock when ISOCH EP DB is set and ISOCH EP s are idle.
12	0h RW	**XHC HS Backbone PXP Trunk Clock Gate U2 non RWE (XHCHSTCGU2NRWE):** This register controls the policy on allowing Backbone PXP trunk gating of core clock when there is atleast 1 non Remote Wake Enabled HS Port in U2. 0 Prevent trunk gate of core clock when a non RWE HS Port is in U2. 1 Allow trunk gate of core clock when a non RWE HS Port is in U2.
11:10	0h RW	**XHC USB2 PLL Shutdown Lx Enable (XHCUSB2PLLSDLE):** This register determines the HS Link state(s) which will be exposed to USB2 PLL Shutdown conditions on behalf of all USB2 HS Ports. Ly is a state allowed to result in USB2 PLL Shutdown when en(x) is asserted. (0) ==) L1 or deeper (1) ==) L2 or deeper
9:8	0h RW	**HS Backbone PXP PLL Shutdown Ux Enable (HSUXDMIPLLSE):** This register determines the Ux state(s) which will be exposed to PXP PLL Shutdown conditions. PLL Shutdown is allowed in: 00b Disabled (Link states shall be disabled for DMI PLL shutdown) 01b U0 or conditions for 10b setting. 10b U2 or conditions for 11b setting. 10b U3, Disconnected, Disabled or Powered-Off.
7:5	0h RW	**SS Backbone PXP PLL Shutdown Ux Enable (SSPLLSUE):** This register determines the Ux state(s) which will be exposed to DMI PLL Shutdown conditions. PLL Shutdown is allowed in: 000b Disabled (Link states shall be ignored for DMI PLL shutdown). 001b U0 or conditions for 010b setting 010b U1 or conditions for 011b setting 011b U2 or conditions for 100b setting 100b U3, Disconnected, Disabled or Powered-Off
4	0h RW	**XHC Backbone Local Clock Gating Enable (XHCBLCGE):** When set, this bit allows XHCI Controller IP backbone clock to be locally gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
3	0h RW	**HS Link Trunk Clock Gating Enable (HSLTCGE):** When set, this bit allows High Speed Link control's 480 MHz and its 48/60 MHz link clock trunk to be gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**SS Link Trunk Clock Gating Enable (SSLTCGE):** When set, this bit allows the SuperSpeed Link control's 250 MHz and its divided 125 MHz link clock trunk to ge gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled.
1	0h RW	**IOSF Backbone Trunk Clock Gating Enable (IOSFBTCGE):** When set, this bit allows the IOSF backbone clock trunk to be gated when idle conditions are met.
0	0h RW	**IOSF Gasket Backbone Local Clock Gating Enable (IOSFBLCGE):** When set, this bit allows the IOSF Gasket backbone clock to be locally gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled.

19.1.281 Audio Time Synchronization (AUDSYNC_MMIO)—Offset 8658h

This 32 bit register is used for audio stream synchronization across different devices. Global signal sample_now captures a value in AUDSYNC register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Rsvd2 (Rsvd2)**
29:16	0h RO/V	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits (29:16) reflect state of bits (13:0) of FRINDEX
15:13	0h RO	**Rsvd1 (Rsvd1)**
12:0	0h RO/V	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done in FLA.

19.1.282 Serial Bus Release Number (SBRN_MMIO)—Offset 8660h

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 30h

Bit Range	Default & Access	Field Name (ID): Description
7:0	30h RO	**Serial Bus Release Number (SBRN):** A value of 30h indicates that this controller follows USB release 3.0.

19.1.283 Frame Length Adjustment (FLADJ_MMIO)—Offset 8661h

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit in the USBSTS register is a one. Changing value of this register while the host controller is operating yields undefined results.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 60h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved (RSVD):** Read-Only. These bits are reserved for future use and should read as "00".
6	1h RO	**No Frame Length Timing Capability (NO_FRAME_LENGTH_TIMING_CAP):** This flag is set to 1 to indicate that the host controller does not support a programmable Frame Length Timing Value field.
5:0	20h RO	**Frame Length Timing Value (FLTV):** SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (number of High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value

19.1.284 Best Effort Service Latency (BESL_MMIO)—Offset 8662h

Dummy register, mirror of physical register as BESL. Bset Effort Service Latency.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW/L	**Default Best Effort Service Latency Deep (DBESLD):** Default Best Effort Service Latency (DBESLD) If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field. This is programmed by BIOS based on platform parameters.
3:0	0h RW/L	**Default Best Effort Service Latency (DBESL):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field. This is programmed by BIOS based on platform parameters.

19.1.285 PCI Power Management Capability ID (PM_CID_MMIO)—Offset 8670h

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
7:0	1h RO	**PCI Power Management Capability ID (PM_CID):** A value of 01h indicates that this is a PCI Power Management capabilities field.

19.1.286 Next Item Pointer #1 (PM_NEXT_MMIO)—Offset 8671h

Dummy register, mirror of physical register as PM_NEXT. This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Next Item Pointer #1 (PM_NEXT):** This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the Access Control bit is set to '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Values of: 80h implies next capability is MSI 00h implies that MSI capability is hidden. Note: This value is never expected to be programmed.

19.1.287 Power Management Capabilities (PM_CAP_MMIO)—Offset 8672h

Dummy register, mirror of physical register as PM_CAP. Normally, this register is read-only to report capabilities to the power management software. In order to report different power management capabilities depending on the system in which the SoC is used, the write access to this register is controlled by the Access Control bit (ACCTRL). The value written to this register does not affect the hardware other than changing the value returned during a read. This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: C1C2h

Bit Range	Default & Access	Field Name (ID): Description
15:11	18h RW/L	**PME_Support (PME_Support):** This 5-bit field indicates the power states in which the function may assert PME#. The SoC XHC does not support the D1 or D2 states. For all other states, the SoC XHC is capable of generating PME#. Software should never need to modify this field.
10	0h RW/L	**D2_Support (D2_Support):** The D2 state is not supported.
9	0h RW/L	**D1_Support (D1_Support):** The D1 state is not supported.
8:6	7h RW/L	**Aux_Current (Aux_Current):** The SoC XHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known.
5	0h RW/L	**DSI (DSI):** The SoC reports 0, indicating that no device-specific initialization is required.
4	0h RO	**Reserved (RSVD)**
3	0h RW/L	**PME Clock (PMEClock):** The SoC reports 0, indicating that no PCI clock is required to generate PME#.

Bit Range	Default & Access	Field Name (ID): Description
2:0	2h RW/L	**Version (Version):** The SoC reports 010, indicating that it complies with Revision 1.1 of the PCI Power Management Specification.

19.1.288 Power Management Control/Status (PM_CS_MMIO)—Offset 8674h

Dummy register, mirror of physical register as PM_CS

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PME_Status (PME_Status):** This bit is set when the SoC XHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14:13	0h RO	**Data_Scale (Data_Scale):** The SoC hardwires these bits to 00 because it does not support the associated Data register.
12:9	0h RO	**Data_Select (Data_Select):** The SoC hardwires these bits to 0000 because it does not support the associated Data register.
8	0h RW	**PME_En (PME_En):** A 1 enables the SoC XHC to generate an internal PME signal when PME_Status is 1. This bit must be explicitly cleared by the operating system each time it is initially loaded.
7:4	0h RO	**Reserved (RSVD)**
3	1h RO	**No Soft Reset (NSR):** No_Soft_Reset - When set ("1"), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. Transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved (RSVD2)**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**PowerState (PowerState):** This 2-bit field is used both to determine the current power state of XHC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3hot state, the SoC must not accept accesses to the XHC memory range, but the configuration space must still be accessible.

19.1.289 Message Signaled Interrupt CID (MSI_CID_MMIO)—Offset 8680h

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 5h

Bit Range	Default & Access	Field Name (ID): Description
7:0	5h RO	**Capability ID (CID):** Indicates that this is an MSI capability

19.1.290 Next item pointer (MSI_NEXT_MMIO)—Offset 8681h

Dummy register, mirror of physical register as MSI_NEXT

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW/L	**Next Pointer (NEXT):** Indicates that this is the last item on the capability list

19.1.291 Message Signaled Interrupt Message Control (MSI_MCTL_MMIO)—Offset 8682h

Dummy register, mirror of physical register as MSI_MCTL

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 86h

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved (RSVD)**
8	0h RO	**Per-Vector Masking Capable (PVM):** Specifies whether controller supports MSI per vector masking. Not supported
7	1h RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages. This device is 64-bit capable.
6:4	0h RW	**Multiple Message Enable (MME):** Indicates the number of messages the controller should assert. This device supports multiple message MSI.
3:1	3h RO	**Multiple Message Capable (MMC):** Indicates the number of messages the controller wishes to assert. This field must be set by HW to reflect the number of Interrupters supported. Encoding number of Vectors requested (number of Interrupters) 000 1 001 2 010 4 011 8 100 16 101 32 110-111 Reserved
0	0h RW	**MSI Enable (MSIE):** If set to 1, MSI is enabled and the traditional interrupt pins are not used to generate interrupts. If cleared to 0, MSI operation is disabled and the traditional interrupt pins are used.

19.1.292 Message Signaled Interrupt Message Address (MSI_MAD_MMIO)—Offset 8684h

Dummy register, mirror of physical register as MSI_MAD

Access Method

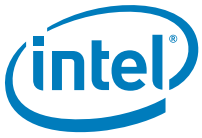
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Addr (Addr):** Lower DW of system specified message address, always DWORD aligned
1:0	0h RO	**Reserved (RSVD)**

19.1.293 Message Signaled Interrupt Upper Address (MSI_MUAD_MMIO)—Offset 8688h

Dummy register, mirror of physical register as MSI_MUAD



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Addr (UpperAddr):** Upper DW of system specified message address.

19.1.294 Message Signaled Interrupt Message Data (MSI_MD_MMIO)—Offset 868Ch

Dummy register, mirror of physical register as MSI_MD

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data (Data):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD(15:0)) during the data phase of the MSI memory write transaction. The Multiple Message Enable field (bits 6-4 of the Message Control register) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010 indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000, the function is not permitted to modify the message data.

19.1.295 Device Idle Capability (DEVIDLE_MMIO)—Offset 8690h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VID (VID)**
27:24	0h RO	**REV (REV)**
23:16	14h RO	**Length (LENGTH):** Indicates that this capability is 16 bytes long.
15:8	0h RO	**Next Capability Pointer (NCP):** This field contains the offset to the next PCI Capability structure or 000h if no other items exist in the linked list of Capabilities.
7:0	9h RO	**Capability ID (CID)**

19.1.296 Vendor Specific Header (VSHDR_MMIO)—Offset 8694h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC Length (VSEC_LENGTH):** This field indicates the number of bytes in the entire VSEC structure, including the PCI Extended Capability header, the Vendor- Specific header, and the Vendor-Specific register
19:16	0h RO	**VSEC Rev (VSEC_REV):** This field is a vendor-defined version number that indicates the version of the VSEC structure. Software must qualify the Vendor ID and VSEC ID before interpreting this field.
15:0	10h RO	**VSEC ID (VSEC_ID):** This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure. Software must qualify the Vendor ID before interpreting this field.

19.1.297 SW LTR POINTER (SWLTRPTR_MMIO)—Offset 8698h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW LTR Update MMIO Offset Location (SW_LTR_UPDT_MMIO_OFFSET):** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set.
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0's based AR Number of the BAR which contains the location of the SW LTR MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR Number. Bar 0 is the 1st BAR. The value of this register is a don't care, if the Valid bit is not set.
0	0h RO	**Valid (VALID):** Set to '1' to indicate that the function has implemented a SW LTR register as specified in the DevIdle that can be located using the SWLTRLOC register and BARNUM. Set to '0' to indicate that the function has not implemented a SW LTR register that is compliant to the DevIdle definition. This could be because the function has not implemented SW LTR at all, or has a device specific version of SW LTR.

19.1.298 Device Idle Pointer Register (DEVIDLEPTR_MMIO)—Offset 869Ch

Dummy register, mirror of physical register as DEVIDLEPTR

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 80AC1h

Bit Range	Default & Access	Field Name (ID): Description
31:4	80ACh RW/L	**DevIdle MMIO Offset Location (DEVIDLELOC):** This register contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set.
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0's based BAR Number of the BAR which contains the location of the DevIdle MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR Number. Bar 0 is the 1st BAR. The value of this register is a don't care, if the Valid bit is not set.

Bit Range	Default & Access	Field Name (ID): Description
0	1h RW/L	**Valid (VALID):** Set to '1' to indicate that the function has implemented a DevIdle register as specified in the DevIdle that can be located using the DEVIDLELOC register and BARNUM. Set to '0' to indicate that the function has not implemented a DevIdle register that is compliant to the DevIdle definition. This could be because the function has not implemented DevIdle at all, or has a device specific version of DevIdle.

19.1.299 Device Idle Power ON Latency (DEVIDLEPOL_MMIO)—Offset 86A0h

Dummy register, mirror of physical register as DEVIDLEPOL

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Rsvd1 (Rsvd1)**
12:10	2h RW/L	**Power On Latency Scale (POLS):** Latency Scale multiplier: 010: 1us 011: 32us All other settings are reserved. The value of this register is multiplied with the Power On Latency Value (POLV) to provide the DevIdle power on exit latency multiplier scale from 1us to 32ms. This register is defined to be RWO (read-write-once) to allow BIOS to set the initial value. This register is undefined if the DevIdle.Valid bit is '0'.
9:0	0h RW/L	**Power On Latency Value (POLV):** 10-bit value that is multiplied by the Power On Latency Scale. A value of 0 indicates a power on latency of less than 1us. This register is defined to be RWO (read-write-once) to allow BIOS to set the initial value. This register is undefined if the DevIdle.Valid bit is '0'.

19.1.300 High Speed Configuration 2 (HSCFG2_MMIO)—Offset 86A4h

Dummy register, mirror of physical register as HSCFG2

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Rsvd1 (Rsvd1)**
18	0h RW	**PORT1_HOST_MODE_OVERRIDE (PORT1_HOST_MODE_OVERRIDE):** When set, this bit causes the Host_Device mux on port 1 to be forced into the Host mode.
17:16	0h RW	**eUSB2SEL (eUSB2SEL):** The two bits are associate with USB2 ports 1 - bit 16 and 2 - bit 2 0: Port is mapped to USB2 1: Port is mapped to eUSB2
15	0h RW	**HS ASYNC Active IN Mask (HSAAIM):** Determines if the Async Active will mask/ignore IN EP s. 0 HS ASYNC Active will include IN EP s. 1 HS ASYNC Active will mask/ignore IN EP s.
14	0h RW	**HS OUT ASYNC Active Polling EP Mask (HSOAAPEPM):** Determines if the Async Active for OUT HS/FS/LS masks/ignores EP s that are polling/PINGing (HS) due to NAK. 0 HS OUT ASYNC Active will include EP s that are polling. 1 HS OUT ASYNC Active will mask/ignore EP s that are polling.
13	1h RW	**HS IN ASYNC Active Polling EP Mask (HSIAAPEPM):** Determines if the Async Active for IN HS/FS/LS masks/ignores EP s that are polling due to NAK. 0 HS IN ASYNC Active will include EP s that are polling. 1 HS IN ASYNC Active will mask/ignore EP s that are polling.
12:11	0h RW	**HS INTR IN Periodic Active Policy Control (HSIIPAPC):** Controls how the HS INTR IN periodic active is used to generate the global periodic active. This will determine how the smallest service interval among active EP s and number of active EP s are used. 0 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold OR Numb of EP Threshold values meet the requirement. 1 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold AND Numb of EP Threshold values meet the requirement. 2 Always allow HS INTR EP s to be used in the generation of the global Periodic Active indication. 3 Never allow HS INTR EP s to be used in the generation of the global Periodic Active indication
10:4	0h RW	**HS INTR IN Periodic Active Num of EP Threshold (HSIIPANEPT):** Defines the threshold used to determine if Periodic Active may include HS/FS/LS INTR IN EP active indication. If there are more than NumEPThreshold active HS/FS/LS INTR EP s then they may be included as part of the periodic active generation.
3:0	0h RW	**HS INTR IN Periodic Active Service Interval Threshold (HSIIPASIT):** Defines the Service Interval threshold used to determine if Periodic Active will include HS/FS/LS INTR IN EP active indication. If there are any active HS/FS/LS INTR EP s with a service interval less than or equal to this threshold then they may be included as part of the periodic active generation.

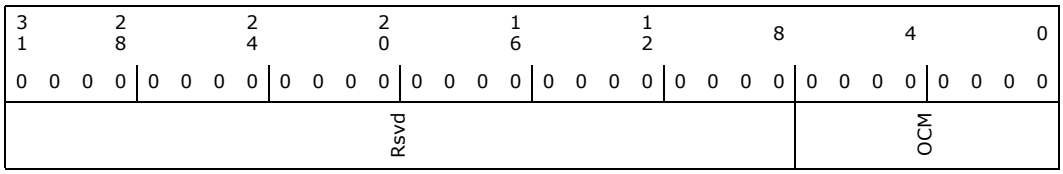
19.1.301 XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1_MMIO)—Offset 86B0h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Rsvd (Rsvd):** Reserved
7:0	0h RW/L	**OC Mapping (OCM)**

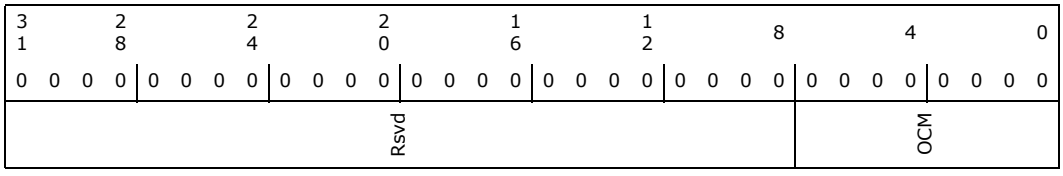
19.1.302 XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM2_MMIO)—Offset 86B4h

Reserved

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Rsvd (Rsvd):** Reserved
7:0	0h RW/L	**OC Mapping (OCM)**

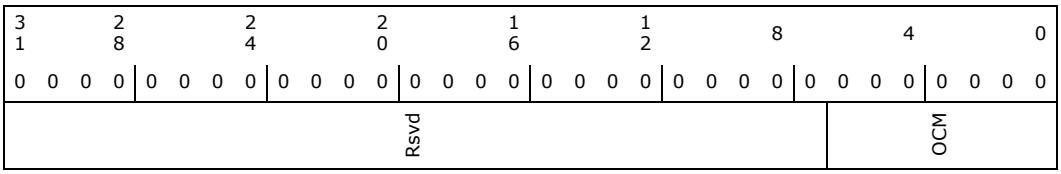
19.1.303 XHCI USB3 Overcurrent Pin Mapping 1 (U3OCM1_MMIO)—Offset 86D0h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



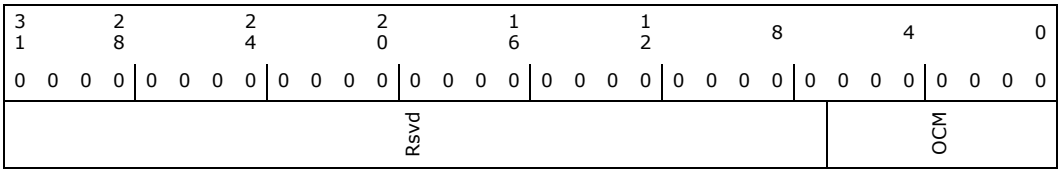
Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Rsvd (Rsvd)**
6:0	0h RW/L	**OC Mapping (OCM)**

19.1.304 XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM2_MMIO)—Offset 86D4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Rsvd (Rsvd)**
6:0	0h RW/L	**OC Mapping (OCM)**

19.1.305 XHCC3 (XHCC3_MMIO)—Offset 86FCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (Rsvd1):** Reserved
3	0h RW	**Error Handling : Disable Command Parity Check (DISABLE_COMMAND_PARITY_CHECK):** When set to 1, XHCI Host Controller disables checking of Command Parity on command received as a target on its IOSF Primary interface
2	0h RW	**Error Handling : Disable Data Parity Check (DISABLE_DATA_PARITY_CHECK):** When set to 1, XHCI Host Controller disables checking of Data Parity on data received as a target on its IOSF Primary interface
1	1h RW	**Error Handling : Enable ECC Error Response (ENABLE_ECC_ERROR_RESPONSE):** When set to 1, XHCI Host Controller will check for ECC on RFs (that support ECC) and halt operation when uncorrectable ECC is detected
0	0h RW/L	**Function Disable (FXN_DISABLE):** When set will disable the xHC from being operational.

19.1.306 Debug Capability ID Register (DCID)—Offset 8700h

This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 5100Ah

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved (RSVD)**
20:16	5h RW	**Debug Capability Event Ring Segment Table Max (DCERSTM):** Note: This register is sticky.
15:8	10h RW	**Next Capability Pointer (NCP):** Note: This register is sticky.
7:0	Ah RW	**Capability ID (CID):** Note: This register is sticky.

19.1.307 Debug Capability Doorbell Register (DCDB)—Offset 8704h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Reserved (RSVD)**
15:8	0h RW	**Doorbell Target (DBTGT):** This field defines the target of the doorbell reference. The table below defines the Debug Capability notification that is generated by ringing the doorbell. Value Definition 0 Data EP 1 OUT Enqueue Pointer Update 1 Data EP 1 IN Enqueue Pointer Update 2:255 Reserved This field returns '0' when read and the value should be treated as undefined by software.
7:0	0h RW	**Reserved (RSVD_1)**

19.1.308 Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)—Offset 8708h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Reserved (RSVD)**
15:0	0h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Debug Capability Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the DCERST Max field in the DCID register Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'.

19.1.309 Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)—Offset 8710h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:4	0h RW	**Event Ring Segment Table Base Address Register (ERSTBAR):** This field defines the high order bits of the start address of the Debug Capability Event Ring Segment Table. Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'.
3:0	0h RW	**Reserved (RSVD)**

19.1.310 Debug Capability Event Ring Dequeue Pointer Register (DCERDP)—Offset 8718h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:4	0h RW	**Dequeue Pointer (DQP):** This field defines the high order bits of the 64-bit address of the current Debug Capability Event Ring Dequeue Pointer. Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'.
3	0h RW	**Reserved (RSVD)**
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in.

19.1.311 Debug Capability Control Register (DCCTRL)—Offset 8720h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Debug Capability Enable (DCE)**

Bit Range	Default & Access	Field Name (ID): Description
30:24	0h RO	**Device Address (DADDR)**
23:16	0h RO	**Debug Max Burst Size (DMBS)**
15:5	0h RO	**Reserved (RSVD)**
4	0h RW/C	**DbC Run Change (DRC)**
3	0h RW/1S	**Halt IN TR (HIT)**
2	0h RW/1S	**Halt OUT TR (HOT)**
1	0h RW	**Link Status Event Enable (LSE)**
0	0h RO	**DbC Run (DCR)**

19.1.312 Debug Capability Status Register (DCST)—Offset 8724h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Debug Port Number (DPNUM):** This field provides the ID of the Root Hub port that the Debug Capability has been automatically attached to. The value is '0' when the Debug Capability is not attached to a Root Hub port.
23:1	0h RO	**Reserved (RSVD)**
0	0h RO	**Event Ring Not Empty (ERNE):** When '1', this field indicates that the Debug Capability Event Ring has a Transfer Event on it. It is automatically cleared to '0' by the xHC when the Debug Capability Event Ring is empty, i.e. the Debug Capability Enqueue Pointer is equal to the Debug Capability Event Ring Dequeue Pointer register.

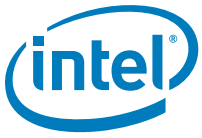
19.1.313 Debug Capability Port Status and Control Register (DCPORTSC)—Offset 8728h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD)**
23	0h RW/C	**Port Config Error Change (CEC):** This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it.
22	0h RW/C	**Port Link Status Change (PLC):** This flag is set to '1' due to the following PLS transitions: U0 -) U3 Suspend signaling detected from Debug Host U3 -) U0 Resume complete Polling -) Disabled Training Error Ux or Recovery -) Inactive Error Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'
21	0h RW/C	**Port Reset Change (PRC):** This bit is set when reset processing on this port is complete (i.e. a '1' to '0' transition of PR). '0' = No change. '1' = Reset complete.Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'.
20:18	0h RO	**Reserved (RSVD_1)**
17	0h RW/C	**Connect Status Change (CSC):** '1' = Change in Current Connect Status. '0' = No change. Indicates a change has occurred in the port's Current Connect Status. The xHC sets this bit to '1' for all changes to the Debug Device connect status, even if system software has not cleared an existing DbC Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, hardware will be "setting" an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'.
16:14	0h RO	**Reserved (RSVD_2)**
13:10	0h RO	**Port Speed (PSPD):** This field identifies the speed of the port. This field is only relevant when a Debug Host is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. 0 Undefined Speed 1-15 Protocol Speed ID (PSI) Note: The Debug Capability onlydoes not supports LS, FS, or HS operation.
9	0h RO	**Reserved (RSVD_3)**
8:5	4h RO	**Port Link State (PLS):** This field reflects its current link state. This field is only relevant when a Debug Host is attached (Debug Port Number) '0'). Value Meaning 0 Link is in the U0 State 1 Link is in the U1 State 2 Link is in the U2 State 3 Link is in the U3 State (Device Suspended) 4 Link is in the Disabled State 5 Link is in the RxDetect State 6 Link is in the Inactive State 7 Link is in the Polling State 8 Link is in the Recovery State 9 Link is in the Hot Reset State 15:10 Reserved Note: Transitions between different states are not reflected until the transition is complete.



Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Port Reset (PR):** '1' = Port is in Reset. '0' = Port is not in Reset. This bit is set to '1' when the bus reset sequence as defined in the USB Specification is detected on the Root Hub port assigned to the Debug capability. It is cleared when the bus reset sequence is completed by the Debug Host, and the DbC shall transition to the USB Default state. A '0' to '1' transition of this bit shall clear DCPORTSC PED ('0'). This field is '0' if DCE or CCS are '0'.
3:2	0h RO	**Reserved (RSVD_4)**
1	0h RW	**Port Enabled/Disabled (PED):** Default = '0'. '1' = Enabled. '0' = Disabled. This flag shall be set to '1' by a '0' to '1' transition of CCS or a '1' to '0' transition of the PR. When PED transitions from '1' to '0' due to the assertion of PR, the port's link shall transition to the Rx.Detect state. This flag may be used by software to enable or disable the operation of the Root Hub port assigned to the Debug Capability. The Debug Capability Root Hub port operation may be disabled by a fault condition (disconnect event or other fault condition, e.g. a LTSSM Polling substate timeout, tPortConfiguration timeout error, etc.), the assertion of DCPORTSC PR, or by software. 0 = Debug Capability Root Hub port is disabled. 1 = Debug Capability Root Hub port is enabled. When the port is disabled (PED = '0') the port's link shall enter the SS.Disabled state and remain there until PED is reasserted ('1') or DCE is negated ('0'). Note that the Root Hub port is remains mapped to Debug Capability while PED = '0'. While PED = '0' the Debug Capability will appear to be disconnected to the Debug Host. Note, this bit is not affected by PORTSC PR bit transitions. This field is '0' if DCE or CCS are '0'.
0	0h RO	**Current Connect Status (CCS):** '1' = A Root Hub port is connected to a Debug Host and assigned to the Debug Capability. '0' = No Debug Host is present. This value reflects the current state of the port, and may not correspond to the value reported by the Connect Status Change (CSC) field in the Port Status Change Event that was generated by a '0' to '1' transition of this bit. This flag is '0' if Debug Capability Enable (DCE) is '0'.

19.1.314 Debug Capability Context Pointer Register (DCCP)—Offset 8730h

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:4	0h RW	**Debug Capability Context Pointer Register (DCCPR):** This field defines the high order bits of the start address of the Debug Capability Context data structure associated with the Debug Capability. Software shall initialize this register before setting the Debug Capability Enable bit in the Debug Capability Control Register to '1'.
3:0	0h RO	**Reserved (RSVD)**

19.1.315 Debug Capability Device Descriptor Info Register 1 (DCDDI1)—Offset 8738h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 80870000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	8087h RW	**Vendor ID (VID):** This field is presented by the Debug Device in the USB Device Descriptor idVendor field.
15:8	0h RO	**Reserved (RSVD)**
7:0	0h RW	**DbC Protocol (DBCPR):** This field is presented by the Debug Device in the USB Interface Descriptor bInterfaceProtocol field. Value Function 0 Debug Target vendor defined. 1 GNU Remote Debug Command Set supported. 2-255 Reserved.

19.1.316 Debug Capability Device Descriptor Info Register 2 (DCDDI2)—Offset 873Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Device Revision (DREV):** This field is presented by the Debug Device in the USB Device Descriptor bcdDevice field.
15:0	0h RW	**Product ID (PID):** This field is presented by the Debug Device in the USB Device Descriptor idProduct field.

19.1.317 Debug Capability Descriptor Parameters (DCDP)—Offset 8740h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 30C3h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD)**
23:16	0h RW	**Max Power Field (MPF):** This field will be used by USB Debug Device to report maximum power consumption when the device is fully operational. This value is returned by bMaxPower field in response to Configuration Descriptor read from the debug device. Note: bU1DevExitLat and bU2DevExitLat fields returned in BOS Descriptor read will be taken from the corresponding fields from the Host Controller space.
15:8	30h RW/S	**NEXT CAPABILITY POINTER (NCP)**
7:0	C3h RW/S	**Capability ID (CID)**

19.1.318 Debug Device Control ODMA (DBGDEV_CTRL_ODMA_REG)—Offset 8748h

This register contains a number of fields that provide a specific level of configurability for the OUT DMA that is part of Debug Device logic. This configurability is above and beyond that defined in the xHCI specification.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RW	**Reserved (RSVD)**
18	0h RW	**Enable ACK FIFO credit accounting (EN_ACK_FCA):** Setting this field will enable ACK FIFO credit accounting. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP
17:14	0h RW	**Reserved (RSVD_1)**

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**Enable ACK FIFO ICA mechanisms (EN_ACK_FIFO_ICA):** Setting this field will enable ACK FIFO individual credit accounting mechanisms for Async vs. Periodic Endpoints. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP
12:9	0h RW	**Reserved (RSVD_2)**
8	0h RW	**Clear ownership of context semaphore (CL_OWN_CS):** Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the Out DMA Response and Completion Finite State Machines
7	0h RW	**Return OD ACK credits (RET_OD_ACK_CR):** Setting this field generates a pulse that implicitly returns all of the Out DMA ACK credits on all ports
6	0h RW	**Reserved (RSVD_3)**
5	0h RW	**Return ODCF SM to idle state (RET_ODCF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Completion Finite State Machine into the IDLE state
4	0h RW	**Return ODRF SM to idle state (RET_ODRF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Response Finite State Machine into the IDLE state
3	0h RW	**Return ODRDF SM to idle state (RET_ODRDF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Read Finite State Machine into the IDLE state
2:0	0h RW	**Reserved (RSVD_4)**

19.1.319 DBC Control Register 1 (DBCCTL_REG)—Offset 8760h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved (RSVD):** RSVD
7	0h RW	**SW_DCE_SEL (SW_DCE_SEL)**
6:3	0h RW	**DISC_RXD_CNT (DISC_RXD_CNT)**
2	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**Force DCE Mode (FORCE_DCE_MODE):** 0: When DCE is set, the DbC switches to Mode 2 1: When DCE is set, the DbC switches to Mode 3
0	0h RW	**Force Disconnect upon DCE (FORCE_DISCONNECT_ON_DCE):** If this bit is set by BIOS, the DbC will temporarily disconnect from the remote host if the DCE is set, and shortly thereafter re-connect. This allows the DbC to switch from Mode1 to Mode2 or Mode 3 operation upon DCE being set.

19.1.320 (PORT1_PROFILE_ATTRIBUTES_REG0)—Offset 890Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.321 (PORT1_PROFILE_ATTRIBUTES_REG1)—Offset 8910h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.322 (PORT1_PROFILE_ATTRIBUTES_REG2)—Offset 8914h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.323 (PORT1_PROFILE_ATTRIBUTES_REG3)—Offset 8918h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.324 (PORT1_PROFILE_ATTRIBUTES_REG4)—Offset 891Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.325 (PORT1_PROFILE_ATTRIBUTES_REG5)—Offset 8920h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.326 (PORT1_PROFILE_ATTRIBUTES_REG6)—Offset 8924h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.327 (PORT1_PROFILE_ATTRIBUTES_REG7)—Offset 8928h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.328 (PORT1_PROFILE_ATTRIBUTES_REG8)—Offset 892Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.329 (PORT1_PROFILE_ATTRIBUTES_REG9)—Offset 8930h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.330 (PORT1_PROFILE_ATTRIBUTES_REG10)—Offset 8934h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.331 (PORT1_PROFILE_ATTRIBUTES_REG11)—Offset 8938h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.332 (PORT1_PROFILE_ATTRIBUTES_REG12)—Offset 893Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.333 (PORT1_PROFILE_ATTRIBUTES_REG13)—Offset 8940h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.334 (PORT1_PROFILE_ATTRIBUTES_REG14)—Offset 8944h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.335 (PORT1_PROFILE_ATTRIBUTES_REG15)—Offset 8948h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.336 (PORT1_PROFILE_ATTRIBUTES_REG16)—Offset 894Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.337 (PORT1_PROFILE_ATTRIBUTES_REG17)—Offset 8950h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.338 (PORT1_PROFILE_ATTRIBUTES_REG18)—Offset 8954h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.339 (PORT1_PROFILE_ATTRIBUTES_REG19)—Offset 8958h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.340 (PORT1_PROFILE_ATTRIBUTES_REG20)—Offset 895Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.341 (PORT1_PROFILE_ATTRIBUTES_REG21)—Offset 8960h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.342 (PORT1_PROFILE_ATTRIBUTES_REG22)—Offset 8964h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.343 (PORT1_PROFILE_ATTRIBUTES_REG23)—Offset 8968h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.344 (PORT1_PROFILE_ATTRIBUTES_REG24)—Offset 896Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.345 (PORT1_PROFILE_ATTRIBUTES_REG25)—Offset 8970h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.346 (PORT1_PROFILE_ATTRIBUTES_REG26)—Offset 8974h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.347 (PORT1_PROFILE_ATTRIBUTES_REG27)—Offset 8978h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.348 (PORT1_PROFILE_ATTRIBUTES_REG28)—Offset 897Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.349 (PORT1_PROFILE_ATTRIBUTES_REG29)—Offset 8980h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.350 (PORT1_PROFILE_ATTRIBUTES_REG30)—Offset 8984h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.351 (PORT1_PROFILE_ATTRIBUTES_REG31)—Offset 8988h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.352 (PORT1_PROFILE_ATTRIBUTES_REG32)—Offset 898Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.353 (PORT1_PROFILE_ATTRIBUTES_REG33)—Offset 8990h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.354 (PORT1_PROFILE_ATTRIBUTES_REG34)—Offset 8994h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.355 (PORT1_PROFILE_ATTRIBUTES_REG35)—Offset 8998h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.356 (PORT1_PROFILE_ATTRIBUTES_REG36)—Offset 899Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.357 (PORT1_PROFILE_ATTRIBUTES_REG37)—Offset 89A0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.358 (PORT1_PROFILE_ATTRIBUTES_REG38)—Offset 89A4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.359 (PORT1_PROFILE_ATTRIBUTES_REG39)—Offset 89A8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.360 (PORT1_PROFILE_ATTRIBUTES_REG40)—Offset 89ACh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.361 (PORT1_PROFILE_ATTRIBUTES_REG41)—Offset 89B0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.362 (PORT1_PROFILE_ATTRIBUTES_REG42)—Offset 89B4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.363 (PORT1_PROFILE_ATTRIBUTES_REG43)—Offset 89B8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.364 (PORT1_PROFILE_ATTRIBUTES_REG44)—Offset 89BCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.365 (PORT1_PROFILE_ATTRIBUTES_REG45)—Offset 89C0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.366 (PORT1_PROFILE_ATTRIBUTES_REG46)—Offset 89C4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.367 (PORT1_PROFILE_ATTRIBUTES_REG47)—Offset 89C8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.368 (PORT1_PROFILE_ATTRIBUTES_REG48)—Offset 89CCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.369 (PORT1_PROFILE_ATTRIBUTES_REG49)—Offset 89D0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.370 (PORT1_PROFILE_ATTRIBUTES_REG50)—Offset 89D4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.371 (PORT1_PROFILE_ATTRIBUTES_REG51)—Offset 89D8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.372 (PORT1_PROFILE_ATTRIBUTES_REG52)—Offset 89DCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.373 (PORT1_PROFILE_ATTRIBUTES_REG53)—Offset 89E0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.374 (PORT1_PROFILE_ATTRIBUTES_REG54)—Offset 89E4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.375 (PORT1_PROFILE_ATTRIBUTES_REG55)—Offset 89E8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.376 (PORT1_PROFILE_ATTRIBUTES_REG56)—Offset 89ECh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.377 (PORT1_PROFILE_ATTRIBUTES_REG57)—Offset 89F0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.378 (PORT1_PROFILE_ATTRIBUTES_REG58)—Offset 89F4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.379 (PORT1_PROFILE_ATTRIBUTES_REG59)—Offset 89F8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.380 (PORT1_PROFILE_ATTRIBUTES_REG60)—Offset 89FCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.381 (PORT1_PROFILE_ATTRIBUTES_REG61)—Offset 8A00h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.382 (PORT1_PROFILE_ATTRIBUTES_REG62)—Offset 8A04h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.383 (PORT1_PROFILE_ATTRIBUTES_REG63)—Offset 8A08h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	**Reserved (RSVD1)**
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

19.1.384 GLOBAL_TIME_SYNC_CAP_REG (GLOBAL_TIME_SYNC_CAP_REG)—Offset 8E10h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 12C9h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED (RSVD)**
15:8	12h RO	**Next Capability pointer (NCP)**
7:0	C9h RO	**Capability ID (CID)**

19.1.385 GLOBAL_TIME_SYNC_CTRL_REG (GLOBAL_TIME_SYNC_CTRL_REG)—Offset 8E14h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**RESERVED (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW/1S	**Time Stamp Counter Capture Initiate (TIME_STAMP_CNTR_CAPTURE_INITIATE):** SW sets this bit to initiate a time capture. Once the time capture is complete and the time values are valid in the Local and Global time capture registers, HW clears the bit.

19.1.386 MICROFRAME_TIME_REG (MICROFRAME_TIME_REG)—Offset 8E18h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**RESERVED (RSVD)**
29:16	0h RO	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits [29:16] reflect state of bits [13:0] of FRINDEX
15:13	0h RO	**RESERVED1 (RSVD1)**
12:0	0h RO	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done via Bus Interval Adjust (BIA).

19.1.387 GLOBAL_TIME_LOW_REG (GLOBAL_TIME_LOW_REG)—Offset 8E20h

Global Time Value (Low):

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**GLOBAL_TIME_LOW_REG (GLOBAL_TIME_LOW):** Global Time Value (Low):

19.1.388 GLOBAL_TIME_HI_REG (GLOBAL_TIME_HI_REG)—Offset 8E24h

Global Time Value (High):

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**GLOBAL_TIME_HI_REG (GLOBAL_TIME_HI):** Global Time Value (High):

19.1.389 Debug Status Capability Register (DEBUG_STATUS_CAPABILITY_REG)—Offset 8E58h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: CBh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Rsvd (Rsvd)**
15:8	0h RO	**Next Capability Pointer (NCP)**
7:0	CBh RO	**Capability ID (CID)**

19.1.390 Host Ctrl USB3 Soft Error Count Register 1 (HOST_CTRL_USB3_ERR_COUNT_REG1)—Offset 8E5Ch

This register is updated by hardware and cleared by software

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED (cfg_reserved)**
15:0	0h RO	**USB3_SOFT_ERR_CNT (cfg_usb3_soft_error_cnt)**

19.1.391 Host Ctrl USB3 Soft Error Count Register 2 (HOST_CTRL_USB3_ERR_COUNT_REG2)—Offset 8E60h

This register is updated by hardware and cleared by software

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED (cfg_reserved)**
15:0	0h RO	**USB3_SOFT_ERR_CNT (cfg_usb3_soft_error_cnt)**

19.1.392 Host Ctrl USB3 Soft Error Count Register 3 (HOST_CTRL_USB3_ERR_COUNT_REG3)—Offset 8E64h

This register is updated by hardware and cleared by software

Access Method

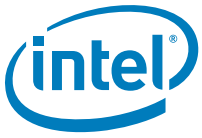
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED (cfg_reserved)**
15:0	0h RO	**USB3_SOFT_ERR_CNT (cfg_usb3_soft_error_cnt)**

19.1.393 Host Ctrl USB3 Soft Error Count Register 4 (HOST_CTRL_USB3_ERR_COUNT_REG4)—Offset 8E68h

This register is updated by hardware and cleared by software



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED (cfg_reserved)**
15:0	0h RO	**USB3_SOFT_ERR_CNT (cfg_usb3_soft_error_cnt)**

19.1.394 Host Ctrl USB3 Soft Error Count Register 5 (HOST_CTRL_USB3_ERR_COUNT_REG5)—Offset 8E6Ch

This register is updated by hardware and cleared by software

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED (cfg_reserved)**
15:0	0h RO	**USB3_SOFT_ERR_CNT (cfg_usb3_soft_error_cnt)**

19.1.395 Host Ctrl USB3 Soft Error Count Register 6 (HOST_CTRL_USB3_ERR_COUNT_REG6)—Offset 8E70h

This register is updated by hardware and cleared by software

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED (cfg_reserved)**
15:0	0h RO	**USB3_SOFT_ERR_CNT (cfg_usb3_soft_error_cnt)**

19.1.396 Host Ctrl USB3 Soft Error Count Register 7 (HOST_CTRL_USB3_ERR_COUNT_REG7)—Offset 8E74h

This register is updated by hardware and cleared by software

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**RESERVED (cfg_reserved)**
15:0	0h RO	**USB3_SOFT_ERR_CNT (cfg_usb3_soft_error_cnt)**

19.1.397 IOSFCTL - Control Register (IOSFCTL)—Offset 0h

Register controls some of the behaviors of the IOSF interface

Access Method

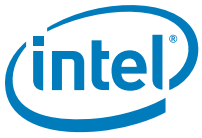
Type: CR Register (Size: 32 bits)	**Device:** **Function:**

Default: Fh

Range	Access Type	Default (reset)	Description
31:8	RO	0x0 (rst)	**Reserved0** Reserved
7:7	RW	0x0 (rst)	**NSNPDIS** Non-snoop Disable. When set, all requests from the Bridge on IOSF Primary are snooped.
6:4	RO	0x0 (rst)	**Reserved1** Reserved
3:0	RW	0xF (rst)	**MAX_RD_PEND** Maximum number of upstream outstanding reads from the Bridge toward the IOSF Primary Channel

19.1.398 Power Management Control Register (PMCTL)—Offset 1D0h

Register controls Power Management function of the Bridge



Access Method

Type: CR Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Range	Access Type	Default (reset)	Description
31:6	RO	0x0 (rst)	**Reserved0** Reserved
5:5	RW	0x0 (rst)	**IOSFSB_TRUNK_GATE_EN** SB Trunk Gate enable
4:4	RW	0x0 (rst)	**IOSFPRIM_TRUNK_GATE_EN** Primary Trunk Gate Enable
3:3	RW	0x0 (rst)	**IOSFSBCLK_GATE_EN** SB clock gate enable
2:2	RW	0x0 (rst)	**OCPCLK_TRUNK_GATE_EN** OCP clk trunk gate enable
1:1	RW	0x0 (rst)	**OCPCLK_GATE_EN** OCP clock gate enable
0:0	RW	0x0 (rst)	**IOSFPRIMCLK_GATE_EN** Primary clock gate enable

19.1.399 PCI Configuration Control 1 Register (PCICFGCTR1)—Offset 200h

Controls the PCI configuration space.

Access Method

Type: CR Register (Size: 32 bits)	**Device:** **Function:**

Default: 100h

Range	Access Type	Default (reset)	Description
31:29	RO	0x0 (rst)	**Reserved0** Reserved
28:28	RW	0x0 (rst)	**DIS_PCI_IDLE_CAP1**

Range	Access Type	Default (reset)	Description
27:20	RW	0x0 (rst)	**PCI_IRQ1** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	RW	0x0 (rst)	**ACPI_IRQ1** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	RW	0x1 (rst)	**IPIN1** Interrupt Pin: This register indicates the values to be used for Global Interrupts.
7:7	RW	0x0 (rst)	**BAR1_DISABLE1** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	RW	0x0 (rst)	**PME_Support1** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1:1	RW	0x0 (rst)	**ACPI_INTR_EN1** When set, the Bridge uses ACPI Sideband opcodes for messages When cleared, the Bridge uses global IOSF opcodes
0:0	RW	0x0 (rst)	**PCI_CFG_DIS1** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

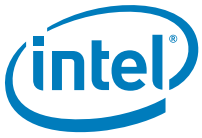
19.1.400 c73usb280_USB2 PER PORT (USB2_PER_PORT_PP0)—Offset 4100h

Access Method

Type: CR Register (Size: 32 bits)	**Device:** **Function:**

Default: 100h

Range	Access Type	Default (reset)	Description
31:31	RW	0x0 (SUS)	**PPUOCGE (Per-Port UTMI_CLK Output Clock Gating Enable)** 1: Dynamic Clock Gating is enabled based on L1/L2 suspend indicator. This is the recommended setting for SYNOPSYS based controllers. 0: Output UTMI_CLK is running unless USB PLL is shutdown. This is the recommended setting for FRESCO based controllers.



Range	Access Type	Default (reset)	Description
30:30	RW	0x0 (SUS)	**RXENAC (RX EN AFE Control)** 1: Enables the dynamic RX EN behavior. This allows compensation code updates at various boundaries. 0: Disables the dynamic RX EN behavior (function of TXVALID only). RXENAC, RXBIASAC: 00: Legacy mode 01: Illegal 10: Allows additional code update window 11: Allows additional code update window with power saving
29:29	RW	0x0 (SUS)	**RXBIASAC (RX BIAS AFE Control)** 1: Enables the AFE bias control 0: Disables the AFE bias control This bit is only valid when internal RXBIAS policy is selected (SELSBRXBIASEN = 0b).
28:28	RW	0x0 (SUS)	**TXBIASAC (TX BIAS AFE Control)** 1: Enables the AFE bias control 0: Disables the AFE bias control This bit is only valid when internal TXBIAS policy is selected (SELSBTXBIASEN = 0b).
27:27	RW	0x0 (SUS)	**RXCLKENACG (RX CLKEN AFE Clock Gating)** 1: Enables the AFE clock gating 0: Disables the AFE clock gating This bit is only valid when internal RXCLKEN policy is selected (SELRXCLKEN = 0b).
26:26	RW	0x0 (SUS)	**TXCLKENACG (TX CLKEN AFE Clock Gating)** 1: Enables the AFE clock gating 0: Disables the AFE clock gating This bit is only valid when internal TXCLKEN policy is selected (SELTXCLKEN = 0b).
25:25	RW	0x0 (SUS)	**ENHSCLK2PORT (ENHSCLK2PORT)** This per-port pin will generate HS clock data pattern for testing purposes for that port and ignore the core data during Tx: 1: The port will transmit 10101..clock data pattern when txen=1. 0: The port will resume to c73usb280_normal operation where data is generated by the controller.
24:24	RW	0x0 (SUS)	**SELSBRXBIASEN (SELSBRXBIASEN)** This is to select between the UTMI internal vs. side-band control over the AFE RX bias enable signal. 1 - select side-band control from Intel SIP controller. 0 - select UTMI internally generated control. This is to be used with third party or external controller IP.

Range	Access Type	Default (reset)	Description
23:23	RW	0x0 (SUS)	**SELSBTXBIASEN (SELSBTXBIASEN)** This is to select between the UTMI internal vs. side-band control over the AFE TX bias enable signal. 1 - select side-band control from Intel SIP controller. 0 - select UTMI internally generated control. This is to be used with third party or external controller IP.
22:22	WO	0x0 (SUS)	**RSVD (RSVD)** RSVD
21:21	RW	0x0 (SUS)	**SELTXCLKEN (SELTXCLKEN)** This is to select between internal mode vs. side-band control on the TX clock enable signal. 0 - override for TXCLKEN to be internally controlled. To be used with third party or external controller IP. 1 - select side-band control from Intel SIP controller.
20:20	RW	0x0 (SUS)	**SELRXCLKEN (SELRXCLKEN)** This is to select between internal mode vs. side-band control on the RX clock enable signal. 0 - override for RXCLKEN to be internally controlled. To be used with third party or external controller IP. 1 - select side-band control from Intel SIP controller.
19:17	RW	0x2 (SUS)	**PERPORTRXISET (PerPort HS Receiver Bias)** Config bit (per port) HS Receiver Bias current offset bit (2:0) 000 - 80uA 001 - 90uA 010 (default) - 100uA 011 - 110uA 100 - 120uA 101 - 130uA 110 - 140uA 111 - 150uA
16:16	RW	0x1 (SUS)	**PERPORTTXPRECHARGEEN (PerPort Common Mode Pre-charge)** Config bit (per port) To select whether to enable or disable the common mode pre-charge during SOP and EOP. Pre-charge hold for 4 cycles before first data transmission. This is to allow common choke ring back to settle down before driving first data bit to meet eye opening spec. 1 - pre-charge ON 0 - pre-charge OFF
15:15	RW	0x1 (SUS)	**RXERROR_FIXEN (RX ERROR FIX ENABLE)** When reg_utmi_rxerror_fixen = 1'b1, Rxerror fix is enabled When reg_utmi_rxerror_fixen = 1'b0, Rxerror fix is disabled

Range	Access Type	Default (reset)	Description
14:14	RW	0x1 (SUS)	**PERPORTTXPEHALF (PerPort Half Bit Pre-emphasis)** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis
13:11	RW	0x3 (SUS)	**PERPORTPETXISET (PerPort HS Pre-emphasis Bias)** Config bit (per port) HS Pre-emphasis Bias current offset bit2 (2:0) Value Preempen: deempen = 01 Preempen: deempen = 10 Preempen: deempen = 11 (preemphasis strength/demphasis strength) Value (De-emphasis ON) (Pre-emphasis ON) (preemphasis strength/demphasis strength) 000 0mV 0mV 0mV 001 40.5mV 20.5mV 20.5mV/20.5mV 010 60.5mV 30.5mV 30.5mV/30.5mV 011 102mV 52mV 52mV/52mV 100 102mV 52mV 52mV/52mV 101 142mV 72.5mV 72.5mV/72.5mV 110 162.5mV 85mV 85mV/85mV 111 202.5mV 105mV 105mV/105mV
10:8	RW	0x2 (SUS)	**PERPORTTXISET (PerPort HS Transmitter Bias)** Config bit (per port) HS Pre-emphasis Bias current offset bit2 (2:0) Value Preempen: deempen = 01 Preempen: deempen = 10 Preempen: deempen = 11 (preemphasis strength/demphasis strength) Value (De-emphasis ON) (Pre-emphasis ON) (preemphasis strength/demphasis strength) 000 0mV 0mV 0mV 001 40.5mV 20.5mV 20.5mV/20.5mV 010 60.5mV 30.5mV 30.5mV/30.5mV 011 102mV 52mV 52mV/52mV 100 102mV 52mV 52mV/52mV 101 142mV 72.5mV 72.5mV/72.5mV 110 162.5mV 85mV 85mV/85mV 111 202.5mV 105mV 105mV/105mV
7:4	RW	0x8 (SUS)	**PORTRESERVED (PORTRESERVED_0123)** PORTRESERVED (PORTRESERVED): Reserved pin for future functionality of the respective ports iusbportreserved[0] is used for differential disconnect purpose. 0 - Differential disconnect and HS squelch uses the same voltage reference (sqref-sqrefb = diffdiscref - diffdiscrefb) 1 - Differential disconnect and HS squelch uses different voltage reference (sqref-sqrefb != diffdiscref - diffdiscrefb) iusbportreserved[1] - iusbafedaten_h_dfxoveride 0 - functional mode. iusbafedaten will be controlled functionally by PCS logic 1 - test mode. The iusbafedaten will be forced to 1 to ensure CL TX is never blocked. iusbportreserved[3:2] - reserved for future functionality.

Range	Access Type	Default (reset)	Description
3:3	RW	0x0 (SUS)	**CLTXEMIREDCCTBYPASS (CL TX EMI Reduction Circuit Bypass)** Assert 1 to bypass the EMI reduction circuit. Default is 0b. AFE pin remains as PORTRESERVED for this project.
2:2	RW	0x0 (SUS)	**PERPORTALLPORTZ (PERPORT ALLPORTZ)** Legacy pin. No longer carries any functionality as the pull-down enable is now controlled by ilane5:0usbpdnen_h
1:1	RW	0x0 (SUS)	**PERPORTPPDPDMBSEL (PERPORT PPDPDMBSEL)** Config bit to select comparator 2:1 mux input either dp or dm for HS TX per port current calibration 1 - select dp (for debug purpose only) 0 - select dm (without 1.5K pullup)
0:0	RW	0x1 (SUS)	**PERPORTTXEOS (PERPORT TX EOS protection enable)** Set to 1b enables the TX EOS protection. To protect high speed driver passgate.

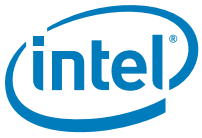
19.1.401 GLB ADP VBUS COMP REG (GLB_ADP_VBUS_COMP_REG)—Offset 402Bh

Access Method

Type: CR Register (Size: 32 bits)	**Device:** **Function:**

Default: 2A4005h

Range	Access Type	Default (reset)	Description
31:30	RO/V	0x0 (SUS)	RSVD (RESERVED)
29:23	RW	0x0 (SUS)	RSVD_1 (RESERVED)
22:22	RW	0x0 (SUS)	**DIFFDISCEN (DIFFDISCEN)** Feed directly to SHIP or AFE : AFE Functional or Test Mode : Functional 0: Used existing single ended disconnect detector 1:Mux over to enable differential disconnect detector.
21:21	RW	0x1 (SUS)	**VBUS_SESS_SAMPLING_EN (VBUS SESSION SAMPLING ENABLE)** Enable vbus session comparator for vbus and session sampling.



Range	Access Type	Default (reset)	Description
20:19	RW	0x1 (SUS)	**IUSBADPRER (IUSBADPRER)** Adp vref select signal 2'b00 = 0.65 2'b01 = 0.675 2'b10 = 0.7 2'b11 = 0.725
18:16	RW	0x2 (SUS)	**IUSBVBUSREF (IUSBVBUSREF)** Vbus vref select signal 3'b000 = 0.7 3'b001 = 0.75 3'b010 = 0.8 3'b011 = 0.85 3'b100 = 0.9 3'b101 = 0.95 3'b110 = xxxx 3'b111 = xxxx
15:14	RW	0x1 (SUS)	**IUSBVBUSSVLDREF_LV (IUSBVBUSSVLDREF_LV)** Vbus sense valid vref select signal 2'b00 = 0.2 2'b01 = 0.25 2'b10 = 0.3 2'b11 = 0.4
13:13	RO/V	0x0 (SUS)	**OUSBIDDIGLVGEN (OUSBIDDIGLVGEN)** OTG ID dig status readout.
12:12	RO/V	0x0 (SUS)	**OUSBVBUSSSESVLDLVGEN (OUSBVBUSSSESVLDLVGEN)** VBUS sense status readout.
11:11	RO/V	0x0 (SUS)	**OUSBVBUSVLDLVGEN (OUSBVBUSVLDLVGEN)** VBUS valid status readout.
10:10	RO/V	0x0 (SUS)	**OADPSNSUSBLVGEN (OADPSNSUSBLVGEN)** ADP sense status readout.
9:9	RO/V	0x0 (SUS)	**OADPPRBUSBLVGEN (OADPPRBUSBLVGEN)** ADP probe status readout.
8:8	RW	0x0 (SUS)	**IUSBIDPULLUPLVGEN (IUSBIDPULLUPLVGEN)** OTG ID dig pullup enable for DCIO.
7:7	RW	0x0 (SUS)	**IUSBADPCHRGENLVGEN (IUSBADPCHRGENLVGEN)** ADP charge enable for DCIO.
6:6	RW	0x0 (SUS)	**IADPSNSENUSBLVGEN (IADPSNSENUSBLVGEN)** ADP sense enable for DCIO.
5:5	RW	0x0 (SUS)	**IADPPRBENUSBLVGEN (IADPPRBENUSBLVGEN)** ADP probe enable for DCIO.
4:4	RW	0x0 (SUS)	**DCMONOTGADP (DC OTG ADP MONITOR)** Enable DC monitor for OTG and ADP.

Range	Access Type	Default (reset)	Description
3:2	RW	0x1 (SUS)	**USBVBUSOFSTMAXLIMIT (USBVBUSOFSTMAXLIMIT)** This register defines the counter limit for the VBUS valid detector offset cancellation SM. 11b = not supporting 10b = not supporting 01b = 5-bits 00b = 4-bits
1:0	RW	0x1 (SUS)	**USBADPOFSTMAXLIMIT (USBADPOFSTMAXLIMIT)** This register defines the counter limit for the ADP probe detector offset cancellation SM. 11b = Not supporting 10b = Not supporting 01b = 5-bits 00b = 4-bits

19.1.402 c73usb280_USB2 GLOBAL PORT 2 (USB2_GLOBAL_PORT_2)—Offset 402Ch

Access Method

Type: CR Register (Size: 32 bits)	**Device:** **Function:**

Default: 1E25000h

Range	Access Type	Default (reset)	Description
31:30	RO/V	0x0 (SUS)	RSVD_RO (RESERVED)
29:28	RW	0x0 (SUS)	RSVD_RW (RESERVED)
27:27	RW	0x0 (SUS)	**REG_GBLCORE_PWRGATE_EN (Global lane core power gating enable)** Feed directly to SHIP or AFE: AFE Functional or Test Mode: Test Mode 1: Enable global lane core well shuf off once all ports are off. 0:Disable global lane shut off when all per-port are off. ie. Global lane will remain on and not autonomously shuf off once all ports are off.
26:26	RW	0x0 (SUS)	**HSDEVCHRPBYPASS (HSDEVCHRPBYPASS)** Enable to bypass the pull-up on Dm pin during device chirp K mode.
25:25	RW	0x0 (SUS)	RSVD_1 (RESERVED)

Range	Access Type	Default (reset)	Description
24:23	RW	0x3 (SUS)	**IUSBEOSDETREFEN (EOS REFERENCE ENABLE SELECT)** Sel signal to select eosdet vref 2'b00 = 0.75V 2'b01 = 0.725V 2'b10 = 0.775V 2'b11 = 0.8V
22:22	RW	0x1 (SUS)	**PWRGATE_FORCE_ON (Power gating DFX force on)** 1: Disallow perport power gating. All LDO remains ON regardless of ihost_phy_pwr_req or suspendm. 0:Allow dynamic control based on ihost_phy_pwr_req or suspend.
21:21	RW	0x1 (SUS)	**PWRGATE_SUSPENDM_POLICY (Per Port Power gating suspend policy)** 1: Per Port power gating based on utmi suspendm only. Once suspendm=0, phy will initiate perport power gating. 0: Per Port power gating based on utmi suspendm and ihost_ppXpwr_req.
20:18	RW	0x0 (SUS)	**IUSBCMPPWRDROOPDET_FREQSEL (High pass frequency select)** Power droop detect control signals to select for High Pass frequency. 000b - 1MHz 001b - 5MHz 010b - 10MHz 011b - 50MHz 100b - 100MHz 101b - 500MHz 110b - Invalid 111b - Invalid
17:17	RW	0x1 (SUS)	**IUSBCMPPWRDROOPDET_CAPBYP_H (Bypass capacitor)** Signal to bypass the high pass filters capacitor.
16:16	RW	0x0 (SUS)	**IUSBCMPPWRDROOPDET_RST_H (Power droop detect reset)** Power droop detect reset signal for common lane.
15:15	RO/V	0x0 (SUS)	**IUSBCMPPWRDROOPDETOUT_H (Power droop detect observation)** Power droop detect output observation signal for common lane.
14:13	RW	0x2 (SUS)	**IUSBCFGKICKTX_L (Transmit kicker)** Kicker strength control during HS Tx 00 - Turn Off kicker 01 - Lowest kicker strength 10 - Default kicker strength 11 - Highest kicker strength

Range	Access Type	Default (reset)	Description
12:11	RW	0x2 (SUS)	**IUSBCFGKICKRX_L (Receive kicker)** Kicker strength control during HS Rx 00 - Turn Off kicker 01 - Lowest kicker strength 10 - Default kicker strength 11 - Highest kicker strength
10:10	RW	0x0 (SUS)	**IUSBMONPORTEN (Enable monitoring or power droop)** 1b1 when monitoring or power droop detector is enabled. 1b0 when using external clock.
9:9	RW	0x0 (SUS)	**VBUSCOMP_DISABLE (DISABLING AFE VBUS COMPARATOR)** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Test mode 1: Disable AFE vbus comparator 0: Allow dynamic sampling enabling
8:8	RW	0x0 (SUS)	**IDDIGCOMP_DISABLE (DISABLING AFE IDDIG COMPARATOR)** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Test mode 1: Disable AFE iddig comparator 0: Allow dynamic sampling enabling
7:7	RW	0x0 (SUS)	**SENSECOMP_DISABLE (DISABLING AFE SENSE COMPARATOR)** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Test mode 1: Disable AFE sense comparator 0: Allow dynamic sampling enabling
6:6	RW	0x0 (SUS)	**DCMONCOMP (DC MONITOR FOR COMPARATOR)** Enable DC monitor for comparator.
5:4	RW	0x0 (SUS)	**SNSPOL (Session valid Sample Policy)** 00: Bypass 01: Force SNS valid output to 0b to the UTMI+ 10: Force SNS valid output to 1b to the UTMI+ 11: Sample mode (10 ms period)
3:2	RW	0x0 (SUS)	**VBSPOL (VBUS valid Sample Policy)** 00: Bypass 01: Force VBUS valid output to 0b to the UTMI+ 10: Force VBUS valid output to 1b to the UTMI+ 11: Sample mode (10 ms period)

Range	Access Type	Default (reset)	Description
1:0	RW	0x0 (SUS)	**IDSPOL (IDDIG Sample Policy)** 00: Bypass 01: Force IDDIG output to 0b to the UTMI+ 10: Force IDDIG output to 1b to the UTMI+ 11: Sample mode (2 ms period)

19.1.403 c73usb280_USB2 COMPBG (USB2_COMPBG)—Offset 7F04h

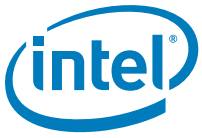
Access Method

Type: CR Register (Size: 32 bits)	**Device:** **Function:**

Default: 600h

Range	Access Type	Default (reset)	Description
31:31	RW	0x0 (SUS)	**COMPRESERVED9 (COMPRESERVED9)** Spare bits related to compensation.
30:30	RO/V	0x0 (SUS)	**CAL_IN_PROGRESS (CAL IN PROGRESS)** This bit is to indicate that Compensation State Machine is still in progress and rcomp/icomp value are not yet updated
29:29	WO	0x0 (SUS)	**FORCECOMP (FORCECOMP)** When set to 1b, this will force global comp Finite State Machine to start calibrating. BIOS has to wait for sufficient time for the calibration complete. This is a pulse trigger event.
28:28	RW	0x0 (SUS)	**COMPRESERVED8 (COMPRESERVED8)** Spare bits related to compensation.
27:27	RW	0x0 (SUS)	**COMPRESERVED7 (COMPRESERVED7)** Spare bits related to compensation.
26:26	RW	0x0 (SUS)	**COMPRESERVED6 (COMPRESERVED6)** Spare bits related to compensation.
25:23	RW	0x0 (SUS)	**OFSTCALREFEN (OFSTCALREFEN)** Comparator Offset CAL reference voltage (500mV) select signal to select reference voltage to AFE global COMP. ofstrefen2 ofstrefen1 ofstrefen0 0 0 0 500mV 0 0 1 300mV 0 1 0 350mV 0 1 1 400mV 1 0 0 450mV 1 0 1 550mV 1 1 0 600mV 1 1 1 650mV

Range	Access Type	Default (reset)	Description
22:22	RW	0x0 (SUS)	**COMPRESERVED5 (COMPRESERVED5)** Spare bits related to compensation.
21:21	RW	0x0 (SUS)	**COMPRESERVED4 (COMPRESERVED4)** Spare bits related to compensation.
20:20	RW	0x0 (SUS)	**COMPRESERVED3 (COMPRESERVED3)** Spare bits related to compensation.
19:17	RW	0x0 (SUS)	**IREFREFEN (IREFREFEN)** IREF reference voltage (300mV) select signal to select reference voltage to AFE global icomp. irefrefen2 irefrefen1 irefrefen0 Value 1 1 1 500mV 1 1 0 487.5mV 1 0 1 475mV 1 0 0 462.5mV 0 1 1 437.5mV 0 1 0 425mV 0 0 1 412.5mV 0 0 0 450mV
16:16	RW	0x0 (SUS)	**COMPRESERVED2 (COMPRESERVED2)** Spare bits related to compensation.
15:15	RW	0x0 (SUS)	**COMPRESERVED1 (COMPRESERVED1)** Spare bits related to compensation. COMPRESERVED1 is used to select the voltage reference for SE HS DISC or DIFF HS DISC. 1b is to select voltage reference for DIFF HS DISC 0b is to select voltage refrence for SE HS DISC
14:13	RW	0x0 (SUS)	**HSSQREFEN (HSSQREFEN)** HS SQ reference voltage (312.5mV) enable signal to select reference voltage to AFE hssqrefen1 hssqrefen0 Vref 1 1 350mV 1 0 325mV 0 1 300mV 0 0 312.5mV



Range	Access Type	Default (reset)	Description
12:11	RW	0x0 (SUS)	**HSSQREFBEN (HSSQREFBEN)** HS SQ reference voltage (200mV) enable signal to select reference voltage to AFE hssqrefben1 hssqrefben0 Vref 1 1 250mV 1 0 225mV 0 1 175mV 0 0 200mV
10:9	RW	0x3 (SUS)	**HSDISCREFEN (HSDISCREFEN)** HS DISC BG reference voltage (675mV) select signal to select reference voltage to AFE port. When COMPRESERVED1=0b, SE HS DISC is selected. This register is combined together with HSSQREFBEN register to produce the following truth table. discrefen1 discrefen0 discrefben1 discrefben0 Vref x 1 1 1 575mV x 1 1 0 650mV x 1 0 1 800mV x 1 0 0 750mV x 0 1 1 625mV x 0 1 0 700mV x 0 0 1 600mV x 0 0 0 675mV(default) When COMPRESERVED1=1b, Diff HS DISC is selected discrefen1 discrefen0 discrefben1 discrefben0 Vref 1 1 1 1 437.5mV 1 1 1 0 562.5mV 1 1 0 1 812.5mV 1 1 0 0 687.5mV(default) 1 0 1 1 375mV 1 0 1 0 500mV 1 0 0 1 750mV 1 0 0 0 625mV 0 1 1 1 312.5mV 0 1 1 0 437.5mV 0 1 0 1 687.5mV 0 1 0 0 562.5mV 0 0 1 1 500mV 0 0 1 0 625mV 0 0 0 1 875mV 0 0 0 0 750mV
8:7	RW	0x0 (SUS)	**HSDISCREFBEN (HSDISCREFBEN)** HS DISC reference voltage enable signal to select reference voltage to AFE port. This bits are comnbined with iusbhsdiscrefen for final voltage selection depending on SE or Diff HS DISC mode

Range	Access Type	Default (reset)	Description
6:6	RW	0x0 (SUS)	**COMPRESERVED0 (COMPRESERVED0)** Spare bits related to compensation.
5:3	RW	0x0 (SUS)	**HSPUREFEN (HSPUREFEN)** HS Pull-up Rcal reference voltage (500mV) select signal to select reference voltage to AFE global comp. hspurefen2 hspurefen1 hspurefen0 Value 1 1 1 387.5mV 1 1 0 375mV 1 0 1 362.5mV 1 0 0 337.5mV 0 1 1 325mV 0 1 0 312.5mV 0 0 1 300mV 0 0 0 350mV
2:0	RW	0x0 (SUS)	**HSPDREFEN (HSPDREFEN)** HS Pull-Down RCAL reference voltage (500mV) select signal to select reference voltage to AFE global comp. hspdrefen2 hspdrefen1 hspdrefen0 Value 1 1 1 537.5mV 1 1 0 512.5mV 1 0 1 500mV 1 0 0 487.5mV 0 1 1 475mV 0 1 0 450mV 0 0 1 425mV 0 0 0 525mV

19.1.404 CONFIG_3—Offset 7014h

Access Method

Type: CR Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Range	Access Type	Default (reset)	Description
31:24	RW/V	(rst)	**i_sfrcalib_fmincnt (i_sfrcalib_fmincnt [31:24])** set to round(1.1GHz/Fref)-1 for proper SFR calibration
23:16	RW/V	(rst)	**i_sfrcalib_fmaxcnt (i_sfrcalib_fmaxcnt [23:16])** set to round(3.43GHz/Fref)-1 for proper SFR calibration

Range	Access Type	Default (reset)	Description
15:8	RW/V	(rst)	**i_tdccalib_osccnt (i_tdccalib_osccnt [15:8])** set to round(1.47GHz/Frefclk)-1 for proper TDC calibration
7:1	RW/V	(rst)	**i_locktimercnt_th (i_locktimercnt_th [7:1])** Set this bus to the number of refclk cycles after which the o_locktimer is asserted,

19.1.405 DBC_GP2_IN_PAYLOAD_BP_LOW—Offset 1Ch

Lower DW of Payload Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Range	Access Type	Default (reset)	Description
31:0	RW	0x0 (core)	**DBC_GP2_IN_PAYLOAD_BP_LOW (DBC_GP2_IN_PAYLOAD_BP_LOW)** Lower DW of Payload Address Pointer

19.1.406 DBC_GP2_IN_PAYLOAD_BP_HI—Offset 20h

Upper DW of Payload Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Range	Access Type	Default (reset)	Description
31:0	RW	0x0 (core)	**DBC_GP2_IN_PAYLOAD_BP_HI (DBC_GP2_IN_PAYLOAD_BP_HI)** Upper DW of Payload Address Pointer

19.1.407 DBC_GP2_IN_PAYLOAD_QUALIFIERS—Offset 24h

DbC GP2 OUT Payload Qualifiers

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Range	Access Type	Default (reset)	Description
31:22	RO	0x0 (core)	**RSVD (Reserved)**
21:8	RW	0x0 (core)	**DESTN_ID (DESTN_ID)** Decode_Mode[1:0] PSF[3:0] Port_Group[0:0] Port[3:0] Channel[2:0]
7:4	RO	0x0 (core)	**RSVD1 (RESERVED1)**
3:0	RW	0x0 (core)	**ROOT_SPACE (ROOT_SPACE)**

19.1.408 DBC_GP2_IN_STATUS_QUALIFIERS—Offset 34h

DbC GP2 OUT STATUS Qualifiers

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Range	Access Type	Default (reset)	Description
31:22	RO	0x0 (core)	**RSVD (Reserved)**
21:8	RW	0x0 (core)	DESTN_ID (DESTN_ID) Decode_Mode[1:0] PSF[3:0] Port_Group[0:0] Port[3:0] Channel[2:0]
7:4	RO	0x0 (core)	**RSVD1 (RESERVED1)**
3:0	RW	0x0 (core)	**ROOT_SPACE (ROOT_SPACE)**

19.1.409 DBC_GP2_IN_STATUS_BP_LOW—Offset 2Ch

Lower DW of STATUS Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Range	Access Type	Default (reset)	Description
31:0	RW	0x0 (core)	**DBC_GP2_IN_STATUS_BP_LOW (DBC_GP2_IN_STATUS_BP_LOW)** Lower DW of STATUS Address Pointer

19.1.410 DBC_GP2_IN_STATUS_BP_HI—Offset 30h

Upper DW of STATUS Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Range	Access Type	Default (reset)	Description
31:0	RW	0x0 (core)	**DBC_GP2_IN_STATUS_BP_HI (DBC_GP2_IN_STATUS_BP_HI)** Upper DW of STATUS Address Pointer

19.1.411 Power Control Enable (PCE_REG) —Offset 00A2h

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** **Function:**

Default: 8h

Range	Access Type	Default (reset)	Description
15:6	RO	0x0 (SUS)	Rsvd (Rsvd)
5:5	RW	0x0 (SUS)	**HAE (Hardware Autonomous Enable)** If set, then the PGCB may request a PG whenever it is idle.
4:4	RW	0x0 (SUS)	Rsvd1 (Rsvd1)
3:3	RW	0x1 (SUS)	**SE (Sleep Enable)** If clear, then IP will never asset Sleep to the retention flops. If set, then IP may assert Sleep during PGing. Note that some platforms may default this bit to 0, others to 1
2:2	RW	0x0 (SUS)	**D3_HOT_EN (D3 HOT ENABLE)** if set, then IP will PG when idle and the PMCSR register in the IP = 11
1:1	RW	0x0 (SUS)	**DEVIDLEN (DEVIDLE Enable)** If '1', then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set.

Range	Access Type	Default (reset)	Description
0:0	RW	0x0 (SUS)	**PMCRE (PMC Request Enable)** If this bit is set to '1', the function will power gate when idle and pmc_ip_sw_pg_req_b ='0'. NOTE: PMCSR[1:0] may be any value and the function must power gate if this bit is set and pmc_ip_sw_pg_req_b is asserted and the device is idle. Default value may be SOC and/or IP specific .

19.1.412 Super Speed Configuration 1 (SSCFG1) —Offset 00A8h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** **Function:**

Default: 8Fh

Range	Access Type	Default (reset)	Description
31:22	RW	0x0 (Core)	**ECO1 (ECO1)** ECO bits are used during silicon bringup for FIBing.
21:18	WO	0x0 (SUS)	**LFPSPMU3 (LFPS Power Management in U3 Enable)** This field allows xHC to turn off LFPS Receiver when the port is in U3. This allows the Host Controller to save some extra power (about 50W per port) in idle states if device connected on a port is not Resume capable or Resume enabled. This choice has to be done by BIOS and based on platform knowledge. For example, if an in-box device is not Resume Capable, BIOS could allow xHC to turn-off Rx LFPS when the port is in U3.Each bit represents a port. Bit (16) is for USB3.0 Port 0, Bit (17) is for USB3.0 Port 1 and so on.0 in a bit position: LFPS Receiver shall be kept enabled when the port is in U3. 1 in a bit position: LFPS Receiver shall be disabled when the port is in U3.
17:17	RW	0x0 (SUS)	**LFPSPME (LFPS Power Management Enable)** This field provides programmability of LFPS Receiver power management capability when USB3.0 ports are Disabled or in Disconnected state.0: Do not power manage LFPS receiver. LFPS receivers are enabled in all states. 1: Power manage LFPS receiver. LFPS receivers will be turned off if USB3.0 port is Disabled or Disconnected.Note: Default value is being kept at 0 in case EXI architecture/design takes the path of not doing dynamic Rx LFPS enabling for EXI signature detect and disable LFPS Power Management to keep Rx LFPS buffer on for debug.
16:16	RW	0x0 (Core)	**SSPPEN (USB3 SS Port Polling Enable)** 0: Prevent USB3 Super-speed port to start Polling.LFPS. 1: Allow USB3 Super-speed port to start Polling.LFPS. NOTE: This bit will take effect in allowing/preventing USB3 SS port from starting Polling.LFPS only if SSPPENAB is cleared.
15:15	RO	0x0 (Core)	Rsvd1 (Rsvd1)
14:14	RW	0x0 (Core)	**MPHYPGEU2 (MODPHY Power Gate Enable for U2)** This bit controls whether xHC will allow modPHY power gating or not when a port is in U2 state.Note that this single bit controls all ports of xHC.0b xHC shall not initiate Power Gate Request If xHC had initiated Power Gate Request before this bit is programmed to 0, xHC shall initiate the handshake to wake modPHY from power gated state. 1b xHC is enabled to initiate Power Gate Request if power gating conditions are met.

Range	Access Type	Default (reset)	Description
13:13	RW	0x0 (Core)	**MPHYPGENONU2 (MODPHY Power Gate Enable for non-U2 states)** This bit controls whether xHC will allow modPHY power gating or not when a port is in states other than U2.Note that this single bit controls all ports of xHC.0b xHC shall not initiate Power Gate Request If xHC had initiated Power Gate Request before this bit is programmed to 0, xHC shall initiate the handshake to wake modPHY from power gated state. 1b xHC is enabled to initiate Power Gate Request if power gating conditions are met.
12:12	RW	0x0 (Core)	**SSAAPE (xHC SS Async Active Propogation Enable)** This register controls the ss async active exposusre to PMC via the xHC active indication 0 SS Async Active is not propogated to PMC 1 SS Async Active is propogated to PMC
11:8	RO	0x0 (Core)	**Rsvd2 (Rsvd2)** Reserved
7:7	RW	0x1 (SUS)	**SSPPENAB (USB3 SS Port Polling Enable Active)** 0: Allow blocking of USB3 Super-speed port from starting Polling.LFPS. 1: Disallow blocking of USB3 Super-speed port from starting Polling.LFPS (A stepping behavior). NOTE: When this bit is cleared, Polling.LFPS blocking is controlled by SSPPEN bit.
6:6	RW	0x0 (SUS)	**ECO2 (ECO2)** ECO bits are used during silicon bringup for FIBing.
5:5	RW	0x0 (SUS)	**RXDETSTGDIS (Receiver Detect Staggering Disable)** When set, this regiter bit disables receiver detect staggering between all 6 USB3 lanes Note that the bit is ONLY meant for SW to disable the staggering if desired. Once it is set to disabled, SW is not allowed to re-enable the staggering by clearing the bit.
4:3	RW	0x1 (SUS)	**G2RXPTTV (Gotorxelecidle Polling Timer Timeout Value)** Timeout value for Gotorxelecidle Polling Timer: 00: 1 to 2 us (Simulation speed up mode only). 01: 19 to 20 us (Default). 10: 23 to 24 us. 11: 199 to 200 us. This register needs to be programmed when G2RXPOLLTMREN = 0.
2:2	RW	0x1 (SUS)	**G2RXPTE (Gotorxelecidle Polling Timer Enable)** If enabled (1), Gasket starts a timer after transmitting high speed data AND not receiving LFPS, and will only de-assert GoToRxElecIdle after timer expires during Polling. If disabled (0), Gasket will assert / de-assert GoToRxElecIdle purely based on Gotorxelecidle assertion upon RxElecIdle de-assertion (LFPS detected) enable bit (G2RXERXEE) and Gotorxelecidle assertion when not transmitting high speed data enable bit (G2RXETXHSDE)
1:1	RW	0x1 (SUS)	**G2RXERXEE (GotoRxElecidle Assertion Upon RxElecIdle Exit Enable)** When enabled (set to '1'), allow Gasket to assert GoToRxElecIdle to UAFE to turn off its receiver upon the de-assertion of GoToRxElecIdle (LFPS detected). This bit needs to be programmed when the USB3 port is not enabled.
0:0	RW	0x1 (SUS)	**G2RXETXHSDE (GotoRxElecidle Assertion When Transmitting High Speed Data Enable)** When enabled (set to '1'), allow Gaskets to assert GoToRxElecIdle to UAFE to turn off its receiver when not transmitting high speed data: P0 and TxElecIdle = 1. This bit needs to be programmed when the USB3 port is not enabled.

19.1.413 High Speed Configuration 1 (HSCFG1) —Offset 00ACh

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** **Function:**

Default: 100h

Range	Access Type	Default (reset)	Description
31:23	RW	0x0 (Core)	**ECO1 (ECO bits Core)** ECO bits are used during silicon bringup for FIBing.
22:22	RW	0x0 (Core)	**SOF_WINDOW_QUAL_DIS (SOF Window Qualification Disable)**
21:21	RW	0x0 (Core)	**FS_LS_SERIAL_MODE_BLOCK_DIS (FS/LS Serial Mode Blocking Disable)**
20:20	RW	0x0 (Core)	**RX_EN_OPT_DIS (RXEN Optimization Disable)**
19:19	RW	0x0 (Core)	**UTMI_GASKET_LOCAL_SUSPENDED_PORT (UTMI Gasket Local Suspended Port)** 480/60/48MHz Clock Gating Enable When set, enables the clock gating when a USB2 port is NOT in suspend. This mode is currently not recommended for production.
18:18	RW	0x0 (Core)	**UTMI_GASKET_LOCAL_SPEED_PORT (UTMI Gasket Local Speed Port)** 480/60/48MHz Clock Gating Enable When set, enables the clock gating when a USB2 port is in Suspend.
17:17	RW	0x0 (Core)	**RX_ACTIVE_EARLY_DEASSERTION_DISABLE (RXACTIVE Early Deassertion Disable)**
16:16	RW	0x0 (Core)	**RST_EN_CLK_CNTR_UPON_TX_VALID_DISABLE (Reset ENCLK Counter Upon TXValid Disable)**
15:11	RO	0x0 (Core)	Rsvd1 (Rsvd1)
10:10	RW	0x0 (Core)	**USBR_CLK_REQ_CONSOLIDATION_DIS (USBr Clock Request Consolidation Disable)** When set xHC will not take into account USBr for the request of bb_clock.
9:9	RW	0x0 (Core)	**HSAAPE (xHC HS Async Active Propogation Enable)** This register controls the hs async active exposusre to PMC via the xHC active indication 0 HS Async Active is not propogated to PMC 1 HS Async Active is propogated to PMC
8:8	RW	0x1 (Core)	**PAPE (xHC Periodic Active Propogation Enable)** This register controls the periodic active exposusre to PMC via the xHC active indication 0 Periodic Active is not propogated to PMC 1 Periodic Active is propogated to PMC
7:2	RW	0x0 (SUS)	**ECO2 (ECO bits SUS)** ECO bits are used during silicon bringup for FIBing.
1:1	RW	0x0 (SUS)	**RSVD**

Range	Access Type	Default (reset)	Description
0:0	RW	0x0 (SUS)	**RSVD**

19.1.414 GEN_REGRW4 —Offset 00BCh

General Purpose Read Write Register4

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Range	Access Type	Default (reset)	Description
31:3	RW	0x0 (rst)	**GEN_REG_RW4** reserved
2:2	RW	0x0 (rst)	**XDCI_PIPE_CLK_GATE_DIS** xdci pipe clock gating disable
1:1	RW	0x0 (rst)	**XDCI_SB_CLK_GATE_DIS** xdci sideband clock gating disable
0:0	RW	0x0 (rst)	**XDCI_PRIM_CLK_GATE_DIS** xdci primary clock gating disable

19.2 Registers Summary

Table 19-2. Summary of 0_20_0_USBx PCI Config Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Vendor ID (VID)—Offset 0h	8086h
2h	3h	Device ID (DID)—Offset 2h	8C31h
4h	5h	Command (CMD)—Offset 4h	0h
6h	7h	Device Status (STS)—Offset 6h	290h

Table 19-2. Summary of 0_20_0_USBx PCI Config Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8h	8h	Revision ID (RID)—Offset 8h	0h
9h	9h	Programming Interface (PI)—Offset 9h	30h
Ah	Ah	Sub Class Code (SCC)—Offset Ah	3h
Bh	Bh	Base Class Code (BCC)—Offset Bh	Ch
Dh	Dh	Master Latency Timer (MLT)—Offset Dh	0h
Eh	Eh	Header Type (HT)—Offset Eh	80h
10h	17h	Memory Base Address (MBAR)—Offset 10h	4h
2Ch	2Dh	USB Subsystem Vendor ID (SSVID)—Offset 2Ch	0h
2Eh	2Fh	USB Subsystem ID (SSID)—Offset 2Eh	0h
34h	34h	Capabilities Pointer (CAP_PTR)—Offset 34h	70h
3Ch	3Ch	Interrupt Line (ILINE)—Offset 3Ch	0h
3Dh	3Dh	Interrupt Pin (IPIN)—Offset 3Dh	0h
40h	43h	XHC System Bus Configuration 1 (XHCC1)—Offset 40h	1FDh
44h	47h	XHC System Bus Configuration 2 (XHCC2)—Offset 44h	3C000h
50h	53h	Clock Gating (XHCLKGTEN)—Offset 50h	0h
58h	5Bh	Audio Time Synchronization (AUDSYNC)—Offset 58h	0h
60h	60h	Serial Bus Release Number (SBRN)—Offset 60h	30h
61h	61h	Frame Length Adjustment (FLADJ)—Offset 61h	60h
62h	62h	Best Effort Service Latency (BESL)—Offset 62h	0h
70h	70h	PCI Power Management Capability ID (PM_CID)—Offset 70h	1h
71h	71h	Next Item Pointer #1 (PM_NEXT)—Offset 71h	80h
72h	73h	Power Management Capabilities (PM_CAP)—Offset 72h	C1C2h
74h	75h	Power Management Control/Status (PM_CS)—Offset 74h	8h
80h	80h	Message Signaled Interrupt CID (MSI_CID)—Offset 80h	5h
81h	81h	Next item pointer (MSI_NEXT)—Offset 81h	0h
82h	83h	Message Signaled Interrupt Message Control (MSI_MCTL)—Offset 82h	86h
84h	87h	Message Signaled Interrupt Message Address (MSI_MAD)—Offset 84h	0h
88h	8Bh	Message Signaled Interrupt Upper Address (MSI_MUAD)—Offset 88h	0h
8Ch	8Dh	Message Signaled Interrupt Message Data (MSI_MD)—Offset 8Ch	0h
90h	93h	Device Idle Capability (DEVIDLE)—Offset 90h	F0140009h
94h	97h	Vendor Specific Header (VSHDR)—Offset 94h	1400010h
98h	9Bh	SW LTR POINTER (SWLTRPTR)—Offset 98h	0h
9Ch	9Fh	Device Idle Pointer Register (DEVIDLEPTR)—Offset 9Ch	80AC1h
A0h	A1h	Device Idle Power ON Latency (DEVIDLEPOL)—Offset A0h	800h
A2h	A3h	High Speed Configuration 2 (HSCFG2)—Offset A4h	8h
A4h	A7h	High Speed Configuration 2 (HSCFG2)—Offset A4h	2000h
A8h	ABh	XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1)—Offset B0h	8Fh
B0h	B3h	XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1)—Offset B0h	0h

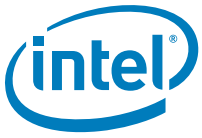


Table 19-2. Summary of 0_20_0_USBx PCI Config Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
B4h	B7h	XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM2)—Offset B4h	0h
B8h	BBh	XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM3)—Offset B8h	0h
BCh	BFh	XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM4)—Offset BCh	0h
D0h	D3h	XHCI USB3 Overcurrent Pin Mapping 1 (U3OCM1)—Offset D0h	0h
D4h	D7h	XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM2)—Offset D4h	0h
D8h	DBh	XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM3)—Offset D8h	0h
DCh	DFh	XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM4)—Offset DCh	0h
FCh	FFh	XHCC3 (XHCC3)—Offset FCh	2h

19.2.1 Vendor ID (VID)—Offset 0h

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 21 **Function:** 0

Default: 8086h

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID)**

19.2.2 Device ID (DID)—Offset 2h

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 21 **Function:** 0

Default: 8C31h

Bit Range	Default & Access	Field Name (ID): Description
15:0	8C31h RO/V	**Device ID (DID):** See Global Device ID table in Chap. 6 for value

19.2.3 Command (CMD)—Offset 4h

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved (RSVD)**
10	0h RW	**Interrupt Disable (ID):** When cleared to 0, the function is capable of generating interrupts. When 1, the function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable.
9	0h RO	**Fast Back to Back Enable (FBE)**
8	0h RW	**SERR# Enable (SERR):** When set to 1, the XHC is capable of generating (internally) SERR#.
7	0h RO	**Wait Cycle Control (WCC)**
6	0h RW	**Parity Error Response (PER):** When set to 1, the XHCI Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the XHCI specification. Note that this applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.
5	0h RO	**VGA Palette Snoop (VPS)**
4	0h RO	**Memory Write Invalidate (MWI)**
3	0h RO	**Special Cycle Enable (SCE)**
2	0h RW	**Bus Master Enable (BME):** When set, it allows XHC to act as a bus master. When cleared, it disable XHC from initiating transactions on the system bus.
1	0h RW	**Memory Space Enable (MSE):** This bit controls access to the XHC Memory Space registers. If this bit is set, accesses to the XHC registers are enabled. The Base Address register for the XHC should be programmed before this bit is set.
0	0h RO	**I/O Space Enable (IOSE):** Reserved as 0. Read-Only.

19.2.4 Device Status (STS)—Offset 6h

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 21 **Function:** 0

Default: 290h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE):** This bit is set by the SoC whenever a parity error is seen on the internal interface to the XHC host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a 1 to this bit location.
14	0h RW/1C	**Signaled System Error (SSE):** This bit is set by the SoC whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set. Software clears this bit by writing a 1 to this bit location.
13	0h RW/1C	**Received Master-Abort Status (RMA):** This bit is set when XHC, as a master, receives a master-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
12	0h RW/1C	**Received Target Abort Status (RTA):** This bit is set when XHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
11	0h RW/1C	**Signaled Target-Abort Status (STA):** This bit is used to indicate when the XHC function responds to a cycle with a target abort.
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only.
8	0h RW/1C	**Master Data Parity Error Detected (MDPED):** This bit is set by the SoC whenever a data parity error is detected on a XHC read completion packet on the internal interface to the XHC host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a 1 to this bit location.
7	1h RO	**Fast Back-to-Back Capable (FBBC):** Reserved as 1 Read-Only.
6	0h RO	**User Definable Features (UDF):** Reserved as 0. Read-Only.
5	0h RO	**66 MHz Capable (MC):** Reserved as 0. Read-Only.
4	1h RO	**Capabilities List (CL):** Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	0h RO/V	**Interrupt Status (IS):** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	0h RO	**Reserved (RSVD)**

19.2.5 Revision ID (RID)—Offset 8h

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO/V	**Revision ID (RID):** See Chap 6 for value.

19.2.6 Programming Interface (PI)—Offset 9h

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 30h

Bit Range	Default & Access	Field Name (ID): Description
7:0	30h RO	**Programming Interface (PI):** A value of 30h indicates that this USB Host Controller conforms to the XHCI specification.

19.2.7 Sub Class Code (SCC)—Offset Ah

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 3h

Bit Range	Default & Access	Field Name (ID): Description
7:0	3h RO	**Sub Class Code (SCC):** A value of 03h indicates that this is a Universal Serial Bus Host Controller.

19.2.8 Base Class Code (BCC)—Offset Bh

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: Ch

Bit Range	Default & Access	Field Name (ID): Description
7:0	Ch RO	**Base Class Code (BCC):** A value of 0Ch indicates that this is a Serial Bus controller.

19.2.9 Master Latency Timer (MLT)—Offset Dh

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Master Latency Timer (MLT):** Because the XHC controller is internally implemented with arbitration on an internal interface, it does not need a master latency timer. The bits will be fixed at 0.

19.2.10 Header Type (HT)—Offset Eh

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Multi-Function Bit (MFB):** Read only indicating single function device.
6:0	0h RO	**Configuration layout (CL):** Hardwired to 0 to indicate a standard PCI configuration layout.

19.2.11 Memory Base Address (MBAR)—Offset 10h

Value in this register will be different after the enumeration process.

Access Method

Type: CFG Register (Size: 64 bits)	**Device:** 21 **Function:** 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
63:16	0h RW	**Base Address (BA):** Bits (63:16) correspond to memory address signals (63:16), respectively. This gives 64 KB of relocatable memory space aligned to 64 KB boundaries.
15:4	0h RO	**Reserved (RSVD):** Reserved. Read-Only 0, this indicates that this function is requesting an 64KB block of memory.
3	0h RO	**Prefetchable (Prefetchable):** This bit is hardwired to 0 indicating that this range should not be prefetched.
2:1	2h RO	**Type (Type):** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** This bit is hardwired to 0 indicating that the base address field in this register maps to memory space

19.2.12 USB Subsystem Vendor ID (SSVID)—Offset 2Ch

This register is modified and maintained by BIOS

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/L	**USB Subsystem Vendor ID (SSVID):** This register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others.

19.2.13 USB Subsystem ID (SSID)—Offset 2Eh

This register is modified and maintained by BIOS

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/L	**USB Subsystem ID (SSID):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s).

19.2.14 Capabilities Pointer (CAP_PTR)—Offset 34h

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 70h

Bit Range	Default & Access	Field Name (ID): Description
7:0	70h RO	**Capabilities Pointer (CAP_PTR):** This register points to the starting offset of the capabilities ranges.

19.2.15 Interrupt Line (ILINE)—Offset 3Ch

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (ILINE):** This data is not used by the SoC. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

19.2.16 Interrupt Pin (IPIN)—Offset 3Dh

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW/L	**Interrupt pin (IPIN):** Bits 7:0 reflect the Interrupt Pin assigned to the host controller by the platform (and are hardwired).

19.2.17 XHC System Bus Configuration 1 (XHCC1)—Offset 40h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 1FDh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/O	**Access Control (ACCTRL):** This bit is used by BIOS to lock/ unlock lockable bits. When set to '1' the write access to bits locked by this bit is disabled (locked state). When set to '0', the write access to bit locked by this bit is enabled (unlocked state). Writable once after platform reset.
30:25	0h RW	**Reserved**
24	0h RW	**Master/Target Abort SERR (RMTASERR):** When set, it allows the out-of-band error reporting from the xHCI Controller to be reported as SERR# (if SERR# reporting is enabled) and thus set the STS.SSE bit.
23	0h RW/C	**Unsupported Request Detected (URD):** Set the HW when xHCI Controller received an unsupported request posted cycle. Cleared by SW when the bit is written with value of '1'.
22	0h RW	**Unsupported Request Report Enable (URRE):** When set this bit allows the URD bit to be reported as SERR# (if SERR# reporting is enabled) and thus set the STS.SSE bit.
21:19	0h RW	**Inactivity Initiated L1 Enable (IIL1E):** If programmed to non-zero, it allows L1 power managed to be enabled after the time-out period specified. 000: Disabled 001: 32 bb_cclk 010: 64 bb_cclk 011: 128 bb_cclk 100: 256 bb_cclk 101: 512 bb_cclk 110: 1024 bb_cclk 111: 131072 bb_cclk
18	0h RW	**XHC Initiated L1 Enable (XHCIL1E):** If set, allow the XHC initiated L1 power management to be enabled.
17	0h RW	**D3 Initiated L1 Enable (D3IL1E):** If set, allow PCI device state D3 initiated L1 power management to be enables.
16:12	0h RW	**Periodic Complete Pre Wake Time (PCPWT):** The value programmed in this field determines how far in advance of the start of the next micro-frame the host controller must de-assert the "Periodic Complete" signal . This allows for platform wake time before the next scheduled periodic transaction. The value programmed in this field represents the # of bytes consumed in the current micro-frame which is required to allow for the periodic complete to de-assert. This allows for a programmable time to cause the periodic complete to de-assert prior to the start of the next micro-frame. Register Format: Bits (16:12) represents the # of bytes remaining with a 256B granularity. Periodic Complete will de-assert if the bytes consumed in the current micro-frame is less

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**SW Assisted xHC Idle (SWAXHCI):** This bit being set will indicate xHC idleness (through SW means), which must be a '1' to allow L1 entry, and subsequently allow backbone clock to be gated. This bit is to be set by Intel xHCI driver after checking that the xHCI Controller will stay in idle state for a significant period of time, e.g. all ports disconnected. This bit can be cleared under the following conditions (see SWAXHCI Policy bits in xHC System Bus Configuration 2 register): n SW: SW could write 0 to clear this bit. n HW: HW, under policy control, will clear this bit on an MMIO access to the Host Controller. n HW: HW, under policy control, will clear this bit when HW exits Idle state.
10:8	1h RW	**L23 to Host Reset Acknowledge Wait Count (L23HRAWC):** If programmed to non zero, it allows a wait period after the L23 PHY has shutdown before returning host reset acknowledge to PMC. 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk
7:6	3h RW	**Upstream Type Arbiter Grant Count Posted (UTAGCP):** Grant count for IOSF upstream L2 request type arbiter for posted type
5:4	3h RW	**Upstream Type Arbiter Grant Count Non Posted (UDAGCNP):** Grant count for IOSF upstream L2 type arbiter for non-posted type
3:2	3h RW	**Upstream Type Arbiter Grant Count Completion (UDAGCCP) (UDAGCCP):** Grant count for IOSF upstream L2 type arbiter for completion type
1:0	1h RW	**Upstream Device Arbiter Grant Count (UDAGC) (UDAGC):** Grant count for IOSF upstream L1 device arbiter

19.2.18 XHC System Bus Configuration 2 (XHCC2)—Offset 44h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 3C000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**OC Configuration Done (OCCFGDONE):** This bit is used by BIOS to prevent spurious switching during OC configuration. It must be set by BIOS after configuration of the OC mapping bits is complete. Once this bit is set, OC mapping shall not be changed by SW.
30:26	0h RW	**Reserved.**

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW	**DMA Request Boundary Crossing Control (DREQBCC):** This bit controls the boundary crossing limit of each Read/Write Request. 0: 4KB 1: 64B
24:22	0h RW	**IDMA Read Request Size Control (IDMA_RDREQSZCTRL):** Read Request Size Control: This bit controls the maximum size of each Read Request. 000: 128B 001: 256B 011 - 110: Reserved 111: 64B
21	0h RW	**XHC Upstream Read Relaxed Ordering Enable (XHCUPRDROE):** This policy controls the Relaxed Ordering attribute for upstream reads. 0 - xHC will clear RO for all upstream read requests. 1 - xHC will set RO for all upstream read requests.
20	0h RW	**IOSF Sideband Register Access Disable (IOSFSRAD):** When set, it disables the IOSF sideband interface from accepting any host space register access.
19:14	Fh RW	**Upstream Non-Posted Pre-Allocation (UNPPA):** This field reserves data sizes, in 64 byte chunks, of the downstream completion resource. This value is zero based. 000000 - 111111: Pre-allocate 64 bytes - 4096 bytes If set greater than the default allows over-allocation If set less than default allows under-allocation Only allowed to be programmed when BME = 0 and no outstanding downstream completion
13:12	0h RW	**SW Assisted xHC Idle Policy (SWAXHCIP):** Note: Irrespective of the setting of this field, SW write of 0 to SWAXHCI will clear the bit. 00b (default): xHC HW clears SWAXHCI bit upon: n MMIO access to Host Controller OR n xHC HW exits Idle state 01b: xHC HW does not autonomously clear SWAXHCI bit. The bit could be cleared only by SW. 10b: xHC HW clears SWAXHCI upon MMIO acces to Host Controller. xHC HW exit from Idle state will not clear SWAXHCI. 11b: Reserved
11	0h RW	**MMIO Read After MMIO Write Delay Disable (RAWDD):** This field controls delay on MMIO Read after MMIO Write. 0b (Default): Delay MMIO Read after MMIO Write 1b: Do not delay MMIO Read after MMIO Write Note that this delay applies after the second of the two DW writes in the case where the IOSF Gasket splits a QW write into two single DW writes to the IP.
10	0h RW	**MMIO Write After MMIO Write Delay Enable (WAWDE):** This field controls delay on MMIO Write after previous MMIO Write. 0b (Default): Do not delay MMIO Write after previous MMIO Write 1b: Delay MMIO Write after previous MMIO Write Note that the delay count does not apply on the second of the two DW writes that are generated by IOSF Gasket when it splits a QW write into two. In other words, the second of the two DW writes could happen without any delay with respect to the first DW write. This choice is being made for ease of ECO. The delay count, in this case, will apply after the second of the two DW writes.

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW	**SW Assisted Cx Inhibit (SWACXIHB):** This field controls how the DMI L1 inhibit signal from USB3 to PMC will behave. 00: Never inhibit Cx 01: Inhibit Cx when Isochronous Endpoint is active (PPT Behavior) 10: Inhibit Cx when Periodic Active as defined in 40.4.3.2.1 11: Always inhibit Cx
7:6	0h RW	**SW Assisted DMI L1 Inhibit (SWADMIL1IHB):** This field controls how the DMI L1 inhibit signal from USB3 to DMI will behave. 00: Never inhibit DMI L1. 01: Inhibit DMI L1 when Isochronous Endpoint is active (PPT Behavior). 10: Inhibit DMI L1 when Priodic Active as defined in 40.4.3.2.1. 11: Inhibit DMI L1 if XHCC1.SWAXHCI = 0.
5:3	0h RW	**L1 Force P2 Clock Gating Wait Count (L1FP2CGWC):** If programmed to non zero, it allows L1 force P2 gating off the clock to be delayed after the time-out period specified. If wake up event is detected before the time-out, pclk remains alive and trigger L1 exit as though CPU host is causing the wake, 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk
2:0	0h RW	**Read Request Size Control (RDREQSZCTRL):** Read Request Size Control: This bit controls the maximum size of each Read Request. 000: 128B 001: 256B 010: 512B 011 - 110: Reserved 111: 64B

19.2.19 Clock Gating (XHCLKGTEN)—Offset 50h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Rsvd2 (Rsvd2):** Reserved
28	0h RW	**Nak'ing USB2.0 EPs for Backbone Clock Gating and PLL Shutdown (NUEFBCGPS):** This field controls whether Naking USB2.0 EPs, once in Naking low priority schedule, should be considered as active for the considerations for backbone clock gating and PLL shutdown or not. 0: Naking USB2.0 EPs are not considered to be active for Backbone Clock Gating and PLL Shutdown evaluation. 1: Naking USB2.0 EPs are considered to be active for Backbone clock gating and PLL shutdown evaluation.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW	**SRAM Power Gate Enable (SRAMPGTEN):** This register enables the SRAM Power Gating when PLL shutdown conditions for all clock domains have been met 0 - Disallow SRAM Power Gating. 1 - Allow SRAM Power Gating
26	0h RW	**SS Link PLL Shutdown Enable (SSLSE):** This register enables the SS P3 state to be exposed to PXP PLL Shutdown conditions on behalf of all USB SS Ports ontop of trunk clock gating. 0 - P3 state NOT allowed to result in PXP PLL shutdown. 1- P3 state allowed to result in PXP PLL shutdown
25	0h RW	**USB2 PLL Shutdown Enable (USB2PLLSE):** When set, this bit allows USB2 PLL to be shutdown when HS Link trunk clock is gated, and xHC can tolerate PLL spin up time for subsequent clock request. Note: if USB2 PLL Shutdown Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
24	0h RW	**IOSF Sideband Trunk Clock Gating Enable (IOSFSTCGE):** When set, this bit allows the IOSF sideband clock trunk to be gated when idle conditions are met.
23:20	0h RW	**HS Backbone PXP Trunk Clock Gate Enable (HSTCGE):** This register determines the HS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==) U0 or deeper (1) ==) NA (no support for U1) (2) ==) U2 (L1) or deeper (3) ==) U3 (L2) or deeper
19:16	0h RW	**SS Backbone PXP Trunk Clock Gate Enable (SSTCGE):** This register determines the SS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==) U0 or deeper (1) ==) U1 or deeper (2) ==) U2 or deeper (3) ==) U3 or deeper
15	0h RW	**XHC Ignore_EU3S (XHCIGEU3S):** This register determines if the xHC will use the EU3S as a condition to allow for Frame timer gating. 0 - xHC may allow frame timer to be gated when EU3S is set and all ports are in the required state. 1 - xHC may allow frame timer to be gated regardless of EU3S.
14	0h RW	**XHC Frame Timer Clock Shutdown Enable (XHCFTCLKSE):** This register determines if the xHC will allow the frame timer clock to be gated. 0 - xHC will not allow ICC PLL 96MHz output to be shutdown thus keeping the frame timer running. 1 - xHC will allow ICC PLL 96MHz output to be shutdown under specific conditions.
13	0h RW	**XHC Backbone PXP Trunk Clock Gate In Presence of ISOCH EP (XHCBBTCGIPISO):** This register controls the policy on allowing Backbone PXP trunk clock gate in the presence of IDLE ISOCH EP s with active DB. Allows the periodic active to be used in enabling Backbone PXP trunk clock gating of core clock. 0 Trunk gate of core clock is not allowed when ISOCH EP DB is set and ISOCH EP s are idle. 1 Allow trunk gate of core clock when ISOCH EP DB is set and ISOCH EP s are idle.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**XHC HS Backbone PXP Trunk Clock Gate U2 non RWE (XHCHSTCGU2NRWE):** This register controls the policy on allowing Backbone PXP trunk gating of core clock when there is atleast 1 non Remote Wake Enabled HS Port in U2. 0 Prevent trunk gate of core clock when a non RWE HS Port is in U2. 1 Allow trunk gate of core clock when a non RWE HS Port is in U2.
11:10	0h RW	**XHC USB2 PLL Shutdown Lx Enable (XHCUSB2PLLSDLE):** This register determines the HS Link state(s) which will be exposed to USB2 PLL Shutdown conditions on behalf of all USB2 HS Ports. Ly is a state allowed to result in USB2 PLL Shutdown when en(x) is asserted. (0) ==) L1 or deeper (1) ==) L2 or deeper
9:8	0h RW	**HS Backbone PXP PLL Shutdown Ux Enable (HSUXDMIPLLSE):** This register determines the Ux state(s) which will be exposed to PXP PLL Shutdown conditions. PLL Shutdown is allowed in: 00b Disabled (Link states shall be disabled for DMI PLL shutdown) 01b U0 or conditions for 10b setting. 10b U2 or conditions for 11b setting. 10b U3, Disconnected, Disabled or Powered-Off.
7:5	0h RW	**SS Backbone PXP PLL Shutdown Ux Enable (SSPLLSUE):** This register determines the Ux state(s) which will be exposed to DMI PLL Shutdown conditions. PLL Shutdown is allowed in: 000b Disabled (Link states shall be ignored for DMI PLL shutdown). 001b U0 or conditions for 010b setting 010b U1 or conditions for 011b setting 011b U2 or conditions for 100b setting 100b U3, Disconnected, Disabled or Powered-Off
4	0h RW	**XHC Backbone Local Clock Gating Enable (XHCBLCGE):** When set, this bit allows XHCI Controller IP backbone clock to be locally gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
3	0h RW	**HS Link Trunk Clock Gating Enable (HSLTCGE):** When set, this bit allows High Speed Link control's 480 MHz and its 48/60 MHz link clock trunk to be gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled.
2	0h RW	**SS Link Trunk Clock Gating Enable (SSLTCGE):** When set, this bit allows the SuperSpeed Link control's 250 MHz and its divided 125 MHz link clock trunk to ge gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**IOSF Backbone Trunk Clock Gating Enable (IOSFBTCGE):** When set, this bit allows the IOSF backbone clock trunk to be gated when idle conditions are met.
0	0h RW	**IOSF Gasket Backbone Local Clock Gating Enable (IOSFBLCGE):** When set, this bit allows the IOSF Gasket backbone clock to be locally gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled.

19.2.20 Audio Time Synchronization (AUDSYNC)—Offset 58h

This 32 bit register is used for audio stream synchronization across different devices. Global signal sample_now captures a value in AUDSYNC register.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Rsvd2 (Rsvd2)**
29:16	0h RO/V	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits (29:16) reflect state of bits (13:0) of FRINDEX
15:13	0h RO	**Rsvd1 (Rsvd1)**
12:0	0h RO/V	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done in FLA.

19.2.21 Serial Bus Release Number (SBRN)—Offset 60h

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 30h

Bit Range	Default & Access	Field Name (ID): Description
7:0	30h RO	**Serial Bus Release Number (SBRN):** A value of 30h indicates that this controller follows USB release 3.0.

19.2.22 Frame Length Adjustment (FLADJ)—Offset 61h

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit in the USBSTS register is a one. Changing value of this register while the host controller is operating yields undefined results.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 60h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved (RSVD):** Read-Only. These bits are reserved for future use and should read as "00".
6	1h RO	**No Frame Length Timing Capability (NO_FRAME_LENGTH_TIMING_CAP):** This flag is set to 1 to indicate that the host controller does not support a programmable Frame Length Timing Value field.
5:0	20h RO	**Frame Length Timing Value (FLTV):** SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (number of High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value

19.2.23 Best Effort Service Latency (BESL)—Offset 62h

Bset Effort Service Latency.

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW/L	**Default Best Effort Service Latency Deep (DBESLD):** Default Best Effort Service Latency (DBESLD) If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field. This is programmed by BIOS based on platform parameters.
3:0	0h RW/L	**Default Best Effort Service Latency (DBESL):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field. This is programmed by BIOS based on platform parameters.

19.2.24 PCI Power Management Capability ID (PM_CID)—Offset 70h

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
7:0	1h RO	**PCI Power Management Capability ID (PM_CID):** A value of 01h indicates that this is a PCI Power Management capabilities field.

19.2.25 Next Item Pointer #1 (PM_NEXT)—Offset 71h

This register is modified and maintained by BIOS

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Next Item Pointer #1 (PM_NEXT):** This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the Access Control bit is set to '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Values of: 80h implies next capability is MSI 00h implies that MSI capability is hidden. Note: This value is never expected to be programmed.

19.2.26 Power Management Capabilities (PM_CAP)—Offset 72h

Normally, this register is read-only to report capabilities to the power management software. In order to report different power management capabilities depending on the system in which the SoC is used, the write access to this register is controlled by the Access Control bit (ACCTRL). The value written to this register does not affect the hardware other than changing the value returned during a read. This register is modified and maintained by BIOS

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 21 **Function:** 0

Default: C1C2h

Bit Range	Default & Access	Field Name (ID): Description
15:11	18h RW/L	**PME_Support (PME_Support):** This 5-bit field indicates the power states in which the function may assert PME#. The SoC XHC does not support the D1 or D2 states. For all other states, the SoC XHC is capable of generating PME#. Software should never need to modify this field.
10	0h RW/L	**D2_Support (D2_Support):** The D2 state is not supported.
9	0h RW/L	**D1_Support (D1_Support):** The D1 state is not supported.
8:6	7h RW/L	**Aux_Current (Aux_Current):** The SoC XHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known.
5	0h RW/L	**DSI (DSI):** The SoC reports 0, indicating that no device-specific initialization is required.
4	0h RO	**Reserved (RSVD)**
3	0h RW/L	**PME Clock (PMEClock):** The SoC reports 0, indicating that no PCI clock is required to generate PME#.

Bit Range	Default & Access	Field Name (ID): Description
2:0	2h RW/L	**Version (Version):** The SoC reports 010, indicating that it complies with Revision 1.1 of the PCI Power Management Specification.

19.2.27 Power Management Control/Status (PM_CS)—Offset 74h

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 21 **Function:** 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PME_Status (PME_Status):** This bit is set when the SoC XHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14:13	0h RO	**Data_Scale (Data_Scale):** The SoC hardwires these bits to 00 because it does not support the associated Data register.
12:9	0h RO	**Data_Select (Data_Select):** The SoC hardwires these bits to 0000 because it does not support the associated Data register.
8	0h RW	**PME_En (PME_En):** A 1 enables the SoC XHC to generate an internal PME signal when PME_Status is 1. This bit must be explicitly cleared by the operating system each time it is initially loaded.
7:4	0h RO	**Reserved (RSVD)**
3	1h RO	**No Soft Reset (NSR):** No_Soft_Reset - When set ("1"), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. Transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	**Reserved (RSVD2)**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**PowerState (PowerState):** This 2-bit field is used both to determine the current power state of XHC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3hot state, the SoC must not accept accesses to the XHC memory range, but the configuration space must still be accessible.

19.2.28 Message Signaled Interrupt CID (MSI_CID)—Offset 80h

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 5h

Bit Range	Default & Access	Field Name (ID): Description
7:0	5h RO	**Capability ID (CID):** Indicates that this is an MSI capability

19.2.29 Next item pointer (MSI_NEXT)—Offset 81h

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW/L	**Next Pointer (NEXT):** Indicates that this is the last item on the capability list

19.2.30 Message Signaled Interrupt Message Control (MSI_MCTL)—Offset 82h

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 21 **Function:** 0

Default: 86h

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved (RSVD)**
8	0h RO	**Per-Vector Masking Capable (PVM):** Specifies whether controller supports MSI per vector masking. Not supported
7	1h RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages. This device is 64-bit capable.
6:4	0h RW	**Multiple Message Enable (MME):** Indicates the number of messages the controller should assert. This device supports multiple message MSI.
3:1	3h RO	**Multiple Message Capable (MMC):** Indicates the number of messages the controller wishes to assert. This field must be set by HW to reflect the number of Interrupters supported. Encoding number of Vectors requested (number of Interrupters) 000 1 001 2 010 4 011 8 100 16 101 32 110-111 Reserved
0	0h RW	**MSI Enable (MSIE):** If set to 1, MSI is enabled and the traditional interrupt pins are not used to generate interrupts. If cleared to 0, MSI operation is disabled and the traditional interrupt pins are used.

19.2.31 Message Signaled Interrupt Message Address (MSI_MAD)—Offset 84h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Addr (Addr):** Lower DW of system specified message address, always DWORD aligned
1:0	0h RO	**Reserved (RSVD)**

19.2.32 Message Signaled Interrupt Upper Address (MSI_MUAD)—Offset 88h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Addr (UpperAddr):** Upper DW of system specified message address.

19.2.33 Message Signaled Interrupt Message Data (MSI_MD)—Offset 8Ch

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data (Data):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD(15:0)) during the data phase of the MSI memory write transaction. The Multiple Message Enable field (bits 6-4 of the Message Control register) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010 indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000, the function is not permitted to modify the message data.

19.2.34 Device Idle Capability (DEVIDLE)—Offset 90h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VID (VID)**
27:24	0h RO	**REV (REV)**
23:16	14h RO	**Length (LENGTH):** Indicates that this capability is 16 bytes long.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Next Capability Pointer (NCP):** This field contains the offset to the next PCI Capability structure or 000h if no other items exist in the linked list of Capabilities.
7:0	9h RO	**Capability ID (CID)**

19.2.35 Vendor Specific Header (VSHDR)—Offset 94h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC Length (VSEC_LENGTH):** This field indicates the number of bytes in the entire VSEC structure, including the PCI Extended Capability header, the Vendor- Specific header, and the Vendor-Specific register
19:16	0h RO	**VSEC Rev (VSEC_REV):** This field is a vendor-defined version number that indicates the version of the VSEC structure. Software must qualify the Vendor ID and VSEC ID before interpreting this field.
15:0	10h RO	**VSEC ID (VSEC_ID):** This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure. Software must qualify the Vendor ID before interpreting this field.

19.2.36 SW LTR POINTER (SWLTRPTR)—Offset 98h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW LTR Update MMIO Offset Location (SW_LTR_UPDT_MMIO_OFFSET):** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set.

Bit Range	Default & Access	Field Name (ID): Description
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0's based AR Number of the BAR which contains the location of the SW LTR MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR Number. Bar 0 is the 1st BAR. The value of this register is a don't care, if the Valid bit is not set.
0	0h RO	**Valid (VALID):** Set to '1' to indicate that the function has implemented a SW LTR register as specified in the DevIdle that can be located using the SWLTRLOC register and BARNUM. Set to '0' to indicate that the function has not implemented a SW LTR register that is compliant to the DevIdle definition. This could be because the function has not implemented SW LTR at all, or has a device specific version of SW LTR.

19.2.37 Device Idle Pointer Register (DEVIDLEPTR)—Offset 9Ch

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 80AC1h

Bit Range	Default & Access	Field Name (ID): Description
31:4	80ACh RW/L	**DevIdle MMIO Offset Location (DEVIDLELOC):** This register contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set.
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0's based BAR Number of the BAR which contains the location of the DevIdle MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR Number. Bar 0 is the 1st BAR. The value of this register is a don't care, if the Valid bit is not set.
0	1h RW/L	**Valid (VALID):** Set to '1' to indicate that the function has implemented a DevIdle register as specified in the DevIdle that can be located using the DEVIDLELOC register and BARNUM. Set to '0' to indicate that the function has not implemented a DevIdle register that is compliant to the DevIdle definition. This could be because the function has not implemented DevIdle at all, or has a device specific version of DevIdle.

19.2.38 Device Idle Power ON Latency (DEVIDLEPOL)—Offset A0h

Access Method

Type: CFG Register (Size: 16 bits)	**Device:** 21 **Function:** 0

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Rsvd1 (Rsvd1)**
12:10	2h RW/L	**Power On Latency Scale (POLS):** Latency Scale multiplier: 010: 1us 011: 32us All other settings are reserved. The value of this register is multiplied with the Power On Latency Value (POLV) to provide the DevIdle power on exit latency multiplier scale from 1us to 32ms. This register is defined to be RWO (read-write-once) to allow BIOS to set the initial value. This register is undefined if the DevIdle.Valid bit is '0'.
9:0	0h RW/L	**Power On Latency Value (POLV):** 10-bit value that is multiplied by the Power On Latency Scale. A value of 0 indicates a power on latency of less than 1us. This register is defined to be RWO (read-write-once) to allow BIOS to set the initial value. This register is undefined if the DevIdle.Valid bit is '0'.

19.2.39 High Speed Configuration 2 (HSCFG2)—Offset A4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Rsvd1 (Rsvd1)**
18	0h RW	**PORT1_HOST_MODE_OVERRIDE (PORT1_HOST_MODE_OVERRIDE):** When set, this bit causes the Host_Device mux on port 1 to be forced into the Host mode.
17:16	0h RW	**eUSB2SEL (eUSB2SEL):** The two bits are associate with USB2 ports 1 - bit 16 and 2 - bit 2 0: Port is mapped to USB2 1: Port is mapped to eUSB2
15	0h RW	**HS ASYNC Active IN Mask (HSAAIM):** Determines if the Async Active will mask/ignore IN EP s. 0 HS ASYNC Active will include IN EP s. 1 HS ASYNC Active will mask/ignore IN EP s.
14	0h RW	**HS OUT ASYNC Active Polling EP Mask (HSOAAPEPM):** Determines if the Async Active for OUT HS/FS/LS masks/ignores EP s that are polling/PINGing (HS) due to NAK. 0 HS OUT ASYNC Active will include EP s that are polling. 1 HS OUT ASYNC Active will mask/ignore EP s that are polling.

Bit Range	Default & Access	Field Name (ID): Description
13	1h RW	**HS IN ASYNC Active Polling EP Mask (HSIAAPEPM):** Determines if the Async Active for IN HS/FS/LS masks/ignores EP s that are polling due to NAK. 0 HS IN ASYNC Active will include EP s that are polling. 1 HS IN ASYNC Active will mask/ignore EP s that are polling.
12:11	0h RW	**HS INTR IN Periodic Active Policy Control (HSIIPAPC):** Controls how the HS INTR IN periodic active is used to generate the global periodic active. This will determine how the smallest service interval among active EP s and number of active EP s are used. 0 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold OR Numb of EP Threshold values meet the requirement. 1 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold AND Numb of EP Threshold values meet the requirement. 2 Always allow HS INTR EP s to be used in the generation of the global Periodic Active indication. 3 Never allow HS INTR EP s to be used in the generation of the global Periodic Active indicaiton
10:4	0h RW	**HS INTR IN Periodic Active Num of EP Threshold (HSIIPANEPT):** Defines the threshold used to determine if Periodic Acive may include HS/FS/LS INTR IN EP active indication. If there are more than NumEPThreshold active HS/FS/LS INTR EP s then they may be included as part of the periodic active generation.
3:0	0h RW	**HS INTR IN Periodic Active Service Interval Threshold (HSIIPASIT):** Defines the Service Interval threshold used to determine if Periodic Acive will include HS/FS/LS INTR IN EP active indication. If there are any active HS/FS/LS INTR EP s with a service interval less than or equal to this threshold then they may be included as part of the periodic active generation.

19.2.40 XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1)—Offset B0h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Rsvd (Rsvd):** Reserved
4:0	0h RW/L	**OC Mapping (OCM)**

19.2.41 XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM2)—Offset B4h

Reserved

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Rsvd (Rsvd):** Reserved
4:0	0h RW/L	**OC Mapping (OCM)**

19.2.42 XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM3)—Offset B8h

Reserved

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Rsvd (Rsvd):** Reserved
4:0	0h RW/L	**OC Mapping (OCM)**

19.2.43 XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM4)—Offset BCh

Reserved

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Rsvd (Rsvd):** Reserved
4:0	0h RW/L	**OC Mapping (OCM)**

19.2.44 XHCI USB3 Overcurrent Pin Mapping 1 (U3OCM1)—Offset D0h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Rsvd (Rsvd)**
3:0	0h RW/L	**OC Mapping (OCM)**

19.2.45 XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM2)—Offset D4h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Rsvd (Rsvd)**
3:0	0h RW/L	**OC Mapping (OCM)**

19.2.46 XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM3)—Offset D8h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Rsvd (Rsvd)**
3:0	0h RW/L	**OC Mapping (OCM)**

19.2.47 XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM4)—Offset DCh

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Rsvd (Rsvd)**
3:0	0h RW/L	**OC Mapping (OCM)**

19.2.48 XHCC3 (XHCC3)—Offset FCh

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 0

Default: 2h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved (Rsvd1):** Reserved
3	0h RW	**Error Handling : Disable Command Parity Check (DISABLE_COMMAND_PARITY_CHECK):** When set to 1, XHCI Host Controller disables checking of Command Parity on command received as a target on its IOSF Primary interface
2	0h RW	**Error Handling : Disable Data Parity Check (DISABLE_DATA_PARITY_CHECK):** When set to 1, XHCI Host Controller disables checking of Data Parity on data received as a target on its IOSF Primary interface

Bit Range	Default & Access	Field Name (ID): Description
1	1h RW	**Error Handling : Enable ECC Error Response (ENABLE_ECC_ERROR_RESPONSE):** When set to 1, XHCI Host Controller will check for ECC on RFs (that support ECC) and halt operation when uncorrectable ECC is detected
0	0h RW/L	**Function Disable (FXN_DISABLE):** When set will disable the xHC from being operational.

19.3 Registers Summary

Table 19-3. Summary of 0_20_0_usbx_exi_on_dbc_registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	DBC_GP2_OUT_PAYLOAD_BP_LOW (DBC_GP2_OUT_PAYLOAD_BP_LOW)—Offset 0h	0h
4h	7h	DBC_GP2_OUT_PAYLOAD_BP_HI (DBC_GP2_OUT_PAYLOAD_BP_HI)—Offset 4h	0h
8h	Bh	DBC_GP2_OUT_PAYLOAD_QUALIFIERS (DBC_GP2_OUT_PAYLOAD_QUALIFIERS)—Offset 8h	0h
Ch	Fh	DBC_GP2_OUT_PAYLOAD_TRANSFER_LENGTH (DBC_GP2_OUT_PAYLOAD_TRANSFER_LENGTH)—Offset Ch	0h
10h	13h	DBC_GP2_OUT_STATUS_BP_LOW (DBC_GP2_OUT_STATUS_BP_LOW)—Offset 10h	0h
14h	17h	DBC_GP2_OUT_STATUS_BP_HI (DBC_GP2_OUT_STATUS_BP_HI)—Offset 14h	0h
18h	1Bh	DBC_GP2_OUT_STATUS_QUALIFIERS (DBC_GP2_OUT_STATUS_QUALIFIERS)—Offset 18h	0h
1Ch	1Fh	DBC_GP2_IN_PAYLOAD_BP_LOW (DBC_GP2_IN_PAYLOAD_BP_LOW)—Offset 1Ch	0h
20h	23h	DBC_GP2_IN_PAYLOAD_BP_HI (DBC_GP2_IN_PAYLOAD_BP_HI)—Offset 20h	0h
24h	27h	DBC_GP2_IN_PAYLOAD_QUALIFIERS (DBC_GP2_IN_PAYLOAD_QUALIFIERS)—Offset 24h	0h
28h	2Bh	DBC_GP2_IN_PAYLOAD_TRANSFER_LENGTH (DBC_GP2_IN_PAYLOAD_TRANSFER_LENGTH)—Offset 28h	0h
2Ch	2Fh	DBC_GP2_IN_STATUS_BP_LOW (DBC_GP2_IN_STATUS_BP_LOW)—Offset 2Ch	0h
30h	33h	DBC_GP2_IN_STATUS_BP_HI (DBC_GP2_IN_STATUS_BP_HI)—Offset 30h	0h
34h	37h	DBC_GP2_IN_STATUS_QUALIFIERS (DBC_GP2_IN_STATUS_QUALIFIERS)—Offset 34h	0h
38h	3Bh	DBC_DFX_OUT_CONTROL (DBC_DFX_OUT_CONTROL)—Offset 38h	0h
3Ch	3Fh	DBC_DFX_IN_PAYLOAD_BP_LOW (DBC_DFX_IN_PAYLOAD_BP_LOW)—Offset 3Ch	0h
40h	43h	DBC_DFX_IN_PAYLOAD_BP_HI (DBC_DFX_IN_PAYLOAD_BP_HI)—Offset 40h	0h
44h	47h	DBC_DFX_IN_PAYLOAD_TRANSFER_LENGTH (DBC_DFX_IN_PAYLOAD_TRANSFER_LENGTH)—Offset 44h	0h
48h	4Bh	DBC_DFX_IN_STATUS_BP_LOW (DBC_DFX_IN_STATUS_BP_LOW)—Offset 48h	0h

Table 19-3. Summary of 0_20_0_usbx_exi_on_dbc_registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4Ch	4Fh	DBC_DFX_IN_STATUS_BP_HI (DBC_DFX_IN_STATUS_BP_HI)—Offset 4Ch	0h
50h	53h	DBC_TRACE_IN_PAYLOAD_BP_LOW (DBC_TRACE_IN_PAYLOAD_BP_LOW)—Offset 50h	0h
54h	57h	DBC_TRACE_IN_PAYLOAD_BP_HI (DBC_TRACE_IN_PAYLOAD_BP_HI)—Offset 54h	0h
58h	5Bh	DBC_TRACE_IN_PAYLOAD_QUALIFIERS (DBC_TRACE_IN_PAYLOAD_QUALIFIERS)—Offset 58h	0h
5Ch	5Fh	DBC_TRACE_IN_PAYLOAD_TRASNFER_DOORBELL (DBC_TRACE_IN_PAYLOAD_TRANSFER_DOORBELL)—Offset 5Ch	0h
60h	63h	DBC_TRACE_IN_STATUS_BP_LOW (DBC_TRACE_IN_STATUS_BP_LOW)—Offset 60h	0h
64h	67h	DBC_TRACE_IN_STATUS_BP_HI (DBC_TRACE_IN_STATUS_BP_HI)—Offset 64h	0h
68h	6Bh	DBC_TRACE_IN_STATUS_QUALIFIERS (DBC_TRACE_IN_STATUS_QUALIFIERS)—Offset 68h	0h
6Ch	6Fh	DBC_ERROR_CONTROL_STATUS_REG (DBC_ERROR_CONTROL_STATUS_REG)—Offset 6Ch	0h
70h	73h	DBC_EXI_CONTROL_STATUS_REG (DBC_EXI_CONTROL_STATUS_REG)—Offset 70h	0h
74h	77h	FABRIC_AGENT_UPSTREAM_GRANT_COUNT_REG (FABRIC_AGENT_UPSTREAM_GRANT_COUNT_REG)—Offset 74h	9249249h
78h	7Bh	DBC_ECO_POLICY_REG1 (DBC_ECO_POLICY_REG1)—Offset 78h	40F00h
7Ch	7Fh	DBC_ECO_POLICY_REG2 (DBC_ECO_POLICY_REG2)—Offset 7Ch	0h
80h	83h	DBC_ECO_POLICY_REG3 (DBC_ECO_POLICY_REG3)—Offset 80h	0h
84h	87h	DBC_ECO_POLICY_REG4 (DBC_ECO_POLICY_REG4)—Offset 84h	0h
88h	8Bh	DBConEXI Capability Port Status and Control Register (DBC_EXI_DCPORTSC)—Offset 88h	80h
100h	103h	DEBUG_SW_CONTROL_STATUS_REG (DEBUG_SW_CONTROL_STATUS_REG)—Offset 100h	0h
104h	107h	DEBUG_REQUEST_INFO_AND_STATUS_REG (DEBUG_REQUEST_INFO_AND_STATUS_REG)—Offset 104h	0h
108h	10Bh	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_0)—Offset 108h	0h
10Ch	10Fh	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_1)—Offset 10Ch	0h
110h	113h	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_2)—Offset 110h	0h
114h	117h	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_3)—Offset 114h	0h
118h	11Bh	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_4)—Offset 118h	0h
11Ch	11Fh	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_5)—Offset 11Ch	0h
120h	123h	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_6)—Offset 120h	0h
124h	127h	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_7)—Offset 124h	0h
128h	12Bh	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_8)—Offset 128h	0h

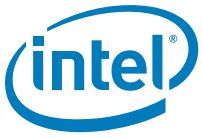


Table 19-3. Summary of 0_20_0_usbx_exi_on_dbc_registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
12Ch	12Fh	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_9)—Offset 12Ch	0h
130h	133h	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_10)—Offset 130h	0h
134h	137h	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_11)—Offset 134h	0h
138h	13Bh	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_12)—Offset 138h	0h
13Ch	13Fh	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_13)—Offset 13Ch	0h
140h	143h	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_14)—Offset 140h	0h
144h	147h	DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_15)—Offset 144h	0h
148h	14Bh	DEBUG_RESPONSE_INFO_AND_STATUS_REG (DEBUG_RESPONSE_INFO_AND_STATUS_REG)—Offset 148h	0h
180h	183h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_0)—Offset 180h	0h
184h	187h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_1)—Offset 184h	0h
188h	18Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_2)—Offset 188h	0h
18Ch	18Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_3)—Offset 18Ch	0h
190h	193h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_4)—Offset 190h	0h
194h	197h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_5)—Offset 194h	0h
198h	19Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_6)—Offset 198h	0h
19Ch	19Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_7)—Offset 19Ch	0h
1A0h	1A3h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_8)—Offset 1A0h	0h
1A4h	1A7h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_9)—Offset 1A4h	0h
1A8h	1ABh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_10)—Offset 1A8h	0h
1ACh	1AFh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_11)—Offset 1ACh	0h
1B0h	1B3h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_12)—Offset 1B0h	0h
1B4h	1B7h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_13)—Offset 1B4h	0h
1B8h	1BBh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_14)—Offset 1B8h	0h
1BCh	1BFh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_15)—Offset 1BCh	0h
1C0h	1C3h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_16)—Offset 1C0h	0h

Table 19-3. Summary of 0_20_0_usbx_exi_on_dbc_registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1C4h	1C7h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_17)—Offset 1C4h	0h
1C8h	1CBh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_18)—Offset 1C8h	0h
1CCh	1CFh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_19)—Offset 1CCh	0h
1D0h	1D3h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_20)—Offset 1D0h	0h
1D4h	1D7h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_21)—Offset 1D4h	0h
1D8h	1DBh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_22)—Offset 1D8h	0h
1DCh	1DFh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_23)—Offset 1DCh	0h
1E0h	1E3h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_24)—Offset 1E0h	0h
1E4h	1E7h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_25)—Offset 1E4h	0h
1E8h	1EBh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_26)—Offset 1E8h	0h
1ECh	1EFh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_27)—Offset 1ECh	0h
1F0h	1F3h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_28)—Offset 1F0h	0h
1F4h	1F7h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_29)—Offset 1F4h	0h
1F8h	1FBh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_30)—Offset 1F8h	0h
1FCh	1FFh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_31)—Offset 1FCh	0h
200h	203h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_32)—Offset 200h	0h
204h	207h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_33)—Offset 204h	0h
208h	20Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_34)—Offset 208h	0h
20Ch	20Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_35)—Offset 20Ch	0h
210h	213h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_36)—Offset 210h	0h
214h	217h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_37)—Offset 214h	0h
218h	21Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_38)—Offset 218h	0h
21Ch	21Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_39)—Offset 21Ch	0h
220h	223h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_40)—Offset 220h	0h
224h	227h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_41)—Offset 224h	0h

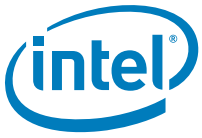


Table 19-3. Summary of 0_20_0_usbx_exi_on_dbc_registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
228h	22Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_42)—Offset 228h	0h
22Ch	22Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_43)—Offset 22Ch	0h
230h	233h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_44)—Offset 230h	0h
234h	237h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_45)—Offset 234h	0h
238h	23Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_46)—Offset 238h	0h
23Ch	23Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_47)—Offset 23Ch	0h
240h	243h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_48)—Offset 240h	0h
244h	247h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_49)—Offset 244h	0h
248h	24Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_50)—Offset 248h	0h
24Ch	24Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_51)—Offset 24Ch	0h
250h	253h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_52)—Offset 250h	0h
254h	257h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_53)—Offset 254h	0h
258h	25Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_54)—Offset 258h	0h
25Ch	25Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_55)—Offset 25Ch	0h
260h	263h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_56)—Offset 260h	0h
264h	267h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_57)—Offset 264h	0h
268h	26Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_58)—Offset 268h	0h
26Ch	26Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_59)—Offset 26Ch	0h
270h	273h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_60)—Offset 270h	0h
274h	277h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_61)—Offset 274h	0h
278h	27Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_62)—Offset 278h	0h
27Ch	27Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_63)—Offset 27Ch	0h
280h	283h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_64)—Offset 280h	0h
284h	287h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_65)—Offset 284h	0h
288h	28Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_66)—Offset 288h	0h

Table 19-3. Summary of 0_20_0_usbx_exi_on_dbc_registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
28Ch	28Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_67)—Offset 28Ch	0h
290h	293h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_68)—Offset 290h	0h
294h	297h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_69)—Offset 294h	0h
298h	29Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_70)—Offset 298h	0h
29Ch	29Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_71)—Offset 29Ch	0h
2A0h	2A3h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_72)—Offset 2A0h	0h
2A4h	2A7h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_73)—Offset 2A4h	0h
2A8h	2ABh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_74)—Offset 2A8h	0h
2ACh	2AFh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_75)—Offset 2ACh	0h
2B0h	2B3h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_76)—Offset 2B0h	0h
2B4h	2B7h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_77)—Offset 2B4h	0h
2B8h	2BBh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_78)—Offset 2B8h	0h
2BCh	2BFh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_79)—Offset 2BCh	0h
2C0h	2C3h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_80)—Offset 2C0h	0h
2C4h	2C7h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_81)—Offset 2C4h	0h
2C8h	2CBh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_82)—Offset 2C8h	0h
2CCh	2CFh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_83)—Offset 2CCh	0h
2D0h	2D3h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_84)—Offset 2D0h	0h
2D4h	2D7h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_85)—Offset 2D4h	0h
2D8h	2DBh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_86)—Offset 2D8h	0h
2DCh	2DFh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_87)—Offset 2DCh	0h
2E0h	2E3h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_88)—Offset 2E0h	0h
2E4h	2E7h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_89)—Offset 2E4h	0h
2E8h	2EBh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_90)—Offset 2E8h	0h
2ECh	2EFh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_91)—Offset 2ECh	0h

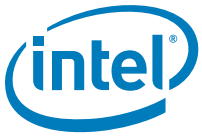


Table 19-3. Summary of 0_20_0_usbx_exi_on_dbc_registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
2F0h	2F3h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_92)—Offset 2F0h	0h
2F4h	2F7h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_93)—Offset 2F4h	0h
2F8h	2FBh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_94)—Offset 2F8h	0h
2FCh	2FFh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_95)—Offset 2FCh	0h
300h	303h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_96)—Offset 300h	0h
304h	307h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_97)—Offset 304h	0h
308h	30Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_98)—Offset 308h	0h
30Ch	30Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_99)—Offset 30Ch	0h
310h	313h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_100)—Offset 310h	0h
314h	317h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_101)—Offset 314h	0h
318h	31Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_102)—Offset 318h	0h
31Ch	31Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_103)—Offset 31Ch	0h
320h	323h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_104)—Offset 320h	0h
324h	327h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_105)—Offset 324h	0h
328h	32Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_106)—Offset 328h	0h
32Ch	32Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_107)—Offset 32Ch	0h
330h	333h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_108)—Offset 330h	0h
334h	337h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_109)—Offset 334h	0h
338h	33Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_110)—Offset 338h	0h
33Ch	33Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_111)—Offset 33Ch	0h
340h	343h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_112)—Offset 340h	0h
344h	347h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_113)—Offset 344h	0h
348h	34Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_114)—Offset 348h	0h
34Ch	34Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_115)—Offset 34Ch	0h
350h	353h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_116)—Offset 350h	0h

Table 19-3. Summary of 0_20_0_usbx_exi_on_dbc_registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
354h	357h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_117)—Offset 354h	0h
358h	35Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_118)—Offset 358h	0h
35Ch	35Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_119)—Offset 35Ch	0h
360h	363h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_120)—Offset 360h	0h
364h	367h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_121)—Offset 364h	0h
368h	36Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_122)—Offset 368h	0h
36Ch	36Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_123)—Offset 36Ch	0h
370h	373h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_124)—Offset 370h	0h
374h	377h	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_125)—Offset 374h	0h
378h	37Bh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_126)—Offset 378h	0h
37Ch	37Fh	DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_127)—Offset 37Ch	0h
380h	383h	DEBUG_RESPONSE_HEADER_STACK_REG (DEBUG_RESPONSE_HEADER_STACK_REG_0)—Offset 380h	0h
384h	387h	DEBUG_RESPONSE_HEADER_STACK_REG (DEBUG_RESPONSE_HEADER_STACK_REG_1)—Offset 384h	0h
388h	38Bh	DEBUG_RESPONSE_HEADER_STACK_REG (DEBUG_RESPONSE_HEADER_STACK_REG_2)—Offset 388h	0h

19.3.1 DBC_GP2_OUT_PAYLOAD_BP_LOW (DBC_GP2_OUT_PAYLOAD_BP_LOW)—Offset 0h

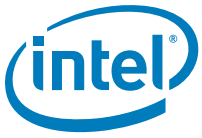
Lower DW of Payload Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_GP2_OUT_PAYLOAD_BP_LOW (DBC_GP2_OUT_PAYLOAD_BP_LOW):** Lower DW of Payload Address Pointer



19.3.2 DBC_GP2_OUT_PAYLOAD_BP_HI (DBC_GP2_OUT_PAYLOAD_BP_HI)—Offset 4h

Upper DW of Payload Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_GP2_OUT_PAYLOAD_BP_HI (DBC_GP2_OUT_PAYLOAD_BP_HI):** Upper DW of Payload Address Pointer

19.3.3 DBC_GP2_OUT_PAYLOAD_QUALIFIERS (DBC_GP2_OUT_PAYLOAD_QUALIFIERS)—Offset 8h

DbC GP2 OUT Payload Qualifiers

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD)**
21:8	0h RW	**DESTN_ID (DESTN_ID):** Decode_Mode[1:0] PSF[3:0] Port_Group[0:0] Port[3:0] Channel[2:0]
7:4	0h RO	**RESERVED1 (RSVD1)**
3:0	0h RW	**ROOT_SPACE (ROOT_SPACE)**

19.3.4 DBC_GP2_OUT_PAYLOAD_TRANSFER_LENGTH (DBC_GP2_OUT_PAYLOAD_TRANSFER_LENGTH)—Offset Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**DATA_VALID (DATA_VALID):** This bit indicates the presence of a valid data buffer and is the doorbell that allows the DbC to initiate a DMA transaction. This bit is cleared by HW upon completion of the DMA upto either the specific transfer length, or thehost controller sending a short packet
30:0	0h RW	**PAYLOAD_TRANSFER_LENGTH (PAYLOAD_TRANSFER_LENGTH):** Length of payload buffer in Bytes (1 based count)

19.3.5 DBC_GP2_OUT_STATUS_BP_LOW (DBC_GP2_OUT_STATUS_BP_LOW)—Offset 10h

Lower DW of STATUS Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_GP2_OUT_STATUS_BP_LOW (DBC_GP2_OUT_STATUS_BP_LOW):** Lower DW of STATUS Address Pointer

19.3.6 DBC_GP2_OUT_STATUS_BP_HI (DBC_GP2_OUT_STATUS_BP_HI)—Offset 14h

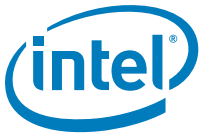
Upper DW of STATUS Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_GP2_OUT_STATUS_BP_HI (DBC_GP2_OUT_STATUS_BP_HI):** Upper DW of STATUS Address Pointer



19.3.7 DBC_GP2_OUT_STATUS_QUALIFIERS (DBC_GP2_OUT_STATUS_QUALIFIERS)—Offset 18h

DbC GP2 OUT STATUS Qualifiers

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD)**
21:8	0h RW	**DESTN_ID (DESTN_ID):** Decode_Mode[1:0] PSF[3:0] Port_Group[0:0] Port[3:0] Channel[2:0]
7:4	0h RO	**RESERVED1 (RSVD1)**
3:0	0h RW	**ROOT_SPACE (ROOT_SPACE)**

19.3.8 DBC_GP2_IN_PAYLOAD_BP_LOW (DBC_GP2_IN_PAYLOAD_BP_LOW)—Offset 1Ch

Lower DW of Payload Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_GP2_IN_PAYLOAD_BP_LOW (DBC_GP2_IN_PAYLOAD_BP_LOW):** Lower DW of Payload Address Pointer

19.3.9 DBC_GP2_IN_PAYLOAD_BP_HI (DBC_GP2_IN_PAYLOAD_BP_HI)—Offset 20h

Upper DW of Payload Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_GP2_IN_PAYLOAD_BP_HI (DBC_GP2_IN_PAYLOAD_BP_HI):** Upper DW of Payload Address Pointer

19.3.10 DBC_GP2_IN_PAYLOAD_QUALIFIERS (DBC_GP2_IN_PAYLOAD_QUALIFIERS)—Offset 24h

DbC GP2 OUT Payload Qualifiers

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD)**
21:8	0h RW	**DESTN_ID (DESTN_ID):** Decode_Mode[1:0] PSF[3:0] Port_Group[0:0] Port[3:0] Channel[2:0]
7:4	0h RO	**RESERVED1 (RSVD1)**
3:0	0h RW	**ROOT_SPACE (ROOT_SPACE)**

19.3.11 DBC_GP2_IN_PAYLOAD_TRANSFER_LENGTH (DBC_GP2_IN_PAYLOAD_TRANSFER_LENGTH)—Offset 28h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**DATA_VALID (DATA_VALID):** This bit indicates the presence of a valid data buffer and is the doorbell that allows the DbC to initiate a DMA transaction. This bit is cleared by HW upon completion of the DMA upto either the specific transfer length, or thehost controller sending a short packet

Bit Range	Default & Access	Field Name (ID): Description
30:0	0h RW	**PAYLOAD_TRANSFER_LENGTH (PAYLOAD_TRANSFER_LENGTH):** Length of payload buffer in Bytes (1 based count)

19.3.12 DBC_GP2_IN_STATUS_BP_LOW (DBC_GP2_IN_STATUS_BP_LOW)—Offset 2Ch

Lower DW of STATUS Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_GP2_IN_STATUS_BP_LOW (DBC_GP2_IN_STATUS_BP_LOW):** Lower DW of STATUS Address Pointer

19.3.13 DBC_GP2_IN_STATUS_BP_HI (DBC_GP2_IN_STATUS_BP_HI)—Offset 30h

Upper DW of STATUS Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_GP2_IN_STATUS_BP_HI (DBC_GP2_IN_STATUS_BP_HI):** Upper DW of STATUS Address Pointer

19.3.14 DBC_GP2_IN_STATUS_QUALIFIERS (DBC_GP2_IN_STATUS_QUALIFIERS)—Offset 34h

DbC GP2 OUT STATUS Qualifiers

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD)**
21:8	0h RW	**DESTN_ID (DESTN_ID):** Decode_Mode[1:0] PSF[3:0] Port_Group[0:0] Port[3:0] Channel[2:0]
7:4	0h RO	**RESERVED1 (RSVD1)**
3:0	0h RW	**ROOT_SPACE (ROOT_SPACE)**

19.3.15 DBC_DFX_OUT_CONTROL (DBC_DFX_OUT_CONTROL)—Offset 38h

DBC_DFX_OUT_CONTROL

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**RESERVED (RSVD)**
8	0h RW	**Credit De-allocate Update (CREDIT_DE_ALLOC_UPDATE):** This is sent by ExI Bridge to DbC whenever a packet is dispatched from the Inbound Buffer or in response to credit Init request. 1: 1 credit dispatched due to deallocation 0: Absolute value of credits in response to a Credit Init request from DbC
7:5	0h RO	**RESERVED (RSVD1)**
4:0	0h RW	**AVAILABLE_CREDITS (AVAILABLE_CREDITS):** ExI Bridge writes the absolute value of the available credit count into this register each time it drains an entry from its buffer. Each credit represents a 64 Byte ExI Packet. Also, coming out of reset, DbC will request for a Credit Init, and ExI Bridge will write the absolute value of available credit to this register.

19.3.16 DBC_DFX_IN_PAYLOAD_BP_LOW (DBC_DFX_IN_PAYLOAD_BP_LOW)—Offset 3Ch

Lower DW of Payload Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_DFX_IN_PAYLOAD_BP_LOW (DBC_DFX_IN_PAYLOAD_BP_LOW):** Lower DW of Payload Address Pointer

19.3.17 DBC_DFX_IN_PAYLOAD_BP_HI (DBC_DFX_IN_PAYLOAD_BP_HI)—Offset 40h

Upper DW of Payload Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_DFX_IN_PAYLOAD_BP_HI (DBC_DFX_IN_PAYLOAD_BP_HI):** Upper DW of Payload Address Pointer

19.3.18 DBC_DFX_IN_PAYLOAD_TRANSFER_LENGTH (DBC_DFX_IN_PAYLOAD_TRANSFER_LENGTH)—Offset 44h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**DATA_VALID (DATA_VALID):** This bit indicates the presence of a valid data buffer and is the doorbell that allows the DbC to initiate a DMA transaction. This bit is cleared by HW upon completion of the DMA upto either the specific transfer length, or thehost controller sending a short packet
30:0	0h RW	**PAYLOAD_TRANSFER_LENGTH (PAYLOAD_TRANSFER_LENGTH):** Length of payload buffer in Bytes (1 based count)

19.3.19 DBC_DFX_IN_STATUS_BP_LOW (DBC_DFX_IN_STATUS_BP_LOW)—Offset 48h

Lower DW of STATUS Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_DFX_IN_STATUS_BP_LOW (DBC_DFX_IN_STATUS_BP_LOW):** Lower DW of STATUS Address Pointer

19.3.20 DBC_DFX_IN_STATUS_BP_HI (DBC_DFX_IN_STATUS_BP_HI)—Offset 4Ch

Upper DW of STATUS Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_DFX_IN_STATUS_BP_HI (DBC_DFX_IN_STATUS_BP_HI):** Upper DW of STATUS Address Pointer

19.3.21 DBC_TRACE_IN_PAYLOAD_BP_LOW (DBC_TRACE_IN_PAYLOAD_BP_LOW)—Offset 50h

Lower DW of Payload Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_TRACE_IN_PAYLOAD_BP_LOW (DBC_TRACE_IN_PAYLOAD_BP_LOW):** Lower DW of Payload Address Pointer

19.3.22 DBC_TRACE_IN_PAYLOAD_BP_HI (DBC_TRACE_IN_PAYLOAD_BP_HI)—Offset 54h

Upper DW of Payload Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_TRACE_IN_PAYLOAD_BP_HI (DBC_TRACE_IN_PAYLOAD_BP_HI):** Upper DW of Payload Address Pointer

19.3.23 DBC_TRACE_IN_PAYLOAD_QUALIFIERS (DBC_TRACE_IN_PAYLOAD_QUALIFIERS)—Offset 58h

DbC TRACE OUT Payload Qualifiers

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD)**
21:8	0h RW	**DESTN_ID (DESTN_ID):** Decode_Mode[1:0] PSF[3:0] Port_Group[0:0] Port[3:0] Channel[2:0]
7:4	0h RO	**RESERVED1 (RSVD1)**
3:0	0h RW	**ROOT_SPACE (ROOT_SPACE)**

19.3.24 DBC_TRACE_IN_PAYLOAD_TRASNFER_DOORBELL (DBC_TRACE_IN_PAYLOAD_TRANSFER_DOORBELL)—Offset 5Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**RSVD (RSVD)**
18:11	0h RW	**PAYLOAD_OFFSET (PAYLOAD_OFFSET):** The Offset in multiples of 1024B from the base pointer from which to transfer the payload referenced by this doorbell.
10:0	0h RW	**PAYLOAD_TRASNFER_LENGTH (PAYLOAD_TRASNFER_LENGTH):** Length of payload buffer in Bytes (1 based count)

19.3.25 DBC_TRACE_IN_STATUS_BP_LOW (DBC_TRACE_IN_STATUS_BP_LOW)—Offset 60h

Lower DW of STATUS Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_TRACE_IN_STATUS_BP_LOW (DBC_TRACE_IN_STATUS_BP_LOW):** Lower DW of STATUS Address Pointer

19.3.26 DBC_TRACE_IN_STATUS_BP_HI (DBC_TRACE_IN_STATUS_BP_HI)—Offset 64h

Upper DW of STATUS Address Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_TRACE_IN_STATUS_BP_HI (DBC_TRACE_IN_STATUS_BP_HI):** Upper DW of STATUS Address Pointer

19.3.27 DBC_TRACE_IN_STATUS_QUALIFIERS (DBC_TRACE_IN_STATUS_QUALIFIERS)—Offset 68h

DbC TRACE OUT STATUS Qualifiers

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved (RSVD)**
21:8	0h RW	**DESTN_ID (DESTN_ID):** Decode_Mode[1:0] PSF[3:0] Port_Group[0:0] Port[3:0] Channel[2:0]
7:4	0h RO	**RESERVED1 (RSVD1)**
3:0	0h RW	**ROOT_SPACE (ROOT_SPACE)**

19.3.28 DBC_ERROR_CONTROL_STATUS_REG (DBC_ERROR_CONTROL_STATUS_REG)—Offset 6Ch

DBC_ERROR_CONTROL_STATUS_REG

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved (RSVD)**
8	0h RW	**DBC_TRACE_IN (DBC_TRACE_IN)**
7	0h RW	**DBC_DFX_OUT (DBC_DFX_OUT)**

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**DBC_DFX_IN (DBC_DFX_IN)**
5	0h RW	**DBC_GP2_OUT (DBC_GP2_OUT)**
4	0h RW	**DBC_GP2_IN (DBC_GP2_IN)**
3	0h RW	**DBC_GP1_OUT (DBC_GP1_OUT)**
2	0h RW	**DBC_GP1_IN (DBC_GP1_IN)**
1	0h RW	**CONTROL_EP (CONTROL_EP)**
0	0h RW	**STATUS_WRITE_ON_ERROR_EN (STATUS_WRITE_ON_ERROR_EN):** Enable status write generation on detecting error on Trace/DFx/GP2 EPs

19.3.29 DBC_EXI_CONTROL_STATUS_REG (DBC_EXI_CONTROL_STATUS_REG)—Offset 70h

DBC_EXI_CONTROL_STATUS_REG

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**DBC_GP2_IN_STATUS_LOG (DBC_GP2_IN_STATUS_LOG):** Set when the DMA transfer request status for GP2 IN is completed. Cleared when a new DMA transfer request is received.
30	0h RO	**DBC_GP2_OUT_STATUS_LOG (DBC_GP2_OUT_STATUS_LOG):** Set when the DMA transfer request status for GP2 OUT is completed. Cleared when a new DMA transfer request is received.
29:13	0h RO	**RSVD (RSVD)**
12	0h RW	**DBC_EXI_CLK_GATING_CTRL (DBC_EXI_CLK_GATING_CTRL):** Disable gating for prim_clk for DbC-ExI logic. By default clock gating is enabled.
11	0h RW	**DBC_SAI_CHECK_POLICY (DBC_SAI_CHECK_POLICY):** 1: Disable SAI checking on read requests only 0: Enable Default SAI check (on Reads & Writes)

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**TRACE_SEQUENCER_PIPELINE_DISABLE (TRACE_SEQUENCER_PIPELINE_DISABLE):** Set to disable pipelining of read requests to fabric for different trace transfer requests. By default, trace sequencer would start issuing reads requests to Fabric for a subsequent transfer request while the reads for the previous one hasnt been returned back to DbC 0: Read Pipelining enabled for Trace 1: Disable read pipelining for Trace
9:7	0h RW	**DBC_MAX_PKT_SIZE (DBC_MAX_PKT_SIZE):** Configurable MPS for Trace, DFx, GP2 EPs Default = 1KB 000 : 1KB 001 : 64B 010 : 128B 011 : 256B 100 : 512B Others : Reserved
6:1	0h RW	**DBC_NUM_PENDING_READS (DBC_NUM_PENDING_READS):** Constrain number of read requests pending on Fabric on behalf of DbC Eps. Sequencers limit the number of read requests that will be initiated on Fabric at any given time to NUM_PENDING_READ. NUM_PENDING_READ = [1..READS_PER_MPS] Where READS_PER_MPS is the number of read requests require for 1 MPS for the given EP. Applies for DbC.[Trace|DFx|GP2] IN EPs
0	0h RW	**DBC_TRACE_PIPELINE_DEPTH1 (DBC_TRACE_PIPELINE_DEPTH1):** Constrain DbC.Trace IN Pipeline to 1 deep. Limit processing of DbC Trace to one transfer at any time. In other words, Until Trace data for the first transfer request from NPKH is completed on USB3 interface and status returned back to NPKH, subsequent transfer request is not started, only 1 Trace sequencer is active at any given time.

19.3.30 FABRIC_AGENT_UPSTREAM_GRANT_COUNT_REG (FABRIC_AGENT_UPSTREAM_GRANT_COUNT_REG)—Offset 74h

FABRIC_AGENT_UPSTREAM_GRANT_COUNT_REG

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 9249249h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:27	1h RW	**IN_PORT_ARB_GRANT_COUNT (IN_PORT_ARB_GRANT_COUNT)**
26:24	1h RW	**GP2_IN_PORT_ARB_GRANT_COUNT (GP2_IN_PORT_ARB_GRANT_COUNT)**

Bit Range	Default & Access	Field Name (ID): Description
23:21	1h RW	**DFX_IN_PORT_ARB_GRANT_COUNT (DFX_IN_PORT_ARB_GRANT_COUNT)**
20:18	1h RW	**TRACE_IN_PORT_ARB_GRANT_COUNT (TRACE_IN_PORT_ARB_GRANT_COUNT)**
17:15	1h RW	**RD_REQ_HYSTERESIS_COUNT (RD_REQ_HYSTERESIS_COUNT)**
14:12	1h RW	**DBC_GRANT_COUNT (DBC_GRANT_COUNT)**
11:9	1h RW	**EXI_GRANT_COUNT (EXI_GRANT_COUNT)**
8:6	1h RW	**GP2_GRANT_COUNT (GP2_GRANT_COUNT)**
5:3	1h RW	**DFX_GRANT_COUNT (DFX_GRANT_COUNT)**
2:0	1h RW	**TRACE_GRANT_COUNT (TRACE_GRANT_COUNT)**

19.3.31 DBC_ECO_POLICY_REG1 (DBC_ECO_POLICY_REG1)—Offset 78h

ECO Policy registers for future use

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40F00h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**RESERVED (RSVD)**
23	0h RW	**GP2_IN_BACK2BACK_SHORT_PKT_FIX_EN (GP2_IN_BACK2BACK_SHORT_PKT_FIX_EN)**
22	0h RW	**DFX_IN_BACK2BACK_SHORT_PKT_FIX_EN (DFX_IN_BACK2BACK_SHORT_PKT_FIX_EN)**
21	0h RW	**TRACE_IN_BACK2BACK_SHORT_PKT_FIX_EN (TRACE_IN_BACK2BACK_SHORT_PKT_FIX_EN)**
20:18	1h RW	**OUT_PORT_ARB_GRANT_COUNT (OUT_PORT_ARB_GRANT_COUNT)**
17	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**OUT_EP_BURST_SIZE (OUT_EP_BURST_SIZE):** Default: HW selects the burst size for OUT EPs based on the mode of operation Kernel Debug Mode Only: Supported OUT EP = 1 (GP1) ; Burst Size = 4 Platform Debug Mode Only: Supported OUT EPs = 2 (DFx, GP2), Burst Size = 2 Kernel and Platform debug mode: Supported OUT EPs = 3 (GP1, DFx, GP2) ; Burst Size = 1 When Set to 1 ; Burst Size = 1
15	0h RW	**IGNORE_EXI_EN (IGNORE_EXI_EN)**
14	0h RW	**IGNORE_DCE (IGNORE_DCE)**
13	0h RW	**DBC_EXI_HCRESET_DISABLE (DBC_EXI_HCRESET_DISABLE):** When set to 1, DBC/DBC-EXI will not take any action on HCReset. Default behavior is to trigger HCReset flow.
12	0h RW	**DBC_ALLOW_PG (DBC_ALLOW_PG):** When set to 1, DBC/ DBC-EXI will allow PG under HW initiated low power modes (D0ix). This could be used in a flow where XHC is allowed to enter low power modes, while debug data will subsequently transported to debug host after re-entry into
11:8	Fh RW	**HC_RESET_WPR_HANDLING_TIMEOUT_VALUES (HC_RESET_WPR_HANDLING_TIMEOUT_VALUES):** 0000 : 0 us (trigger exit right away) 0001 : 250 us 0010 : 500 us 1111 : 3.75 ms
7	0h RW	**TIMEOUT_BASED_HC_RESET_WPR_HANDLING (TIMEOUT_BASED_HC_RESET_WPR_HANDLING):** When set, enable timer based mechanism to allow HCReset and Warm Port Reset to override any hung situation due to any flows not completing as expected. Use HC Reset/WPR Handling Timeout values for forcing HCReset/ WPR flows
6	0h RW	**RSVD1 (RSVD1):** Reserved
5	0h RW	**INTERNAL_DBC_EXI_ENABLE (INTERNAL_DBC_EXI_ENABLE):** Enable address decode of transactions using Source Decode transactions based on Source ID instead of the default MBAR based address based decode.
4	0h RW	**EXI_ENABLE_OVERRIDE_ENABLE (EXI_ENABLE_OVERRIDE_ENABLE):** When this bit is set, the Internal DBC ExI Enable takes priority over the external ExI Enable signal received from EXI Bridge IP Default behavior is to use exio_scr_ectrl_eavails input from ExI Bridge
3	0h RW	**TRACE_STATUS_ADDRESS (TRACE_STATUS_ADDRESS):** When this bit is set, the address for Status Write request will include the address offset. Default address for Trace Status is the base address of the trace request

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**ENABLE_NON_TRANSFER_STATUS (ENABLE_NON_TRANSFER_STATUS):** Enables generation of a status write on each of the interfaces with status indicating the cause of an exception flow trigger condition Default behavior is for the sequencer to return a status completion (for transfer success, or exception scenarios) only when a pending/active DMA is in progress
1	0h RW	**ENABLE_DBC_EXI_ON_CREDIT_INIT_COMPLETION (ENABLE_DBC_EXI_ON_CREDIT_INIT_COMPLETION):** Setting this bit will enforce Credit Init completion as necessary condition to allow transfers on all 3 interfaces (Trace, GP2, DFx). Default behavior requires successful Credit Init completion as necessary condition only to allow DFX OUT EP transfer and not affect other interfaces (Trace, GP2)
0	0h RW	**CREDIT_INIT_TRIGGER (CREDIT_INIT_TRIGGER):** Writing a 1 to this bit will trigger Credit Init request. A Credit Init request will be initiated irrespective of the status of the last Credit Init request initiated.

19.3.32 DBC_ECO_POLICY_REG2 (DBC_ECO_POLICY_REG2)—Offset 7Ch

ECO Policy registers for future use

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**RESERVED (RSVD)**
5	0h RO	**DBC_EXI_RUN (DBC_EXI_RUN):** Internal version of RUN. Set only when DBC_EXI is enabled and link up as upstream port was due to DBC_EXI =1
4	0h RO	**DBC_RUN (DBC_RUN):** Internal version of RUN bit. Set only when DBC(DD) is enabled and link up as upstream port was due to DCE=1
3	0h RO	**DBC_EXI_EN (DBC_EXI_EN):** DBC_EXI_EN Internal version of EXI_EN
2	0h RO	**DBC_EN (DBC_EN):** DBC_EN Internal version of DBC_EN tracked by HW

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	**CREDIT_INIT_STATUS (CREDIT_INIT_STATUS):** Tracks the status of Credit Init Handshake. HW updates this register. 00 : Credit Init not yet requested 01 : Credit Init Pending: request sent to ExI Bridge Not received Init Credit value from ExI Bridge 10 : Credit Init Done : Received Init Credit value from ExI Bridge 11 : Reserved

19.3.33 DBC_ECO_POLICY_REG3 (DBC_ECO_POLICY_REG3)—Offset 80h

ECO Policy registers for future use

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_ECO_POLICY_REG3 (DBC_ECO_POLICY_REG3)**

19.3.34 DBC_ECO_POLICY_REG4 (DBC_ECO_POLICY_REG4)—Offset 84h

ECO Policy registers for future use

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DBC_ECO_POLICY_REG4 (DBC_ECO_POLICY_REG4)**

19.3.35 DBConEXI Capability Port Status and Control Register (DBC_EXI_DCPORTSC)—Offset 88h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved (RSVD)**
23	0h RW/C	**Port Config Error Change (CEC):** This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it.
22	0h RW/C	**Port Link Status Change (PLC):** This flag is set to '1' due to the following PLS transitions: U0 -) U3 Suspend signaling detected from Debug Host U3 -) U0 Resume complete Polling -) Disabled Training Error Ux or Recovery -) Inactive Error Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'
21	0h RW/C	**Port Reset Change (PRC):** This bit is set when reset processing on this port is complete (i.e. a '1' to '0' transition of PR). '0' = No change. '1' = Reset complete.Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'.
20:18	0h RO	**Reserved (RSVD_1)**
17	0h RW/C	**Connect Status Change (CSC):** '1' = Change in Current Connect Status. '0' = No change. Indicates a change has occurred in the port's Current Connect Status. The xHC sets this bit to '1' for all changes to the Debug Device connect status, even if system software has not cleared an existing DbC Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, hardware will be "setting" an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'.
16:14	0h RO	**Reserved (RSVD_2)**
13:10	0h RO	**Port Speed (PSPD):** This field identifies the speed of the port. This field is only relevant when a Debug Host is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. 0 Undefined Speed 1-15 Protocol Speed ID (PSI) Note: The Debug Capability onlydoes not supports LS, FS, or HS operation.
9	0h RO	**Reserved (RSVD_3)**
8:5	4h RO	**Port Link State (PLS):** This field reflects its current link state. This field is only relevant when a Debug Host is attached (Debug Port Number) '0'). Value Meaning 0 Link is in the U0 State 1 Link is in the U1 State 2 Link is in the U2 State 3 Link is in the U3 State (Device Suspended) 4 Link is in the Disabled State 5 Link is in the RxDetect State 6 Link is in the Inactive State 7 Link is in the Polling State 8 Link is in the Recovery State 9 Link is in the Hot Reset State 15:10 Reserved Note: Transitions between different states are not reflected until the transition is complete.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Port Reset (PR):** '1' = Port is in Reset. '0' = Port is not in Reset. This bit is set to '1' when the bus reset sequence as defined in the USB Specification is detected on the Root Hub port assigned to the Debug capability. It is cleared when the bus reset sequence is completed by the Debug Host, and the DbC shall transition to the USB Default state. A '0' to '1' transition of this bit shall clear DBC_EXI_DCPORTSC PED ('0'). This field is '0' if DCE or CCS are '0'.
3:2	0h RO	**Reserved (RSVD_4)**
1	0h RW	**Port Enabled/Disabled (PED):** Default = '0'. '1' = Enabled. '0' = Disabled. This flag shall be set to '1' by a '0' to '1' transition of CCS or a '1' to '0' transition of the PR. When PED transitions from '1' to '0' due to the assertion of PR, the port's link shall transition to the Rx.Detect state. This flag may be used by software to enable or disable the operation of the Root Hub port assigned to the Debug Capability. The Debug Capability Root Hub port operation may be disabled by a fault condition (disconnect event or other fault condition, e.g. a LTSSM Polling substate timeout, tPortConfiguration timeout error, etc.), the assertion of DBC_EXI_DCPORTSC PR, or by software. 0 = Debug Capability Root Hub port is disabled. 1 = Debug Capability Root Hub port is enabled. When the port is disabled (PED = '0') the port's link shall enter the SS.Disabled state and remain there until PED is reasserted ('1') or DCE is negated ('0'). Note that the Root Hub port is remains mapped to Debug Capability while PED = '0'. While PED = '0' the Debug Capability will appear to be disconnected to the Debug Host. Note, this bit is not affected by PORTSC PR bit transitions. This field is '0' if DCE or CCS are '0'.
0	0h RO	**Current Connect Status (CCS):** '1' = A Root Hub port is connected to a Debug Host and assigned to the Debug Capability. '0' = No Debug Host is present. This value reflects the current state of the port, and may not correspond to the value reported by the Connect Status Change (CSC) field in the Port Status Change Event that was generated by a '0' to '1' transition of this bit. This flag is '0' if Debug Capability Enable (DCE) is '0'.

19.3.36 DEBUG_SW_CONTROL_STATUS_REG (DEBUG_SW_CONTROL_STATUS_REG)—Offset 100h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**RSVD (RSVD)**
7	0h RW	**FAST_SW_TIMEOUT_MODE (FAST_SW_TIMEOUT_MODE):** 1 : Enable Fast Timeout Simulation Mode. When set, timeout values used for SW response Timeout mode will be in micro-seconds. 0 : Normal mode. Timeout values are as defined by SW response Timeout register.
6	0h RW/1C	**SW_TIMEOUT_STATUS (SW_TIMEOUT_STATUS):** 1: Set by HW when Timeout occurred and HW disabled SW Handling 0: Timeout not triggered Set by HW, Cleared by SW. Timeout will also clear Debug SW Available bit.
5:2	0h RW	**SW_RESPONSE_TIMEOUT (SW_RESPONSE_TIMEOUT):** 0000 : 1 ms 0001: 20 ms 0010: 40 ms 0011: 60 ms 0100: 80 ms 0101: 100 ms 0110: 200ms 1111: 1100ms
1	0h RW	**SW_RESPONSE_TIMEOUT_ENABLE (SW_RESPONSE_TIMEOUT_ENABLE):** 1: HW will timeout and trigger STALL response if SW did not respond within SW Timeout period 0: Timeout is not triggered.
0	0h RW	**DEBUG_SW_AVAILABLE (DEBUG_SW_AVAILABLE):** 1: Debug SW has been loaded and is available 0: Debug SW is not available When Debug SW is available, then HW presents the Control Transfer requests to SW and relies on SW to handle the requests.

19.3.37 DEBUG_REQUEST_INFO_AND_STATUS_REG (DEBUG_REQUEST_INFO_AND_STATUS_REG)—Offset 104h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RESPONSE_PACKET_LAST (RESPONSE_PACKET_LAST):** Specifies that this response packet is the last packet for satisfying the current request or if there is additional packets to complete the request. 1 : Current response packet is the last data packet for the current request 0: Current response packet is not the last data packet for the current request. There is one or more additional data packets required to complete the request. For example, If the response data buffer is 512B, and the response is > 512B, then there will be multiple response data packets required, and this bit is set to 0 except for the last one.

Bit Range	Default & Access	Field Name (ID): Description
30:27	0h RW	**RESPONSE_TYPE (RESPONSE_TYPE):** Specifies the type of response that needs to be generated 000 : DATA Response 001: ACK 010: STALL (Request not supported) Others: Reserved For DATA response, associate DATA is written into the Response Stack by SW.
26	0h RW/1S	**DEBUG_RESPONSE_AVAIL (DEBUG_RESPONSE_AVAIL):** 1: Valid SW response available for HW 0: No response available SW sets this bit when it has generated a response for a debug request received. HW clears this bit after the response has been consumed (completed the transfer to host).
25:15	0h RO	**RSVD (RSVD)**
14:12	0h RW	**DEBUG_REQUEST_ERROR_TYPE (DEBUG_REQUEST_ERROR_TYPE):** Indicates that cause/Type of the error detect. Valid only when Debug Request Error Detected bit is 1
11	0h RW	**DEBUG_REQUEST_ERROR_DETECTED (DEBUG_REQUEST_ERROR_DETECTED):** HW sets this bit to indicate to Debug SW that an error was detected on the packet received on the USB3 link
10:1	0h RO	**DEBUG_REQUEST_LENGTH (DEBUG_REQUEST_LENGTH):** Length of any data associated with the current request. This field is valid only when a debug request is pending.
0	0h RW/1C	**DEBUG_REQUEST_PENDING (DEBUG_REQUEST_PENDING):** 1: Debug request is available for SW to consume 0: No request is pending for SW HW sets this bit to indicate to Debug SW that a control transfer request is pending for SW to handle. SW clears this bit once it has consumed the request.

19.3.38 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_0)—Offset 108h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.39 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_1)—Offset 10Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.40 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_2)—Offset 110h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.41 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_3)—Offset 114h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.42 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_4)—Offset 118h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.43 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_5)—Offset 11Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.44 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_6)—Offset 120h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.45 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_7)—Offset 124h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.46 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_8)—Offset 128h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.47 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_9)—Offset 12Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.48 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_10)—Offset 130h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.49 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_11)—Offset 134h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.50 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_12)—Offset 138h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.51 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_13)—Offset 13Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.52 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_14)—Offset 140h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.53 DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_REG_15)—Offset 144h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_REQUEST_STACK (DEBUG_REQUEST_STACK_WORD):** 64B Stack for incoming Device request and Data

19.3.54 DEBUG_RESPONSE_INFO_AND_STATUS_REG (DEBUG_RESPONSE_INFO_AND_STATUS_REG)—Offset 148h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**RESPONSE_DATA_LENGTH (RESPONSE_DATA_LENGTH):** Length of data associated with the current response. This field is valid only when a debug response is available. (bit[0] is set). The length of the data packet will be equal to the response data stack size except when the Request Packet Last = 1 where it may a short packet (< response data stack size)
15:0	0h RO	**RSVD (RSVD)**

19.3.55 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_0)—Offset 180h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.56 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_1)—Offset 184h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.57 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_2)—Offset 188h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.58 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_3)—Offset 18Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.59 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_4)—Offset 190h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.60 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_5)—Offset 194h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.61 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_6)—Offset 198h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.62 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_7)—Offset 19Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.63 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_8)—Offset 1A0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.64 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_9)—Offset 1A4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.65 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_10)—Offset 1A8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.66 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_11)—Offset 1ACh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.67 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_12)—Offset 1B0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.68 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_13)—Offset 1B4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.69 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_14)—Offset 1B8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.70 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_15)—Offset 1BCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.71 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_16)—Offset 1C0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.72 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_17)—Offset 1C4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.73 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_18)—Offset 1C8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.74 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_19)—Offset 1CCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.75 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_20)—Offset 1D0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.76 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_21)—Offset 1D4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.77 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_22)—Offset 1D8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.78 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_23)—Offset 1DCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.79 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_24)—Offset 1E0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.80 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_25)—Offset 1E4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.81 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_26)—Offset 1E8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.82 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_27)—Offset 1ECh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.83 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_28)—Offset 1F0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.84 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_29)—Offset 1F4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.85 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_30)—Offset 1F8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.86 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_31)—Offset 1FCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.87 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_32)—Offset 200h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.88 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_33)—Offset 204h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.89 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_34)—Offset 208h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.90 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_35)—Offset 20Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.91 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_36)—Offset 210h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.92 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_37)—Offset 214h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.93 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_38)—Offset 218h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.94 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_39)—Offset 21Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.95 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_40)—Offset 220h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.96 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_41)—Offset 224h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.97 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_42)—Offset 228h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.98 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_43)—Offset 22Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.99 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_44)—Offset 230h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.100 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_45)—Offset 234h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.101 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_46)—Offset 238h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.102 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_47)—Offset 23Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.103 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_48)—Offset 240h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.104 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_49)—Offset 244h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.105 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_50)—Offset 248h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.106 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_51)—Offset 24Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.107 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_52)—Offset 250h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.108 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_53)—Offset 254h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.109 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_54)—Offset 258h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.110 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_55)—Offset 25Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.111 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_56)—Offset 260h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.112 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_57)—Offset 264h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.113 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_58)—Offset 268h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.114 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_59)—Offset 26Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.115 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_60)—Offset 270h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.116 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_61)—Offset 274h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.117 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_62)—Offset 278h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.118 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_63)—Offset 27Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.119 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_64)—Offset 280h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.120 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_65)—Offset 284h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.121 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_66)—Offset 288h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.122 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_67)—Offset 28Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.123 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_68)—Offset 290h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.124 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_69)—Offset 294h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.125 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_70)—Offset 298h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.126 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_71)—Offset 29Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.127 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_72)—Offset 2A0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.128 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_73)—Offset 2A4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.129 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_74)—Offset 2A8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.130 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_75)—Offset 2ACh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.131 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_76)—Offset 2B0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.132 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_77)—Offset 2B4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.133 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_78)—Offset 2B8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.134 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_79)—Offset 2BCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.135 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_80)—Offset 2C0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.136 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_81)—Offset 2C4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.137 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_82)—Offset 2C8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.138 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_83)—Offset 2CCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.139 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_84)—Offset 2D0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.140 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_85)—Offset 2D4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.141 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_86)—Offset 2D8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.142 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_87)—Offset 2DCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.143 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_88)—Offset 2E0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.144 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_89)—Offset 2E4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.145 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_90)—Offset 2E8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.146 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_91)—Offset 2ECh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.147 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_92)—Offset 2F0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.148 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_93)—Offset 2F4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.149 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_94)—Offset 2F8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.150 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_95)—Offset 2FCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.151 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_96)—Offset 300h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.152 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_97)—Offset 304h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.153 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_98)—Offset 308h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.154 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_99)—Offset 30Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.155 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_100)—Offset 310h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.156 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_101)—Offset 314h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.157 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_102)—Offset 318h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.158 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_103)—Offset 31Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.159 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_104)—Offset 320h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.160 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_105)—Offset 324h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.161 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_106)—Offset 328h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.162 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_107)—Offset 32Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.163 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_108)—Offset 330h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.164 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_109)—Offset 334h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.165 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_110)—Offset 338h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.166 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_111)—Offset 33Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.167 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_112)—Offset 340h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.168 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_113)—Offset 344h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.169 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_114)—Offset 348h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.170 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_115)—Offset 34Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.171 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_116)—Offset 350h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.172 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_117)—Offset 354h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.173 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_118)—Offset 358h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.174 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_119)—Offset 35Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.175 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_120)—Offset 360h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.176 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_121)—Offset 364h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.177 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_122)—Offset 368h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.178 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_123)—Offset 36Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.179 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_124)—Offset 370h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.180 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_125)—Offset 374h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.181 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_126)—Offset 378h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.182 DEBUG_RESPONSE_DATA_STACK (DEBUG_RESPONSE_DATA_STACK_REG_127)—Offset 37Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_DATA (DEBUG_RESPONSE_DATA):** Response Data generated by SW for the current response. Data is valid only when a debug response is available (bit[0] is set) and Response Type = DATA

19.3.183 DEBUG_RESPONSE_HEADER_STACK_REG (DEBUG_RESPONSE_HEADER_STACK_REG_0)—Offset 380h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_HEADER (DEBUG_RESPONSE_HEADER):** Response header generated by SW as a response to the current request/command processed by the SW

19.3.184 DEBUG_RESPONSE_HEADER_STACK_REG (DEBUG_RESPONSE_HEADER_STACK_REG_1)—Offset 384h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_HEADER (DEBUG_RESPONSE_HEADER):** Response header generated by SW as a response to the current request/command processed by the SW

19.3.185 DEBUG_RESPONSE_HEADER_STACK_REG (DEBUG_RESPONSE_HEADER_STACK_REG_2)—Offset 388h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DEBUG_RESPONSE_HEADER (DEBUG_RESPONSE_HEADER):** Response header generated by SW as a response to the current request/command processed by the SW

19.4 Registers Summary

Table 19-4. Summary of USBX device top Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C700h	C703h	DCFG (DCFG)—Offset C700h	80804h
C704h	C707h	DCTL (DCTL)—Offset C704h	F00000h
C708h	C70Bh	DEVTEN (DEVTEN)—Offset C708h	0h
C70Ch	C70Fh	DSTS (DSTS)—Offset C70Ch	520004h
C710h	C713h	DGCMDPAR (DGCMDPAR)—Offset C710h	0h
C714h	C717h	DGCMD (DGCMD)—Offset C714h	0h
C720h	C723h	DALEPENA (DALEPENA)—Offset C720h	0h
C800h	C803h	DEPCMDPAR2_0 (DEPCMDPAR2_0)—Offset C800h	0h
C804h	C807h	DEPCMDPAR1_0 (DEPCMDPAR1_0)—Offset C804h	0h
C808h	C80Bh	DEPCMDPAR0_0 (DEPCMDPAR0_0)—Offset C808h	0h
C80Ch	C80Fh	DEPCMD_0 (DEPCMD_0)—Offset C80Ch	0h
C810h	C813h	DEPCMDPAR2_1 (DEPCMDPAR2_1)—Offset C810h	0h
C814h	C817h	DEPCMDPAR1_1 (DEPCMDPAR1_1)—Offset C814h	0h
C818h	C81Bh	DEPCMDPAR0_1 (DEPCMDPAR0_1)—Offset C818h	0h
C81Ch	C81Fh	DEPCMD_1 (DEPCMD_1)—Offset C81Ch	0h
C820h	C823h	DEPCMDPAR2_2 (DEPCMDPAR2_2)—Offset C820h	0h
C824h	C827h	DEPCMDPAR1_2 (DEPCMDPAR1_2)—Offset C824h	0h
C828h	C82Bh	DEPCMDPAR0_2 (DEPCMDPAR0_2)—Offset C828h	0h
C82Ch	C82Fh	DEPCMD_2 (DEPCMD_2)—Offset C82Ch	0h
C830h	C833h	DEPCMDPAR2_3 (DEPCMDPAR2_3)—Offset C830h	0h
C834h	C837h	DEPCMDPAR1_3 (DEPCMDPAR1_3)—Offset C834h	0h

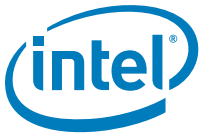


Table 19-4. Summary of USBX device top Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C838h	C83Bh	DEPCMDPAR0_3 (DEPCMDPAR0_3)—Offset C838h	0h
C83Ch	C83Fh	DEPCMD_3 (DEPCMD_3)—Offset C83Ch	0h
C840h	C843h	DEPCMDPAR2_4 (DEPCMDPAR2_4)—Offset C840h	0h
C844h	C847h	DEPCMDPAR1_4 (DEPCMDPAR1_4)—Offset C844h	0h
C848h	C84Bh	DEPCMDPAR0_4 (DEPCMDPAR0_4)—Offset C848h	0h
C84Ch	C84Fh	DEPCMD_4 (DEPCMD_4)—Offset C84Ch	0h
C850h	C853h	DEPCMDPAR2_5 (DEPCMDPAR2_5)—Offset C850h	0h
C854h	C857h	DEPCMDPAR1_5 (DEPCMDPAR1_5)—Offset C854h	0h
C858h	C85Bh	DEPCMDPAR0_5 (DEPCMDPAR0_5)—Offset C858h	0h
C85Ch	C85Fh	DEPCMD_5 (DEPCMD_5)—Offset C85Ch	0h
C860h	C863h	DEPCMDPAR2_6 (DEPCMDPAR2_6)—Offset C860h	0h
C864h	C867h	DEPCMDPAR1_6 (DEPCMDPAR1_6)—Offset C864h	0h
C868h	C86Bh	DEPCMDPAR0_6 (DEPCMDPAR0_6)—Offset C868h	0h
C86Ch	C86Fh	DEPCMD_6 (DEPCMD_6)—Offset C86Ch	0h
C870h	C873h	DEPCMDPAR2_7 (DEPCMDPAR2_7)—Offset C870h	0h
C874h	C877h	DEPCMDPAR1_7 (DEPCMDPAR1_7)—Offset C874h	0h
C878h	C87Bh	DEPCMDPAR0_7 (DEPCMDPAR0_7)—Offset C878h	0h
C87Ch	C87Fh	DEPCMD_7 (DEPCMD_7)—Offset C87Ch	0h
C880h	C883h	DEPCMDPAR2_8 (DEPCMDPAR2_8)—Offset C880h	0h
C884h	C887h	DEPCMDPAR1_8 (DEPCMDPAR1_8)—Offset C884h	0h
C888h	C88Bh	DEPCMDPAR0_8 (DEPCMDPAR0_8)—Offset C888h	0h
C88Ch	C88Fh	DEPCMD_8 (DEPCMD_8)—Offset C88Ch	0h
C890h	C893h	DEPCMDPAR2_9 (DEPCMDPAR2_9)—Offset C890h	0h
C894h	C897h	DEPCMDPAR1_9 (DEPCMDPAR1_9)—Offset C894h	0h
C898h	C89Bh	DEPCMDPAR0_9 (DEPCMDPAR0_9)—Offset C898h	0h
C89Ch	C89Fh	DEPCMD_9 (DEPCMD_9)—Offset C89Ch	0h
C8A0h	C8A3h	DEPCMDPAR2_10 (DEPCMDPAR2_10)—Offset C8A0h	0h
C8A4h	C8A7h	DEPCMDPAR1_10 (DEPCMDPAR1_10)—Offset C8A4h	0h
C8A8h	C8ABh	DEPCMDPAR0_10 (DEPCMDPAR0_10)—Offset C8A8h	0h
C8ACh	C8AFh	DEPCMD_10 (DEPCMD_10)—Offset C8ACh	0h
C8B0h	C8B3h	DEPCMDPAR2_11 (DEPCMDPAR2_11)—Offset C8B0h	0h
C8B4h	C8B7h	DEPCMDPAR1_11 (DEPCMDPAR1_11)—Offset C8B4h	0h
C8B8h	C8BBh	DEPCMDPAR0_11 (DEPCMDPAR0_11)—Offset C8B8h	0h
C8BCh	C8BFh	DEPCMD_11 (DEPCMD_11)—Offset C8BCh	0h
C8C0h	C8C3h	DEPCMDPAR2_12 (DEPCMDPAR2_12)—Offset C8C0h	0h
C8C4h	C8C7h	DEPCMDPAR1_12 (DEPCMDPAR1_12)—Offset C8C4h	0h
C8C8h	C8CBh	DEPCMDPAR0_12 (DEPCMDPAR0_12)—Offset C8C8h	0h
C8CCh	C8CFh	DEPCMD_12 (DEPCMD_12)—Offset C8CCh	0h
C8D0h	C8D3h	DEPCMDPAR2_13 (DEPCMDPAR2_13)—Offset C8D0h	0h
C8D4h	C8D7h	DEPCMDPAR1_13 (DEPCMDPAR1_13)—Offset C8D4h	0h

Table 19-4. Summary of USBX device top Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C8D8h	C8DBh	DEPCMDPAR0_13 (DEPCMDPAR0_13)—Offset C8D8h	0h
C8DCh	C8DFh	DEPCMD_13 (DEPCMD_13)—Offset C8DCh	0h
C8E0h	C8E3h	DEPCMDPAR2_14 (DEPCMDPAR2_14)—Offset C8E0h	0h
C8E4h	C8E7h	DEPCMDPAR1_14 (DEPCMDPAR1_14)—Offset C8E4h	0h
C8E8h	C8EBh	DEPCMDPAR0_14 (DEPCMDPAR0_14)—Offset C8E8h	0h
C8ECh	C8EFh	DEPCMD_14 (DEPCMD_14)—Offset C8ECh	0h
C8F0h	C8F3h	DEPCMDPAR2_15 (DEPCMDPAR2_15)—Offset C8F0h	0h
C8F4h	C8F7h	DEPCMDPAR1_15 (DEPCMDPAR1_15)—Offset C8F4h	0h
C8F8h	C8FBh	DEPCMDPAR0_15 (DEPCMDPAR0_15)—Offset C8F8h	0h
C8FCh	C8FFh	DEPCMD_15 (DEPCMD_15)—Offset C8FCh	0h
C900h	C903h	DEPCMDPAR2_16 (DEPCMDPAR2_16)—Offset C900h	0h
C904h	C907h	DEPCMDPAR1_16 (DEPCMDPAR1_16)—Offset C904h	0h
C908h	C90Bh	DEPCMDPAR0_16 (DEPCMDPAR0_16)—Offset C908h	0h
C90Ch	C90Fh	DEPCMD_16 (DEPCMD_16)—Offset C90Ch	0h
C910h	C913h	DEPCMDPAR2_17 (DEPCMDPAR2_17)—Offset C910h	0h
C914h	C917h	DEPCMDPAR1_17 (DEPCMDPAR1_17)—Offset C914h	0h
C918h	C91Bh	DEPCMDPAR0_17 (DEPCMDPAR0_17)—Offset C918h	0h
C91Ch	C91Fh	DEPCMD_17 (DEPCMD_17)—Offset C91Ch	0h
C920h	C923h	DEPCMDPAR2_18 (DEPCMDPAR2_18)—Offset C920h	0h
C924h	C927h	DEPCMDPAR1_18 (DEPCMDPAR1_18)—Offset C924h	0h
C928h	C92Bh	DEPCMDPAR0_18 (DEPCMDPAR0_18)—Offset C928h	0h
C92Ch	C92Fh	DEPCMD_18 (DEPCMD_18)—Offset C92Ch	0h
C930h	C933h	DEPCMDPAR2_19 (DEPCMDPAR2_19)—Offset C930h	0h
C934h	C937h	DEPCMDPAR1_19 (DEPCMDPAR1_19)—Offset C934h	0h
C938h	C93Bh	DEPCMDPAR0_19 (DEPCMDPAR0_19)—Offset C938h	0h
C93Ch	C93Fh	DEPCMD_19 (DEPCMD_19)—Offset C93Ch	0h
C940h	C943h	DEPCMDPAR2_20 (DEPCMDPAR2_20)—Offset C940h	0h
C944h	C947h	DEPCMDPAR1_20 (DEPCMDPAR1_20)—Offset C944h	0h
C948h	C94Bh	DEPCMDPAR0_20 (DEPCMDPAR0_20)—Offset C948h	0h
C94Ch	C94Fh	DEPCMD_20 (DEPCMD_20)—Offset C94Ch	0h
C950h	C953h	DEPCMDPAR2_21 (DEPCMDPAR2_21)—Offset C950h	0h
C954h	C957h	DEPCMDPAR1_21 (DEPCMDPAR1_21)—Offset C954h	0h
C958h	C95Bh	DEPCMDPAR0_21 (DEPCMDPAR0_21)—Offset C958h	0h
C95Ch	C95Fh	DEPCMD_21 (DEPCMD_21)—Offset C95Ch	0h
C960h	C963h	DEPCMDPAR2_22 (DEPCMDPAR2_22)—Offset C960h	0h
C964h	C967h	DEPCMDPAR1_22 (DEPCMDPAR1_22)—Offset C964h	0h
C968h	C96Bh	DEPCMDPAR0_22 (DEPCMDPAR0_22)—Offset C968h	0h
C96Ch	C96Fh	DEPCMD_22 (DEPCMD_22)—Offset C96Ch	0h
C970h	C973h	DEPCMDPAR2_23 (DEPCMDPAR2_23)—Offset C970h	0h
C974h	C977h	DEPCMDPAR1_23 (DEPCMDPAR1_23)—Offset C974h	0h

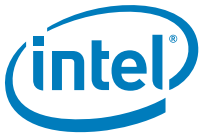


Table 19-4. Summary of USBX device top Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C978h	C97Bh	DEPCMDPAR0_23 (DEPCMDPAR0_23)—Offset C978h	0h
C97Ch	C97Fh	DEPCMD_23 (DEPCMD_23)—Offset C97Ch	0h
C980h	C983h	DEPCMDPAR2_24 (DEPCMDPAR2_24)—Offset C980h	0h
C984h	C987h	DEPCMDPAR1_24 (DEPCMDPAR1_24)—Offset C984h	0h
C988h	C98Bh	DEPCMDPAR0_24 (DEPCMDPAR0_24)—Offset C988h	0h
C98Ch	C98Fh	DEPCMD_24 (DEPCMD_24)—Offset C98Ch	0h
C990h	C993h	DEPCMDPAR2_25 (DEPCMDPAR2_25)—Offset C990h	0h
C994h	C997h	DEPCMDPAR1_25 (DEPCMDPAR1_25)—Offset C994h	0h
C998h	C99Bh	DEPCMDPAR0_25 (DEPCMDPAR0_25)—Offset C998h	0h
C99Ch	C99Fh	DEPCMD_25 (DEPCMD_25)—Offset C99Ch	0h
C9A0h	C9A3h	DEPCMDPAR2_26 (DEPCMDPAR2_26)—Offset C9A0h	0h
C9A4h	C9A7h	DEPCMDPAR1_26 (DEPCMDPAR1_26)—Offset C9A4h	0h
C9A8h	C9ABh	DEPCMDPAR0_26 (DEPCMDPAR0_26)—Offset C9A8h	0h
C9ACh	C9AFh	DEPCMD_26 (DEPCMD_26)—Offset C9ACh	0h
C9B0h	C9B3h	DEPCMDPAR2_27 (DEPCMDPAR2_27)—Offset C9B0h	0h
C9B4h	C9B7h	DEPCMDPAR1_27 (DEPCMDPAR1_27)—Offset C9B4h	0h
C9B8h	C9BBh	DEPCMDPAR0_27 (DEPCMDPAR0_27)—Offset C9B8h	0h
C9BCh	C9BFh	DEPCMD_27 (DEPCMD_27)—Offset C9BCh	0h
C9C0h	C9C3h	DEPCMDPAR2_28 (DEPCMDPAR2_28)—Offset C9C0h	0h
C9C4h	C9C7h	DEPCMDPAR1_28 (DEPCMDPAR1_28)—Offset C9C4h	0h
C9C8h	C9CBh	DEPCMDPAR0_28 (DEPCMDPAR0_28)—Offset C9C8h	0h
C9CCh	C9CFh	DEPCMD_28 (DEPCMD_28)—Offset C9CCh	0h
C9D0h	C9D3h	DEPCMDPAR2_29 (DEPCMDPAR2_29)—Offset C9D0h	0h
C9D4h	C9D7h	DEPCMDPAR1_29 (DEPCMDPAR1_29)—Offset C9D4h	0h
C9D8h	C9DBh	DEPCMDPAR0_29 (DEPCMDPAR0_29)—Offset C9D8h	0h
C9DCh	C9DFh	DEPCMD_29 (DEPCMD_29)—Offset C9DCh	0h
C9E0h	C9E3h	DEPCMDPAR2_30 (DEPCMDPAR2_30)—Offset C9E0h	0h
C9E4h	C9E7h	DEPCMDPAR1_30 (DEPCMDPAR1_30)—Offset C9E4h	0h
C9E8h	C9EBh	DEPCMDPAR0_30 (DEPCMDPAR0_30)—Offset C9E8h	0h
C9ECh	C9EFh	DEPCMD_30 (DEPCMD_30)—Offset C9ECh	0h
C9F0h	C9F3h	DEPCMDPAR2_31 (DEPCMDPAR2_31)—Offset C9F0h	0h
C9F4h	C9F7h	DEPCMDPAR1_31 (DEPCMDPAR1_31)—Offset C9F4h	0h
C9F8h	C9FBh	DEPCMDPAR0_31 (DEPCMDPAR0_31)—Offset C9F8h	0h
C9FCh	C9FFh	DEPCMD_31 (DEPCMD_31)—Offset C9FCh	0h

19.4.1 DCFG (DCFG)—Offset C700h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 80804h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RW	**reserved_32_25 (reserved_32_25)**
24	0h RW	**reserved_24 (reserved_24)**
23	0h RW	**IgnStrmPP (IgnStrmPP)**
22	0h RW	**LPMCAP (LPMCAP)**
21:17	4h RW	**NUMP (NUMP)**
16:12	0h RW	**INTRNUM (INTRNUM)**
11:10	2h RW	**PERFRINT (PERFRINT)**
9:3	0h RW	**DEVADDR (DEVADDR)**
2:0	4h RW	**DEVSPD (DEVSPD)**

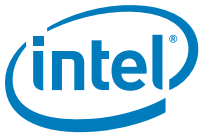
19.4.2 DCTL (DCTL)—Offset C704h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: F00000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RUN_STOP (RUN_STOP)**
30	0h RW	**CSFTRST (CSFTRST)**
29	0h RO	**reserved_30_29 (reserved_30_29)**
28:24	0h RW	**HIRDTHRES (HIRDTHRES)**
23:20	Fh RW	**LPM_NYET_thres (LPM_NYET_thres)**
19	0h RW	**KeepConnect (KeepConnect)**
18	0h RW	**L1HibernationEn (L1HibernationEn)**
17	0h RW	**CRS (CRS)**



Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**CSS (CSS)**
15:13	0h RO	**reserved_16_13 (reserved_16_13)**
12	0h RW	**INITU2ENA (INITU2ENA)**
11	0h RW	**ACCEPTU2ENA (ACCEPTU2ENA)**
10	0h RW	**INITU1ENA (INITU1ENA)**
9	0h RW	**ACCEPTU1ENA (ACCEPTU1ENA)**
8:5	0h WO	**ULSTCHNGREQ (ULSTCHNGREQ)**
4:1	0h RW	**TSTCTL (TSTCTL)**
0	0h RO	**reserved_1_0 (reserved_1_0)**

19.4.3 DEVTEN (DEVTEN)—Offset C708h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**reserved_32_14 (reserved_32_14)**
13	0h RW	**Reserved_13_13 (Reserved_13_13)**
12	0h RW	**VENDEVTSTRCVDEN (VENDEVTSTRCVDEN)**
11	0h RO	**reserved_12_11 (reserved_12_11)**
10	0h RO	**reserved_11_10 (reserved_11_10)**
9	0h RW	**ERRTICERREVTEN (ERRTICERREVTEN)**
8	0h RO	**reserved_9_8 (reserved_9_8)**
7	0h RW	**SOFTEVTEN (SOFTEVTEN)**

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**U3L2L1SuspEn (U3L2L1SuspEn)**
5	0h RW	**HibernationReqEvtEn (HibernationReqEvtEn)**
4	0h RW	**WKUPEVTEN (WKUPEVTEN)**
3	0h RW	**ULSTCNGEN (ULSTCNGEN)**
2	0h RW	**CONNECTDONEEVTEN (CONNECTDONEEVTEN)**
1	0h RW	**USBRSTEVTEN (USBRSTEVTEN)**
0	0h RW	**DISSCONNEVTEN (DISSCONNEVTEN)**

19.4.4 DSTS (DSTS)—Offset C70Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 520004h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**reserved_32_30 (reserved_32_30)**
29	0h RO	**DCNRD (DCNRD)**
28	0h RO	**reserved_29_28 (reserved_29_28)**
27	0h RW	**PLC (PLC)**
26	0h RW	**CSC (CSC)**
25	0h RO	**RSS (RSS)**
24	0h RO	**SSS (SSS)**
23	0h RO	**COREIDLE (COREIDLE)**
22	1h RO	**DEVCTRLHLT (DEVCTRLHLT)**
21:18	4h RO	**USBLNKST (USBLNKST)**

Bit Range	Default & Access	Field Name (ID): Description
17	1h RO	**RXFIFOEMPTY (RXFIFOEMPTY)**
16:3	0h RO	**SOFFN (SOFFN)**
2:0	4h RO	**CONNECTSPD (CONNECTSPD)**

19.4.5 DGCMDPAR (DGCMDPAR)—Offset C710h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.6 DGCMD (DGCMD)—Offset C714h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**reserved_32_16 (reserved_32_16)**
15:12	0h RO	**CMDSTATUS (CMDSTATUS)**
11	0h RO	**reserved_12_11 (reserved_12_11)**
10	0h NA	**CMDACT (CMDACT)**
9	0h RO	**reserved_10_9 (reserved_10_9)**
8	0h RW	**CMDIOC (CMDIOC)**

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**CMDTYP (CMDTYP)**

19.4.7 DALEPENA (DALEPENA)—Offset C720h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**USBACTEP (USBACTEP)**

19.4.8 DEPCMDPAR2_0 (DEPCMDPAR2_0)—Offset C800h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.9 DEPCMDPAR1_0 (DEPCMDPAR1_0)—Offset C804h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.10 DEPCMDPAR0_0 (DEPCMDPAR0_0)—Offset C808h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.11 DEPCMD_0 (DEPCMD_0)—Offset C80Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.12 DEPCMDPAR2_1 (DEPCMDPAR2_1)—Offset C810h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.13 DEPCMDPAR1_1 (DEPCMDPAR1_1)—Offset C814h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.14 DEPCMDPAR0_1 (DEPCMDPAR0_1)—Offset C818h

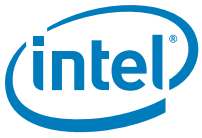
Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.15 DEPCMD_1 (DEPCMD_1)—Offset C81Ch



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.16 DEPCMDPAR2_2 (DEPCMDPAR2_2)—Offset C820h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.17 DEPCMDPAR1_2 (DEPCMDPAR1_2)—Offset C824h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.18 DEPCMDPAR0_2 (DEPCMDPAR0_2)—Offset C828h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.19 DEPCMD_2 (DEPCMD_2)—Offset C82Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.20 DEPCMDPAR2_3 (DEPCMDPAR2_3)—Offset C830h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.21 DEPCMDPAR1_3 (DEPCMDPAR1_3)—Offset C834h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.22 DEPCMDPAR0_3 (DEPCMDPAR0_3)—Offset C838h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.23 DEPCMD_3 (DEPCMD_3)—Offset C83Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.24 DEPCMDPAR2_4 (DEPCMDPAR2_4)—Offset C840h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.25 DEPCMDPAR1_4 (DEPCMDPAR1_4)—Offset C844h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.26 DEPCMDPAR0_4 (DEPCMDPAR0_4)—Offset C848h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.27 DEPCMD_4 (DEPCMD_4)—Offset C84Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.28 DEPCMDPAR2_5 (DEPCMDPAR2_5)—Offset C850h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.29 DEPCMDPAR1_5 (DEPCMDPAR1_5)—Offset C854h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.30 DEPCMDPAR0_5 (DEPCMDPAR0_5)—Offset C858h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.31 DEPCMD_5 (DEPCMD_5)—Offset C85Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.32 DEPCMDPAR2_6 (DEPCMDPAR2_6)—Offset C860h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.33 DEPCMDPAR1_6 (DEPCMDPAR1_6)—Offset C864h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.34 DEPCMDPAR0_6 (DEPCMDPAR0_6)—Offset C868h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.35 DEPCMD_6 (DEPCMD_6)—Offset C86Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.36 DEPCMDPAR2_7 (DEPCMDPAR2_7)—Offset C870h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.37 DEPCMDPAR1_7 (DEPCMDPAR1_7)—Offset C874h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.38 DEPCMDPAR0_7 (DEPCMDPAR0_7)—Offset C878h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.39 DEPCMD_7 (DEPCMD_7)—Offset C87Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.40 DEPCMDPAR2_8 (DEPCMDPAR2_8)—Offset C880h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.41 DEPCMDPAR1_8 (DEPCMDPAR1_8)—Offset C884h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.42 DEPCMDPAR0_8 (DEPCMDPAR0_8)—Offset C888h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.43 DEPCMD_8 (DEPCMD_8)—Offset C88Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.44 DEPCMDPAR2_9 (DEPCMDPAR2_9)—Offset C890h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

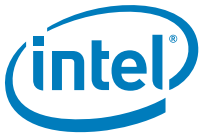
19.4.45 DEPCMDPAR1_9 (DEPCMDPAR1_9)—Offset C894h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**



19.4.46 DEPCMDPAR0_9 (DEPCMDPAR0_9)—Offset C898h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.47 DEPCMD_9 (DEPCMD_9)—Offset C89Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.48 DEPCMDPAR2_10 (DEPCMDPAR2_10)—Offset C8A0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.49 DEPCMDPAR1_10 (DEPCMDPAR1_10)—Offset C8A4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.50 DEPCMDPAR0_10 (DEPCMDPAR0_10)—Offset C8A8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.51 DEPCMD_10 (DEPCMD_10)—Offset C8ACh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.52 DEPCMDPAR2_11 (DEPCMDPAR2_11)—Offset C8B0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.53 DEPCMDPAR1_11 (DEPCMDPAR1_11)—Offset C8B4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.54 DEPCMDPAR0_11 (DEPCMDPAR0_11)—Offset C8B8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.55 DEPCMD_11 (DEPCMD_11)—Offset C8BCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.56 DEPCMDPAR2_12 (DEPCMDPAR2_12)—Offset C8C0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.57 DEPCMDPAR1_12 (DEPCMDPAR1_12)—Offset C8C4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.58 DEPCMDPAR0_12 (DEPCMDPAR0_12)—Offset C8C8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.59 DEPCMD_12 (DEPCMD_12)—Offset C8CCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.60 DEPCMDPAR2_13 (DEPCMDPAR2_13)—Offset C8D0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.61 DEPCMDPAR1_13 (DEPCMDPAR1_13)—Offset C8D4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.62 DEPCMDPAR0_13 (DEPCMDPAR0_13)—Offset C8D8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.63 DEPCMD_13 (DEPCMD_13)—Offset C8DCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.64 DEPCMDPAR2_14 (DEPCMDPAR2_14)—Offset C8E0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.65 DEPCMDPAR1_14 (DEPCMDPAR1_14)—Offset C8E4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.66 DEPCMDPAR0_14 (DEPCMDPAR0_14)—Offset C8E8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.67 DEPCMD_14 (DEPCMD_14)—Offset C8ECh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.68 DEPCMDPAR2_15 (DEPCMDPAR2_15)—Offset C8F0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.69 DEPCMDPAR1_15 (DEPCMDPAR1_15)—Offset C8F4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.70 DEPCMDPAR0_15 (DEPCMDPAR0_15)—Offset C8F8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.71 DEPCMD_15 (DEPCMD_15)—Offset C8FCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.72 DEPCMDPAR2_16 (DEPCMDPAR2_16)—Offset C900h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.73 DEPCMDPAR1_16 (DEPCMDPAR1_16)—Offset C904h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.74 DEPCMDPAR0_16 (DEPCMDPAR0_16)—Offset C908h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.75 DEPCMD_16 (DEPCMD_16)—Offset C90Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.76 DEPCMDPAR2_17 (DEPCMDPAR2_17)—Offset C910h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

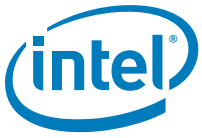
19.4.77 DEPCMDPAR1_17 (DEPCMDPAR1_17)—Offset C914h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**



19.4.78 DEPCMDPAR0_17 (DEPCMDPAR0_17)—Offset C918h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.79 DEPCMD_17 (DEPCMD_17)—Offset C91Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.80 DEPCMDPAR2_18 (DEPCMDPAR2_18)—Offset C920h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.81 DEPCMDPAR1_18 (DEPCMDPAR1_18)—Offset C924h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.82 DEPCMDPAR0_18 (DEPCMDPAR0_18)—Offset C928h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.83 DEPCMD_18 (DEPCMD_18)—Offset C92Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.84 DEPCMDPAR2_19 (DEPCMDPAR2_19)—Offset C930h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.85 DEPCMDPAR1_19 (DEPCMDPAR1_19)—Offset C934h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.86 DEPCMDPAR0_19 (DEPCMDPAR0_19)—Offset C938h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.87 DEPCMD_19 (DEPCMD_19)—Offset C93Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.88 DEPCMDPAR2_20 (DEPCMDPAR2_20)—Offset C940h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.89 DEPCMDPAR1_20 (DEPCMDPAR1_20)—Offset C944h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.90 DEPCMDPAR0_20 (DEPCMDPAR0_20)—Offset C948h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.91 DEPCMD_20 (DEPCMD_20)—Offset C94Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.92 DEPCMDPAR2_21 (DEPCMDPAR2_21)—Offset C950h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.93 DEPCMDPAR1_21 (DEPCMDPAR1_21)—Offset C954h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.94 DEPCMDPAR0_21 (DEPCMDPAR0_21)—Offset C958h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.95 DEPCMD_21 (DEPCMD_21)—Offset C95Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.96 DEPCMDPAR2_22 (DEPCMDPAR2_22)—Offset C960h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.97 DEPCMDPAR1_22 (DEPCMDPAR1_22)—Offset C964h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.98 DEPCMDPAR0_22 (DEPCMDPAR0_22)—Offset C968h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.99 DEPCMD_22 (DEPCMD_22)—Offset C96Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.100 DEPCMDPAR2_23 (DEPCMDPAR2_23)—Offset C970h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.101 DEPCMDPAR1_23 (DEPCMDPAR1_23)—Offset C974h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.102 DEPCMDPAR0_23 (DEPCMDPAR0_23)—Offset C978h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.103 DEPCMD_23 (DEPCMD_23)—Offset C97Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.104 DEPCMDPAR2_24 (DEPCMDPAR2_24)—Offset C980h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.105 DEPCMDPAR1_24 (DEPCMDPAR1_24)—Offset C984h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.106 DEPCMDPAR0_24 (DEPCMDPAR0_24)—Offset C988h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.107 DEPCMD_24 (DEPCMD_24)—Offset C98Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.108 DEPCMDPAR2_25 (DEPCMDPAR2_25)—Offset C990h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

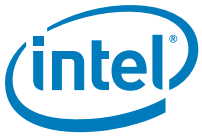
19.4.109 DEPCMDPAR1_25 (DEPCMDPAR1_25)—Offset C994h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**



19.4.110 DEPCMDPAR0_25 (DEPCMDPAR0_25)—Offset C998h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.111 DEPCMD_25 (DEPCMD_25)—Offset C99Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.112 DEPCMDPAR2_26 (DEPCMDPAR2_26)—Offset C9A0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.113 DEPCMDPAR1_26 (DEPCMDPAR1_26)—Offset C9A4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.114 DEPCMDPAR0_26 (DEPCMDPAR0_26)—Offset C9A8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.115 DEPCMD_26 (DEPCMD_26)—Offset C9ACh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.116 DEPCMDPAR2_27 (DEPCMDPAR2_27)—Offset C9B0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.117 DEPCMDPAR1_27 (DEPCMDPAR1_27)—Offset C9B4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.118 DEPCMDPAR0_27 (DEPCMDPAR0_27)—Offset C9B8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.119 DEPCMD_27 (DEPCMD_27)—Offset C9BCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.120 DEPCMDPAR2_28 (DEPCMDPAR2_28)—Offset C9C0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.121 DEPCMDPAR1_28 (DEPCMDPAR1_28)—Offset C9C4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.122 DEPCMDPAR0_28 (DEPCMDPAR0_28)—Offset C9C8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.123 DEPCMD_28 (DEPCMD_28)—Offset C9CCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.124 DEPCMDPAR2_29 (DEPCMDPAR2_29)—Offset C9D0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

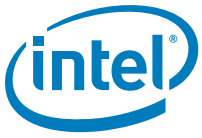
19.4.125 DEPCMDPAR1_29 (DEPCMDPAR1_29)—Offset C9D4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**



19.4.126 DEPCMDPAR0_29 (DEPCMDPAR0_29)—Offset C9D8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.127 DEPCMD_29 (DEPCMD_29)—Offset C9DCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.128 DEPCMDPAR2_30 (DEPCMDPAR2_30)—Offset C9E0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.129 DEPCMDPAR1_30 (DEPCMDPAR1_30)—Offset C9E4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.130 DEPCMDPAR0_30 (DEPCMDPAR0_30)—Offset C9E8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.131 DEPCMD_30 (DEPCMD_30)—Offset C9ECh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**

19.4.132 DEPCMDPAR2_31 (DEPCMDPAR2_31)—Offset C9F0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.133 DEPCMDPAR1_31 (DEPCMDPAR1_31)—Offset C9F4h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

19.4.134 DEPCMDPAR0_31 (DEPCMDPAR0_31)—Offset C9F8h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER)**

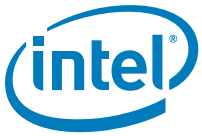
19.4.135 DEPCMD_31 (DEPCMD_31)—Offset C9FCh

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**COMMANDPARAM (COMMANDPARAM)**
15:12	0h RW	**CMDSTATUS (CMDSTATUS)**
11	0h RW	**HIPRI_FORCERM (HIPRI_FORCERM)**
10	0h RW	**CMDACT (CMDACT)**
9	0h RW	**reserved_10_1 (reserved_10_1)**
8	0h RW	**CMDIOC (CMDIOC)**
7:4	0h RW	**reserved_8_4 (reserved_8_4)**
3:0	0h RW	**CMDTYP (CMDTYP)**



19.5 Registers Summary

Table 19-5. Summary of USBX device top Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C100h	C103h	GSBUSCFG0 (GSBUSCFG0)—Offset C100h	6h
C104h	C107h	GSBUSCFG1 (GSBUSCFG1)—Offset C104h	F00h
C108h	C10Bh	GTXTHRCFG (GTXTHRCFG)—Offset C108h	0h
C10Ch	C10Fh	GRXTHRCFG (GRXTHRCFG)—Offset C10Ch	24400000h
C110h	C113h	GCTL (GCTL)—Offset C110h	102000h
C114h	C117h	GPMSTS (GPMSTS)—Offset C114h	0h
C118h	C11Bh	GSTS (GSTS)—Offset C118h	3E800000h
C11Ch	C11Fh	GUCTL1 (GUCTL1)—Offset C11Ch	2h
C120h	C123h	GSNPSID (GSNPSID)—Offset C120h	5533260Ah
C124h	C127h	GGPIO (GGPIO)—Offset C124h	0h
C128h	C12Bh	GUID (GUID)—Offset C128h	8086A0h
C12Ch	C12Fh	GUCTL (GUCTL)—Offset C12Ch	10h
C130h	C133h	GBUSERRADDRLO (GBUSERRADDRLO)—Offset C130h	0h
C134h	C137h	GBUSERRADDRHI (GBUSERRADDRHI)—Offset C134h	0h
C138h	C13Bh	GPRTBIMAPLO (GPRTBIMAPLO)—Offset C138h	0h
C13Ch	C13Fh	GPRTBIMAPHI (GPRTBIMAPHI)—Offset C13Ch	0h
C140h	C143h	GHWPARAMS0 (GHWPARAMS0)—Offset C140h	40204008h
C144h	C147h	GHWPARAMS1 (GHWPARAMS1)—Offset C144h	260C93Bh
C148h	C14Bh	GHWPARAMS2 (GHWPARAMS2)—Offset C148h	8086A0h
C14Ch	C14Fh	GHWPARAMS3 (GHWPARAMS3)—Offset C14Ch	10420085h
C150h	C153h	GHWPARAMS4 (GHWPARAMS4)—Offset C150h	47A22004h
C154h	C157h	GHWPARAMS5 (GHWPARAMS5)—Offset C154h	4202088h
C158h	C15Bh	GHWPARAMS6 (GHWPARAMS6)—Offset C158h	2F60020h
C15Ch	C15Fh	GHWPARAMS7 (GHWPARAMS7)—Offset C15Ch	38507E6h
C160h	C163h	GDBGFIFOSPACE (GDBGFIFOSPACE)—Offset C160h	420000h
C164h	C167h	GDBGLTSSM (GDBGLTSSM)—Offset C164h	1010440h
C168h	C16Bh	GDBGLNMCC (GDBGLNMCC)—Offset C168h	0h
C16Ch	C16Fh	GDBGBMU (GDBGBMU)—Offset C16Ch	0h
C170h	C173h	GDBGLSPMUX_DEV (GDBGLSPMUX_DEV)—Offset C170h	3F0000h
C174h	C177h	GDBGLSP (GDBGLSP)—Offset C174h	0h
C178h	C17Bh	GDBGEPINFO0 (GDBGEPINFO0)—Offset C178h	0h
C17Ch	C17Fh	GDBGEPINFO1 (GDBGEPINFO1)—Offset C17Ch	800000h
C180h	C183h	GPRTBIMAP_HSLO (GPRTBIMAP_HSLO)—Offset C180h	0h
C184h	C187h	GPRTBIMAP_HSHI (GPRTBIMAP_HSHI)—Offset C184h	0h
C188h	C18Bh	GPRTBIMAP_FSLO (GPRTBIMAP_FSLO)—Offset C188h	0h
C18Ch	C18Fh	GPRTBIMAP_FSHI (GPRTBIMAP_FSHI)—Offset C18Ch	0h
C200h	C203h	GUSB2PHYCFG_0 (GUSB2PHYCFG_0)—Offset C200h	2400h
C240h	C243h	GUSB2I2CCTL_0 (GUSB2I2CCTL_0)—Offset C240h	0h

Table 19-5. Summary of USBX device top Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C280h	C283h	GUSB2PHYACC_ULPI_0 (GUSB2PHYACC_ULPI_0)—Offset C280h	0h
C2C0h	C2C3h	GUSB3PIPECTL_0 (GUSB3PIPECTL_0)—Offset C2C0h	2020002h
C300h	C303h	GTXFIFOSIZ0_0 (GTXFIFOSIZ0_0)—Offset C300h	42h
C304h	C307h	GTXFIFOSIZ1_0 (GTXFIFOSIZ1_0)—Offset C304h	420184h
C308h	C30Bh	GTXFIFOSIZ2_0 (GTXFIFOSIZ2_0)—Offset C308h	1C60184h
C30Ch	C30Fh	GTXFIFOSIZ3_0 (GTXFIFOSIZ3_0)—Offset C30Ch	34A0184h
C310h	C313h	GTXFIFOSIZ4_0 (GTXFIFOSIZ4_0)—Offset C310h	4CE0082h
C314h	C317h	GTXFIFOSIZ5_0 (GTXFIFOSIZ5_0)—Offset C314h	5500082h
C318h	C31Bh	GTXFIFOSIZ6_0 (GTXFIFOSIZ6_0)—Offset C318h	5D20082h
C31Ch	C31Fh	GTXFIFOSIZ7_0 (GTXFIFOSIZ7_0)—Offset C31Ch	6540082h
C320h	C323h	GTXFIFOSIZ8_0 (GTXFIFOSIZ8_0)—Offset C320h	6D60022h
C324h	C327h	GTXFIFOSIZ9_0 (GTXFIFOSIZ9_0)—Offset C324h	6F80022h
C328h	C32Bh	GTXFIFOSIZ10_0 (GTXFIFOSIZ10_0)—Offset C328h	71A0022h
C32Ch	C32Fh	GTXFIFOSIZ11_0 (GTXFIFOSIZ11_0)—Offset C32Ch	73C0022h
C330h	C333h	GTXFIFOSIZ12_0 (GTXFIFOSIZ12_0)—Offset C330h	75E0022h
C334h	C337h	GTXFIFOSIZ13_0 (GTXFIFOSIZ13_0)—Offset C334h	7800022h
C338h	C33Bh	GTXFIFOSIZ14_0 (GTXFIFOSIZ14_0)—Offset C338h	7A20022h
C33Ch	C33Fh	GTXFIFOSIZ15_0 (GTXFIFOSIZ15_0)—Offset C33Ch	7C40022h
C380h	C383h	GRXFIFOSIZ0_0 (GRXFIFOSIZ0_0)—Offset C380h	385h
C400h	C403h	GEVNTADRLO_0 (GEVNTADRLO_0)—Offset C400h	0h
C404h	C407h	GEVNTADRHI_0 (GEVNTADRHI_0)—Offset C404h	0h
C408h	C40Bh	GEVNTSIZ_0 (GEVNTSIZ_0)—Offset C408h	0h
C40Ch	C40Fh	GEVNTCOUNT_0 (GEVNTCOUNT_0)—Offset C40Ch	0h
C600h	C603h	GHWPARAMS8 (GHWPARAMS8)—Offset C600h	2F6h
C610h	C613h	GTXFIFOPRIDEV (GTXFIFOPRIDEV)—Offset C610h	0h
C630h	C633h	GFLADJ (GFLADJ)—Offset C630h	0h

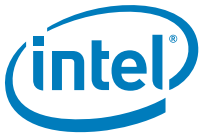
19.5.1 GSBUSCFG0 (GSBUSCFG0)—Offset C100h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**reserved_32_16 (reserved_32_16)**



Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**reserved_16_15 (reserved_16_15)**
14:13	0h RW	**reserved_15_13 (reserved_15_13)**
12	0h RW	**STOREANDFORWARD (STOREANDFORWARD)**
11	0h RW	**DATBIGEND (DATBIGEND)**
10	0h RW	**DESBIGEND (DESBIGEND)**
9:8	0h RO	**reserved_10_8 (reserved_10_8)**
7	0h RW	**INCR256BRSTENA (INCR256BRSTENA)**
6	0h RW	**INCR128BRSTENA (INCR128BRSTENA)**
5	0h RW	**INCR64BRSTENA (INCR64BRSTENA)**
4	0h RW	**INCR32BRSTENA (INCR32BRSTENA)**
3	0h RW	**INCR16BRSTENA (INCR16BRSTENA)**
2	1h RW	**INCR8BRSTENA (INCR8BRSTENA)**
1	1h RW	**INCR4BRSTENA (INCR4BRSTENA)**
0	0h RW	**INCRBRSTENA (INCRBRSTENA)**

19.5.2 GSBUSCFG1 (GSBUSCFG1)—Offset C104h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: F00h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**reserved_32_13 (reserved_32_13)**
12	0h RW	**EN1KPAGE (EN1KPAGE)**
11:8	Fh RW	**PipeTransLimit (PipeTransLimit)**

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW	**DATADRSPC (DATADRSPC)**
3:0	0h RW	**DESADRSPC (DESADRSPC)**

19.5.3 GTXTHRCFG (GTXTHRCFG)—Offset C108h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

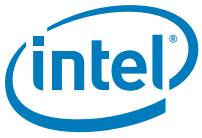
Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**USBISOTHREN (USBISOTHREN)**
30	0h RW	**reserved_31_30 (reserved_31_30)**
29	0h RO	**USBTxPktCntSel (USBTxPktCntSel)**
28	0h RO	**reserved_29_28 (reserved_29_28)**
27:24	0h RO	**USBTxPktCnt (USBTxPktCnt)**
23:16	0h RW	**USBMaxTxBurstSize (USBMaxTxBurstSize)**
15	0h RW	**Reserved_15_15 (Reserved_15_15)**
14	0h RW	**reserved_15_14 (reserved_15_14)**
13:11	0h RO	**reserved_14_11 (reserved_14_11)**
10:0	0h RW	**reserved_11_0 (reserved_11_0)**

19.5.4 GRXTHRCFG (GRXTHRCFG)—Offset C10Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 24400000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**reserved_32_30 (reserved_32_30)**
29	1h RW	**USBRxPktCntSel (USBRxPktCntSel)**
28	0h RO	**reserved_29_28 (reserved_29_28)**
27:24	4h RW	**USBRxPktCnt (USBRxPktCnt)**
23:19	8h RW	**USBMaxRxBurstSize (USBMaxRxBurstSize)**
18:16	0h RO	**reserved_19_16 (reserved_19_16)**
15	0h RW	**reserved_16_15 (reserved_16_15)**
14:11	0h RO	**reserved_15_11 (reserved_15_11)**
10:0	0h RO	**reserved_11_0 (reserved_11_0)**

19.5.5 GCTL (GCTL)—Offset C110h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 102000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	2h RW	**PWRDNSCALE (PWRDNSCALE)**
18	0h RW	**MASTERFILTBYPASS (MASTERFILTBYPASS)**
17	0h RW	**BYPSSETADDR (BYPSSETADDR)**
16	0h RW	**U2RSTECN (U2RSTECN)**
15:14	0h RW	**FRMSCLDWN (FRMSCLDWN)**
13:12	2h RW	**PRTCAPDIR (PRTCAPDIR)**
11	0h RW	**CORESOFTRESET (CORESOFTRESET)**
10	0h RW	**SOFITPSYNC (SOFITPSYNC)**

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**U1U2TimerScale (U1U2TimerScale)**
8	0h RW	**DEBUGATTACH (DEBUGATTACH)**
7:6	0h RW	**RAMCLKSEL (RAMCLKSEL)**
5:4	0h RW	**SCALEDOWN (SCALEDOWN)**
3	0h RW	**DISSCRAMBLE (DISSCRAMBLE)**
2	0h RW	**U2EXIT_LFPS (U2EXIT_LFPS)**
1	0h RW	**GblHibernationEn (GblHibernationEn)**
0	0h RW	**DSBLCLKGTNG (DSBLCLKGTNG)**

19.5.6 GPMSTS (GPMSTS)—Offset C114h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h WO	**PortSel (PortSel)**
27:16	0h RW	**Reserved_16_27 (Reserved_16_27)**
15:12	0h RO	**U3Wakeup (U3Wakeup)**
11:9	0h RW	**Reserved_9_11 (Reserved_9_11)**
8:0	0h RO	**U2Wakeup (U2Wakeup)**

19.5.7 GSTS (GSTS)—Offset C118h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3E800000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	3E8h RO	**CBELT (CBELT)**
19:12	0h RO	**reserved_20_12 (reserved_20_12)**
11	0h RO	**RSVD**
10	0h RO	**OTG_IP (OTG_IP)**
9	0h RO	**BC_IP (BC_IP)**
8	0h RO	**ADP_IP (ADP_IP)**
7	0h RO	**Host_IP (Host_IP)**
6	0h RO	**Device_IP (Device_IP)**
5	0h RO	**CSRTimeout (CSRTimeout)**
4	0h RO	**BUSERRADDRVLD (BUSERRADDRVLD)**
3:2	0h RO	**reserved_4_2 (reserved_4_2)**
1:0	0h RO	**CURMOD (CURMOD)**

19.5.8 GUCTL1 (GUCTL1)—Offset C11Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**reserved_32_15 (reserved_32_15)**
14:9	0h RW	**Reserved_15_9 (Reserved_15_9)**
8	0h RW	**L1_SUSP_THRLD_EN_FOR_HOST (L1_SUSP_THRLD_EN_FOR_HOST)**
7:4	0h RW	**L1_SUSP_THRLD_FOR_HOST (L1_SUSP_THRLD_FOR_HOST)**

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**HC_ERRATA_ENABLE (HC_ERRATA_ENABLE)**
2	0h RW	**HC_PARCHK_DISABLE (HC_PARCHK_DISABLE)**
1	1h RW	**OVRLD_L1_SUSP_COM (OVRLD_L1_SUSP_COM)**
0	0h RW	**LOA_FILTER_EN (LOA_FILTER_EN)**

19.5.9 GSNPSID (GSNPSID)—Offset C120h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 5533260Ah

Bit Range	Default & Access	Field Name (ID): Description
31:0	5533260Ah RO	**SYNOPSYSID (SYNOPSYSID)**

19.5.10 GGPIO (GGPIO)—Offset C124h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**GPO (GPO)**
15:0	0h RO	**GPI (GPI)**

19.5.11 GUID (GUID)—Offset C128h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8086A0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	8086A0h RW	**USERID (USERID)**

19.5.12 GUCTL (GUCTL)—Offset C12Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RW	**REFCLKPER (REFCLKPER)**
21	0h RW	**NoExtrDl (NoExtrDl)**
20:18	0h RW	**PSQExtrResSp (PSQExtrResSp)**
17	0h RW	**SprsCtrlTransEn (SprsCtrlTransEn)**
16	0h RO	**reserved_17_16 (reserved_17_16)**
15	0h RO	**reserved_16_15 (reserved_16_15)**
14	0h RW	**USBHstInAutoRetryEn (USBHstInAutoRetryEn)**
13	0h RW	**EnOverlapChk (EnOverlapChk)**
12	0h RW	**ExtCapSupptEN (ExtCapSupptEN)**
11	0h RW	**InsrtExtrFSBODI (InsrtExtrFSBODI)**
10:9	0h RW	**DTCT (DTCT)**
8:0	10h RW	**DTFT (DTFT)**

19.5.13 GBUSERRADDRLO (GBUSERRADDRLO)—Offset C130h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**BUSERRADDR (BUSERRADDR)**

19.5.14 GBUSERRADDRHI (GBUSERRADDRHI)—Offset C134h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**BUSERRADDR (BUSERRADDR)**

19.5.15 GPRTBIMAPLO (GPRTBIMAPLO)—Offset C138h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**BINUM8 (BINUM8)**
27:24	0h RO	**BINUM7 (BINUM7)**
23:20	0h RO	**BINUM6 (BINUM6)**
19:16	0h RO	**BINUM5 (BINUM5)**
15:12	0h RO	**BINUM4 (BINUM4)**
11:8	0h RO	**BINUM3 (BINUM3)**

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	**BINUM2 (BINUM2)**
3:0	0h RW	**BINUM1 (BINUM1)**

19.5.16 GPRTBIMAPHI (GPRTBIMAPHI)—Offset C13Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**reserved_32_28 (reserved_32_28)**
27:24	0h RO	**BINUM15 (BINUM15)**
23:20	0h RO	**BINUM14 (BINUM14)**
19:16	0h RO	**BINUM13 (BINUM13)**
15:12	0h RO	**BINUM12 (BINUM12)**
11:8	0h RO	**BINUM11 (BINUM11)**
7:4	0h RO	**BINUM10 (BINUM10)**
3:0	0h RO	**BINUM9 (BINUM9)**

19.5.17 GHWPARAMS0 (GHWPARAMS0)—Offset C140h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40204008h

Bit Range	Default & Access	Field Name (ID): Description
31:24	40h RO	**DWC_USB3_ADWIDTH_31_24 (DWC_USB3_ADWIDTH_31_24)**
23:16	20h RO	**DWC_USB3_SDWIDTH_23_16 (DWC_USB3_SDWIDTH_23_16)**
15:8	40h RO	**DWC_USB3_MDWIDTH_15_8 (DWC_USB3_MDWIDTH_15_8)**
7:6	0h RO	**DWC_USB3_SBUS_TYPE_7_6 (DWC_USB3_SBUS_TYPE_7_6)**
5:3	1h RO	**DWC_USB3_MBUS_TYPE_5_3 (DWC_USB3_MBUS_TYPE_5_3)**
2:0	0h RO	**DWC_USB3_MODE_2_0 (DWC_USB3_MODE_2_0)**

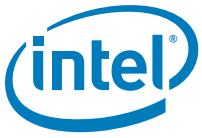
19.5.18 GHWPARAMS1 (GHWPARAMS1)—Offset C144h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 260C93Bh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved_31 (Reserved_31)**
30	0h RO	**DWC_USB3_RM_OPT_FEATURES_30 (DWC_USB3_RM_OPT_FEATURES_30)**
29	0h RO	**Reserved1_29 (Reserved1_29)**
28	0h RO	**DWC_USB3_RAM_BUS_CLKS_SYNC_28 (DWC_USB3_RAM_BUS_CLKS_SYNC_28)**
27	0h RO	**DWC_USB3_MAC_RAM_CLKS_SYNC_27 (DWC_USB3_MAC_RAM_CLKS_SYNC_27)**
26	0h RO	**DWC_USB3_MAC_PHY_CLKS_SYNC_26 (DWC_USB3_MAC_PHY_CLKS_SYNC_26)**
25:24	2h RO	**DWC_USB3_EN_PWROPT_25_24 (DWC_USB3_EN_PWROPT_25_24)**
23	0h RO	**DWC_USB3_SPRAM_TYP_23 (DWC_USB3_SPRAM_TYP_23)**
22:21	3h RO	**DWC_USB3_NUM_RAMS_22_21 (DWC_USB3_NUM_RAMS_22_21)**



Bit Range	Default & Access	Field Name (ID): Description
20:15	1h RO	**DWC_USB3_DEVICE_NUM_INT_20_15 (DWC_USB3_DEVICE_NUM_INT_20_15)**
14:12	4h RO	**DWC_USB3_ASPACEWIDTH_14_12 (DWC_USB3_ASPACEWIDTH_14_12)**
11:9	4h RO	**DWC_USB3_REQINFOWIDTH_11_9 (DWC_USB3_REQINFOWIDTH_11_9)**
8:6	4h RO	**DWC_USB3_DATAINFOWIDTH_8_6 (DWC_USB3_DATAINFOWIDTH_8_6)**
5:3	7h RO	**DWC_USB3_BURSTWIDTH_5_3 (DWC_USB3_BURSTWIDTH_5_3)**
2:0	3h RO	**DWC_USB3_IDWIDTH_2_0 (DWC_USB3_IDWIDTH_2_0)**

19.5.19 GHWPARAMS2 (GHWPARAMS2)—Offset C148h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8086A0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	8086A0h RO	**DWC_USB3_USERID_31_0 (DWC_USB3_USERID_31_0)**

19.5.20 GHWPARAMS3 (GHWPARAMS3)—Offset C14Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10420085h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved_31 (Reserved_31)**
30:23	20h RO	**DWC_USB3_CACHE_TOTAL_XFER_RESOURCES_30_23 (DWC_USB3_CACHE_TOTAL_XFER_RESOURCES_30_23)**

Bit Range	Default & Access	Field Name (ID): Description
22:18	10h RO	**DWC_USB3_NUM_IN_EPS_22_18 (DWC_USB3_NUM_IN_EPS_22_18)**
17:12	20h RO	**DWC_USB3_NUM_EPS_17_12 (DWC_USB3_NUM_EPS_17_12)**
11	0h RO	**DWC_USB3_ULPI_CARKIT_11 (DWC_USB3_ULPI_CARKIT_11)**
10	0h RO	**DWC_USB3_VENDOR_CTL_INTERFACE_10 (DWC_USB3_VENDOR_CTL_INTERFACE_10)**
9:8	0h RO	**ghwparams3_9_8 (ghwparams3_9_8)**
7:6	2h RO	**DWC_USB3_HSPHY_DWIDTH_7_6 (DWC_USB3_HSPHY_DWIDTH_7_6)**
5:4	0h RO	**DWC_USB3_FSPHY_INTERFACE_5_4 (DWC_USB3_FSPHY_INTERFACE_5_4)**
3:2	1h RO	**DWC_USB3_HSPHY_INTERFACE_3_2 (DWC_USB3_HSPHY_INTERFACE_3_2)**
1:0	1h RO	**DWC_USB3_SSPHY_INTERFACE_1_0 (DWC_USB3_SSPHY_INTERFACE_1_0)**

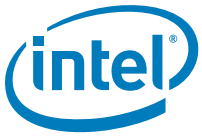
19.5.21 GHWPARAMS4 (GHWPARAMS4)—Offset C150h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 47A22004h

Bit Range	Default & Access	Field Name (ID): Description
31:28	4h RO	**DWC_USB3_BMU_LSP_DEPTH_31_28 (DWC_USB3_BMU_LSP_DEPTH_31_28)**
27:24	7h RO	**DWC_USB3_BMU_PTL_DEPTH_27_24 (DWC_USB3_BMU_PTL_DEPTH_27_24)**
23	1h RO	**DWC_USB3_EN_ISOC_SUPT_23 (DWC_USB3_EN_ISOC_SUPT_23)**
22	0h RO	**Reserved_22 (Reserved_22)**
21	1h RO	**DWC_USB3_EXT_BUFF_CONTROL_21 (DWC_USB3_EXT_BUFF_CONTROL_21)**
20:17	1h RO	**DWC_USB3_NUM_SS_USB_INSTANCES_20_17 (DWC_USB3_NUM_SS_USB_INSTANCES_20_17)**



Bit Range	Default & Access	Field Name (ID): Description
16:13	1h RO	**RSVD**
12	0h RO	**ghwparams4_12 (ghwparams4_12)**
11	0h RO	**ghwparams4_11 (ghwparams4_11)**
10:9	0h RO	**ghwparams4_10_9 (ghwparams4_10_9)**
8:7	0h RO	**ghwparams4_8_7 (ghwparams4_8_7)**
6	0h RO	**ghwparams4_6 (ghwparams4_6)**
5:0	4h RO	**DWC_USB3_CACHE_TRBS_PER_TRANSFER_5_0 (DWC_USB3_CACHE_TRBS_PER_TRANSFER_5_0)**

19.5.22 GHWPARAMS5 (GHWPARAMS5)—Offset C154h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4202088h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved_31_28 (Reserved_31_28)**
27:22	10h RO	**DWC_USB3_DFQ_FIFO_DEPTH_27_22 (DWC_USB3_DFQ_FIFO_DEPTH_27_22)**
21:16	20h RO	**DWC_USB3_DWQ_FIFO_DEPTH_21_16 (DWC_USB3_DWQ_FIFO_DEPTH_21_16)**
15:10	8h RO	**DWC_USB3_TXQ_FIFO_DEPTH_15_10 (DWC_USB3_TXQ_FIFO_DEPTH_15_10)**
9:4	8h RO	**DWC_USB3_RXQ_FIFO_DEPTH_9_4 (DWC_USB3_RXQ_FIFO_DEPTH_9_4)**
3:0	8h RO	**DWC_USB3_BMU_BUSGM_DEPTH_3_0 (DWC_USB3_BMU_BUSGM_DEPTH_3_0)**

19.5.23 GHWPARAMS6 (GHWPARAMS6)—Offset C158h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2F60020h

Bit Range	Default & Access	Field Name (ID): Description
31:16	2F6h RO	**DWC_USB3_RAM0_DEPTH_31_16 (DWC_USB3_RAM0_DEPTH_31_16)**
15	0h RO	**BusFltrsSupport (BusFltrsSupport)**
14	0h RO	**BCSupport (BCSupport)**
13	0h RO	**OTG_SS_Support (OTG_SS_Support)**
12	0h RO	**ADPSupport (ADPSupport)**
11	0h RO	**HNPSupport (HNPSupport)**
10	0h RO	**SRPSupport (SRPSupport)**
9:8	0h RO	**Reserved_9_8 (Reserved_9_8)**
7	0h RO	**DWC_USB3_EN_FPGA_7 (DWC_USB3_EN_FPGA_7)**
6	0h RO	**Reserved1_6 (Reserved1_6)**
5:0	20h RO	**DWC_USB3_PSQ_FIFO_DEPTH_5_0 (DWC_USB3_PSQ_FIFO_DEPTH_5_0)**

19.5.24 GHWPARAMS7 (GHWPARAMS7)—Offset C15Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 38507E6h

Bit Range	Default & Access	Field Name (ID): Description
31:16	385h RO	**DWC_USB3_RAM2_DEPTH_31_16 (DWC_USB3_RAM2_DEPTH_31_16)**
15:0	7E6h RO	**DWC_USB3_RAM1_DEPTH_15_0 (DWC_USB3_RAM1_DEPTH_15_0)**

19.5.25 GDBGFIFOSPACE (GDBGFIFOSPACE)—Offset C160h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 420000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	42h RO	**SPACE_AVAILABLE (SPACE_AVAILABLE)**
15:8	0h RO	**reserved_16_8 (reserved_16_8)**
7:0	0h RW	**FIFO_QUEUE_SELECT (FIFO_QUEUE_SELECT)**

19.5.26 GDBGLTSSM (GDBGLTSSM)—Offset C164h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1010440h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**reserved_32_30 (reserved_32_30)**
29	0h RO	**X3_XS_SWAPPING (X3_XS_SWAPPING)**
28	0h RO	**X3_DS_HOST_SHUTDOWN (X3_DS_HOST_SHUTDOWN)**
27	0h RO	**PRTDIRECTION (PRTDIRECTION)**
26	0h RO	**LTDBTIMEOUT (LTDBTIMEOUT)**
25:22	4h RO	**LTDBLINKSTATE (LTDBLINKSTATE)**
21:18	0h RO	**LTDBSUBSTATE (LTDBSUBSTATE)**
17	0h RO	**ELASTICBUFFERMODE (ELASTICBUFFERMODE)**
16	1h RO	**TXELECLDLE (TXELECLDLE)**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**RXPOLARITY (RXPOLARITY)**
14	0h RO	**TxDetRxLoopback (TxDetRxLoopback)**
13:11	0h RO	**LTDBPhyCmdState (LTDBPhyCmdState)**
10:9	2h RO	**POWERDOWN (POWERDOWN)**
8	0h RO	**RXEQTRAIN (RXEQTRAIN)**
7:6	1h RO	**TXDEEMPHASIS (TXDEEMPHASIS)**
5:3	0h RO	**LTDBClkState (LTDBClkState)**
2	0h RO	**TXSWING (TXSWING)**
1	0h RO	**RXTERMINATION (RXTERMINATION)**
0	0h RO	**TXONESZEROS (TXONESZEROS)**

19.5.27 GDBGLNMCC (GDBGLNMCC)—Offset C168h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Reserved_31_31 (Reserved_31_31)**
30:9	0h RO	**reserved_31_9 (reserved_31_9)**
8:0	0h RO	**LNMCC_BERC (LNMCC_BERC)**

19.5.28 GDBGBMU (GDBGBMU)—Offset C16Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**BMU_BCU (BMU_BCU)**
7:4	0h RO	**BMU_DCU (BMU_DCU)**
3:0	0h RO	**BMU_CCU (BMU_CCU)**

19.5.29 GDBGLSPMUX_DEV (GDBGLSPMUX_DEV)—Offset C170h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3F0000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**reserved_32_24 (reserved_32_24)**
23:16	3Fh RW	**logic_analyzer_trace (logic_analyzer_trace)**
15:14	0h RW	**reserved_16_14 (reserved_16_14)**
13:8	0h RW	**HOSTSELECT (HOSTSELECT)**
7:4	0h RW	**DEVSELECT (DEVSELECT)**
3:0	0h RW	**EPSELECT (EPSELECT)**

19.5.30 GDBGLSP (GDBGLSP)—Offset C174h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**LSPDEBUG (LSPDEBUG)**

19.5.31 GDBGEPINFO0 (GDBGEPINFO0)—Offset C178h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EPDEBUG (EPDEBUG)**

19.5.32 GDBGEPINFO1 (GDBGEPINFO1)—Offset C17Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 800000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	800000h RO	**EPDEBUG (EPDEBUG)**

19.5.33 GPRTBIMAP_HSLO (GPRTBIMAP_HSLO)—Offset C180h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**BINUM8 (BINUM8)**
27:24	0h RO	**BINUM7 (BINUM7)**
23:20	0h RO	**BINUM6 (BINUM6)**
19:16	0h RO	**BINUM5 (BINUM5)**
15:12	0h RO	**BINUM4 (BINUM4)**
11:8	0h RO	**BINUM3 (BINUM3)**
7:4	0h RO	**BINUM2 (BINUM2)**
3:0	0h RW	**BINUM1 (BINUM1)**

19.5.34 GPRTBIMAP_HSHI (GPRTBIMAP_HSHI)—Offset C184h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**reserved_32_28 (reserved_32_28)**
27:24	0h RO	**BINUM15 (BINUM15)**
23:20	0h RO	**BINUM14 (BINUM14)**
19:16	0h RO	**BINUM13 (BINUM13)**
15:12	0h RO	**BINUM12 (BINUM12)**
11:8	0h RO	**BINUM11 (BINUM11)**
7:4	0h RO	**BINUM10 (BINUM10)**
3:0	0h RO	**BINUM9 (BINUM9)**

19.5.35 GPRTBIMAP_FSLO (GPRTBIMAP_FSLO)—Offset C188h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**BINUM8 (BINUM8)**
27:24	0h RO	**BINUM7 (BINUM7)**
23:20	0h RO	**BINUM6 (BINUM6)**
19:16	0h RO	**BINUM5 (BINUM5)**
15:12	0h RO	**BINUM4 (BINUM4)**
11:8	0h RO	**BINUM3 (BINUM3)**
7:4	0h RO	**BINUM2 (BINUM2)**
3:0	0h RW	**BINUM1 (BINUM1)**

19.5.36 GPRTBIMAP_FSHI (GPRTBIMAP_FSHI)—Offset C18Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**reserved_32_28 (reserved_32_28)**
27:24	0h RO	**BINUM15 (BINUM15)**
23:20	0h RO	**BINUM14 (BINUM14)**
19:16	0h RO	**BINUM13 (BINUM13)**

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**BINUM12 (BINUM12)**
11:8	0h RO	**BINUM11 (BINUM11)**
7:4	0h RO	**BINUM10 (BINUM10)**
3:0	0h RO	**BINUM9 (BINUM9)**

19.5.37 GUSB2PHYCFG_0 (GUSB2PHYCFG_0)—Offset C200h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2400h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**PHYSOFTRST (PHYSOFTRST)**
30	0h RW	**U2_FREECLK_EXISTS (U2_FREECLK_EXISTS)**
29	0h RW	**ULPI_LPM_WITH_OPMODE_CHK (ULPI_LPM_WITH_OPMODE_CHK)**
28:27	0h RW	**RSVD**
26	0h RW	**RSVD**
25:19	0h RO	**reserved_25_19 (reserved_25_19)**
18	0h RW	**ULPIEXTVBUSINDIACTOR (ULPIEXTVBUSINDIACTOR)**
17	0h RW	**ULPIEXTVBUSDRV (ULPIEXTVBUSDRV)**
16	0h RW	**ULPICLKSUSM (ULPICLKSUSM)**
15	0h RW	**ULPIAUTORES (ULPIAUTORES)**
14	0h RO	**reserved_15_14 (reserved_15_14)**
13:10	9h RW	**USBTRDTIM (USBTRDTIM)**
9	0h RW	**XCVRDLY (XCVRDLY)**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**ENBLSLPM (ENBLSLPM)**
7	0h WO	**PHYSEL (PHYSEL)**
6	0h RW	**SUSPENDUSB20 (SUSPENDUSB20)**
5	0h RO	**FSINTF (FSINTF)**
4	0h RO	**ULPI_UTMI_Sel (ULPI_UTMI_Sel)**
3	0h RW	**PHYIF (PHYIF)**
2:0	0h RW	**B1L (B1L)**

19.5.38 GUSB2I2CCTL_0 (GUSB2I2CCTL_0)—Offset C240h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**reserved_32_0 (reserved_32_0)**

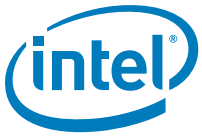
19.5.39 GUSB2PHYACC_ULPI_0 (GUSB2PHYACC_ULPI_0)—Offset C280h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**reserved_32_27 (reserved_32_27)**
26	0h RO	**DISUIPIDRVR (DISUIPIDRVR)**



Bit Range	Default & Access	Field Name (ID): Description
25	0h RO	**NEWREGREQ (NEWREGREQ)**
24	0h RO	**VSTSDONE (VSTSDONE)**
23	0h RO	**VSTSBSY (VSTSBSY)**
22	0h RO	**REGWR (REGWR)**
21:16	0h RO	**REGADDR (REGADDR)**
15:13	0h RW	**Reserved_13_15 (Reserved_13_15)**
12:8	0h RO	**EXTREGADDR (EXTREGADDR)**
7:0	0h RO	**REGDATA (REGDATA)**

19.5.40 GUSB3PIPECTL_0 (GUSB3PIPECTL_0)—Offset C2C0h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2020002h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**PHYSoftRst (PHYSoftRst)**
30	0h RW	**HstPrtCmpl (HstPrtCmpl)**
29	0h RW	**U2SSInactP3ok (U2SSInactP3ok)**
28	0h RW	**DisRxDetP3 (DisRxDetP3)**
27	0h RW	**Ux_exit_in_Px (Ux_exit_in_Px)**
26	0h RW	**ping_enhancement_en (ping_enhancement_en)**
25	1h RW	**u1u2exitfail_to_recov (u1u2exitfail_to_recov)**
24	0h RW	**request_p1p2p3 (request_p1p2p3)**
23	0h RW	**StartRxDetU3RxDet (StartRxDetU3RxDet)**

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW	**DisRxDetU3RxDet (DisRxDetU3RxDet)**
21:19	0h RW	**DelayP1P2P3 (DelayP1P2P3)**
18	0h RW	**DELAYP1TRANS (DELAYP1TRANS)**
17	1h RW	**SUSPENDENABLE (SUSPENDENABLE)**
16:15	0h RO	**DATWIDTH (DATWIDTH)**
14	0h RW	**AbortRxDetInU2 (AbortRxDetInU2)**
13	0h RW	**SkipRxDet (SkipRxDet)**
12	0h RW	**LFPSP0Algn (LFPSP0Algn)**
11	0h RW	**P3P2TranOK (P3P2TranOK)**
10	0h RW	**P3ExSigP2 (P3ExSigP2)**
9	0h RW	**LFPSFILTER (LFPSFILTER)**
8	0h RW	**RX_DETECT_to_Polling_LFPS_Control (RX_DETECT_to_Polling_LFPS_Control)**
7	0h RW	**RSVD**
6	0h RW	**TX_SWING (TX_SWING)**
5:3	0h RW	**TX_MARGIN (TX_MARGIN)**
2:1	1h RW	**TX_DE_EPPHASIS (TX_DE_EPPHASIS)**
0	0h RW	**ELASTIC_BUFFER_MODE (ELASTIC_BUFFER_MODE)**

19.5.41 GTXFIFOSIZ0_0 (GTXFIFOSIZ0_0)—Offset C300h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 42h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	42h RW	**TXFDEP_N (TXFDEP_N)**

19.5.42 GTXFIFOSIZ1_0 (GTXFIFOSIZ1_0)—Offset C304h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 420184h

Bit Range	Default & Access	Field Name (ID): Description
31:16	42h RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	184h RW	**TXFDEP_N (TXFDEP_N)**

19.5.43 GTXFIFOSIZ2_0 (GTXFIFOSIZ2_0)—Offset C308h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1C60184h

Bit Range	Default & Access	Field Name (ID): Description
31:16	1C6h RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	184h RW	**TXFDEP_N (TXFDEP_N)**

19.5.44 GTXFIFOSIZ3_0 (GTXFIFOSIZ3_0)—Offset C30Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 34A0184h

Bit Range	Default & Access	Field Name (ID): Description
31:16	34Ah RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	184h RW	**TXFDEP_N (TXFDEP_N)**

19.5.45 GTXFIFOSIZ4_0 (GTXFIFOSIZ4_0)—Offset C310h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 4CE0082h

Bit Range	Default & Access	Field Name (ID): Description
31:16	4CEh RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	82h RW	**TXFDEP_N (TXFDEP_N)**

19.5.46 GTXFIFOSIZ5_0 (GTXFIFOSIZ5_0)—Offset C314h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 5500082h

Bit Range	Default & Access	Field Name (ID): Description
31:16	550h RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	82h RW	**TXFDEP_N (TXFDEP_N)**

19.5.47 GTXFIFOSIZ6_0 (GTXFIFOSIZ6_0)—Offset C318h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 5D20082h

Bit Range	Default & Access	Field Name (ID): Description
31:16	5D2h RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	82h RW	**TXFDEP_N (TXFDEP_N)**

19.5.48 GTXFIFOSIZ7_0 (GTXFIFOSIZ7_0)—Offset C31Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6540082h

Bit Range	Default & Access	Field Name (ID): Description
31:16	654h RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	82h RW	**TXFDEP_N (TXFDEP_N)**

19.5.49 GTXFIFOSIZ8_0 (GTXFIFOSIZ8_0)—Offset C320h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6D60022h

Bit Range	Default & Access	Field Name (ID): Description
31:16	6D6h RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	22h RW	**TXFDEP_N (TXFDEP_N)**

19.5.50 GTXFIFOSIZ9_0 (GTXFIFOSIZ9_0)—Offset C324h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 6F80022h

Bit Range	Default & Access	Field Name (ID): Description
31:16	6F8h RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	22h RW	**TXFDEP_N (TXFDEP_N)**

19.5.51 GTXFIFOSIZ10_0 (GTXFIFOSIZ10_0)—Offset C328h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 71A0022h

Bit Range	Default & Access	Field Name (ID): Description
31:16	71Ah RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	22h RW	**TXFDEP_N (TXFDEP_N)**

19.5.52 GTXFIFOSIZ11_0 (GTXFIFOSIZ11_0)—Offset C32Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 73C0022h

Bit Range	Default & Access	Field Name (ID): Description
31:16	73Ch RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	22h RW	**TXFDEP_N (TXFDEP_N)**

19.5.53 GTXFIFOSIZ12_0 (GTXFIFOSIZ12_0)—Offset C330h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 75E0022h

Bit Range	Default & Access	Field Name (ID): Description
31:16	75Eh RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	22h RW	**TXFDEP_N (TXFDEP_N)**

19.5.54 GTXFIFOSIZ13_0 (GTXFIFOSIZ13_0)—Offset C334h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 7800022h

Bit Range	Default & Access	Field Name (ID): Description
31:16	780h RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	22h RW	**TXFDEP_N (TXFDEP_N)**

19.5.55 GTXFIFOSIZ14_0 (GTXFIFOSIZ14_0)—Offset C338h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 7A20022h

Bit Range	Default & Access	Field Name (ID): Description
31:16	7A2h RW	**TXFSTADDR_N (TXFSTADDR_N)**

Bit Range	Default & Access	Field Name (ID): Description
15:0	22h RW	**TXFDEP_N (TXFDEP_N)**

19.5.56 GTXFIFOSIZ15_0 (GTXFIFOSIZ15_0)—Offset C33Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 7C40022h

Bit Range	Default & Access	Field Name (ID): Description
31:16	7C4h RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	22h RW	**TXFDEP_N (TXFDEP_N)**

19.5.57 GRXFIFOSIZ0_0 (GRXFIFOSIZ0_0)—Offset C380h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 385h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**RXFSTADDR_N (RXFSTADDR_N)**
15:0	385h RW	**RXFDEP_N (RXFDEP_N)**

19.5.58 GEVNTADRLO_0 (GEVNTADRLO_0)—Offset C400h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**EVNTADRLO (EVNTADRLO)**

19.5.59 GEVNTADRHI_0 (GEVNTADRHI_0)—Offset C404h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**EVNTADRHI (EVNTADRHI)**

19.5.60 GEVNTSIZ_0 (GEVNTSIZ_0)—Offset C408h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**EVNTINTRPTMASK (EVNTINTRPTMASK)**
30:16	0h RO	**reserved_31_16 (reserved_31_16)**
15:0	0h RW	**EVENTSIZ (EVENTSIZ)**

19.5.61 GEVNTCOUNT_0 (GEVNTCOUNT_0)—Offset C40Ch

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**reserved_32_16 (reserved_32_16)**
15:0	0h NA	**EVNTCOUNT (EVNTCOUNT)**

19.5.62 GHWPARAMS8 (GHWPARAMS8)—Offset C600h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 2F6h

Bit Range	Default & Access	Field Name (ID): Description
31:0	2F6h RO	**DWC_USB3_DCACHE_DEPTH_INFO_32_0 (DWC_USB3_DCACHE_DEPTH_INFO_32_0)**

19.5.63 GTXFIFOPRIDEV (GTXFIFOPRIDEV)—Offset C610h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**reserved_32_16 (reserved_32_16)**
15:0	0h RW	**gtxfifopridev (gtxfifopridev)**

19.5.64 GFLADJ (GFLADJ)—Offset C630h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**GFLADJ_REFCLK_240MHZDECR_PLS1 (GFLADJ_REFCLK_240MHZDECR_PLS1)**
30:24	0h RW	**GFLADJ_REFCLK_240MHZ_DECR (GFLADJ_REFCLK_240MHZ_DECR)**
23	0h RW	**GFLADJ_REFCLK_LPM_SEL (GFLADJ_REFCLK_LPM_SEL)**
22	0h RW	**reserved_22 (reserved_22)**
21:8	0h RW	**GFLADJ_REFCLK_FLADJ (GFLADJ_REFCLK_FLADJ)**
7	0h RW	**GFLADJ_30MHZ_SDBND_SEL (GFLADJ_30MHZ_SDBND_SEL)**
6	0h RW	**reserved_6 (reserved_6)**
5:0	0h RW	**GFLADJ_30MHZ (GFLADJ_30MHZ)**

19.6 Registers Summary

Table 19-6. Summary of USBX device top Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
10F808h	10F809h	APBFC_U3PMU_CFG0 (APBFC_U3PMU_CFG0)—Offset 10F808h	800h
10F80Ch	10F80Dh	APBFC_U3PMU_CFG1 (APBFC_U3PMU_CFG1)—Offset 10F80Ch	0h
10F810h	10F811h	APBFC_U3PMU_CFG2 (APBFC_U3PMU_CFG2)—Offset 10F810h	Bh
10F814h	10F815h	APBFC_U3PMU_CFG3 (APBFC_U3PMU_CFG3)—Offset 10F814h	1008h
10F818h	10F819h	APBFC_U3PMU_CFG4 (APBFC_U3PMU_CFG4)—Offset 10F818h	0h
10F81Ch	10F81Dh	APBFC_U3PMU_CFG5 (APBFC_U3PMU_CFG5)—Offset 10F81Ch	0h
10F820h	10F821h	APBFC_U3PMU_CFG6 (APBFC_U3PMU_CFG6)—Offset 10F820h	1000h
10F830h	10F831h	APBFC_D0I3C (APBFC_D0I3C)—Offset 10F830h	8h

19.6.1 APBFC_U3PMU_CFG0 (APBFC_U3PMU_CFG0)—Offset 10F808h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**DRD_CONTROL_BIT_15 (DRD_CONTROL_BIT_15)**
14:3	100h RW	**DEBOUNCE_VAL (DEBOUNCE_VAL):** ID ping debounce timer (DEBOUNCE_VAL): in the unit of RTC clock (33us) default to 8.448 ms
2	0h RW	**SYNCHRONIZE_SS_HS_SWITCH (SYNCHRONIZE_SS_HS_SWITCH):** Synchronize the SS and HS switch: 0 (default) Does not synchronize. i.e. HS switch on the debounced id pin, while SS switch independently controlled by the sequencer. 1 synchronize HS and SS switch. Both speeds switch when sequencer switch.
1:0	0h RW	**DRD_CONFIG (DRD_CONFIG):** 00 Dynamic DRD switch mode 01 static host mode 10 static device mode 11 -- reserved

19.6.2 APBFC_U3PMU_CFG1 (APBFC_U3PMU_CFG1)—Offset 10F80Ch

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**XDCI_DRD_CTRL_EN (DRD_CONTROL_BIT_31):** When DRD_ACCESS_MODE (bit 2) =1, 0 -- The policies below is controlled by register in the XHCI MMIO 1 -- The policies below is controlled by register in the XDCI MMIO When DRD_ACCESS_MODE =0, this bit is a don?t care.
14:12	0h RW	**DRD_WDT_VAL (DRD_WDT_VAL):** DRD WDT timer: 0-based incremental of 500ms
11	0h RW	**EN_HOST_TO_DEV_WDT (EN_HOST_TO_DEV_WDT):** enable DRD WDT switch from host to device 0 - disable watchdog timer 1- enable watchdog timer
10	0h RW	**EN_DEV_TO_HOST_WDT (EN_DEV_TO_HOST_WDT):** enable DRD WDT switch from device to host 0 - disable watchdog timer 1- enable watchdog timer
9	0h RW	**EN_RST_WDT (EN_RST_WDT):** enable DRD WDT switch out of cold reset 0 - disable watchdog timer 1- enable watchdog timer
8	0h RW	**SW_VBUS_VALID (SW_VBUS_VALID):** if SW_IDPIN_EN (bit 5) is 1, 0 - deassert sw vbus valid 1 - assert sw vbus valid
7	0h RW	**RSVD1 (RSVD1):** RESERVED

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**EN_PIPE_RX_ON_IDPIN (EN_PIPE_RX_ON_IDPIN):** During the connection to a device, there may be a delay in DRD switch from XDCI to XHCI mode,the rx term can be low after idpin deasserts. If this bit is 0, the rx term will be assert immediately after idpin toggle. Otherwise, the device may fall back to USB2 mode. 1 -- drive 0s on utmi rx signals to controller if not connected.
5	0h RW	**SW_IDPIN_EN (SW_IDPIN_EN):** SW_IDPIN_EN 1 -- enable SW id pin (pre DRD) 0 -- disable SW id pin.
4	0h RW	**SW_IDPIN (SW_IDPIN):** if SW_IDPIN_EN (bit 21) is 1, 0 - host mode 1 - device mode
3	0h RW	**USB2_SUSP_OR_DIS (USB2_SUSP_OR_DIS):** 1 - The DRD UTMI suspendm will be controlled by host/device based on the DRD switch. 0 - whenever device or host deassert suspendm, the DRD UTMI suspendm will be deasserted.
2	0h RW	**DRD_ACCESS_MODE (DRD_ACCESS_MODE):** 0 - The DUAL_ROLE register from host and device are ORed to control DRD 1 - The DUAL_ROLE register from host and device are selected by XDCI_DRD_CTRL_EN (bit 31) to control DRD
1	0h RW	**EN_DIRECT_DRD_SWITCH_ON_USB3PORT_BY_IDPIN (EN_DIRECT_DRD_SWITCH_ON_USB3PORT_BY_IDPIN):** 1 enable the direct DRD switch on USB3 port by idpin 0 disable the direct DRD switch
0	0h RW	**SW_SWITCH_ENABLE (SW_SWITCH_ENABLE):** SW switch enable 0 (default) ID pin HW controlled DRD. 1 -- SW controlled DRD (ignore idpin), switch based on the DRD_CONFIG.

19.6.3 APBFC_U3PMU_CFG2 (APBFC_U3PMU_CFG2)—Offset 10F810h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: Bh

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**ltdb_sub_state_2_0:** USB3 Link sub state[3:0]
12	0h RO	**reserved1**
11:10	0h RO	**current_power_state_u3pmu:** The current power state of the core. When equal to '3', the PMU is controlling the PHY, and when equal to '0', the core is controlling the PHY

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RO	**current_power_state_u2pmu:** The current power state of the core. When equal to '3', the PMU is controlling the PHY, and when equal to '0', the core is controlling the PHY
7	0h RO	**connect_state_u3pmu:** When '1', indicates the PMU is maintaining at least one connection to the host or a device (the link is in U3). When '0', indicates the PMU has no connection to the host or any device.
6	0h RO	**connect_state_u2pmu:** When '1', indicates the PMU is maintaining at least one connection to the host or a device (the link is in L1, L2). When '0', indicates the PMU has no connection to the host or any device
5	0h RO	**utmi_l1_suspend_com_n:** Common L1 suspend
4	0h RO	**utmi_suspend_com_n:** Common suspend
3	1h RO	**utmi_suspend_n:** USB 2.0 Port Suspend
2:1	1h RO	**usb2_enumspeed:** Device Enumerated Speed
0	1h RO	**b2rl_cur_mode:** Current Mode. Current Mode 1'b0 Host ,1'b1 Device

19.6.4 APBFC_U3PMU_CFG3 (APBFC_U3PMU_CFG3)—Offset 10F814h

General Purpose Input Register

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 1008h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**BVALID_HW (HW_BVALID):** hardware bvalid
14	0h RO	**gsts_buserraddvld:** Bus error
13	0h RO	**DRD_MODE (DRD_MODE):** SS DRD mode 0 device mode 1 host mode
12	1h RO	**IDPIN (IDPIN):** IDPIN value (debounce)
11:10	0h RO	**u2_dssr_state:** USB2 DSSR State

Bit Range	Default & Access	Field Name (ID): Description
9:5	0h RO	**u2_prt_state:** USB2 Port State
4:1	4h RO	**ltdb_link_state:** USB3 Link state
0	0h RO	**ltdb_sub_state_3:** USB3 Link sub state[3]

19.6.5 APBFC_U3PMU_CFG4 (APBFC_U3PMU_CFG4)—Offset 10F818h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RW	**hub_port_perm_attach:** reserved
13	0h RW	**host_port_power_control:** reserved
12	0h RW	**xhci_revision:** reserved
11:8	0h RW	**bus_filter_bypass:** Bus Filter Bypass. Disables the internal bus filters that are enabled by DWC_USB3_EN_BUS_FILTERS coreConsultant parameter. This static signal is present only when DWC_USB3_EN_BUS_FILTERS is 1. It is expected that this signal is set or reset at power-on reset and is not changed during the normal operation of the core.
7	0h RW	**Reserved2:** reserved
6	0h RW	**Reserved1:** reserved
5	0h RW	**otg_phy_pwr_off_veto:** reserved
4	0h RW	**otg_cnt_pwr_off_veto:** Indicates that controller power should not power off even on RTD3hot.Also a veto signal to keep LPPLL on. Note: Currently LPPLL results in a veto for S0iX flows
3	0h RW	**Brdg_rst:** reset the core see also regRW1[31]
2	0h RW	**USB2PHY_BVALID_MASK_DIS:** 0: enable USB2 PHY BVALID mask 1: disable

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**pm_power_state_request:** This port defines the PCI power management state requested by the software. When the core is configured with two power rail support (DWC_USB3_EN_PWROPT=2), the valid states are: ? 00: D0 ? 11: D3 Active State

19.6.6 APBFC_U3PMU_CFG5 (APBFC_U3PMU_CFG5)—Offset 10F81Ch

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Brdg_rst_mux:** This is a mux the core reset between the normal reset or reset and with bdg_reset regRW1[3]
14	0h RW	**En_otg_interrupt:** reserved
13:8	0h RW	**fladj_30mhz_reg:** HS jitter adjusment
7	0h RW	**core_hub_port_overcurrent:** This is a generic register provided for product specific behavior
6	0h RW	**GEN_REG_RW1:** This is a generic register provided for product specific behavior
5	0h RW	**otg_phy_pwr_off_req:** reserved
4	0h RW	**u2_pme_en:** Determines whether ULPI flis PME events are allowed to trigger PME events to brige/GPIO
3	0h RW	**u3_pme_en:** Determines whether USB3 flis PME events are allowed to trigger PME events to brige/GPIO
2	0h RW	**core_pme_en:** Determines whether core PME events are allowed to trigger PME events to brige/GPIO
1	0h RW	**ulpiphy_refclk_disable:** reserved
0	0h RW	**ipma_cmn_refclk_disable:** reserved

19.6.7 APBFC_U3PMU_CFG6 (APBFC_U3PMU_CFG6)—Offset 10F820h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 1000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**HW_BVALID_DEV:** HW Vbus Bvalid indication
14	0h RO	**RESERVED (RSVD2)**
13	0h RO	**HOST_OWNED_DEV:** DRD mode,0 is device mode 1 is host mode
12	1h RO	**IDPIN_DEV:** ID pin Debounced version
11:0	0h RO	**RESERVED (RSVD3)**

19.6.8 APBFC_D0I3C (APBFC_D0I3C)—Offset 10F830h

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RW	**RESERVED (RSVD)**
3	1h RW/1C	**RestoreRequired (RESTORE_REQUIRED):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0I3 (D0I3):** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1:0	0h RW	**RESERVED (RSVD1)**

19.7 Registers Summary

Table 19-7. Summary of USBX device top Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
B0h	B3h	(GEN_REGRW1)—Offset B0h	0h
B4h	B7h	(GEN_REGRW2)—Offset B4h	0h

Table 19-7. Summary of USBX device top Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
B8h	BBh	(GEN_REGRW3)—Offset B8h	0h
BCh	BFh	(GEN_REGRW4)—Offset BCh	0h
C0h	C3h	(GEN_INPUT_REGRW)—Offset C0h	1008000Bh

19.7.1 (GEN_REGRW1)—Offset B0h

General Purpose Read Write Register1

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW1**

19.7.2 (GEN_REGRW2)—Offset B4h

General Purpose Read Write Register2

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW2**

19.7.3 (GEN_REGRW3)—Offset B8h

General Purpose Read Write Register3

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW3**

19.7.4 (GEN_REGRW4)—Offset BCh

General Purpose Read Write Register4

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW	**GEN_REG_RW4:** reserved
2	0h RW	**XDCI_PIPE_CLK_GATE_DIS:** xdci pipe clock gating disable
1	0h RW	**XDCI_SB_CLK_GATE_DIS:** xdci sideband clock gating disable
0	0h RW	**XDCI_PRIM_CLK_GATE_DIS:** xdci primary clock gating disable

19.7.5 (GEN_INPUT_REGRW)—Offset C0h

General Purpose Input Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 1008000Bh

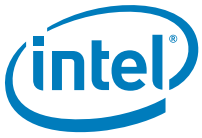
Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**BVALID_HW (HW_BVALID):** hardware bvalid
30	0h RO	**gsts_buserraddvld:** Bus error
29	0h RO	**DRD_MODE (DRD_MODE):** SS DRD mode 0 device mode 1 host mode
28	1h RO	**IDPIN (IDPIN):** IDPIN value (debounce)
27:26	0h RO	**u2_dssr_state:** USB2 DSSR State

Bit Range	Default & Access	Field Name (ID): Description
25:21	0h RO	**u2_prt_state:** USB2 Port State
20:17	4h RO	**ltdb_link_state:** USB3 Link state
16:13	0h RO	**ltdb_sub_state:** USB3 Link sub state
12	0h RO	**reserved1**
11:10	0h RO	**current_power_state_u3pmu:** The current power state of the core. When equal to '3', the PMU is controlling the PHY, and when equal to '0', the core is controlling the PHY
9:8	0h RO	**current_power_state_u2pmu:** The current power state of the core. When equal to '3', the PMU is controlling the PHY, and when equal to '0', the core is controlling the PHY
7	0h RO	**connect_state_u3pmu:** When '1', indicates the PMU is maintaining at least one connection to the host or a device (the link is in U3). When '0', indicates the PMU has no connection to the host or any device.
6	0h RO	**connect_state_u2pmu:** When '1', indicates the PMU is maintaining at least one connection to the host or a device (the link is in L1, L2). When '0', indicates the PMU has no connection to the host or any device
5	0h RO	**utmi_l1_suspend_com_n:** Common L1 suspend
4	0h RO	**utmi_suspend_com_n:** Common suspend
3	1h RO	**utmi_suspend_n:** USB 2.0 Port Suspend
2:1	1h RO	**usb2_enumspeed:** Device Enumerated Speed
0	1h RO	**b2rl_cur_mode:** Current Mode. Current Mode 1'b0 Host ,1'b1 Device

19.8 Registers Summary

Table 19-8. Summary of USBX device top Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
B0h	B3h	(GEN_REGRW1)—Offset B0h	0h
B4h	B7h	(GEN_REGRW2)—Offset B4h	0h
B8h	BBh	(GEN_REGRW3)—Offset B8h	0h
BCh	BFh	(GEN_REGRW4)—Offset BCh	0h
C0h	C3h	(GEN_INPUT_REGRW)—Offset C0h	1008000Bh



19.8.1 (GEN_REGRW1)—Offset B0h

General Purpose Read Write Register1

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW1**

19.8.2 (GEN_REGRW2)—Offset B4h

General Purpose Read Write Register2

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW2**

19.8.3 (GEN_REGRW3)—Offset B8h

General Purpose Read Write Register3

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW3**

19.8.4 (GEN_REGRW4)—Offset BCh

General Purpose Read Write Register4

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW	**GEN_REG_RW4:** reserved
2	0h RW	**XDCI_PIPE_CLK_GATE_DIS:** xdci pipe clock gating disable
1	0h RW	**XDCI_SB_CLK_GATE_DIS:** xdci sideband clock gating disable
0	0h RW	**XDCI_PRIM_CLK_GATE_DIS:** xdci primary clock gating disable

19.8.5 (GEN_INPUT_REGRW)—Offset C0h

General Purpose Input Register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1008000Bh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**BVALID_HW (HW_BVALID):** hardware bvalid
30	0h RO	**gsts_buserraddvld:** Bus error
29	0h RO	**DRD_MODE (DRD_MODE):** SS DRD mode 0 device mode 1 host mode
28	1h RO	**IDPIN (IDPIN):** IDPIN value (debounce)
27:26	0h RO	**u2_dssr_state:** USB2 DSSR State
25:21	0h RO	**u2_prt_state:** USB2 Port State
20:17	4h RO	**ltdb_link_state:** USB3 Link state
16:13	0h RO	**ltdb_sub_state:** USB3 Link sub state
12	0h RO	**reserved1**

Bit Range	Default & Access	Field Name (ID): Description
11:10	0h RO	**current_power_state_u3pmu:** The current power state of the core. When equal to '3', the PMU is controlling the PHY, and when equal to '0', the core is controlling the PHY
9:8	0h RO	**current_power_state_u2pmu:** The current power state of the core. When equal to '3', the PMU is controlling the PHY, and when equal to '0', the core is controlling the PHY
7	0h RO	**connect_state_u3pmu:** When '1', indicates the PMU is maintaining at least one connection to the host or a device (the link is in U3). When '0', indicates the PMU has no connection to the host or any device.
6	0h RO	**connect_state_u2pmu:** When '1', indicates the PMU is maintaining at least one connection to the host or a device (the link is in L1, L2). When '0', indicates the PMU has no connection to the host or any device
5	0h RO	**utmi_l1_suspend_com_n:** Common L1 suspend
4	0h RO	**utmi_suspend_com_n:** Common suspend
3	1h RO	**utmi_suspend_n:** USB 2.0 Port Suspend
2:1	1h RO	**usb2_enumspeed:** Device Enumerated Speed
0	1h RO	**b2rl_cur_mode:** Current Mode. Current Mode 1'b0 Host ,1'b1 Device

19.9 Registers Summary

Table 19-9. Summary of USBX device top Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	(DEVVENDID)—Offset 0h	8086h
4h	7h	(STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	(REVCLASSCODE)—Offset 8h	C03FE00h
Ch	Fh	(CLLATHEADERBIST)—Offset Ch	0h
10h	17h	(BAR)—Offset 10h	4h
18h	1Fh	(BAR1)—Offset 18h	4h
2Ch	2Fh	(SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	(EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	(CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	(INTERRUPTREG)—Offset 3Ch	100h
80h	83h	(POWERCAPID)—Offset 80h	48039001h
84h	87h	(PMECTRLSTATUS)—Offset 84h	8h
90h	93h	(PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	(DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h

Table 19-9. Summary of USBX device top Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
98h	9Bh	(D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	(DEVICE_IDLE_POINTER_REG)—Offset 9Ch	10F8301h
A0h	A3h	(D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	80800h

19.9.1 (DEVVENDID)—Offset 0h

DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**DEVICEID**
15:0	8086h RO	**VENDORID**

19.9.2 (STATUSCOMMAND)—Offset 4h

STATUSCOMMAND- Status and Command

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0**
29	0h RW/1C	**RMA**
28	0h RW/1C	**RTA**
27:21	0h RO	**Reserved1**
20	1h RO	**CAPLIST**
19	0h RO	**INTR_STATUS**

Bit Range	Default & Access	Field Name (ID): Description
18:16	0h RO	**Reserved2**
15:11	0h RO	**Reserved3**
10	0h RW	**INTR_DISABLE**
9	0h RO	**Reserved4**
8	0h RW	**SERR_ENABLE**
7:3	0h RO	**Reserved5**
2	0h RW	**BME**
1	0h RW	**MSE**
0	0h RO	**Reserved6**

19.9.3 (REVCLASSCODE)—Offset 8h

REVCLASSCODE - Revision ID and Class Code

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: C03FE00h

Bit Range	Default & Access	Field Name (ID): Description
31:8	C03FEh RO	**CLASS_CODES**
7:0	0h RO	**RID**

19.9.4 (CLLATHEADERBIST)—Offset Ch

CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved0**
23	0h RO	**MULFNDEV**
22:16	0h RO	**HEADERTYPE**
15:8	0h RO	**LATTIMER**
7:0	0h RW	**CACHELINE_SIZE**

19.9.5 (BAR)—Offset 10h

BAR -Base Address Register

Access Method

Type: CFG Register (Size: 64 bits)	**Device:** 21 **Function:** 1

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
63:21	0h RW	**BASEADDR**
20:12	0h RO	**RSVD**
11:4	0h RO	**SIZEINDICATOR**
3	0h RO	**PREFETCHABLE**
2:1	2h RO	**TYPE**
0	0h RO	**MESSAGE_SPACE**

19.9.6 (BAR1)—Offset 18h

BAR1 -Base Address Register1

Access Method

Type: CFG Register (Size: 64 bits)	**Device:** 21 **Function:** 1

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RW	**BASEADDR1_HIGH**
31:12	0h RW	**BASEADDR1**
11:4	0h RO	**SIZEINDICATOR1**
3	0h RO	**PREFETCHABLE1**
2:1	2h RO	**TYPE1**
0	0h RO	**MESSAGE_SPACE1**

19.9.7 (SUBSYSTEMID)—Offset 2Ch

SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID**
15:0	0h RW/O	**SUBSYSTEMVENDORID**

19.9.8 (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE**

19.9.9 (CAPABILITYPTR)—Offset 34h

CAPABILITYPTR - Capabilities Pointer

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved0**
7:0	80h RO	**CAPPTR_POWER**

19.9.10 (INTERRUPTREG)—Offset 3Ch

INTERRUPTREG - Interrupt Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT**
23:16	0h RO	**MIN_GNT**
15:12	0h RO	**Reserved0**
11:8	1h RO	**INTPIN**
7:0	0h RW	**INTLINE**

19.9.11 (POWERCAPID)—Offset 80h

POWERCAPID - PowerManagement Capability ID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 48039001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	9h RO	**PMESUPPORT**
26:19	0h RO	**Reserved0**
18:16	3h RO	**VERSION**
15:8	90h RO	**NXTCAP**
7:0	1h RO	**POWER_CAP**

19.9.12 (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved0**
15	0h RW/1C	**PMESTATUS**
14:9	0h RO	**Reserved1**
8	0h RW	**PMEENABLE**
7:4	0h RO	**Reserved2**
3	1h RO	**NO_SOFT_RESET**
2	0h RO	**Reserved3**
1:0	0h RW	**POWERSTATE**

19.9.13 (PCIDEVIDLE_CAP_RECORD)—Offset 90h

PCI DEVICE IDLE CAPABILITY RECORD

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP**
27:24	0h RO	**REVID**
23:16	14h RO	**CAP_LENGTH**
15:8	0h RO	**NEXT_CAP**
7:0	9h RO	**CAPID**

19.9.14 (DEVID_VEND_SPECIFIC_REG)—Offset 94h

DEVID VENDOR SPECIFIC REG

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH**
19:16	0h RO	**VSEC_REV**
15:0	10h RO	**VSECID**

19.9.15 (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

SW LTR Update MMIO Location Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW_LAT_DWORD_OFFSET**
3:1	0h RO	**SW_LAT_BAR_NUM**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**SW_LAT_VALID**

19.9.16 (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 10F8301h

Bit Range	Default & Access	Field Name (ID): Description
31:4	10F830h RO	**DWORD_OFFSET**
3:1	0h RO	**BAR_NUM**
0	1h RO	**VALID**

19.9.17 (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

DEVICE PG CONFIG

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 21 **Function:** 1

Default: 80800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved0**
21	0h RW	**HAE**
20	0h RO	**Reserved1**
19	1h RW	**SLEEP_EN**
18	0h RW	**PGE**
17	0h RW	**I3_ENABLE**

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**D3_ENABLE**
15:13	0h RO	**Reserved2**
12:10	2h RW/O	**POW_LAT_SCALE**
9:0	0h RW/O	**POW_LAT_VALUE**

19.10 Registers Summary

Table 19-10. Summary of USBX device top Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	(DEVVENDID)—Offset 0h	8086h
4h	7h	(STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	(REVCLASSCODE)—Offset 8h	C03FE00h
Ch	Fh	(CLLATHEADERBIST)—Offset Ch	0h
10h	17h	(BAR)—Offset 10h	4h
18h	1Fh	(BAR1)—Offset 18h	4h
2Ch	2Fh	(SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	(EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	(CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	(INTERRUPTREG)—Offset 3Ch	100h
80h	83h	(POWERCAPID)—Offset 80h	48039001h
84h	87h	(PMECTRLSTATUS)—Offset 84h	8h
90h	93h	(PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	(DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	(D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	(DEVICE_IDLE_POINTER_REG)—Offset 9Ch	10F8301h
A0h	A3h	(D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	80800h

19.10.1 (DEVVENDID)—Offset 0h

DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**DEVICEID**
15:0	8086h RO	**VENDORID**

19.10.2 (STATUSCOMMAND)—Offset 4h

STATUSCOMMAND- Status and Command

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0**
29	0h RW/1C	**RMA**
28	0h RW/1C	**RTA**
27:21	0h RO	**Reserved1**
20	1h RO	**CAPLIST**
19	0h RO	**INTR_STATUS**
18:16	0h RO	**Reserved2**
15:11	0h RO	**Reserved3**
10	0h RW	**INTR_DISABLE**
9	0h RO	**Reserved4**
8	0h RW	**SERR_ENABLE**
7:3	0h RO	**Reserved5**
2	0h RW	**BME**
1	0h RW	**MSE**
0	0h RO	**Reserved6**

19.10.3 (REVCLASSCODE)—Offset 8h

REVCLASSCODE - Revision ID and Class Code

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: C03FE00h

Bit Range	Default & Access	Field Name (ID): Description
31:8	C03FEh RO	**CLASS_CODES**
7:0	0h RO	**RID**

19.10.4 (CLLATHEADERBIST)—Offset Ch

CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved0**
23	0h RO	**MULFNDEV**
22:16	0h RO	**HEADERTYPE**
15:8	0h RO	**LATTIMER**
7:0	0h RW	**CACHELINE_SIZE**

19.10.5 (BAR)—Offset 10h

BAR -Base Address Register

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
63:21	0h RW	**BASEADDR**
20:12	0h RO	**RSVD**
11:4	0h RO	**SIZEINDICATOR**
3	0h RO	**PREFETCHABLE**
2:1	2h RO	**TYPE**
0	0h RO	**MESSAGE_SPACE**

19.10.6 (BAR1)—Offset 18h

BAR1 -Base Address Register1

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RW	**BASEADDR1_HIGH**
31:12	0h RW	**BASEADDR1**
11:4	0h RO	**SIZEINDICATOR1**
3	0h RO	**PREFETCHABLE1**
2:1	2h RO	**TYPE1**
0	0h RO	**MESSAGE_SPACE1**

19.10.7 (SUBSYSTEMID)—Offset 2Ch

SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID**
15:0	0h RW/O	**SUBSYSTEMVENDORID**

19.10.8 (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE**

19.10.9 (CAPABILITYPTR)—Offset 34h

CAPABILITYPTR - Capabilities Pointer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved0**
7:0	80h RO	**CAPPTR_POWER**

19.10.10 (INTERRUPTREG)—Offset 3Ch

INTERRUPTREG - Interrupt Register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT**
23:16	0h RO	**MIN_GNT**
15:12	0h RO	**Reserved0**
11:8	1h RO	**INTPIN**
7:0	0h RW	**INTLINE**

19.10.11 (POWERCAPID)—Offset 80h

POWERCAPID - PowerManagement Capability ID

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 48039001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	9h RO	**PMESUPPORT**
26:19	0h RO	**Reserved0**
18:16	3h RO	**VERSION**
15:8	90h RO	**NXTCAP**
7:0	1h RO	**POWER_CAP**

19.10.12 (PMECTRLSTATUS)—Offset 84h

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved0**

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PMESTATUS**
14:9	0h RO	**Reserved1**
8	0h RW	**PMEENABLE**
7:4	0h RO	**Reserved2**
3	1h RO	**NO_SOFT_RESET**
2	0h RO	**Reserved3**
1:0	0h RW	**POWERSTATE**

19.10.13 (PCIDEVIDLE_CAP_RECORD)—Offset 90h

PCI DEVICE IDLE CAPABILITY RECORD

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP**
27:24	0h RO	**REVID**
23:16	14h RO	**CAP_LENGTH**
15:8	0h RO	**NEXT_CAP**
7:0	9h RO	**CAPID**

19.10.14 (DEVID_VEND_SPECIFIC_REG)—Offset 94h

DEVID VENDOR SPECIFIC REG

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH**
19:16	0h RO	**VSEC_REV**
15:0	10h RO	**VSECID**

19.10.15 (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

SW LTR Update MMIO Location Register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW_LAT_DWORD_OFFSET**
3:1	0h RO	**SW_LAT_BAR_NUM**
0	0h RO	**SW_LAT_VALID**

19.10.16 (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 10F8301h

Bit Range	Default & Access	Field Name (ID): Description
31:4	10F830h RO	**DWORD_OFFSET**
3:1	0h RO	**BAR_NUM**
0	1h RO	**VALID**

19.10.17 (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

DEVICE PG CONFIG

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 80800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved0**
21	0h RW	**HAE**
20	0h RO	**Reserved1**
19	1h RW	**SLEEP_EN**
18	0h RW	**PGE**
17	0h RW	**I3_ENABLE**
16	0h RW	**D3_ENABLE**
15:13	0h RO	**Reserved2**
12:10	2h RW/O	**POW_LAT_SCALE**
9:0	0h RW/O	**POW_LAT_VALUE**

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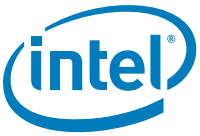


20 Storage

20.1 Registers Summary

Table 20-1. Summary of CONVERGE_LAYER Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
804h	807h	(SW_LTR_val)—Offset 804h	800h
808h	80Bh	(Auto_LTR_val)—Offset 808h	800h
810h	813h	(Cap_byps)—Offset 810h	0h
814h	817h	(Cap_byps_reg1)—Offset 814h	3041EF3Ch
818h	81Bh	(Cap_byps_reg2)—Offset 818h	40040C8h
81Ch	81Fh	(reg_D0i3)—Offset 81Ch	8h
820h	823h	(Tx_CMD_dly)—Offset 820h	400h
824h	827h	(Tx_DATA_dly_1)—Offset 824h	A18h
828h	82Bh	(Tx_DATA_dly_2)—Offset 828h	1C1C1C00h
82Ch	82Fh	(Rx_CMD_Data_dly_1)—Offset 82Ch	0h
830h	833h	(Rx_Strobe_Ctrl_Path)—Offset 830h	0h
834h	837h	(Rx_CMD_Data_dly_2)—Offset 834h	0h
838h	83Bh	(Master_Dll)—Offset 838h	1h
840h	843h	(Auto_tuning)—Offset 840h	0h
900h	903h	(emmc_Root_Space)—Offset 900h	0h

20.1.1 (SW_LTR_val)—Offset 804h

Sets the Software Latency Tolerance Reporting fields

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop_Requirement:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
12:10	2h RW	**Snoop_latency_scale:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop_value:** 10-bit latency value

20.1.2 (Auto_LTR_val)—Offset 808h

Sets the Auto Latency Tolerance Reporting fields

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop_Requirement:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	**Reserved_low:** Reserved_low
12:10	2h RW	**Snoop_latency_scale:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop_value:** 10-bit latency value

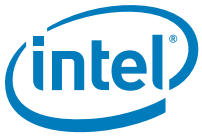
20.1.3 (Cap_byps)—Offset 810h

Capabilities Bypass Control register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**Enable_Cap_Bypass:** 8'h5A - Enable Capabilities Bypass. All other - Capabilities Bypass Disable (using default values)

20.1.4 (Cap_byps_reg1)—Offset 814h

eMMC Capabilities Bypass register 1

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3041EF3Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	1h RW	**hs400_support:** 1: HS400 Mode Supported. 0: HS400 Mode NOT Supported
28	1h RW	**timeout_clock_unit:** 1'b1 - to Select MHz Clock ,1'b0 - to Select KHz Clock
27:22	1h RW	**timeout_clock_freq:** Timeout clock frequency
21	0h RW	**SPI_mode_support:** SPI Mode Support 1'b1 - SPI Mode Supported ,1'b0 - SPI Mode Not Supported
20:17	0h RW	**timer_count:** Timer Count for Re-Tuning This is the Timer Count for Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 4'b0 disables Re-Tuning Timer
16	1h RW	**tuning_for_SDR50:** Use Tuning for SDR50 1'b1 - Use Tuning 1'b0 - Don't use Tuning
15	1h RW	**ddr50_support:** 1: DDR50 Mode Supported. 0: DDR50 Mode NOT Supported
14	1h RW	**sdr104_support:** 1: SDR104 Mode Supported. 0: SDR104 Mode NOT Supported
13	1h RW	**sdr50_support:** 1: SDR50 Mode Supported. 0: SDR50 Mode NOT Supported
12:11	1h RW	**Slot_Type:** 00 - Removable SD Card Slot. 01 - Embedded Slot for One Device. 10 - Shared Bus Slot. 11 - Reserved
10	1h RW	**Async_Interrupt_Support:** 1: Asynchronous Interrupt Supported. 0: Asynchronous Interrupt NOT Supported
9	1h RW	**Sys_Addr_64bit_Support:** 1 - Core supports 64-bit System Address Bus. 0 - Core supports only 32-bit System Address Bus

Bit Range	Default & Access	Field Name (ID): Description
8	1h RW	**Voltage_Support_1_8V:** 1: 1.8V Supported. 0: 1.8V NOT Supported
7	0h RW	**Voltage_Support_3V:** 1: 3.0V Supported. 0: 3.0V NOT Supported
6	0h RW	**Voltage_Support_3_3V:** 1: 3.3V Supported. 0: 3.3V NOT Supported
5	1h RW	**Suspend_Resume_Support:** 1: Suspend/Resume Supported. 0: Suspend/Resume NOT Supported
4	1h RW	**SDMA_Support:** 1: SDMA mode Supported. 0: SDMA mode NOT Supported
3	1h RW	**High_Speed_Support:** 1: HIGH_SPEED mode Supported. 0: HIGH_SPEED mode NOT Supported
2	1h RW	**ADMA2_Support:** 1: ADMA2 mode Supported. 0: ADMA2 mode NOT Supported
1:0	0h RW	**Max_Burst_Length:** Maximum Block Length supported by the Core/Device. 00: 512 (Bytes). 01: 1024. 10: 2048. 11: Reserved

20.1.5 (Cap_byps_reg2)—Offset 818h

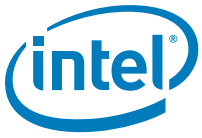
eMMC Capabilities Bypass register 2

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40040C8h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:21	20h RW	**tuning_count_val:** Tuning Count Value Configures the Number of Taps (Phases) of the rxclk_in that is supported. The Tuning State machine uses this information to select one of the Taps (Phases) of the rxclk_in during the Tuning Procedure.
20	0h RW	**tuning_dis:** Disable the 1.5x Tuning count when calculating total tuning count. The internal tuning count will be set to the corecfg_Tuningcount when this signal is asserted
19	0h RW	**driver_type_4:** Driver Type 4 Support 1'b1 - Supported 1'b0 - NOT Supported
18	0h RW	**driver_type_D:** Driver Type D Support 1'b1 - Supported 1'b0 - NOT Supported
17	0h RW	**driver_type_C:** Driver Type C Support 1'b1 - Supported 1'b0 - NOT Supported



Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**driver_type_A:** Driver Type A Support 1'b1 - Supported 1'b0 - NOT Supported
15	0h RO	Reserved.
14	1h RW	**support_8_bit_embedded:** 8-bit Support for Embedded Device 1'b1 - Supported 1'b0 - NOT Supported
13:8	0h RO	Reserved.
7:0	C8h RW	**base_sd_clock:** Base Clock Frequency for SD Clock

20.1.6 (reg_D0i3)—Offset 81Ch

D0i3 Control register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RW/1C	**RestoreRequired:** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0i3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RO	**Interrupt_Request:** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register. Not supported in SCS!
0	0h RO	**Cmd_In_Progress:** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles

20.1.7 (Tx_CMD_dly)—Offset 820h

Front end module Tx Command Path Delay register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 400h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:8	4h RW	**ddr_mode:** Tx CMD Delay (DDR Mode). 0 - 39 - Select number of active delay elements. Each = 125pSec. 40 - 127 - Reserved
7	0h RO	Reserved.
6:0	0h RW	**sdr_mode:** Tx CMD Delay (SDR Mode). 0 - 39 - Select number of active delay elements. Each = 125pSec. 40 - 127 - Reserved

20.1.8 (Tx_DATA_dly_1)—Offset 824h

Front end module Tx data Path Delay register 1

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: A18h

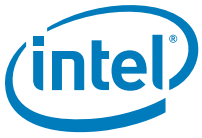
Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:8	Ah RW	**hs400_mode:** Tx Data Delay (HS400 Mode). 0 - 78 - Select number of active delay elements. Each = 125pSec. 79 - 127 - Reserved
7	0h RO	Reserved.
6:0	18h RW	**sdr104_hs200:** Tx Data Delay (SDR104/HS200 Mode) 0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved

20.1.9 (Tx_DATA_dly_2)—Offset 828h

Front end module Tx data Path Delay register 2

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**



Default: 1C1C1C00h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:24	1Ch RW	**sdr50_mode:** Tx Data Delay (SDR50 Mode) 0-79 - Select the required delay, as a multiple of 125pSec. 80 - 127 - Reserved
23	0h RO	Reserved.
22:16	1Ch RW	**ddr50_mode:** Tx Data Delay (DDR50 Mode). 0 - 78 - Select number of active delay elements. Each = 125pSec. 79 - 127 - Reserved
15	0h RO	Reserved.
14:8	1Ch RW	**sdr25_hs50_mode:** Tx Data Delay (SDR25/HS50 Mode)0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved
7	0h RO	Reserved.
6:0	0h RW	**sdr12_comp_mode:** Tx Data Delay (SDR12/Compatibility Mode) 0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved

20.1.10 (Rx_CMD_Data_dly_1)—Offset 82Ch

Front end module Rx data Path Delay register 1

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:24	0h RW	**sdr50_mode:** Rx CMD + Data Delay (SDR50 Mode). 0 - 79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved
23	0h RO	Reserved.
22:16	0h RW	**ddr50_mode:** Rx CMD + Data Delay (DDR50 Mode). 0 - 78 - Select number of active delay elements. Each = 125pSec. 79 - 127 - Reserved
15	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:8	0h RW	**sdr25_hs50:** Rx CMD + Data Delay (SDR25/HS50 Mode) 0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved
7	0h RO	Reserved.
6:0	0h RW	**sdr12_comp:** Rx CMD + Data Delay (SDR12/Compatibility Mode) 0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved

20.1.11 (Rx_Strobe_Ctrl_Path)—Offset 830h

Front end module Rx strobe Path Delay register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW	**auto_tuning:** Enable Auto Tuning for HS400 Strobe Path 0 - Auto Tuning Disabled 1 - Auto Tuning Enabled
15	0h RO	Reserved.
14:8	0h RW	**hs400_mode1:** Rx Strobe Delay DLL 1(HS400 Mode) 0 - 39 - Select number of active delay elements. Each = 125pSec 0 - 63 - Reserved
7	0h RO	Reserved.
6:0	0h RW	**hs400_mode2:** Rx Strobe Delay DLL 2(HS400 Mode) 0 - 39 - Select number of active delay elements. Each = 125pSec 40 - 63 - Reserved

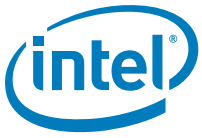
20.1.12 (Rx_CMD_Data_dly_2)—Offset 834h

Front end module Rx data Path Delay register 2

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:16	0h RW	**clk_source:** Clock Source for Rx Path 00 - Rx Clock after Output Buffer 01 - Rx Clock before Output Buffer 10 - Automatic Selection based on Working mode (HS 200 before buffer, all others after buffer) 11 - Reserved
15:14	0h RO	Reserved.
13:8	0h RW	**path_pll:** Rx Path PLL #3 Delay value For Auto Tuning Mode 0-39 - Select the required delay, as a multiple of 125pSec.40 - 63 - Reserved
7	0h RO	Reserved.
6:0	0h RW	**cmd_data_sdr104_hs200:** Rx CMD + Data Delay (SDR104/ HS200 Mode) 0-79 - Select the required delay, as a multiple of 125pSec. 80 - 127 - Reserved

20.1.13 (Master_Dll)—Offset 838h

Master DLL Software control register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW	**SW_reset_dll:** SW reset for Master DLL 0 - No SW Reset for Master DLL 1 - Force Reset for Master DLL
23	0h RO	**DLL_lock:** Master DLL Lock Indication
22:8	0h RW	**coarse_code:** Set coarse code to DLL. (only valid when Software control is Enabled)
7:4	0h RW	**fine_code:** Set fine code to DLL. (only valid when Software control is Enabled)
3	0h RO/V	**less:** Phase Detection Less Indication
2	0h RO/V	**more:** Phase Detector More Indication
1	0h RW	**Master_DLL_Software_Ctrl:** Master DLL Software Ctrl. 0 - Master DLL Automatic Control (SW Control Disabled). 1 - Master DLL Software Control Enabled

Bit Range	Default & Access	Field Name (ID): Description
0	1h RW	**Ctrl_of_Mst_DLL_Ref_Clk:** Ctrl of Master DLL Ref Clock. 0 - Clock is Disabled. 1 - Clock is Enabled

20.1.14 (Auto_tuning)—Offset 840h

Auto Tuning Value

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO/V	**Auto_tuning_val**

20.1.15 (emmc_Root_Space)—Offset 900h

Root space select to indicate which root space the IP will output its upstream accesses

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**root_space:** Root Space Select Selects the Root Space in which the IP output its upstream accesses 0 - Root Space 0 1 - Root Space 1

20.2 Registers Summary

Table 20-2. Summary of CONVERGE_LAYER Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
804h	807h	(SW_LTR_val)—Offset 804h	800h
808h	80Bh	(Auto_LTR_val)—Offset 808h	800h

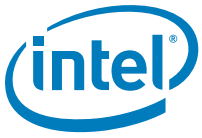


Table 20-2. Summary of CONVERGE_LAYER Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
810h	813h	(Cap_byps)—Offset 810h	0h
814h	817h	(Cap_byps_reg1)—Offset 814h	3041EF3Ch
818h	81Bh	(Cap_byps_reg2)—Offset 818h	40040C8h
81Ch	81Fh	(reg_D0i3)—Offset 81Ch	8h
820h	823h	(Tx_CMD_dly)—Offset 820h	400h
824h	827h	(Tx_DATA_dly_1)—Offset 824h	A18h
828h	82Bh	(Tx_DATA_dly_2)—Offset 828h	1C1C1C00h
82Ch	82Fh	(Rx_CMD_Data_dly_1)—Offset 82Ch	0h
830h	833h	(Rx_Strobe_Ctrl_Path)—Offset 830h	0h
834h	837h	(Rx_CMD_Data_dly_2)—Offset 834h	0h
838h	83Bh	(Master_Dll)—Offset 838h	1h
840h	843h	(Auto_tuning)—Offset 840h	0h
900h	903h	(emmc_Root_Space)—Offset 900h	0h

20.2.1 (SW_LTR_val)—Offset 804h

Sets the Software Latency Tolerance Reporting fields

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop_Requirement:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop_latency_scale:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop_value:** 10-bit latency value

20.2.2 (Auto_LTR_val)—Offset 808h

Sets the Auto Latency Tolerance Reporting fields

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop_Requirement:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	**Reserved_low:** Reserved_low
12:10	2h RW	**Snoop_latency_scale:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop_value:** 10-bit latency value

20.2.3 (Cap_byps)—Offset 810h

Capabilities Bypass Control register

Access Method

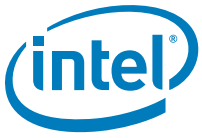
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**Enable_Cap_Bypass:** 8'h5A - Enable Capabilities Bypass. All other - Capabilities Bypass Disable (using default values)

20.2.4 (Cap_byps_reg1)—Offset 814h

eMMC Capabilities Bypass register 1



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3041EF3Ch

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	1h RW	**hs400_support:** 1: HS400 Mode Supported. 0: HS400 Mode NOT Supported
28	1h RW	**timeout_clock_unit:** 1'b1 - to Select MHz Clock ,1'b0 - to Select KHz Clock
27:22	1h RW	**timeout_clock_freq:** Timeout clock frequency
21	0h RW	**SPI_mode_support:** SPI Mode Support 1'b1 - SPI Mode Supported ,1'b0 - SPI Mode Not Supported
20:17	0h RW	**timer_count:** Timer Count for Re-Tuning This is the Timer Count for Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 4'b0 disables Re-Tuning Timer
16	1h RW	**tuning_for_SDR50:** Use Tuning for SDR50 1'b1 - Use Tuning 1'b0 - Don't use Tuning
15	1h RW	**ddr50_support:** 1: DDR50 Mode Supported. 0: DDR50 Mode NOT Supported
14	1h RW	**sdr104_support:** 1: SDR104 Mode Supported. 0: SDR104 Mode NOT Supported
13	1h RW	**sdr50_support:** 1: SDR50 Mode Supported. 0: SDR50 Mode NOT Supported
12:11	1h RW	**Slot_Type:** 00 - Removable SD Card Slot. 01 - Embedded Slot for One Device. 10 - Shared Bus Slot. 11 - Reserved
10	1h RW	**Async_Interrupt_Support:** 1: Asynchronous Interrupt Supported. 0: Asynchronous Interrupt NOT Supported
9	1h RW	**Sys_Addr_64bit_Support:** 1 - Core supports 64-bit System Address Bus. 0 - Core supports only 32-bit System Address Bus
8	1h RW	**Voltage_Support_1_8V:** 1: 1.8V Supported. 0: 1.8V NOT Supported
7	0h RW	**Voltage_Support_3V:** 1: 3.0V Supported. 0: 3.0V NOT Supported
6	0h RW	**Voltage_Support_3_3V:** 1: 3.3V Supported. 0: 3.3V NOT Supported
5	1h RW	**Suspend_Resume_Support:** 1: Suspend/Resume Supported. 0: Suspend/Resume NOT Supported
4	1h RW	**SDMA_Support:** 1: SDMA mode Supported. 0: SDMA mode NOT Supported

Bit Range	Default & Access	Field Name (ID): Description
3	1h RW	**High_Speed_Support:** 1: HIGH_SPEED mode Supported. 0: HIGH_SPEED mode NOT Supported
2	1h RW	**ADMA2_Support:** 1: ADMA2 mode Supported. 0: ADMA2 mode NOT Supported
1:0	0h RW	**Max_Burst_Length:** Maximum Block Length supported by the Core/Device. 00: 512 (Bytes). 01: 1024. 10: 2048. 11: Reserved

20.2.5 (Cap_byps_reg2)—Offset 818h

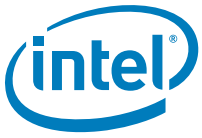
eMMC Capabilities Bypass register 2

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40040C8h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:21	20h RW	**tuning_count_val:** Tuning Count Value Configures the Number of Taps (Phases) of the rxclk_in that is supported. The Tuning State machine uses this information to select one of the Taps (Phases) of the rxclk_in during the Tuning Procedure.
20	0h RW	**tuning_dis:** Disable the 1.5x Tuning count when calculating total tuning count. The internal tuning count will be set to the corecfg_Tuningcount when this signal is asserted
19	0h RW	**driver_type_4:** Driver Type 4 Support 1'b1 - Supported 1'b0 - NOT Supported
18	0h RW	**driver_type_D:** Driver Type D Support 1'b1 - Supported 1'b0 - NOT Supported
17	0h RW	**driver_type_C:** Driver Type C Support 1'b1 - Supported 1'b0 - NOT Supported
16	0h RW	**driver_type_A:** Driver Type A Support 1'b1 - Supported 1'b0 - NOT Supported
15	0h RO	Reserved.
14	1h RW	**support_8_bit_embedded:** 8-bit Support for Embedded Device 1'b1 - Supported 1'b0 - NOT Supported
13:8	0h RO	Reserved.
7:0	C8h RW	**base_sd_clock:** Base Clock Frequency for SD Clock



20.2.6 (reg_D0i3)—Offset 81Ch

D0i3 Control register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RW/1C	**RestoreRequired:** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0i3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RO	**Interrupt_Request:** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register. Not supported in SCS!
0	0h RO	**Cmd_In_Progress:** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles

20.2.7 (Tx_CMD_dly)—Offset 820h

Front end module Tx Command Path Delay register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 400h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:8	4h RW	**ddr_mode:** Tx CMD Delay (DDR Mode). 0 - 39 - Select number of active delay elements. Each = 125pSec. 40 - 127 - Reserved

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:0	0h RW	**sdr_mode:** Tx CMD Delay (SDR Mode). 0 - 39 - Select number of active delay elements. Each = 125pSec. 40 - 127 - Reserved

20.2.8 (Tx_DATA_dly_1)—Offset 824h

Front end module Tx data Path Delay register 1

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: A18h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:8	Ah RW	**hs400_mode:** Tx Data Delay (HS400 Mode). 0 - 78 - Select number of active delay elements. Each = 125pSec. 79 - 127 - Reserved
7	0h RO	Reserved.
6:0	18h RW	**sdr104_hs200:** Tx Data Delay (SDR104/HS200 Mode) 0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved

20.2.9 (Tx_DATA_dly_2)—Offset 828h

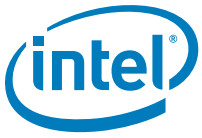
Front end module Tx data Path Delay register 2

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1C1C1C00h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:24	1Ch RW	**sdr50_mode:** Tx Data Delay (SDR50 Mode) 0-79 - Select the required delay, as a multiple of 125pSec. 80 - 127 - Reserved
23	0h RO	Reserved.



Bit Range	Default & Access	Field Name (ID): Description
22:16	1Ch RW	**ddr50_mode:** Tx Data Delay (DDR50 Mode). 0 - 78 - Select number of active delay elements. Each = 125pSec. 79 - 127 - Reserved
15	0h RO	Reserved.
14:8	1Ch RW	**sdr25_hs50_mode:** Tx Data Delay (SDR25/HS50 Mode)0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved
7	0h RO	Reserved.
6:0	0h RW	**sdr12_comp_mode:** Tx Data Delay (SDR12/Compatibility Mode) 0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved

20.2.10 (Rx_CMD_Data_dly_1)—Offset 82Ch

Front end module Rx data Path Delay register 1

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:24	0h RW	**sdr50_mode:** Rx CMD + Data Delay (SDR50 Mode). 0 - 79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved
23	0h RO	Reserved.
22:16	0h RW	**ddr50_mode:** Rx CMD + Data Delay (DDR50 Mode). 0 - 78 - Select number of active delay elements. Each = 125pSec. 79 - 127 - Reserved
15	0h RO	Reserved.
14:8	0h RW	**sdr25_hs50:** Rx CMD + Data Delay (SDR25/HS50 Mode) 0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved
7	0h RO	Reserved.
6:0	0h RW	**sdr12_comp:** Rx CMD + Data Delay (SDR12/Compatibility Mode) 0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved

20.2.11 (Rx_Strobe_Ctrl_Path)—Offset 830h

Front end module Rx strobe Path Delay register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW	**auto_tuning:** Enable Auto Tuning for HS400 Strobe Path 0 - Auto Tuning Disabled 1 - Auto Tuning Enabled
15	0h RO	Reserved.
14:8	0h RW	**hs400_mode1:** Rx Strobe Delay DLL 1(HS400 Mode) 0 - 39 - Select number of active delay elements. Each = 125pSec 0 - 63 - Reserved
7	0h RO	Reserved.
6:0	0h RW	**hs400_mode2:** Rx Strobe Delay DLL 2(HS400 Mode) 0 - 39 - Select number of active delay elements. Each = 125pSec 40 - 63 - Reserved

20.2.12 (Rx_CMD_Data_dly_2)—Offset 834h

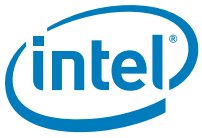
Front end module Rx data Path Delay register 2

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:16	0h RW	**clk_source:** Clock Source for Rx Path 00 - Rx Clock after Output Buffer 01 - Rx Clock before Output Buffer 10 - Automatic Selection based on Working mode (HS 200 before buffer, all others after buffer) 11 - Reserved
15:14	0h RO	Reserved.



Bit Range	Default & Access	Field Name (ID): Description
13:8	0h RW	**path_pll:** Rx Path PLL #3 Delay value For Auto Tuning Mode 0-39 - Select the required delay, as a multiple of 125pSec.40 - 63 - Reserved
7	0h RO	Reserved.
6:0	0h RW	**cmd_data_sdr104_hs200:** Rx CMD + Data Delay (SDR104/ HS200 Mode) 0-79 - Select the required delay, as a multiple of 125pSec. 80 - 127 - Reserved

20.2.13 (Master_Dll)—Offset 838h

Master DLL Software control register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW	**SW_reset_dll:** SW reset for Master DLL 0 - No SW Reset for Master DLL 1 - Force Reset for Master DLL
23	0h RO	**DLL_lock:** Master DLL Lock Indication
22:8	0h RW	**coarse_code:** Set coarse code to DLL. (only valid when Software control is Enabled)
7:4	0h RW	**fine_code:** Set fine code to DLL. (only valid when Software control is Enabled)
3	0h RO/V	**less:** Phase Detection Less Indication
2	0h RO/V	**more:** Phase Detector More Indication
1	0h RW	**Master_DLL_Software_Ctrl:** Master DLL Software Ctrl. 0 - Master DLL Automatic Control (SW Control Disabled). 1 - Master DLL Software Control Enabled
0	1h RW	**Ctrl_of_Mst_DLL_Ref_Clk:** Ctrl of Master DLL Ref Clock. 0 - Clock is Disabled. 1 - Clock is Enabled

20.2.14 (Auto_tuning)—Offset 840h

Auto Tuning Value

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO/V	**Auto_tuning_val**

20.2.15 (emmc_Root_Space)—Offset 900h

Root space select to indicate which root space the IP will output its upstream accesses

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**root_space:** Root Space Select Selects the Root Space in which the IP output its upstream accesses 0 - Root Space 0 1 - Root Space 1

20.3 Registers Summary

Table 20-3. Summary of CONVERGE_LAYER Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
804h	807h	(SW_LTR_val)—Offset 804h	800h
808h	80Bh	(Auto_LTR_val)—Offset 808h	800h
810h	813h	(Cap_byps)—Offset 810h	0h
814h	817h	(Cap_byps_reg1)—Offset 814h	3041EF3Ch
818h	81Bh	(Cap_byps_reg2)—Offset 818h	40040C8h
81Ch	81Fh	(reg_D0i3)—Offset 81Ch	8h
820h	823h	(Tx_CMD_dly)—Offset 820h	400h
824h	827h	(Tx_DATA_dly_1)—Offset 824h	A18h
828h	82Bh	(Tx_DATA_dly_2)—Offset 828h	1C1C1C00h
82Ch	82Fh	(Rx_CMD_Data_dly_1)—Offset 82Ch	0h
830h	833h	(Rx_Strobe_Ctrl_Path)—Offset 830h	0h

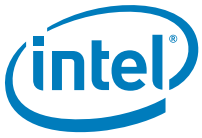


Table 20-3. Summary of CONVERGE_LAYER Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
834h	837h	(Rx_CMD_Data_dly_2)—Offset 834h	0h
838h	83Bh	(Master_Dll)—Offset 838h	1h
840h	843h	(Auto_tuning)—Offset 840h	0h
900h	903h	(emmc_Root_Space)—Offset 900h	0h

20.3.1 (SW_LTR_val)—Offset 804h

Sets the Software Latency Tolerance Reporting fields

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop_Requirement:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop_latency_scale:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop_value:** 10-bit latency value

20.3.2 (Auto_LTR_val)—Offset 808h

Sets the Auto Latency Tolerance Reporting fields

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop_Requirement:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	**Reserved_low:** Reserved_low
12:10	2h RW	**Snoop_latency_scale:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop_value:** 10-bit latency value

20.3.3 (Cap_byps)—Offset 810h

Capabilities Bypass Control register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**Enable_Cap_Bypass:** 8'h5A - Enable Capabilities Bypass. All other - Capabilities Bypass Disable (using default values)

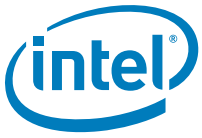
20.3.4 (Cap_byps_reg1)—Offset 814h

eMMC Capabilities Bypass register 1

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 3041EF3Ch



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	1h RW	**hs400_support:** 1: HS400 Mode Supported. 0: HS400 Mode NOT Supported
28	1h RW	**timeout_clock_unit:** 1'b1 - to Select MHz Clock ,1'b0 - to Select KHz Clock
27:22	1h RW	**timeout_clock_freq:** Timeout clock frequency
21	0h RW	**SPI_mode_support:** SPI Mode Support 1'b1 - SPI Mode Supported ,1'b0 - SPI Mode Not Supported
20:17	0h RW	**timer_count:** Timer Count for Re-Tuning This is the Timer Count for Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 4'b0 disables Re-Tuning Timer
16	1h RW	**tuning_for_SDR50:** Use Tuning for SDR50 1'b1 - Use Tuning 1'b0 - Don't use Tuning
15	1h RW	**ddr50_support:** 1: DDR50 Mode Supported. 0: DDR50 Mode NOT Supported
14	1h RW	**sdr104_support:** 1: SDR104 Mode Supported. 0: SDR104 Mode NOT Supported
13	1h RW	**sdr50_support:** 1: SDR50 Mode Supported. 0: SDR50 Mode NOT Supported
12:11	1h RW	**Slot_Type:** 00 - Removable SD Card Slot. 01 - Embedded Slot for One Device. 10 - Shared Bus Slot. 11 - Reserved
10	1h RW	**Async_Interrupt_Support:** 1: Asynchronous Interrupt Supported. 0: Asynchronous Interrupt NOT Supported
9	1h RW	**Sys_Addr_64bit_Support:** 1 - Core supports 64-bit System Address Bus. 0 - Core supports only 32-bit System Address Bus
8	1h RW	**Voltage_Support_1_8V:** 1: 1.8V Supported. 0: 1.8V NOT Supported
7	0h RW	**Voltage_Support_3V:** 1: 3.0V Supported. 0: 3.0V NOT Supported
6	0h RW	**Voltage_Support_3_3V:** 1: 3.3V Supported. 0: 3.3V NOT Supported
5	1h RW	**Suspend_Resume_Support:** 1: Suspend/Resume Supported. 0: Suspend/Resume NOT Supported
4	1h RW	**SDMA_Support:** 1: SDMA mode Supported. 0: SDMA mode NOT Supported
3	1h RW	**High_Speed_Support:** 1: HIGH_SPEED mode Supported. 0: HIGH_SPEED mode NOT Supported
2	1h RW	**ADMA2_Support:** 1: ADMA2 mode Supported. 0: ADMA2 mode NOT Supported
1:0	0h RW	**Max_Burst_Length:** Maximum Block Length supported by the Core/Device. 00: 512 (Bytes). 01: 1024. 10: 2048. 11: Reserved

20.3.5 (Cap_byps_reg2)—Offset 818h

eMMC Capabilities Bypass register 2

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 40040C8h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:21	20h RW	**tuning_count_val:** Tuning Count Value Configures the Number of Taps (Phases) of the rxclk_in that is supported. The Tuning State machine uses this information to select one of the Taps (Phases) of the rxclk_in during the Tuning Procedure.
20	0h RW	**tuning_dis:** Disable the 1.5x Tuning count when calculating total tuning count. The internal tuning count will be set to the corecfg_Tuningcount when this signal is asserted
19	0h RW	**driver_type_4:** Driver Type 4 Support 1'b1 - Supported 1'b0 - NOT Supported
18	0h RW	**driver_type_D:** Driver Type D Support 1'b1 - Supported 1'b0 - NOT Supported
17	0h RW	**driver_type_C:** Driver Type C Support 1'b1 - Supported 1'b0 - NOT Supported
16	0h RW	**driver_type_A:** Driver Type A Support 1'b1 - Supported 1'b0 - NOT Supported
15	0h RO	Reserved.
14	1h RW	**support_8_bit_embedded:** 8-bit Support for Embedded Device 1'b1 - Supported 1'b0 - NOT Supported
13:8	0h RO	Reserved.
7:0	C8h RW	**base_sd_clock:** Base Clock Frequency for SD Clock

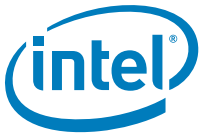
20.3.6 (reg_D0i3)—Offset 81Ch

D0i3 Control register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RW/1C	**RestoreRequired:** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0i3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RO	**Interrupt_Request:** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register. Not supported in SCS!
0	0h RO	**Cmd_In_Progress:** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles

20.3.7 (Tx_CMD_dly)—Offset 820h

Front end module Tx Command Path Delay register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 400h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:8	4h RW	**ddr_mode:** Tx CMD Delay (DDR Mode). 0 - 39 - Select number of active delay elements. Each = 125pSec. 40 - 127 - Reserved
7	0h RO	Reserved.
6:0	0h RW	**sdr_mode:** Tx CMD Delay (SDR Mode). 0 - 39 - Select number of active delay elements. Each = 125pSec. 40 - 127 - Reserved

20.3.8 (Tx_DATA_dly_1)—Offset 824h

Front end module Tx data Path Delay register 1

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: A18h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:8	Ah RW	**hs400_mode:** Tx Data Delay (HS400 Mode). 0 - 78 - Select number of active delay elements. Each = 125pSec. 79 - 127 - Reserved
7	0h RO	Reserved.
6:0	18h RW	**sdr104_hs200:** Tx Data Delay (SDR104/HS200 Mode) 0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved

20.3.9 (Tx_DATA_dly_2)—Offset 828h

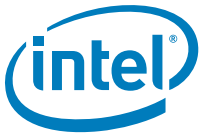
Front end module Tx data Path Delay register 2

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1C1C1C00h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:24	1Ch RW	**sdr50_mode:** Tx Data Delay (SDR50 Mode) 0-79 - Select the required delay, as a multiple of 125pSec. 80 - 127 - Reserved
23	0h RO	Reserved.
22:16	1Ch RW	**ddr50_mode:** Tx Data Delay (DDR50 Mode). 0 - 78 - Select number of active delay elements. Each = 125pSec. 79 - 127 - Reserved
15	0h RO	Reserved.
14:8	1Ch RW	**sdr25_hs50_mode:** Tx Data Delay (SDR25/HS50 Mode)0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved
7	0h RO	Reserved.



Bit Range	Default & Access	Field Name (ID): Description
6:0	0h RW	**sdr12_comp_mode:** Tx Data Delay (SDR12/Compatibility Mode) 0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved

20.3.10 (Rx_CMD_Data_dly_1)—Offset 82Ch

Front end module Rx data Path Delay register 1

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:24	0h RW	**sdr50_mode:** Rx CMD + Data Delay (SDR50 Mode). 0 - 79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved
23	0h RO	Reserved.
22:16	0h RW	**ddr50_mode:** Rx CMD + Data Delay (DDR50 Mode). 0 - 78 - Select number of active delay elements. Each = 125pSec. 79 - 127 - Reserved
15	0h RO	Reserved.
14:8	0h RW	**sdr25_hs50:** Rx CMD + Data Delay (SDR25/HS50 Mode) 0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved
7	0h RO	Reserved.
6:0	0h RW	**sdr12_comp:** Rx CMD + Data Delay (SDR12/Compatibility Mode) 0-79 - Select the required delay, as a multiple of 125pSec.80 - 127 - Reserved

20.3.11 (Rx_Strobe_Ctrl_Path)—Offset 830h

Front end module Rx strobe Path Delay register

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW	**auto_tuning:** Enable Auto Tuning for HS400 Strobe Path 0 - Auto Tuning Disabled 1 - Auto Tuning Enabled
15	0h RO	Reserved.
14:8	0h RW	**hs400_mode1:** Rx Strobe Delay DLL 1(HS400 Mode) 0 - 39 - Select number of active delay elements. Each = 125pSec 0 - 63 - Reserved
7	0h RO	Reserved.
6:0	0h RW	**hs400_mode2:** Rx Strobe Delay DLL 2(HS400 Mode) 0 - 39 - Select number of active delay elements. Each = 125pSec 40 - 63 - Reserved

20.3.12 (Rx_CMD_Data_dly_2)—Offset 834h

Front end module Rx data Path Delay register 2

Access Method

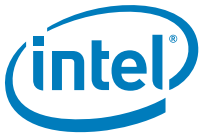
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:16	0h RW	**clk_source:** Clock Source for Rx Path 00 - Rx Clock after Output Buffer 01 - Rx Clock before Output Buffer 10 - Automatic Selection based on Working mode (HS 200 before buffer, all others after buffer) 11 - Reserved
15:14	0h RO	Reserved.
13:8	0h RW	**path_pll:** Rx Path PLL #3 Delay value For Auto Tuning Mode 0-39 - Select the required delay, as a multiple of 125pSec.40 - 63 - Reserved
7	0h RO	Reserved.
6:0	0h RW	**cmd_data_sdr104_hs200:** Rx CMD + Data Delay (SDR104/ HS200 Mode) 0-79 - Select the required delay, as a multiple of 125pSec. 80 - 127 - Reserved

20.3.13 (Master_Dll)—Offset 838h

Master DLL Software control register



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW	**SW_reset_dll:** SW reset for Master DLL 0 - No SW Reset for Master DLL 1 - Force Reset for Master DLL
23	0h RO	**DLL_lock:** Master DLL Lock Indication
22:8	0h RW	**coarse_code:** Set coarse code to DLL. (only valid when Software control is Enabled)
7:4	0h RW	**fine_code:** Set fine code to DLL. (only valid when Software control is Enabled)
3	0h RO/V	**less:** Phase Detection Less Indication
2	0h RO/V	**more:** Phase Detector More Indication
1	0h RW	**Master_DLL_Software_Ctrl:** Master DLL Software Ctrl. 0 - Master DLL Automatic Control (SW Control Disabled). 1 - Master DLL Software Control Enabled
0	1h RW	**Ctrl_of_Mst_DLL_Ref_Clk:** Ctrl of Master DLL Ref Clock. 0 - Clock is Disabled. 1 - Clock is Enabled

20.3.14 (Auto_tuning)—Offset 840h

Auto Tuning Value

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO/V	**Auto_tuning_val**

20.3.15 (emmc_Root_Space)—Offset 900h

Root space select to indicate which root space the IP will output its upstream accesses

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**root_space:** Root Space Select Selects the Root Space in which the IP output its upstream accesses 0 - Root Space 0 1 - Root Space 1

20.4 Registers Summary

Table 20-4. Summary of soc_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	(DEVVENDID)—Offset 0h	8086h
4h	7h	(STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	(REVCLASSCODE)—Offset 8h	8050100h
Ch	Fh	(CLLATHEADERBIST)—Offset Ch	0h
10h	13h	(BAR)—Offset 10h	4h
14h	17h	(BAR_HIGH)—Offset 14h	0h
18h	1Bh	(BAR1)—Offset 18h	4h
1Ch	1Fh	(BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	(SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	(EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	(CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	(INTERRUPTREG)—Offset 3Ch	0h
80h	83h	(POWERCAPID)—Offset 80h	39001h
84h	87h	(PMECTRLSTATUS)—Offset 84h	8h
90h	93h	(PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	(DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	(D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	8041h
9Ch	9Fh	(DEVICE_IDLE_POINTER_REG)—Offset 9Ch	81C1h
A0h	A3h	(D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	290800h

20.4.1 (DEVVENDID)—Offset 0h

DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**DEVICEID**
15:0	8086h RO	**VENDORID**

20.4.2 (STATUSCOMMAND)—Offset 4h

STATUSCOMMAND- Status and Command

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0**
29	0h RW/1C	**RMA**
28	0h RW/1C	**RTA**
27:21	0h RO	**Reserved1**
20	1h RO	**CAPLIST**
19	0h RO	**INTR_STATUS**
18:16	0h RO	**Reserved2**
15:11	0h RO	**Reserved3**
10	0h RW	**INTR_DISABLE**
9	0h RO	**Reserved4**
8	0h RW	**SERR_ENABLE**
7:3	0h RO	**Reserved5**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**BME**
1	0h RW	**MSE**
0	0h RO	**Reserved6**

20.4.3 (REVCLASSCODE)—Offset 8h

REVCLASSCODE - Revision ID and Class Code

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 8050100h

Bit Range	Default & Access	Field Name (ID): Description
31:8	80501h RO	**CLASS_CODES**
7:0	0h RO	**RID**

20.4.4 (CLLATHEADERBIST)—Offset Ch

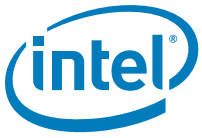
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved0**
23	0h RO	**MULFNDEV**
22:16	0h RO	**HEADERTYPE**
15:8	0h RO	**LATTIMER**
7:0	0h RW	**CACHELINE_SIZE**



20.4.5 (BAR)—Offset 10h

BAR -Base Address Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR**
11:4	0h RO	**SIZEINDICATOR**
3	0h RO	**PREFETCHABLE**
2:1	2h RO	**TYPE**
0	0h RO	**MESSAGE_SPACE**

20.4.6 (BAR_HIGH)—Offset 14h

BAR -Base Address Register High

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR_HIGH**

20.4.7 (BAR1)—Offset 18h

BAR1 -Base Address Register1

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR1**
11:4	0h RO	**SIZEINDICATOR1**
3	0h RO	**PREFETCHABLE1**
2:1	2h RO	**TYPE1**
0	0h RO	**MESSAGE_SPACE1**

20.4.8 (BAR1_HIGH)—Offset 1Ch

BAR1 -Base Address Register1 High

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR1_HIGH**

20.4.9 (SUBSYSTEMID)—Offset 2Ch

SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

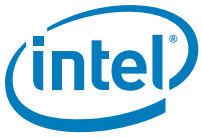
Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID**
15:0	0h RW/O	**SUBSYSTEMVENDORID**

20.4.10 (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address



Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE**

20.4.11 (CAPABILITYPTR)—Offset 34h

CAPABILITYPTR - Capabilities Pointer

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved0**
7:0	80h RO	**CAPPTR_POWER**

20.4.12 (INTERRUPTREG)—Offset 3Ch

INTERRUPTREG - Interrupt Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT**
23:16	0h RO	**MIN_GNT**
15:12	0h RO	**Reserved0**
11:8	0h RO	**INTPIN**

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**INTLINE**

20.4.13 (POWERCAPID)—Offset 80h

POWERCAPID - PowerManagement Capability ID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 39001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**PMESUPPORT**
26:19	0h RO	**Reserved0**
18:16	3h RO	**VERSION**
15:8	90h RO	**NXTCAP**
7:0	1h RO	**POWER_CAP**

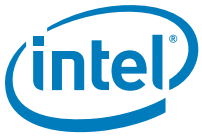
20.4.14 (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved0**
15	0h RW/1C	**PMESTATUS**
14:9	0h RO	**Reserved1**
8	0h RW	**PMEENABLE**
7:4	0h RO	**Reserved2**



Bit Range	Default & Access	Field Name (ID): Description
3	1h RO	**NO_SOFT_RESET**
2	0h RO	**Reserved3**
1:0	0h RW	**POWERSTATE**

20.4.15 (PCIDEVIDLE_CAP_RECORD)—Offset 90h

PCI DEVICE IDLE CAPABILITY RECORD

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP**
27:24	0h RO	**REVID**
23:16	14h RO	**CAP_LENGTH**
15:8	0h RO	**NEXT_CAP**
7:0	9h RO	**CAPID**

20.4.16 (DEVID_VEND_SPECIFIC_REG)—Offset 94h

DEVID VENDOR SPECIFIC REG

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH**
19:16	0h RO	**VSEC_REV**

Bit Range	Default & Access	Field Name (ID): Description
15:0	10h RO	**VSECID**

20.4.17 (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

SW LTR Update MMIO Location Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 8041h

Bit Range	Default & Access	Field Name (ID): Description
31:4	804h RO	**SW_LAT_DWORD_OFFSET**
3:1	0h RO	**SW_LAT_BAR_NUM**
0	1h RO	**SW_LAT_VALID**

20.4.18 (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

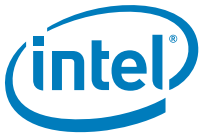
Default: 81C1h

Bit Range	Default & Access	Field Name (ID): Description
31:4	81Ch RO	**DWORD_OFFSET**
3:1	0h RO	**BAR_NUM**
0	1h RO	**VALID**

20.4.19 (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

DEVICE PG CONFIG

Access Method



Type: CFG Register (Size: 32 bits)	**Device:** 28 **Function:** 0

Default: 290800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved0**
21	1h RW	**HAE**
20	0h RO	**Reserved1**
19	1h RW	**SLEEP_EN**
18	0h RW	**PGE**
17	0h RW	**I3_ENABLE**
16	1h RW	**PMCRE**
15:13	0h RO	**Reserved2**
12:10	2h RW/O	**POW_LAT_SCALE**
9:0	0h RW/O	**POW_LAT_VALUE**

20.5 Registers Summary

Table 20-5. Summary of SDHOST_OCP Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	SDMA System Address Register/Argument2 Register (sdmasysaddr)—Offset 0h	0h
4h	5h	BlockSize Register (blocksize)—Offset 4h	0h
6h	7h	BlockCount Register (blockcount)—Offset 6h	0h
8h	Bh	Argument1 Register (argument1)—Offset 8h	0h
Ch	Dh	TransferMode Register (transfermode)—Offset Ch	0h
Eh	Fh	Command Register (command)—Offset Eh	0h
10h	13h	Response Register (response01)—Offset 10h	0h
14h	15h	Response Register (response2)—Offset 14h	0h
16h	17h	Response Register (response3)—Offset 16h	0h
18h	19h	Response Register (response4)—Offset 18h	0h
1Ah	1Bh	Response Register (response5)—Offset 1Ah	0h
1Ch	1Dh	Response Register (response6)—Offset 1Ch	0h
1Eh	1Fh	Response Register (response7)—Offset 1Eh	0h

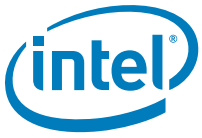
Table 20-5. Summary of SDHOST_OCP Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
20h	23h	Buffer DataPort Register (dataport)—Offset 20h	0h
28h	28h	HostControl1 Register (hostcontrol1)—Offset 28h	0h
29h	29h	PowerControl Register (powercontrol)—Offset 29h	0h
2Ah	2Ah	BlockGapControl Register (blockgapcontrol)—Offset 2Ah	80h
2Bh	2Bh	Wakeup Control Register (wakeupcontrol)—Offset 2Bh	0h
2Ch	2Dh	Clock Control Register (clockcontrol)—Offset 2Ch	0h
2Eh	2Eh	Timeout Control Register (timeoutcontrol)—Offset 2Eh	0h
2Fh	2Fh	Software Reset Register (softwarereset)—Offset 2Fh	0h
30h	31h	Normal Interrupt Status Register (normalintrsts)—Offset 30h	0h
32h	33h	ErrorInterruptStatus_Register (errorintrsts)—Offset 32h	0h
34h	35h	Normal Interrupt Status Enable Register (normalintrstsena)—Offset 34h	0h
36h	37h	Error Interrupt Status Enable Register (errorintrstsena)—Offset 36h	0h
38h	39h	Normal Interrupt Signal Enable Register (normalintrsigena)—Offset 38h	0h
3Ah	3Bh	Error Interrupt Signal Enable Register (errorintrsigena)—Offset 3Ah	0h
3Ch	3Dh	Auto CMD12 Error Status Register (autocmderrsts)—Offset 3Ch	0h
3Eh	3Fh	Host Control2 Register (hostcontrol2)—Offset 3Eh	0h
40h	47h	Capabilities Register (capabilities)—Offset 40h	0h
48h	4Fh	Maximum Current Capabilities Register (maxcurrentcap)—Offset 48h	0h
50h	51h	Force Event REGISTER for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus)—Offset 50h	0h
52h	53h	Force Event Register for Error Interrupt Status (forceeventforerrintsts)—Offset 52h	0h
54h	54h	ADMA Error Status Register (admaerrsts)—Offset 54h	0h
58h	5Bh	ADMA System Address Register0&1 (admasysaddr01)—Offset 58h	0h
5Ch	5Dh	ADMA System Address Register1 (admasysaddr2)—Offset 5Ch	0h
5Eh	5Fh	ADMA System Address Register1 (admasysaddr3)—Offset 5Eh	0h
70h	73h	Boot Timeout Control Register (boottimeoutcnt)—Offset 70h	0h
FCh	FDh	Slot Interrupt Status Register (slotintrsts)—Offset FCh	0h
FEh	FFh	Host Controller Version Register (hostcontrollerver)—Offset FEh	1002h

20.5.1 SDMA System Address Register/Argument2 Register (sdmasysaddr)—Offset 0h

This register contains concatinates reg_sdmasysaddrlo and reg_sdmasysaddrhi

Access Method



Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**sdma_sysaddress (sdma_sysaddress):** refer to reg_sdmasysaddrlo and reg_sdmasysaddrhi

20.5.2 BlockSize Register (blocksize)—Offset 4h

This register is used to configure the number of bytes in a data block

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14:12	0h	**sdma_bufboundary (sdma_bufboundary):** This Field specifies DMA Buffer Boundary
11:0	0h	**xfer_blocksize (xfer_blocksize):** This Field specifies Block Size for Data Transfers

20.5.3 BlockCount Register (blockcount)—Offset 6h

This register is used to configure the number of data blocks

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**xfer_blockcount (xfer_blockcount):** This Register specifies Block Size for Data Transfers

20.5.4 Argument1 Register (argument1)—Offset 8h

This register contains concatinates argument1lo and argument1hi registers to result SD Command Argument

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**command_argument1 (command_argument1):** refer t oreg_argument1lo and reg_argument1hi.

20.5.5 TransferMode Register (transfermode)—Offset Ch

This register is used to control the operations of data transfers

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5	0h	**xfermode_multiblksel (xfermode_multiblksel):** This bit enables multiple block data transfers.
4	0h	**xfermode_dataxferdir (xfermode_dataxferdir):** This bit defines the direction of data transfers.
3:2	0h	**xfermode_autocmdena (xfermode_autocmdena):** This field determines use of auto command functions.
1	0h	**xfermode_blkcntena (xfermode_blkcntena):** This bit is used to enable the Block count register, which is only relevant for multiple block transfers
0	0h	**xfermode_dmaenable (xfermode_dmaenable):** '1' to enable DMA,

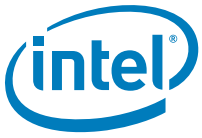
20.5.6 Command Register (command)—Offset Eh

This register is used to program the Command for host controller

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:8	0h	**command_cmdindex (command_cmdindex):** This bit shall be set to the command number (CMD0-63, ACMD0-63).
7:6	0h	**command_cmdtype (command_cmdtype):** This bit is used for select different command types.
5	0h	**command_datapresent (command_datapresent):** This bit is used to checking whether data present or not.
4	0h	**command_indexchkena (command_indexchkena):** This bit is used to enable/disable Command Index checking.
3	0h	**command_crcchkena (command_crcchkena):** This bit is used to enable/disable CRC checking.
2	0h RO	Reserved.
1:0	0h	**command_responsetype (command_responsetype):** Response Type Select.

20.5.7 Response Register (response01)—Offset 10h

This register is used to store responses from SD Cards (concatinates response0 & response1 registers)

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.5.8 Response Register (response2)—Offset 14h

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.5.9 Response Register (response3)—Offset 16h

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.5.10 Response Register (response4)—Offset 18h

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.5.11 Response Register (response5)—Offset 1Ah

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.5.12 Response Register (response6)—Offset 1Ch

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.5.13 Response Register (response7)—Offset 1Eh

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.5.14 Buffer DataPort Register (dataport)—Offset 20h

This register is used to access internal buffer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**sdhcdmactrl_piobufrddata (sdhcdmactrl_piobufrddata):** The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

20.5.15 HostControl1 Register (hostcontrol1)—Offset 28h

This register is used to program DMA modes, LED Control, Data Transfer Width, High Speed Enable, Card detect test level and signal selection

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h	**hostctrl1_cdsigselect (hostctrl1_cdsigselect):** This bit selects source for card detection.
6	0h	**hostctrl1_cdtestlevel (hostctrl1_cdtestlevel):** This bit is used for indicating whether card is inserted or not.
5	0h	**hostctrl1_extdatawidth (hostctrl1_extdatawidth):** This bit controls 8-bit bus width mode for embedded device.
4:3	0h	**hostctrl1_dmaselect (hostctrl1_dmaselect):** One of supported DMA modes can be selected.
2	0h	**hostctrl1_highspeedena (hostctrl1_highspeedena):** This bit is used for setting speed mode.
1	0h	**hostctrl1_datawidth (hostctrl1_datawidth):** This bit selects the data width of the HC.
0	0h	**hostctrl1_ledcontrol (hostctrl1_ledcontrol):** This bit is used to caution the user not to remove the card while the SD card is being accessed.

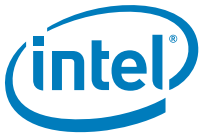
20.5.16 PowerControl Register (powercontrol)—Offset 29h

This register is used to program the SD Bus power and voltage level

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h	**emmc_hwreset (emmc_hwreset):** Hardware reset signal is generated for eMMC card.
3:1	0h	**pwrctrl_sdbusvoltage (pwrctrl_sdbusvoltage):** By setting these bits, the HD selects the voltage level for the SD card.
0	0h	**pwrctrl_sdbuspower (pwrctrl_sdbuspower):** This bit is used detect whether power is on or off.

20.5.17 BlockGapControl Register (blockgapcontrol)—Offset 2Ah

This register is used to program the block gap request, read wait control and interrupt at block gap

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h	**blkgapctrl_bootackena (blkgapctrl_bootackena):** To check for the boot acknowledge in boot operation.
6	0h	**blkgapctrl_altbootmode (blkgapctrl_altbootmode):** To start boot code access in alternative mode.
5	0h	**blkgapctrl_bootenable (blkgapctrl_bootenable):** To start boot code access. '0' To stop boot code access, '1' To start boot code access
4	0h	**blkgapctrl_spimode (blkgapctrl_spimode):** SPI mode enable bit. '0' SD Mode, '1' SPI Mode
3	0h	**blkgapctrl_interrupt (blkgapctrl_interrupt):** This bit is valid only in 4-bit mode of the SD card andselects a sample point in the interrupt cycle.
2	0h	**blkgapctrl_rdwaitctrl (blkgapctrl_rdwaitctrl):** The read wait function is optional for SD cards.
1	0h	**blkgapctrl_continue (blkgapctrl_continue):** This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request.
0	0h	**blkgapctrl_stopatblkgap (blkgapctrl_stopatblkgap):** This bit is used to stop executing a transaction at the next block gap for non- DMA,SDMA and ADMA transfers.

20.5.18 Wakeup Control Register (wakeupcontrol)—Offset 2Bh

This register is used to program the wakeup functionality

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h	**wkupctrl_cardremoval (wkupctrl_cardremoval):** This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register.
1	0h	**wkupctrl_cardinsertion (wkupctrl_cardinsertion):** This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register.
0	0h	**wkupctrl_cardinterrupt (wkupctrl_cardinterrupt):** This bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt Status register.

20.5.19 Clock Control Register (clockcontrol)—Offset 2Ch

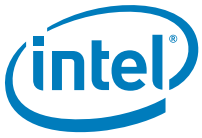
This register is used to program the Clock frequency select, generator select, Clock enable, Internal Clock state fields

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h	**clkctrl_sdclkfreqsel (clkctrl_sdclkfreqsel):** This register is used to select the frequency of the SDCLK pin.
7:6	0h	**clkctrl_sdclkfreqsel_upperbits (clkctrl_sdclkfreqsel_upperbits):** Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select
5	0h	**clkctrl_clkgensel (clkctrl_clkgensel):** This bit is used to select the clock generator mode in SDCLK Frequency Select.
4:3	0h RO	Reserved.
2	0h	**clkctrl_sdclkena (clkctrl_sdclkena):** This bit enables/disables SD Clock. '0' Disable, '1' Enable



Bit Range	Default & Access	Field Name (ID): Description
1	0h	**sdhcclkgen_intclkstable_dsync (sdhcclkgen_intclkstable_dsync):** This bit is set to 1 when SD clock is stable after writing to Internal Clock Enable in this register to 1.
0	0h	**clkctrl_intclkena (clkctrl_intclkena):** This bit enables setting of internal clock.'0' Stop, '1' Oscillate

20.5.20 Timeout Control Register (timeoutcontrol)—Offset 2Eh

The register sets the Data Timeout counter value

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3:0	0h	**timeout_ctrvalue (timeout_ctrvalue):** This value determines the interval by which DAT line time-outs are detected.

20.5.21 Software Reset Register (softwarereset)—Offset 2Fh

This register is used to program the software reset for data, command and for all.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h	**swreset_for_dat (swreset_for_dat):** Only part of data circuit is reset. '0' Work, '1' Reset
1	0h	**swreset_for_cmd (swreset_for_cmd):** Only part of command circuit is reset.'0' Work, '1' reset.
0	0h	**swreset_for_all (swreset_for_all):** If this bit is set to 1, the SD card shall reset itself and must be re initialized by the HD.

20.5.22 Normal Interrupt Status Register (normalintrsts)—Offset 30h

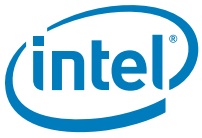
This register gives the status of all the interrupts

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h	**reg_errorintrsts (reg_errorintrsts):** This bit is set If any of the bits in the Error Interrupt Status Register are set.
14	0h	**normalintrsts_bootcomplete (normalintrsts_bootcomplete):** This status is set if the boot operation gets terminated.
13	0h	**normalintrsts_rcvbootack (normalintrsts_rcvbootack):** This status is set if the boot acknowledge is received from device.
12	0h	**normalintrsts_retuningevent (normalintrsts_retuningevent):** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1.
11	0h	**normalintrsts_intc (normalintrsts_intc):** This status is set if INT_C is enabled and INT_C# pin is in low level. It is cleared by resetting the INT_C interrupt factor.
10	0h	**normalintrsts_intb (normalintrsts_intb):** This status is set if INT_B is enabled and INT_B# pin is in low level. It is cleared by resetting
9	0h	**normalintrsts_inta (normalintrsts_inta):** This status is set if INT_A is enabled and INT_A# pin is in low level. It is cleared by resetting
8	0h	**normalintrsts_cardintsts (normalintrsts_cardintsts):** This status is set to generate Card Interrupt. '0' No Card Interrupt, '1' Generate Card Interrupt
7	0h	**normalintrsts_cardremsts (normalintrsts_cardremsts):** This status is set if the Card Inserted in the Present State register changes from 1 to 0.
6	0h	**normalintrsts_cardinssts (normalintrsts_cardinssts):** This status is set if the Card Inserted in the Present State register changes from 0 to 1.
5	0h	**normalintrsts_bufrdready (normalintrsts_bufrdready):** This status is set if the Buffer Read Enable changes from 0 to 1.
4	0h	**normalintrsts_bufwrready (normalintrsts_bufwrready):** This status is set if the Buffer Write Enable changes from 0 to 1.



Bit Range	Default & Access	Field Name (ID): Description
3	0h	**normalintrsts_dmainterrupt (normalintrsts_dmainterrupt):** This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size regiser.
2	0h	**normalintrsts_blkgapevent (normalintrsts_blkgapevent):** If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set.
1	0h	**normalintrsts_xfercomplete (normalintrsts_xfercomplete):** This bit is set when a read / write transaction is completed.
0	0h	**normalintrsts_cmdcomplete (normalintrsts_cmdcomplete):** This bit is set when we get the end bit of the command response.

20.5.23 ErrorInterruptStatus_Register (errorintrsts)—Offset 32h

This register gives the status of the error interrupts

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h	**errorintrsts_hosterror (errorintrsts_hosterror):** Occurs when detecting Host ERROR
11:10	0h RO	Reserved.
9	0h	**errorintrsts_admaerror (errorintrsts_admaerror):** This bit is set when the Host Controller detects errors during ADMA based data transfer.
8	0h	**errorintrsts_autocmderror (errorintrsts_autocmderror):** This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1.
7	0h	**errorintrsts_currlimiterror (errorintrsts_currlimiterror):** If this bit is 1, it means that the HC is not supplying power to SD card due to some failure.Reading 0 means that the HC is supplying power and no error has occurred.
6	0h	**errorintrsts_dataendbiterror (errorintrsts_dataendbiterror):** Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status.

Bit Range	Default & Access	Field Name (ID): Description
5	0h	**errorintrsts_datacrcerror (errorintrsts_datacrcerror):** Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 010.
4	0h	**errorintrsts_datatimeouterror (errorintrsts_datatimeouterror):** This status is set if Data Timeout error occurs.
3	0h	**errorintrsts_cmdindexerror (errorintrsts_cmdindexerror):** Occurs if a Command Index error occurs in the Command Response.
2	0h	**errorintrsts_cmdendbiterror (errorintrsts_cmdendbiterror):** Occurs when detecting that the end bit of a command response is 0.
1	0h	**errorintrsts_cmdcrcerror (errorintrsts_cmdcrcerror):** This bit is set when Command CRC Error is generated. '0' No Error, '1' CRC Error
0	0h	**errorintrsts_cmdtimeouterror (errorintrsts_cmdtimeouterror):** This bit is set if no response is returned within 64 SDCLK cycles from the end bit of the command.

20.5.24 Normal Interrupt Status Enable Register (normalintrstsena)—Offset 34h

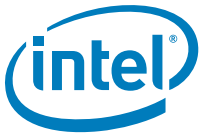
This register is used to enable the normal interrupt status register fields

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h	**normalintrsts_enableregbit15 (normalintrsts_enableregbit15):** The HC shall control error Interrupts using the Error Interrupt Status Enable register.
14	0h	**normalintrsts_enableregbit14 (normalintrsts_enableregbit14):** This status is set if the boot operation gets terminated.
13	0h	**normalintrsts_enableregbit13 (normalintrsts_enableregbit13):** This status is set if the boot acknowledge is received from device.
12	0h	**normalintrsts_enableregbit12 (normalintrsts_enableregbit12):** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1.



Bit Range	Default & Access	Field Name (ID): Description
11	0h	**normalintrsts_enableregbit11 (normalintrsts_enableregbit11):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System.
10	0h	**normalintrsts_enableregbit10 (normalintrsts_enableregbit10):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System.
9	0h	**normalintrsts_enableregbit9 (normalintrsts_enableregbit9):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System.
8	0h	**sdhcregset_cardintstsena (sdhcregset_cardintstsena):** If this bit is set to 0, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1.
7	0h	**sdhcregset_cardremstsena (sdhcregset_cardremstsena):** This status is set if the Card Inserted in the Present State register changes from 1 to 0.
6	0h	**sdhcregset_cardinsstsena (sdhcregset_cardinsstsena):** This status is set if the Card Inserted in the Present State register changes from 0 to 1.
5	0h	**normalintrsts_enableregbit5 (normalintrsts_enableregbit5):** This status is set if the Buffer Read Enable changes from 0 to 1.
4	0h	**normalintrsts_enableregbit4 (normalintrsts_enableregbit4):** This status is set if the Buffer Write Enable changes from 0 to 1.
3	0h	**normalintrsts_enableregbit3 (normalintrsts_enableregbit3):** This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size regiser.
2	0h	**normalintrsts_enableregbit2 (normalintrsts_enableregbit2):** If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set.
1	0h	**normalintrsts_enableregbit1 (normalintrsts_enableregbit1):** This bit is set when a read / write transaction is completed.
0	0h	**normalintrsts_enableregbit0 (normalintrsts_enableregbit0):** This bit is set when we get the end bit of the command response.

20.5.25 Error Interrupt Status Enable Register (errorintrstsena)—Offset 36h

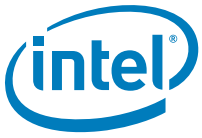
This register is used to enable the Error Interrupt Status register fields

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h	**errorintrsts_enableregbit12 (errorintrsts_enableregbit12):** Occurs when detecting ERROR in m_hresp(dma transaction)
11	0h RO	Reserved.
10	0h	**errorintrsts_enableregbit10 (errorintrsts_enableregbit10):** This status is set if INT_B is enabled and INT_B# pin is in low level. It is cleared by resetting
9	0h	**errorintrsts_enableregbit9 (errorintrsts_enableregbit9):** This bit is set when the Host Controller detects errors during ADMA based data transfer.
8	0h	**errorintrsts_enableregbit8 (errorintrsts_enableregbit8):** This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1.
7	0h	**errorintrsts_enableregbit7 (errorintrsts_enableregbit7):** If this bit is 1, it means that the HC is not supplying power to SD card due to some failure.Reading 0 means that the HC is supplying power and no error has occurred.
6	0h	**errorintrsts_enableregbit6 (errorintrsts_enableregbit6):** Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status.
5	0h	**errorintrsts_enableregbit5 (errorintrsts_enableregbit5):** Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 010.
4	0h	**errorintrsts_enableregbit4 (errorintrsts_enableregbit4):** This status is set if Data Timeout error occurs.
3	0h	**errorintrsts_enableregbit3 (errorintrsts_enableregbit3):** Occurs if a Command Index error occurs in the Command Response.
2	0h	**errorintrsts_enableregbit2 (errorintrsts_enableregbit2):** Occurs when detecting that the end bit of a command response is 0.
1	0h	**errorintrsts_enableregbit1 (errorintrsts_enableregbit1):** This bit is set when Command CRC Error is generated.
0	0h	**errorintrsts_enableregbit0 (errorintrsts_enableregbit0):** This bit is set if no response is returned within 64 SDCLK cycles from the end bit of the command.



20.5.26 Normal Interrupt Signal Enable Register (normalintrsigena)—Offset 38h

This register is used to enable the Normal Interrupt Signal register

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h	**normalintrsts_enableregbit15 (normalintrsts_enableregbit15):** The HD shall control error Interrupts using the Error Interrupt Signal Enable register.
14	0h	**normalintrsts_enableregbit14 (normalintrsts_enableregbit14):** Boot Terminate Interrupt Signal Enable
13	0h	**normalintrsts_enableregbit13 (normalintrsts_enableregbit13):** Boot ack rcv Signal Enable
12	0h	**normalintrsts_enableregbit12 (normalintrsts_enableregbit12):** Re-Tuning Event Signal Enable
11	0h	**normalintrsts_enableregbit11 (normalintrsts_enableregbit11):** INT_C Signal Enable
10	0h	**normalintrsts_enableregbit10 (normalintrsts_enableregbit10):** INT_B Signal Enable
9	0h	**normalintrsts_enableregbit9 (normalintrsts_enableregbit9):** INT_A Signal Enable
8	0h	**sdhcregset_cardintstsena (sdhcregset_cardintstsena):** Card Interrupt Signal Enable
7	0h	**sdhcregset_cardremstsena (sdhcregset_cardremstsena):** Card Removal Signal Enable
6	0h	**sdhcregset_cardinsstsena (sdhcregset_cardinsstsena):** Card Insertion Signal Enable
5	0h	**normalintrsts_enableregbit5 (normalintrsts_enableregbit5):** Buffer Read Ready Signal Enable
4	0h	**normalintrsts_enableregbit4 (normalintrsts_enableregbit4):** Buffer Write Ready Signal Enable
3	0h	**normalintrsts_enableregbit3 (normalintrsts_enableregbit3):** DMA Interrupt Signal Enable
2	0h	**normalintrsts_enableregbit2 (normalintrsts_enableregbit2):** Block Gap Event Signal Enable

Bit Range	Default & Access	Field Name (ID): Description
1	0h	**normalintrsts_enableregbit1 (normalintrsts_enableregbit1):** Transfer Complete Signal Enable
0	0h	**normalintrsts_enableregbit0 (normalintrsts_enableregbit0):** Command Complete Signal Enable

20.5.27 Error Interrupt Signal Enable Register (errorintrsigena)—Offset 3Ah

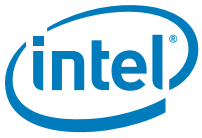
This register is used to enable Error Interrupt Signal register

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h	**errorintrsig_enableregbit12 (errorintrsig_enableregbit12):** Target Response Error Signal Enable
11	0h RO	Reserved.
10	0h	**errorintrsig_enableregbit10 (errorintrsig_enableregbit10):** Tuning Error Signal Enable
9	0h	**errorintrsig_enableregbit9 (errorintrsig_enableregbit9):** ADMA Error Signal Enable
8	0h	**errorintrsig_enableregbit8 (errorintrsig_enableregbit8):** Auto CMD Error Signal Enable
7	0h	**errorintrsig_enableregbit7 (errorintrsig_enableregbit7):** Current Limit Error Signal Enable
6	0h	**errorintrsig_enableregbit6 (errorintrsig_enableregbit6):** Data End Bit Error Signal Enable
5	0h	**errorintrsig_enableregbit5 (errorintrsig_enableregbit5):** Data CRC Error Signal Enable
4	0h	**errorintrsig_enableregbit4 (errorintrsig_enableregbit4):** Data Timeout Error Signal Enable
3	0h	**errorintrsig_enableregbit3 (errorintrsig_enableregbit3):** Command Index Error Signal Enable
2	0h	**errorintrsig_enableregbit2 (errorintrsig_enableregbit2):** Command End Bit Error Signal Enable



Bit Range	Default & Access	Field Name (ID): Description
1	0h	**errorintrsig_enableregbit1 (errorintrsig_enableregbit1):** Command CRC Error Signal Enable
0	0h	**errorintrsig_enableregbit0 (errorintrsig_enableregbit0):** Command Timeout Error Signal Enable

20.5.28 Auto CMD12 Error Status Register (autocmderrsts)—Offset 3Ch

This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD 23

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h	**autocmderrsts_nexterror (autocmderrsts_nexterror):** Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 error(D04- D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23
6:5	0h RO	Reserved.
4	0h	**autocmderrsts_indexerror (autocmderrsts_indexerror):** Occurs if the Command Index error occurs in response to a command.
3	0h	**autocmderrsts_endbiterror (autocmderrsts_endbiterror):** Occurs when detecting that the end bit of command response is 0.
2	0h	**autocmderrsts_crcerror (autocmderrsts_crcerror):** Occurs when detecting a CRC error in the command response.
1	0h	**autocmderrsts_timeouterror (autocmderrsts_timeouterror):** Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command.
0	0h	**autocmderrsts_notexecerror (autocmderrsts_notexecerror):** Setting this bit to 1 means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error.

20.5.29 Host Control2 Register (hostcontrol2)—Offset 3Eh

This register is used to program UHS Select Mode,UHS Select Mode,Driver Strength Select,Execute Tuning,Sampling Clock Select,Asynchronous Interrupt Enable and Preset value enable

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

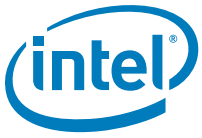
Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h	**hostctrl2_presetvalueenable (hostctrl2_presetvalueenable):** This bit enables the functions defined in the Preset Value registers.
14	0h	**hostctrl2_asynchintrenable (hostctrl2_asynchintrenable):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register.
13:10	0h RO	Reserved.
9	0h	**hostctrl2_driverstrength_bit2 (hostctrl2_driverstrength_bit2):** This is the programmed Drive STrength output and Bit[2] of the sdhccore_drivestrength value.
8	0h RO	Reserved.
7	0h	**hostctrl2_samplingclkselect (hostctrl2_samplingclkselect):** This bit is set by tuning procedure when Execute Tuning is cleared.
6	0h	**hostctrl2_executetuning (hostctrl2_executetuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed.
5:4	0h	**hostctrl2_driverstrength (hostctrl2_driverstrength):** Host Controller output driver in 1.8V signaling is selected by this bit.
3	0h	**hostctrl2_1p8vsignallingena (hostctrl2_1p8vsignallingena):** This bit controls voltage regulator for I/O cell.
2:0	0h	**hostctrl2_uhsmodeselect (hostctrl2_uhsmodeselect):** This field is used to select one of UHS-I modes and effective when 1.8V Signaling Enable is set to 1.

20.5.30 Capabilities Register (capabilities)—Offset 40h

This register provides the host driver with information specific to the host controller implementation

Access Method



Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

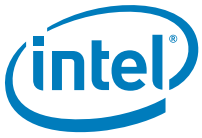
Bit Range	Default & Access	Field Name (ID): Description
63	0h	**corecfg_hs400support (corecfg_hs400support):** This field indicates whether HS400 is supported or not.
62:58	0h RO	Reserved.
57	0h	**corecfg_spiblkmode (corecfg_spiblkmode):** This field indicates whether SPI Block Mode is supported or not.
56	0h	**corecfg_spisupport (corecfg_spisupport):** This field indicates whether SPI Mode is supported or not.
55:48	0h	**corecfg_clockmultiplier (corecfg_clockmultiplier):** This field indicates clock multiplier value of programmable clock generator.
47:46	0h	**corecfg_retuningmodes (corecfg_retuningmodes):** This field defines the re-tuning capability of a Host Controller.
45	0h	**corecfg_tuningforsdr50 (corecfg_tuningforsdr50):** If this bit is set to 1, this Host Controller requires tuning to operate SDR50.
44	0h RO	Reserved.
43:40	0h	**corecfg_retuningtimercnt (corecfg_retuningtimercnt):** This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3.
39	0h	**corecfg_type4support (corecfg_type4support):** This bit indicates support of Type 4 Driver.
38	0h	**corecfg_ddriversupport (corecfg_ddriversupport):** This bit indicates support of Driver Type D for 1.8 Signaling.
37	0h	**corecfg_cdriversupport (corecfg_cdriversupport):** This bit indicates support of Driver Type C for 1.8 Signaling.
36	0h	**corecfg_adriversupport (corecfg_adriversupport):** This bit indicates support of Driver Type A for 1.8 Signaling.
35	0h RO	Reserved.
34	0h	**corecfg_ddr50support (corecfg_ddr50support):** This bit indicates whether DDR50 is supported.
33	0h	**corecfg_sdr104support (corecfg_sdr104support):** This bit indicates whether SDR104 is supported.SDR104 requires tuning.
32	0h	**corecfg_sdr50support (corecfg_sdr50support):** This bit indicates whether SDR50 is supported.
31:30	0h	**corecfg_slottype (corecfg_slottype):** This field indicates usage of a slot by a specific Host System
29	0h	**corecfg_asynchintrsupport (corecfg_asynchintrsupport):** Asynchronous Interrupt Support

Bit Range	Default & Access	Field Name (ID): Description
28	0h	**corecfg_64bitsupport (corecfg_64bitsupport):** This bit indicates whether the HC supports 64bit System Bus
27	0h RO	Reserved.
26	0h	**corecfg_1p8voltsupport (corecfg_1p8voltsupport):** This bit indicates whether the HC supports 1.8V.
25	0h	**corecfg_3p0voltsupport (corecfg_3p0voltsupport):** This bit indicates whether the HC supports 3.0V.
24	0h	**corecfg_3p3voltsupport (corecfg_3p3voltsupport):** This bit indicates whether the HC supports 3.3V.
23	0h	**corecfg_suspressupport (corecfg_suspressupport):** This bit indicates whether the HC supports Suspend/Resume functionality.
22	0h	**corecfg_sdmasupport (corecfg_sdmasupport):** This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly.
21	0h	**corecfg_highspeedsupport (corecfg_highspeedsupport):** This bit indicates whether the HC and the Host System support High Speed mode.
20	0h RO	Reserved.
19	0h	**corecfg_adma2support (corecfg_adma2support):** '0'ADMA2 Not Supported
18	0h	**corecfg_8bitsupport (corecfg_8bitsupport):** This bit indicates whether the Host Controller is capable of using 8-bit bus width mode.
17:16	0h	**corecfg_maxblklength (corecfg_maxblklength):** This value indicates the maximum block size that the HD can read and write to the buffer in the HC.
15:8	0h	**corecfg_baseclkfreq (corecfg_baseclkfreq):** 6-bit Base Clock Frequency
7	0h	**corecfg_timeoutclkunit (corecfg_timeoutclkunit):** This bit shows the unit of base clock frequency used to detect Data Timeout Error.
6	0h RO	Reserved.
5:0	0h	**corecfg_timeoutclkfreq (corecfg_timeoutclkfreq):** This bit shows the base clock frequency used to detect Data Timeout Error.

20.5.31 Maximum Current Capabilities Register (maxcurrentcap)—Offset 48h

This register indicates maximum current capability for each voltage

Access Method



Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:24	0h RO	Reserved.
23:16	0h	**corecfg_maxcurrent1p8v (corecfg_maxcurrent1p8v):** Maximum Current for 1.8V
15:8	0h	**corecfg_maxcurrent3p0v (corecfg_maxcurrent3p0v):** Maximum Current for 3.0V
7:0	0h	**corecfg_maxcurrent3p3v (corecfg_maxcurrent3p3v):** Maximum Current for 3.3V

20.5.32 Force Event REGISTER for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus)—Offset 50h

This register is not physically implemented, rather it is an address where Auto CMD Error Status register can be written.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h	**forcecmdnotissuedbyautocmd12err (forcecmdnotissuedbyautocmd12err):** Force Event for Command Not Issued by AUTO CMD12 Error
6:5	0h RO	Reserved.
4	0h	**forceautocmdindexerr (forceautocmdindexerr):** Force Event for AUTO CMD Index Error
3	0h	**forceautocmdendbiterr (forceautocmdendbiterr):** Force Event for AUTO CMD End Bit Error
2	0h	**forceautocmdcrcerr (forceautocmdcrcerr):** Force Event for AUTO CMD Timeout Error
1	0h	**forceautocmdtimeouterr (forceautocmdtimeouterr):** Force Event for AUTO CMD Timeout Error
0	0h	**forceautocmdnotexec (forceautocmdnotexec):** Force Event for AUTO CMD12 Not Executed

20.5.33 Force Event Register for Error Interrupt Status (forceeventforerrintsts)—Offset 52h

This register is not physically implemented, rather it is an address where Error Interrupt Status register can be written.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

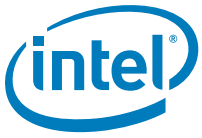
Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h	**forcetuningerr (forcetuningerr):** Force Event for Tuning Error
9	0h	**forceadmaerr (forceadmaerr):** Force Event for ADMA Error'0' no interrupt, '1' interrupt generated
8	0h	**forceautocmderr (forceautocmderr):** Force Event for Auto CMD Error '0' no interrupt, '1' interrupt generated
7	0h	**forcecurrlimerr (forcecurrlimerr):** Force Event for Current Limit Error '0' no interrupt, '1' interrupt generated
6	0h	**forcedatendbiterr (forcedatendbiterr):** Force Event for Data End Bit Error. '0' no interrupt, '1' interrupt generated
5	0h	**forcedatcrcerr (forcedatcrcerr):** Force Event for Data CRC Error
4	0h	**forcedattimeouterr (forcedattimeouterr):** Force Event for Data Timeout Error '0' no interrupt, '1' interrupt generated
3	0h	**forcecmdindexerr (forcecmdindexerr):** Force Event for Command Index Error
2	0h	**forcecmdendbiterr (forcecmdendbiterr):** Force Event for Command End Bit Error '0' no interrupt, '1' interrupt generated
1	0h	**forcecmdcrcerr (forcecmdcrcerr):** Force Event for Command CRC Error
0	0h	**forcecmdtimeouterr (forcecmdtimeouterr):** Force Event for CMD Timeout Error '0' No interrupt, '1' interrupt generated

20.5.34 ADMA Error Status Register (admaerrsts)—Offset 54h

When the ADMA Error interrupt occur, this register holds the ADMA State in ADMA Error States field and ADMA System Address holds address around the error descriptor

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**



Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h	**admaerrsts_admalenmismatcherr (admaerrsts_admalenmismatcherr):** ADMA Length Mismatch Error
1:0	0h	**admaerrsts_admaerrorstate (admaerrsts_admaerrorstate):** This field indicates the state of ADMA when error is occurred during ADMA data transfer.

20.5.35 ADMA System Address Register0&1 (admasysaddr01)—Offset 58h

This register contains the physical address used for ADMA data transfer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**adma_sysaddress0 (adma_sysaddress0):** This register holds byte address of executing command of the Descriptor table.

20.5.36 ADMA System Address Register1 (admasysaddr2)—Offset 5Ch

This register contains the physical address used for ADMA data transfer

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**adma_sysaddress2 (adma_sysaddress2):** This register holds byte address of executing command of the Descriptor table.

20.5.37 ADMA System Address Register1 (admasysaddr3)—Offset 5Eh

This register contains the physical address used for ADMA data transfer

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**adma_sysaddress3 (adma_sysaddress3):** This register holds byte address of executing command of the Descriptor table.

20.5.38 Boot Timeout Control Register (boottimeoutcnt)—Offset 70h

This is used to program the boot timeout value counter

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**boot_timeoutcnt (boot_timeoutcnt):** This value determines the interval by which DAT line time-outs are detected during boot operation for eMMC4.4 card.

20.5.39 Slot Interrupt Status Register (slotintrsts)—Offset FCh

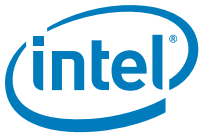
This register is used to read the interrupt signal for each slot.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h	**sdhchostif_slotintrsts (sdhchostif_slotintrsts):** These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot.

20.5.40 Host Controller Version Register (hostcontrollerver)—Offset FEh

This register is used to read the vendor version number and specification version number

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 1002h

Bit Range	Default & Access	Field Name (ID): Description
15:8	10h	**SDHC_VENVERNUM (SDHC_VENVERNUM):** This status is reserved for the vendor version number.
7:0	2h	**SpecificationVersionNumber (SpecificationVersionNumber):** This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version.

20.6 Registers Summary

Table 20-6. Summary of soc_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	(DEVVENDID)—Offset 0h	8086h
4h	7h	(STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	(REVCLASSCODE)—Offset 8h	8050100h
Ch	Fh	(CLLATHEADERBIST)—Offset Ch	0h
10h	13h	(BAR)—Offset 10h	4h
14h	17h	(BAR_HIGH)—Offset 14h	0h
18h	1Bh	(BAR1)—Offset 18h	4h
1Ch	1Fh	(BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	(SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	(EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	(CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	(INTERRUPTREG)—Offset 3Ch	0h
80h	83h	(POWERCAPID)—Offset 80h	39001h
84h	87h	(PMECTRLSTATUS)—Offset 84h	8h

Table 20-6. Summary of soc_regs_wrapper Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
90h	93h	(PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	(DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	(D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	8041h
9Ch	9Fh	(DEVICE_IDLE_POINTER_REG)—Offset 9Ch	81C1h
A0h	A3h	(D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	290800h

20.6.1 (DEVVENDID)—Offset 0h

DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**DEVICEID**
15:0	8086h RO	**VENDORID**

20.6.2 (STATUSCOMMAND)—Offset 4h

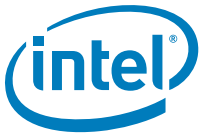
STATUSCOMMAND- Status and Command

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0**
29	0h RW/1C	**RMA**
28	0h RW/1C	**RTA**
27:21	0h RO	**Reserved1**
20	1h RO	**CAPLIST**



Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**INTR_STATUS**
18:16	0h RO	**Reserved2**
15:11	0h RO	**Reserved3**
10	0h RW	**INTR_DISABLE**
9	0h RO	**Reserved4**
8	0h RW	**SERR_ENABLE**
7:3	0h RO	**Reserved5**
2	0h RW	**BME**
1	0h RW	**MSE**
0	0h RO	**Reserved6**

20.6.3 (REVCLASSCODE)—Offset 8h

REVCLASSCODE - Revision ID and Class Code

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 8050100h

Bit Range	Default & Access	Field Name (ID): Description
31:8	80501h RO	**CLASS_CODES**
7:0	0h RO	**RID**

20.6.4 (CLLATHEADERBIST)—Offset Ch

CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved0**
23	0h RO	**MULFNDEV**
22:16	0h RO	**HEADERTYPE**
15:8	0h RO	**LATTIMER**
7:0	0h RW	**CACHELINE_SIZE**

20.6.5 (BAR)—Offset 10h

BAR -Base Address Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR**
11:4	0h RO	**SIZEINDICATOR**
3	0h RO	**PREFETCHABLE**
2:1	2h RO	**TYPE**
0	0h RO	**MESSAGE_SPACE**

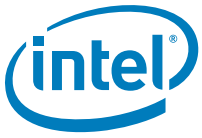
20.6.6 (BAR_HIGH)—Offset 14h

BAR -Base Address Register High

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR_HIGH**

20.6.7 (BAR1)—Offset 18h

BAR1 -Base Address Register1

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR1**
11:4	0h RO	**SIZEINDICATOR1**
3	0h RO	**PREFETCHABLE1**
2:1	2h RO	**TYPE1**
0	0h RO	**MESSAGE_SPACE1**

20.6.8 (BAR1_HIGH)—Offset 1Ch

BAR1 -Base Address Register1 High

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR1_HIGH**

20.6.9 (SUBSYSTEMID)—Offset 2Ch

SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID**
15:0	0h RW/O	**SUBSYSTEMVENDORID**

20.6.10 (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE**

20.6.11 (CAPABILITYPTR)—Offset 34h

CAPABILITYPTR - Capabilities Pointer

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

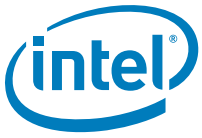
Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved0**
7:0	80h RO	**CAPPTR_POWER**

20.6.12 (INTERRUPTREG)—Offset 3Ch

INTERRUPTREG - Interrupt Register

Access Method



Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT**
23:16	0h RO	**MIN_GNT**
15:12	0h RO	**Reserved0**
11:8	0h RO	**INTPIN**
7:0	0h RW	**INTLINE**

20.6.13 (POWERCAPID)—Offset 80h

POWERCAPID - PowerManagement Capability ID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 39001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**PMESUPPORT**
26:19	0h RO	**Reserved0**
18:16	3h RO	**VERSION**
15:8	90h RO	**NXTCAP**
7:0	1h RO	**POWER_CAP**

20.6.14 (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved0**
15	0h RW/1C	**PMESTATUS**
14:9	0h RO	**Reserved1**
8	0h RW	**PMEENABLE**
7:4	0h RO	**Reserved2**
3	1h RO	**NO_SOFT_RESET**
2	0h RO	**Reserved3**
1:0	0h RW	**POWERSTATE**

20.6.15 (PCIDEVIDLE_CAP_RECORD)—Offset 90h

PCI DEVICE IDLE CAPABILITY RECORD

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP**
27:24	0h RO	**REVID**
23:16	14h RO	**CAP_LENGTH**
15:8	0h RO	**NEXT_CAP**
7:0	9h RO	**CAPID**

20.6.16 (DEVID_VEND_SPECIFIC_REG)—Offset 94h

DEVID VENDOR SPECIFIC REG

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH**
19:16	0h RO	**VSEC_REV**
15:0	10h RO	**VSECID**

20.6.17 (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

SW LTR Update MMIO Location Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 8041h

Bit Range	Default & Access	Field Name (ID): Description
31:4	804h RO	**SW_LAT_DWORD_OFFSET**
3:1	0h RO	**SW_LAT_BAR_NUM**
0	1h RO	**SW_LAT_VALID**

20.6.18 (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 81C1h

Bit Range	Default & Access	Field Name (ID): Description
31:4	81Ch RO	**DWORD_OFFSET**
3:1	0h RO	**BAR_NUM**
0	1h RO	**VALID**

20.6.19 (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

DEVICE PG CONFIG

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 0

Default: 290800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved0**
21	1h RW	**HAE**
20	0h RO	**Reserved1**
19	1h RW	**SLEEP_EN**
18	0h RW	**PGE**
17	0h RW	**I3_ENABLE**
16	1h RW	**PMCRE**
15:13	0h RO	**Reserved2**
12:10	2h RW/O	**POW_LAT_SCALE**
9:0	0h RW/O	**POW_LAT_VALUE**

20.7 Registers Summary

Table 20-7. Summary of SDHOST_OCP Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	SDMA System Address Register/Argument2 Register (sdmasysaddr)—Offset 0h	0h
4h	5h	BlockSize Register (blocksize)—Offset 4h	0h
6h	7h	BlockCount Register (blockcount)—Offset 6h	0h
8h	Bh	Argument1 Register (argument1)—Offset 8h	0h
Ch	Dh	TransferMode Register (transfermode)—Offset Ch	0h
Eh	Fh	Command Register (command)—Offset Eh	0h
10h	13h	Response Register (response01)—Offset 10h	0h
14h	15h	Response Register (response2)—Offset 14h	0h
16h	17h	Response Register (response3)—Offset 16h	0h

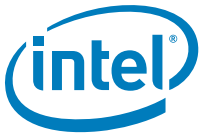


Table 20-7. Summary of SDHOST_OCP Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
18h	19h	Response Register (response4)—Offset 18h	0h
1Ah	1Bh	Response Register (response5)—Offset 1Ah	0h
1Ch	1Dh	Response Register (response6)—Offset 1Ch	0h
1Eh	1Fh	Response Register (response7)—Offset 1Eh	0h
20h	23h	Buffer DataPort Register (dataport)—Offset 20h	0h
28h	28h	HostControl1 Register (hostcontrol1)—Offset 28h	0h
29h	29h	PowerControl Register (powercontrol)—Offset 29h	0h
2Ah	2Ah	BlockGapControl Register (blockgapcontrol)—Offset 2Ah	80h
2Bh	2Bh	Wakeup Control Register (wakeupcontrol)—Offset 2Bh	0h
2Ch	2Dh	Clock Control Register (clockcontrol)—Offset 2Ch	0h
2Eh	2Eh	Timeout Control Register (timeoutcontrol)—Offset 2Eh	0h
2Fh	2Fh	Software Reset Register (softwarereset)—Offset 2Fh	0h
30h	31h	Normal Interrupt Status Register (normalintrsts)—Offset 30h	0h
32h	33h	ErrorInterruptStatus_Register (errorintrsts)—Offset 32h	0h
34h	35h	Normal Interrupt Status Enable Register (normalintrstsena)—Offset 34h	0h
36h	37h	Error Interrupt Status Enable Register (errorintrstsena)—Offset 36h	0h
38h	39h	Normal Interrupt Signal Enable Register (normalintrsigena)—Offset 38h	0h
3Ah	3Bh	Error Interrupt Signal Enable Register (errorintrsigena)—Offset 3Ah	0h
3Ch	3Dh	Auto CMD12 Error Status Register (autocmderrsts)—Offset 3Ch	0h
3Eh	3Fh	Host Control2 Register (hostcontrol2)—Offset 3Eh	0h
40h	47h	Capabilities Register (capabilities)—Offset 40h	0h
48h	4Fh	Maximum Current Capabilities Register (maxcurrentcap)—Offset 48h	0h
50h	51h	Force Event REGISTER for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus)—Offset 50h	0h
52h	53h	Force Event Register for Error Interrupt Status (forceeventforerrintsts)—Offset 52h	0h
54h	54h	ADMA Error Status Register (admaerrsts)—Offset 54h	0h
58h	5Bh	ADMA System Address Register0&1 (admasysaddr01)—Offset 58h	0h
5Ch	5Dh	ADMA System Address Register1 (admasysaddr2)—Offset 5Ch	0h
5Eh	5Fh	ADMA System Address Register1 (admasysaddr3)—Offset 5Eh	0h
70h	73h	Boot Timeout Control Register (boottimeoutcnt)—Offset 70h	0h
FCh	FDh	Slot Interrupt Status Register (slotintrsts)—Offset FCh	0h
FEh	FFh	Host Controller Version Register (hostcontrollerver)—Offset FEh	1002h

20.7.1 SDMA System Address Register/Argument2 Register (sdmasysaddr)—Offset 0h

This register contains concatinates reg_sdmasysaddrlo and reg_sdmasysaddrhi

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**sdma_sysaddress (sdma_sysaddress):** refer to reg_sdmasysaddrlo and reg_sdmasysaddrhi

20.7.2 BlockSize Register (blocksize)—Offset 4h

This register is used to configure the number of bytes in a data block

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14:12	0h	**sdma_bufboundary (sdma_bufboundary):** This Field specifies DMA Buffer Boundary
11:0	0h	**xfer_blocksize (xfer_blocksize):** This Field specifies Block Size for Data Transfers

20.7.3 BlockCount Register (blockcount)—Offset 6h

This register is used to configure the number of data blocks

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**xfer_blockcount (xfer_blockcount):** This Register specifies Block Size for Data Transfers

20.7.4 Argument1 Register (argument1)—Offset 8h

This register contains concatinates argument1lo and argument1hi registers to result SD Command Argument

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**command_argument1 (command_argument1):** refer t oreg_argument1lo and reg_argument1hi.

20.7.5 TransferMode Register (transfermode)—Offset Ch

This register is used to control the operations of data transfers

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5	0h	**xfermode_multiblksel (xfermode_multiblksel):** This bit enables multiple block data transfers.
4	0h	**xfermode_dataxferdir (xfermode_dataxferdir):** This bit defines the direction of data transfers.
3:2	0h	**xfermode_autocmdena (xfermode_autocmdena):** This field determines use of auto command functions.
1	0h	**xfermode_blkcntena (xfermode_blkcntena):** This bit is used to enable the Block count register, which is only relevant for multiple block transfers
0	0h	**xfermode_dmaenable (xfermode_dmaenable):** '1' to enable DMA,

20.7.6 Command Register (command)—Offset Eh

This register is used to program the Command for host controller

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:8	0h	**command_cmdindex (command_cmdindex):** This bit shall be set to the command number (CMD0-63, ACMD0-63).
7:6	0h	**command_cmdtype (command_cmdtype):** This bit is used for select different command types.
5	0h	**command_datapresent (command_datapresent):** This bit is used to checking whether data present or not.
4	0h	**command_indexchkena (command_indexchkena):** This bit is used to enable/disable Command Index checking.
3	0h	**command_crcchkena (command_crcchkena):** This bit is used to enable/disable CRC checking.
2	0h RO	Reserved.
1:0	0h	**command_responsetype (command_responsetype):** Response Type Select.

20.7.7 Response Register (response01)—Offset 10h

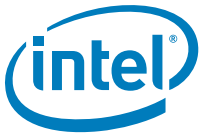
This register is used to store responses from SD Cards (concatinates response0 & response1 registers)

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit



20.7.8 Response Register (response2)—Offset 14h

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.7.9 Response Register (response3)—Offset 16h

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.7.10 Response Register (response4)—Offset 18h

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.7.11 Response Register (response5)—Offset 1Ah

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.7.12 Response Register (response6)—Offset 1Ch

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.7.13 Response Register (response7)—Offset 1Eh

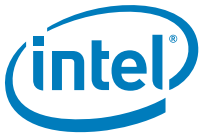
This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit



20.7.14 Buffer DataPort Register (dataport)—Offset 20h

This register is used to access internal buffer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**sdhcdmactrl_piobufrddata (sdhcdmactrl_piobufrddata):** The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

20.7.15 HostControl1 Register (hostcontrol1)—Offset 28h

This register is used to program DMA modes, LED Control, Data Transfer Width, High Speed Enable, Card detect test level and signal selection

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h	**hostctrl1_cdsigselect (hostctrl1_cdsigselect):** This bit selects source for card detection.
6	0h	**hostctrl1_cdtestlevel (hostctrl1_cdtestlevel):** This bit is used for indicating whether card is inserted or not.
5	0h	**hostctrl1_extdatawidth (hostctrl1_extdatawidth):** This bit controls 8-bit bus width mode for embedded device.
4:3	0h	**hostctrl1_dmaselect (hostctrl1_dmaselect):** One of supported DMA modes can be selected.
2	0h	**hostctrl1_highspeedena (hostctrl1_highspeedena):** This bit is used for setting speed mode.
1	0h	**hostctrl1_datawidth (hostctrl1_datawidth):** This bit selects the data width of the HC.
0	0h	**hostctrl1_ledcontrol (hostctrl1_ledcontrol):** This bit is used to caution the user not to remove the card while the SD card is being accessed.

20.7.16 PowerControl Register (powercontrol)—Offset 29h

This register is used to program the SD Bus power and voltage level

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h	**emmc_hwreset (emmc_hwreset):** Hardware reset signal is generated for eMMC card.
3:1	0h	**pwrctrl_sdbusvoltage (pwrctrl_sdbusvoltage):** By setting these bits, the HD selects the voltage level for the SD card.
0	0h	**pwrctrl_sdbuspower (pwrctrl_sdbuspower):** This bit is used detect whether power is on or off.

20.7.17 BlockGapControl Register (blockgapcontrol)—Offset 2Ah

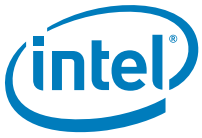
This register is used to program the block gap request, read wait control and interrupt at block gap

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h	**blkgapctrl_bootackena (blkgapctrl_bootackena):** To check for the boot acknowledge in boot operation.
6	0h	**blkgapctrl_altbootmode (blkgapctrl_altbootmode):** To start boot code access in alternative mode.
5	0h	**blkgapctrl_bootenable (blkgapctrl_bootenable):** To start boot code access. '0' To stop boot code access, '1' To start boot code access
4	0h	**blkgapctrl_spimode (blkgapctrl_spimode):** SPI mode enable bit. '0' SD Mode, '1' SPI Mode
3	0h	**blkgapctrl_interrupt (blkgapctrl_interrupt):** This bit is valid only in 4-bit mode of the SD card andselects a sample point in the interrupt cycle.
2	0h	**blkgapctrl_rdwaitctrl (blkgapctrl_rdwaitctrl):** The read wait function is optional for SD cards.



Bit Range	Default & Access	Field Name (ID): Description
1	0h	**blkgapctrl_continue (blkgapctrl_continue):** This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request.
0	0h	**blkgapctrl_stopatblkgap (blkgapctrl_stopatblkgap):** This bit is used to stop executing a transaction at the next block gap for non- DMA,SDMA and ADMA transfers.

20.7.18 Wakeup Control Register (wakeupcontrol)—Offset 2Bh

This register is used to program the wakeup functionality

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h	**wkupctrl_cardremoval (wkupctrl_cardremoval):** This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register.
1	0h	**wkupctrl_cardinsertion (wkupctrl_cardinsertion):** This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register.
0	0h	**wkupctrl_cardinterrupt (wkupctrl_cardinterrupt):** This bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt Status register.

20.7.19 Clock Control Register (clockcontrol)—Offset 2Ch

This register is used to program the Clock frequency select, generator select, Clock enable, Internal Clock state fields

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h	**clkctrl_sdclkfreqsel (clkctrl_sdclkfreqsel):** This register is used to select the frequency of the SDCLK pin.

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h	**clkctrl_sdclkfreqsel_upperbits (clkctrl_sdclkfreqsel_upperbits):** Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select
5	0h	**clkctrl_clkgensel (clkctrl_clkgensel):** This bit is used to select the clock generator mode in SDCLK Frequency Select.
4:3	0h RO	Reserved.
2	0h	**clkctrl_sdclkena (clkctrl_sdclkena):** This bit enables/disables SD Clock. '0' Disable, '1' Enable
1	0h	**sdhcclkgen_intclkstable_dsync (sdhcclkgen_intclkstable_dsync):** This bit is set to 1 when SD clock is stable after writing to Internal Clock Enable in this register to 1.
0	0h	**clkctrl_intclkena (clkctrl_intclkena):** This bit enables setting of internal clock.'0' Stop, '1' Oscillate

20.7.20 Timeout Control Register (timeoutcontrol)—Offset 2Eh

The register sets the Data Timeout counter value

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3:0	0h	**timeout_ctrvalue (timeout_ctrvalue):** This value determines the interval by which DAT line time-outs are detected.

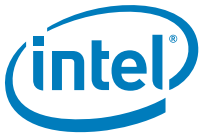
20.7.21 Software Reset Register (softwarereset)—Offset 2Fh

This register is used to program the software reset for data, command and for all.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h	**swreset_for_dat (swreset_for_dat):** Only part of data circuit is reset. '0' Work, '1' Reset
1	0h	**swreset_for_cmd (swreset_for_cmd):** Only part of command circuit is reset.'0' Work, '1' reset.
0	0h	**swreset_for_all (swreset_for_all):** If this bit is set to 1, the SD card shall reset itself and must be re initialized by the HD.

20.7.22 Normal Interrupt Status Register (normalintrsts)—Offset 30h

This register gives the status of all the interrupts

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h	**reg_errorintrsts (reg_errorintrsts):** This bit is set If any of the bits in the Error Interrupt Status Register are set.
14	0h	**normalintrsts_bootcomplete (normalintrsts_bootcomplete):** This status is set if the boot operation gets terminated.
13	0h	**normalintrsts_rcvbootack (normalintrsts_rcvbootack):** This status is set if the boot acknowledge is received from device.
12	0h	**normalintrsts_retuningevent (normalintrsts_retuningevent):** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1.
11	0h	**normalintrsts_intc (normalintrsts_intc):** This status is set if INT_C is enabled and INT_C# pin is in low level. It is cleared by resetting the INT_C interrupt factor.
10	0h	**normalintrsts_intb (normalintrsts_intb):** This status is set if INT_B is enabled and INT_B# pin is in low level. It is cleared by resetting
9	0h	**normalintrsts_inta (normalintrsts_inta):** This status is set if INT_A is enabled and INT_A# pin is in low level. It is cleared by resetting
8	0h	**normalintrsts_cardintsts (normalintrsts_cardintsts):** This status is set to generate Card Interrupt. '0' No Card Interrupt, '1' Generate Card Interrupt

Bit Range	Default & Access	Field Name (ID): Description
7	0h	**normalintrsts_cardremsts (normalintrsts_cardremsts):** This status is set if the Card Inserted in the Present State register changes from 1 to 0.
6	0h	**normalintrsts_cardinssts (normalintrsts_cardinssts):** This status is set if the Card Inserted in the Present State register changes from 0 to 1.
5	0h	**normalintrsts_bufrdready (normalintrsts_bufrdready):** This status is set if the Buffer Read Enable changes from 0 to 1.
4	0h	**normalintrsts_bufwrready (normalintrsts_bufwrready):** This status is set if the Buffer Write Enable changes from 0 to 1.
3	0h	**normalintrsts_dmainterrupt (normalintrsts_dmainterrupt):** This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size regiser.
2	0h	**normalintrsts_blkgapevent (normalintrsts_blkgapevent):** If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set.
1	0h	**normalintrsts_xfercomplete (normalintrsts_xfercomplete):** This bit is set when a read / write transaction is completed.
0	0h	**normalintrsts_cmdcomplete (normalintrsts_cmdcomplete):** This bit is set when we get the end bit of the command response.

20.7.23 ErrorInterruptStatus_Register (errorintrsts)—Offset 32h

This register gives the status of the error interrupts

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h	**errorintrsts_hosterror (errorintrsts_hosterror):** Occurs when detecting Host ERROR
11:10	0h RO	Reserved.
9	0h	**errorintrsts_admaerror (errorintrsts_admaerror):** This bit is set when the Host Controller detects errors during ADMA based data transfer.

Bit Range	Default & Access	Field Name (ID): Description
8	0h	**errorintrsts_autocmderror (errorintrsts_autocmderror):** This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1.
7	0h	**errorintrsts_currlimiterror (errorintrsts_currlimiterror):** If this bit is 1, it means that the HC is not supplying power to SD card due to some failure.Reading 0 means that the HC is supplying power and no error has occurred.
6	0h	**errorintrsts_dataendbiterror (errorintrsts_dataendbiterror):** Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status.
5	0h	**errorintrsts_datacrcerror (errorintrsts_datacrcerror):** Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 010.
4	0h	**errorintrsts_datatimeouterror (errorintrsts_datatimeouterror):** This status is set if Data Timeout error occurs.
3	0h	**errorintrsts_cmdindexerror (errorintrsts_cmdindexerror):** Occurs if a Command Index error occurs in the Command Response.
2	0h	**errorintrsts_cmdendbiterror (errorintrsts_cmdendbiterror):** Occurs when detecting that the end bit of a command response is 0.
1	0h	**errorintrsts_cmdcrcerror (errorintrsts_cmdcrcerror):** This bit is set when Command CRC Error is generated. '0' No Error, '1' CRC Error
0	0h	**errorintrsts_cmdtimeouterror (errorintrsts_cmdtimeouterror):** This bit is set if no response is returned within 64 SDCLK cycles from the end bit of the command.

20.7.24 Normal Interrupt Status Enable Register (normalintrstsena)—Offset 34h

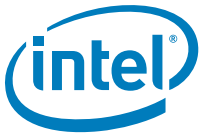
This register is used to enable the normal interrupt status register fields

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h	**normalintrsts_enableregbit15 (normalintrsts_enableregbit15):** The HC shall control error Interrupts using the Error Interrupt Status Enable register.
14	0h	**normalintrsts_enableregbit14 (normalintrsts_enableregbit14):** This status is set if the boot operation gets terminated.
13	0h	**normalintrsts_enableregbit13 (normalintrsts_enableregbit13):** This status is set if the boot acknowledge is received from device.
12	0h	**normalintrsts_enableregbit12 (normalintrsts_enableregbit12):** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1.
11	0h	**normalintrsts_enableregbit11 (normalintrsts_enableregbit11):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System.
10	0h	**normalintrsts_enableregbit10 (normalintrsts_enableregbit10):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System.
9	0h	**normalintrsts_enableregbit9 (normalintrsts_enableregbit9):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System.
8	0h	**sdhcregset_cardintstsena (sdhcregset_cardintstsena):** If this bit is set to 0, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1.
7	0h	**sdhcregset_cardremstsena (sdhcregset_cardremstsena):** This status is set if the Card Inserted in the Present State register changes from 1 to 0.
6	0h	**sdhcregset_cardinsstsena (sdhcregset_cardinsstsena):** This status is set if the Card Inserted in the Present State register changes from 0 to 1.
5	0h	**normalintrsts_enableregbit5 (normalintrsts_enableregbit5):** This status is set if the Buffer Read Enable changes from 0 to 1.
4	0h	**normalintrsts_enableregbit4 (normalintrsts_enableregbit4):** This status is set if the Buffer Write Enable changes from 0 to 1.
3	0h	**normalintrsts_enableregbit3 (normalintrsts_enableregbit3):** This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size regiser.
2	0h	**normalintrsts_enableregbit2 (normalintrsts_enableregbit2):** If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set.



Bit Range	Default & Access	Field Name (ID): Description
1	0h	**normalintrsts_enableregbit1 (normalintrsts_enableregbit1):** This bit is set when a read / write transaction is completed.
0	0h	**normalintrsts_enableregbit0 (normalintrsts_enableregbit0):** This bit is set when we get the end bit of the command response.

20.7.25 Error Interrupt Status Enable Register (errorintrstsena)—Offset 36h

This register is used to enable the Error Interrupt Status register fields

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h	**errorintrsts_enableregbit12 (errorintrsts_enableregbit12):** Occurs when detecting ERROR in m_hresp(dma transaction)
11	0h RO	Reserved.
10	0h	**errorintrsts_enableregbit10 (errorintrsts_enableregbit10):** This status is set if INT_B is enabled and INT_B# pin is in low level. It is cleared by resetting
9	0h	**errorintrsts_enableregbit9 (errorintrsts_enableregbit9):** This bit is set when the Host Controller detects errors during ADMA based data transfer.
8	0h	**errorintrsts_enableregbit8 (errorintrsts_enableregbit8):** This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1.
7	0h	**errorintrsts_enableregbit7 (errorintrsts_enableregbit7):** If this bit is 1, it means that the HC is not supplying power to SD card due to some failure.Reading 0 means that the HC is supplying power and no error has occurred.
6	0h	**errorintrsts_enableregbit6 (errorintrsts_enableregbit6):** Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status.
5	0h	**errorintrsts_enableregbit5 (errorintrsts_enableregbit5):** Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 010.

Bit Range	Default & Access	Field Name (ID): Description
4	0h	**errorintrsts_enableregbit4 (errorintrsts_enableregbit4):** This status is set if Data Timeout error occurs.
3	0h	**errorintrsts_enableregbit3 (errorintrsts_enableregbit3):** Occurs if a Command Index error occurs in the Command Response.
2	0h	**errorintrsts_enableregbit2 (errorintrsts_enableregbit2):** Occurs when detecting that the end bit of a command response is 0.
1	0h	**errorintrsts_enableregbit1 (errorintrsts_enableregbit1):** This bit is set when Command CRC Error is generated.
0	0h	**errorintrsts_enableregbit0 (errorintrsts_enableregbit0):** This bit is set if no response is returned within 64 SDCLK cycles from the end bit of the command.

20.7.26 Normal Interrupt Signal Enable Register (normalintrsigena)—Offset 38h

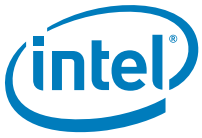
This register is used to enable the Normal Interrupt Signal register

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h	**normalintrsts_enableregbit15 (normalintrsts_enableregbit15):** The HD shall control error Interrupts using the Error Interrupt Signal Enable register.
14	0h	**normalintrsts_enableregbit14 (normalintrsts_enableregbit14):** Boot Terminate Interrupt Signal Enable
13	0h	**normalintrsts_enableregbit13 (normalintrsts_enableregbit13):** Boot ack rcv Signal Enable
12	0h	**normalintrsts_enableregbit12 (normalintrsts_enableregbit12):** Re-Tuning Event Signal Enable
11	0h	**normalintrsts_enableregbit11 (normalintrsts_enableregbit11):** INT_C Signal Enable
10	0h	**normalintrsts_enableregbit10 (normalintrsts_enableregbit10):** INT_B Signal Enable
9	0h	**normalintrsts_enableregbit9 (normalintrsts_enableregbit9):** INT_A Signal Enable



Bit Range	Default & Access	Field Name (ID): Description
8	0h	**sdhcregset_cardintstsena (sdhcregset_cardintstsena):** Card Interrupt Signal Enable
7	0h	**sdhcregset_cardremstsena (sdhcregset_cardremstsena):** Card Removal Signal Enable
6	0h	**sdhcregset_cardinsstsena (sdhcregset_cardinsstsena):** Card Insertion Signal Enable
5	0h	**normalintrsts_enableregbit5 (normalintrsts_enableregbit5):** Buffer Read Ready Signal Enable
4	0h	**normalintrsts_enableregbit4 (normalintrsts_enableregbit4):** Buffer Write Ready Signal Enable
3	0h	**normalintrsts_enableregbit3 (normalintrsts_enableregbit3):** DMA Interrupt Signal Enable
2	0h	**normalintrsts_enableregbit2 (normalintrsts_enableregbit2):** Block Gap Event Signal Enable
1	0h	**normalintrsts_enableregbit1 (normalintrsts_enableregbit1):** Transfer Complete Signal Enable
0	0h	**normalintrsts_enableregbit0 (normalintrsts_enableregbit0):** Command Complete Signal Enable

20.7.27 Error Interrupt Signal Enable Register (errorintrsigena)—Offset 3Ah

This register is used to enable Error Interrupt Signal register

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h	**errorintrsig_enableregbit12 (errorintrsig_enableregbit12):** Target Response Error Signal Enable
11	0h RO	Reserved.
10	0h	**errorintrsig_enableregbit10 (errorintrsig_enableregbit10):** Tuning Error Signal Enable

Bit Range	Default & Access	Field Name (ID): Description
9	0h	**errorintrsig_enableregbit9 (errorintrsig_enableregbit9):** ADMA Error Signal Enable
8	0h	**errorintrsig_enableregbit8 (errorintrsig_enableregbit8):** Auto CMD Error Signal Enable
7	0h	**errorintrsig_enableregbit7 (errorintrsig_enableregbit7):** Current Limit Error Signal Enable
6	0h	**errorintrsig_enableregbit6 (errorintrsig_enableregbit6):** Data End Bit Error Signal Enable
5	0h	**errorintrsig_enableregbit5 (errorintrsig_enableregbit5):** Data CRC Error Signal Enable
4	0h	**errorintrsig_enableregbit4 (errorintrsig_enableregbit4):** Data Timeout Error Signal Enable
3	0h	**errorintrsig_enableregbit3 (errorintrsig_enableregbit3):** Command Index Error Signal Enable
2	0h	**errorintrsig_enableregbit2 (errorintrsig_enableregbit2):** Command End Bit Error Signal Enable
1	0h	**errorintrsig_enableregbit1 (errorintrsig_enableregbit1):** Command CRC Error Signal Enable
0	0h	**errorintrsig_enableregbit0 (errorintrsig_enableregbit0):** Command Timeout Error Signal Enable

20.7.28 Auto CMD12 Error Status Register (autocmderrsts)—Offset 3Ch

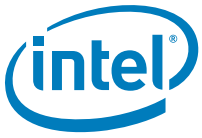
This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD 23

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h	**autocmderrsts_nexterror (autocmderrsts_nexterror):** Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 error(D04- D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23
6:5	0h RO	Reserved.



Bit Range	Default & Access	Field Name (ID): Description
4	0h	**autocmderrsts_indexerror (autocmderrsts_indexerror):** Occurs if the Command Index error occurs in response to a command.
3	0h	**autocmderrsts_endbiterror (autocmderrsts_endbiterror):** Occurs when detecting that the end bit of command response is 0.
2	0h	**autocmderrsts_crcerror (autocmderrsts_crcerror):** Occurs when detecting a CRC error in the command response.
1	0h	**autocmderrsts_timeouterror (autocmderrsts_timeouterror):** Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command.
0	0h	**autocmderrsts_notexecerror (autocmderrsts_notexecerror):** Setting this bit to 1 means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error.

20.7.29 Host Control2 Register (hostcontrol2)—Offset 3Eh

This register is used to program UHS Select Mode,UHS Select Mode,Driver Strength Select,Execute Tuning,Sampling Clock Select,Asynchronous Interrupt Enable and Preset value enable

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h	**hostctrl2_presetvalueenable (hostctrl2_presetvalueenable):** This bit enables the functions defined in the Preset Value registers.
14	0h	**hostctrl2_asynchintrenable (hostctrl2_asynchintrenable):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register.
13:10	0h RO	Reserved.
9	0h	**hostctrl2_driverstrength_bit2 (hostctrl2_driverstrength_bit2):** This is the programmed Drive STrength output and Bit[2] of the sdhccore_drivestrength value.
8	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7	0h	**hostctrl2_samplingclkselect (hostctrl2_samplingclkselect):** This bit is set by tuning procedure when Execute Tuning is cleared.
6	0h	**hostctrl2_executetuning (hostctrl2_executetuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed.
5:4	0h	**hostctrl2_driverstrength (hostctrl2_driverstrength):** Host Controller output driver in 1.8V signaling is selected by this bit.
3	0h	**hostctrl2_1p8vsignallingena (hostctrl2_1p8vsignallingena):** This bit controls voltage regulator for I/O cell.
2:0	0h	**hostctrl2_uhsmodeselect (hostctrl2_uhsmodeselect):** This field is used to select one of UHS-I modes and effective when 1.8V Signaling Enable is set to 1.

20.7.30 Capabilities Register (capabilities)—Offset 40h

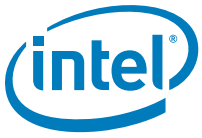
This register provides the host driver with information specific to the host controller implementation

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h	**corecfg_hs400support (corecfg_hs400support):** This field indicates whether HS400 is supported or not.
62:58	0h RO	Reserved.
57	0h	**corecfg_spiblkmode (corecfg_spiblkmode):** This field indicates whether SPI Block Mode is supported or not.
56	0h	**corecfg_spisupport (corecfg_spisupport):** This field indicates whether SPI Mode is supported or not.
55:48	0h	**corecfg_clockmultiplier (corecfg_clockmultiplier):** This field indicates clock multiplier value of programmable clock generator.
47:46	0h	**corecfg_retuningmodes (corecfg_retuningmodes):** This field defines the re-tuning capability of a Host Controller.
45	0h	**corecfg_tuningforsdr50 (corecfg_tuningforsdr50):** If this bit is set to 1, this Host Controller requires tuning to operate SDR50.
44	0h RO	Reserved.



Bit Range	Default & Access	Field Name (ID): Description
43:40	0h	**corecfg_retuningtimercnt (corecfg_retuningtimercnt):** This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3.
39	0h	**corecfg_type4support (corecfg_type4support):** This bit indicates support of Type 4 Driver.
38	0h	**corecfg_ddriversupport (corecfg_ddriversupport):** This bit indicates support of Driver Type D for 1.8 Signaling.
37	0h	**corecfg_cdriversupport (corecfg_cdriversupport):** This bit indicates support of Driver Type C for 1.8 Signaling.
36	0h	**corecfg_adriversupport (corecfg_adriversupport):** This bit indicates support of Driver Type A for 1.8 Signaling.
35	0h RO	Reserved.
34	0h	**corecfg_ddr50support (corecfg_ddr50support):** This bit indicates whether DDR50 is supported.
33	0h	**corecfg_sdr104support (corecfg_sdr104support):** This bit indicates whether SDR104 is supported.SDR104 requires tuning.
32	0h	**corecfg_sdr50support (corecfg_sdr50support):** This bit indicates whether SDR50 is supported.
31:30	0h	**corecfg_slottype (corecfg_slottype):** This field indicates usage of a slot by a specific Host System
29	0h	**corecfg_asynchintrsupport (corecfg_asynchintrsupport):** Asynchronous Interrupt Support
28	0h	**corecfg_64bitsupport (corecfg_64bitsupport):** This bit indicates whether the HC supports 64bit System Bus
27	0h RO	Reserved.
26	0h	**corecfg_1p8voltsupport (corecfg_1p8voltsupport):** This bit indicates whether the HC supports 1.8V.
25	0h	**corecfg_3p0voltsupport (corecfg_3p0voltsupport):** This bit indicates whether the HC supports 3.0V.
24	0h	**corecfg_3p3voltsupport (corecfg_3p3voltsupport):** This bit indicates whether the HC supports 3.3V.
23	0h	**corecfg_suspressupport (corecfg_suspressupport):** This bit indicates whether the HC supports Suspend/Resume functionality.
22	0h	**corecfg_sdmasupport (corecfg_sdmasupport):** This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly.
21	0h	**corecfg_highspeedsupport (corecfg_highspeedsupport):** This bit indicates whether the HC and the Host System support High Speed mode.
20	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
19	0h	**corecfg_adma2support (corecfg_adma2support):** '0'ADMA2 Not Supported
18	0h	**corecfg_8bitsupport (corecfg_8bitsupport):** This bit indicates whether the Host Controller is capable of using 8-bit bus width mode.
17:16	0h	**corecfg_maxblklength (corecfg_maxblklength):** This value indicates the maximum block size that the HD can read and write to the buffer in the HC.
15:8	0h	**corecfg_baseclkfreq (corecfg_baseclkfreq):** 6-bit Base Clock Frequency
7	0h	**corecfg_timeoutclkunit (corecfg_timeoutclkunit):** This bit shows the unit of base clock frequency used to detect Data Timeout Error.
6	0h RO	Reserved.
5:0	0h	**corecfg_timeoutclkfreq (corecfg_timeoutclkfreq):** This bit shows the base clock frequency used to detect Data Timeout Error.

20.7.31 Maximum Current Capabilities Register (maxcurrentcap)—Offset 48h

This register indicates maximum current capability for each voltage

Access Method

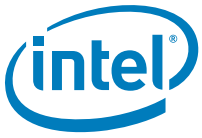
Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:24	0h RO	Reserved.
23:16	0h	**corecfg_maxcurrent1p8v (corecfg_maxcurrent1p8v):** Maximum Current for 1.8V
15:8	0h	**corecfg_maxcurrent3p0v (corecfg_maxcurrent3p0v):** Maximum Current for 3.0V
7:0	0h	**corecfg_maxcurrent3p3v (corecfg_maxcurrent3p3v):** Maximum Current for 3.3V

20.7.32 Force Event REGISTER for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus)—Offset 50h

This register is not physically implemented, rather it is an address where Auto CMD Error Status register can be written.



Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h	**forcecmdnotissuedbyautocmd12err (forcecmdnotissuedbyautocmd12err):** Force Event for Command Not Issued by AUTO CMD12 Error
6:5	0h RO	Reserved.
4	0h	**forceautocmdindexerr (forceautocmdindexerr):** Force Event for AUTO CMD Index Error
3	0h	**forceautocmdendbiterr (forceautocmdendbiterr):** Force Event for AUTO CMD End Bit Error
2	0h	**forceautocmdcrcerr (forceautocmdcrcerr):** Force Event for AUTO CMD Timeout Error
1	0h	**forceautocmdtimeouterr (forceautocmdtimeouterr):** Force Event for AUTO CMD Timeout Error
0	0h	**forceautocmdnotexec (forceautocmdnotexec):** Force Event for AUTO CMD12 Not Executed

20.7.33 Force Event Register for Error Interrupt Status (forceeventforerrintsts)—Offset 52h

This register is not physically implemented, rather it is an address where Error Interrupt Status register can be written.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h	**forcetuningerr (forcetuningerr):** Force Event for Tuning Error
9	0h	**forceadmaerr (forceadmaerr):** Force Event for ADMA Error'0' no interrupt, '1' interrupt generated

Bit Range	Default & Access	Field Name (ID): Description
8	0h	**forceautocmderr (forceautocmderr):** Force Event for Auto CMD Error '0' no interrupt, '1' interrupt generated
7	0h	**forcecurrlimerr (forcecurrlimerr):** Force Event for Current Limit Error '0' no interrupt, '1' interrupt generated
6	0h	**forcedatendbiterr (forcedatendbiterr):** Force Event for Data End Bit Error. '0' no interrupt, '1' interrupt generated
5	0h	**forcedatcrcerr (forcedatcrcerr):** Force Event for Data CRC Error
4	0h	**forcedattimeouterr (forcedattimeouterr):** Force Event for Data Timeout Error '0' no interrupt, '1' interrupt generated
3	0h	**forcecmdindexerr (forcecmdindexerr):** Force Event for Command Index Error
2	0h	**forcecmdendbiterr (forcecmdendbiterr):** Force Event for Command End Bit Error '0' no interrupt, '1' interrupt generated
1	0h	**forcecmdcrcerr (forcecmdcrcerr):** Force Event for Command CRC Error
0	0h	**forcecmdtimeouterr (forcecmdtimeouterr):** Force Event for CMD Timeout Error '0' No interrupt, '1' interrupt generated

20.7.34 ADMA Error Status Register (admaerrsts)—Offset 54h

When the ADMA Error interrupt occur, this register holds the ADMA State in ADMA Error States field and ADMA System Address holds address around the error descriptor

Access Method

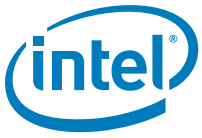
Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h	**admaerrsts_admalenmismatcherr (admaerrsts_admalenmismatcherr):** ADMA Length Mismatch Error
1:0	0h	**admaerrsts_admaerrorstate (admaerrsts_admaerrorstate):** This field indicates the state of ADMA when error is occurred during ADMA data transfer.

20.7.35 ADMA System Address Register0&1 (admasysaddr01)—Offset 58h

This register contains the physical address used for ADMA data transfer



Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**adma_sysaddress0 (adma_sysaddress0):** This register holds byte address of executing command of the Descriptor table.

20.7.36 ADMA System Address Register1 (admasysaddr2)—Offset 5Ch

This register contains the physical address used for ADMA data transfer

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**adma_sysaddress2 (adma_sysaddress2):** This register holds byte address of executing command of the Descriptor table.

20.7.37 ADMA System Address Register1 (admasysaddr3)—Offset 5Eh

This register contains the physical address used for ADMA data transfer

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**adma_sysaddress3 (adma_sysaddress3):** This register holds byte address of executing command of the Descriptor table.

20.7.38 Boot Timeout Control Register (boottimeoutcnt)—Offset 70h

This is used to program the boot timeout value counter

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**boot_timeoutcnt (boot_timeoutcnt):** This value determines the interval by which DAT line time-outs are detected during boot operation for eMMC4.4 card.

20.7.39 Slot Interrupt Status Register (slotintrsts)—Offset FCh

This register is used to read the interrupt signal for each slot.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h	**sdhchostif_slotintrsts (sdhchostif_slotintrsts):** These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot.

20.7.40 Host Controller Version Register (hostcontrollerver)—Offset FEh

This register is used to read the vendor version number and specification version number

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 1002h

Bit Range	Default & Access	Field Name (ID): Description
15:8	10h	**SDHC_VENVERNUM (SDHC_VENVERNUM):** This status is reserved for the vendor version number.

Bit Range	Default & Access	Field Name (ID): Description
7:0	2h	**SpecificationVersionNumber (SpecificationVersionNumber):** This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version.

20.8 Registers Summary

Table 20-8. Summary of soc_regs_wrapper Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	(DEVVENDID)—Offset 0h	8086h
4h	7h	(STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	(REVCLASSCODE)—Offset 8h	8050100h
Ch	Fh	(CLLATHEADERBIST)—Offset Ch	0h
10h	13h	(BAR)—Offset 10h	4h
14h	17h	(BAR_HIGH)—Offset 14h	0h
18h	1Bh	(BAR1)—Offset 18h	4h
1Ch	1Fh	(BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	(SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	(EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	(CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	(INTERRUPTREG)—Offset 3Ch	0h
80h	83h	(POWERCAPID)—Offset 80h	39001h
84h	87h	(PMECTRLSTATUS)—Offset 84h	8h
90h	93h	(PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	(DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	(D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	8041h
9Ch	9Fh	(DEVICE_IDLE_POINTER_REG)—Offset 9Ch	81C1h
A0h	A3h	(D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	290800h

20.8.1 (DEVVENDID)—Offset 0h

DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**DEVICEID**
15:0	8086h RO	**VENDORID**

20.8.2 (STATUSCOMMAND)—Offset 4h

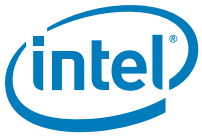
STATUSCOMMAND- Status and Command

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved0**
29	0h RW/1C	**RMA**
28	0h RW/1C	**RTA**
27:21	0h RO	**Reserved1**
20	1h RO	**CAPLIST**
19	0h RO	**INTR_STATUS**
18:16	0h RO	**Reserved2**
15:11	0h RO	**Reserved3**
10	0h RW	**INTR_DISABLE**
9	0h RO	**Reserved4**
8	0h RW	**SERR_ENABLE**
7:3	0h RO	**Reserved5**
2	0h RW	**BME**
1	0h RW	**MSE**
0	0h RO	**Reserved6**



20.8.3 (REVCLASSCODE)—Offset 8h

REVCLASSCODE - Revision ID and Class Code

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 8050100h

Bit Range	Default & Access	Field Name (ID): Description
31:8	80501h RO	**CLASS_CODES**
7:0	0h RO	**RID**

20.8.4 (CLLATHEADERBIST)—Offset Ch

CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved0**
23	0h RO	**MULFNDEV**
22:16	0h RO	**HEADERTYPE**
15:8	0h RO	**LATTIMER**
7:0	0h RW	**CACHELINE_SIZE**

20.8.5 (BAR)—Offset 10h

BAR -Base Address Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR**
11:4	0h RO	**SIZEINDICATOR**
3	0h RO	**PREFETCHABLE**
2:1	2h RO	**TYPE**
0	0h RO	**MESSAGE_SPACE**

20.8.6 (BAR_HIGH)—Offset 14h

BAR -Base Address Register High

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR_HIGH**

20.8.7 (BAR1)—Offset 18h

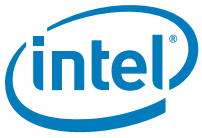
BAR1 -Base Address Register1

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR1**
11:4	0h RO	**SIZEINDICATOR1**
3	0h RO	**PREFETCHABLE1**
2:1	2h RO	**TYPE1**



Bit Range	Default & Access	Field Name (ID): Description
0	0h RO	**MESSAGE_SPACE1**

20.8.8 (BAR1_HIGH)—Offset 1Ch

BAR1 -Base Address Register1 High

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR1_HIGH**

20.8.9 (SUBSYSTEMID)—Offset 2Ch

SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID**
15:0	0h RW/O	**SUBSYSTEMVENDORID**

20.8.10 (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE**

20.8.11 (CAPABILITYPTR)—Offset 34h

CAPABILITYPTR - Capabilities Pointer

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved0**
7:0	80h RO	**CAPPTR_POWER**

20.8.12 (INTERRUPTREG)—Offset 3Ch

INTERRUPTREG - Interrupt Register

Access Method

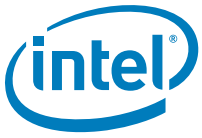
Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT**
23:16	0h RO	**MIN_GNT**
15:12	0h RO	**Reserved0**
11:8	0h RO	**INTPIN**
7:0	0h RW	**INTLINE**

20.8.13 (POWERCAPID)—Offset 80h

POWERCAPID - PowerManagement Capability ID



Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 39001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**PMESUPPORT**
26:19	0h RO	**Reserved0**
18:16	3h RO	**VERSION**
15:8	90h RO	**NXTCAP**
7:0	1h RO	**POWER_CAP**

20.8.14 (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved0**
15	0h RW/1C	**PMESTATUS**
14:9	0h RO	**Reserved1**
8	0h RW	**PMEENABLE**
7:4	0h RO	**Reserved2**
3	1h RO	**NO_SOFT_RESET**
2	0h RO	**Reserved3**
1:0	0h RW	**POWERSTATE**

20.8.15 (PCIDEVIDLE_CAP_RECORD)—Offset 90h

PCI DEVICE IDLE CAPABILITY RECORD

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP**
27:24	0h RO	**REVID**
23:16	14h RO	**CAP_LENGTH**
15:8	0h RO	**NEXT_CAP**
7:0	9h RO	**CAPID**

20.8.16 (DEVID_VEND_SPECIFIC_REG)—Offset 94h

DEVID VENDOR SPECIFIC REG

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH**
19:16	0h RO	**VSEC_REV**
15:0	10h RO	**VSECID**

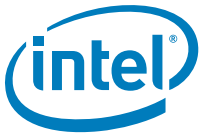
20.8.17 (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

SW LTR Update MMIO Location Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 8041h



Bit Range	Default & Access	Field Name (ID): Description
31:4	804h RO	**SW_LAT_DWORD_OFFSET**
3:1	0h RO	**SW_LAT_BAR_NUM**
0	1h RO	**SW_LAT_VALID**

20.8.18 (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 81C1h

Bit Range	Default & Access	Field Name (ID): Description
31:4	81Ch RO	**DWORD_OFFSET**
3:1	0h RO	**BAR_NUM**
0	1h RO	**VALID**

20.8.19 (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

DEVICE PG CONFIG

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 27 **Function:** 0

Default: 290800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved0**
21	1h RW	**HAE**
20	0h RO	**Reserved1**
19	1h RW	**SLEEP_EN**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**PGE**
17	0h RW	**I3_ENABLE**
16	1h RW	**PMCRE**
15:13	0h RO	**Reserved2**
12:10	2h RW/O	**POW_LAT_SCALE**
9:0	0h RW/O	**POW_LAT_VALUE**

20.9 Registers Summary

Table 20-9. Summary of SDHOST_OCP Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	SDMA System Address Register/Argument2 Register (sdmasysaddr)—Offset 0h	0h
4h	5h	BlockSize Register (blocksize)—Offset 4h	0h
6h	7h	BlockCount Register (blockcount)—Offset 6h	0h
8h	Bh	Argument1 Register (argument1)—Offset 8h	0h
Ch	Dh	TransferMode Register (transfermode)—Offset Ch	0h
Eh	Fh	Command Register (command)—Offset Eh	0h
10h	13h	Response Register (response01)—Offset 10h	0h
14h	15h	Response Register (response2)—Offset 14h	0h
16h	17h	Response Register (response3)—Offset 16h	0h
18h	19h	Response Register (response4)—Offset 18h	0h
1Ah	1Bh	Response Register (response5)—Offset 1Ah	0h
1Ch	1Dh	Response Register (response6)—Offset 1Ch	0h
1Eh	1Fh	Response Register (response7)—Offset 1Eh	0h
20h	23h	Buffer DataPort Register (dataport)—Offset 20h	0h
28h	28h	HostControl1 Register (hostcontrol1)—Offset 28h	0h
29h	29h	PowerControl Register (powercontrol)—Offset 29h	0h
2Ah	2Ah	BlockGapControl Register (blockgapcontrol)—Offset 2Ah	80h
2Bh	2Bh	Wakeup Control Register (wakeupcontrol)—Offset 2Bh	0h
2Ch	2Dh	Clock Control Register (clockcontrol)—Offset 2Ch	0h
2Eh	2Eh	Timeout Control Register (timeoutcontrol)—Offset 2Eh	0h
2Fh	2Fh	Software Reset Register (softwarereset)—Offset 2Fh	0h
30h	31h	Normal Interrupt Status Register (normalintrsts)—Offset 30h	0h
32h	33h	ErrorInterruptStatus_Register (errorintrsts)—Offset 32h	0h
34h	35h	Normal Interrupt Status Enable Register (normalintrstsena)—Offset 34h	0h

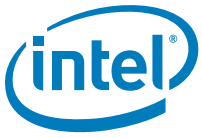


Table 20-9. Summary of SDHOST_OCP Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
36h	37h	Error Interrupt Status Enable Register (errorintrstsena)—Offset 36h	0h
38h	39h	Normal Interrupt Signal Enable Register (normalintrsigena)—Offset 38h	0h
3Ah	3Bh	Error Interrupt Signal Enable Register (errorintrsigena)—Offset 3Ah	0h
3Ch	3Dh	Auto CMD12 Error Status Register (autocmderrsts)—Offset 3Ch	0h
3Eh	3Fh	Host Control2 Register (hostcontrol2)—Offset 3Eh	0h
40h	47h	Capabilities Register (capabilities)—Offset 40h	0h
48h	4Fh	Maximum Current Capabilities Register (maxcurrentcap)—Offset 48h	0h
50h	51h	Force Event REGISTER for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus)—Offset 50h	0h
52h	53h	Force Event Register for Error Interrupt Status (forceeventforerrintsts)—Offset 52h	0h
54h	54h	ADMA Error Status Register (admaerrsts)—Offset 54h	0h
58h	5Bh	ADMA System Address Register0&1 (admasysaddr01)—Offset 58h	0h
5Ch	5Dh	ADMA System Address Register1 (admasysaddr2)—Offset 5Ch	0h
5Eh	5Fh	ADMA System Address Register1 (admasysaddr3)—Offset 5Eh	0h
70h	73h	Boot Timeout Control Register (boottimeoutcnt)—Offset 70h	0h
FCh	FDh	Slot Interrupt Status Register (slotintrsts)—Offset FCh	0h
FEh	FFh	Host Controller Version Register (hostcontrollerver)—Offset FEh	1002h

20.9.1 SDMA System Address Register/Argument2 Register (sdmasysaddr)—Offset 0h

This register contains concatinates reg_sdmasysaddrlo and reg_sdmasysaddrhi

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**sdma_sysaddress (sdma_sysaddress):** refer to reg_sdmasysaddrlo and reg_sdmasysaddrhi

20.9.2 BlockSize Register (blocksize)—Offset 4h

This register is used to configure the number of bytes in a data block

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14:12	0h	**sdma_bufboundary (sdma_bufboundary):** This Field specifies DMA Buffer Boundary
11:0	0h	**xfer_blocksize (xfer_blocksize):** This Field specifies Block Size for Data Transfers

20.9.3 BlockCount Register (blockcount)—Offset 6h

This register is used to configure the number of data blocks

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**xfer_blockcount (xfer_blockcount):** This Register specifies Block Size for Data Transfers

20.9.4 Argument1 Register (argument1)—Offset 8h

This register contains concatinates argument1lo and argument1hi registers to result SD Command Argument

Access Method

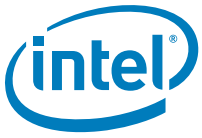
Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**command_argument1 (command_argument1):** refer t oreg_argument1lo and reg_argument1hi.

20.9.5 TransferMode Register (transfermode)—Offset Ch

This register is used to control the operations of data transfers



Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5	0h	**xfermode_multiblksel (xfermode_multiblksel):** This bit enables multiple block data transfers.
4	0h	**xfermode_dataxferdir (xfermode_dataxferdir):** This bit defines the direction of data transfers.
3:2	0h	**xfermode_autocmdena (xfermode_autocmdena):** This field determines use of auto command functions.
1	0h	**xfermode_blkcntena (xfermode_blkcntena):** This bit is used to enable the Block count register, which is only relevant for multiple block transfers
0	0h	**xfermode_dmaenable (xfermode_dmaenable):** '1' to enable DMA,

20.9.6 Command Register (command)—Offset Eh

This register is used to program the Command for host controller

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:8	0h	**command_cmdindex (command_cmdindex):** This bit shall be set to the command number (CMD0-63, ACMD0-63).
7:6	0h	**command_cmdtype (command_cmdtype):** This bit is used for select different command types.
5	0h	**command_datapresent (command_datapresent):** This bit is used to checking whether data present or not.
4	0h	**command_indexchkena (command_indexchkena):** This bit is used to enable/disable Command Index checking.
3	0h	**command_crcchkena (command_crcchkena):** This bit is used to enable/disable CRC checking.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	Reserved.
1:0	0h	**command_responsetype (command_responsetype):** Response Type Select.

20.9.7 Response Register (response01)—Offset 10h

This register is used to store responses from SD Cards (concatinates response0 & response1 registers)

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.9.8 Response Register (response2)—Offset 14h

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

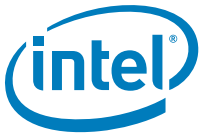
Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.9.9 Response Register (response3)—Offset 16h

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**



Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.9.10 Response Register (response4)—Offset 18h

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.9.11 Response Register (response5)—Offset 1Ah

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.9.12 Response Register (response6)—Offset 1Ch

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.9.13 Response Register (response7)—Offset 1Eh

This register is used to store responses from SD Cards

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

20.9.14 Buffer DataPort Register (dataport)—Offset 20h

This register is used to access internal buffer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

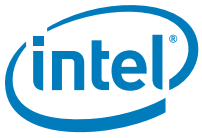
Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**sdhcdmactrl_piobufrddata (sdhcdmactrl_piobufrddata):** The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

20.9.15 HostControl1 Register (hostcontrol1)—Offset 28h

This register is used to program DMA modes, LED Control, Data Transfer Width, High Speed Enable, Card detect test level and signal selection

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**



Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h	**hostctrl1_cdsigselect (hostctrl1_cdsigselect):** This bit selects source for card detection.
6	0h	**hostctrl1_cdtestlevel (hostctrl1_cdtestlevel):** This bit is used for indicating whether card is inserted or not.
5	0h	**hostctrl1_extdatawidth (hostctrl1_extdatawidth):** This bit controls 8-bit bus width mode for embedded device.
4:3	0h	**hostctrl1_dmaselect (hostctrl1_dmaselect):** One of supported DMA modes can be selected.
2	0h	**hostctrl1_highspeedena (hostctrl1_highspeedena):** This bit is used for setting speed mode.
1	0h	**hostctrl1_datawidth (hostctrl1_datawidth):** This bit selects the data width of the HC.
0	0h	**hostctrl1_ledcontrol (hostctrl1_ledcontrol):** This bit is used to caution the user not to remove the card while the SD card is being accessed.

20.9.16 PowerControl Register (powercontrol)—Offset 29h

This register is used to program the SD Bus power and voltage level

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h	**emmc_hwreset (emmc_hwreset):** Hardware reset signal is generated for eMMC card.
3:1	0h	**pwrctrl_sdbusvoltage (pwrctrl_sdbusvoltage):** By setting these bits, the HD selects the voltage level for the SD card.
0	0h	**pwrctrl_sdbuspower (pwrctrl_sdbuspower):** This bit is used detect whether power is on or off.

20.9.17 BlockGapControl Register (blockgapcontrol)—Offset 2Ah

This register is used to program the block gap request, read wait control and interrupt at block gap

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7	1h	**blkgapctrl_bootackena (blkgapctrl_bootackena):** To check for the boot acknowledge in boot operation.
6	0h	**blkgapctrl_altbootmode (blkgapctrl_altbootmode):** To start boot code access in alternative mode.
5	0h	**blkgapctrl_bootenable (blkgapctrl_bootenable):** To start boot code access. '0' To stop boot code access, '1' To start boot code access
4	0h	**blkgapctrl_spimode (blkgapctrl_spimode):** SPI mode enable bit. '0' SD Mode, '1' SPI Mode
3	0h	**blkgapctrl_interrupt (blkgapctrl_interrupt):** This bit is valid only in 4-bit mode of the SD card andselects a sample point in the interrupt cycle.
2	0h	**blkgapctrl_rdwaitctrl (blkgapctrl_rdwaitctrl):** The read wait function is optional for SD cards.
1	0h	**blkgapctrl_continue (blkgapctrl_continue):** This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request.
0	0h	**blkgapctrl_stopatblkgap (blkgapctrl_stopatblkgap):** This bit is used to stop executing a transaction at the next block gap for non- DMA,SDMA and ADMA transfers.

20.9.18 Wakeup Control Register (wakeupcontrol)—Offset 2Bh

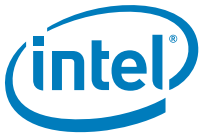
This register is used to program the wakeup functionality

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h	**wkupctrl_cardremoval (wkupctrl_cardremoval):** This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register.



Bit Range	Default & Access	Field Name (ID): Description
1	0h	**wkupctrl_cardinsertion (wkupctrl_cardinsertion):** This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register.
0	0h	**wkupctrl_cardinterrupt (wkupctrl_cardinterrupt):** This bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt Status register.

20.9.19 Clock Control Register (clockcontrol)—Offset 2Ch

This register is used to program the Clock frequency select, generator select, Clock enable, Internal Clock state fields

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h	**clkctrl_sdclkfreqsel (clkctrl_sdclkfreqsel):** This register is used to select the frequency of the SDCLK pin.
7:6	0h	**clkctrl_sdclkfreqsel_upperbits (clkctrl_sdclkfreqsel_upperbits):** Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select
5	0h	**clkctrl_clkgensel (clkctrl_clkgensel):** This bit is used to select the clock generator mode in SDCLK Frequency Select.
4:3	0h RO	Reserved.
2	0h	**clkctrl_sdclkena (clkctrl_sdclkena):** This bit enables/disables SD Clock. '0' Disable, '1' Enable
1	0h	**sdhcclkgen_intclkstable_dsync (sdhcclkgen_intclkstable_dsync):** This bit is set to 1 when SD clock is stable after writing to Internal Clock Enable in this register to 1.
0	0h	**clkctrl_intclkena (clkctrl_intclkena):** This bit enables setting of internal clock.'0' Stop, '1' Oscillate

20.9.20 Timeout Control Register (timeoutcontrol)—Offset 2Eh

The register sets the Data Timeout counter value

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3:0	0h	**timeout_ctrvalue (timeout_ctrvalue):** This value determines the interval by which DAT line time-outs are detected.

20.9.21 Software Reset Register (softwarereset)—Offset 2Fh

This register is used to program the software reset for data, command and for all.

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h	**swreset_for_dat (swreset_for_dat):** Only part of data circuit is reset. '0' Work, '1' Reset
1	0h	**swreset_for_cmd (swreset_for_cmd):** Only part of command circuit is reset.'0' Work, '1' reset.
0	0h	**swreset_for_all (swreset_for_all):** If this bit is set to 1, the SD card shall reset itself and must be re initialized by the HD.

20.9.22 Normal Interrupt Status Register (normalintrsts)—Offset 30h

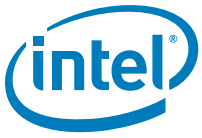
This register gives the status of all the interrupts

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h	**reg_errorintrsts (reg_errorintrsts):** This bit is set If any of the bits in the Error Interrupt Status Register are set.



Bit Range	Default & Access	Field Name (ID): Description
14	0h	**normalintrsts_bootcomplete (normalintrsts_bootcomplete):** This status is set if the boot operation gets terminated.
13	0h	**normalintrsts_rcvbootack (normalintrsts_rcvbootack):** This status is set if the boot acknowledge is received from device.
12	0h	**normalintrsts_retuningevent (normalintrsts_retuningevent):** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1.
11	0h	**normalintrsts_intc (normalintrsts_intc):** This status is set if INT_C is enabled and INT_C# pin is in low level. It is cleared by resetting the INT_C interrupt factor.
10	0h	**normalintrsts_intb (normalintrsts_intb):** This status is set if INT_B is enabled and INT_B# pin is in low level. It is cleared by resetting
9	0h	**normalintrsts_inta (normalintrsts_inta):** This status is set if INT_A is enabled and INT_A# pin is in low level. It is cleared by resetting
8	0h	**normalintrsts_cardintsts (normalintrsts_cardintsts):** This status is set to generate Card Interrupt. '0' No Card Interrupt, '1' Generate Card Interrupt
7	0h	**normalintrsts_cardremsts (normalintrsts_cardremsts):** This status is set if the Card Inserted in the Present State register changes from 1 to 0.
6	0h	**normalintrsts_cardinssts (normalintrsts_cardinssts):** This status is set if the Card Inserted in the Present State register changes from 0 to 1.
5	0h	**normalintrsts_bufrdready (normalintrsts_bufrdready):** This status is set if the Buffer Read Enable changes from 0 to 1.
4	0h	**normalintrsts_bufwrready (normalintrsts_bufwrready):** This status is set if the Buffer Write Enable changes from 0 to 1.
3	0h	**normalintrsts_dmainterrupt (normalintrsts_dmainterrupt):** This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size regiser.
2	0h	**normalintrsts_blkgapevent (normalintrsts_blkgapevent):** If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set.
1	0h	**normalintrsts_xfercomplete (normalintrsts_xfercomplete):** This bit is set when a read / write transaction is completed.
0	0h	**normalintrsts_cmdcomplete (normalintrsts_cmdcomplete):** This bit is set when we get the end bit of the command response.

20.9.23 ErrorInterruptStatus_Register (errorintrsts)—Offset 32h

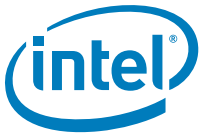
This register gives the status of the error interrupts

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h	**errorintrsts_hosterror (errorintrsts_hosterror):** Occurs when detecting Host ERROR
11:10	0h RO	Reserved.
9	0h	**errorintrsts_admaerror (errorintrsts_admaerror):** This bit is set when the Host Controller detects errors during ADMA based data transfer.
8	0h	**errorintrsts_autocmderror (errorintrsts_autocmderror):** This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1.
7	0h	**errorintrsts_currlimiterror (errorintrsts_currlimiterror):** If this bit is 1, it means that the HC is not supplying power to SD card due to some failure.Reading 0 means that the HC is supplying power and no error has occurred.
6	0h	**errorintrsts_dataendbiterror (errorintrsts_dataendbiterror):** Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status.
5	0h	**errorintrsts_datacrcerror (errorintrsts_datacrcerror):** Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 010.
4	0h	**errorintrsts_datatimeouterror (errorintrsts_datatimeouterror):** This status is set if Data Timeout error occurs.
3	0h	**errorintrsts_cmdindexerror (errorintrsts_cmdindexerror):** Occurs if a Command Index error occurs in the Command Response.
2	0h	**errorintrsts_cmdendbiterror (errorintrsts_cmdendbiterror):** Occurs when detecting that the end bit of a command response is 0.
1	0h	**errorintrsts_cmdcrcerror (errorintrsts_cmdcrcerror):** This bit is set when Command CRC Error is generated. '0' No Error, '1' CRC Error



Bit Range	Default & Access	Field Name (ID): Description
0	0h	**errorintrsts_cmdtimeouterror (errorintrsts_cmdtimeouterror):** This bit is set if no response is returned within 64 SDCLK cycles from the end bit of the command.

20.9.24 Normal Interrupt Status Enable Register (normalintrstsena)—Offset 34h

This register is used to enable the normal interrupt status register fields

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h	**normalintrsts_enableregbit15 (normalintrsts_enableregbit15):** The HC shall control error Interrupts using the Error Interrupt Status Enable register.
14	0h	**normalintrsts_enableregbit14 (normalintrsts_enableregbit14):** This status is set if the boot operation gets terminated.
13	0h	**normalintrsts_enableregbit13 (normalintrsts_enableregbit13):** This status is set if the boot acknowledge is received from device.
12	0h	**normalintrsts_enableregbit12 (normalintrsts_enableregbit12):** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1.
11	0h	**normalintrsts_enableregbit11 (normalintrsts_enableregbit11):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System.
10	0h	**normalintrsts_enableregbit10 (normalintrsts_enableregbit10):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System.
9	0h	**normalintrsts_enableregbit9 (normalintrsts_enableregbit9):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System.
8	0h	**sdhcregset_cardintstsena (sdhcregset_cardintstsena):** If this bit is set to 0, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1.
7	0h	**sdhcregset_cardremstsena (sdhcregset_cardremstsena):** This status is set if the Card Inserted in the Present State register changes from 1 to 0.

Bit Range	Default & Access	Field Name (ID): Description
6	0h	**sdhcregset_cardinsstsena (sdhcregset_cardinsstsena):** This status is set if the Card Inserted in the Present State register changes from 0 to 1.
5	0h	**normalintrsts_enableregbit5 (normalintrsts_enableregbit5):** This status is set if the Buffer Read Enable changes from 0 to 1.
4	0h	**normalintrsts_enableregbit4 (normalintrsts_enableregbit4):** This status is set if the Buffer Write Enable changes from 0 to 1.
3	0h	**normalintrsts_enableregbit3 (normalintrsts_enableregbit3):** This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size regiser.
2	0h	**normalintrsts_enableregbit2 (normalintrsts_enableregbit2):** If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set.
1	0h	**normalintrsts_enableregbit1 (normalintrsts_enableregbit1):** This bit is set when a read / write transaction is completed.
0	0h	**normalintrsts_enableregbit0 (normalintrsts_enableregbit0):** This bit is set when we get the end bit of the command response.

20.9.25 Error Interrupt Status Enable Register (errorintrstsena)—Offset 36h

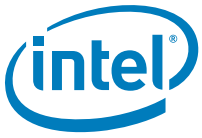
This register is used to enable the Error Interrupt Status register fields

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h	**errorintrsts_enableregbit12 (errorintrsts_enableregbit12):** Occurs when detecting ERROR in m_hresp(dma transaction)
11	0h RO	Reserved.
10	0h	**errorintrsts_enableregbit10 (errorintrsts_enableregbit10):** This status is set if INT_B is enabled and INT_B# pin is in low level. It is cleared by resetting



Bit Range	Default & Access	Field Name (ID): Description
9	0h	**errorintrsts_enableregbit9 (errorintrsts_enableregbit9):** This bit is set when the Host Controller detects errors during ADMA based data transfer.
8	0h	**errorintrsts_enableregbit8 (errorintrsts_enableregbit8):** This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1.
7	0h	**errorintrsts_enableregbit7 (errorintrsts_enableregbit7):** If this bit is 1, it means that the HC is not supplying power to SD card due to some failure.Reading 0 means that the HC is supplying power and no error has occurred.
6	0h	**errorintrsts_enableregbit6 (errorintrsts_enableregbit6):** Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status.
5	0h	**errorintrsts_enableregbit5 (errorintrsts_enableregbit5):** Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 010.
4	0h	**errorintrsts_enableregbit4 (errorintrsts_enableregbit4):** This status is set if Data Timeout error occurs.
3	0h	**errorintrsts_enableregbit3 (errorintrsts_enableregbit3):** Occurs if a Command Index error occurs in the Command Response.
2	0h	**errorintrsts_enableregbit2 (errorintrsts_enableregbit2):** Occurs when detecting that the end bit of a command response is 0.
1	0h	**errorintrsts_enableregbit1 (errorintrsts_enableregbit1):** This bit is set when Command CRC Error is generated.
0	0h	**errorintrsts_enableregbit0 (errorintrsts_enableregbit0):** This bit is set if no response is returned within 64 SDCLK cycles from the end bit of the command.

20.9.26 Normal Interrupt Signal Enable Register (normalintrsigena)—Offset 38h

This register is used to enable the Normal Interrupt Signal register

Access Method

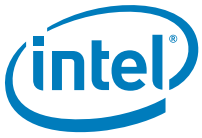
Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h	**normalintrsts_enableregbit15 (normalintrsts_enableregbit15):** The HD shall control error Interrupts using the Error Interrupt Signal Enable register.
14	0h	**normalintrsts_enableregbit14 (normalintrsts_enableregbit14):** Boot Terminate Interrupt Signal Enable
13	0h	**normalintrsts_enableregbit13 (normalintrsts_enableregbit13):** Boot ack rcv Signal Enable
12	0h	**normalintrsts_enableregbit12 (normalintrsts_enableregbit12):** Re-Tuning Event Signal Enable
11	0h	**normalintrsts_enableregbit11 (normalintrsts_enableregbit11):** INT_C Signal Enable
10	0h	**normalintrsts_enableregbit10 (normalintrsts_enableregbit10):** INT_B Signal Enable
9	0h	**normalintrsts_enableregbit9 (normalintrsts_enableregbit9):** INT_A Signal Enable
8	0h	**sdhcregset_cardintstsena (sdhcregset_cardintstsena):** Card Interrupt Signal Enable
7	0h	**sdhcregset_cardremstsena (sdhcregset_cardremstsena):** Card Removal Signal Enable
6	0h	**sdhcregset_cardinsstsena (sdhcregset_cardinsstsena):** Card Insertion Signal Enable
5	0h	**normalintrsts_enableregbit5 (normalintrsts_enableregbit5):** Buffer Read Ready Signal Enable
4	0h	**normalintrsts_enableregbit4 (normalintrsts_enableregbit4):** Buffer Write Ready Signal Enable
3	0h	**normalintrsts_enableregbit3 (normalintrsts_enableregbit3):** DMA Interrupt Signal Enable
2	0h	**normalintrsts_enableregbit2 (normalintrsts_enableregbit2):** Block Gap Event Signal Enable
1	0h	**normalintrsts_enableregbit1 (normalintrsts_enableregbit1):** Transfer Complete Signal Enable
0	0h	**normalintrsts_enableregbit0 (normalintrsts_enableregbit0):** Command Complete Signal Enable

20.9.27 Error Interrupt Signal Enable Register (errorintrsigena)—Offset 3Ah

This register is used to enable Error Interrupt Signal register



Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h	**errorintrsig_enableregbit12 (errorintrsig_enableregbit12):** Target Response Error Signal Enable
11	0h RO	Reserved.
10	0h	**errorintrsig_enableregbit10 (errorintrsig_enableregbit10):** Tuning Error Signal Enable
9	0h	**errorintrsig_enableregbit9 (errorintrsig_enableregbit9):** ADMA Error Signal Enable
8	0h	**errorintrsig_enableregbit8 (errorintrsig_enableregbit8):** Auto CMD Error Signal Enable
7	0h	**errorintrsig_enableregbit7 (errorintrsig_enableregbit7):** Current Limit Error Signal Enable
6	0h	**errorintrsig_enableregbit6 (errorintrsig_enableregbit6):** Data End Bit Error Signal Enable
5	0h	**errorintrsig_enableregbit5 (errorintrsig_enableregbit5):** Data CRC Error Signal Enable
4	0h	**errorintrsig_enableregbit4 (errorintrsig_enableregbit4):** Data Timeout Error Signal Enable
3	0h	**errorintrsig_enableregbit3 (errorintrsig_enableregbit3):** Command Index Error Signal Enable
2	0h	**errorintrsig_enableregbit2 (errorintrsig_enableregbit2):** Command End Bit Error Signal Enable
1	0h	**errorintrsig_enableregbit1 (errorintrsig_enableregbit1):** Command CRC Error Signal Enable
0	0h	**errorintrsig_enableregbit0 (errorintrsig_enableregbit0):** Command Timeout Error Signal Enable

20.9.28 Auto CMD12 Error Status Register (autocmderrsts)—Offset 3Ch

This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD 23

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h	**autocmderrsts_nexterror (autocmderrsts_nexterror):** Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 error(D04- D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23
6:5	0h RO	Reserved.
4	0h	**autocmderrsts_indexerror (autocmderrsts_indexerror):** Occurs if the Command Index error occurs in response to a command.
3	0h	**autocmderrsts_endbiterror (autocmderrsts_endbiterror):** Occurs when detecting that the end bit of command response is 0.
2	0h	**autocmderrsts_crcerror (autocmderrsts_crcerror):** Occurs when detecting a CRC error in the command response.
1	0h	**autocmderrsts_timeouterror (autocmderrsts_timeouterror):** Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command.
0	0h	**autocmderrsts_notexecerror (autocmderrsts_notexecerror):** Setting this bit to 1 means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error.

20.9.29 Host Control2 Register (hostcontrol2)—Offset 3Eh

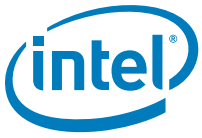
This register is used to program UHS Select Mode,UHS Select Mode,Driver Strength Select,Execute Tuning,Sampling Clock Select,Asynchronous Interrupt Enable and Preset value enable

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h	**hostctrl2_presetvalueenable (hostctrl2_presetvalueenable):** This bit enables the functions defined in the Preset Value registers.



Bit Range	Default & Access	Field Name (ID): Description
14	0h	**hostctrl2_asynchintrenable (hostctrl2_asynchintrenable):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register.
13:10	0h RO	Reserved.
9	0h	**hostctrl2_driverstrength_bit2 (hostctrl2_driverstrength_bit2):** This is the programmed Drive STrength output and Bit[2] of the sdhccore_drivestrength value.
8	0h RO	Reserved.
7	0h	**hostctrl2_samplingclkselect (hostctrl2_samplingclkselect):** This bit is set by tuning procedure when Execute Tuning is cleared.
6	0h	**hostctrl2_executetuning (hostctrl2_executetuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed.
5:4	0h	**hostctrl2_driverstrength (hostctrl2_driverstrength):** Host Controller output driver in 1.8V signaling is selected by this bit.
3	0h	**hostctrl2_1p8vsignallingena (hostctrl2_1p8vsignallingena):** This bit controls voltage regulator for I/O cell.
2:0	0h	**hostctrl2_uhsmodeselect (hostctrl2_uhsmodeselect):** This field is used to select one of UHS-I modes and effective when 1.8V Signaling Enable is set to 1.

20.9.30 Capabilities Register (capabilities)—Offset 40h

This register provides the host driver with information specific to the host controller implementation

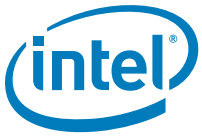
Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63	0h	**corecfg_hs400support (corecfg_hs400support):** This field indicates whether HS400 is supported or not.
62:58	0h RO	Reserved.
57	0h	**corecfg_spiblkmode (corecfg_spiblkmode):** This field indicates whether SPI Block Mode is supported or not.

Bit Range	Default & Access	Field Name (ID): Description
56	0h	**corecfg_spisupport (corecfg_spisupport):** This field indicates whether SPI Mode is supported or not.
55:48	0h	**corecfg_clockmultiplier (corecfg_clockmultiplier):** This field indicates clock multiplier value of programmable clock generator.
47:46	0h	**corecfg_retuningmodes (corecfg_retuningmodes):** This field defines the re-tuning capability of a Host Controller.
45	0h	**corecfg_tuningforsdr50 (corecfg_tuningforsdr50):** If this bit is set to 1, this Host Controller requires tuning to operate SDR50.
44	0h RO	Reserved.
43:40	0h	**corecfg_retuningtimercnt (corecfg_retuningtimercnt):** This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3.
39	0h	**corecfg_type4support (corecfg_type4support):** This bit indicates support of Type 4 Driver.
38	0h	**corecfg_ddriversupport (corecfg_ddriversupport):** This bit indicates support of Driver Type D for 1.8 Signaling.
37	0h	**corecfg_cdriversupport (corecfg_cdriversupport):** This bit indicates support of Driver Type C for 1.8 Signaling.
36	0h	**corecfg_adriversupport (corecfg_adriversupport):** This bit indicates support of Driver Type A for 1.8 Signaling.
35	0h RO	Reserved.
34	0h	**corecfg_ddr50support (corecfg_ddr50support):** This bit indicates whether DDR50 is supported.
33	0h	**corecfg_sdr104support (corecfg_sdr104support):** This bit indicates whether SDR104 is supported.SDR104 requires tuning.
32	0h	**corecfg_sdr50support (corecfg_sdr50support):** This bit indicates whether SDR50 is supported.
31:30	0h	**corecfg_slottype (corecfg_slottype):** This field indicates usage of a slot by a specific Host System
29	0h	**corecfg_asynchintrsupport (corecfg_asynchintrsupport):** Asynchronous Interrupt Support
28	0h	**corecfg_64bitsupport (corecfg_64bitsupport):** This bit indicates whether the HC supports 64bit System Bus
27	0h RO	Reserved.
26	0h	**corecfg_1p8voltsupport (corecfg_1p8voltsupport):** This bit indicates whether the HC supports 1.8V.
25	0h	**corecfg_3p0voltsupport (corecfg_3p0voltsupport):** This bit indicates whether the HC supports 3.0V.
24	0h	**corecfg_3p3voltsupport (corecfg_3p3voltsupport):** This bit indicates whether the HC supports 3.3V.



Bit Range	Default & Access	Field Name (ID): Description
23	0h	**corecfg_suspressupport (corecfg_suspressupport):** This bit indicates whether the HC supports Suspend/Resume functionality.
22	0h	**corecfg_sdmasupport (corecfg_sdmasupport):** This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly.
21	0h	**corecfg_highspeedsupport (corecfg_highspeedsupport):** This bit indicates whether the HC and the Host System support High Speed mode.
20	0h RO	Reserved.
19	0h	**corecfg_adma2support (corecfg_adma2support):** '0'ADMA2 Not Supported
18	0h	**corecfg_8bitsupport (corecfg_8bitsupport):** This bit indicates whether the Host Controller is capable of using 8-bit bus width mode.
17:16	0h	**corecfg_maxblklength (corecfg_maxblklength):** This value indicates the maximum block size that the HD can read and write to the buffer in the HC.
15:8	0h	**corecfg_baseclkfreq (corecfg_baseclkfreq):** 6-bit Base Clock Frequency
7	0h	**corecfg_timeoutclkunit (corecfg_timeoutclkunit):** This bit shows the unit of base clock frequency used to detect Data Timeout Error.
6	0h RO	Reserved.
5:0	0h	**corecfg_timeoutclkfreq (corecfg_timeoutclkfreq):** This bit shows the base clock frequency used to detect Data Timeout Error.

20.9.31 Maximum Current Capabilities Register (maxcurrentcap)—Offset 48h

This register indicates maximum current capability for each voltage

Access Method

Type: MEM Register (Size: 64 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
63:24	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h	**corecfg_maxcurrent1p8v (corecfg_maxcurrent1p8v):** Maximum Current for 1.8V
15:8	0h	**corecfg_maxcurrent3p0v (corecfg_maxcurrent3p0v):** Maximum Current for 3.0V
7:0	0h	**corecfg_maxcurrent3p3v (corecfg_maxcurrent3p3v):** Maximum Current for 3.3V

20.9.32 Force Event REGISTER for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus)—Offset 50h

This register is not physically implemented, rather it is an address where Auto CMD Error Status register can be written.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

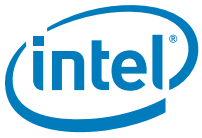
Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h	**forcecmdnotissuedbyautocmd12err (forcecmdnotissuedbyautocmd12err):** Force Event for Command Not Issued by AUTO CMD12 Error
6:5	0h RO	Reserved.
4	0h	**forceautocmdindexerr (forceautocmdindexerr):** Force Event for AUTO CMD Index Error
3	0h	**forceautocmdendbiterr (forceautocmdendbiterr):** Force Event for AUTO CMD End Bit Error
2	0h	**forceautocmdcrcerr (forceautocmdcrcerr):** Force Event for AUTO CMD Timeout Error
1	0h	**forceautocmdtimeouterr (forceautocmdtimeouterr):** Force Event for AUTO CMD Timeout Error
0	0h	**forceautocmdnotexec (forceautocmdnotexec):** Force Event for AUTO CMD12 Not Executed

20.9.33 Force Event Register for Error Interrupt Status (forceeventforerrintsts)—Offset 52h

This register is not physically implemented, rather it is an address where Error Interrupt Status register can be written.

Access Method



Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h	**forcetuningerr (forcetuningerr):** Force Event for Tuning Error
9	0h	**forceadmaerr (forceadmaerr):** Force Event for ADMA Error'0' no interrupt, '1' interrupt generated
8	0h	**forceautocmderr (forceautocmderr):** Force Event for Auto CMD Error '0' no interrupt, '1' interrupt generated
7	0h	**forcecurrlimerr (forcecurrlimerr):** Force Event for Current Limit Error '0' no interrupt, '1' interrupt generated
6	0h	**forcedatendbiterr (forcedatendbiterr):** Force Event for Data End Bit Error. '0' no interrupt, '1' interrupt generated
5	0h	**forcedatcrcerr (forcedatcrcerr):** Force Event for Data CRC Error
4	0h	**forcedattimeouterr (forcedattimeouterr):** Force Event for Data Timeout Error '0' no interrupt, '1' interrupt generated
3	0h	**forcecmdindexerr (forcecmdindexerr):** Force Event for Command Index Error
2	0h	**forcecmdendbiterr (forcecmdendbiterr):** Force Event for Command End Bit Error '0' no interrupt, '1' interrupt generated
1	0h	**forcecmdcrcerr (forcecmdcrcerr):** Force Event for Command CRC Error
0	0h	**forcecmdtimeouterr (forcecmdtimeouterr):** Force Event for CMD Timeout Error '0' No interrupt, '1' interrupt generated

20.9.34 ADMA Error Status Register (admaerrsts)—Offset 54h

When the ADMA Error interrupt occur, this register holds the ADMA State in ADMA Error States field and ADMA System Address holds address around the error descriptor

Access Method

Type: MEM Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h	**admaerrsts_admalenmismatcherr (admaerrsts_admalenmismatcherr):** ADMA Length Mismatch Error
1:0	0h	**admaerrsts_admaerrorstate (admaerrsts_admaerrorstate):** This field indicates the state of ADMA when error is occurred during ADMA data transfer.

20.9.35 ADMA System Address Register0&1 (admasysaddr01)—Offset 58h

This register contains the physical address used for ADMA data transfer

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**adma_sysaddress0 (adma_sysaddress0):** This register holds byte address of executing command of the Descriptor table.

20.9.36 ADMA System Address Register1 (admasysaddr2)—Offset 5Ch

This register contains the physical address used for ADMA data transfer

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**adma_sysaddress2 (adma_sysaddress2):** This register holds byte address of executing command of the Descriptor table.

20.9.37 ADMA System Address Register1 (admasysaddr3)—Offset 5Eh

This register contains the physical address used for ADMA data transfer

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**adma_sysaddress3 (adma_sysaddress3):** This register holds byte address of executing command of the Descriptor table.

20.9.38 Boot Timeout Control Register (boottimeoutcnt)—Offset 70h

This is used to program the boot timeout value counter

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**boot_timeoutcnt (boot_timeoutcnt):** This value determines the interval by which DAT line time-outs are detected during boot operation for eMMC4.4 card.

20.9.39 Slot Interrupt Status Register (slotintrsts)—Offset FCh

This register is used to read the interrupt signal for each slot.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h	**sdhchostif_slotintrsts (sdhchostif_slotintrsts):** These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot.

20.9.40 Host Controller Version Register (hostcontrollerver)—Offset FEh

This register is used to read the vendor version number and specification version number

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** **Function:**

Default: 1002h

Bit Range	Default & Access	Field Name (ID): Description
15:8	10h	**SDHC_VENVERNUM (SDHC_VENVERNUM):** This status is reserved for the vendor version number.
7:0	2h	**SpecificationVersionNumber(SpecificationVersionNumber) :** This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version.

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